1996-1997

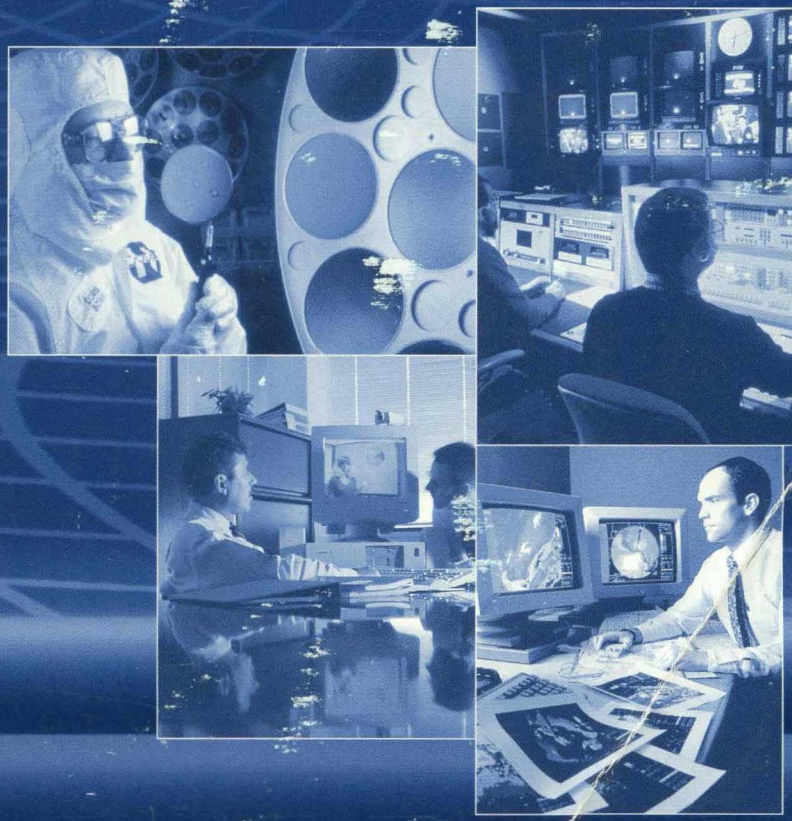
LINEAR ICs FOR ANALOG SIGNAL PROCESSING APPLICATIONS

HARRIS

DB
500.3

Op Amps, Comparators, S/H, Video Switches,
Transistor Arrays, and Special Analog Circuits

LINEAR ICs
FOR ANALOG SIGNAL PROCESSING APPLICATIONS
1996 - 1997



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HARRIS LINEAR PRODUCTS

Harris Semiconductor is a pioneer in developing and producing advanced Linear products for the most demanding Commercial, Industrial and Automotive applications worldwide. Harris offers an extensive line of Linear components including: High Speed and General Purpose Op Amps, Comparators, Sample/Hold Amps, Video Crosspoint Switches, Special Analog Circuits and Transistor Arrays.

This data book fully describes Harris Semiconductor's Linear ICs. It includes a complete set of data sheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris Quality and Reliability program. Section 12, Harris' On-Line Services, describes how our customers have access to the most recent technical updates.

It is our intention to provide you with the most up-to-date information on Linear Products. For complete, current and detailed technical specifications on any Harris devices, please contact the nearest Harris sales, representative or distributor office, listed in Section 13; or direct literature requests to:

Harris Semiconductor Data Services Department
P.O. Box 883, MS 53-204
Melbourne, FL 32902
Phone: 1-800-442-7747
Fax: 407-724-7240

For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG201; ordering information above).

See Section 12 for Harris' On-Line Services

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HARRIS SEMICONDUCTOR

LINEAR INTEGRATED CIRCUITS

FOR COMMERCIAL AND INDUSTRIAL APPLICATIONS

*A Product Selection Guide is located at the beginning of the section.

LINEAR 1

NEW PRODUCTS

VIDEO OP AMPS AND BUFFERS

HFA1109
LOW POWER, WIDEBAND, VIDEO OP AMP

AnswerFAX DOCUMENT # 4019

- Wide -3dB Bandwidth 550MHz
- High Slew Rate 1200V/µs
- Gain Flatness to 250MHz . . . . . ±0.5dB
- Fast Settling Time (0.1%). 17ns
- Differential Gain/Phase . . . . . 0.02%/0.02 Degrees
- Low Supply Current 10mA
- 8 Lead PDIP and SOIC

HFA1105
LOW POWER VIDEO OP AMP

AnswerFAX DOCUMENT # 3395

- -3dB Bandwidth (A_V = +2) 330MHz
- High Slew Rate 1000V/µs
- Gain Flatness to 75MHz. . . . . ±0.1dB
- Fast Settling Time (0.1%). 15ns
- Differential Gain/Phase . . . . . 0.02%/0.03 Degrees
- Low Supply Current 6mA
- 8 Lead PDIP and SOIC

HFA1106
VIDEO OP AMP WITH EXTERNAL COMPENSATION

AnswerFAX DOCUMENT # 3922

- -3dB Bandwidth 315MHz
- High Slew Rate 700V/µs
- Differential Gain/Phase. . . . . 0.02%/0.05 Degrees
- Low Supply Current 5.8mA
- Compensation Pin for Bandwidth Limiting
- 8 Lead PDIP and SOIC

HFA1149
LOW POWER, WIDEBAND OP AMP WITH OUTPUT DISABLE

AnswerFAX DOCUMENT # 4019

- Wide -3dB Bandwidth 550MHz
- High Slew Rate 1200V/µs
- Gain Flatness to 250MHz . . . . . ±0.5dB
- Differential Gain/Phase . . . . . 0.02%/0.02 Degrees
- Low Supply Current 10mA
- Fast Enable/Disable Times 18ns/11ns
- 8 Lead PDIP and SOIC

HFA1145
LOW POWER VIDEO OP AMP WITH DISABLE

AnswerFAX DOCUMENT # 3955

- -3dB Bandwidth. 330MHz
- High Slew Rate 1000V/µs
- Differential Gain/Phase . . . . . 0.02%/0.03 Degrees
- Gain Flatness to 75MHz. . . . . ±0.1dB
- Low Supply Current. 6mA
- Output Enable/Disable (T_{ON}/T_{OFF} = 180ns/35ns)
- 8 Lead PDIP and SOIC

HFA1113
PROG. GAIN VIDEO BUFFER WITH OUTPUT LIMITING

AnswerFAX DOCUMENT # 1342

- Wide -3dB Bandwidth 850MHz
- High Slew Rate 2400V/µs
- Differential Gain/Phase . . . . . 0.02%/0.04 Degrees
- User Programmable Gain of +2, ±1
- User Programmable Output Limiting
- 8 Lead PDIP and SOIC

HFA1114
CABLE DRIVING BUFFER WITH SUMMING NODE

AnswerFAX DOCUMENT # 3151

- Wide -3dB Bandwidth 850MHz
- High Slew Rate 2400V/µs
- Differential Gain/Phase . . . . . 0.02%/0.04 Degrees
- User Programmable Gain (+2, ±1)
- Summing Node Pinout Enables Tailoring of System Response For Cable Length
- 8 Lead PDIP and SOIC

HA4600
400MHz VIDEO BUFFER WITH OUTPUT DISABLE

AnswerFAX DOCUMENT # 3990

- Low Power Dissipation 105mW
- Symmetrical Slew Rates. 1700V/µs
- 0.1dB Gain Flatness 250MHz
- Off Isolation (100MHz) 85dB
- Differential Gain and Phase 0.01%/0.01Degrees
- High ESD Rating. . . . . >2000V
- 8 Lead PDIP and SOIC

HFA1135
VIDEO OP AMP WITH OUTPUT LIMITING

AnswerFAX DOCUMENT # 3653

- -3dB Bandwidth 360MHz
- High Slew Rate 1200V/µs
- Fast Settling Time (0.1%) 15ns
- Differential Gain/Phase . . . . . 0.02%/0.04 Degrees
- Low Supply Current 7mA
- User Programmable Output Limiting
- Fast Overdrive Recovery . . . . . <1ns
- 8 Lead PDIP and SOIC

HFA1115
LOW POWER PROGRAMMABLE GAIN VIDEO BUFFER

AnswerFAX DOCUMENT # 3606

- -3dB Bandwidth 225MHz
- High Slew Rate 1100V/µs
- Differential Gain/Phase . . . . . 0.02%/0.03 Degrees
- User Programmable Gain (+2, ±1)
- User Programmable Output Limiting
- Low Supply Current 7mA
- 8 Lead PDIP and SOIC

HFA1205
DUAL LOW POWER VIDEO OP AMP

AnswerFAX DOCUMENT # 3605

- -3dB Bandwidth (A_V = +2) 400MHz
- High Slew Rate 1275V/µs
- Differential Gain/Phase . . . . . 0.03%/0.03 Degrees
- Low Supply Current . . . . . 6mA/Op Amp
- Gain Flatness to 50MHz . . . . . ±0.03dB
- 8 Lead PDIP and SOIC

HFA1212
DUAL PROGRAMMABLE GAIN VIDEO BUFFER

AnswerFAX DOCUMENT # 3607

- -3dB Bandwidth (A_V = +2) 350MHz
- High Slew Rate 1100V/µs
- Differential Gain/Phase . . . . . 0.02%/0.02 Degrees
- User Programmable Gain (+2, ±1)
- Low Supply Current . . . . . 6mA/Op Amp
- 8 Lead PDIP and SOIC

HFA1245
DUAL LOW POWER VIDEO AMP WITH DISABLE

AnswerFAX DOCUMENT # 3682

- -3dB Bandwidth (A_V = +2) 530MHz
- High Slew Rate 1050V/µs
- Differential Gain/Phase . . . . . 0.02%/0.03 Degrees
- Gain Flatness to 50MHz . . . . . ±0.11dB
- Low Supply Current . . . . . 6mA/Op Amp
- Output Enable/Disable (T_{ON}/T_{OFF} = 160ns/20ns)
- 14 Lead PDIP and SOIC

HFA1405
QUAD LOW POWER VIDEO OP AMP

AnswerFAX DOCUMENT # 3604

- -3dB Bandwidth (A_V = +2) 560MHz
- High Slew Rate 1700V/µs
- Differential Gain/Phase . . . . . 0.02%/0.03 Degrees
- Gain Flatness to 50MHz . . . . . ±0.03dB
- Low Supply Current . . . . . 6mA/Op Amp
- 14 Lead SOIC and PDIP

HFA1412
QUAD PROGRAMMABLE GAIN VIDEO BUFFER

AnswerFAX DOCUMENT # 4152

- -3dB Bandwidth (A_V = +2) 350MHz
- High Slew Rate 1100V/µs
- Differential Gain/Phase . . . . . 0.02%/0.02 Degrees
- User Programmable Gain (+2, ±1)
- Low Supply Current . . . . . 6mA/Op Amp
- 14 Lead PDIP and SOIC

HA5023/HA5013/HA5025
DUAL/TRIPLE/QUAD VIDEO OP AMPS

AnswerFAX DOCUMENT # 3393/3654/3591

- -3dB Bandwidth 125MHz
- Slew Rate 475V/µs
- Differential Gain/Phase . . . . . 0.03%/0.03 Degrees
- High ESD Protection 4000V
- Low Supply Current . . . . . 7.5mA/Op Amp
- ±5V to ±15V Operation
- PDIP and SOIC

HA-5020/HA5022/HA5024
SINGLE/DUAL/QUAD VIDEO OP AMP WITH DISABLE

AnswerFAX DOCUMENT # 2845/3392/3550

- -3dB Bandwidth 125MHz
- Differential Gain/Phase. . . . . 0.03%/0.03 Degrees
- High ESD Protection 4000V
- Low Supply Current . . . . . 7.5mA/Op Amp
- ±5V to ±15V Operation
- Individual Output Disable/Enable
- PDIP and SOIC

SAMPLE/HOLD

HA5351
FAST ACQUISITION SAMPLE/HOLD

AnswerFAX DOCUMENT # 3690

- Fast Acquisition to 0.01% 70ns
- Low Offset Error 2mV
- Low Pedestal Error 10mV
- Low Droop Rate. 2μV/μs
- Wide Unity Gain Bandwidth. 40MHz
- Low THD (Hold Mode). . . . . -72dBc
- Low Power Dissipation. 220mW
- 8 Lead PDIP and SOIC

PIN DRIVER

HFA5251
ULTRA HIGH SPEED ATE PIN DRIVERS

AnswerFAX DOCUMENT # 3689

- High ECL Data Rate 800MHz
- $1V_{P-P}$ Rise/Fall Time 500ps
- Precise Output Impedance 50Ω
- Output Swing . . . . . -2V to +7V
- High Impedance Three-State Output Control
- Die Form Only

HFA5253
ULTRA HIGH SPEED ATE PIN DRIVER

AnswerFAX DOCUMENT # 4003

- High ECL Data Rate 800MHz
- $1V_{P-P}$ Rise/Fall Time 500ps
- Wide Output Swing . . . . . -3V to +8V
- Precise Output Impedance 50Ω
- HIZ Output Leakage 100nA
- Slew Rate Control
- 20 Lead Power SOIC and Die

WIRELESS COMMUNICATIONS

HFA3046, HFA3096, HFA3127, HFA3128
ULTRA HIGH FREQUENCY TRANSISTOR ARRAYS

AnswerFAX DOCUMENT # 3076

- NPN Transistor F_T 8GHz
- NPN Current Gain (h_{FE}) 70
- PNP Transistor F_T 5.5GHz
- PNP Current Gain (h_{FE}) 40
- 14 Lead SOIC (HFA3046)
- 16 Lead SOIC (HFA3096, HFA3127, HFA3128)

HFA3102
DUAL DIFFERENTIAL AMPLIFIER

AnswerFAX DOCUMENT # 3635

- High Gain Bandwidth Product 10GHz
- High Power Gain BW Product 5GHz
- High Current Gain (h_{FE}) 70
- Noise Figure (Transistor) 3.5dB
- Low Collector Leakage Current . . . . . <0.01nA
- Excellent h_{FE} and V_{BE} Matching
- Pin Compatible to UPA102G
- 14 Lead SOIC

HFA3101
GILBERT CELL TRANSISTOR ARRAY

AnswerFAX DOCUMENT # 3663

- NPN Transistor Array Configured as a Gilbert Cell
- High Gain Bandwidth Product 10GHz
- High Power Gain BW Product 5GHz
- Current Gain (h_{FE}) 70
- Low Collector Leakage Current . . . . . <0.01nA
- Pin Compatible to UPA101
- 8 Lead SOIC

HFA3600
LOW NOISE AMPLIFIER/MIXER

AnswerFAX DOCUMENT # 3655

- Low Noise Figure
  - LNA . . . . . 2.3dB at 900MHz
  - Mixer . . . . . 12.1dB at 900MHz
  - LNA + Mixer . . . . . 3.97dB at 900MHz
- High Power Gain
  - LNA . . . . . 12.8dB at 900MHz
  - Mixer . . . . . 7.0dB at 900MHz
  - LNA + Mixer . . . . . 19.8dB at 900MHz
- High Intercept
  - LNA . . . . . +12.8dBm at Output
  - Mixer . . . . . +3.2dBm at Output
  - LNA + Mixer . . . . . -16.7dBm at Input
- 14 Lead SOIC

VIDEO CROSSPOINT SWITCHES

HA4201
WIDEBAND CROSSPOINT SWITCH WITH TALLY OUTPUT

AnswerFAX DOCUMENT # 3680

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1700V/µs
- 0.1dB Gain Flatness 250MHz
- Off Isolation (100MHz) 85dB
- Differential Gain 0.01%
- Differential Phase . . . . . 0.01 Degrees
- 8 Lead PDIP and SOIC

HA4244
WIDEBAND CROSSPOINT SWITCH WITH LATCHED CONTROL SIGNAL

AnswerFAX DOCUMENT # 4078

- Synchronous Enable Control (Latched)
- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1700V/µs
- 0.1dB Gain Flatness 250MHz
- Off Isolation (100MHz) 85dB
- Differential Gain 0.01%
- Differential Phase . . . . . 0.01 Degrees
- 8 Lead SOIC

HA4314B
400MHz 4 x 1, VIDEO CROSSPOINT SWITCH

AnswerFAX DOCUMENT # 3679

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1400V/µs
- 0.1dB Gain Flatness 100MHz
- Differential Gain/Phase . . . . . 0.01%/0.01 Degrees
- Pin Compatible to GX4314/L
- 14 Lead PDIP and SOIC

HA4344B
400MHz 4 x 1, VIDEO CROSSPOINT SWITCH

AnswerFAX DOCUMENT # 3956

- Synchronous Controls (Latched)
- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1400V/µs
- 0.1dB Gain Flatness 165MHz
- Differential Gain/Phase . . . . . 0.01%/0.01 Degrees
- 16 Lead PDIP and SOIC

HA4404B
400MHz 4 x 1, VIDEO CROSSPOINT SWITCH

AnswerFAX DOCUMENT # 3678

- Open Collector Tally Outputs
- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1400V/µs
- 0.1dB Gain Flatness 165MHz
- Differential Gain/Phase . . . . . 0.01%/0.01 Degrees
- 16 Lead PDIP and SOIC

HA455
HIGH PERFORMANCE 8 x 8 VIDEO CROSSPOINT SWITCH

AnswerFAX DOCUMENT # 4244

- Fully Buffered Inputs and Outputs (A_V = +1)
- Wide -3dB Bandwidth 130MHz
- Slew Rate 250V/µs
- Differential Gain/Phase . . . . . 0.02%/0.02 Degrees
- Crosstalk (at 10MHz) . . . . . -60dB
- 44 Lead MQFP

HA456
80MHz, LOW POWER 8 x 8 VIDEO CROSSPOINT SWITCH

AnswerFAX DOCUMENT # 4153

- Fully Buffered Inputs and Outputs (A_V = +1)
- -3dB Bandwidth 80MHz
- Slew Rate 170V/µs
- Differential Gain/Phase . . . . . 0.04%/0.2 Degrees
- Crosstalk (at 10MHz) . . . . . -60dB
- 44 Lead PLCC and MQFP

HA457
WIDEBAND, A_V = 2, 8 x 8 VIDEO CROSSPOINT SWITCH

AnswerFAX DOCUMENT # 4231

- Fully Buffered Inputs and Outputs (A_V = +2)
- Wide -3dB Bandwidth 150MHz
- Slew Rate 350V/µs
- Differential Gain/Phase . . . . . 0.01%/0.02 Degrees
- Crosstalk (at 10MHz) . . . . . -60dB
- 44 Lead MQFP

LINEAR 2

TABLE OF CONTENTS AND GENERAL INFORMATION

Alpha Numeric Product Index

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Alpha Numeric Product Index (Continued)

Product Index by Family

Product Index by Family (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
3507J	HA2-2525-5	Yes	
3508J	HA2-2625-5	Yes	
3551J	HA2-5162-5	†	Reduced I_{BIAS}/greater Bandwidth
3551S	HA2-5160-2	†	Reduced I_{BIAS}/greater Bandwidth
AD389BD	HA1-5320-2	No	Faster Acquisition/Reduced Droop
AD389KD	HA1-5320-5	No	Faster Acquisition/Reduced Droop
AD507JH	HA2-2625-5	Yes	
AD507KH	HA2-2625-5	Yes	
AD507SH	HA2-2620-2	Yes	
AD509JH	HA2-2525-5	Yes	Substitute HA2-2529-5
AD509KH	HA2-2525-5	Yes	Substitute HA2-2529-5
AD509SH	HA2-2520-2	Yes	Substitute HA2-2529-2
AD518JH	HA2-2515-5	Yes	
AD518JN	HA3-2515-5	Yes	
AD518KH	HA2-2515-5	Yes	
AD518SH	HA2-2510-2	Yes	
AD539JD	HA1-2547-5	No	Enhanced Bandwidth
AD539KD	HA1-2547-5	No	Enhanced Bandwidth
AD539SD	HA1-2547-9	No	Enhanced Bandwidth
AD542JH	HA1-5170-5	†	Enhanced ACs
AD5539JN	HA3-2839-5	†	
AD5539JQ	HA1-2839-5	†	
AD5539SQ	HA1-2539-2	†	
AD582KD	HA1-2425-5	No	Faster Acquisition/Enhanced ACs
AD582SD	HA1-2420-2	No	Faster Acquisition/Enhanced ACs
AD583KD	HA1-2425-5	Yes	Faster Acquisition/Greater I_{OUT}
AD585AQ	HA1-5320-5	No	Faster Acquisition/Reduced Droop
AD585SQ	HA1-5320-2	No	Faster Acquisition/Reduced Droop
AD8001AN	HFA1105IP	Yes	
AD8001AR	HFA1105IB	Yes	
AD810AN	HA3-5020-9	Yes	Better AC Specifications
AD811AN	HA3-5020-9	Yes	Lower Power
AD811AR-8	HFA1105IB	Yes	Lower Power, Better AC Specs
AD811SQ/883	HA7-5020/883	Yes	Lower Power, Price
AD812AN	HA5023IP	Yes	Better AC and Video Specs
AD812AR	HA5023IB	Yes	Better Video Spec
AD812AR-8	HA5023IB	Yes	Better AC and Video Specs
AD813AN	HA5013IP	Yes	Better AC and Video Specs
AD813AR-14	HA5013IP	Yes	Better AC and Video Specs
AD817AN	HA3-2841-5	Yes	
AD817AR	HA9P2841-5	Yes	
AD818AN	HA3-2841-5	Yes	
AD818AN	HA3-5020-9	Yes	Better Video, V_{FB} vs C_{FB}
AD818AR	HA9P2841-5	Yes	
AD826AN	HA5023IP	Yes	Better AC and Video Specs V_{FB} vs C_{FB}

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
AD826AR	HA5023IB	Yes	Better AC and Video Specs V_{FB} vs C_{FB}
AD827JN	HA5023IP	Yes	Better Specs, V_{FB} vs C_{FB}
AD827JR	HA5022IB	Yes	Better Specs, V_{FB} vs C_{FB}
AD828AN	HA5023IP	Yes	Lower Power V_{FB} vs C_{FB}
AD828AR	HA5023IP	Yes	Lower Power V_{FB} vs C_{FB}
AD840JN	HA3B2840-5	Yes	Lower Cost
AD840JQ	HA1-2840-5	Yes	Lower Cost
AD840KN	HA3B2840-5	Yes	Lower Cost
AD840KQ	HA1-2840-5	Yes	Lower Cost
AD840SQ	HA1-2840/883	Yes	Lower Cost
AD840SQ/883	HA1-2840/883	Yes	Lower Cost
AD841JH	HA2-2541-5	Yes	
AD841JN	HA3-2841-5	Yes	Lower Cost
AD841JQ	HA1-2541-5	Yes	
AD841KH	HA2-2541-5	Yes	
AD841KN	HA3-2841-5	Yes	Lower Cost
AD841KQ	HA3-2841-5	Yes	Enhanced ACs/lower Power
AD841SH	HA2-2541/883	Yes	Enhanced ACs/lower Power
AD841SQ	HA1-2841/883	Yes	Lower Cost
AD841SQ/883	HA1-2841/883	Yes	Lower Cost
AD842JH	HA2-2542-5	Yes	
AD842JN	HA3B2842-5	Yes	Lower Cost
AD842JQ	HA1-2542-5	Yes	
AD842KH	HA2-2542-5	Yes	
AD842KN	HA3B2842-5	Yes	Lower Cost
AD842KQ	HA1-2542-5	Yes	
AD842SH	HA2-2542/883	Yes	Enhanced ACs/lower Cost
AD842SQ	HA1-2842/883	Yes	Lower Cost
AD842SQ/883	HA1-2842/883	Yes	Lower Cost
AD844AN	HA3-5020-9	Yes	Enhanced ACs and Video Performance
AD844AQ	HA7-5020-9	Yes	Enhanced ACs and Video Performance
AD844BQ	HA7-5020-9	Yes	Enhanced ACs and Video Performance
AD844SQ/883B	HA7-5020/883	Yes	Enhanced ACs and Video Performance
AD846AN	HA3-5020-9	Yes	Enhanced ACs/lower Cost
AD846AQ	HA7-5020-9	Yes	Enhanced ACs/lower Cost
AD846BQ	HA7-5020-9	Yes	Enhanced ACs/lower Cost
AD846SQ	HA7-5020/883	Yes	Enhanced ACs/lower Cost
AD847JN	HA3-2544C-5	Yes	
AD847SQ	HA7-2544-2	Yes	
AD9620AD	HFA1110IJ	Yes	Performance, Price
AD9620SD	HFA1110MJ/883	Yes	Performance, Price
AD9621AQ	HFA1100IJ	Yes	Better Specs, V_{FB} vs C_{FB}
AD9621AR	HFA1105IB	Yes	Lower Power, V_{FB} vs C_{FB}
AD9622AQ	HFA1100IJ	Yes	Better Specs, V_{FB} vs C_{FB}
AD9622AR	HFA1105IB	Yes	Lower Power, V_{FB} vs C_{FB}
AD9623AQ	HFA1100IJ	Yes	Higher Speed, V_{FB} vs C_{FB}
AD9623AR	HFA1105IB	Yes	Lower Power, V_{FB} vs C_{FB}

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
AD9624AQ	HFA1100IJ	Yes	Higher Speed, V_{FB} vs C_{FB}
AD9624AR	HFA1105IB	Yes	Lower Power, V_{FB} vs C_{FB}
AD9630AN	HFA1110IP	Yes	Performance, Price
AD9630AQ	HFA1110IJ	Yes	Performance, Price
AD9630AR	HFA1110IB	Yes	Performance, Price
AD9630SQ	HFA1110MJ/883	Yes	Performance, Price
ADEL2020AN	HA3-5020-9	Yes	
ADLH0032CG	HA2-2542-5	†	Monolithic/lower Cost
ADLH0032G	HA2-2542-2	†	Monolithic/lower Cost
ADLH0033CG	HA2-5033-5	†	Enhanced ACs/monolithic/lower Cost
ADLH0033G	HA2-5033-2	†	Enhanced ACs/monolithic/lower Cost
ADOP27AQ	HA7-5127A-2	Yes	Enhanced ACs/Reduced I_{CC}
ADOP27EQ	HA7-5127A-5	Yes	Enhanced ACs/Reduced I_{CC}
ADOP27GQ	HA7-5127-5	Yes	Enhanced ACs/Reduced I_{CC}
ADOP37AQ	HA7-5137A-2	Yes	Enhanced ACs/Reduced I_{CC}
ADOP37EQ	HA7-5137A-5	Yes	Enhanced ACs/Reduced I_{CC}
ADOP37GQ	HA7-5137-5	Yes	Enhanced ACs/Reduced I_{CC}
AM-450-2	HA2-2505-5	Yes	Guaranteed V_{OUT}/ACs
AM-450-2M	HA2-2502-2	Yes	Guaranteed V_{OUT}/ACs
AM-452-2	HA2-2525-5	Yes	Guaranteed V_{OUT}/ACs
AM-452-2M	HA2-2522-2	Yes	Guaranteed V_{OUT}/ACs
AM-460-2	HA2-2605-5	Yes	Guaranteed V_{OUT}/ACs
AM-460-2M	HA2-2602-2	Yes	Guaranteed V_{OUT}/ACs
AM-462-2	HA2-2625-5	Yes	Guaranteed V_{OUT}/ACs
AM-462-2M	HA2-2620-2	Yes	Guaranteed V_{OUT}/ACs
AM-7650-1	ICL7650SCPD	Yes	Almost Identical
AM-7650-2	ICL7650SCTV-1	Yes	Almost Identical
BUF634P	HA3-5002-5	Yes	
CA3054	CA3054	Yes	V_{OUT} Version Available
CA3146P	CA3146E	Yes	
CLC109AJP	HA3-5002-5	Yes	Higher Output Current
CLC110A8D	HFA1110MJ/883	Yes	Better Performance
CLC110AID	HFA1110IJ	Yes	Better Performance
CLC110AJP	HFA1110IP	Yes	Better Performance
CLC110ALC	HFA1110Y	N/A	Die
CLC400A8D	HFA1120MJ/883	†	Better Performance
CLC400AID	HFA1120IJ	†	Better Performance
CLC400AJE	HFA1105IB	Yes	Faster, Lower Power, ±5V Only
CLC400AJE	HFA1120IB	†	Better Performance
CLC400AJP	HFA1120IP	†	Better Performance
CLC400ALC	HFA1120Y	N/A	Die
CLC401A8D	HFA1100MJ/883	Yes	Better Performance
CLC401AIB	HFA1100IJ	Yes	Better Performance
CLC401AID	HFA1100IJ	Yes	Better Performance
CLC401AJE	HFA1105IB	Yes	Faster, Lower Power
CLC401AJP	HFA1100IP	Yes	Better Performance
CLC401ALC	HFA1100Y	N/A	Die

† Primary Pins are pin-to-pin; secondary/optional pins are not.

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PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
CLC402A8D	HFA1100MJ/883	Yes	Better Performance
CLC402AIB	HFA1100IJ	Yes	Better Performance
CLC402AID	HFA1100IJ	Yes	Better Performance
CLC402AJE	HFA1100IB	Yes	Better Performance
CLC402AJE	HFA1105IB	Yes	Faster, Lower Power
CLC402AJP	HFA1100IP	Yes	Better Performance
CLC402ALC	HFA1100Y	N/A	Die
CLC404A8D	HFA1100MJ/883	Yes	Better Performance
CLC404AIB	HFA1100IJ	Yes	Better Performance
CLC404AID	HFA1100IJ	Yes	Better Performance
CLC404AJE	HFA1100IB	Yes	Better Performance
CLC404AJE	HFA1105IB	Yes	Faster, Lower Power
CLC404AJP	HFA1100IP	Yes	Better Performance
CLC404ALC	HFA1100Y	N/A	Die
CLC406A8D	HFA1100MJ/883	Yes	Better Performance
CLC406AIB	HFA1100IJ	Yes	Better Performance
CLC406AID	HFA1100IJ	Yes	Better Performance
CLC406AJE	HFA1100IB	Yes	Better Performance
CLC406AJE	HFA1105IB	Yes	Faster, Lower Power
CLC406AJP	HFA1100IP	Yes	Better Performance
CLC406ALC	HFA1100Y	N/A	Die
CLC409A8D	HFA1100MJ/883	Yes	Better Performance
CLC409AIB	HFA1100IJ	Yes	Better Performance
CLC409AID	HFA1100IJ	Yes	Better Performance
CLC409AJE	HFA1109IB	Yes	
CLC409AJP	HFA1109IP	Yes	Better Performance
CLC409ALC	HFA1109Y	N/A	Better Performance
CLC410AJP	HFA1149IP	Yes	
CLC410A8D	HFA1120MJ/883	†	CLC Has Enable
CLC410AID	HFA1120IJ	†	CLC Has Enable
CLC410AJE	HFA1149IB	Yes	
CLC410AJP	HFA1149IP	†	CLC Has Enable
CLC410ALC	HFA1149Y	N/A	CLC Has Enable
CLC414AJE	HA5025IB	Yes	Better Video and DC Specifications
CLC414AJP	HA5025IP	Yes	Better Video and DC Specifications
CLC415AJE	HA5025IB	Yes	Better DC Specifications
CLC415AJP	HA5025IP	Yes	Better DC Specifications
CLC425AJE	HFA1100IB	Yes	V_{FB} vs C_{FB}
CLC425AJP	HFA1100IP	Yes	V_{FB} vs C_{FB}
CLC428AJE	HA5023IB	Yes	V_{FB} vs C_{FB}
CLC428AJP	HA5023IP	Yes	V_{FB} vs C_{FB}
CLC430	HA-5020	Yes	Enhanced AC and Video Performance
CLC430AIB	HA7-5020-9	Yes	Better AC Performance
CLC430AID	HA7-5020-9	Yes	Better AC Performance
CLC430AJE	HA9P5020-9	Yes	Better AC Performance
CLC430AJP	HA3-5020-9	Yes	Better AC Performance
CLC432AJE	HA5023IB	Yes	Better AC and Video Specs

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Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
CLC432AJP	HA5023IP	Yes	Better AC and Video Specs
CLC449AJE	HFA1100IB	Yes	
CLC449AJP	HFA1100IP	Yes	
CLC501A8D	HFA1130MJ/883	Yes	Better Performance
CLC501AID	HFA1130IJ	Yes	Better Performance
CLC501AJE	HFA1130IB	Yes	Better Performance
CLC501AJP	HFA1130IP	Yes	Better Performance
CLC502A8D	HFA1130MJ/883	Yes	Better Performance
CLC502AID	HFA1130IJ	Yes	Better Performance
CLC502AJE	HFA1130IB	Yes	Better Performance
CLC502AJP	HFA1130IP	Yes	Better Performance
EHA1-2539-2	HA1-2539-2	Yes	
EHA1-2539-5	HA1-2839-5	Yes	Lower Cost
EHA1-2539/883B	HA1-2839/883	Yes	Lower Cost
EHA1-2540-2	HA1-2540-2	Yes	
EHA1-2540/883	HA1-2840/883	Yes	Lower Cost
EHA1-5190-2	HA1-5190-2	Yes	
EHA1-5195-5	HA1-5195-5	Yes	
EHA2-2500-2	HA2-2500-2	Yes	
EHA2-2502-2	HA2-2502-2	Yes	
EHA2-2505-5	HA2-2505-5	Yes	
EHA2-2510-2	HA2-2510-2	Yes	
EHA2-2512-2	HA2-2512-2	Yes	
EHA2-2515-5	HA2-2515-5	Yes	
EHA2-2520-2	HA2-2520-2	Yes	Substitute HA2-2529-2
EHA2-2522-2	HA2-2522-2	Yes	Substitute HA2-2529-2
EHA2-2525-5	HA2-2525-5	Yes	Substitute HA2-2529-5
EHA2-2600-2	HA2-2600-2	Yes	
EHA2-2602-2	HA2-2602-2	Yes	
EHA2-2605-5	HA2-2605-5	Yes	
EHA2-2620-2	HA2-2620-2	Yes	
EHA2-2622-2	HA2-2622-2	Yes	
EHA2-2625-5	HA2-2625-5	Yes	
EHA2-5190-2	HA2-5190-2	Yes	
EHA2-5195-5	HA2-5195-5	Yes	
EHA3-2539-5	HA3-2839-5	Yes	Lower Cost
EHA3-2540-5	HA3-2540-5	Yes	
EHA3-2540-5	HA3B2840-5	Yes	Lower Cost
EHA7-2500-2	HA7-2500-2	Yes	
EHA7-2502-2	HA7-2502-2	Yes	
EHA7-2505-5	HA7-2505-5	Yes	
EHA7-2510-2	HA7-2510-2	Yes	
EHA7-2512-2	HA7-2512-2	Yes	
EHA7-2515-5	HA7-2515-5	Yes	
EHA7-2520-2	HA7-2520-2	Yes	
EHA7-2522-2	HA7-2522-2	Yes	
EHA7-2525-5	HA7-2525-5	Yes	

† Primary Pins are pin-to-pin; secondary/optional pins are not.

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
EHA7-2600-2	HA7-2600-2	Yes	
EHA7-2602-2	HA7-2602-2	Yes	
EHA7-2605-5	HA7-2605-5	Yes	
EHA7-2620-2	HA7-2620-2	Yes	
EHA7-2622-2	HA7-2622-2	Yes	
EHA7-2625-5	HA7-2625-5	Yes	
EL2003CH	HA2-5002-5	Yes	Greater Slew Rate/Reduced I_{CC}
EL2003CJ	HA7-5002-5	No	Greater Slew Rate/Reduced I_{CC}
EL2003CN	HA3-5002-5	No	Greater Slew Rate/Reduced I_{CC}
EL2003CPL	HA9P5002-9	No	Greater Slew Rate/Reduced I_{CC}
EL2003H	HA2-5002-2	Yes	Greater Slew Rate/Reduced I_{CC}
EL2003J	HA7-5002-2	No	Greater Slew Rate/Reduced I_{CC}
EL2005CG	HA2-5033-5	†	Greater Bandwidth
EL2005G	HA2-5033-2	†	Greater Bandwidth
EL2020CJ	HA7-5020-5	Yes	Better Performance
EL2020CM	HA9P5020-5	†	Enhanced ACs and V_{OUT}/lower Cost
EL2020CN	HA3-5020-5	Yes	Better Performance
EL2020J	HA7-5020/883	Yes	Enhanced ACs and V_{OUT}/lower Cost
EL2020J/883B	HA7-5020/883	Yes	Better Performance
EL2030CJ	HA7-5020-5	†	Enhanced V_{OUT}/lower Cost
EL2030CN	HA3-5020-5	Yes	Disable Feature
EL2030J/883B	HA7-5020/883	†	Enhanced V_{OUT}/lower Cost
EL2033CJ	HA7-5002-5	†	Greater Slew Rate/Reduced I_{CC}
EL2033CN	HA3-5002-5	†	Greater Slew Rate/Reduced I_{CC}
EL2033J	HA7-5002-2	†	Greater Slew Rate/Reduced I_{CC}
EL2039CJ	HA1-2839-5	Yes	Lower Cost
EL2039CN	HA3-2839-5	Yes	Lower Cost
EL2039J	HA1-2839/883	Yes	Enhanced ACs/lower Power/lower Cost
EL2039J/883	HA1-2839/883	Yes	Lower Cost
EL2040CN	HA3B2840-5	Yes	Lower Cost
EL2040J	HA1-2840/883	Yes	Enhanced ACs/lower Power/lower Cost
EL2040J/883	HA1-2840/883	Yes	Lower Cost
EL2041CG	HA2-2541-5	Yes	Enhanced ACs/lower Power/lower Cost
EL2041CJ	HA3-2841-5	Yes	Enhanced ACs/lower Power
EL2041G	HA2-2841/883	Yes	Enhanced ACs/lower Power/lower Cost
EL2041J	HA1-2841/883	Yes	Enhanced ACs/lower Power/lower Cost
EL2044CN	HA3-2841-5	†	Low Power
EL2044CS	HA9P2841-5	Yes	Primary Pins are Pin-to-pin Compatible; Optional Pins are No
EL2070CN	HFA1120IP	†	Better Performance
EL2070CS	HFA1120IB	†	Better Performance
EL2070J/883B	HFA1120MJ/883	†	Better Performance
EL2071CN	HFA1100IP	†	Better Performance
EL2071CS	HFA1120IB	†	Better Performance
EL2071J/883B	HFA1120MJ/883	†	Better Performance
EL2072CN	HFA1110IP	Yes	Better Performance
EL2072CS	HFA1110IB	Yes	Better Performance

† Primary Pins are pin-to-pin; secondary/optional pins are not.

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
EL2072J/883B	HFA1110MJ/883	Yes	Better Performance
EL2120CN	HA3-5020-5	Yes	Lower Power
EL2120CS	HA9P5020-5	Yes	Lower Power
EL2130CN	HFA1100IP	Yes	Better Performance
EL2130CS	HFA1100IB	Yes	Better Performance
EL2130CS	HFA1105IB	Yes	Better Performance, Lower Power
EL2160CN	HA3-5020-5	Yes	
EL2160CS	HA9P5020-5	Yes	
EL2166CN	HA3-5020-5	Yes	
EL2166CS	HA9P5020-5	Yes	
EL2171CN	HFA1100IP	Yes	Better Performance
EL2171CS	HFA1100IB	Yes	Better Performance
EL2171J/883B	HFA1100IJ/883	Yes	Better Performance
EL2190G	HA2-5190-2	Yes	
EL2190J	HA1-5190-2	Yes	
EL2195CG	HA2-5195-5	Yes	
EL2195CJ	HA1-5195-5	Yes	
EL2210CM	HA5023IB	Yes	Better AC and Video Specs
EL2210CN	HA5023IP	Yes	Better AC and Video Specs
EL2211CM	HA5023IB	Yes	Better AC and Video Specs
EL2211CN	HA5023IP	Yes	Better AC and Video Specs
EL2232CN	HA5023IP	Yes	±5V Only
EL2260CN	HA5023IP	Yes	Better Video and DC Specifications, ±5V Only
EL2260CS	HA5023IB	Yes	Better Video and DC Specifications, ±5V Only
EL2310CN	HA5013IP	Yes	Better Performance
EL2310CS	HA5013IB	Yes	Better Performance
EL2311CN	HA5013IP	Yes	Better Performance
EL2311CS	HA5013IB	Yes	Better Performance
EL2410CN	HA5025IP	Yes	Better Performance
EL2410CS	HA5025IB	Yes	Better Performance
EL2411CN	HA5025IP	Yes	Better Performance
EL2411CS	HA5025IB	Yes	Better Performance
EL2460CN	HA5025IP	Yes	Better Video and DC Specifications
EL2460CS	HA5025IB	Yes	Better Video and DC Specifications
EL400CN	HFA1120IP	†	Better Performance
EL400CS	HFA1120IB	†	Better Performance
EL400J/883B	HFA1120MJ/883	†	Better Performance
ELH0032CG	HA2-2542-5	†	
ELH0032G	HA2-2542-2	†	
ELH0033CG	HA2-5033-5	†	Greater Bandwidth
ELH0033G	HA2-5033-2	†	Greater Bandwidth
GB4600-CDA	HA4600CP	Yes	Lower Power, Faster Switching
GB4600-CKA	HA4600CB	Yes	Lower Power, Faster Switching
GX4201-CDA	HA4201CP	Yes	Lower Power, Faster Switching
GX4201-CKA	HA4201CB	Yes	Lower Power, Faster Switching
GX4314-CDB	HA4314ACP	Yes	Lower Power, Faster Switching
GX4314-CKB	HA4314ACB	Yes	Lower Power, Faster Switching

† Primary Pins are pin-to-pin; secondary/optional pins are not.

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
GX4314LCDB	HA4314ACP	Yes	Lower Power, Faster Switching
GX4314LCKB	HA4314ACB	Yes	Lower Power, Faster Switching
GX4404-CDC	HA4404ACP	Yes	Lower Power, Faster Switching
GX4404-CKD	HA4404ACB	Yes	Lower Power, Faster Switching
HOS-100AH	HA2-5033-2	†	Greater Bandwidth/lower Cost
HOS-100SH	HA2-5033-2	†	Greater Bandwidth/lower Cost
HOS050	HA2-2542-2	†	Lower Cost
HOS050A	HA2-2542-2	†	Lower Cost
HOS050C	HA2-2542-2	†	Lower Cost
ICL7611ACPA	ICL7611ACPA	Yes	
ICL7611ACTV	ICL7611ACTV	Yes	
ICL7611AMTV	ICL7611AMTV	Yes	
ICL7611BCPA	ICL7611BCPA	Yes	
ICL7611BCTV	ICL7611BCTV	Yes	
ICL7611BMTV	ICL7611BMTV	Yes	
ICL7611DCPA	ICL7611DCPA	Yes	
ICL7611DCSA	ICL7611DCBA	Yes	
ICL7611DCTV	ICL7611DCTV	Yes	
ICL7611DMTV	ICL7611DMTV	Yes	
ICL7612ACPA	ICL7612ACPA	Yes	
ICL7612ACTV	ICL7612ACTV	Yes	
ICL7612AMTV	ICL7612AMTV	Yes	
ICL7612BCPA	ICL7612BCPA	Yes	
ICL7612BCTV	ICL7612BCTV	Yes	
ICL7612BMTV	ICL7612BMTV	Yes	
ICL7612DCPA	ICL7612DCPA	Yes	
ICL7612DCSA	ICL7612DCBA	Yes	
ICL7612DCTV	ICL7612DCTV	Yes	
ICL7612DMTV	ICL7612DMTV	Yes	
ICL7621ACPA	ICL7621ACPA	Yes	
ICL7621ACTV	ICL7621ACTV	Yes	
ICL7621AMTV	ICL7621AMTV	Yes	
ICL7621BCPA	ICL7621BCPA	Yes	
ICL7621BCTV	ICL7621BCTV	Yes	
ICL7621BMTV	ICL7621BMTV	Yes	
ICL7621DCPA	ICL7621DCPA	Yes	
ICL7621DCSA	ICL7621DCBA	Yes	
ICL7621DCTV	ICL7621DCTV	Yes	
ICL7621DMTV	ICL7621DMTV	Yes	
ICL7641CCPD	ICL7641CCPD	Yes	
ICL7641ECPD	ICL7641ECPD	Yes	
ICL7642CCJD	ICL7642CCJD	Yes	
ICL7642CCPD	ICL7642CCPD	Yes	
ICL7642CMJD	ICL7642CMJD	Yes	
ICL7642ECJD	ICL7642ECJD	Yes	
ICL7642ECPD	ICL7642ECPD	Yes	
ICL7642EMJD	ICL7642EMJD	Yes	

† Primary Pins are pin-to-pin; secondary/optional pins are not.

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PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
ICL7650BCPA-1	ICL7650SCPA-1	Yes	Reduced V_{IO}/I_{BIAS}
ICL7650BCPD	ICL7650SCPD	Yes	Reduced V_{IO}/I_{BIAS}
ICL7650BCTV-1	ICL7650SCTV-1	Yes	Reduced V_{IO}/I_{BIAS}
ICM7242IPA	ICM7242IPA	Yes	
ICM7555CD	ICM7555CBA	Yes	
ICM7555CN	ICM7555IPA	Yes	Wider Operating Voltage Range
ICM7555IN	ICM7555IPA	Yes	Wider Operating Voltage Range
ICM7555IPA	ICM7555IPA	Yes	Wider Operating Voltage Range
ICM7555ITV	ICM7555ITV	Yes	
ICM7555MTV	ICM7555MTV	Yes	
ICM7556IPD	ICM7556IPD	Yes	Wider Operating Supply Range
ICM7556MJD	ICM7556MJD	Yes	Wider Operating Supply Range
KF351N	CA3140E	Yes	Reduced I_{BIAS}/I_{IO}
KS272ACN	CA5260AE	Yes	Specified at +5V Supply
KS272AIN	CA5260AE	Yes	Specified at +5V Supply
KS272CN	CA5260E	Yes	Specified at +5V Supply
KS272IN	CA5260E	Yes	Specified at +5V Supply
KS274CN	CA5470E	Yes	Greater Bandwidth/spec. at +5V Supply
KS274IN	CA5470E	Yes	Greater Bandwidth/spec. at +5V Supply
LF157H	CA3130AT	Yes	Reduced I_{BIAS}
LF198AH	HA1-2420-2 (CDIP)	No	Faster Acquisition
LF198H	HA1-2420-2 (CDIP)	No	Faster Acquisition
LF351D	CA3140M	Yes	Reduced I_{BIAS}/I_{IO}
LF351H	CA3140T	Yes	Reduced I_{BIAS}/I_{IO}
LF351M	CA3140M	Yes	Reduced I_{BIAS}/I_{IO}
LF351N	CA3140E	Yes	Reduced I_{BIAS}/I_{IO}
LF351P	CA3140E	Yes	Reduced I_{BIAS}/I_{IO}
LF353N	CA3240E	Yes	Reduced I_{BIAS}/I_{IO}
LF353P	CA3240E	Yes	Reduced I_{BIAS}/I_{IO}
LF357AH	CA3130AT	Yes	Reduced I_{BIAS}
LF357H	CA3130T	Yes	Reduced I_{BIAS}/I_{IO}
LF357M	CA3130M	Yes	Reduced I_{BIAS}/I_{IO}
LF357N	CA3130E	Yes	Reduced I_{BIAS}/I_{IO}
LF398AH	HA1-2425-5 (CDIP)	No	Faster Acquisition
LF398AN	HA3-2425-5	No	Faster Acquisition
LF398H (CAN)	HA1-2425-5 (CDIP)	No	Faster Acquisition
LF398N	HA3-2425-5	No	Faster Acquisition
LF400CH	CA3100T	†	Similar ACs
LF411CD	CA3140AM	Yes	Reduced I_{BIAS}/I_{IO}
LF411CH	CA3140AT	Yes	Reduced I_{BIAS}/I_{IO}
LF411CN	CA3140AE	Yes	Reduced I_{BIAS}/I_{IO}
LF411CP	CA3140AE	Yes	Reduced I_{BIAS}/I_{IO}
LF411MH	CA3140AT	Yes	Reduced I_{BIAS}/I_{IO}
LF412CD	CA3240AE	Yes	Reduced I_{BIAS}/I_{IO}
LF412CN	CA3140AE	Yes	Reduced I_{BIAS}/I_{IO}
LF412CP	CA3240AE	Yes	Reduced I_{BIAS}/I_{IO}
LH0002CH	HA2-5002-5	†	Enhanced ACs/DCs/monolithic

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
LH0002CN	HA3-5002-5	No	Enhanced ACs/DCs/monolithic
LH0002H	HA2-5002-2	†	Enhanced ACs/DCs/monolithic
LH0022CD	CA3140AE (PDIP)	No	Greater Bandwidth/slew Rate
LH0022CH	CA3140AT	Yes	Greater Bandwidth/slew Rate
LH0032ACG	HA2-2542-S	Yes	Monolithic/lower Cost
LH0032AG	HA2-2542-2	Yes	Monolithic/lower Cost
LH0032CG	HA2-2542-5	Yes	Monolithic/lower Cost
LH0032G	HA2-2542-2	Yes	Monolithic/lower Cost
LH0033ACG	HA2-5033-5	†	Greater Bandwidth/monolithic/lower Cost
LH0033AG	HA2-5033-2	†	Monolithic/lower Cost
LH0033CG	HA2-5033-5	†	Greater Bandwidth/monolithic/lower Cost
LH0033CJ	HA3-5033-5	†	Monolithic/lower Cost
LH0033G	HA2-5033-2	†	Monolithic/lower Cost
LH0042CD	CA3140E (PDIP)	No	Greater Bandwidth/slew Rate
LH0042CH	CA3140T	Yes	Greater Bandwidth/slew Rate
LH4161CH	HA2-2544-5	No	Pdip Substitute Is HA3-2544C-5
LH4161CJ	HA7-2544-5	No	
LH4161H	HA2-2544-2	No	
LH4161J	HA7-2544-2	No	
LM143H	HA2-2640-2	†	Enhanced ACs
LM193H	CA3290AT	Yes	Mosfet Input
LM2901N	CA3290AE	Yes	Mosfet Input
LM2903N	CA3290AE	Yes	Mosfet Input
LM293H	CA3290AT	Yes	Mosfet Input
LM3045J	CA3045F	Yes	
LM3046D	CA3046M	Yes	
LM3046N	CA3046E	Yes	
LM3080AN	CA3080AE	Yes	
LM3080N	CA3080E	Yes	
LM3086J	CA3086F	Yes	
LM3086M	CA3086M	Yes	
LM3086N	CA3086	Yes	
LM3146M	CA3146M	Yes	Enhanced A Version Offered
LM3146N	CA3146E	Yes	Enhanced A Version Offered
LM3302N	CA3290E/LM3302N	Yes	
LM343H	HA2-2645-5	†	Enhanced ACs
LM393H	CA3290AT	Yes	Mosfet Input
LM393N	CA3290AE	Yes	Mosfet Input
LM556CN	ICM7556IPD	Yes	CMOS/Reduced I_{CC}
LM604ACM	HA9P2406-5	No	Enhanced ACs
LM604ACN	HA3-2406-5	No	Enhanced ACs
LM604AMJ	HA1-2400-2	No	Enhanced ACs
LM604CM	HA9P2406-5	No	Enhanced ACs
LM604CN	HA3-2406-5	No	Enhanced ACs
LM6118J	HA7-5222-9	Yes	Lower V_{IO}
LM6161J	HA7-2544-2	†	Guaranteed Differential Phase/gain
LM6162M	HA9P5020-5	Yes	Better Specs With Disable

† Primary Pins are pin-to-pin; secondary/optional pins are not.

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PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
LM6162N	HA3-2841-5	Yes	Better AC and Video Specs
LM6164J	HA1-5190-2	No	Reduced Voltage Noise
LM6165J	HA1-2540-2	No	Enhanced Slew Rate/A_{VOL}
LM6181AIN	HA3-5020-9	Yes	
LM6181IN	HA3-5020-9	Yes	
LM6182AIN	HA5023IP	Yes	
LM6182IN	HA5023IP	Yes	
LM6218AJ	HA7-5222-9	Yes	Lower V_{IO}
LM6262M	HA9P5020-5	Yes	Better Specs With Disable
LM6262N	HA3-2841-5	Yes	Better AC and Video Specs
LM6262N	HA3-5020-5	Yes	Better Specs With Disable
LM6361N	HA3-2544C-5	†	Guaranteed Differential Phase/gain
LM6362M	HA9P5020-5	Yes	Better Specs With Disable
LM6362N	HA3-2841-5	Yes	Better AC and Video Specs
LM6362N	HA3-5020-5	Yes	Better Specs With Disable
LM6364N	HA1-5195-5	No	Reduced Voltage Noise
LM6365N	HA3-2540C-5	No	Enhanced Slew Rate/A_{VOL}
LMC555CH	ICM7555ITV	Yes	Reduced I_{CC}/wider Supply Range
LMC555CM	ICM7555CBA	Yes	Reduced I_{CC}/wider Supply Range
LMC555CN	ICM7555IPA	Yes	Reduced I_{CC}/wider Supply Range
LMC668ACJ	ICL7650SIJD	Yes	Enhanced V_{OUT}
LMC668ACJ-8	ICL7650SIJA-1	Yes	Enhanced V_{OUT}
LMC668ACN	ICL7650SIPD	Yes	Enhanced V_{OUT}
LS204AT	HA2-5102-2	Yes	Reduced Noise Voltage
LS204CB	HA3-5102-5	Yes	Reduced Noise Voltage
LS204CM	HA9P-5102-5	Yes	Reduced Noise Voltage
LS204CT	HA2-5102-5	Yes	Reduced Noise Voltage
LS204T	HA2-5102-2	Yes	Reduced Noise Voltage
LS404CB	HA3-5104-5	Yes	Reduced Noise Voltage
LS404CM	HA9P-5104-5	No	Reduced Noise Voltage, Wide Body 16 Ld. SOIC
LS404M	HA9P-5104-9	No	Reduced Noise Voltage, Wide Body 16 Ld. SOIC
LT1014AMJ	HA1-5134A-2	Yes	Reduced V_{IO}/enhanced ACs
LT1014CJ	HA1-5134-5	Yes	Reduced V_{IO}/enhanced ACs
LT1014MJ	HA1-5134-2	Yes	Reduced V_{IO}/enhanced ACs
LT1022CH	HA2-5160-5	†	Greater Bandwidth/slew Rate
LT1022MH	HA2-5160-2	†	Greater Bandwidth/slew Rate
LT1037ACJ8	HA7-5137A-5	Yes	Enhanced ACs/Reduced I_{CC}
LT1037AMJ8	HA7-5137A-2	Yes	Enhanced ACs/Reduced I_{CC}
LT1037CJ8	HA7-5137-5	Yes	Enhanced ACs/Reduced I_{CC}
LT1037MJ8	HA7-5137-2	Yes	Enhanced ACs/Reduced I_{CC}
LT1126ACN8	HA3-5222-5	Yes	
LT1126AMJ8	HA7-5222/883	Yes	
LT1126CJ8	HA7-5222-5	Yes	
LT1126CN8	HA3-5222-5	Yes	
LT1126MJ8	HA7-5222/883	Yes	
LT1190CN8	HA3-2841-5	Yes	Better Video Specs, Lower Power
LT1190CS8	HA9P2841-5	Yes	Better Video Specs, Lower Power

† Primary Pins are pin-to-pin; secondary/optional pins are not.

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
LT1192CN8	HA3-2842-5	Yes	Better Video Specs, Lower Power
LT1192CS8	HA9P2842-5	Yes	Better Video Specs, Lower Power
LT1195CN8	HA3-2841-5	Yes	Better Video Specs, Lower Power
LT1195CS8	HA9P2841-5	Yes	Better Video Specs, Lower Power
LT1206CN8	HA3-5002-5	Yes	Better AC Specs
LT1208CN8	HA5023IP	Yes	Better Performance
LT1208CS8	HA5023IB	Yes	Better Performance
LT1209CN	HA5025IP	Yes	
LT1220CN8	HA3-2841-5	Yes	
LT1221CN8	HA3-2841-5	Yes	
LT1221MJ8	HA7-2841/883	Yes	
LT1222CJ8	HA7-2840-5	†	
LT1222CN8	HA3-2840-5	†	
LT1222MJ8	HA7-2840/883	†	
LT1223CJ8	HA7-5020-5	Yes	Enhanced ACs and Video Performance
LT1223CN8	HA3-5020-5	Yes	Enhanced ACs and Video Performance
LT1223CS8	HA9P5020-5	Yes	Enhanced ACs and Video Performance
LT1223MJ8	HA7-5020/883	Yes	Enhanced ACs and Video Performance
LT1224CN8	HA3-2841-5	Yes	Better Video Specifications
LT1224CS8	HA9P2841-5	Yes	Better Video Specifications
LT1224MJ8	HA7-2841/883	Yes	Better Video Specifications
LT1225CN8	HA3-2841-5	Yes	For Gains >5
LT1225CS8	HA9P2841-5	Yes	For Gains >5
LT1225MJ8	HA7-2841/883	Yes	For Gains >5
LT1226CJ8	HA7-2840-5	†	For Gains >25
LT1226CN8	HA3-2840-5	†	For Gains >25
LT1226CS8	HA9P2840-5	†	For Gains >25
LT1226MJ8	HA7-2840/883	†	For Gains >25
LT1227CN8	HA3-5020-5	Yes	Lower Cost
LT1227CS8	HA9P5020-5	Yes	Lower Cost
LT1227MJ8	HA7-5020/883	Yes	Lower Cost
LT1229CN8	HA5023IP	Yes	Better Video and DC Specifications, ±5V Only
LT1229CS8	HA5023IB	Yes	Better Video and DC Specifications, ±5V Only
LT1230CS	HA5025IB	Yes	Better Video and DC Specifications
LT123OCN	HA5025IP	Yes	Better Video and DC Specifications
LT1252CN8	HA3-5020-5	Yes	
LT1252CS8	HA9P5020-5	Yes	
LT1253CN8	HA5023IP	Yes	Better AC and Video Specs
LT1253CS8	HA5023IB	Yes	Better AC and Video Specs
LT1254CN	HA5025IP	Yes	Better AC and Video Specs
LT1254CS	HA5025IB	Yes	Better Slew Rate and Video Specs
LT1259CN	HA5022IP	Yes	Functional Equivalent
LT1259CS	HA5022IB	Yes	Functional Equivalent
LT1260CN	HA5013IP	Yes	
LT1260CS	HA5013IB	Yes	
LT1360CN8	HA3-2841-5	Yes	
LT1360CN8	HA3-5020-5	Yes	V_{FB} vs C_{FB}

† Primary Pins are pin-to-pin; secondary/optional pins are not.

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
LT1360CS8	HA9P2841-5	Yes	
LT1360CS8	HA9P5020-5	Yes	V_{FB} vs C_{FB}
LT1361CN8	HA5023IP	Yes	V_{FB} vs C_{FB}
LT1361CS8	HA5023IB	Yes	V_{FB} vs C_{FB}
LT1362CN	HA5025IP	Yes	V_{FB} vs C_{FB}
LT1362CS	HA5025IB	Yes	Functional Equivalent
LT1363CN8	HA3-2841-5	Yes	
LT1363CN8	HA3-5020-5	Yes	V_{FB} vs C_{FB}
LT1363CS8	HA9P2841-5	Yes	
LT1363CS8	HA9P5020-5	Yes	V_{FB} vs C_{FB}
LT1364CN8	HA5023IP	Yes	V_{FB} vs C_{FB}
LT1364CS8	HA5023IB	Yes	V_{FB} vs C_{FB}
LT1365CN	HA5025IP	Yes	V_{FB} vs C_{FB}
LT1365CS	HA5025IB	Yes	V_{FB} vs C_{FB}
LTC1050ACH	ICL7650SITV-1	†	Reduced I_{BIAS}/I_{IO}
LTC1050ACN8	ICL7650SIPA-1	†	Reduced I_{BIAS}/I_{IO}
LTC1050AMH	ICL7650SMTV-1	†	Reduced I_{BIAS}/I_{IO}
LTC1050CH	ICL7650SITV-1	†	Reduced I_{BIAS}/I_{IO}/greater A_{VOL}
LTC1050CN8	ICL7650SIPA-1	†	Reduced I_{BIAS}/I_{IO}/greater A_{VOL}
LTC1050CP	ICL7650SIPA-1	†	Reduced I_{BIAS}/I_{IO}
LTC1050MH	ICL7650SMTV-1	†	Reduced I_{BIAS}/I_{IO}/greater A_{VOL}
MAX404CPA	HA3-2842-5	Yes	
MAX404CSA	HA9P2842-5	Yes	Better Video Specs, Lower Power
MAX404EPA	HA3-2842-9	Yes	Better Video Specs, Lower Power
MAX404ESA	HA9P2842-5	Yes	Better Video Specs, Lower Power
MAX452CPA	HA3-2841-5	Yes	Lower Power
MAX452CSA	HA9P2841-5	Yes	Lower Power
MAX452EJA	HA3-2841-9	Yes	Lower Power
MAX452EPA	HA3-2841-9	Yes	Lower Power
MAX457CPA	HA5023IP	Yes	Better Performance, Lower Power
MAX457CSA	HA5023IB	Yes	Better Performance, Lower Power
MAX457EPA	HA5023IP	Yes	Better Performance, Lower Power
MAX460IGC	HA2-5033-5	†	Greater Bandwidth
MAX460MGC	HA2-5033-2	†	Greater Bandwidth
MAX467CPE	HA5013IP	Yes	Better AC Specs, Lower Power
MAX467CWE	HA5013IB	Yes	Better AC Specs, Lower Power
MC1776CD	ICL7611DCBA	Yes	Lower Power Drain
MC1776CG	ICL7611BCTV	Yes	Lower Power Drain
MC1776CP1	ICL7611BCPA	Yes	Lower Power Drain
MC1776G	ICL7611BMTV	Yes	Lower Power Drain
MC3302N	CA3290E	Yes	Mosfet Input
MC3303D	CA5470M	Yes	Mos Input/enhanced ACs
MC3303N	CA5470E	Yes	Femos Input/enhanced ACs
MC33071P	CA3140AE	Yes	Reduced I_{BIAS}/I_{IO}
MC33072P	CA3240AE	Yes	Reduced I_{BIAS}/I_{IO}
MC3346D	CA3046M	Yes	Full -55 To 125^{o}C Operation
MC3346P	CA3046E	Yes	Full -55 To 125^{o}C Operation

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
MC34001BG	CA3140AT	Yes	Reduced I_{BIAS}/I_{IO}
MC34001BP	CA3140AE	Yes	Reduced I_{BIAS}/I_{IO}
MC34001G	CA3140T	Yes	Reduced I_{BIAS}/I_{IO}
MC34001P	CA3140E	Yes	Reduced I_{BIAS}/I_{IO}
MC34002BG	CA3240AT	Yes	Reduced I_{BIAS}/I_{IO}
MC34002BP	CA3240AE	Yes	Reduced I_{BIAS}/I_{IO}
MC34002G	CA3240T	Yes	Reduced I_{BIAS}/I_{IO}
MC34002P	CA3240E	Yes	Reduced I_{BIAS}/I_{IO}
MC3403D	CA5470M	Yes	Mos Input/enhanced ACs
MC3403N	CA5470E	Yes	Mos Input/enhanced ACs
MC34071P	CA3140AE	Yes	Reduced I_{BIAS}/I_{IO}
MC34072P	CA3240AE	Yes	Reduced I_{BIAS}/I_{IO}
MC3456L	ICM7556MJD	Yes	CMOS/Reduced I_{CC}
MC3456P	ICM7556IPD	Yes	CMOS/Reduced I_{CC}
MC3556L	ICM7556MJD	Yes	CMOS/Reduced I_{CC}
MC668ACN-8	ICL7650SCPA-1	Yes	Enhanced V_{OUT}
NE5230N	CA5160AE	No	Mos Input
NE5517AN	CA3280AE	No	Reduced V_{IO}
NE5517D	CA3280M	No	Reduced V_{IO}
NE5517N	CA3280E	No	Reduced V_{IO}
NE5532AFE	HA7-5102-5	Yes	Enhanced V_{OUT}/Reduced I_{CC}
NE5532AN	HA3-5102-5	Yes	Enhanced V_{OUT}/Reduced I_{CC}
NE5532FE	HA7-5102-5	Yes	Enhanced V_{OUT}/Reduced I_{CC}
NE5532N	HA3-5102-5	Yes	Enhanced V_{OUT}/Reduced I_{CC}
NE5534AFE	HA7-5101-5	†	Enhanced V_{OUT}
NE5534AN	HA3-5101-5	†	Enhanced V_{OUT}
NE5534FE	HA7-5101-5	†	Enhanced V_{OUT}
NE5534N	HA3-5101-5	†	Enhanced V_{OUT}
NE5539D	HA9P-2539-5	†	Specified at ±15V Supplies
NE5539F	HA1-2839-5	†	Specified at ±15V Supplies
NE5539N	HA3-2839-5	†	Specified at ±15V Supplies
NE556-1N	ICM7556IPD	Yes	CMOS/Reduced I_{CC}
NE556N	ICM7556IPD	Yes	CMOS/Reduced I_{CC}
OP-15CH	CA3140AT	Yes	Reduced I_{BIAS}/I_{IO}
OP-15GN8	CA3140AE	Yes	Reduced I_{BIAS}/I_{IO}
OP11AY	HA1-5134-2	Yes	Enhanced ACs
OP11EY	HA1-5134-5	Yes	Enhanced ACs
OP11FY	HA1-5104-5	Yes	Enhanced ACs
OP160GP	HA3-5020-9	Yes	
OP160GS	HA9P5020-5	Yes	
OP215GZ	CA3240AE (PDIP)	Yes	
OP220CJ	HA2-5142-2	Yes	Enhanced ACs
OP220CZ	HA7-5142-2	Yes	Enhanced ACs
OP220GJ	HA2-5142-5	Yes	Enhanced ACs
OP220GZ	HA7-5142-5	Yes	Enhanced ACs
OP271AZ	HA7-5102-2	Yes	Lower Voltage Noise/greater Bandwidth

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
OP271EZ	HA7-5102-5	Yes	Lower Voltage Noise/greater Bandwidth
OP271FZ	HA7-5102-5	Yes	Lower Voltage Noise/greater Bandwidth
OP271GP	HA3-5102-5	Yes	Lower Voltage Noise/greater Bandwidth
OP271GS	HA9P-5102-9	Yes	Lower Voltage Noise/greater Bandwidth
OP27AJ8	HA7-5127A-2	Yes	Enhanced ACs/Reduced I_{CC}
OP27AZ	HA7-5127A-2	Yes	Enhanced ACs/Reduced I_{CC}
OP27CJ8	HA7-5127-2	Yes	Enhanced ACs/Reduced I_{CC}
OP27CZ	HA7-5127-2	Yes	Enhanced ACs/Reduced I_{CC}
OP27EJ8	HA7-5127A-5	Yes	Enhanced ACs/Reduced I_{CC}
OP27EZ	HA7-5127A-5	Yes	Enhanced ACs/Reduced I_{CC}
OP27GJ8	HA7-5127-5	Yes	Enhanced ACs/Reduced I_{CC}
OP27GZ	HA7-5127-5	Yes	Enhanced ACs/Reduced I_{CC}
OP37AJ8	HA7-5137A-2	Yes	Enhanced ACs/Reduced I_{CC}
OP37AZ	HA7-5137A-2	Yes	Enhanced ACs/Reduced I_{CC}
OP37CJ8	HA7-5137-2	Yes	Enhanced ACs/Reduced I_{CC}
OP37CZ	HA7-5137-2	Yes	Enhanced ACs/Reduced I_{CC}
OP37EJ8	HA7-5137A-5	Yes	Enhanced ACs/Reduced I_{CC}
OP37EZ	HA7-5137A-5	Yes	Enhanced ACs/Reduced I_{CC}
OP37GJ8	HA7-5137-5	Yes	Enhanced ACs/Reduced I_{CC}
OP37GZ	HA7-5137-5	Yes	Enhanced ACs/Reduced I_{CC}
OP400AY	HA1-5134A-2	Yes	
OP400EY	HA1-5134A-5	Yes	
OP400FY	HA1-5134-5	Yes	
OP420BY	HA1-5144-2	Yes	Enhanced ACs
OP420CY	HA1-5144-2	Yes	Enhanced ACs
OP420HY	HA1-5144-5	Yes	Enhanced ACs
OP470AY	HA1-5104-2	Yes	
OP470EY	HA1-5104-5	Yes	
OP470FY	HA1-5104-5	Yes	
OP470GP	HA3-5104-5	Yes	
OP470GS	HA9P5104-5	Yes	
OP470GS	HA9P5104-5	Yes	
OP47AD	HA7-5147A-2	Yes	Greater Bandwidth/min A_{CL} = 10
OP47AT	HA2-5147A-2	Yes	Greater Bandwidth/min A_{CL} = 10
OP47CD	HA7-5147-2	Yes	Greater Bandwidth/min A_{CL} = 10
OP47CT	HA2-5147-2	Yes	Greater Bandwidth/min A_{CL} = 10
OP47EN	HA7-5147A-5 (CDIP)	Yes	Greater Bandwidth/min A_{CL} = 10
OP47GN	HA7-5147-5 (CDIP)	Yes	Greater Bandwidth/min A_{CL} = 10
OP62AJ	HA2-5221-5	†	Greater Slew Rate
OP62AZ	HA7-5221-9	†	Greater Slew Rate
OP62EJ	HA2-5221-5	†	Greater Slew Rate
OP62EZ	HA7-5221-9	†	Greater Slew Rate
OP62FJ	HA2-5221-5	†	Greater Slew Rate
OP62FZ	HA7-5221-9	†	Greater Slew Rate
OP63AJ	HA2-5221-5	†	Reduced V_{IO}
OP63AZ	HA7-5221-9	†	Reduced V_{IO}
OP63EJ	HA2-5221-5	†	Reduced V_{IO}

† Primary Pins are pin-to-pin; secondary/optional pins are not.

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
OP63EZ	HA7-5221-9	†	Reduced V_{IO}
OP63FJ	HA2-5221-5	†	Reduced V_{IO}
OP63FZ	HA7-5221-9	†	Reduced V_{IO}
OP64AJ	HA2-5221-5	†	Reduced V_{IO}
OP64AZ	HA7-2622-2	Yes	
OP64AZ	HA7-5221-9	†	Reduced V_{IO}
OP64EJ	HA2-5221-5	†	Reduced V_{IO}
OP64EZ	HA7-5221-9	†	Reduced V_{IO}
OP64FJ	HA2-5221-5	†	Reduced V_{IO}
OP64FZ	HA7-2625-5	Yes	
OP64FZ	HA7-5221-9	†	Reduced V_{IO}
OP80FJ	CA5420AT	†	Single Supply Operation
OP80GJ	CA5420T	†	Single Supply Operation
OP80GP	CA5420E	†	Single Supply Operation
OPA121KP	CA3140AE	†	Mos Input/enhanced ACs
OPA2111KM	HA2-5102-5	Yes	Greater Bandwidth
OPA2111KP	HA3-5102-5	Yes	Greater Bandwidth
OPA27AZ	HA7-5127A-2	Yes	Enhanced ACs/Reduced I_{CC}
OPA27CZ	HA7-5127-2	Yes	Enhanced ACs/Reduced I_{CC}
OPA27EZ	HA7-5127A-5	Yes	Enhanced ACs/Reduced I_{CC}
OPA27GZ	HA7-5127-5	Yes	Enhanced ACs/Reduced I_{CC}
OPA37AZ	HA7-5137A-2	Yes	Enhanced ACs/Reduced I_{CC}
OPA37CZ	HA7-5137-2	Yes	Enhanced ACs/Reduced I_{CC}
OPA37EZ	HA7-5137A-5	Yes	Enhanced ACs/Reduced I_{CC}
OPA37GZ	HA7-5137-5	Yes	Enhanced ACs/Reduced I_{CC}
OPA404AG	HA1-5114-5	Yes	Lower Voltage Noise/enhanced ACs
OPA404BG	HA1-5114-5	Yes	Lower Voltage Noise/enhanced ACs
OPA404KP	HA3-5114-5	Yes	Lower Voltage Noise/enhanced ACs
OPA404KU	HA9P5114-5	Yes	Lower Voltage Noise/enhanced ACs
OPA404SG	HA1-5114-2	Yes	Lower Voltage Noise/enhanced ACs
OPA445AP	HA7-2645-5	Yes	
OPA445BM	HA2-2640-2	Yes	
OPA445SM	HA2-2640-2	Yes	
OPA623AU	HFA1105IB	Yes	Better Video and DC Specifications
OPA633AH	HA2-5033-2	Yes	
OPA633KP	HA3-5033-5	Yes	
OPA633SH	HA2-5033-5	Yes	
OPA644H	HFA1100IJ	Yes	Better Bandwidth
OPA644HB	HFA1100IJ	Yes	Better Bandwidth
OPA644P	HFA1100IP	Yes	Better Bandwidth
OPA644PB	HFA1100IP	Yes	Better Bandwidth
OPA644U	HFA1100IB	Yes	Better Bandwidth
OPA644UB	HFA1100IB	Yes	Better Bandwidth
OPA648H	HFA1100IJ	Yes	
OPA648P	HFA1100IP	Yes	
OPA648U	HFA1100IB	Yes	

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
OPA658P	HFA1100IP	Yes	Harris Is Higher I_{CC}
OPA658PB	HFA1100IP	Yes	Harris Is Higher I_{CC}
OPA658U	HFA1100IB	Yes	Harris Is Higher I_{CC}
OPA658U	HFA1105IB	Yes	Harris Is Lower AC
OPA658UB	HFA1100IB	Yes	Harris Is Higher I_{CC}
OPA658UB	HFA1105IB	Yes	Harris Is Lower ACs
RC3403AN	CA5470E	Yes	Mos Input/enhanced ACs
RC4741D	HA1-4741-2	Yes	Guaranteed ACs
RC4741M	HA9P4741-9	Yes	Guaranteed ACs
RC5532AN	HA3-5102-5	Yes	Enhanced V_{OUT}/Reduced I_{CC}
RC5532N	HA3-5102-5	Yes	Enhanced V_{OUT}/Reduced I_{CC}
RC5534AN	HA3-5101-5	†	Enhanced V_{OUT}/Reduced I_{CC}
RC5534N	HA3-5101-5	†	Enhanced V_{OUT}/Reduced I_{CC}
RM5334T	HA2-5101-2	†	Reduced I_{CC}
RM5532AD	HA7-5102-2	Yes	Reduced I_{CC}
RM5532AT	HA2-5102-2	Yes	Reduced I_{CC}
RM5532D	HA7-5102-2	Yes	Reduced I_{CC}
RM5532T	HA2-5102-2	Yes	Reduced I_{CC}
RM5534AD	HA7-5101-2	†	Reduced I_{CC}
RM5534AT	HA2-5101-2	†	Reduced I_{CC}
RM5534D	HA7-5101-2	†	Reduced I_{CC}
SA556-1N	ICM7556IPD	Yes	CMOS/Reduced I_{CC}
SA556N	ICM7556IPD	Yes	CMOS/Reduced I_{CC}
SE5532AFE	HA7-5102-2	Yes	Reduced I_{CC}
SE5532FE	HA7-5102-2	Yes	Reduced I_{CC}
SE5534AFE	HA7-5101-2	†	Reduced I_{BIAS}/I_{IO}
SE5534FE	HA7-5101-2	†	Reduced I_{BIAS}/I_{IO}
SE5539F	HA1-2539-2	†	Specified at ±15V Supplies
SE556-1CN	ICM7556MJD	Yes	CMOS/Reduced I_{CC}
SE556-1F	ICM7556MJD	Yes	CMOS/Reduced I_{CC}
SE556F	ICM7556MJD	Yes	CMOS/Reduced I_{CC}
SG1536T	HA2-2640-2	†	Reduced V_{IO}/enhanced ACs
SG1536Y	HA7-2640-2	†	Reduced V_{IO}/enhanced ACs
SG3045J	CA3045F	Yes	
SG3049T	CA3049T	Yes	Greater Bandwidth/Reduced Noise
SG3083	CA3083	Yes	
SG3183D	CA3183M	Yes	Identical Specs at 25°C
SG3183N	CA3183E	Yes	Identical Specs at 25°C
SHC5320KH	HA1-5320-5	Yes	
SHC5320SH	HA1-5320-2	Yes	
SHC85	HA1-2425-5	No	Enhanced ACs
SHC85ET	HA1-2420-2	No	Enhanced ACs
SHM-20C	HA1-5320-5	Yes	Guaranteed Acquisition Time
SHM-20M	HA1-5320-2	Yes	Guaranteed Acquisition Time
SHM-IC-1	HA1-2425-5	Yes	Almost Identical
SHM-IC-1M	HA1-2420-2	Yes	Almost Identical

† Primary Pins are pin-to-pin; secondary/optional pins are not.

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
SL3045C-DG	CA3045F	Yes	
SL3046C-DP	CA3046E	Yes	
SL3127C-DC	CA3127F	Yes	V_{OUT} Version Available
SL3127C-DP	CA3127E	Yes	
SL3145C-DC	CA3045F	Yes	Greater Breakdown Voltages
SL3145C-DP	CA3046E	Yes	Greater Breakdown Voltages
SL3227-DP	CA3227E	Yes	Greater Breakdown Voltages
SL3227-MP	CA3227M	Yes	Greater Breakdown Voltages
SL3245-DP	CA3246E	Yes	Programmable Biasing Current
SL3245-MP	CA3246M	Yes	Faster Acquisition/lower Droop
SMP10AY	HA1-2420-2	†	Faster Acquisition/lower Droop
SMP10BY	HA1-2420-2	†	Faster Acquisition/lower Droop
SMP10EY	HA1-2425-5	†	Faster Acquisition/lower Droop
SMP10FY	HA1-2425-5	†	Faster Acquisition/lower Droop
SMP11AY	HA1-2420-2	†	Faster Acquisition/lower Droop
SMP11BY	HA1-2420-2	†	Faster Acquisition/lower Droop
SMP11EY	HA1-2425-5	†	
SMP11FY	HA1-2425-5	†	
SP1-2541-2	HA1-2541-2	Yes	
SP1-2541-5	HA1-2541-5	Yes	
SP1-2542-2	HA1-2542-2	Yes	
SP1-2542-5	HA1-2542-5	Yes	
SP1-5330-2	HA1-5330-2	Yes	
SP1-5330-5	HA1-5330-5	Yes	
SP2-2500-2	HA2-2500-2	Yes	
SP2-2502-2	HA2-2502-2	Yes	
SP2-2505-5	HA2-2505-5	Yes	
SP2-2510-2	HA2-2510-2	Yes	
SP2-2512-2	HA2-2512-2	Yes	
SP2-2515-5	HA2-2515-5	Yes	
SP2-2520-2	HA2-2520-2	Yes	Substitute HA2-2529-2
SP2-2522-2	HA2-2522-2	Yes	Substitute HA2-2529-2
SP2-2525-5	HA2-2525-5	Yes	Substitute HA2-2529-5
SP2-2541-2	HA2-2541-2	Yes	
SP2-2541-5	HA2-2541-5	Yes	
SP2-2542-2	HA2-2542-2	Yes	
SP2-2542-5	HA2-2542-5	Yes	
SP2-2600-2	HA2-2600-2	Yes	
SP2-2602-2	HA2-2602-2	Yes	
SP2-2605-5	HA2-2605-5	Yes	
SP2-2620-2	HA2-2620-2	Yes	
SP2-2622-2	HA2-2622-2	Yes	
SP2-2625-5	HA2-2625-5	Yes	
SP3-2505-5	HA3-2505-5	Yes	
SP3-2515-5	HA3-2515-5	Yes	
SP3-2525-5	HA3-2525-5	Yes	Substitute HA3-2529-5
SP3-2542-5	HA3B2842-5	Yes	

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
SP3-2605-5	HA3-2605-5	Yes	
SP3-2625-5	HA3-2625-5	Yes	
SP7-2500-2	HA7-2500-2	Yes	
SP7-2502-2	HA7-2502-2	Yes	
SP7-2505-5	HA7-2505-5	Yes	
SP7-2510-2	HA7-2510-2	Yes	
SP7-2512-2	HA7-2512-2	Yes	
SP7-2515-5	HA7-2515-5	Yes	
SP7-2520-2	HA7-2520-2	Yes	Substitute HA7-2529-2
SP7-2522-2	HA7-2522-2	Yes	Substitute HA7-2529-2
SP7-2525-5	HA7-2525-5	Yes	Substitute HA7-2529-5
SP7-2600-2	HA7-2600-2	Yes	
SP7-2602-2	HA7-2602-2	Yes	
SP7-2605-5	HA7-2605-5	Yes	
SP7-2620-2	HA7-2620-2	Yes	
SP7-2622-2	HA7-2622-2	Yes	
SP7-2625-5	HA7-2625-5	Yes	
TA75393P	CA3290AE/CA3290E	Yes	Reduced $I_{BIAS}/I_{IO}/I_{CC}$
TA75557F	HA9P5102-9	No	Greater Bandwidth/Reduced Vnoise
TA75557P	HA3-5102-5	Yes	Greater Bandwidth/Reduced Vnoise
TA75559F	HA9P5112-9	No	Greater Bandwidth/Reduced Vnoise
TA75559P	HA3-5112-5	Yes	Greater Bandwidth/Reduced Vnoise
TCA971	CA3146AE/CA3046E	Yes	Greater VCBO With CA3146
TCA971G	CA3146AM/CA3046M	Yes	Greater VCBO With CA3146
TCA991	CA3146E/CA3046E	Yes	Greater VCBO With CA3146
TCA991G	CA3146M/CA3046M	Yes	Greater VCBO With CA3146
TD62507F	CA3183AM	No	Alt. Product Is CA3083
TD62507P	CA3183AE	No	Alt. Product Is CA3083
TDB2046DP	CA3046E	Yes	Full -55 To 125°C Operation
TDB2046FP	CA3046M	Yes	Full -55 To 125°C Operation
TLC252ACD	CA5260AM	Yes	Specified at +5V Supply
TLC252ACP	CA5260AE	Yes	Specified at +5V Supply
TLC252CD	CA5260M	Yes	Specified at +5V Supply
TLC252CP	CA5260E	Yes	Specified at +5V Supply
TLC254CD	CA5470M	Yes	Specified at +5V Supply
TLC254CN	CA5470E	Yes	Specified at +5V Supply
TLC272ACD	CA5260AM	Yes	Greater V_{OUT} Range/Reduced I_{CC}
TLC272ACP	CA5260AE	Yes	Greater V_{OUT} Range/Reduced I_{CC}
TLC272AID	CA5260AM	Yes	Greater V_{OUT} Range/Reduced I_{CC}
TLC272AIP	CA5260AE	Yes	Greater V_{OUT} Range/Reduced I_{CC}
TLC272CD	CA5260M	Yes	Greater V_{OUT} Range/Reduced I_{CC}
TLC272CP	CA5260E	Yes	Greater V_{OUT} Range/Reduced I_{CC}
TLC272ID	CA5260M	Yes	Greater V_{OUT} Range/Reduced I_{CC}
TLC272IP	CA5260E	Yes	Greater V_{OUT} Range/Reduced I_{CC}
TLC272MJG	CA5260E (PDIP)	Yes	Greater V_{OUT} Range/Reduced I_{CC}
TLC274CD	CA5470M	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC274CN	CA5470E	Yes	Greater V_{OUT}/bandwidth/slew Rate

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
TLC274ID	CA5470M	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC274IN	CA5470E	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC274MJ	CA5470E (PDIP)	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC27M2ACD	CA5260AM	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC27M2ACP	CA5260AE	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC27M2AID	CA5260AM	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC27M2AIP	CA5260AE	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC27M2CD	CA5260M	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC27M2CP	CA5260E	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC27M2ID	CA5260M	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC27M2IP	CA5260E	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC27M2MJG	CA5260E (PDIP)	Yes	Greater V_{OUT}/bandwidth/slew Rate
TLC555CD	ICM7555CBA	Yes	Reduced I_{CC}
TLC555IP	ICM7555IPA	Yes	Reduced I_{CC}
TLC556CN	ICM7556IPD	Yes	Reduced I_{CC}
TLC556IN	ICM7556IPD	Yes	Reduced I_{CC}
TLC556MJ	ICM7556MJD	Yes	Reduced I_{CC}
TP1321	HA-5195	Yes	
TP1322	HA-2520	Yes	
TP1326	HA-2600	Yes	
TP1332	HA-2645	Yes	
TP1339	HA-2620	No	
TP1341	HA-2840	Yes	
TP1342	HA-2839	Yes	
TP1344	HA-5160	Yes	
TP1345	HA-5162	Yes	
TP4856	HA1-2420/25	Yes	Guaranteed Acquisition Time
TP4866	HA1-5320	Yes	Guaranteed Acquisition Time
TSC7650ACPA	ICL7650SCPA-1	Yes	Reduced Tempco/voltage Noise
TSC7650ACPD	ICL7650SCPD	Yes	Reduced Tempco/voltage Noise
TSC7650AIJA	ICL7650SIJA-1	Yes	Reduced Tempco/voltage Noise
TSC7650AIJD	ICL7650SIJD	Yes	Reduced Tempco/voltage Noise
UC0P01CN	CA3140AE	Yes	Mosfet Input
UC0P01GJ	CA3140AE (PDIP)	Yes	Mosfet Input
ULN2046A-1	CA3146E	Yes	Full -40 To 85°C Operation
ULN2046L-1	CA3146M	Yes	
ULN2083A	CA3083	Yes	Full -55 To 125°C Operation
ULN2083A-1	CA3183E	Yes	Full -40 To 85°C Operation
ULN2083L	CA3083M	Yes	Full -55 To 125°C Operation
ULN2086A	CA3086	Yes	Full -55 To 125°C Operation
XR-13600AP	CA3280AE	No	Reduced V_{IO}/enhanced ACs
XR-13600CP	CA3280E	No	Reduced V_{IO}/enhanced ACs
XR-2242CP	ICM7242IPA	Yes	Greatly Reduced I_{CC}
XR-3403CP	CA5470E	Yes	Mos Input/enhanced ACs
XR-4739CN	HA7-5102-5	No	Enhanced ACs/DCs
XR-4739CP	HA3-5102-5	No	Enhanced ACs/DCs
XR-4741CN	HA1-4741-5	Yes	Guaranteed Channel Separation

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Commercial Linear Product Cross Reference

PART NUMBER	HARRIS DEVICE	PIN-TO-PIN	HARRIS ADVANTAGE/COMMENT
XR-4741CP	HA3-4741-5	Yes	Guaranteed Channel Separation
XR-4741M	HA1-4741-2	Yes	Guaranteed Channel Separation
XR-5532AN	HA7-5102-5	Yes	Reduced V_{IO}/I_{BIAS}
XR-5532AP	HA3-5102-5	Yes	Reduced V_{IO}/I_{BIAS}
XR-5532N	HA7-5102-5	Yes	Reduced V_{IO}/I_{BIAS}
XR-5532P	HA3-5102-5	Yes	Reduced V_{IO}/I_{BIAS}
XR-5534ACN	HA7-5101-5	†	Greater A_{VOL}/Reduced V_{IO}
XR-5534ACP	HA3-5101-5	†	Greater A_{VOL}/Reduced V_{IO}
XR-5534AM	HA7-5101-2	†	Greater A_{VOL}
XR-5534CN	HA7-5101-5	†	Greater A_{VOL}/reduced V_{IO}
XR-5534CP	HA3-5101-5	†	Greater A_{VOL}/reduced V_{IO}
XR-5534M	HA7-5101-2	†	Greater A_{VOL}
XR-8038CN	ICL8038CCJD	Yes	
XR-8038CP	ICL8038CCPD	Yes	
XR-8038M	ICL8038AMJD	Yes	
XR-8038N	ICL8038BCJD	Yes	
uPA103G	HFA3046B	Yes	Lower Cost
uPC357C	CA3130E	Yes	Reduced I_{BIAS}
uPC4741C	HA3-4741-5	Yes	Guaranteed Specs Over Temp
uPC4741G2	HA9P4741-9	†	Guaranteed Specs Over Temp
uPD5555C	ICM7555CPA	Yes	Reduced I_{CC}
uPD5556C	ICM7556CPD	Yes	Reduced I_{CC}

† Primary Pins are pin-to-pin; secondary/optional pins are not.

Data Acquisition Products

A/D CONVERTERS DISPLAY

CA3162/CA3162A	A/D Converter for $3^1/_2$-Digit Display
ICL71C03/ICL8052	Precision $4^1/_2$-Digit A/D Converter
ICL71C03/ICL8068	Precision $4^1/_2$-Digit A/D Converter
ICL7106	$3^1/_2$-Digit LCD Single-Chip A/D Converter
ICL7107	$3^1/_2$-Digit LED Single-Chip A/D Converter
ICL7116/7117	$3^1/_2$-Digit with Display Hold Single-Chip A/D Converter
ICL7126	$3^1/_2$-Digit Low Power Single-Chip A/D Converter
ICL7129	$4^1/_2$-Digit LCD Single-Chip A/D Converter
ICL7136	$3^1/_2$-Digit LCD Low Power A/D Converter
ICL7137	$3^1/_2$-Digit LED Low Power Single-Chip A/D Converter
ICL7139	$3^3/_4$-Digit Autoranging Multimeter
ICL7149	Low Cost $3^3/_4$-Digit Autoranging Multimeter

A/D CONVERTERS INTEGRATING

ICL7104/ICL8052	14/16-Bit µP-Compatible 2-Chip A/D Converter
ICL7104/ICL8068	14/16-Bit µP-Compatible 2-Chip A/D Converter
ICL7109	12-Bit µP-Compatible A/D Converter
ICL7135	$4^1/_2$-Digit BCD Output A/D Converter

A/D SUCCESSIVE APPROXIMATION

ADC0802/3/4	8-Bit µP-Compatible A/D Converter
CA3310/CA3310A	CMOS 10-Bit A/D Converter with Internal Track and Hold
HI-574A	Fast, Complete 12-Bit A/D Converter with Microprocessor Interface
HI5812	Low Power, Sampling 12-Bit A/D Converter
HI-674A	l2µs, Complete 12-Bit A/D Converter with Microprocessor Interface
HI-774	8µs Complete 12-Bit A/D Converter with Microprocessor Interface

A/D CONVERTERS FLASH

HI3304	4-Bit 25 MSPS A/D Converter
HI1826	6-Bit 140 MSPS A/D Converter
HI1866	6-Bit 140 MSPS A/D Converter
HI3306	6-Bit 15 MSPS A/D Converter
HI-5701	6-Bit 30 MSPS A/D Converter
HI3318	8-Bit 15 MSPS A/D Converter
HI1386	8-Bit 75 MSPS A/D Converter
HI1396	8-Bit 125 MSPS A/D Converter
HI1166	8-Bit 250 MSPS A/D Converter
HI1276	8-Bit 500 MSPS A/D Converter

D/A CONVERTERS

AD7520	10/12-Bit Multiplying DIA Converter
AD7521	10/12-Bit Multiplying DIA Converter
AD7530	10/12-Bit Multiplying DIA Converter

AD7531	10/12-Bit Multiplying D1A Converter
AD7523	8-Bit Multiplying D/A Converter
AD7533	10-Bit Multiplying D/A Converter
AD7541	12-Bit Multiplying D/A Converter
AD7545	12-Bit Buffered Multiplying CMOS DAC
HI-DAC80V	12-Bit, Low Cost, Monolithic D/A Converter
HI-DAC85V	12-Bit, Low Cost, Monolithic D/A Converter

D/A CONVERTERS HIGH SPEED

HI2304	Triple 8-Bit 20MHz D/A Converter
HI1106	8-Bit 35MHz D/A Converter
HI1260	Triple 8-Bit 35MHz D/A Converter
HI20206	Triple 8-Bit 35MHz D/A Converter
HI1171	8-Bit 40MHz CMOS D/A Converter
HI1178	Triple 8-Bit 40MHz D/A Converter
HI1177	Dual 8-Bit 40MHz D/A Converter
HI3338	8-Bit 50MHz D/A Converter
HI20203	8-Bit 160MHz D/A Converter
HI3050	Triple 10-Bit 50MHz D/A Converter
HI2307	Triple 10-Bit 50MHz D/A Converter

ANALOG SWITCHES

DG181	Dual SPST (30Ω) Switch
DG182	Dual SPST (75Ω) Switch
DG184	Dual DPST (30Ω) Switch
DG185	Dual DPST (75Ω) Switch
DG187	SPST (30Ω) Switch
DG188	SPST (75Ω) Switch
DG190	Dual SPST (30Ω) Switch
DG191	Dual SPST (75Ω) Switch
DG200	Dual SPST CMOS Analog Switch
DG201A	Quad Monolithic SPST CMOS Analog Switch
DG202	Quad Monolithic SPST CMOS Analog Switch
DG211	Quad Monolithic SPST CMOS Analog Switch
DG212	Quad Monolithic SPST CMOS Analog Switch
DG300A	Dual SPST TTL Compatible CMOS Analog Switch
DG301A	SPDT TTL Compatible CMOS Analog Switch
DG302A	Dual DPST TTL Compatible CMOS Analog Switch
DG303A	Dual SPDT TTL Compatible CMOS Analog Switch
DG308A	Quad Monolithic SPST CMOS Analog Switch
DG309	Quad Monolithic SPST CMOS Analog Switch
DG401/403/405	Dual CMOS Analog Switches
DG411/412/413	Quad SPST CMOS Analog Switches
DG441/442	Quad SPST CMOS Analog Switches
HI-200	Dual SPST CMOS Analog Switch
HI-201	Quad SPST CMOS Analog Switch

HI-201HS	High-Speed Quad SPST CMOS Analog Switch
HI-222	High Frequency Video Switch
HI-300	Dual SPST CMOS Analog Switch
HI-301	SPDT CMOS Analog Switch
HI-302	Dual DPST CMOS Analog Switch
HI-303	Dual SPDT CMOS Analog Switch
HI-304	Dual SPST CMOS Analog Switch
HI-305	SPDT CMOS Analog Switch
HI-306	Dual DPST CMOS Analog Switch
HI-307	Dual SPDT CMOS Analog Switch
HI-381	Dual SPST CMOS Analog Switch
HI-384	Dual DPST CMOS Analog Switch
HI-387	SPDT CMOS Analog Switch
HI-390	Dual SPDT CMOS Analog Switch
HI-5040	SPST CMOS Analog Switch
HI-5041	Dual SPST CMOS Analog Switch
HI-5042	SPDT CMOS Analog Switch
HI-5043	Dual SPDT CMOS Analog Switch
HI-5044	DPST CMOS Analog Switch
HI-5045	Dual DPST CMOS Analog Switch
HI-5046	DPDT CMOS Analog Switch
HI-5046A	DPDT CMOS Analog Switch
HI-5047	4PST CMOS Analog Switch
HI-5047A	4PST CMOS Analog Switch
HI-5048	Dual SPST CMOS Analog Switch
HI-5049	Dual DPST CMOS Analog Switch
HI-5050	SPDT CMOS Analog Switch
HI-5051	Dual SPDT CMOS Analog Switch
IH401A	Quad Varafet Analog Switch
IH5040	SPST 75 Ohm High-Level CMOS Analog Switch
IH5041	Dual SPST 75 Ohm High-Level CMOS Analog Switch
IH5042	SPDT 75 Ohm High-Level CMOS Analog Switch
IH5043	Dual SPDT 75 Ohm High-Level CMOS Analog Switch
IH5044	DPST 75 Ohm High-Level CMOS Analog Switch
IH5045	Dual DPST 75 Ohm High-Level CMOS Analog Switch
IH5046	DPDT 75 Ohm High-Level CMOS Analog Switch
IH5047	4PST 75 Ohm High-Level CMOS Analog Switch
IH5052	Quad SPST CMOS Analog Switch
IH5053	Quad SPST CMOS Analog Switch
IH5140	SPST High-Level CMOS Analog Switch
IH5141	Dual SPST High-Level CMOS Analog Switch
IH5142	SPDT High-Level CMOS Analog Switch
IH5143	Dual SPDT High-Level CMOS Analog Switch
IH5144	DPST High-Level CMOS Analog Switch
IH5145	Dual DPST High-Level CMOS Analog Switch

IH5148	Dual SPST High-Level CMOS Analog Switch
IH5149	Dual DPST High-Level CMOS Analog Switch
IH5150	SPDT High-Level CMOS Analog Switch
IH5151	Dual SPDT High-Level CMOS Analog Switch
IH5341	Dual SPST CMOS RF/Video Switch
IH5352	Quad SPST CMOS RF/Video Switch

MULTIPLEXERS

DG406/407	16-Channel/Dual 8-Channel CMOS Analog Multiplexer
DG408/409	Single 8-Channel/Differential 4-Channel CMOS Analog Multiplexers
DG506A	16-Channel/Dual 8-Channel CMOS Analog Multiplexer
DG507A	16-Channel/Dual 8-Channel CMOS Analog Multiplexer
DG508A	8-Channel/Dual 4-Channel CMOS Analog Multiplexer
DG509A	8-Channel/Dual 4-Channel CMOS Analog Multiplexer
DG526	16-Channel/Dual 8-Channel CMOS Latchable Multiplexer
DG527	16-Channel/Dual 8-Channel CMOS Latchable Multiplexer
DG528	8-Channel/Dual 4-Channel Latchable Multiplexer
DG529	8-Channel/Dual 4-Channel Latchable Multiplexer
HI-1818A/1828A	Low Resistance Single 8/Differential 4-Channel CMOS Analog Multiplexers
HI-506	Single 16/Differential 8-Channel CMOS Analog Multiplexer
HI-507	Single 16/Differential 8-Channel CMOS Analog Multiplexer
HI-506A	Single 16/Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-507A	Single 16/Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-508	Single 8/Differential 4-Channel CMOS Analog Multiplexer
HI-509	Single 8/Differential 4-Channel CMOS Analog Multiplexer
HI-508A	Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-509A	Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-516	16-Channel/Differential 8-Channel CMOS High-Speed Analog Multiplexer
HI-518	8-Channel/Differential 4-Channel CMOS High-Speed Analog Mulitplexer
HI-524	4-Channel Wideband and Video Multiplexer
HI-539	Monolithic, 4-Channel, Low Level, Differential Multiplexer
HI-546	Single 16/Differential 8-Channel CMOS Analog Mulitplexer with Active Overvoltage Protection
HI-547	Single 16/Differential 8-Channel CMOS Analog Mulitplexer with Active Overvoltage Protection
HI-548	Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-549	Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
IH6108	8-Channel CMOS Analog Multiplexer
IH6208	4-Channel Differential CMOS Analog Multiplexer

DISPLAY DRIVERS

CA3161	BCD to Seven Segment Decoder/Driver
CA3168	2-Digit BCD to Seven Segment Decoder/Driver
ICM7211	4-Digit LCD/LED Display Driver
ICM7212	4-Digit LCD/LED Display Driver
ICM7218	8-Digit LED Multiplexed Display Driver
ICM7228	8-Digit LED Multiplexed Display Driver
ICM7231	Numeric/Alphanumeric Triplexed LCD Display Driver

ICM7232	Numeric/Alphanumeric Triplexed LCD Display Driver
ICM7243	8-Character µP-Compatible LED Display Driver

REAL-TIME CLOCK

ICM7170	µP-Compatible Real-Time Clock

COUNTERS WITH DISPLAY DRIVERS/TIMEBASE GENERATORS

ICM7207/A	CMOS Timebase Generator
ICM7208	7-Digit LED Display Counter
ICM7209	Timebase Generator
ICM7213	One Second/One Minute Timebase Generator
ICM7216A/B/D	8-Digit Multi-Function Frequency Counter/Timer
ICM7217	4-Digit LED Display Programmable Up/Down Counter
ICM7224	$4^1/_2$-Digit LCD/LED Display Counter
ICM7226A/B	8-Digit Multi-Function Frequency Counter/Timer
ICM7249	$5^1/_2$-Digit LCD µ-Power Event/Hour Meter

SPECIAL PURPOSE

AD590	2-Wire Current Output Temperature Transducer
ICL8069	Low Voltage Reference

DATA COMMUNICATIONS

ICL232	+5 Volt Powered Dual RS-232 Transmitter/Receiver
HIN200	+5 Volt 5T/0R Powered Dual RS-232 Transmitter/Receiver
HIN201	+5 Volt 2T/2R Powered Dual RS-232 Transmitter/Receiver
HIN202	+5 Volt 2T/2R Powered Dual RS-232 Transmitter/Receiver
HIN204	+5 Volt 4T/0R Powered Dual RS-232 Transmitter/Receiver
HIN206	+5 Volt 4T/3R Powered Dual RS-232 Transmitter/Receiver
HIN207	+5 Volt 5T/3R Powered Dual RS-232 Transmitter/Receiver
HIN208	+5 Volt 4T/4R Powered Dual RS-232 Transmitter/Receiver
HIN209	+5 Volt 3T/5R Powered Dual RS-232 Transmitter/Receiver
HIN211	+5 Volt 4T/4R Powered Dual RS-232 Transmitter/Receiver
HIN213	+5 Volt 4T/5R Powered Dual RS-232 Transmitter/Receiver

Digital Signal Processing Products

MULTIPLIERS

HMA510	16 x 16-Bit CMOS Parallel Multiplier Accumulator
HMU16/HMU17	16 x 16-Bit CMOS Parallel Multipliers

ONE DIMENSIONAL FILTERS

DECI • MATE	Harris HSP43220 Decimating Digital Filter Development Software
HSP43124	Serial I/O Filter
HSP43168	Dual FIR Filter
HSP43216	Half Band Filter
HSP43220	Decimating Digital Filter
HSP43881	Digital Filter
HSP43891	Digital Filter

TWO DIMENSIONAL FILTERS

HSP48901	3 x 3 Image Filter
HSP48908	Two Dimensional Convolver

SIGNAL SYNTHESIZERS

HSP45102	12-Bit Numerically Controlled Oscillator
HSP45106	16-Bit Numerically Controlled Oscillator
HSP45116	Numerically Controlled Oscillator/Modulator
HSP45116A	Numerically Controlled Oscillator/Modulator
HSP45116-DB	HSP45116 Evaluation Daughter Board

SPECIAL FUNCTION

HSP45240	Address Sequencer
HSP45256	Binary Correlator
HSP48410	Histogrammer/Accumulating Buffer
HSP9501	Programmable Data Buffer
HSP9520/9521	Binary Correlator
HSP-EVAL	DSP Evaluation Platform

COMMUNICATIONS

HSP50016	Digital Down Converter
HSP50110	Digital Quadrature Tuner
HSP50210	Digital Costas Loop
HSP50110/210EVAL	Demo Chipset Evaluation Board
HSP50306	QPSK Demodulator (Note 1)
HSP50307	Burst QPSK Modulator (Note 1)
HSP50307EVAL	Burst QPSK Modulator Evaluation Board
HSP50214	Programmable Downconverter (Note 1)
HSP50215	Programmable Upconverter (Note 2)

NOTES:

1. New Product Offerings
2. New Product Offerings In Short Term Road Map

FOR MORE INFORMATION CONTACT YOUR LOCAL SALES OFFICE OR DISTRIBUTOR

LINEAR 3

OPERATIONAL AMPLIFIERS

Operational Amplifiers (Continued)

Operational Amplifiers (Continued)

Selection Guide

WIDEBAND: Min/Max Limits at 25°C, Unless Otherwise Specified

DEVICE	GBWP (TYP) (MHz)	FPBW (TYP) (MHz)	SLEW RATE (TYP) (V/μs)	A_{VOL} (dB)/ A_{ZOL} (V/mA)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/OP AMP)
BUFFERS										
HFA1112	850	260	2400	-	+1, -1, +2	25	35000	-	39	26.0
HFA1113	850	260	2400	-	+1, -1, +2	25	35000	-	39	26.0
HFA1114	**850**	**260**	**2400**	**-**	**+1, -1, +2**	**25**	**35000**	**-**	**39**	**26.0**
HFA1110	750	150	1300	-	+1	25	40000	-	39	26.0
HA4600	400	-	1700	-	+1	10	50000	-	-	13.0
HA-5033	250	17.5	1100	-	+1	15	35000	-	54	25.0
HFA1115	**225**	**140**	**1100**	**-**	**+1, -1, +2**	**10**	**15000**	**-**	**45**	**7.1**
HA-5002	110	20.7	1300	-	+1	20	7000	-	54	10.0
DUAL BUFFERS										
HFA1212	**340**	**140**	**1100**	**-**	**+1, -1, +2**	**10**	**15000**	**-**	**45**	**6.1**
QUAD BUFFERS										
HFA1412	**225**	**140**	**1100**	**-**	**+1, -1, +2**	**10**	**15000**	**-**	**45**	**6.1**
SINGLE OP AMPS										
HFA1100	850	300	2300	500 (Note 1)	1	6.0	40000	40	45	26.0
HFA1120	850	300	2300	500 (Note 1)	1	6.0	40000	40	45	26.0
HFA1130	850	300	2300	500 (Note 1)	1	6.0	40000	40	45	26.0
HA-2539	600	9.5	600	80	10	10.0	20000	60	60	25.0
HA-2839	600	10.0	625	86	10	2.0	14500	75	75	15.0
HA-2840	600	10.0	625	86	10	2.0	14500	75	75	15.0
HFA1109	**500**	**TBD**	**1200**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**10.0**
HFA1149	**500**	**TBD**	**1200**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**10.0**
HA-2850	470	5.4	340	86	10	2.0	14500	75	75	8.0
HA-2540	400	6.0	400	80	10	10.0	20000	60	60	25.0
HFA1105	**350**	**140**	**1000**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**6.1**
HFA1145	**350**	**140**	**1000**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**6.1**
HFA1135	**350**	**170**	**1200**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**7.1**
HFA1106	**315**	**100**	**700**	**500** (Note 1)	**1** (Note 2)	**5.0**	**15000**	**47**	**50**	**6.1**
HA-5190	150	6.5	200	83	5	5.0	15000	74	70	28.0
HA-5195	150	6.5	200	83	5	6.0	15000	74	70	28.0
HA-5147	140	0.5	35	117	10	0.1	80	100	86	4.0

NOTE: Bold type designates a new product from Harris.

WIDEBAND: Min/Max Limits at 25°C, Unless Otherwise Specified **(Continued)**

DEVICE	GBWP (TYP) (MHz)	FPBW (TYP) (MHz)	SLEW RATE (TYP) (V/µs)	A_{VOL} (dB)/ A_{ZOL} (V/mA)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/OP AMP)
HA-5147A	120	0.5	35	120	10	0.03	40	114	108	4.0
HA-5020	100	17.5	1100	3500 (Note 1)	1	8.0	8000	60	64	10.0
HA-2620	100	0.6	35	100	5 (Note 2)	4.0	15	80	80	3.7
HA-2622	100	0.6	35	98	5 (Note 2)	5.0	25	74	74	4.0
HA-2625	100	0.6	35	98	5 (Note 2)	5.0	25	74	74	4.0
HA-5111	100	0.8	50	120	10 (Note 2)	3.0	200	80	80	6.0
HA-5160	100	1.9	120	97	10 (Note 2)	3.0	0.05	74	74	10.0
HA-5162	100	1.10	70	88	10 (Note 2)	15.0	0.065	70	70	12.0
HA-5221	100	0.56	35	106	1	0.75	80	86	86	11.0
HA-2842C	**150**	**18.0**	**1200**	**94**	**2** (Note 2)	**3.0**	**10000**	**80**	**70**	**15.0**
HA-2842	80	6.0	400	94	2	3.0	10000	80	70	15.0
HA-2841	50	3.8	240	88	1	3.0	10000	80	70	11.0
DUAL OP AMPS										
HFA1245	**530**	**150**	**1050**	**500** (Note 1)	**1**	**5**	**15000**	**45**	**48**	**6.1**
HFA1205	**400**	**180**	**1275**	**500** (Note 1)	**1**	**5**	**15000**	**45**	**48**	**6.1**
HA5022	**125**	**28**	**475**	**1000** (Note 1)	**1**	**3.0**	**8000**	**53**	**60**	**10.0**
HA5023	**125**	**28**	**475**	**1000** (Note 1)	**1**	**3.0**	**8000**	**53**	**60**	**10.0**
HA-5222	100.0	0.56	35	106	1	0.75	80.0	86	86	11.0
HA-5112	60.0	0.32	20	100	10	2.0	200.0	86	86	2.5
TRIPLE OP AMPS										
HA5013	**125**	**28**	**475**	**3500** (Note 1)	**1**	**3.0**	**8000**	**53**	**60**	**10.0**
QUAD OP AMPS										
HFA1405	**400**	**TBD**	**1000**	**500** (Note 1)	**1**	**5**	**15000**	**45**	**48**	**6.1**
HA5024	**125**	**28**	**475**	**3500** (Note 1)	**1**	**3.0**	**8000**	**53**	**60**	**10.0**
HA5025	**125**	**28**	**475**	**3500** (Note 1)	**1**	**3.0**	**8000**	**53**	**60**	**10.0**
HA-5114	60.0	0.32	20.0	100	10	2.5	200.0	86	86	1.63
HA-2444	50.0	5.1	160	71	1	7.0	15000	70	65	6.25

NOTE: Bold type designates a new product from Harris.

WIDEBAND: Min/Max Limits at 25°C, Unless Otherwise Specified **(Continued)**

DEVICE	GBWP (TYP) (MHz)	FPBW (TYP) (MHz)	SLEW RATE (TYP) (V/μs)	A_{VOL} (dB)/ A_{ZOL} (V/mA)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/OP AMP)
HA-2400	40.0	0.95	30.0	94	10 (Note 2)	9.0	200.0	80	74	1.5
HA-2404	40.0	0.95	30.0	94	10 (Note 2)	9.0	200.0	80	74	1.5
HA-2405	40.0	0.95	30.0	94	10 (Note 2)	9.0	250.0	74	74	1.5

NOTES:

1. A_{ZOL} applies to current feedback amplifiers only (HA-5004, HA-502X, HFA11XX, HFA12XX, HFA14XX).
2. Product features an external compensation pin to limit bandwidth for noise reduction or to allow unity gain operation.

HIGH SLEW RATE: Min/Max Limits at 25°C, Unless Otherwise Specified

DEVICE	SLEW RATE (TYP) (V/μs)	GBWP (TYP) (MHz)	FPBW (TYP) (MHz)	A_{VOL} (dB)/ A_{ZOL} (V/mA)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/OP AMP)
BUFFERS										
HFA1112	2400	850	260	-	+1, -1, +2	25.0	35000	-	39	26.0
HFA1113	2400	850	260	-	+1, -1, +2	25.0	35000	-	39	26.0
HFA1114	**2400**	**850**	**260**	**-**	**+1, -1, +2**	**25**	**35000**	**-**	**39**	**26.0**
HA4600	1700	400	-	-	+1	10	50000	-	-	13.0
HFA1110	1300	750	150	-	+1	25.0	40000	-	39	26.0
HA-5002	1300	110	20.7	-	+1	20.0	7000	-	54	10.0
HFA1115	**1100**	**225**	**140**	**-**	**+1, -1, +2**	**10**	**15000**	**-**	**45**	**7.1**
HA-5033	1100	250	17.5	-	+1	15.0	35000	-	54	25.0
DUAL BUFFERS										
HFA1212	**1100**	**340**	**140**	**-**	**+1, -1, +2**	**10**	**15000**	**-**	**45**	**6.1**
QUAD BUFFERS										
HFA1412	**1100**	**225**	**140**	**-**	**+1, -1, +2**	**10**	**15000**	**-**	**45**	**6.1**
SINGLE OP AMPS										
HFA1100	2300	850	300	500 (Note 1)	1	6.0	40000	40	45	26.0
HFA1120	2300	850	300	500 (Note 1)	1	6.0	40000	40	45	26.0
HFA1130	2300	850	300	500 (Note 1)	1	6.0	40000	40	45	26.0
HFA1109	**1200**	**500**	**TBD**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**10.0**
HFA1149	**1200**	**500**	**TBD**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**10.0**
HFA1135	**1200**	**350**	**170**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**7.1**
HA-2842C	**1200**	**150**	**18.0**	**94**	**2** (Note 2)	**3.0**	**10000**	**80**	**70**	**15.0**

NOTE: Bold type designates a new product from Harris.

HIGH SLEW RATE: Min/Max Limits at 25°C, Unless Otherwise Specified **(Continued)**

DEVICE	SLEW RATE (TYP) (V/μs)	GBWP (TYP) (MHz)	FPBW (TYP) (MHz)	A_{VOL} (dB)/ A_{ZOL} (V/mA)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/OP AMP)
HA-5020	1100	100	17.5	3500 (Note 1)	1	8.0	8000	60	64	10.0
HFA1105	**1000**	**350**	**140**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**6.1**
HFA1145	**1000**	**350**	**140**	**500** (Note 1)	**1**	**5.0**	**15000**	**47**	**50**	**6.1**
HA-2839	625	600	10.0	86	10	2.0	14500	75	75	15.0
HA-2840	625	600	10.0	86	10	2.0	14500	75	75	15.0
HA-2539	600	600	9.5	80	10	10.0	20000	60	60	25.0
HA-2540	400	400	6.0	80	10	10.0	20000	60	60	25.0
HA-2842	400	80	6.0	94	2	3.0	10000	80	70	15.0
HA-2542	350	70	5.5	80	2 (Note 2)	10.0	35000	70	70	34.5
HA-2850	340	400	5.4	86	10	2.0	14500	75	75	8.0
HA-2841	240	50	3.8	88	1	3.0	10000	80	70	11.0
HA-2541	250	40	4.0	80	1	2.0	35000	70	70	40.0
HA-5190	200	150	6.5	83	5	5.0	15000	74	70	28.0
HA-5195	200	150	6.5	83	5	6.0	15000	74	70	28.0
HA-2544	150	50	4.2	71	1	15.0	15000	75	70	12.0
HA-2520	120	20	2	80	3 (Note 2)	8.0	200	80	80	6.0
HA-2522	120	20	2	78	3 (Note 2)	10.0	250	74	74	6.0
HA-2525	120	20	2	78	3 (Note 2)	10.0	250	74	74	6.0
HA-5160	120	100	1.9	97	10 (Note 2)	3.0	0.05	74	74	10.0
DUAL OP AMPS										
HFA1205	**1275**	**400**	**140**	**500** (Note 1)	**1**	**5**	**15000**	**45**	**48**	**6.1**
HFA1245	**1050**	**530**	**130**	**500** (Note 1)	**1**	**5**	**15000**	**45**	**48**	**6.1**
HA5022	**475**	**125**	**28**	**1000** (Note 1)	**1**	**3.0**	**8000**	**53**	**60**	**10.0**
HA5023	**475**	**125**	**28**	**1000** (Note 1)	**1**	**3.0**	**8000**	**53**	**60**	**10.0**
CA3280	125	9.0	1.99	94	1	3.0	5000	80	86	2.4
CA3280A	125	9.0	1.99	94	1	0.5	5000	94	94	2.4
TRIPLE OP AMPS										
HA5013	**475**	**125**	**28**	**3500** (Note 1)	**1**	**3.0**	**8000**	**53**	**60**	**10.0**

NOTE: Bold type designates a new product from Harris.

HIGH SLEW RATE: Min/Max Limits at 25°C, Unless Otherwise Specified **(Continued)**

DEVICE	SLEW RATE (TYP) (V/μs)	GBWP (TYP) (MHz)	FPBW (TYP) (MHz)	A_{VOL} (dB)/ A_{ZOL} (V/mA)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/OP AMP)
QUAD OP AMPS										
HFA1405	**1000**	**400**	**TBD**	**500 (Note 1)**	**1**	**5.0**	**15000**	**45**	**48**	**6.1**
HA5024	**475**	**125**	**28**	**3500 (Note 1)**	**1**	**3.0**	**8000**	**53**	**60**	**10.0**
HA5025	**475**	**125**	**28**	**3500 (Note 1)**	**1**	**3.0**	**8000**	**53**	**60**	**10.0**
HA-2444	160	50	5.1	71	1	7.0	15000	70	65	6.25

NOTES:

1. A_{ZOL} applies to current feedback amplifiers only (HA-5004, HA-502X, HFA11XX, HFA12XX, HFA14XX).
2. Product features an external compensation pin to limit bandwidth for noise reduction or to allow unity gain operation.

VIDEO: Typical Values at 25°C, Unless Otherwise Specified

DEVICE	FEATURES	DIF. GAIN (%)	DIF. PHASE (DEG)	0.1dB FLAT GAIN (MHz)	GBWP (MHz)	SLEW RATE (V/μs)	OUTPUT CURRENT (mA)	SUPPLY VOLTAGE RANGE (±V)	SUPPLY CURRENT (mA/OP AMP)
BUFFERS									
HA4600	**Video Buffer w/Output Disable**	**0.01**	**0.01**	**250**	**480**	**1700**	**20**	**4.5 - 5.5**	**10.5**
HFA1110	+1, Std. Buffer Pinout	0.02	0.02	>100	750	1300	60	4.5 - 5.5	21.0
HFA1112	-1, +1, +2 (Selectable) Standard Op Amp Pinout	0.02	0.04	>100	850	2400	60	4.5 - 5.5	21.0
HFA1113	**-1, +1, +2 (Selectable) Standard Op Amp Pinout, V_{OUT} Limits**	**0.02**	**0.04**	**>100**	**850**	**2400**	**60**	**4.5 - 5.5**	**21.0**
HFA1114	**-1, +1, +2 (Selectable) Summing Node Pinout**	**0.02**	**0.04**	**>100**	**850**	**1100**	**60**	**4.5 - 5.5**	**21.0**
HFA1115	-1, +1, +2 (Selectable) Standard Op Amp Pinout, V_{OUT} Limits	0.02	0.03	>50	225	1100	60	4.5 - 5.5	5.9
HA-5033	+1, Std. Buffer Pinout	0.03	0.02	-	250	1100	100	5 - 16	21.0
HA-5002	+1, Std. Buffer Pinout	0.06	0.21	-	110	1300	200	5 - 20	8.3
DUAL BUFFERS									
HFA1212	**-1, +1, +2 (Selectable)**	**0.02**	**0.02**	**>50**	**340**	**1100**	**60**	**4.5 - 5.5**	**5.9**
QUAD BUFFERS									
HFA1412	**-1, +1, +2 (Selectable)**	**0.02**	**0.02**	**>50**	**225**	**1100**	**60**	**4.5 - 5.5**	**5.9**
SINGLE OP AMPS									
HFA1109	**$A_V \geq 1$, CFB, Wideband**	**0.02**	**0.03**	**100**	**500**	**1200**	**30**	**4.5 - 5.5**	**10.0**
HFA1149	**$A_V \geq 1$, CFB, Programmable Output Disable**	**0.02**	**0.03**	**100**	**500**	**1200**	**30**	**4.5 - 5.5**	**10.0**
HFA1105	**$A_V \geq 1$, Low I_{CC}, CFB**	**0.02**	**0.03**	**>50**	**350**	**1000**	**60**	**4.5 - 5.5**	**5.9**
HFA1145	**$A_V \geq 1$, Low I_{CC}, CFB, Output Disable**	**0.02**	**0.03**	**>50**	**350**	**1000**	**60**	**4.5 - 5.5**	**5.9**
HFA1135	**$A_V \geq 1$, Low I_{CC}, CFB, Programmable Output Limiting**	**0.02**	**0.04**	**>50**	**360**	**1200**	**60**	**4.5 - 5.5**	**6.9**

NOTE: Bold type designates a new product from Harris.

VIDEO: Typical Values at 25°C, Unless Otherwise Specified **(Continued)**

DEVICE	FEATURES	DIF. GAIN (%)	DIF. PHASE (DEG)	0.1dB FLAT GAIN (MHz)	GBWP (MHz)	SLEW RATE (V/μs)	OUTPUT CURRENT (mA)	SUPPLY VOLTAGE RANGE (±V)	SUPPLY CURRENT (mA/OP AMP)
HFA1106	**HFA1105 with Compensation Pin for Bandwidth Limiting**	**0.02**	**0.05**	**100**	**315**	**700**	**60**	**4.5 - 5.5**	**5.9**
HA-2842	$A_V \geq 2$, Cable Driver	0.02	0.03	>10	80	400	100	6 - 17	14.2
HA-5020	$A_V \geq 1$, Output Disable, CFB (Current Feedback)	0.02	0.03	5	100	1100	32	4.5 - 18	7.5
HFA1100	$A_V \geq 1$, CFB	0.03	0.05	75	850	2300	60	4.5 - 5.5	21.0
HFA1120	HFA1100 with Offset Adjust	0.03	0.05	75	850	2300	60	4.5 - 5.5	21.0
HFA1130	$A_V \geq 1$, CFB, Programmable Output Limiting	0.03	0.05	75	850	2300	60	4.5 - 5-5	21.0
HA-2544	$A_V \geq 1$	0.03	0.03	5	50	150	35	8 - 17	10.0
HA-2841	$A_V \geq 1$, Low I_{CC}	0.03	0.03	>10	50	240	30	6 - 17	10.0
DUAL OP AMPS									
HFA1245	**$A_V \geq 1$, Low I_{CC}, CFB, Output Disable**	**0.02**	**0.03**	**50**	**530**	**1050**	**60**	**4.5 - 5.5**	**5.9**
HFA1205	**$A_V \geq 1$, Low I_{CC}, CFB**	**0.03**	**0.03**	**>50**	**400**	**1275**	**60**	**4.5 - 5.5**	**5.9**
HA5022	**$A_V \geq 1$, CFB, Output Disable**	**0.03**	**0.03**	**20**	**125**	**475**	**20**	**4.5 - 18**	**7.5**
HA5023	**$A_V \geq 1$, CFB**	**0.03**	**0.03**	**20**	**125**	**475**	**20**	**4.5 - 18**	**7.5**
TRIPLE OP AMPS									
HA5013	**$A_V \geq 1$, CFB**	**0.03**	**0.03**	**20**	**125**	**475**	**20**	**4.5 - 18**	**7.5**
QUAD OP AMPS									
HFA1405	**$A_V \geq 1$, Low I_{CC}, CFB**	**0.03**	**0.03**	**TBD**	**400**	**>1000**	**60**	**4.5 - 5.5**	**5.9**
HA5024	**$A_V \geq 1$, CFB, Output Disable**	**0.03**	**0.03**	**20**	**125**	**475**	**20**	**4.5 - 18**	**7.5**
HA5025	**$A_V \geq 1$, CFB**	**0.03**	**0.03**	**20**	**125**	**475**	**20**	**4.5 - 18**	**7.5**
HA-2444	$A_V \geq 1$, 4-Channel, Mux'd Output	0.03	0.03	10	50	160	25	8.5 - 17	5.0

NOTES:

1. Single Supply Range.

LOW NOISE: Min/Max Limits at 25°C, Unless Otherwise Specified

DEVICE	NOISE VOLTAGE 1kHz (TYP) ($nV/\sqrt{Hz}$)	NOISE CURRENT 1kHz (TYP) ($pA/\sqrt{Hz}$)	GBWP (TYP) (MHz)	SLEW RATE (TYP) (V/μs)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	SUPPLY CURRENT (mA/OP AMP)
SINGLE OP AMPS								
HA-5127A	3.0	0.4	8.5	10	1	0.025	40	4.0
HA-5137A	3.0	0.4	63	20	5	0.025	40	4.0
HA-5147A	3.0	0.4	120	35	10	0.025	40	4.0
HA-5101	3.0	0.6	10	10	1	3.0	200	6.0
HA-5111	3.0	0.6	100	50	10	3.0	200	6.0
HA-5221	3.4	0.97	100	35	1	0.75	80	11.0
HA-5020	4.5	2.5 (Note 1)	100	1100	1	8.0	8000 (Note 1)	10.0

NOTE: Bold type designates a new product from Harris.

LOW NOISE: Min/Max Limits at 25°C, Unless Otherwise Specified **(Continued)**

DEVICE	NOISE VOLTAGE 1kHz (TYP) (nV/√Hz)	NOISE CURRENT 1kHz (TYP) (pA/√Hz)	GBWP (TYP) (MHz)	SLEW RATE (TYP) (V/µs)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	SUPPLY CURRENT (mA/OP AMP)
HFA1105	**3.5**	**2.5** (Note 1)	**350**	**1000**	**1**	**5.0**	**15000**	**6.1**
HFA1106	**3.5**	**2.5** (Note 1)	**315**	**700**	**1** (Note 2)	**5.0**	**15000**	**6.1**
HFA1135	**3.5**	**2.5** (Note 1)	**350**	**1200**	**1**	**5.0**	**15000**	**6.1**
HFA1145	**3.5**	**2.5** (Note 1)	**350**	**1000**	**1**	**5.0**	**15000**	**7.1**
HA-5190	6.0	5.0	150	200	5	5.0	15000	28.0
HA-2839	6.0	6.0	600	625	10	2.0	14500	15.0
HA-2840	6.0	6.0	600	625	10	2.0	14500	15.0
HA-2539	6.0	6.0	600	600	10	10.0	20000	25.0
HA-2540	6.0	6.0	400	400	10	10.0	20000	25.0
HA-5170	10.0	0.01	8.0	8.0	1	0.3	0.1	2.5
HA-2542	10.0	3.0	70	350	2 (Note 2)	10.0	35000	34.5
HA-2541	10.0	4.0	40	250	1	2.0	35000	40.0
DUAL OP AMPS								
HA-5222	3.4	0.97	100	35	1	0.75	80	11.0
HFA1205	**3.5**	**2.5** (Note 1)	**400**	**1275**	**1**	**5.0**	**15000**	**6.1**
HFA1245	**3.5**	**2.5** (Note 1)	**530**	**1050**	**1**	**5.0**	**15000**	**6.1**
HA-5102	4.3	0.57	8.0	3.0	1	2.0	200	2.5
HA-5112	4.3	0.57	60	20	10	2.0	200	2.5
HA5022	**4.5**	**2.5** (Note 1)	**125**	**475**	**1**	**3.0**	**8000** (Note 1)	**10.0**
HA5023	**4.5**	**2.5** (Note 1)	**125**	**475**	**1**	**3.0**	**8000** (Note 1)	**10.0**
QUAD OP AMPS								
HFA1405	**3.5**	**2.5** (Note 1)	**400**	**>1000**	**1**	**5.0**	**15000**	**6.1**
HA-5104	4.3	0.57	8.0	3.0	1	2.5	200	1.63
HA-5114	4.3	0.57	60	20	10	2.5	200	1.63
HA5024	**4.5**	**2.5** (Note 1)	**125**	**475**	**1**	**3.0**	**8000** (Note 1)	**10.0**
HA5025	**4.5**	**2.5** (Note 1)	**125**	**475**	**1**	**3.0**	**8000** (Note 1)	**10.0**
HA-5134	7.0	1.0	4.0	1.0	1	0.2	50	2.0

NOTES:

1. +Input. These are current feedback amplifiers, so value for -Input will be larger.
2. Product features an external compensation pin to limit bandwidth for additional noise reduction or to allow unity gain operation.

NOTE: Bold type designates a new product from Harris.

GENERAL PURPOSE: Typical Values at 25°C, Unless Otherwise Specified

DEVICE	DESCRIPTION	MINIMUM STABLE GAIN	GBWP (MHz)	SLEW RATE (V/μs)	OFFSET VOLTAGE (mV)	BIAS CURRENT (μA)	SUPPLY VOLTAGE RANGE (±V)	SUPPLY CURRENT (mA/OP AMP)
SINGLE OP AMPS								
HA-2544	Ultra-Stable, High Performance	1	50	150	6.0	7.00	8-17.5	10.0
CA3100	Wideband Amplifier	1	38	70	1.0	0.7	7-18	8.5
CA3130A	BiMOS, CMOS Output, Output Strobe	1	15	30	2.0	5.0pA	2.5-8	2.0
HA-2500	Wideband, High Slew Rate, High Input Impedance	1	12	30	2.0	0.1	10-20	4.0
HA-2510	Wideband, High Slew Rate, High Input Impedance	1	12	60	4.0	0.1	10-20	4.0
HA-2600	Wideband, Compensated, High Input Impedance	1	12	7	0.5	0.001	4-22.5	3.0
HA-5101	Low Noise, High Performance	1	10	10	0.5	0.1	3-20	4.0
HA-5127A	Low Noise, Precision, Compensated	1	8.5	10	0.01	0.01	5-22	3.5
HA-5170	JFET Input, Precision	1	8	8	0.1	20pA	5-22	1.9
CA3140A	BiMOS, Output Strobe Capability	1	4.5	9	2.0	10.0pA	2-18	4.0
HA-2640	High Voltage, Compensated	1	4	5	2.0	0.01	10-50	3.2
CA3160A	BiMOS, CMOS Output, Output Strobe	1	4	10	2.0	5.0pA	2.5-8	2.0
CA3080	Operational Transconductance Amp	1	2	75	0.4	2.0	2-18	1.0
CA741	Low Cost, Mil/Com Temp	1	1	0.5	1.0	0.08	5-22	1.7
LM741	Low Cost, Mil/Com Temp	1	1	0.5	1.0	0.08	5-22	1.7
HA-2520	Uncompensated	3 (Note 1)	20	120	5.0	0.125	10-20	4.0
HA-5137A	Low Noise, Precision	5	80	20	0.01	0.01	5-22	3.5
HA-2620	Wideband, Uncompensated, High Input Impedance	5 (Note 1)	100	35	0.5	0.001	4-22.5	3.0
HA-5195	Wideband, Fast Settling	5	150	200	3.0	5.0	12-17.5	19.0
HA-5147A	Low Noise, Precision, Wideband	10	140	35	0.01	0.01	5-22	3.5
HA-5111	Low Noise, High Performance, Uncompensated	10 (Note 1)	100	50	0.5	0.1	3-20	4.0
DUAL								
CA3280A	Operational Transconductance Amp	1	9	125	0.25	1.8	2-18	2.0
HA-5102	Low Noise, High Performance	1	8	3	0.5	0.13	3-20	1.5
CA3240A	BiMOS, High Input Impedance	1	4.5	9	2.0	10.0pA	2-18	4.0
CA3260A	BiMOS, CMOS Output, High Input Impedance	1	4	10	2.0	5.0pA	2-8	0.6
CA5260A	Mil Temp Version of CA3260A	1	3	5	2.0	5.0pA	2.25-8	0.6
CA158A	Wide Supply Range, Mil Temp	1	1	0.25	1.0	0.02	1.5-16	0.75
CA1558	Low Cost, Mil Temp Range	1	1	0.5	1.0	0.08	5-22	1.7

NOTE: Bold type designates a new product from Harris.

GENERAL PURPOSE: Typical Values at 25°C, Unless Otherwise Specified **(Continued)**

DEVICE	DESCRIPTION	MINIMUM STABLE GAIN	GBWP (MHz)	SLEW RATE (V/μs)	OFFSET VOLTAGE (mV)	BIAS CURRENT (μA)	SUPPLY VOLTAGE RANGE (±V)	SUPPLY CURRENT (mA/OP AMP)
LM358	Wide Supply Range, Low Cost	1	1	0.5	2.0	0.05	1.5 - 16	0.7
LM1458	Low Cost	1	1	0.5	2.0	0.08	5-18	1.7
LM2904	Wide Supply Range, Ind. Temp	1	1	0.5	2.0	0.05	1.5 - 13	0.7
HA-5112	Low Noise, High Performance, Uncompensated	10	60	20	0.5	0.13	3-20	1.5
QUAD								
CA5470	High Input Impedance, Wide Supply Range, Mil Temp	1	14	5	5.0	1.0pA	1.5-8	2.5
HA-5104	Low Noise, High Performance	1	8	3	0.5	0.13	3-20	1.25
CA124	Wide Supply Range, Mil Temp	1	1	0.5	2.0	0.045	2.5-16	0.2
HA-4741	Quad 741, Wide Supply	1	3.5	1.6	0.5	0.06	2-20	4.5
HA-5114	Low Noise, High Performance, Uncompensated	10	60	20	0.5	0.13	3-20	1.25
LM2902	Low Cost, Ind. Temp	1	1	0.5	2.0	0.04	2.5 - 16	0.2
LM324	Low Cost	1	1	0.5	2.0	0.05	2.5 - 16	0.2

NOTE:

1. Can be compensated to unity gain.

PRECISION: Min/Max Limits at 25°C, Unless Otherwise Specified

DEVICE	OFFSET VOLTAGE (mV)	V_{IO} DRIFT (TYP) (μV/°C)	BIAS CURRENT (nA)	OFFSET CURRENT (nA)	CMRR (dB)	PSRR (dB)	GBWP (TYP) (MHz)	SLEW RATE (TYP) (V/μs)	A_{VOL} (dB)	SUPPLY CURRENT (mA/OP AMP)
SINGLE OP AMPS										
ICL7650S	0.005	0.02	0.01	0.02	120	120	2.0	2.5	135	3.0
HA-5127A	0.025	0.20	40.0	35.0	114	108	8.5	10.0	120	4.0
HA-5130	0.025	0.40	2.0	2.0	110	100	2.5	0.8	120	1.7
HA-5137A	0.025	0.20	40.0	35.0	114	108	63.0	20.0	120	4.0
HA-5147A	0.025	0.20	40.0	35.0	114	108	120.0	35.0	120	4.0
HA-5135	0.075	0.40	4.0	4.0	106	94	2.5	0.8	120	1.7
HA-5137	0.100	0.40	80.0	75.0	100	96	63.0	20.0	117	4.0
HA-5147	0.100	0.40	80.0	75.0	100	96	120.0	35.0	117	4.0
HA-5170	0.300	2.0	0.1	0.03	85	85	8.0	8.0	109	2.5
HA-5221	0.750	0.5	80.0	50.0	86	86	100.0	35.0	106	11.0
DUAL OP AMPS										
HA-5222	0.75	0.5	80	50	86	86	100.0	35.0	106	11.0
CA158A	2.0	7.0	50	10	70	65	1.0	0.5	94	1.5
HA-5102	2.0	3.0	200	75	86	86	8.0	3.0	100	2.5
HA-5112	2.0	3.0	200	75	86	86	60.0	20.0	100	2.5
ICL7621A	2.0	10.0	0.05	0.03	76	80	0.5	0.16	86	0.25

NOTE: Bold type designates a new product from Harris.

PRECISION: Min/Max Limits at 25°C, Unless Otherwise Specified **(Continued)**

DEVICE	OFFSET VOLTAGE (mV)	V_{IO} DRIFT (TYP) (μV/°C)	BIAS CURRENT (nA)	OFFSET CURRENT (nA)	CMRR (dB)	PSRR (dB)	GBWP (TYP) (MHz)	SLEW RATE (TYP) (V/μs)	A_{VOL} (dB)	SUPPLY CURRENT (mA/OP AMP)
CA3280A	0.5	3.0	5000	700	94	94	9.0	125.0	94	2.4
CA258A	3.0	7.0	80	15	70	65	1.0	0.5	94	1.5
CA358A	3.0	7.0	100	30	65	65	1.0	0.5	88	1.5
HA-5142	6.0	3.0	100.0	10.0	77	77	0.4	1.5	86	0.15
QUAD OP AMPS										
HA-5134	0.2	0.3	50.0	50.0	100	100	4.0	1.0	118	2.0
HA-5114	2.5	3.0	200.0	75.0	86	86	60.0	20.0	100	1.63
HA-5104	2.5	3.0	200.0	75.0	86	86	8.0	3.0	100	1.63
CA124	5.0	7.0	150.0	30.0	70	65	1.0	0.5	94	0.5
HA-5144	6.0	3.0	100.0	10.0	77	77	0.4	1.5	86	0.15
CA224	7.0	7.0	250.0	50.0	65	65	1.0	0.5	88	0.5
CA324	7.0	7.0	250.0	50.0	65	65	1.0	0.5	86	0.5
CA2902	7.0	7.0	250.0	50.0	65	65	1.0	0.5	86	0.3

LOW BIAS CURRENT: Min/Max Limits at 25°C, Unless Otherwise Specified

DEVICE	BIAS CURRENT (nA)	OFFSET CURRENT (nA)	OFFSET VOLTAGE (mV)	CM RANGE AT NOMINAL SUPPLIES (V)	A_{VOL} (dB)	GBWP (TYP) (MHz)	SLEW RATE (TYP) (V/μs)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA/OP AMP)
SINGLE OP AMPS										
CA5420A	0.001	0.0005	5.0	-0 to +3.7 at +5, -0	85	0.5	0.5	75	75	0.5
CA5420	0.002	0.001	10.0	-0 to +3.7 at +5, -0	85	0.5	0.5	70	70	0.5
ICL7650S	0.01	0.02	0.005	-5 to +3.5 at +5, -5	135	2.0	2.5	120	120	3.0
CA3130A	0.03	0.02	5.0	-0 to +10.0 at +15, -0	94	15.0	30.0	80	76	15.0
HA-5160	0.05	0.01	3.0	-10.0 to +10.0 at +15, -15	98	100.0	120	74	74	10.0
HA-5170	0.10	0.03	0.3	-10.0 to +10.0 at +15, -15	110	8.0	8.0	90	90	2.5
DUAL OP AMPS										
CA5260	0.015	0.01	15.0	-0 to +2.5 at +5, -0	80	3.0	5.0	70	70	1.0
CA5260A	0.015	0.01	4.0	-0 to +2.5 at +5, -0	83	3.0	5.0	80	75	1.0
CA3260A	0.03	0.02	5.0	-0 to +10.0 at +15, -0	94	4.0	10.0	80	76	1.5
CA3240A	0.04	0.02	5.0	-15 to +12.0 at +15, -15	86	4.5	9.0	70	76	6.0
CA3240	0.05	0.03	15.0	-15 to +11.0 at +15, -15	86	4.5	9.0	70	76	6.0
CA3260	0.05	0.03	15.0	-0 to +10.0 at +15, -0	94	4.0	10.0	70	70	1.5
ICL7621A	0.05	0.03	2.0	-4.2 to +4.2 at +5, -5	86	0.5	0.16	76	80	0.25
CA158A	50.0	10.0	2.0	-15 to +13.5 at +15, -15	94	1.0	0.5	70	65	1.5
QUAD OP AMPS										
CA5470	0.05	0.05	25.0	-0 to +3.5 at +5, -0	80	14.0	5.0	55	60	3.0
ICL7641	0.05	0.03	10.0	-3.7 to +3.7 at +5, -5	76	1.4	1.6	60	70	2.5
ICL7642	0.05	0.03	10.0	-4.4 to +4.4 at +5, -5	80	0.04	0.02	70	80	0.03
HA-5134	50.0	50.0	0.2	-10 to +10 at +15, -15	118	4.0	1.0	100	100	2.0

NOTE: Bold type designates a new product from Harris.

5V SINGLE-SUPPLY: Min/Max Limits at 25°C, Unless Otherwise Specified

DEVICE	SUPPLY CURRENT (TYP) (mA/OP AMP)	INPUT OFFSET VOLTAGE (mV)	DOES INPUT INCLUDE GROUND?	RAIL-TO-RAIL OUTPUT?	INPUT BIAS CURRENT (nA)	GAIN BANDWIDTH PRODUCT (TYP) (MHz)	SLEW RATE (TYP) (V/µs)	MINIMUM SINGLE SUPPLY VOLTAGE (V)	OUTPUT SHORT CIRCUIT CURRENT (TYP) (mA) SOURCE = + SINK = - SUPPLY AT 5V, 0V
SINGLE OP AMPS									
ICL7612A	0.01	2	Yes	Yes	0.05	0.04	0.016	2.0	+12.5, -0.8
ICL7611A	0.01	2	No	Yes	0.05	0.04	0.016	2.0	+12.5, -0.8
ICL7612D	0.01	15	Yes	Yes	0.05	0.04	0.016	2.0	+12.5, -0.8
ICL7611D	0.01	15	No	Yes	0.05	0.04	0.016	2.0	+12.5, -0.8
CA3078A (Note 1)	0.025	3.5	No	No	12	1.5	0.5	1.5	+12.0, -12.0
CA3078 (Note 1)	0.13	4.5	No	No	170	8	1.5	1.5	+12.0, -12.0
CA3130A (Note 1)	0.30	5	Yes	Yes	0.03	15	10	5.0	+3.2, -2.2
CA3130 (Note 1)	0.30	15	Yes	Yes	0.05	15	10	5.0	+3.2, -2.2
CA3160A (Note 1)	0.30	5	Yes	Yes	0.03	4	10	5.0	+3.2, -2.2
CA3160 (Note 1)	0.30	15	Yes	Yes	0.05	4	10	5.0	+3.2, -2.2
CA5420A	0.40	5	Yes	Yes	0.001	0.5	0.5	2.0	+2.6, -2.4
CA5420	0.40	10	Yes	Yes	0.002	0.5	0.5	2.0	+2.6, -2.4
CA3140A (Note 1)	1.60	5	Yes	No	0.04	3.7	9	4.0	+10.0, -1.0
CA3140 (Note 1)	1.60	15	Yes	No	0.05	3.7	9	4.0	+10.0, -1.0
HFA1100	**5.5**	**6.0**	**No**	**No**	**40000**	**300**	**500**	**4.5**	**-**
DUAL OP AMPS									
HA-5142	0.05	6	Yes	No	100	0.4	1.5	3.0	+4.5, -4.5
ICL7621A (Note 1)	0.10	2	No	Yes	0.05	0.5	0.16	2.0	+12.5, -0.4
ICL7621D (Note 1)	0.10	15	No	Yes	0.05	0.5	0.16	2.0	+12.5, -0.4
CA158A	0.35	3	Yes	No	100	1	0.5	3.0	+40, -20
CA358	0.35	7	Yes	No	250	1	0.5	3.0	+40, -20
CA3260A (Note 1)	0.60	5	Yes	Yes	0.03	4	10	4.0	+3.2, -2.2
CA3260 (Note 1)	0.60	15	Yes	Yes	0.05	4	10	4.0	+3.2, -2.2
CA5260A	0.80	4	Yes	Yes	0.015	3	5	4.5	+2.2, -2.0
CA5260	0.80	15	Yes	Yes	0.015	3	5	4.5	+2.2, -2.0

NOTE: Bold type designates a new product from Harris.

5V SINGLE-SUPPLY: Min/Max Limits at 25°C, Unless Otherwise Specified **(Continued)**

DEVICE	SUPPLY CURRENT (TYP) (mA/OP AMP)	INPUT OFFSET VOLTAGE (mV)	DOES INPUT INCLUDE GROUND?	RAIL-TO-RAIL OUTPUT?	INPUT BIAS CURRENT (nA)	GAIN BANDWIDTH PRODUCT (TYP) (MHz)	SLEW RATE (TYP) (V/µs)	MINIMUM SINGLE SUPPLY VOLTAGE (V)	OUTPUT SHORT CIRCUIT CURRENT (TYP) (mA) SOURCE = + SINK = - SUPPLY AT 5V, 0V
CA3240A (Note 1)	2.00	5	Yes	No	0.04	3.7	9	5.0	+20.0, -1.0
CA3240 (Note 1)	2.00	15	Yes	No	0.05	3.7	9	5.0	+20.0, -1.0
QUAD OP AMPS									
ICL7642C	0.01	10	No	Yes	0.05	0.044	0.016	2.0	+10.0, -0.05
ICL7642E	0.01	20	No	Yes	0.05	0.044	0.016	2.0	+12.5, -0.05
HA-5144	0.05	6	Yes	No	100	0.4	1.5	3.0	+4.5, -4.5
CA324	0.20	7	Yes	No	250	1	0.5	5.0	+40, -20
CA124	0.20	5	Yes	No	150	1	0.5	5.0	+40, -20
ICL7641C (Note 1)	1.00	10	No	Yes	0.05	1.4	1.6	5.0	+12.5, -0.8
ICL7641E (Note 1)	1.00	20	No	Yes	0.05	1.4	1.6	5.0	+12.5, -0.8
CA5470	1.50	22	Yes	No	0.05	14	5	3.0	+5.5, -1.2

NOTES:

1. Limits are for single 5V operation if data is available in datasheet.
2. Supply Current for single 5V supply, if specified in datasheet.

LOW POWER: Min/Max Limits at 25°C, Unless Otherwise Specified (Note 1)

DEVICE	SUPPLY CURRENT (mA/OP AMP)	SUPPLY VOLTAGE RANGE (±V)	SLEW RATE (TYP) (V/µs)	GBWP (TYP) (MHz)	CM RANGE AT NOMINAL SUPPLY (V)	OUTPUT VOLTAGE SWING (V)	OUTPUT SHORT CIRCUIT CURRENT (TYP) (mA) SOURCE = + SINK = -	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	PSRR (dB)
SINGLE OP AMPS										
CA3078A	0.02	0.75-18	0.5	1.5	-5 to +5 at +6, -6	±5.1	±12.0	3.5	12.0	70
ICL7611A	0.02	1.0-9.0	0.02	0.044	-4.4 to +4.4 at +5, -5	±4.9	+25.0, -7.0	2.0	0.05	80
ICL7612A	0.02	1.0-9.0	0.02	0.044	-5.3 to +5.3 at +5, -5	±4.9	+25.0, -7.0	2.0	0.05	80
CA3078	0.13	0.75-7.0	1.5	8.0	-5 to +5 at +6, -6	±5.1	±12.0	4.5	170.0	70
CA5420A	0.55	1.0-11.0	0.5	0.5	-0 to +3.7 at +5, -0	+4.9, +0.15	+2.6, -2.4	5.0	0.005	70
DUAL OP AMPS										
HA-5142	0.15	1.5-17.5	1.5	0.4	-0 to +3.0 at +5, -0	+3.8, +1.0	+4.5, -4.5	6.0	100	77
ICL7621A	0.25	1.0-9.0	0.16	0.5	-4.2 to +4.2 at +5, -5	±4.9	+15.0, -0.9	2.0	0.05	80
CA158A	1.5	1.5-16.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15.0	+40.0, -20	2.0	50.0	65
CA258A	1.5	1.5-16.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15.0	+40.0, -20	3.0	80.0	65

NOTE: Bold type designates a new product from Harris.

LOW POWER: Min/Max Limits at 25°C, Unless Otherwise Specified (Note 1) **(Continued)**

DEVICE	SUPPLY CURRENT (mA/OP AMP)	SUPPLY VOLTAGE RANGE (±V)	SLEW RATE (TYP) (V/µs)	GBWP (TYP) (MHz)	CM RANGE AT NOMINAL SUPPLY (V)	OUTPUT VOLTAGE SWING (V)	OUTPUT SHORT CIRCUIT CURRENT (TYP) (mA) SOURCE = + SINK = -	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	PSRR (dB)
CA2904	1.5	1.5-13.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15.0	+40.0, -20	7.0	250.0	50
CA258	1.5	1.5-16.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15.0	+40.0, -20	5.0	150.0	65
CA358	1.5	1.5-16.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15.0	+40.0, -20	7.0	250.0	65
CA158	1.5	1.5-16.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15.0	+40.0, -20	5.0	150.0	65
CA358A	1.5	1.5-16.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15.0	+40.0, -20	3.0	100.0	65
CA3260A	1.5	2.0-8.0	10	4	-0 to +10 at +15, -0	+14.99, +0.01	+22.0, -20	5.0	0.03	77
CA5260A	2.0	2.25-8.0	5.0	3.0	-0 to +2.5 at +5, -0	+4.99, +0.01	+2.2, -2.0	5.0	0.030	76
QUAD OP AMPS										
ICL7642	0.02	1.0-9.0	0.02	0.04	-4.4 to +4.4 at +5, -5	±4.5	+10, -0.08	10.0	0.05	80
HA-5144	0.15	1.5-17.5	1.5	0.4	-0 to +3 at +5, -0	+3.8, +1.0	+4.5, -4.5	6.0	100.0	77
CA124	0.5	2.5-16.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15	+40.0, -20	5.0	150.0	65
CA224	0.5	2.5-16.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15	+40.0, -20	7.0	250.0	65
CA324	0.5	2.5-16.0	0.5	1.0	-15 to +13.5 at +15, -15	+13.5, -15	+40.0, -20	7.0	250.0	65
ICL7641	2.5	1.5-9.0	1.6	1.4	-3.7 to +3.7 at +5, -5	±4.5	+25, -7.0	10.0	0.05	80

NOTE:

1. See "CM Range" column for the Nominal Supply Voltage at which these specifications apply.

NOTE: Bold type designates a new product from Harris.

HARRIS SEMICONDUCTOR

CA124, CA224, CA324, LM324, LM2902

Quad, 1MHz, Operational Amplifiers for Commercial, Industrial, and Military Applications

November 1996

Features

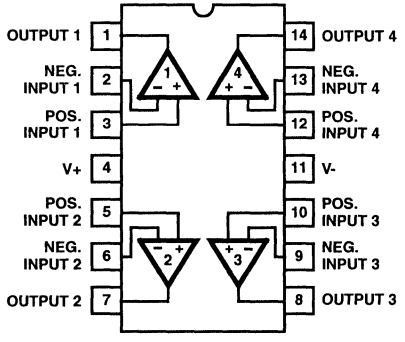
- Operation from Single or Dual Supplies
- Unity-Gain Bandwidth . . . . . 1MHz (Typ)
- DC Voltage Gain . . . . . 100dB (Typ)
- Input Bias Current . . . . . 45nA (Typ)
- Input Offset Voltage . . . . . 2mV (Typ)
- Input Offset Current
  - CA224, CA324, LM324, LM2902 . . . . . 5nA (Typ)
  - CA124 . . . . . 3nA (Typ)
- Replacement for Industry Types 124, 224, 324

Applications

- Summing Amplifiers
- Multivibrators
- Oscillators
- Transducer Amplifiers
- DC Gain Blocks

Pinout

CA124, CA224, CA324, LM2902 (PDIP, SOIC)
LM324 (PDIP)
TOP VIEW



Description

The CA124, CA224, CA324, LM324, and LM2902 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specially to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range from 0V to V+ -1.5V (single-supply operation) make these devices suitable for battery operation.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA0124E	-55 to 125	14 Ld PDIP	E14.3
CA0124M (124)	-55 to 125	14 Ld SOIC	M14.15
CA0124M96 (124)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15
CA0224E	-40 to 85	14 Ld PDIP	E14.3
CA0224M (224)	-40 to 85	14 Ld SOIC	M14.15
CA0224M96 (224)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15
CA0324E	0 to 70	14 Ld PDIP	E14.3
CA0324M (324)	0 to 70	14 Ld SOIC	M14.15
CA0324M96 (324)	0 to 70	14 Ld SOIC Tape and Reel	M14.15
LM324N	0 to 70	14 Ld PDIP	E14.3
LM2902N	-40 to 85	14 Ld PDIP	E14.3
LM2902M (2902)	-40 to 85	14 Ld SOIC	M14.15
LM2902M96 (2902)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 796.3

Absolute Maximum Ratings

Supply Voltage . . . . . 32V or ±16V
Differential Input Voltage. 32V
Input Voltage. . . . . -0.3V to 32V
Input Current (V_I < -0.3V, Note 1) 50mA
Output Short Circuit Duration (V+ ≤ 15V, Note 2) . . . . . Continuous

Operating Conditions

Temperature Range
CA124 . . . . . -55°C to 125°C
CA224, LM2902 . . . . . -40°C to 85°C
CA324, LM324 . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PDIP Package	100
SOIC Package	175

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

NOTES:

1. This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.
2. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Values Apply for Each Operational Amplifier. Supply Voltage V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	CA124			CA224, CA324, LM324			LM2902			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 6)		25	-	2	5	-	2	7	-	-	-	mV
		Full	-	-	7	-	-	9	-	-	10	mV
Average Input Offset Voltage Drift	R_S = 0Ω	Full	-	7	-	-	7	-	-	7	-	µV/°C
Differential Input Voltage (Note 5)		Full	-	-	V+	-	-	V+	-	-	V+	V
Input Common Mode Voltage Range (Note 5)	V+ = 30V	25	0	-	V+ -1.5	0	-	V+ -1.5	-	-	-	V
	V+ = 30V	Full	0	-	V+ -2	0	-	V+ -2	-	-	-	V
	V+ = 26V	Full	-	-	-	-	-	-	0	-	V+ -2	V
Common Mode Rejection Ratio	DC	25	70	85	-	65	70	-	-	-	-	dB
Power Supply Rejection Ratio	DC	25	65	100	-	65	100	-	-	-	-	dB
Input Bias Current (Note 4)	I_I+ or I_I-	25	-	45	150	-	45	250	-	-	-	nA
	I_I+ or I_I-	Full	-	-	300	-	-	500	-	40	500	nA
Input Offset Current	I_I+ - I_I-	25	-	3	30	-	5	50	-	-	-	nA
	I_I+ - I_I-	Full	-	-	100	-	-	150	-	45	200	nA
Average Input Offset Current Drift		Full	-	10	-	-	10	-	-	10	-	pA/°C

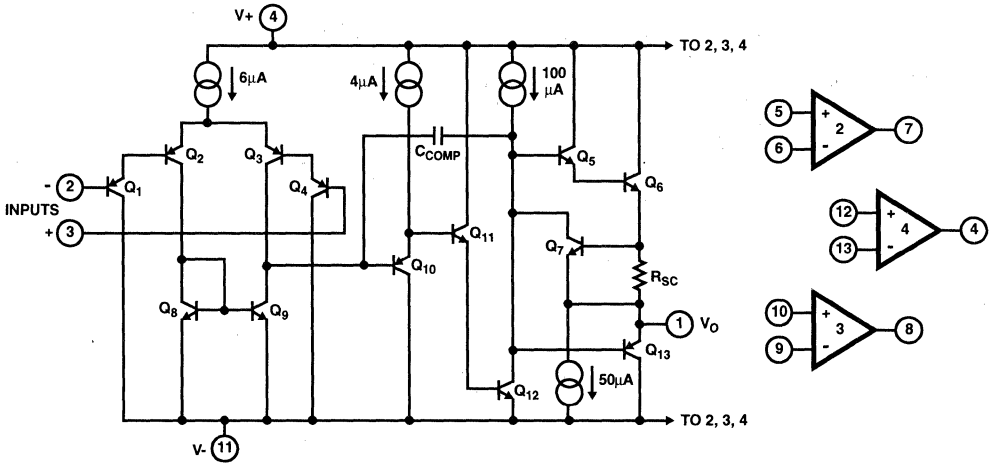
Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage V+ = 5V, V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER		TEST CONDITIONS	TEMP. (°C)	CA124			CA224, CA324, LM324			LM2902			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V+ = 15V (For Large V_O Swing)	25	94	100	-	88	100	-	-	-	-	dB
		$R_L \geq 2k\Omega$, V+ = 15V (For Large V_O Swing)	Full	88	-	-	83	-	-	83	-	-	dB
Output Voltage Swing		$R_L = 2k\Omega$	25	0	-	V+ -1.5	0	-	V+ -1.5	-	-	-	V
	High Level	$R_L = 2k\Omega$, V+ = 30V	Full	26	-	-	26	-	-	-	-	-	V
		$R_L = 2k\Omega$, V+ = 26V	Full	-	-	-	-	-	-	22	-	-	V
		$R_L = 10k\Omega$, V+ = 30V	Full	27	28	-	27	28	-	23	28	-	V
	Low Level	$R_L = 10k\Omega$	Full	-	5	20	-	5	20	-	5	100	mV
Output Current	Source	$V_I+ = +1V$, $V_I- = 0V$, V+ = 15V	25	20	40	-	20	40	-	-	-	-	mA
		$V_I+ = 1V$, $V_I- = 0$, V+ = 15V	Full	10	20	-	10	20	-	10	20	-	mA
	Sink	$V_I+ = 0V$, $V_I- = 1V$, V+ = 15V	25	10	20	-	10	20	-	-	-	-	mA
		$V_I+ = 0V$, $V_I- = 1V$, $V_O = 200mV$	25	12	50	-	12	50	-	-	-	-	µA
		$V_I- = 1V$, $V_I+ = 0$, V+ = 15V	Full	5	8	-	5	8	-	5	8	-	mA
Crosstalk		f = 1 to 20kHz (Input Referred)	25	-	-120	-	-	-120	-	-	-	-	dB
Total Supply Current		$R_L = \infty$	Full	-	0.8	2	-	0.8	2	-	0.7	1.2	mA
		$R_L = \infty$, V+ = 26V	Full	-	-	-	-	-	-	-	1.5	3	mA

NOTES:

4. Due to the PNP input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.
5. The input signal voltage and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
6. $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V, and over the full input common mode voltage range (0V to V+ - 1.5V).

Schematic Diagram (One of Four Operational Amplifiers)



Typical Performance Curves

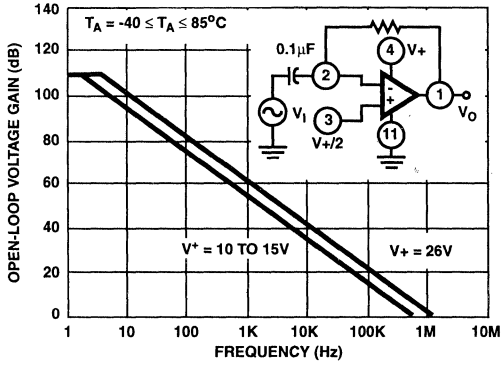


FIGURE 1. OPEN LOOP FREQUENCY RESPONSE

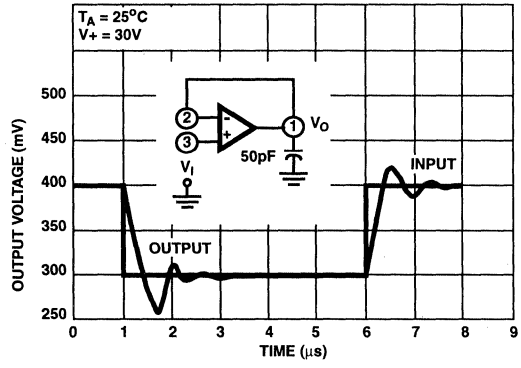


FIGURE 2. VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

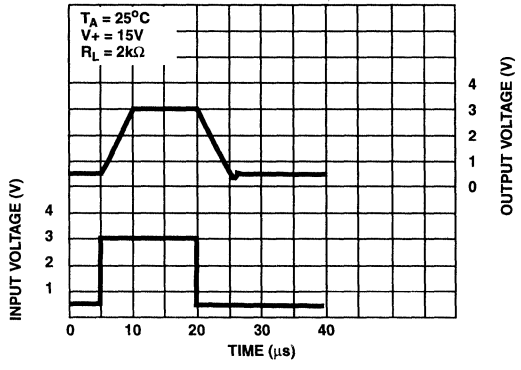


FIGURE 3. VOLTAGE FOLLOWER PULSE RESPONSE (LARGE SIGNAL)

Typical Performance Curves (Continued)

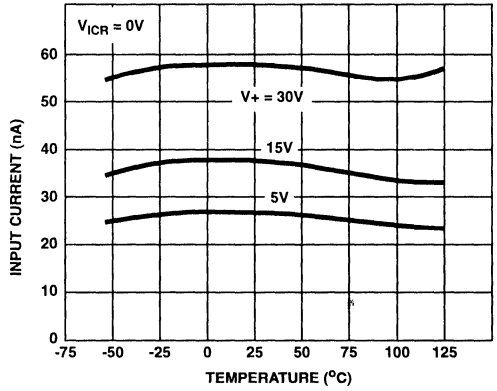


FIGURE 4. INPUT CURRENT vs AMBIENT TEMPERATURE

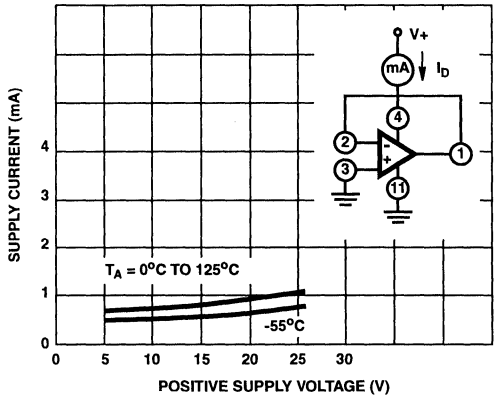


FIGURE 5. SUPPLY CURRENT vs SUPPLY VOLTAGE

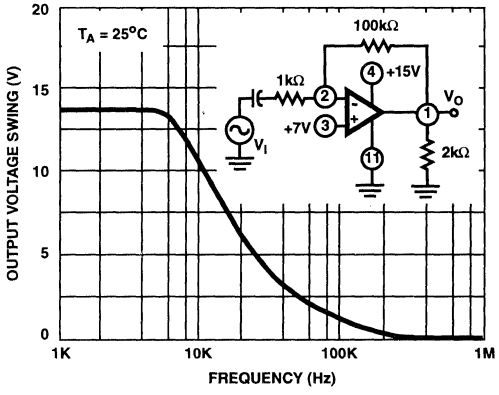


FIGURE 6. LARGE SIGNAL FREQUENCY RESPONSE

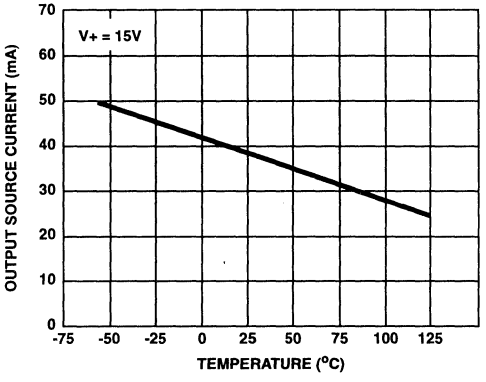


FIGURE 7. OUTPUT CURRENT vs AMBIENT TEMPERATURE

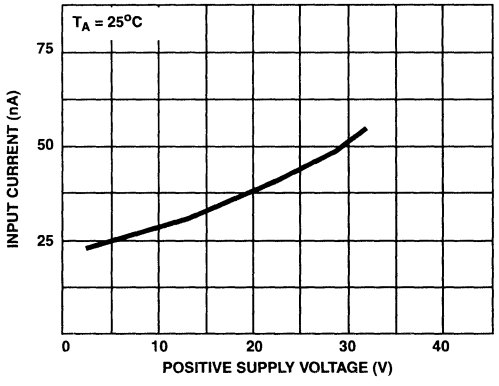


FIGURE 8. INPUT CURRENT vs SUPPLY VOLTAGE

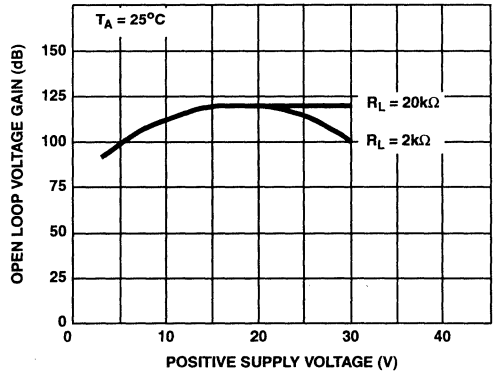


FIGURE 9. VOLTAGE GAIN vs SUPPLY VOLTAGE

HARRIS SEMICONDUCTOR

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

Dual, 1MHz, Operational Amplifiers for Commercial Industrial, and Military Applications

June 1996

Features

- Internal Frequency Compensation for Unity Gain
- High DC Voltage Gain ..... 100dB (Typ)
- Wide Bandwidth at Unity Gain ..... 1MHz (Typ)
- Wide Power Supply Range:
  - Single Supply ..... 3V to 30V
  - Dual Supplies ..... ±1.5V to ±15V
- Low Supply Current ..... 1.5 mA (Typ)
- Low Input Bias Current
- Low Input Offset Voltage and Current
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range Equal to V+ Range
- Large Output Voltage Swing ..... 0V to V+ -1.5V

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA0158E	-55 to 125	8 Ld PDIP	E8.3
CA0158AE	-55 to 125	8 Ld PDIP	E8.3
CA0158M	-55 to 125	8 Ld SOIC	M8.15
CA0158M96	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA0158T	-55 to 125	8 Pin Can	T8.C
CA0158AT	-55 to 125	8 Pin Can	T8.C
CA0258E	-25 to 85	8 Ld PDIP	E8.3
CA0258AE	-25 to 85	8 Ld PDIP	E8.3
CA0258M	-25 to 85	8 Ld SOIC	M8.15
CA0258M96	-25 to 85	8 Ld SOIC Tape and Reel	M8.15
CA0258AM	-25 to 85	8 Ld SOIC	M8.15
CA0258AM96	-25 to 85	8 Ld SOIC Tape and Reel	M8.15
CA0258T	-25 to 85	8 Pin Can	T8.C
CA0258AT	-25 to 85	8 Pin Can	T8.C
CA0358E	0 to 70	8 Ld PDIP	E8.3
CA0358AE	0 to 70	8 Ld PDIP	E8.3
CA0358M	0 to 70	8 Ld SOIC	M8.15
CA0358AM	0 to 70	8 Ld SOIC	M8.15
CA0358M96	0 to 70	8 Ld SOIC Tape and Reel	M8.15
CA0358AM96	0 to 70	8 Ld SOIC Tape and Reel	M8.15
CA0358T	0 to 70	8 Pin Can	T8.C
CA0358AT	0 to 70	8 Pin Can	T8.C
CA2904E	-40 to 85	8 Ld PDIP	E8.3
CA2904M	-40 to 85	8 Ld SOIC	M8.15
CA2904M96	-40 to 85	8 Ld SOIC Tape and Reel	M8.15
LM358N	0 to 70	8 Ld PDIP	E8.3
LM2904N	0 to 70	8 Ld PDIP	E8.3

Description

The CA158, CA158A, CA258, CA258A, CA358, CA358A and CA2904 types consist of two independent, high gain, internally frequency compensated operational amplifiers which are designed specifically to operate from a single power supply over a wide range of voltages. They may also be operated from split power supplies. The supply current is basically independent of the supply voltage over the recommended voltage range.

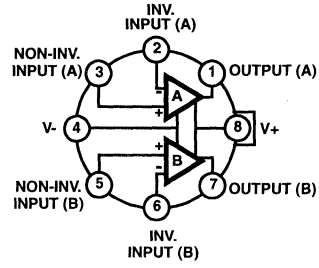
These devices are particularly useful in interface circuits with digital systems and can be operated from the single common $5V_{DC}$ power supply. They are also intended for transducer amplifiers, DC gain blocks and many other conventional op amp circuits which can benefit from the single power supply capability.

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are an equivalent to or a replacement for the industry types 158, 158A, 258, 258A, 358, 358A, and CA2904.

Technical Data on LM Branded types is identical to the corresponding CA Branded types.

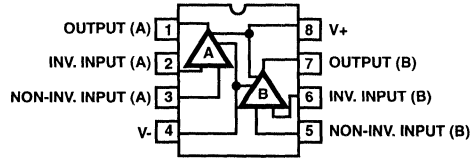
Pinouts

CA158, CA258, CA358 (METAL CAN)
TOP VIEW



CA158, CA258, CA358, CA2904 (PDIP, SOIC)
LM358, LM2904 (PDIP)

TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1019.3**

Absolute Maximum Ratings

Supply Voltage
- CA2904, LM2904 ..... 26V or ±13V
- Other Types ..... 32V or ±16V

Differential Input Voltage (All Types) 32V
Input Voltage ..... -0.3V to V+
Input Current (V_I < -0.3V, Note 1) 50mA
Output Short Circuit Duration (V+ ≤ 15V, Note 2) ..... Continuous

Operating Conditions

Temperature Range
- CA158, CA158A ..... -55°C to 125°C
- CA258, CA258A ..... -25°C to 85°C
- CA2904, LM2904 ..... -40°C to 85°C
- CA358, CA358A, LM358 ..... 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	130	N/A
SOIC Package	170	N/A
Can Package	155	67

Maximum Junction Temperature (Can Package) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.
2. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Values Apply for Each Operational Amplifier. Supply Voltage V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	CA158A			CA258A			CA358A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 6)		25	-	1	2	-	1	3	-	2	3	mV
		Full	-	-	4	-	-	4	-	-	5	mV
Average Input Offset Voltage Drift	R_S = 0Ω	Full	-	7	15	-	7	15	-	7	20	µV/°C
Input Common Mode Voltage Range (Note 5)	V+ = 30V	25	0	-	V+ -1.5	0	-	V+ -1.5	0	-	V+ -1.5	V
	V+ = 30V	Full	0	-	V+ -2	0	-	V+ -2	0	-	V+ -2	V
Common Mode Rejection Ratio	DC	25	70	85	-	70	85	-	65	85	-	dB
Power Supply Rejection Ratio	DC	25	65	100	-	65	100	-	65	100	-	dB
Input Bias Current (Note 4)	I_I+ or I_I-	25	-	20	50	-	40	80	-	45	100	nA
	I_I+ or I_I-	Full	-	40	100	-	40	100	-	40	200	nA
Input Offset Current	I_I+ - I_I-	25	-	2	10	-	2	15	-	5	30	nA
	I_I+ - I_I-	Full	-	-	30	-	-	30	-	-	75	nA
Average Input Offset Current Drift		Full	-	10	200	-	10	200	-	10	300	pA/°C
Large Signal Voltage Gain	R_L ≥ 2kΩ, V+ = 15V (For Large V_O Swing)	25	50	100	-	50	100	-	25	100	-	kV/V

Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage V+ = 5V, V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	CA158A			CA258A			CA358A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Swing	R_L = 2kΩ	25	0	-	V+ -1.5	0	-	V+ -1.5	0	-	V+ -1.5	V
Output Current Source	V_I+ = +1V, V_I- = 0V, V+ = 15V	25	20	40	-	20	40	-	20	40	-	mA
Output Current Sink	V_I+ = 0V, V_I- = 1V, V+ = 15V	25	10	20	-	10	20	-	10	20	-	mA
	V_I+ = 0V, V_I- = 1V, V_O = 200mV	25	12	50	-	12	50	-	12	50	-	µA
Short Circuit Output Current (Note 2)	R_L = 0Ω	25	-	40	60	-	40	60	-	40	60	mA
Crosstalk	f = 1 to 20kHz (Input Referred)	25	-	-120	-	-	-120	-	-	-120	-	dB
Total Supply Current	R_L = ∞	Full	-	0.7	1.2	-	0.7	1.2	-	0.7	1.2	mA
	R_L = ∞, V+ = 30V	Full	-	1.5	3	-	1.5	3	-	1.5	3	mA

NOTES:

4. Due to the PNP input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.
5. The input signal voltage and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
6. V_O = 1.4V, R_S = 0Ω with V+ from 5V to 30V, and over the full input common mode voltage range (0V to V+ - 1.5V).

Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	CA158, CA258			CA358, LM358			CA2904, LM2904			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 9)		25	-	2	5	-	2	7	-	2	7	mV
		Full	-	-	7	-	-	9	-	-	10	mV
Average Input Offset Voltage Drift	R_S = 0Ω	Full	-	7	-	-	7	-	-	7	-	µV/°C
Input Common Mode Voltage Range (Note 8)	V+ = 30V	25	0	-	V+ -1.5	0	-	V+ -1.5	0	-	V+ -1.5	V
	V+ = 30V	Full	0	-	V+ -2	0	-	V+ -2	0	-	V+ -2	V
Common Mode Rejection Ratio	DC	25	70	85	-	65	70	-	50	70	-	dB
Power Supply Rejection Ratio	DC	25	65	100	-	65	100	-	50	100	-	dB
Input Bias Current (Note 7)	I_I+ or I_I-	25	-	45	150	-	45	250	-	45	250	nA
	I_I+ or I_I-	Full	-	40	300	-	40	500	-	40	500	nA
Input Offset Current	I_I+ - I_I-	25	-	3	30	-	5	50	-	5	50	nA
	I_I+ - I_I-	Full	-	-	100	-	-	150	-	45	200	nA
Average Input Offset Current Drift		Full	-	10	-	-	10	-	-	10	-	pA/°C

Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage V+ = 5V, V- = 0V, Unless Otherwise Specified **(Continued)**

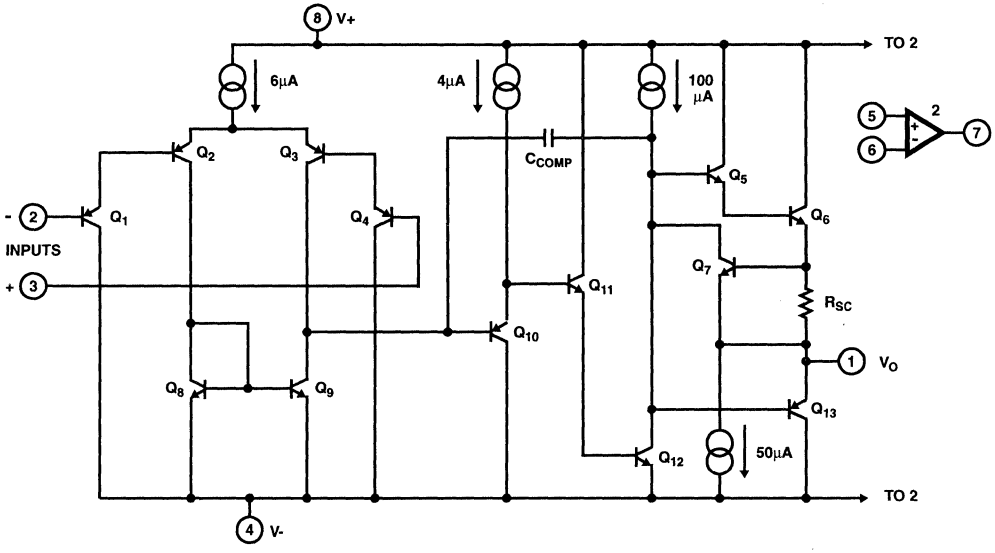
PARAMETER	TEST CONDITIONS	TEMP (°C)	CA158, CA258			CA358, LM358			CA2904, LM2904			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V+ = 15V (For Large V_O Swing)	25	50	100	-	25	100	-	-	100	-	kV/V
Output Voltage Swing	$R_L = 2k\Omega$	25	0	-	V+ -1.5	0	-	V+ -1.5	0	-	V+ -1.5	V
Output Current Source	$V_I+ = +1V$, $V_I- = 0V$, V+ = 15V	25	20	40	-	20	40	-	20	40	-	mA
Sink	$V_I+ = 0V$, $V_I- = 1V$, V+ = 15V	25	10	20	-	10	20	-	10	20	-	mA
	$V_I+ = 0V$, $V_I- = 1V$, $V_O = 200mV$	25	12	50	-	12	50	-	-	-	-	µA
Short Circuit Output Current (Note 2)	$R_L = 0\Omega$	25	-	40	60	-	40	60	-	40	60	mA
Crosstalk	f = 1 to 20kHz (Input Referred)	25	-	-120	-	-	-120	-	-	-120	-	dB
Total Supply Current	$R_L = \infty$	Full	-	0.7	1.2	-	0.7	1.2	-	0.7	1.2	mA
	$R_L = \infty$, V+ = 30V	Full	-	1.5	3	-	1.5	3	-	1.5	3	mA

NOTES:

7. Due to the PNP input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.
8. The input signal voltage and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
9. $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V, and over the full input common mode voltage range (0V to V+ - 1.5V).

Schematic Diagram

ONE OF TWO OPERATIONAL AMPLIFIERS



Typical Performance Curves

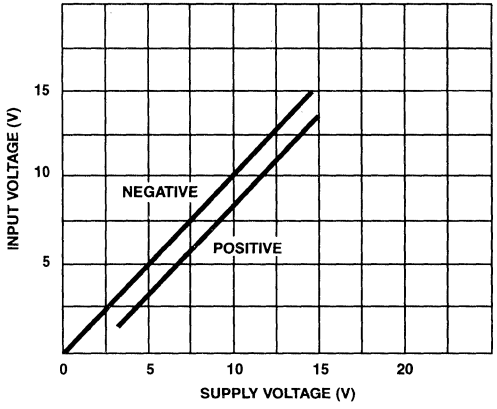


FIGURE 1. INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

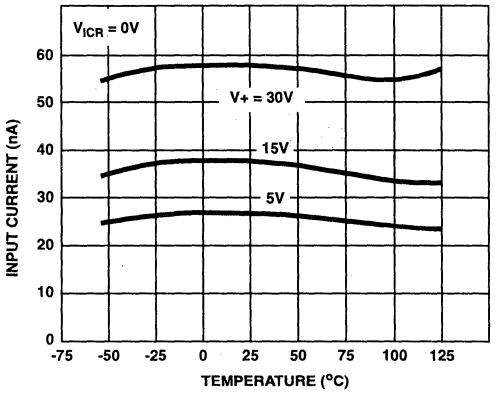


FIGURE 2. INPUT CURRENT vs AMBIENT TEMPERATURE

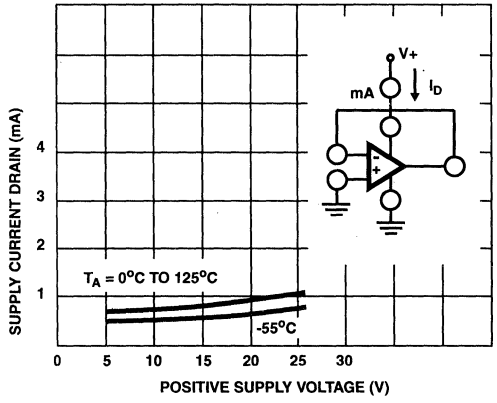


FIGURE 3. SUPPLY CURRENT DRAIN vs SUPPLY VOLTAGE

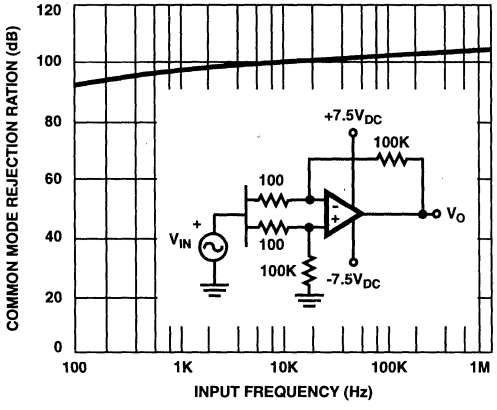


FIGURE 4. COMMON MODE REJECTION RATIO vs INPUT FREQUENCY

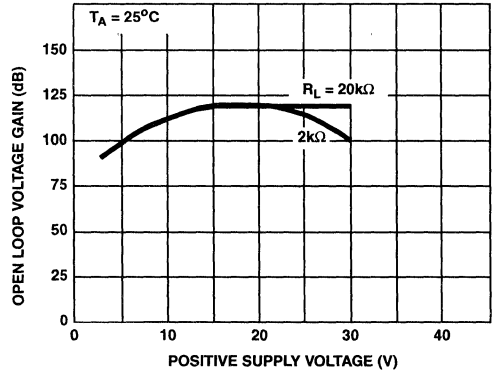


FIGURE 5. VOLTAGE GAIN vs SUPPLY VOLTAGE

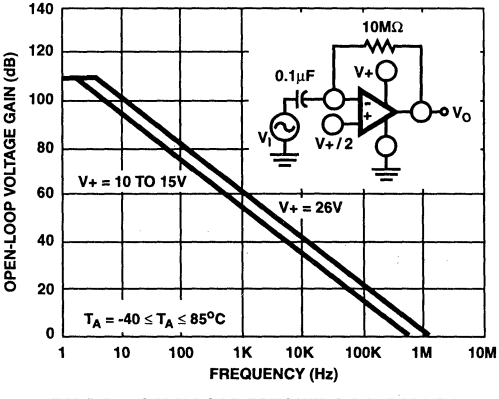


FIGURE 6. OPEN-LOOP FREQUENCY RESPONSE

Typical Performance Curves (Continued)

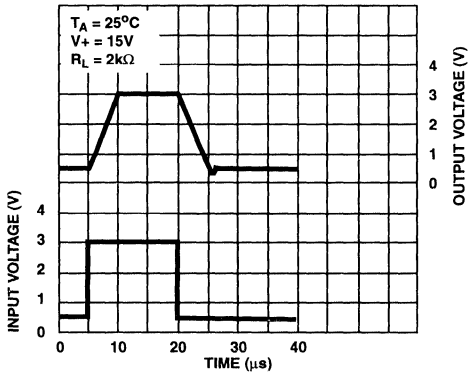


FIGURE 7. VOLTAGE FOLLOWER PULSE RESPONSE (LARGE SIGNAL)

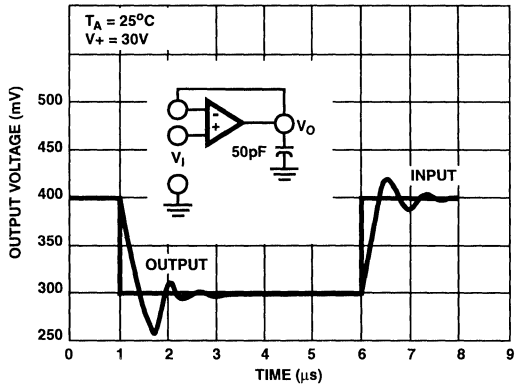


FIGURE 8. VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

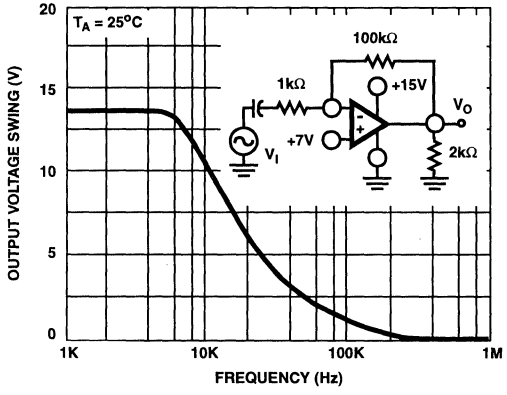


FIGURE 9. LARGE-SIGNAL FREQUENCY RESPONSE

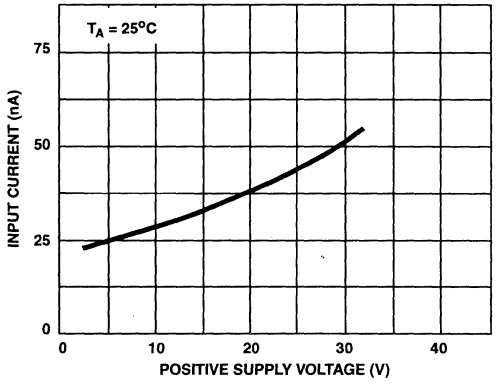


FIGURE 10. INPUT CURRENT vs SUPPLY VOLTAGE

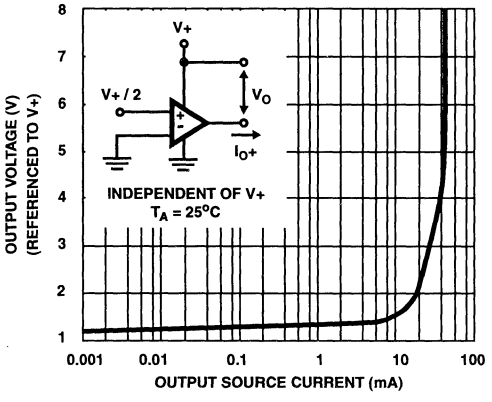


FIGURE 11. OUTPUT SOURCE CURRENT CHARACTERISTICS

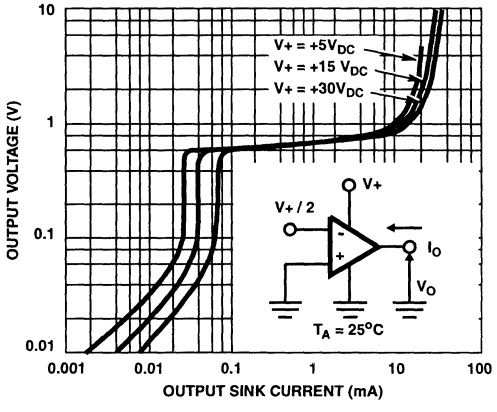


FIGURE 12. OUTPUT SINK CURRENT CHARACTERISTICS

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued)

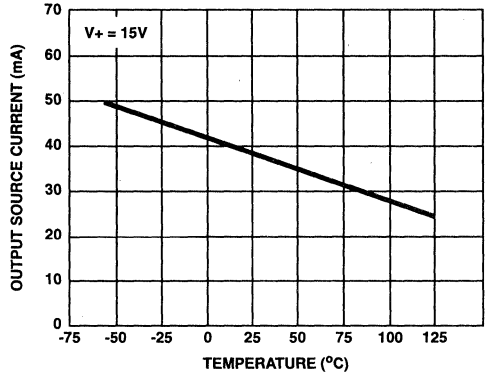
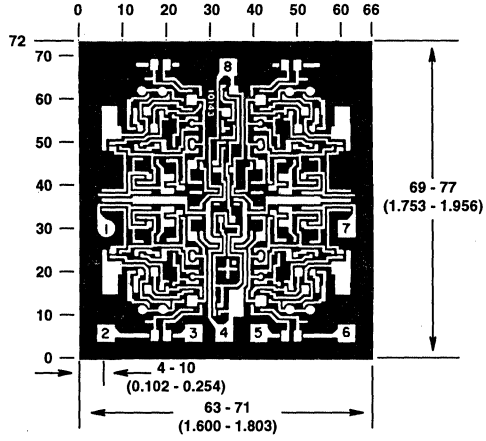


FIGURE 13. OUTPUT CURRENT vs AMBIENT TEMPERATURE

Metallization Mask Layout



Dimensions in parentheses are in millimeters and derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^{0} instead of 90^{0} with respect to the face of the chip. Therefore, the isolated chip is actually 7mils (0.17mm) larger in both dimensions.

HARRIS SEMICONDUCTOR

CA741, CA741C, CA1458, CA1558, LM741, LM741C, LM1458

Single and Dual, High Gain Operational Amplifiers for Military, Industrial and Commercial Applications

November 1996

Features

- Input Bias Current . . . . . 500nA (Max)
- Input Offset Current. . . . . 200nA (Max)

Applications

- Comparator
- DC Amplifier
- Integrator or Differentiator
- Multivibrator
- Summing Amplifier
- Narrow Band or Band Pass Filter

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA0741E	-55 to 125	8 Ld PDIP	E8.3
CA0741CE	0 to 70	8 Ld PDIP	E8.3
CA1458E	0 to 70	8 Ld PDIP	E8.3
CA1558E	-55 to 125	8 Ld PDIP	E8.3
CA0741T	-55 to 125	8 Pin Metal Can	T8.C
CA0741CT	0 to 70	8 Pin Metal Can	T8.C
CA1458T	0 to 70	8 Pin Metal Can	T8.C
CA1558T	-55 to 125	8 Pin Metal Can	T8.C
LM741N	-55 to 125	8 Ld PDIP	E8.3
LM741CN	0 to 70	8 Ld PDIP	E8.3
LM741H	-55 to 125	8 Pin Metal Can	T8.C
LM741CH	0 to 70	8 Pin Metal Can	T8.C
LM1458N	0 to 70	8 Ld PDIP	E8.3

Description

The CA1458, CA1558 (dual types); CA741C, CA741 (single types); high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated circuit devices provide output short circuit protection and latch-free operation. These types also feature wide common mode and differential mode signal ranges and have low offset voltage nulling capability when used with an appropriately valued potentiometer. A 10kΩ potentiometer is used for offset nulling types CA741C, CA741 (see Figure 1). Types CA1458, CA1558 have no specific terminals for offset nulling. Each type consists of a differential input amplifier that effectively drives a gain and level shifting stage having a complementary emitter follower output.

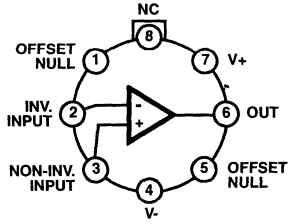
The manufacturing process make it possible to produce IC operational amplifiers with low burst "popcorn" noise characteristics. The CA741 gives limit specifications for burst noise in the data bulletin, File Number 530. Contact your Sales Representative for information pertinent to other operational amplifier types that meet low burst noise specifications.

Technical Data on LM Branded types is identical to the corresponding CA Branded types.

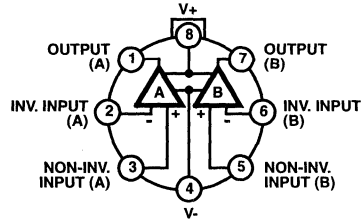
3 OPERATIONAL AMPLIFIERS

Pinouts

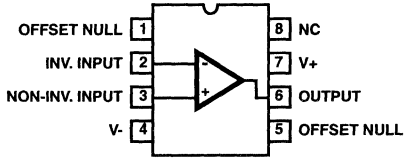
CA741, CA741C, LM741, LM741C (CAN)
TOP VIEW



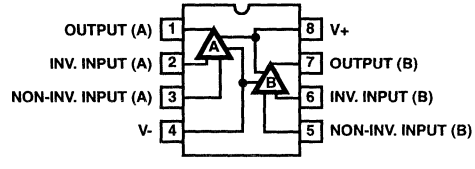
CA1458, CA1558 (METAL CAN)
TOP VIEW



CA741, CA741C, LM741, LM741C (PDIP)
TOP VIEW



CA1458, CA1558, LM1458 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **531.3**

Absolute Maximum Ratings

Supply Voltage
- CA741C, CA1458, LM741C, LM1458 (Note 1) 36V
- CA741, CA1558, LM741 (Note 1) 44V

Differential Input Voltage 30V
Input Voltage . . . . . $\pm V_{SUPPLY}$
Offset Terminal to V- Terminal Voltage (CA741C, CA741) . . . ±0.5V
Output Short Circuit Duration . . . . . Indefinite

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	130	N/A
Can Package	155	67

Maximum Junction Temperature (Can Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range
- CA741, CA1558, LM741 . . . . . -55°C to 125°C
- CA741C, CA1458, LM741C, LM1458 (Note 2) . . . . . 0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:
1. Values apply for each section of the dual amplifiers.
2. All types in any package style can be operated over the temperature range of -55°C to 125°C, although the published limits for certain electrical specification apply only over the temperature range of 0°C to 70°C.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Typical Values Intended Only for Design Guidance, $V_{SUPPLY} = \pm 15V$

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUE (ALL TYPES)	UNITS
Input Capacitance	C_I		1.4	pF
Offset Voltage Adjustment Range			±15	mV
Output Resistance	R_O		75	Ω
Output Short Circuit Current			25	mA
Transient Response Rise Time	t_r	Unity Gain, $V_I = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$	0.3	µs
Overshoot	O.S.		5.0	%
Slew Rate (Closed Loop)	SR	$R_L \geq 2k\Omega$	0.5	V/µs

Electrical Specifications

For Equipment Design, $V_{SUPPLY} = \pm 15V$

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) CA741, CA1558, LM741			(NOTE 4) CA741C, CA1458, LM741C, LM1458			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10k\Omega$	25	-	1	5	-	2	6	mV
		Full	-	1	6	-	-	7.5	mV
Input Common Mode Voltage Range		25	-	-	-	±12V	±13V	-	V
		Full	±12V	±13V	-	-	-	-	V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	25	-	-	-	70	90	-	dB
		Full	70	90	-	-	-	-	dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	25	-	-	-	-	30	150	µV/V
		Full	-	30	150	-	-	-	µV/V
Input Resistance		25	0.3	2	-	0.3	2	-	MΩ

Electrical Specifications For Equipment Design, $V_{SUPPLY} = \pm 15V$ **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) CA741, CA1558, LM741			(NOTE 4) CA741C, CA1458, LM741C, LM1458			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Bias Current		25	-	80	500	-	80	500	nA
		Full	-	-	-	-	-	800	nA
		-55	-	300	1500	-	-	-	nA
		125	-	30	500	-	-	-	nA
Input Offset Current		25	-	20	200	-	20	200	nA
		Full	-	-	-	-	-	300	nA
		-55	-	85	500	-	-	-	nA
		125	-	7	200	-	-	-	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	50,000	200,000	-	20,000	200,000	-	V/V
		Full	25,000	-	-	15,000	-	-	V/V
Output Voltage Swing	$R_L \geq 10k\Omega$	25	-	-	-	±12V	±14V	-	V
		Full	±12V	±14V	-	-	-	-	
	$R_L \geq 2k\Omega$	25	-	-	-	±10V	±13V	-	V
		Full	±10V	±13V	-	±10V	±13V	-	
Supply Current		25	-	1.7	2.8	-	1.7	2.8	mA
		-55	-	2	3.3	-	-	-	mA
		125	-	1.5	2.5	-	-	-	mA
Device Power Dissipation		25	-	50	85	-	50	85	mW
		-55	-	60	100	-	-	-	mW
		125	-	45	75	-	-	-	mW

NOTE:

4. Values apply for each section of the dual amplifiers.

Test Circuits

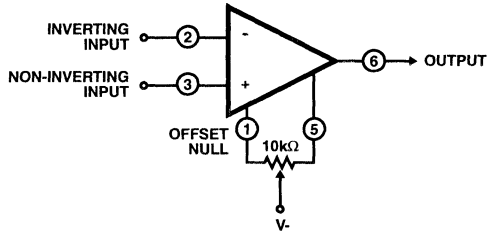


FIGURE 1. OFFSET VOLTAGE NULL CIRCUIT FOR CA741C, CA741, LM741C, AND LM741

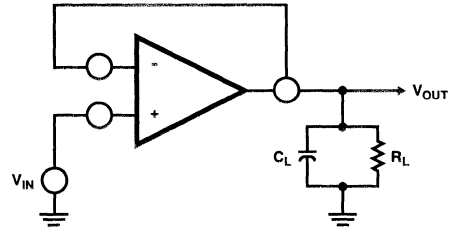
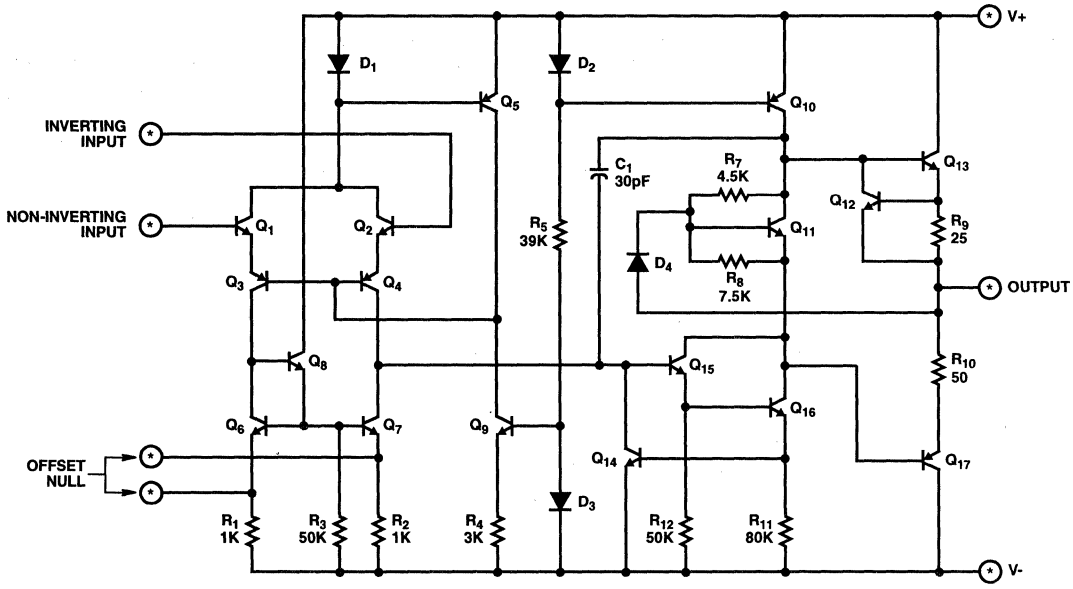


FIGURE 2. TRANSIENT RESPONSE TEST CIRCUIT FOR ALL TYPES

Schematic Diagram (Notes 5, 6)

CA741C, CA741, LM741C, LM741 AND FOR EACH AMPLIFIER OF THE CA1458, CA1558, AND LM1458



NOTES:

5. See Pinouts for Terminal Numbers of Respective Types.
6. All Resistance Values are in Ohms.

Typical Performance Curves

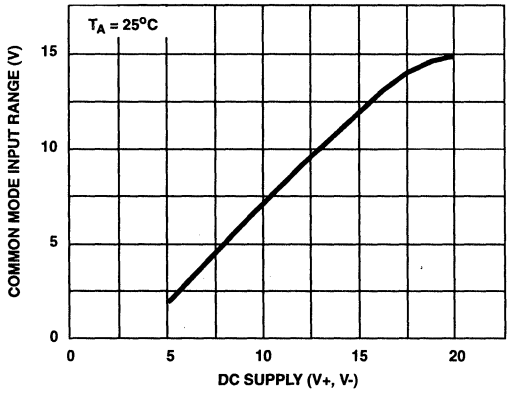


FIGURE 3. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE FOR ALL TYPES

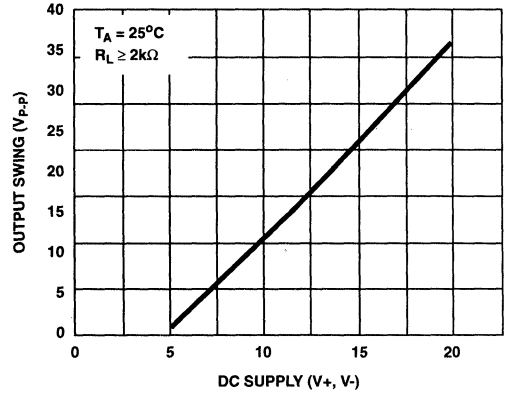


FIGURE 4. OUTPUT VOLTAGE vs SUPPLY VOLTAGE FOR ALL TYPES

Typical Performance Curves (Continued)

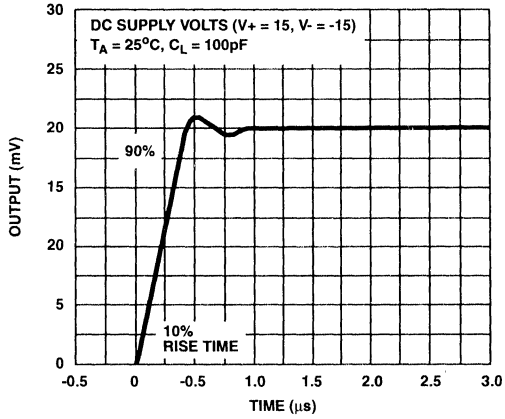
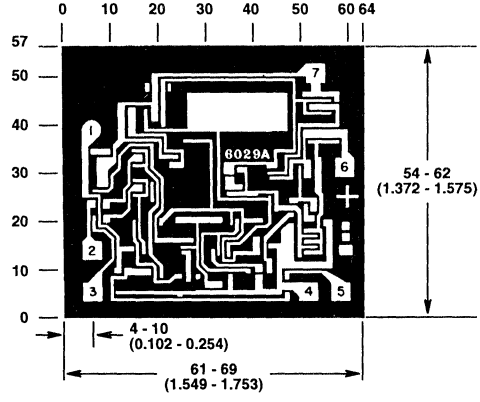


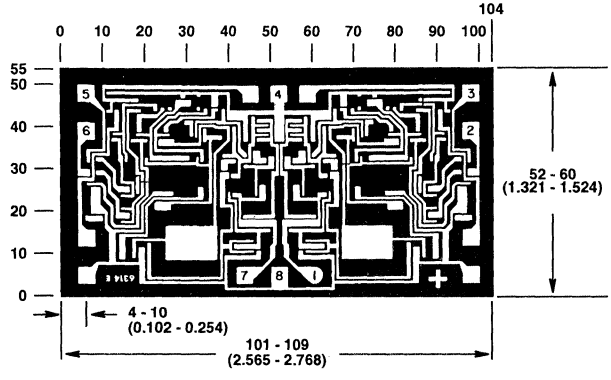
FIGURE 5. TRANSIENT RESPONSE FOR CA741C AND CA741

Metallization Mask Layout

CA741CH



CA1458H



NOTE: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

HARRIS SEMICONDUCTOR

CA3020, CA3020A

NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

8MHz Power Amps For Military, Industrial and Commercial Equipment

November 1996

Features

- High Power Output Class B Amplifier
  - CA3020 ..... 0.5W (Typ) at V_{CC} = 9V
  - CA3020A ..... 1.0W (Typ) at V_{CC} = 12V
- Wide Frequency Range .. Up to 8MHz with Resistive Loads
- High Power Gain..... 75dB (Typ)
- Single Power Supply For Class B Operation With Transformer
  - CA3020 ..... 3V to 9V
  - CA3020A ..... 3V to 12V
- Built-In Temperature-Tracking Voltage Regulator Provides Stable Operation Over -55°C to 125°C Temperature Range

Applications

- AF Power Amplifiers For Portable and Fixed Sound and Communications Systems
- Servo-Control Amplifiers
- Wide-Band Linear Mixers
- Video Power Amplifiers
- Transmission-Line Driver Amplifiers (Balanced and Unbalanced)
- Fan-In and Fan-Out Amplifiers For Computer Logic Circuits
- Lamp-Control Amplifiers
- Motor-Control Amplifiers
- Power Multivibrators
- Power Switches

Description

The CA3020 and CA3020A are integrated-circuit, multi-stage, multipurpose, wide-band power amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as class B power amplifiers. The CA3020A can provide a maximum power output of 1W from a $12V_{DC}$ supply with a typical power gain of 75dB. The CA3020 provides 0.5W power output from a 9V supply with the same power gain.

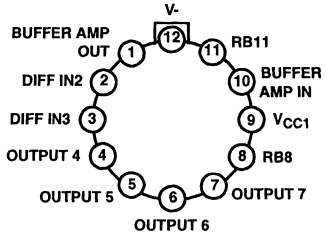
Refer to AN5766 for application information.

Ordering Information

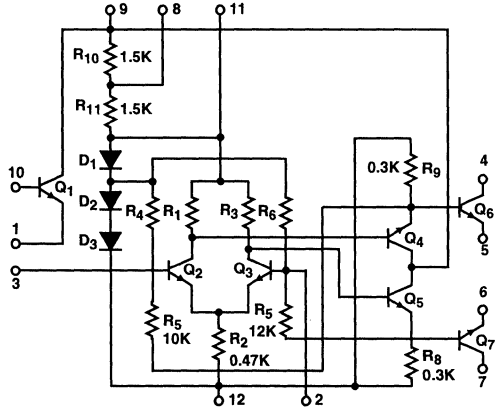
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3020	-55 to 125	12 Pin Metal Can	T12.B
CA3020A	-55 to 125	12 Pin Metal Can	T12.B

Pinout

CA3020
(METAL CAN)
TOP VIEW



Schematic Diagram



The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as 30%.

Harris reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

CA3060

110kHz, Operational Transconductance Amplifier Array

November 1996

Features

- Low Power Consumption as Low as 100mW Per Amplifier
- Independent Biasing for Each Amplifier
- High Forward Transconductance
- Programmable Range of Input Characteristics
- Low Input Bias and Input Offset Current
- High Input and Output Impedance
- No Effect on Device Under Output Short-Circuit Conditions
- Zener Diode Bias Regulator

Applications

- For Low Power Conventional Operational Amplifier Applications
- Active Filters
- Comparators
- Gyrators
- Mixers
- Modulators
- Multiplexers
- Multipliers
- Strobing and Gating Functions
- Sample and Hold Functions

Description

The CA3060 monolithic integrated circuit consists of an array of three independent Operational Transconductance Amplifiers (see Note). This type of amplifier has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, $g_M R_L$). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filters.

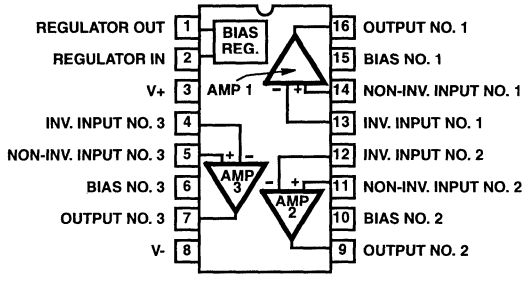
The three amplifiers in the CA3060 are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific application. The electrical characteristics of each amplifier are a function of the amplifier bias current (I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant DC level between input and output of each amplifier also makes the CA3060 suitable for a variety of nonlinear applications such as mixers, multipliers, and modulators.

In addition, the CA3060 incorporates a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

NOTE: Generic applications of the OTA are described in AN-6668. For improved input operating ranges, refer to CA3080 and CA3280 data sheets (File Nos. 475 and 1174) and application notes AN6668 and AN6818.

Pinout

CA3060
(PDIP)
TOP VIEW



Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3060E	-40 to 85	16 Ld PDIP	E16.3

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **537.3**

CA3078, CA3078A

November 1996

2kHz, Micropower Operational Amplifier

Features

- Low Standby Power . . . . . As Low As 700nW
- Wide Supply Voltage Range . . . . . ±0.75V to ±15V
- High Peak Output Current . . . . . 6.5mA (Min)
- Adjustable Quiescent Current
- Output Short Circuit Protection

Applications

- Portable Electronics
- Medical Electronics
- Instrumentation
- Telemetry
- Intrusion Alarms

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3078AE	-55 to 125	8 Ld PDIP	E8.3
CA3078AM (3078A)	-55 to 125	8 Ld SOIC	M8.15
CA3078AM96 (3078A)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA3078AT	-55 to 125	8 Pin Metal Can	T8.C
CA3078E	0 to 70	8 Ld PDIP	E8.3
CA3078M (3078)	0 to 70	8 Ld SOIC	M8.15
CA3078T	0 to 70	8 Pin Metal Can	T8.C

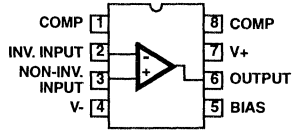
Description

The CA3078 and CA3078A are high gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078 and CA3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5V battery is a practical reality with these devices.

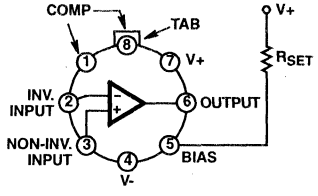
The CA3078A is a premium device having a supply voltage range of V± = 0.75V to V± = 15V. The CA3078 has the same lower supply voltage limit but the upper limit is V+ = +6V and V- = -6V.

Pinouts

CA3078 (PDIP, SOIC)
TOP VIEW



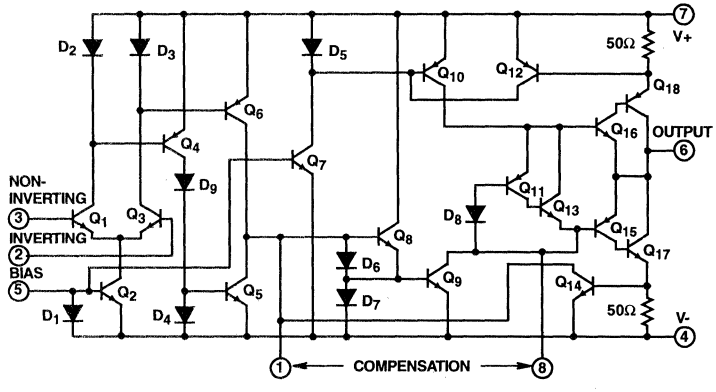
CA3078 (METAL CAN)
TOP VIEW



NOTE: Pin 4 is connected to case.

Schematic Diagram

CA3078 AND CA3078A



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **535.3**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminal)
- CA3078 . . . . . 14V
- CA3078A 36V

Differential Input Voltage 6V
Input Voltage . . . . . V+ to V-
Input Current 0.1mA
Output Short Circuit Duration (Note 1) . . . . . No Limitation

Operating Conditions

Temperature Range
- CA3078 . . . . . $0^{o}C$ to $70^{o}C$
- CA3078A . . . . . $-55^{o}C$ to $125^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
PDIP Package	130	N/A
SOIC Package	170	N/A
Metal Can Package	175	100

Maximum Junction Temperature (Metal Can Package) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications For Equipment Design

PARAMETER	TEST CONDITIONS			CA3078 LIMITS					CA3078A LIMITS					UNITS
				R_{SET} = 1MΩ					R_{SET} = 5.1MΩ					
				$T_A = 25^{o}C$			$T_A = 0^{o}C$ to $70^{o}C$		$T_A = 25^{o}C$			$T_A = -55^{o}C$ to $125^{o}C$		
	V+ and V-	R_S (kΩ)	R_L (kΩ)	MIN	TYP	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IO}	±6V	≤10	-	-	1.3	4.5	-	5	-	0.70	3.5	-	4.5	mV
I_{IO}		-	-	-	6	32	-	40	-	0.50	2.5	-	5.0	nA
I_{IB}		-	-	-	60	170	-	200	-	7	12	-	50	nA
A_{OL}		-	≥10	88	92	-	86	-	92	100	-	90	-	dB
I_Q		-	-	-	100	130	-	150	-	20	25	-	45	µA
P_D		-	-	-	1200	1560	-	1800	-	240	300	-	540	µW
V_{OM}		-	≥10	±5.1	±5.3	-	±5	-	±5.1	±5.3	-	±5	-	V
V_{ICR}		≤10	-	-	-5.5 to +5.8	-	-5 to +5	-	-	-5.5 to +5.8	-	-5 to +5	-	V
CMRR		≤10	-	80	110	-	-	-	80	115	-	-	-	dB
I_{OM+} or I_{OM-}		-	-	-	12	-	6.5	30	-	12	-	6.5	30	mA
$\Delta V_{IO}/\Delta V+$		≤10	-	76	93	-	-	-	76	105	-	-	-	µV/V
$\Delta V_{IO}/\Delta V-$		≤10	-	76	93	-	-	-	76	105	-	-	-	µV/V
									R_{SET} = 13MΩ					
V_{IO}	±15V	≤10	-	-	-	-	-	-	-	1.4	3.5	-	4.5	mV
A_{OL}		-	≥10	-	-	-	-	-	92	100	-	88	-	dB
I_Q		-	-	-	-	-	-	-	-	20	30	-	50	µA
P_D		-	-	-	-	-	-	-	-	600	750	-	1350	µW
V_{OM}		-	≥10	-	-	-	-	-	±13.7	±14.1	-	±13.5	-	V
CMRR		≤10	-	-	-	-	-	-	80	106	-	-	-	dB
I_{IB}		-	-	-	-	-	-	-	-	7	14	-	55	nA
I_{IO}		-	-	-	-	-	-	-	-	0.50	2.7	-	5.5	nA

Electrical Specifications $T_A = 25^oC$, Typical Values Intended Only for Design Guidance

PARAMETER	CA3078		CA3078A		UNITS
	V+ = +1.3V, V- = -1.3V R_{SET} = 2MΩ	V+ = +0.75V, V- = -0.75V R_{SET} = 10MΩ	V+ = +1.3V, V- = -1.3V R_{SET} = 2MΩ	V+ = +0.75V, V- = -0.75V R_{SET} = 10MΩ	
V_{IO}	1.3	1.5	0.7	0.9	mV
I_{IO}	1.7	0.5	0.3	0.054	nA
I_{IB}	9	1.3	3.7	0.45	nA
A_{OL}	80	60	84	65	dB
I_Q	10	1	10	1	µA
P_D	26	1.5	26	1.5	µW
V_{OP-P}	1.4	0.3	1.4	0.3	V
V_{ICR}	-0.8 to +1.1	-0.2 to +0.5	-0.8 to +1.1	-0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}\pm$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V\pm$	20	50	20	50	µV/V

Electrical Specifications $T_A = 25^oC$ and $V_{SUPPLY} = \pm 6V$, Typical Values Intended Only for Design Guidance

PARAMETER	TEST CONDITIONS	CA3078	CA3078A		UNITS
		R_{SET} = 1MΩ	R_{SET} = 5.1MΩ	R_{SET} = 1MΩ	
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10k\Omega$	6	5	6	$\mu V/^oC$
$\Delta I_{IO}/\Delta T_A$	$R_S \leq 10k\Omega$	70	6.3	70	$pA/^oC$
BW_{OL}	3dB pt.	2	0.3	2	kHz
SR	See Figures 23, 24	0.04	0.027	0.04	V/µs
		1.5	0.5	1.5	V/µs
t_R	10% to 90% Rise Time	2.5	3	2.5	µs
R_I	-	0.87	7.4	1.7	MΩ
R_O	-	0.8	1	0.8	kΩ
e_N(10Hz)	R_S = 0	25	40	-	$nV/\sqrt{Hz}$
i_N(10Hz)	R_S = 1MΩ	1	0.25	-	$pA/\sqrt{Hz}$

Test Circuits

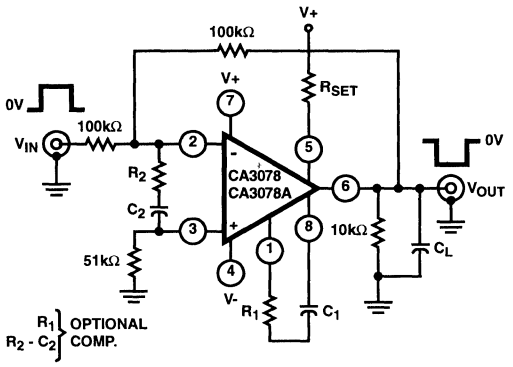


FIGURE 1. TRANSIENT RESPONSE AND SLEW RATE, UNITY GAIN (INVERTING) TEST CIRCUIT

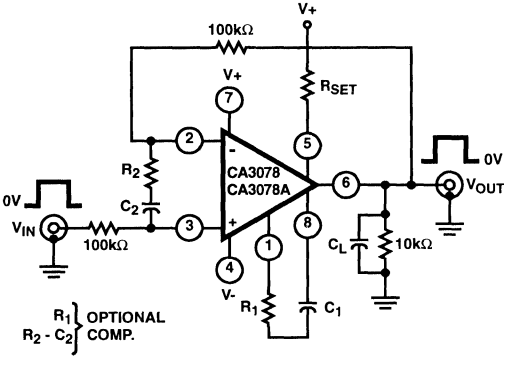
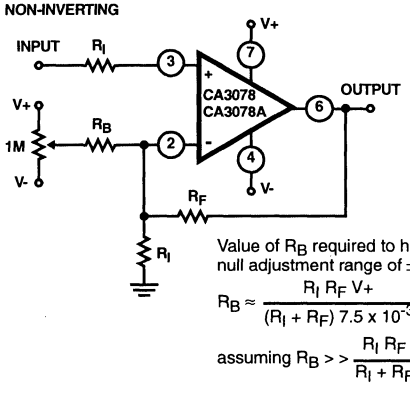


FIGURE 2. SLEW RATE, UNITY GAIN (NON-INVERTING) TEST CIRCUIT



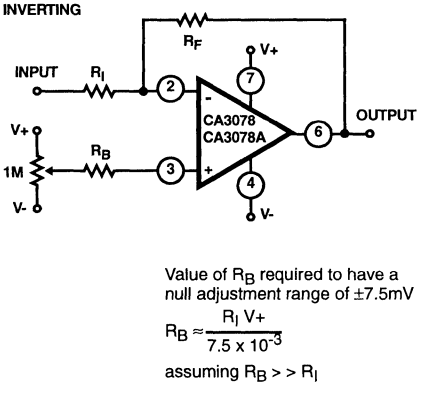


FIGURE 3. OFFSET VOLTAGE NULL CIRCUITS

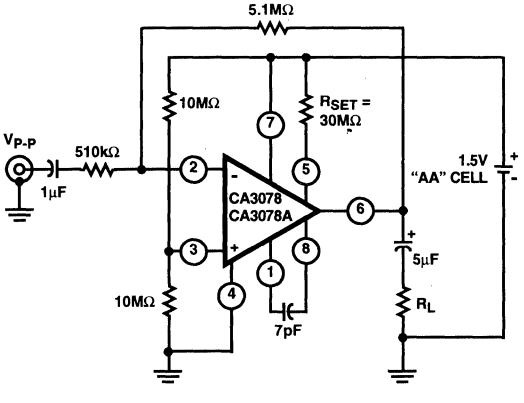


FIGURE 4. INVERTING 20dB AMPLIFIER CIRCUIT

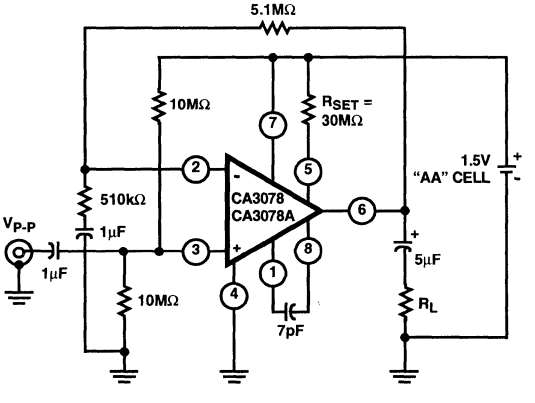


FIGURE 5. NON-INVERTING 20dB AMPLIFIER CIRCUIT

TABLE 1. UNITY GAIN SLEW RATE vs COMPENSATION - CA3078 AND CA3078A

V_{SUPPLY} = ±6V, Output Voltage (V_O) = ±5V, Load Resistance (R_L) = 10kΩ, Transient Response: 10% overshoot for an output voltage of 100mV, Ambient Temperature (T_A) = 25°C

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) FIGURE 1					UNITY GAIN (NON-INVERTING) FIGURE 2				
	R_1 kΩ	C_1 pF	R_2 kΩ	C_2 µF	SLEW RATE V/µs	R_1 kΩ	C_1 pF	R_2 kΩ	C_2 µF	SLEW RATE V/µs
CA3078 - I_Q = 100µA										
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor and Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078A - I_Q = 20µA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor and Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

Application Information

Compensation Techniques

The CA3078A and CA3078 can be phase compensated with one or two external components depending upon the closed loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from Terminal 1 to Terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figures 25 and 26. These curves represent the compensation necessary at quiescent currents of 100µA and 20µA, respectively, for a transient response with 10% overshoot. Figures 23 and 24 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from Terminal 1 to Terminal 8, with speed being sacrificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 100µA and 20µA.

Single Supply Operation

The CA3078A and CA3078 can operate from a single supply with a minimum total supply voltage of 1.5V. Figures 4 and 5 show the CA3078A or CA3078 in inverting and non-inverting 20dB amplifier configurations utilizing a 1.5V type "AA" cell for a supply. The total consumption for either circuit is approximately 675nW. The output voltage swing in this configuration is 300mV$_{P-P}$ with a 20kΩ load.

Typical Performance Curves

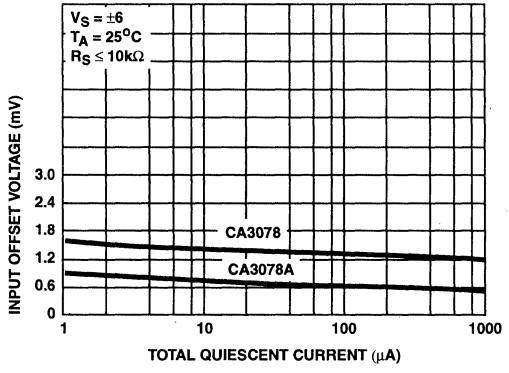


FIGURE 6. INPUT OFFSET VOLTAGE vs TOTAL QUIESCENT CURRENT

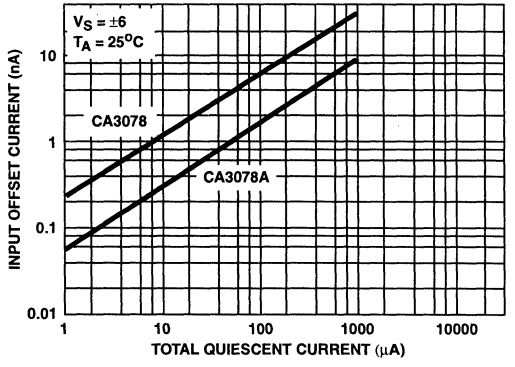


FIGURE 7. INPUT OFFSET CURRENT vs TOTAL QUIESCENT CURRENT

Typical Performance Curves (Continued)

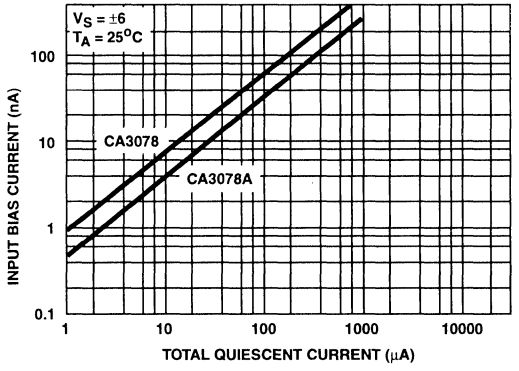


FIGURE 8. INPUT BIAS CURRENT vs TOTAL QUIESCENT CURRENT

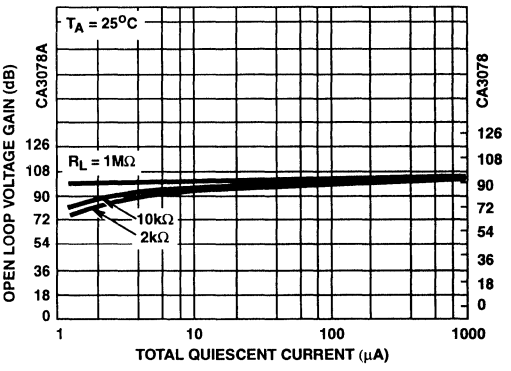


FIGURE 9. OPEN LOOP VOLTAGE GAIN vs TOTAL QUIESCENT CURRENT

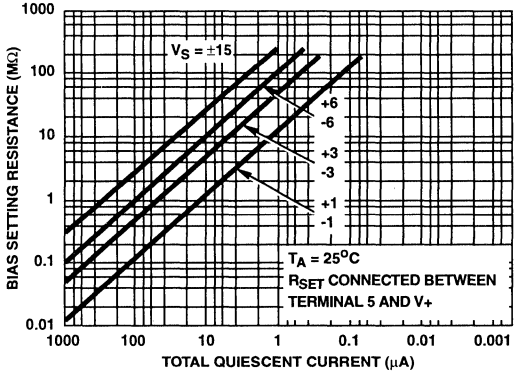


FIGURE 10. BIAS SETTING RESISTANCE vs TOTAL QUIESCENT CURRENT

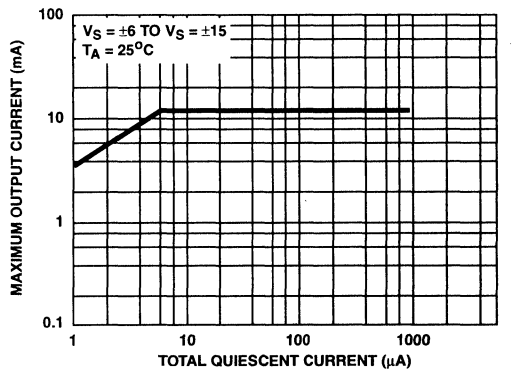


FIGURE 11. MAXIMUM OUTPUT CURRENT vs TOTAL QUIESCENT CURRENT

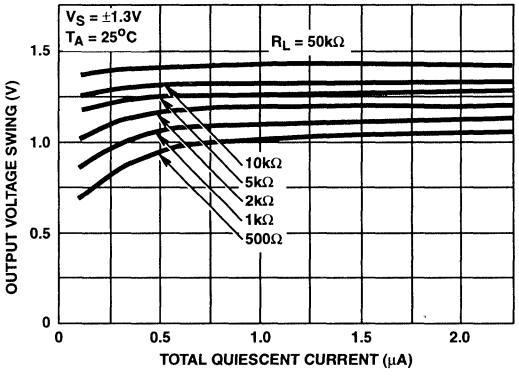


FIGURE 12. OUTPUT VOLTAGE SWING vs TOTAL QUIESCENT CURRENT

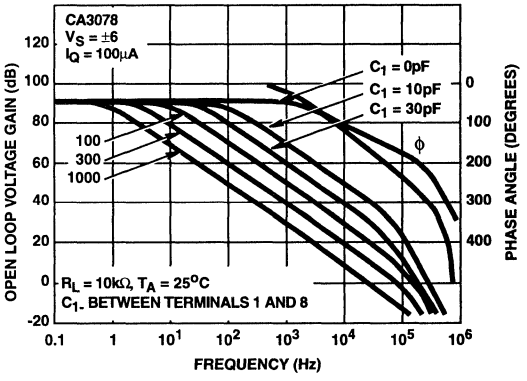


FIGURE 13. OPEN LOOP VOLTAGE GAIN vs FREQUENCY FOR CA3078

Typical Performance Curves (Continued)

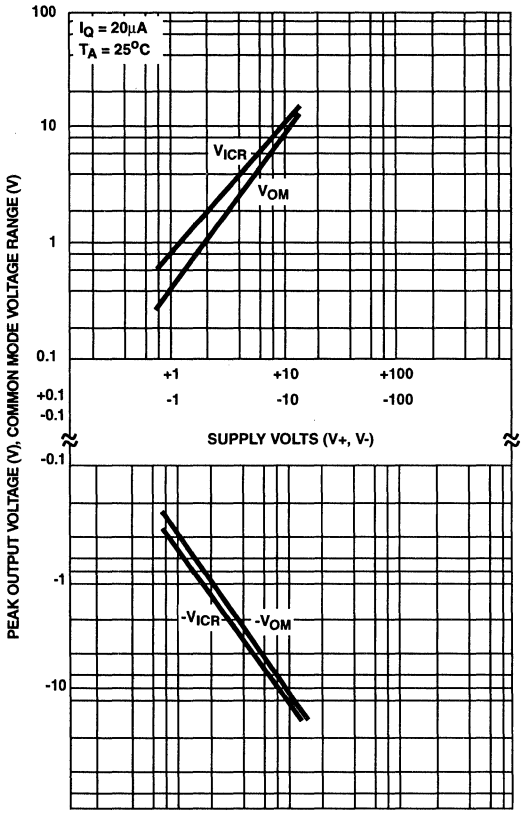


FIGURE 14. OUTPUT AND COMMON MODE VOLTAGE vs SUPPLY VOLTAGE

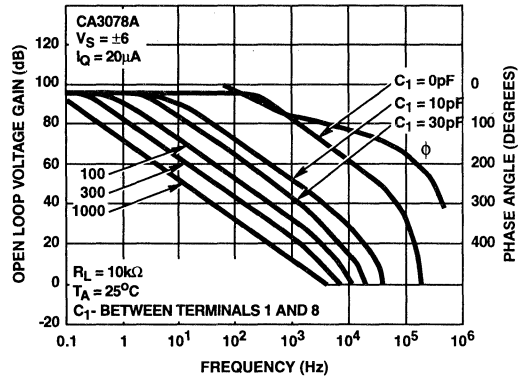


FIGURE 15. OPEN LOOP VOLTAGE GAIN vs FREQUENCY FOR CA3078A

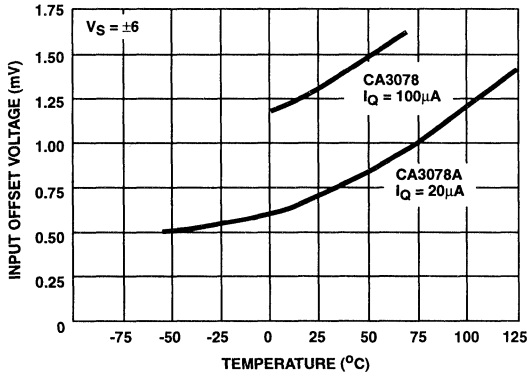


FIGURE 16. INPUT OFFSET VOLTAGE vs TEMPERATURE

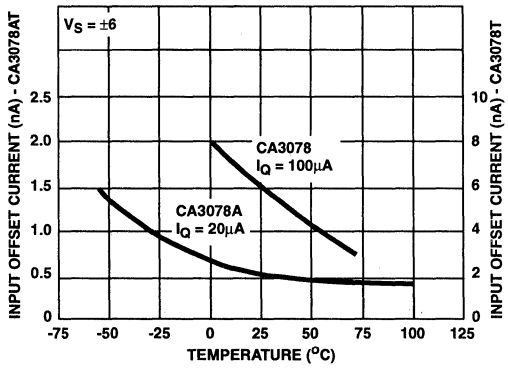


FIGURE 17. INPUT OFFSET CURRENT vs TEMPERATURE

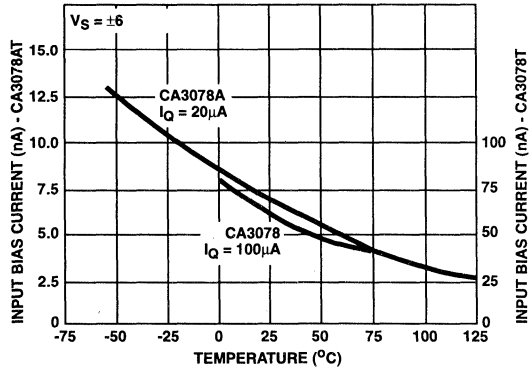


FIGURE 18. INPUT BIAS CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

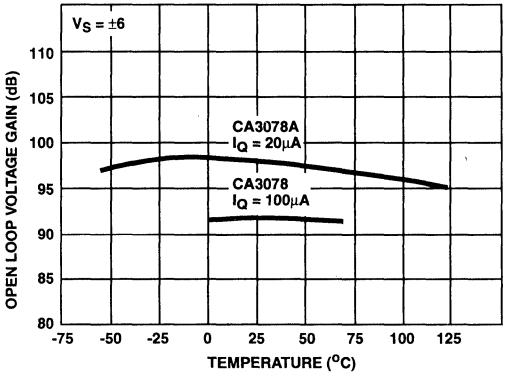


FIGURE 19. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

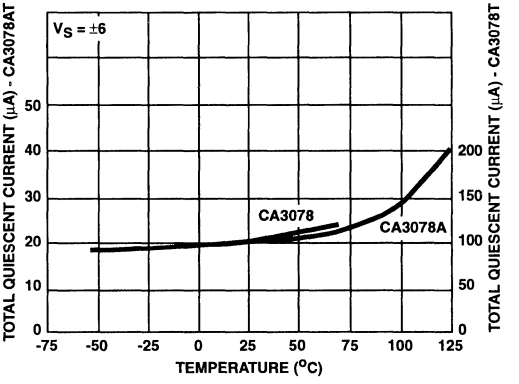


FIGURE 20. TOTAL QUIESCENT CURRENT vs TEMPERATURE

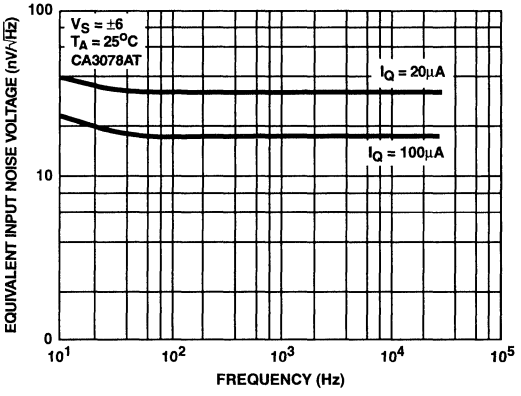


FIGURE 21. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

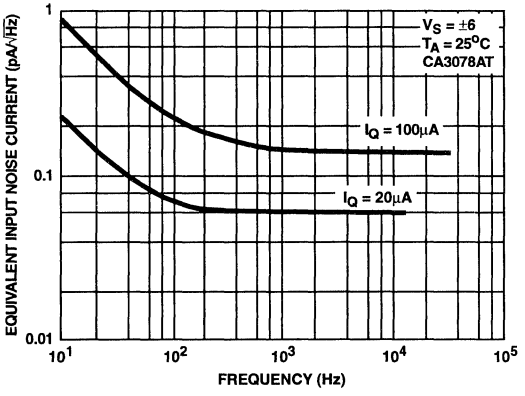
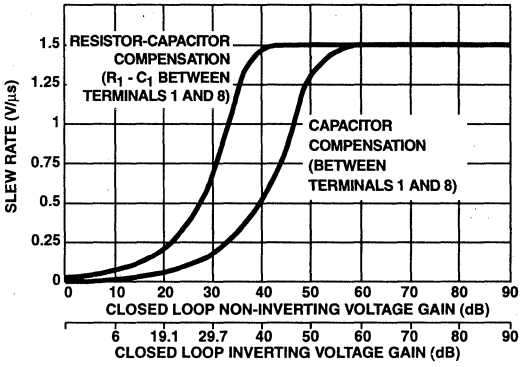


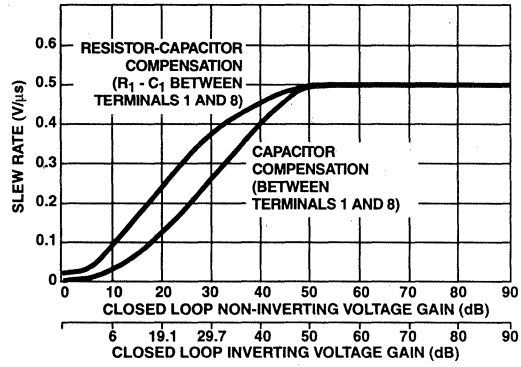
FIGURE 22. EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

Typical Performance Curves (Continued)



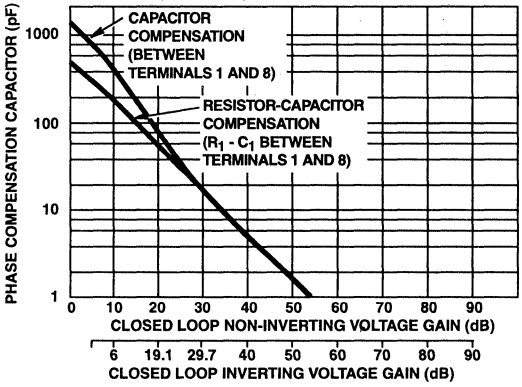
Supply Volts: V+ = +6, V- = -6
Quiescent Current (I_Q) = 100µA
Ambient Temperature (T_A) = 25°C
Load Impedance: R_L = 10kΩ, C_L = 100pF
Feedback Resistance (R_F) = 0.1MΩ
Output Voltage (V_{OP-P}) = 10V
R_1 determined for transient response with 10% overshoot on a 100mV output signal ($R_1 \times C_1 = 2.5 \times 10^{-6}$)

FIGURE 23. SLEW RATE vs CLOSED LOOP GAIN FOR I_Q = 100µA - CA3078



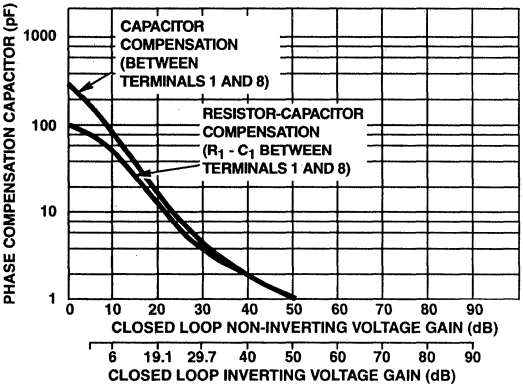
Supply Volts: V+ = +6, V- = -6
Quiescent Current (I_Q) = 20µA
Ambient Temperature (T_A) = 25°C
Load Impedance: R_L = 10kΩ, C_L = 100pF
Feedback Resistance (R_F) = 0.1MΩ
Output Voltage (V_{OP-P}) = 10V
R_1 determined for transient response with 10% overshoot on a 100mV output signal ($R_1 \times C_1 = 2 \times 10^{-6}$)

FIGURE 24. SLEW RATE vs CLOSED LOOP GAIN FOR I_Q = 20µA - CA3078A



Supply Volts: V+ = +6, V- = -6
Quiescent Current (I_Q) = 100µA
Ambient Temperature (T_A) = 25°C
Load Impedance: R_L = 10kΩ, C_L = 100pF
Feedback Resistance (R_F) = 0.1MΩ
Output Voltage (V_{OP-P}) = 100mV
R_1 determined for transient response with 10% overshoot on a 100mV output signal ($R_1 \times C_1 = 2.5 \times 10^{-6}$)

FIGURE 25. PHASE COMPENSATION CAPACITANCE vs CLOSED LOOP GAIN - CA3078



Supply Volts: V+ = +6, V- = -6
Quiescent Current (I_Q) = 20µA
Ambient Temperature (T_A) = 25°C
Load Impedance: R_L = 10kΩ, C_L = 100pF
Feedback Resistance (R_F) = 0.1MΩ
Output Voltage (V_{OP-P}) = 100mV
R_1 determined for transient response with 10% overshoot on a 100mV output signal ($R_1 \times C_1 = 2 \times 10^{-6}$)

FIGURE 26. PHASE COMPENSATION CAPACITANCE vs CLOSED LOOP GAIN - CA3078A

CA3080, CA3080A

2MHz, Operational Transconductance Amplifier (OTA)

November 1996

Features

- Slew Rate (Unity Gain, Compensated)..... 50V/μs
- Adjustable Power Consumption ..... 10μW to 30μW
- Flexible Supply Voltage Range..... ±2V to ±15V
- Fully Adjustable Gain .....0 to $g_M R_L$ Limit
- Tight g_M Spread:
  - CA3080 ..... 2:1
  - CA3080A 1.6:1
- Extended g_M Linearity..... 3 Decades

Applications

- Sample and Hold
- Multiplexer
- Voltage Follower
- Multiplier
- Comparator

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3080	0 to 70	8 Pin Metal Can	T8.C
CA3080A	-55 to 125	8 Pin Metal Can	T8.C
CA3080AE	-55 to 125	8 Ld PDIP	E8.3
CA3080AM (3080A)	-55 to 125	8 Ld SOIC	M8.15
CA3080AM96 (3080A)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA3080E	0 to 70	8 Ld PDIP	E8.3
CA3080M (3080)	0 to 70	8 Ld SOIC	M8.15
CA3080M96 (3080)	0 to 70	8 Ld SOIC Tape and Reel	M8.15

Description

The CA3080 and CA3080A types are Gatable-Gain Blocks which utilize the unique operational-transconductance-amplifier (OTA) concept described in Application Note AN6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

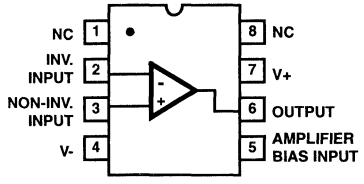
The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_M) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A types are notable for their excellent slew rate (50V/μs), which makes them especially useful for multiplexer and fast unity-gain voltage followers. These types are especially applicable for multiplexer applications because power is consumed only when the devices are in the "ON" channel state.

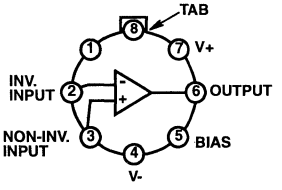
The CA3080A's characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplexing, etc.

Pinouts

CA3080
(PDIP, SOIC)
TOP VIEW



CA3080
(METAL CAN)
TOP VIEW



NOTE: Pin 4 is connected to case.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminal) 36V
Differential Input Voltage 5V
Input Voltage . . . . . V+ to V-
Input Signal Current 1mA
Amplifier Bias Current (I_{ABC}) 2mA
Output Short Circuit Duration (Note 1) . . . . . No Limitation

Operating Conditions

Temperature Range
CA3080 . . . . . 0°C to 70°C
CA3080A . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	130	N/A
SOIC Package	170	N/A
Metal Can Package	200	120

Maximum Junction Temperature (Metal Can) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

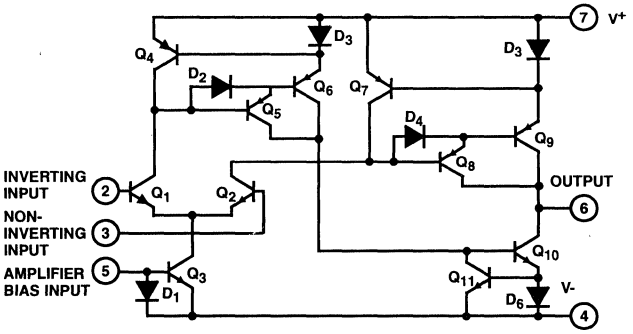
For Equipment Design, $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	TEMP	CA3080			CA3080A			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage		$I_{ABC} = 5\mu A$	25	-	0.3	-	-	0.3	2	mV
		$I_{ABC} = 500\mu A$	25	-	0.4	5	-	0.4	2	mV
			Full	-	-	6	-	-	5	mV
Input Offset Voltage Change		$I_{ABC} = 500\mu A$ to $5\mu A$	25	-	0.2	-	-	0.1	3	mV
Input Offset Voltage Temp. Drift		$I_{ABC} = 100\mu A$	Full	-	-	-	-	3.0	-	µV/°C
Input Offset Voltage Sensitivity	Positive	$I_{ABC} = 500\mu A$	25	-	-	150	-	-	150	µV/V
	Negative		25	-	-	150	-	-	150	µV/V
Input Offset Current		$I_{ABC} = 500\mu A$	25	-	0.12	0.6	-	0.12	0.6	µA
Input Bias Current		$I_{ABC} = 500\mu A$	25	-	2	5	-	2	5	µA
			Full	-	-	7	-	-	15	µA
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4V$	25	-	0.008	-	-	0.008	5	nA
Amplifier Bias Voltage		$I_{ABC} = 500\mu A$	25	-	0.71	-	-	0.71	-	V
Input Resistance		$I_{ABC} = 500\mu A$	25	10	26	-	10	26	-	kΩ
Input Capacitance		$I_{ABC} = 500\mu A$, f = 1MHz	25	-	3.6	-	-	3.6	-	pF
Input-to-Output Capacitance		$I_{ABC} = 500\mu A$, f = 1MHz	25	-	0.024	-	-	0.024	-	pF
Common-Mode Input-Voltage Range		$I_{ABC} = 500\mu A$	25	12 to -12	13.6 to -14.6	-	12 to -12	13.6 to -14.6	-	V
Forward Transconductance (Large Signal)		$I_{ABC} = 500\mu A$	25	6700	9600	13000	7700	9600	12000	µS
			Full	5400	-	-	4000	-	-	µS
Output Capacitance		$I_{ABC} = 500\mu A$, f = 1MHz	25	-	5.6	-	-	5.6	-	pF
Output Resistance		$I_{ABC} = 500\mu A$	25	-	15	-	-	15	-	MΩ
Peak Output Current		$I_{ABC} = 5\mu A$, $R_L = 0\Omega$	25	-	5	-	3	5	7	µA
		$I_{ABC} = 500\mu A$, $R_L = 0\Omega$	25	350	500	650	350	500	650	µA
			Full	300	-	-	300	-	-	µA

Electrical Specifications For Equipment Design, $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified **(Continued)**

PARAMETER		TEST CONDITIONS	TEMP	CA3080			CA3080A			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Peak Output Voltage	Positive	$I_{ABC} = 5\mu A$, $R_L = \infty$	25	-	13.8	-	12	13.8	-	V
	Negative		25	-	-14.5	-	-12	-14.5	-	V
	Positive	$I_{ABC} = 500\mu A$, $R_L = \infty$	25	12	13.5	-	12	13.5	-	V
	Negative		25	-12	-14.4	-	-12	-14.4	-	V
Amplifier Supply Current		$I_{ABC} = 500\mu A$	25	0.8	1	1.2	0.8	1	1.2	mA
Device Dissipation		$I_{ABC} = 500\mu A$	25	24	30	36	24	30	36	mW
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	25	-	0.08	-	-	0.08	5	nA
		$I_{ABC} = 0$, $V_{TP} = 36V$	25	-	0.3	-	-	0.3	5	nA
Propagation Delay		$I_{ABC} = 500\mu A$	25	-	45	-	-	45	-	ns
Common-Mode Rejection Ratio		$I_{ABC} = 500\mu A$	25	80	110	-	80	110	-	dB
Open-Loop Bandwidth		$I_{ABC} = 500\mu A$	25	-	2	-	-	2	-	MHz
Slew Rate		Uncompensated	25	-	75	-	-	75	-	V/μs
		Compensated	25	-	50	-	-	50	-	V/μs

Schematic Diagram



Typical Applications

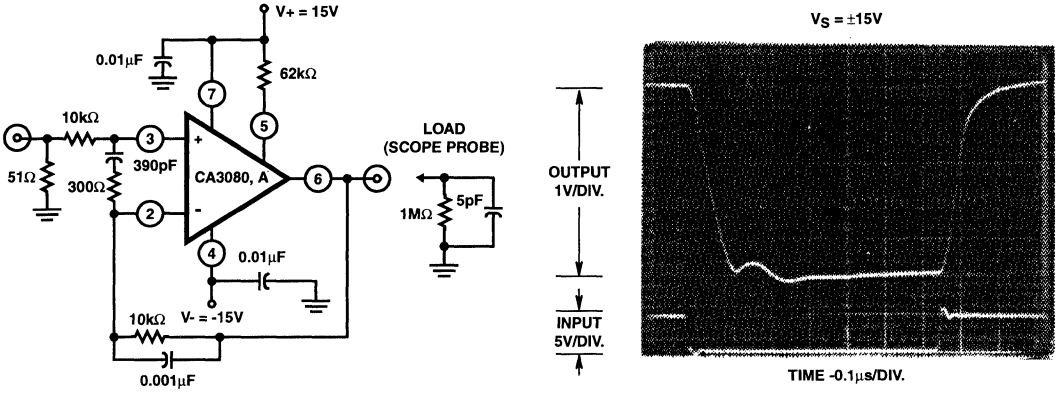


FIGURE 1. SCHEMATIC DIAGRAM OF THE CA3080 AND CA3080A IN A UNITY-GAIN VOLTAGE FOLLOWER CONFIGURATION AND ASSOCIATED WAVEFORM

Typical Applications (Continued)

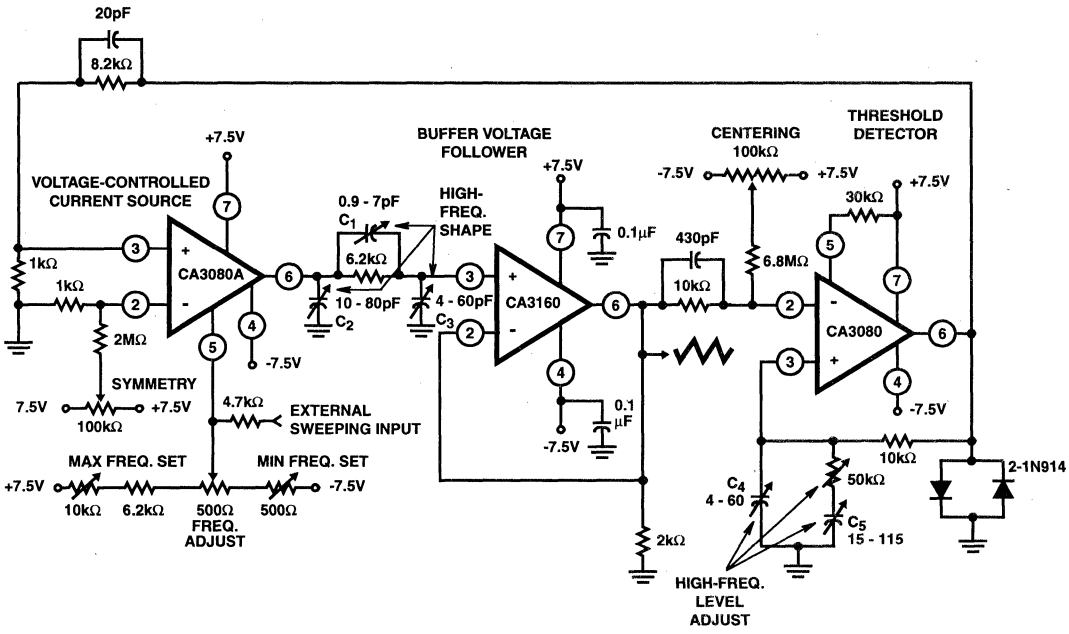
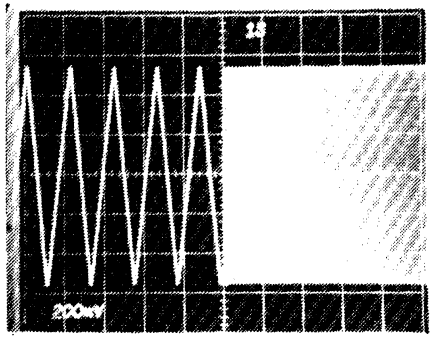
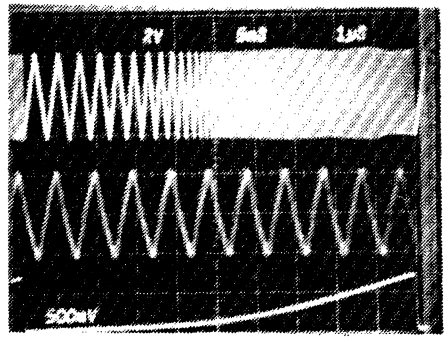


FIGURE 2. 1,000,000/1 SINGLE-CONTROL FUNCTION GENERATOR - 1MHz TO 1Hz



NOTE: A Square-Wave Signal Modulates The External Sweeping Input to Produce 1Hz and 1MHz, showing the 1,000,000/1 frequency range of the function generator.

FIGURE 3A. TWO-TONE OUTPUT SIGHAL FROM THE FUNCTION GENERATOR

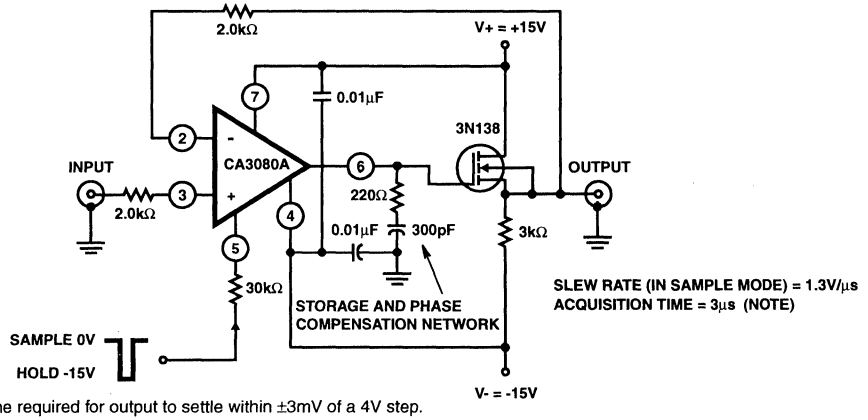


NOTE: The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1MHz signal via delayed oscilloscope triggering of the upper swept output signal.

FIGURE 3B. TRIPLE-TRACE OF THE FUNCTION GENERATOR SWEEPING TO 1MHz

FIGURE 3. FUNCTION GENERATOR DYNAMIC CHARACTERISTICS WAVEFORMS

Typical Applications (Continued)



NOTE: Time required for output to settle within ±3mV of a 4V step.

FIGURE 4. SCHEMATIC DIAGRAM OF THE CA3080A IN A SAMPLE-HOLD CONFIGURATION

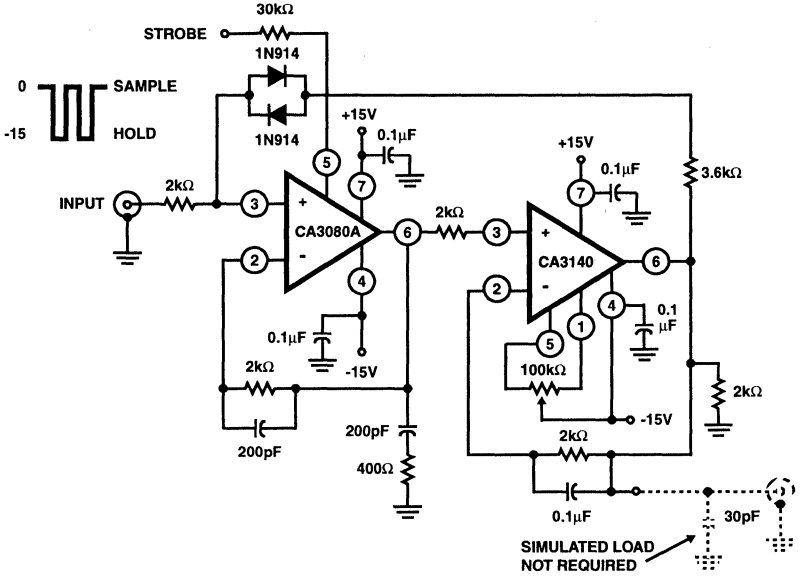
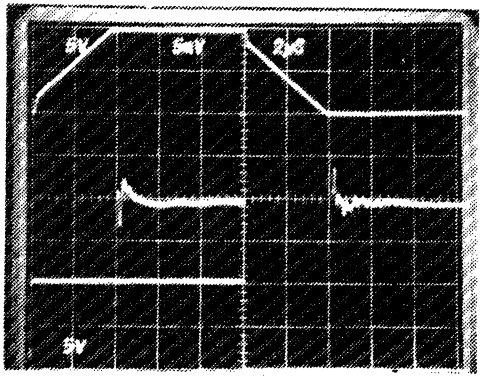


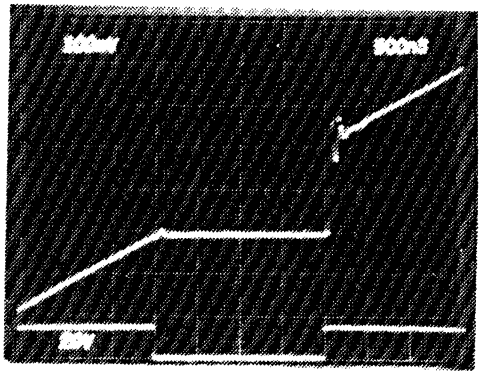
FIGURE 5. SAMPLE AND HOLD CIRCUIT

Typical Applications (Continued)



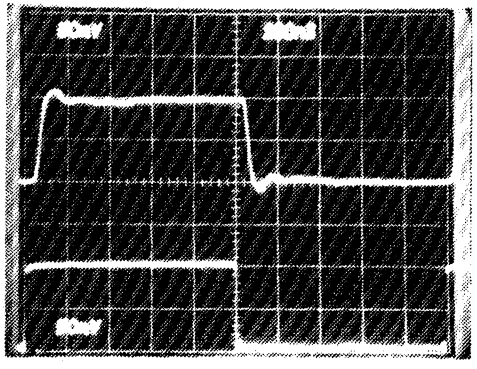
Top Trace: Output Signal
5V/Div., 2μs/Div.
Bottom Trace: Input Signal
5V/Div., 2μs/Div.
Center Trace: Difference of Input and Output Signals Through Tektronix Amplifier 7A13
5mV/Div., 2μs/Div.

FIGURE 6. LARGE SIGNAL RESPONSE AND SETTLING TIME FOR CIRCUIT SHOWN IN FIGURE 23



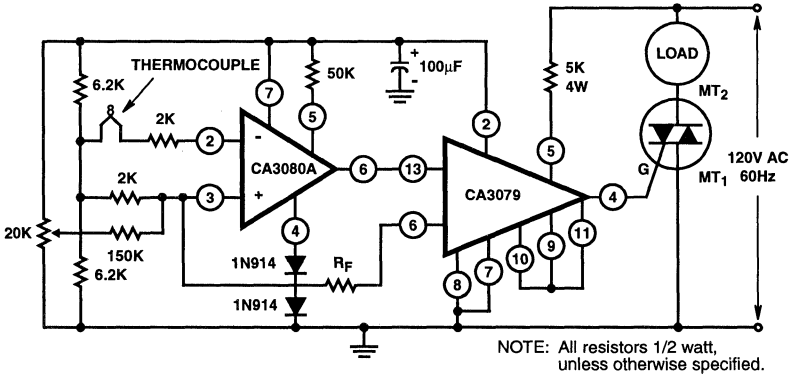
Top Trace: System Output; 100mV/Div., 500ns/Div.
Bottom Trace: Sampling Signal; 20V/Div., 500ns/Div.

FIGURE 7. SAMPLING RESPONSE FOR CIRCUIT SHOWN IN FIGURE 23



Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.

FIGURE 8. INPUT AND OUTPUT RESPONSE FOR CIRCUIT SHOWN IN FIGURE 23



NOTE: All resistors 1/2 watt, unless otherwise specified.

FIGURE 9. THERMOCOUPLE TEMPERATURE CONTROL WITH CA3079 ZERO VOLTAGE SWITCH AS THE OUTPUT AMPLIFIER

Typical Applications (Continued)

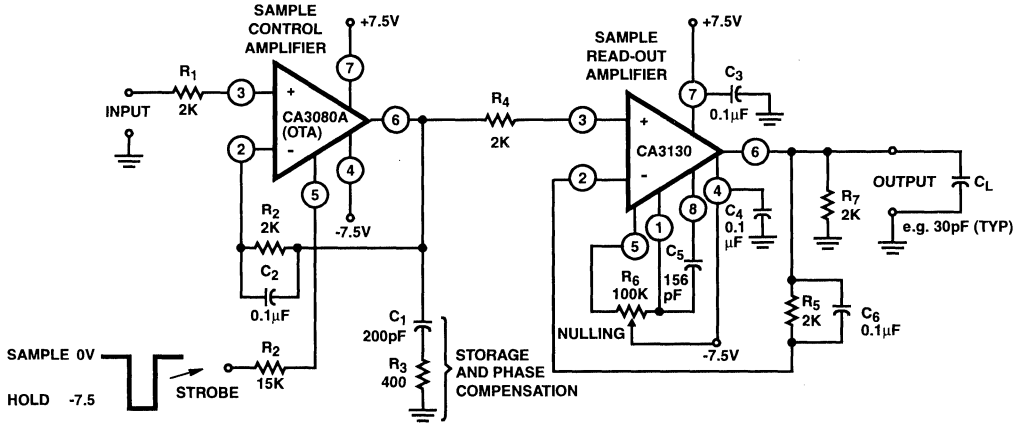
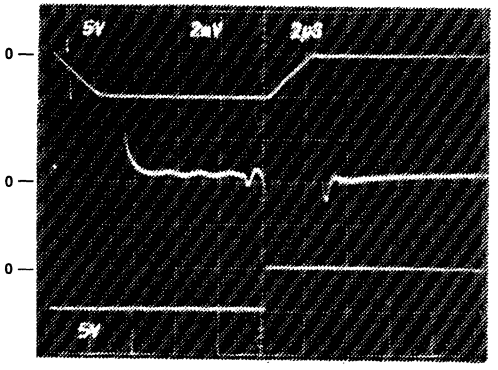
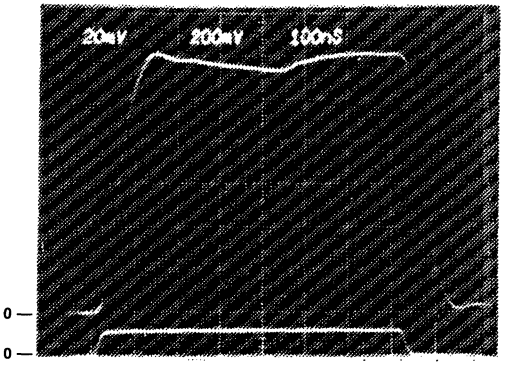


FIGURE 10. SCHEMATIC DIAGRAM OF THE CA3080A IN A SAMPLE-HOLD CIRCUIT WITH BIMOS OUTPUT AMPLIFIER



Top Trace: Output; 5V/Div., 2μs/Div.
Center Trace: Differential Comparison of Input and Output 2mV/Div., 2μs/Div.
Bottom Trace: Input; 5V/Div., 2μs/Div.

FIGURE 11. LARGE-SIGNAL RESPONSE FOR CIRCUIT SHOWN IN FIGURE 28



Top Trace: Output 20mV/Div., 100ns/Div.
Bottom Trace: Input 200mV/Div., 100ns/Div.

FIGURE 12. SMALL-SIGNAL RESPONSE FOR CIRCUIT SHOWN IN FIGURE 28

Typical Applications (Continued)

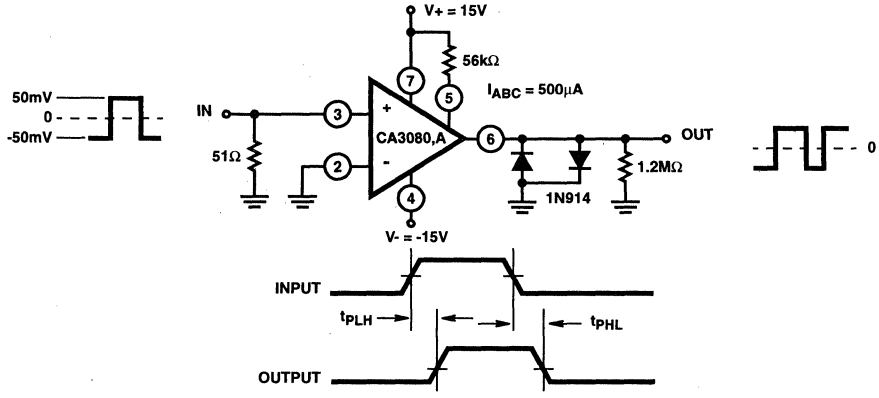


FIGURE 13. PROPAGATION DELAY TEST CIRCUIT AND ASSOCIATED WAVEFORMS

Typical Performance Curves

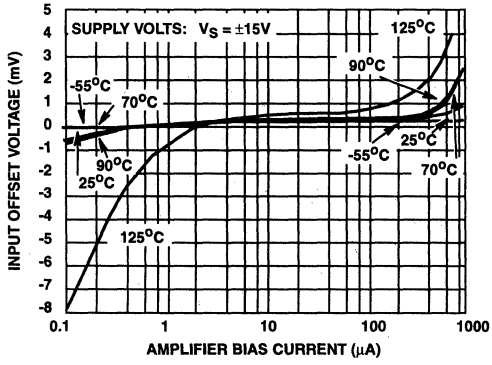


FIGURE 14. INPUT OFFSET VOLTAGE vs AMPLIFIER BIAS CURRENT

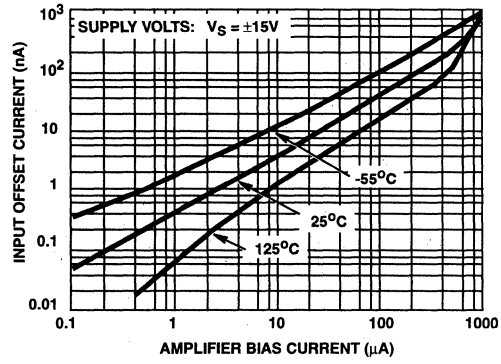


FIGURE 15. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT

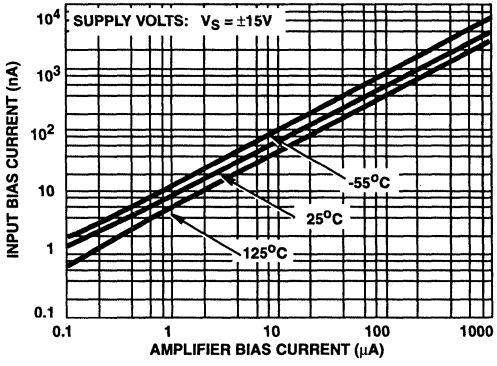


FIGURE 16. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT

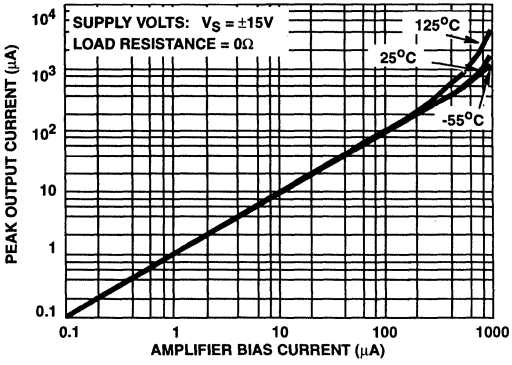


FIGURE 17. PEAK OUTPUT CURRENT vs AMPLIFIER BIAS CURRENT

Typical Performance Curves (Continued)

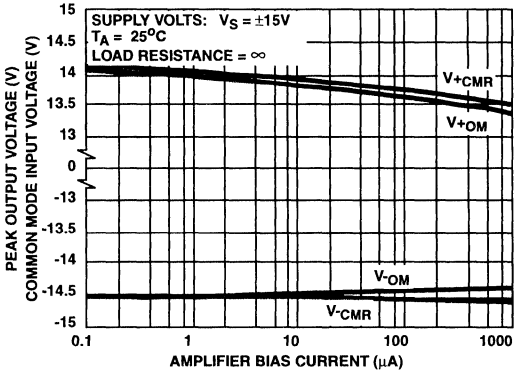


FIGURE 18. PEAK OUTPUT VOLTAGE vs AMPLIFIER BIAS CURRENT

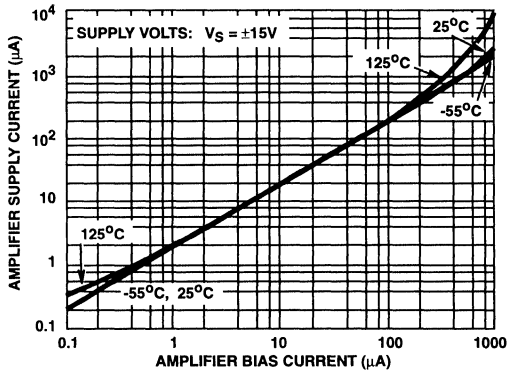


FIGURE 19. AMPLIFIER SUPPLY CURRENT vs AMPLIFIER BIAS CURRENT

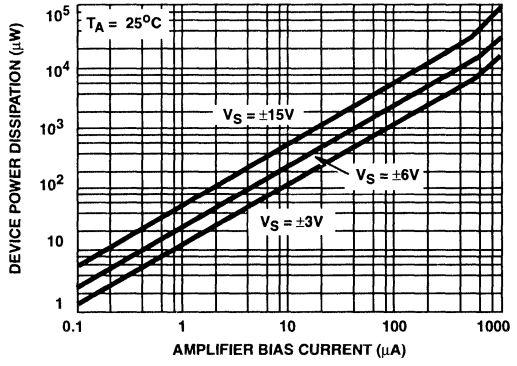


FIGURE 20. TOTAL POWER DISSIPATION vs AMPLIFIER BIAS CURRENT

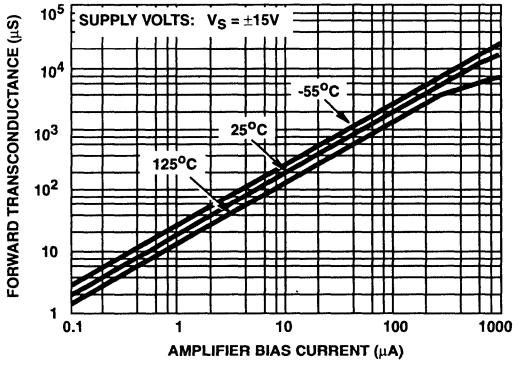


FIGURE 21. TRANSCONDUCTANCE vs AMPLIFIER BIAS CURRENT

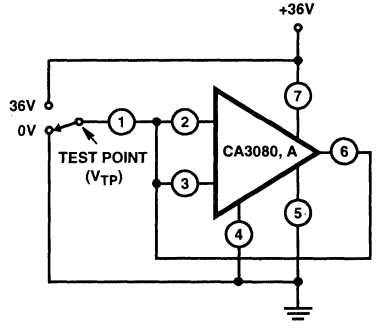


FIGURE 22. LEAKAGE CURRENT TEST CIRCUIT

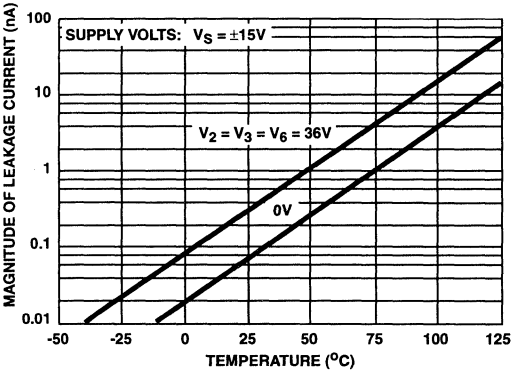


FIGURE 23. LEAKAGE CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

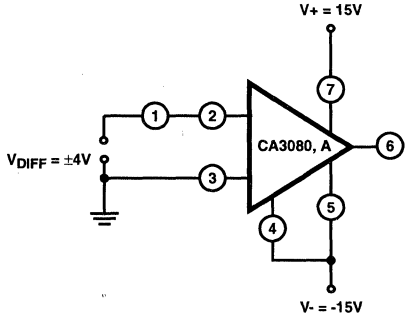


FIGURE 24. DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

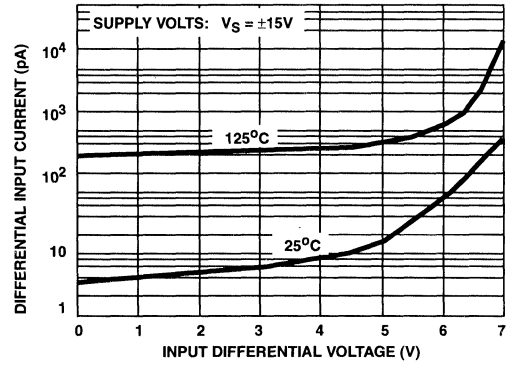


FIGURE 25. INPUT CURRENT vs INPUT DIFFERENTIAL VOLTAGE

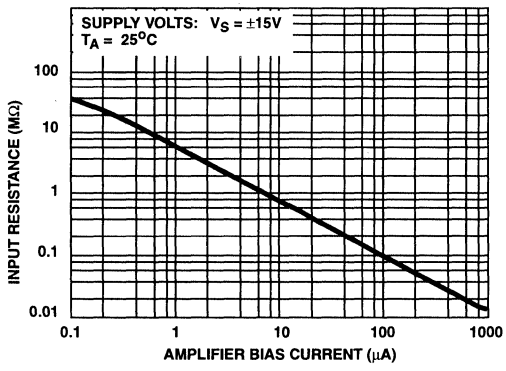


FIGURE 26. INPUT RESISTANCE vs AMPLIFIER BIAS CURRENT

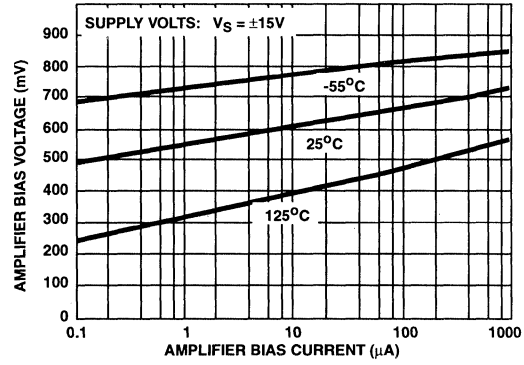


FIGURE 27. AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT

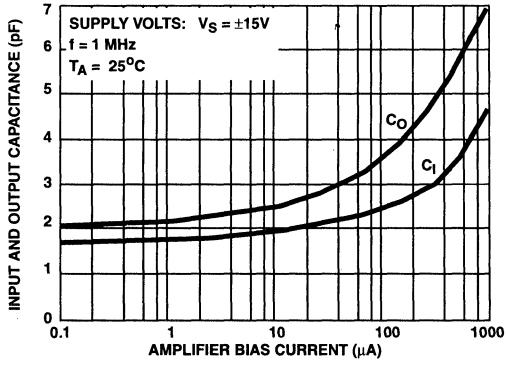


FIGURE 28. INPUT AND OUTPUT CAPACITANCE vs AMPLIFIER BIAS CURRENT

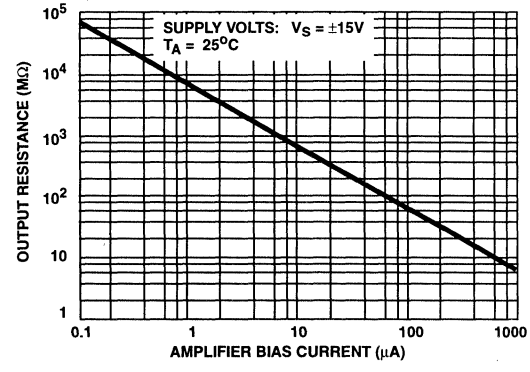


FIGURE 29. OUTPUT RESISTANCE vs AMPLIFIER BIAS CURRENT

Typical Performance Curves (Continued)

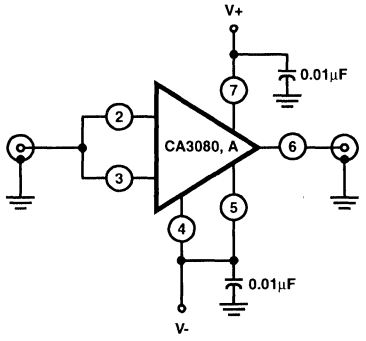


FIGURE 30. INPUT-TO-OUTPUT CAPACITANCE TEST CIRCUIT

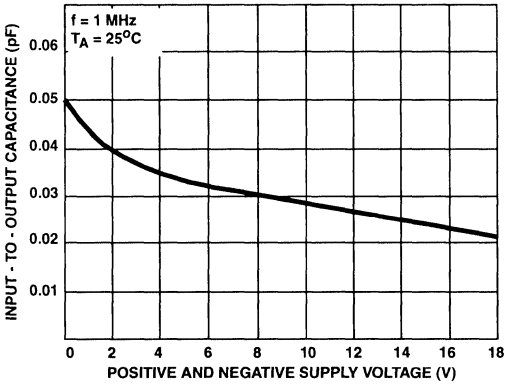


FIGURE 31. INPUT-TO-OUTPUT CAPACITANCE vs SUPPLY VOLTAGE

NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

November 1996

CA3094, CA3094A, CA3094B

30MHz, High Output Current Operational Transconductance Amplifier (OTA)

Features

- CA3094T, E, M for Operation Up to 24V
- CA3094AT, E, M for Operation Up to 36V
- CA3094BT, M for Operation Up to 44V
- Designed for Single or Dual Power Supply
- Programmable: Strobing, Gating, Squelching, AGC Capabilities
- Can Deliver 3W (Average) or 10W (Peak) to External Load (in Switching Mode)
- High Power, Single Ended Class A Amplifier will Deliver Power Output of 0.6W (1.6W Device Dissipation)
- Total Harmonic Distortion (THD) at 0.6W in Class A Operation 1.4% (Typ)

Applications

- Error Signal Detector: Temperature Control with Thermistor Sensor; Speed Control for Shunt Wound DC Motor
- Over Current, Over Voltage, Over Temperature Protectors
- Dual Tracking Power Supply with CA3085
- Wide Frequency Range Oscillator
- Analog Timer
- Level Detector
- Alarm Systems
- Voltage Follower
- Ramp Voltage Generator
- High Power Comparator
- Ground Fault Interrupter (GFI) Circuits

Description

The CA3094 is a differential input power control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional control output signal up to 100mA. This signal is sufficient to directly drive high current thyristors, relays, DC loads, or power transistors. The CA3094 has the generic characteristics of the CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100mA.

The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100µA, a 1mV change at the input will change the output from 0 to 100µA (typical).

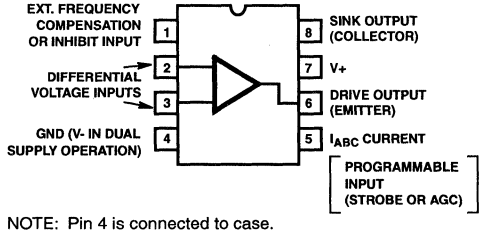
The CA3094 is intended for operation up to 24V and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24V is a primary design requirement (see Figures 28, 29 and 30 in Typical Applications text). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36V and 44V, respectively (single or dual supply).

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3094T, AT, BT	-55 to 125	8 Pin Metal Can	T8.C
CA3094E, AE, BE	-55 to 125	8 Ld PDIP	E8.3
CA3094M, AM, BM (3094, A, B)	-55 to 125	8 Ld SOIC	M8.15

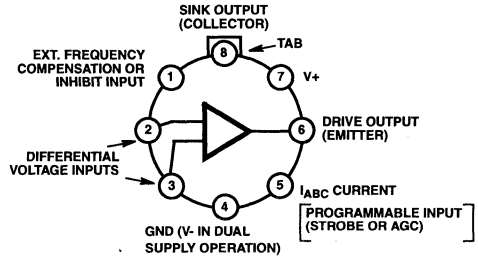
Pinouts

CA3094 (PDIP, SOIC)
TOP VIEW



NOTE: Pin 4 is connected to case.

CA3094 (METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **598.4**

CA3100

November 1996

38MHz, Operational Amplifier

Features

- High Open Loop Gain at Video Frequencies ..... 42dB (Typ) at 1MHz
- Unity Gain Crossover Frequency (f_T) ..... 38MHz (Typ)
- Full Power Bandwidth $V_O = 18V_{P-P}$ ..... 1.2MHz (Typ)
- Slew Rate
  - 20dB Amplifier ..... 70V/μs (Typ)
  - Unity Gain Amplifier..... 25V/μs (Typ)
- Settling Time ..... 0.6μs (Typ)
- Output Current..... ±15mA (Min)
- Single Capacitor Compensation
- Offset Null Terminals

Applications

- Video Amplifiers
- Fast Peak Detectors
- Meter Driver Amplifiers
- High Frequency Feedback Amplifiers
- Video Pre-Drivers
- Oscillators
- Multivibrators
- Voltage Controlled Oscillator
- Fast Comparators

Description

The CA3100 is a large signal wideband, high speed operational amplifier which has a unity gain cross over frequency (f_T) of approximately 38MHz and an open loop, 3dB corner frequency of approximately 110kHz. It can operate at a total supply voltage of from 14V to 36V (±7V to ±18V when using split supplies) and can provide at least $18V_{P-P}$ and $30mA_{P-P}$ at the output when operating from ±15V supplies. The CA3100 can be compensated with a single external capacitor and has DC offset adjust terminals for those applications requiring offset null. (See Figure 1).

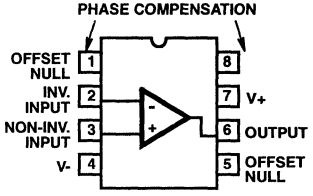
The CA3100 circuit contains both bipolar and PMOS transistors on a single monolithic chip.

Ordering Information

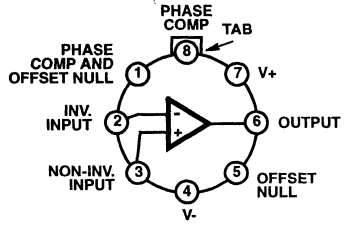
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3100E	-40 to 85	8 Ld PDIP	E8.3
CA3100M (3100)	-40 to 85	8 Ld SOIC	M8.15
CA3100T	-55 to 125	8 Pin Metal Can	T8.C

Pinouts

CA3100
(PDIP, SOIC)
TOP VIEW



CA3100
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 36V
Differential Input Voltage 12V
Input Voltage to Ground . . . . . V+ to V-
Offset Terminal to V- Terminal Voltage . . . . . ±0.5V
Output Current (Note 2) 50mA

Operating Conditions

Temperature Range
CA3100E, CA3100M . . . . . -40°C to 85°C
CA3100T . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	100	N/A
SOIC Package	165	N/A
Metal Can Package	170	85

Maximum Junction Temperature (Metal Can) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. CA3100 does not contain circuitry to protect against short circuits in the output.

Electrical Specifications $T_A = 25°C$, $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC						
Input Offset Voltage	V_{IO}	$V_O = 0$ ±0.1V	-	±1	±5	mV
Input Bias Current	I_{IB}	$V_O = 0$ ±1V	-	0.7	2	µA
Input Offset Current	I_{IO}	$V_O = 0$ ±1V	-	±0.05	±0.4	µA
Common Mode Input Voltage Range	V_{ICR}	CMRR ≥ 76dB	±12	+14 -13	-	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$	76	90	-	dB
Maximum Output Voltage	$V_{OM}+$	Differential Input Voltage = 0 ±0.1V, $R_L = 2k\Omega$	+9	+11	-	V
	$V_{OM}-$		-9	-11	-	V
Maximum Output Current	$I_{OM}+$	Differential Input Voltage = 0 + 0.1V, $R_L = 250\Omega$	+15	+30	-	mA
	$I_{OM}-$		-15	-30	-	mA
Supply Current	I+	$V_O = 0$ ±0.1V, $R_L \geq 10k\Omega$	-	8.5	10.5	mA
Power Supply Rejection Ratio	PSRR	$\Delta V+ = \pm 1V$, $\Delta V- = \pm 1V$	60	70	-	dB
DYNAMIC						
Unity-Gain Crossover Frequency	f_T	$C_C = 0$, $V_O = 0.3V_{P-P}$	-	38	-	MHz
Open Loop Voltage Gain	A_{OL}	f = 1kHz, $V_O = \pm 1V$, (Note 3)	56	61	-	dB
		f = 1MHz, $C_C = 0$, $V_O = 10V_{P-P}$	36	42	-	dB
Slew Rate	SR	$A_V = 10$, $C_C = 0$, $V_I = 1V$ (Pulse)	50	70	-	V/µs
		$A_V = 1$, $C_C = 10pF$, $V_I = 10V$ (Pulse)	-	25	-	V/µs
Full Power Bandwidth (Note 4)	FPBW	$A_V = 10$, $C_C = 0$, $V_O = 18V_{P-P}$	0.8	1.2	-	MHz
		$A_V = 1$, $C_C = 10pF$, $V_O = 18V_{P-P}$	-	0.4	-	MHz
Open Loop Differential Input Impedance	Z_I	f = 1MHz	-	30	-	kΩ
Open Loop Output Impedance	Z_O	f = 1MHz	-	110	-	Ω

Electrical Specifications $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Wideband Noise Voltage (RTI)	e_N (Total)	BW = 1MHz, R_S = 1kΩ	-	8	-	μV_{RMS}
Settling Time (To Within ±50mV of 9V Output Swing)	t_S	R_L = 2kΩ, C_L = 20pF	-	0.6	-	μs

NOTES:

3. Low frequency dynamic characteristic.
4. Full Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_{OP-P}}$.

Test Circuits

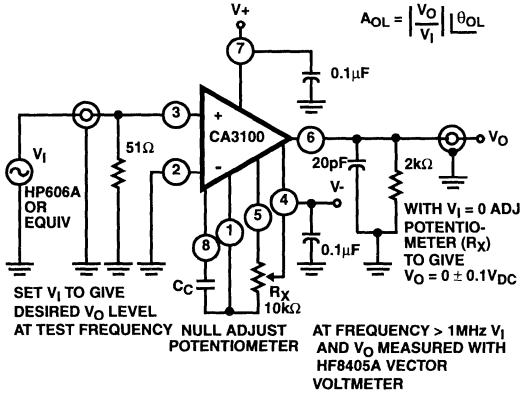


FIGURE 1. OPEN-LOOP VOLTAGE GAIN TEST CIRCUIT AND OFFSET ADJUST CIRCUIT

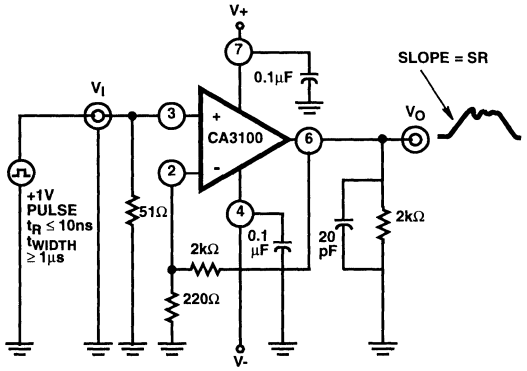


FIGURE 2. SLEW RATE IN 10X AMPLIFIER TEST CIRCUIT

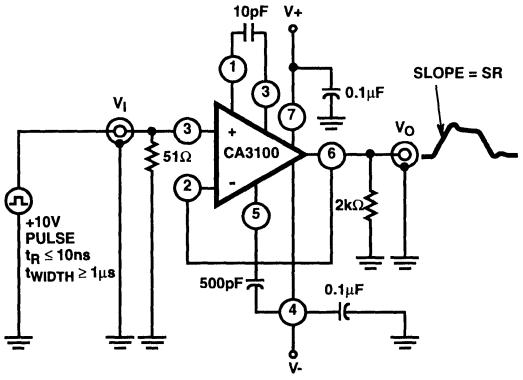


FIGURE 3. FOLLOWER SLEW RATE TEST CIRCUIT

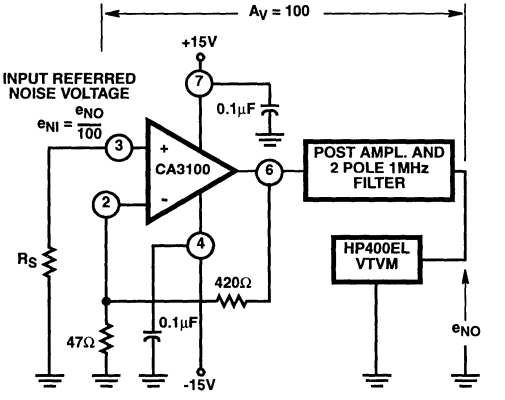


FIGURE 4. WIDEBAND INPUT NOISE VOLTAGE TEST CIRCUIT

Test Circuits (Continued)

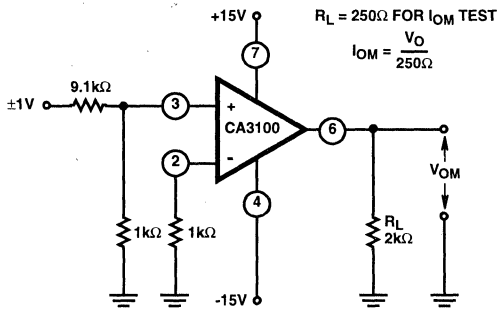


FIGURE 5. OUTPUT VOLTAGE SWING (V_{OM}), OUTPUT CURRENT SWING (I_{OM}) TEST CIRCUIT

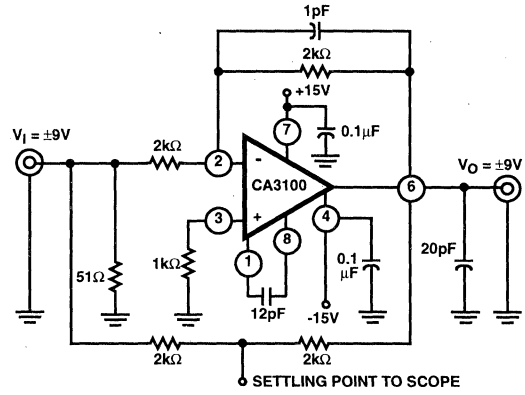
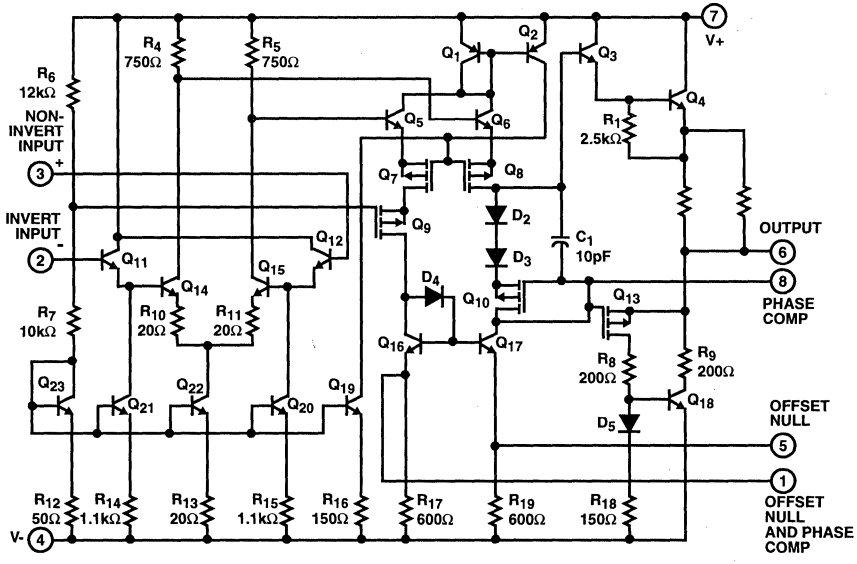


FIGURE 6. SETTLING TIME TEST CIRCUIT

Schematic Diagram



Typical Applications

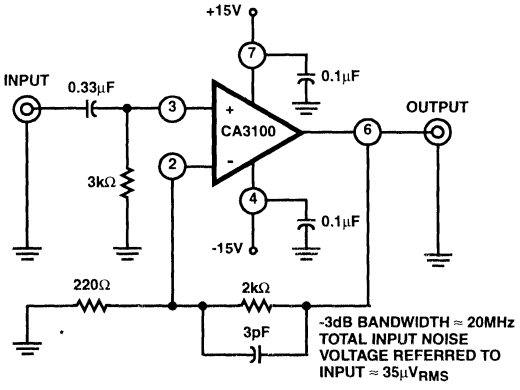


FIGURE 7. 20dB VIDEO AMPLIFIER

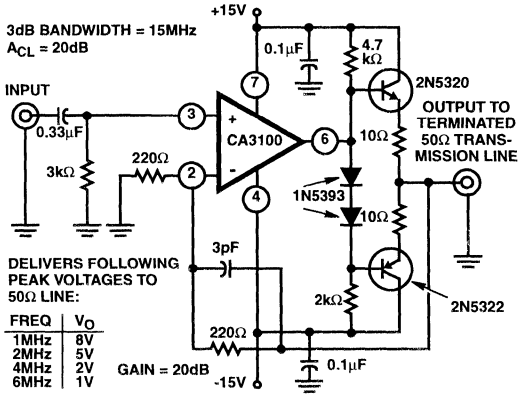


FIGURE 8. 20dB VIDEO LINE DRIVER

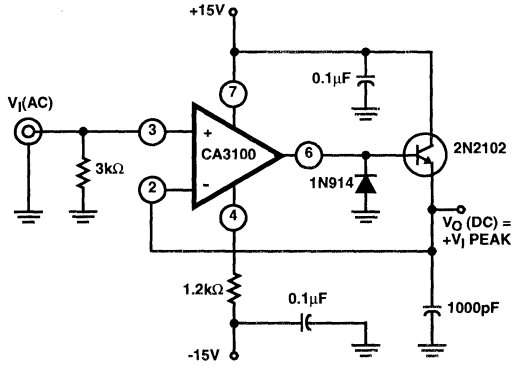


FIGURE 9. FAST POSITIVE PEAK DETECTOR

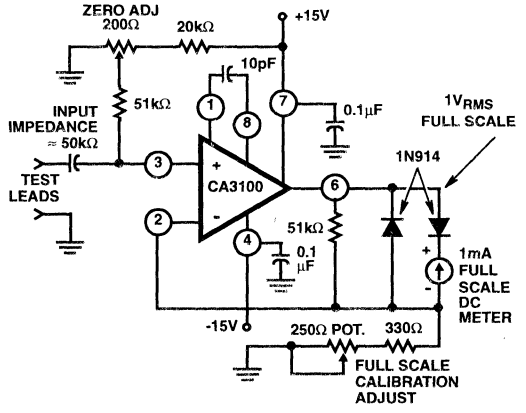


FIGURE 10. 1MHz METER-DRIVER AMPLIFIER

Typical Performance Curves

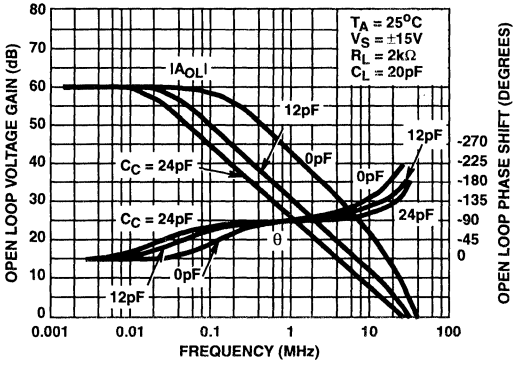


FIGURE 11. OPEN LOOP GAIN, OPEN LOOP PHASE SHIFT vs FREQUENCY

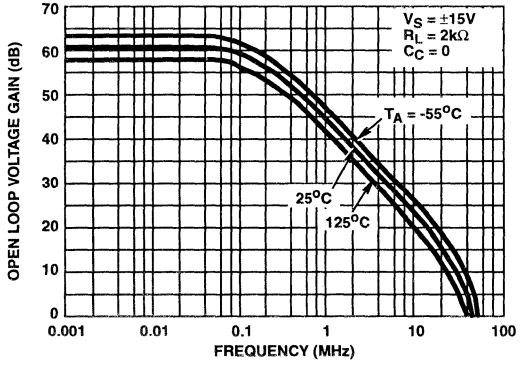


FIGURE 12. OPEN LOOP GAIN vs FREQUENCY

Typical Performance Curves (Continued)

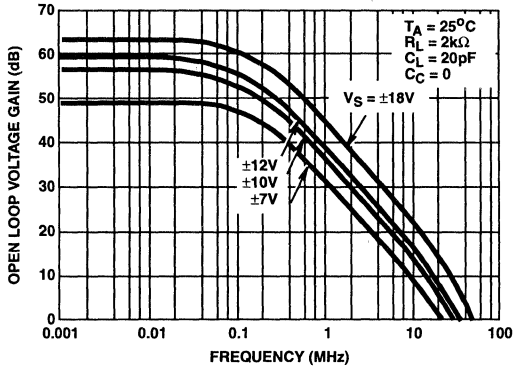


FIGURE 13. OPEN LOOP GAIN vs FREQUENCY

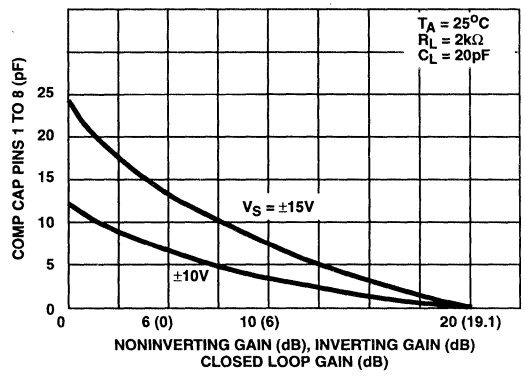


FIGURE 14. REQUIRED COMPENSATION CAPACITANCE vs CLOSED LOOP GAIN

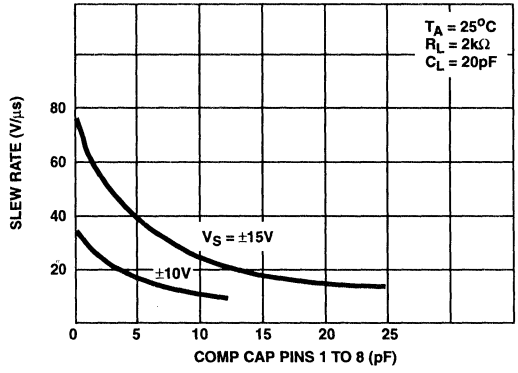


FIGURE 15. SLEW RATE vs COMPENSATION CAPACITANCE

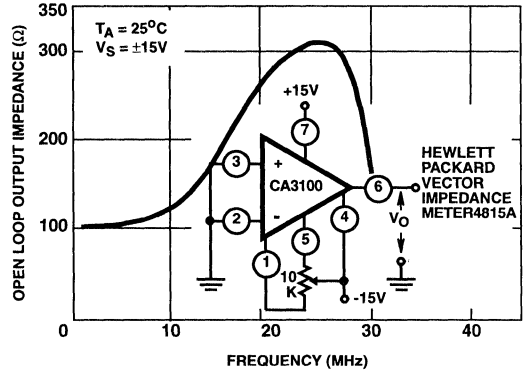


FIGURE 16. TYPICAL OPEN LOOP OUTPUT IMPEDANCE vs FREQUENCY

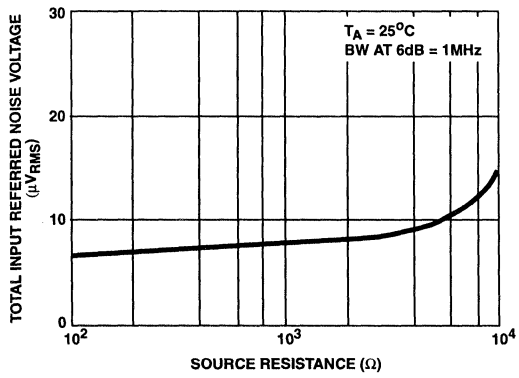


FIGURE 17. WIDEBAND INPUT NOISE VOLTAGE vs SOURCE RESISTANCE

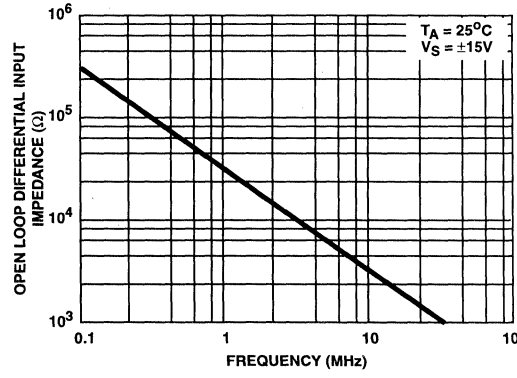


FIGURE 18. TYPICAL OPEN LOOP DIFFERENTIAL INPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

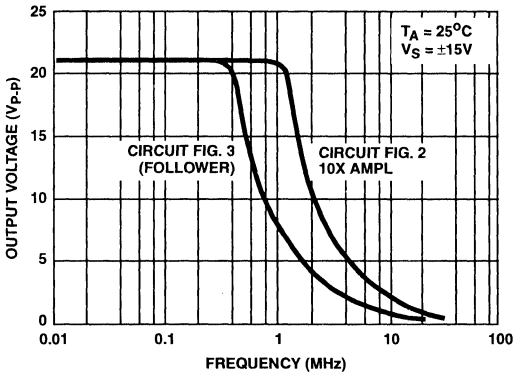


FIGURE 19. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

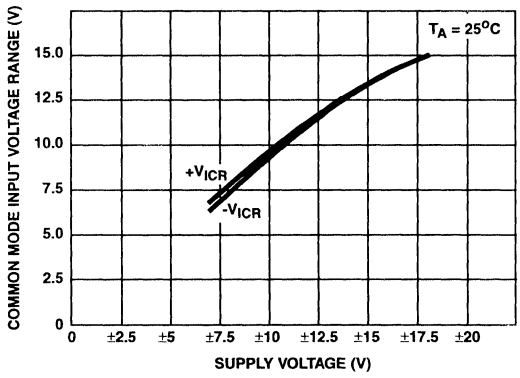


FIGURE 20. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

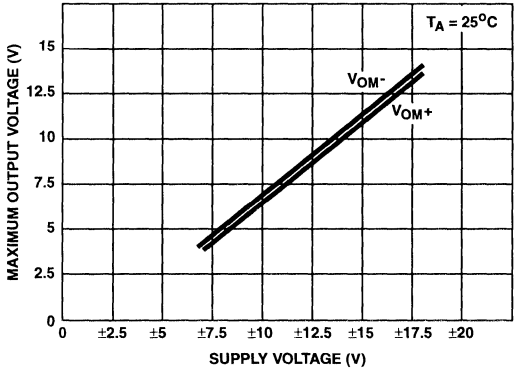


FIGURE 21. MAXIMUM OUTPUT VOLTAGE vs SUPPLY VOLTAGE

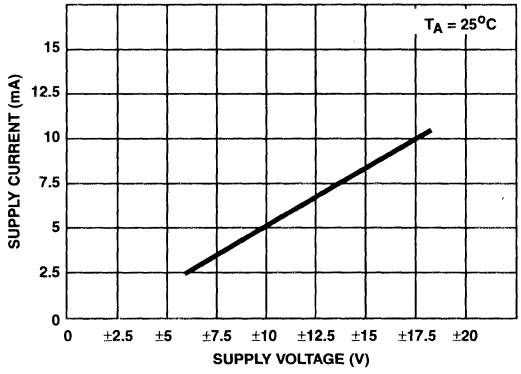


FIGURE 22. SUPPLY CURRENT vs SUPPLY VOLTAGE

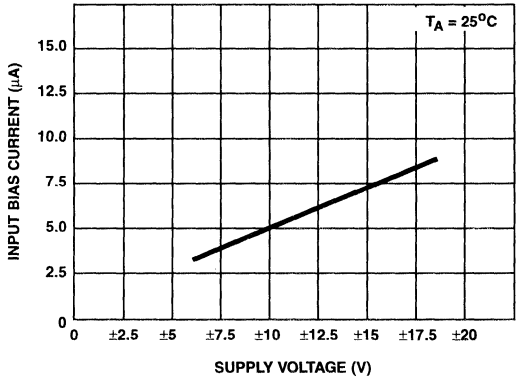


FIGURE 23. INPUT BIAS CURRENT vs SUPPLY VOLTAGE

HARRIS SEMICONDUCTOR

CA3130, CA3130A

15MHz, BiMOS Operational Amplifier with MOSFET Input/CMOS Output

November 1996

Features

- MOSFET Input Stage Provides:
  - Very High Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I = 5pA (Typ) at 15V Operation
    = 2pA (Typ) at 5V Operation
- Ideal for Single-Supply Applications
- Common-Mode Input-Voltage Range Includes Negative Supply Rail; Input Terminals can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or both) Supply Rails

Applications

- Ground-Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long-Duration Timers/Monostables
- High-Input-Impedance Comparators (Ideal Interface with Digital CMOS)
- High-Input-Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single-Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Peak Detectors
- Single-Supply Full-Wave Precision Rectifiers
- Photo-Diode Sensor Amplifiers

Description

CA3130A and CA3130 are op amps that combine the advantage of both CMOS and bipolar transistors.

Gate-protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS transistors in the input stage results in common-mode input-voltage capability down to 0.5V below the negative-supply terminal, an important attribute in single-supply applications.

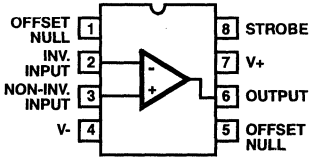
A CMOS transistor-pair, capable of swinging the output voltage to within 10mV of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5V to 16V, (±2.5V to ±8V). They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

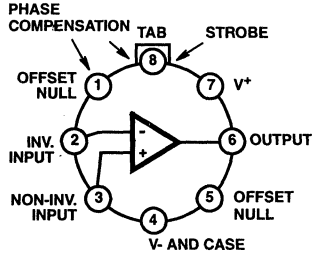
The CA3130A offers superior input characteristics over those of the CA3130.

Pinouts

CA3131, CA3130A
(PDIP, SOIC)
TOP VIEW



CA3130, CA3130A
(METAL CAN)
TOP VIEW



Ordering Information

PART NO. (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3130AE	-55 to 125	8 Ld PDIP	E8.3
CA3130AM (3130A)	-55 to 125	8 Ld SOIC	M8.15
CA3130AM96 (3130A)	-55 to 125	8 Ld SOIC (Note)	M8.15
CA3130AT	-55 to 125	8 Pin Metal Can	T8.C
CA3130BT	-55 to 125	8 Pin Metal Can	T8.C
CA3130E	-55 to 125	8 Ld PDIP	E8.3
CA3130M (3130)	-55 to 125	8 Ld SOIC	M8.15
CA3130M96 (3130)	-55 to 125	8 Ld SOIC (Note)	M8.15
CA3130T	-55 to 125	8 Pin Metal Can	T8.C

NOTE: Denotes Tape and Reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **817.3**

Absolute Maximum Ratings

DC Supply Voltage (Between V+ And V- Terminals) 16V
Differential Input Voltage. 8V
DC Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Input-Terminal Current 1mA
Output Short-Circuit Duration (Note 1). . . . . Indefinite

Operating Conditions

Temperature Range . . . . . $-50^{o}C$ to $125^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
PDIP Package	100	N/A
SOIC Package	160	N/A
Metal Can Package	170	85

Maximum Junction Temperature (Metal Can Package). . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s). . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$T_A = 25^{o}C$, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3130			CA3130A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\lvert V_{IO}\rvert$	$V_S = \pm 7.5V$	-	8	15	-	2	5	mV
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	10	-	-	10	-	$\mu V/^{o}C$
Input Offset Current	$\lvert I_{IO}\rvert$	$V_S = \pm 7.5V$	-	0.5	30	-	0.5	20	pA
Input Current	I_I	$V_S = \pm 7.5V$	-	5	50	-	5	30	pA
Large-Signal Voltage Gain	A_{OL}	$V_O = 10V_{P-P}$, $R_L = 2k\Omega$	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common-Mode Rejection Ratio	CMRR		70	90	-	80	90	-	dB
Common-Mode Input Voltage Range	V_{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V_S$	$V_S = \pm 7.5V$	-	32	320	-	32	150	$\mu V/V$
Maximum Output Voltage	V_{OM+}	$R_L = 2k\Omega$	12	13.3	-	12	13.3	-	V
	V_{OM-}	$R_L = 2k\Omega$	-	0.002	0.01	-	0.002	0.01	V
	V_{OM+}	$R_L = \infty$	14.99	15	-	14.99	15	-	V
	V_{OM-}	$R_L = \infty$	-	0	0.01	-	0	0.01	V
Maximum Output Current	I_{OM+} (Source) at $V_O = 0V$		12	22	45	12	22	45	mA
	I_{OM-} (Sink) at $V_O = 15V$		12	20	45	12	20	45	mA
Supply Current	I+	$V_O = 7.5V$, $R_L = \infty$	-	10	15	-	10	15	mA
	I+	$V_O = 0V$, $R_L = \infty$	-	2	3	-	2	3	mA

Electrical Specifications Typical Values Intended Only for Design Guidance, $V_{SUPPLY} = \pm 7.5V$, $T_A = 25^oC$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3130, CA3130A	UNITS
Input Offset Voltage Adjustment Range		10kΩ Across Terminals 4 and 5 or 4 and 1	±22	mV
Input Resistance	R_I		1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	pF
Equivalent Input Noise Voltage	e_N	BW = 0.2MHz, R_S = 1MΩ (Note 3)	23	μV
Open Loop Unity Gain Crossover Frequency (For Unity Gain Stability ≥47pF Required.)	f_T	C_C = 0	15	MHz
		C_C = 47pF	4	MHz
Slew Rate:	SR			
Open Loop		C_C = 0	30	V/μs
Closed Loop		C_C = 56pF	10	V/μs
Transient Response:		C_C = 56pF, C_L = 25pF, R_L = 2kΩ (Voltage Follower)		
Rise Time	t_r		0.09	μs
Overshoot	OS		10	%
Settling Time (To <0.1%, $V_{IN} = 4V_{P-P}$)	t_S		1.2	μs

NOTE:

3. Although a 1MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10MΩ.

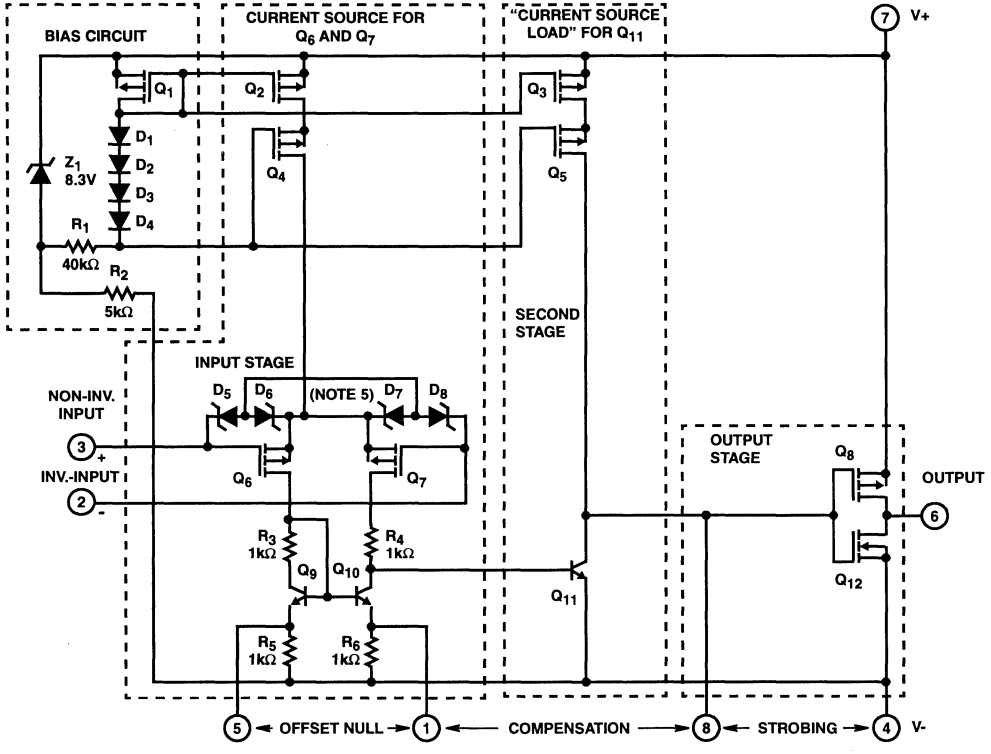
Electrical Specifications Typical Values Intended Only for Design Guidance, V+ = 5V, V- = 0V, $T_A = 25^oC$ Unless Otherwise Specified (Note 4)

PARAMETER	SYMBOL	TEST CONDITIONS	CA3130	CA3130A	UNITS
Input Offset Voltage	V_{IO}		8	2	mV
Input Offset Current	I_{IO}		0.1	0.1	pA
Input Current	I_I		2	2	pA
Common-Mode Rejection Ratio	CMRR		80	90	dB
Large-Signal Voltage Gain	A_{OL}	$V_O = 4V_{P-P}$, R_L = 5kΩ	100	100	kV/V
			100	100	dB
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current	I+	V_O = 5V, $R_L = \infty$	300	300	μA
		V_O = 2.5V, $R_L = \infty$	500	500	μA
Power Supply Rejection Ratio	$\Delta V_{IO}/\Delta V+$		200	200	μV/V

NOTE:

4. Operation at 5V is not recommended for temperatures below 25^oC.

Schematic Diagram



NOTE:

5. Diodes D_5 through D_8 provide gate-oxide protection for MOSFET input stage.

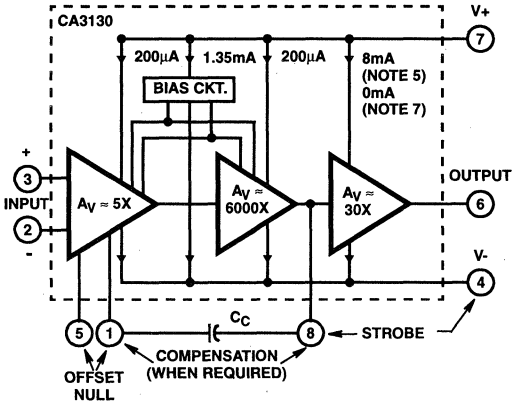
Application Information

Circuit Description

Figure 1 is a block diagram of the CA3130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Figure 1, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Terminal 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g.,when the amplifier output is used to drive CMOS digital circuits in Comparator applications).

Input Stage

The circuit of the CA3130 is shown in the schematic diagram. It consists of a differential-input stage using PMOS field-effect transistors (Q_6, Q_7) working into a mirror-pair of bipolar transistors (Q_9, Q_{10}) functioning as load resistors together with resistors R_3 through R_6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q_{11}). Offset nulling, when desired, can be effected by connecting a 100,000Ω potentiometer across Terminals 1 and 5 and the potentiometer slider arm to Terminal 4. Cascade-connected PMOS transistors Q_2, Q_4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D_5 through D_8 provide gate-oxide protection against high-voltage transients, including static electricity during handling for Q_6 and Q_7.



NOTES:

6. Total supply voltage (for indicated voltage gains) = 15V with input terminals biased so that Terminal 6 potential is +7.5V above Terminal 4.
7. Total supply voltage (for indicated voltage gains) = 15V with output terminal driven to either supply rail.

FIGURE 1. BLOCK DIAGRAM OF THE CA3130 SERIES

Second-Stage

Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q_{11} and its cascade-connected load resistance provided by PMOS transistors Q_3 and Q_5. The source of bias potentials for these PMOS transistors is subsequently described. Miller Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terminals 1 and 8. A 47pF capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit

At total supply voltages, somewhat above 8.3V, resistor R_2 and zener diode Z_1 serve to establish a voltage of 8.3V across the series-connected circuit, consisting of resistor R_1, diodes D_1 through D_4, and PMOS transistor Q_1. A tap at the junction of resistor R_1 and diode D_4 provides a gate-bias potential of about 4.5V for PMOS transistors Q_4 and Q_5 with respect to Terminal 7. A potential of about 2.2V is developed across diode-connected PMOS transistor Q_1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q_2 and Q_3. It should be noted that Q_1 is "mirror-connected (see Note 8)" to both Q_2 and Q_3. Since transistors Q_1, Q_2, Q_3 are designed to be identical, the approximately 200µA current in Q_1 establishes a similar current in Q_2 and Q_3 as constant current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3V, zener diode Z_1 becomes nonconductive and the potential, developed across series-connected R_1, D_1-D_4, and Q_1, varies directly with variations in supply voltage. Consequently, the gate bias for Q_4, Q_5 and Q_2, Q_3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3V. Operation at total supply voltages below about 4.5V results in seriously degraded performance.

Output Stage

The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 2. Typical op amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01% accuracy levels, including the negative supply rail.

NOTE:

8. For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see File Number 619, data sheet on CA3600E "CMOS Transistor Array".

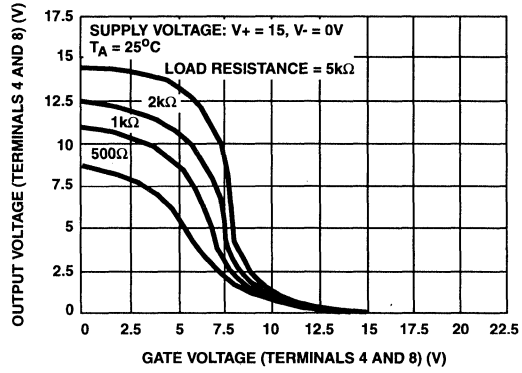


FIGURE 2. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS OUTPUT STAGE

Input Current Variation with Common Mode Input Voltage

As shown in the Table of Electrical Specifications, the input current for the CA3130 Series Op Amps is typically 5pA at $T_A = 25^oC$ when Terminals 2 and 3 are at a common-mode potential of +7.5V with respect to negative supply Terminal 4. Figure 3 contains data showing the variation of input current as a function of common-mode input voltage at $T_A = 25^oC$. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common-mode input voltage does not exceed 2V. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the

metal can package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the Metal Can case of the CA3130 is also internally tied to Terminal 4, input Terminal 3 is essentially "guarded" from spurious leakage currents.

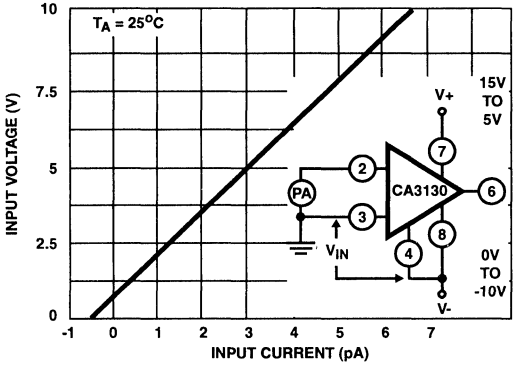


FIGURE 3. INPUT CURRENT vs COMMON-MODE VOLTAGE

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000Ω potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Figure 4 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

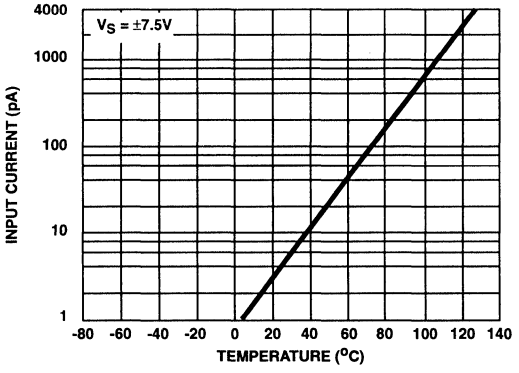


FIGURE 4. INPUT CURRENT vs TEMPERATURE

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input Offset Voltage (V_{IO}) Variation with DC Bias and Device Operating Life

It is well known that the characteristics of a MOSFET device can change slightly when a DC gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential DC bias voltage applied across Terminals 2 and 3. Figure 5 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (metal can package) during life testing. At lower temperatures (metal can and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The $2V_{DC}$ differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

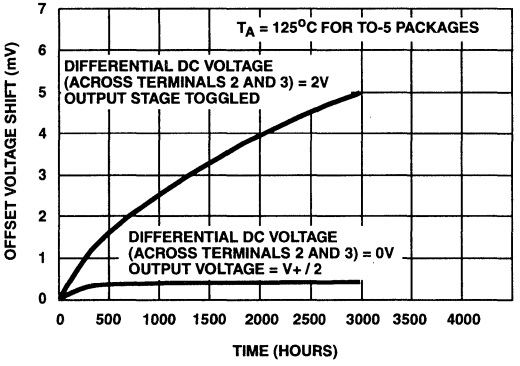


FIGURE 5. TYPICAL INCREMENTAL OFFSET-VOLTAGE SHIFT vs OPERATING LIFE

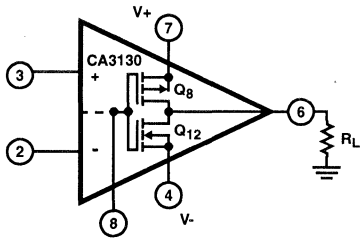


FIGURE 6A. DUAL POWER SUPPLY OPERATION

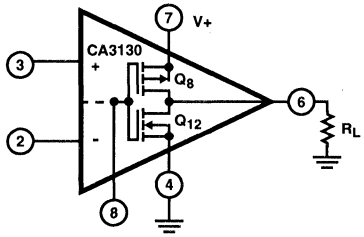


FIGURE 6B. SINGLE POWER SUPPLY OPERATION

FIGURE 6. CA3130 OUTPUT STAGE IN DUAL AND SINGLE POWER SUPPLY OPERATION

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single-and dual-supply service. Figures 6A and 6B show the CA3130 connected for both dual-and single-supply operation.

Dual-supply Operation: When the output voltage at Terminal 6 is 0V, the currents supplied by the two power supplies are equal. When the gate terminals of Q_8 and Q_{12} are driven increasingly positive with respect to ground, current flow through Q_{12} (from the negative supply) to the load is increased and current flow through Q_8 (from the positive supply) decreases correspondingly. When the gate terminals of Q_8 and Q_{12} are driven increasingly negative with respect to ground, current flow through Q_8 is increased and current flow through Q_{12} is decreased accordingly.

Single-supply Operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage drops across Q_8 and Q_{12} are of equal magnitude. Figure 20 shows typical quiescent supply-current vs supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Figure 2). If either Q_8 or Q_{12} are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q_{12} is completely cut off and the supply-current to series-connected transistors Q_8, Q_{12} goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Figure 20) even though the output stage is strobed off. Figure 6A shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$ by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2kΩ) is connected between Terminal 6 and ground in the circuit of Figure 6B. Let it be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2. Since PMOS transistor Q_8 must now supply quiescent current to both R_L and transistor Q_{12}, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Figure 22 shows the voltage-drop across PMOS transistor Q_8 as a function of load current at several supply voltages. Figure 2 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is on the order of 1MΩ or more. In this case, the total input-referred noise voltage is typically only 23μV when the test-circuit amplifier of Figure 7 is operated at a total supply voltage of 15V. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1MΩ, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

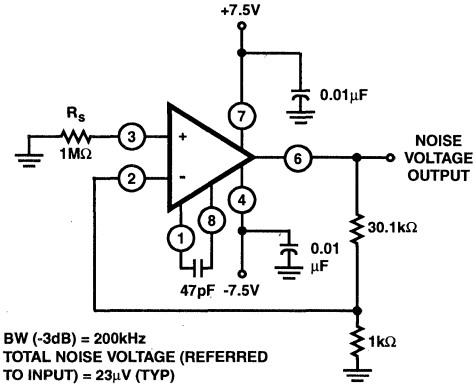


FIGURE 7. TEST-CIRCUIT AMPLIFIER (30-dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENTS

Typical Applications

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Figure 8 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Figure 9, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 9A with input-signal ramping. The waveforms in Figure 9B show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5V below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 9B also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described later, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.

9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC) is shown in Figure 10. This system combines the concepts of multiple-switch CMOS ICs, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10V logic levels are used in the circuit of Figure 10.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of 1% tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000Ω resistors from the same manufacturing lot.

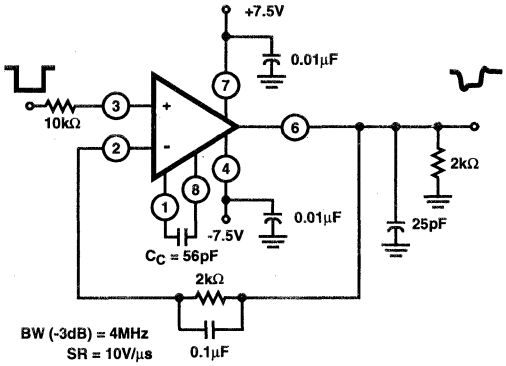
A single 15V supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10V level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

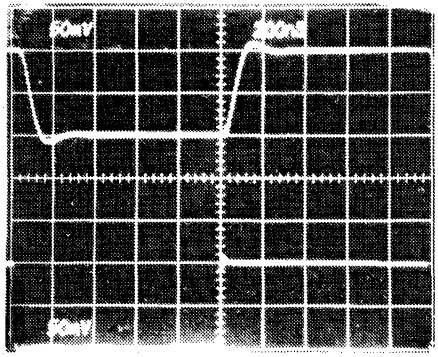
Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Figure 11. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to $-R_2/R_1$. When the equality of the two equations shown in Figure 11 is satisfied, the full-wave output is symmetrical.

Peak Detectors

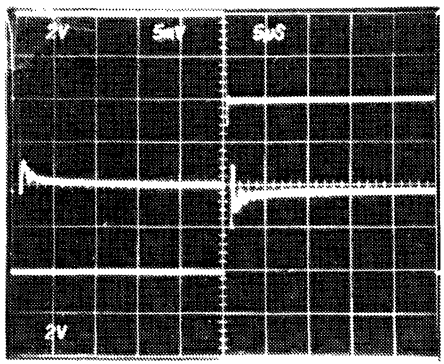
Peak-detector circuits are easily implemented with the CA3130, as illustrated in Figure 12 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q_{11}, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q_{11}, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.





Top Trace: Output
Center Trace: Input

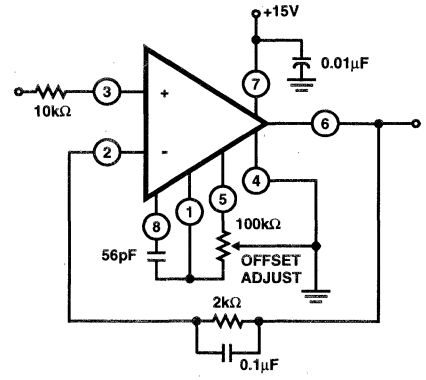
FIGURE 8A. SMALL-SIGNAL RESPONSE (50mV/DIV., 200ns/DIV.)



Top Trace: Output Signal; 2V/Div., 5µs/Div.
Center Trace: Difference Signa; 5mV/Div., 5µs/Div.
Bottom Trace: Input Signal; 2V/Div., 5µs/Div.

FIGURE 8B. INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)

FIGURE 8. SPLIT SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS



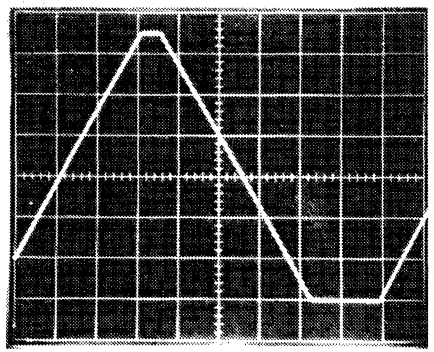
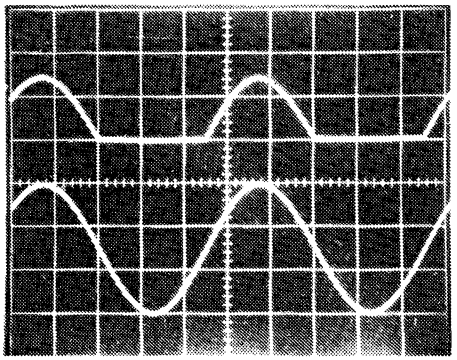


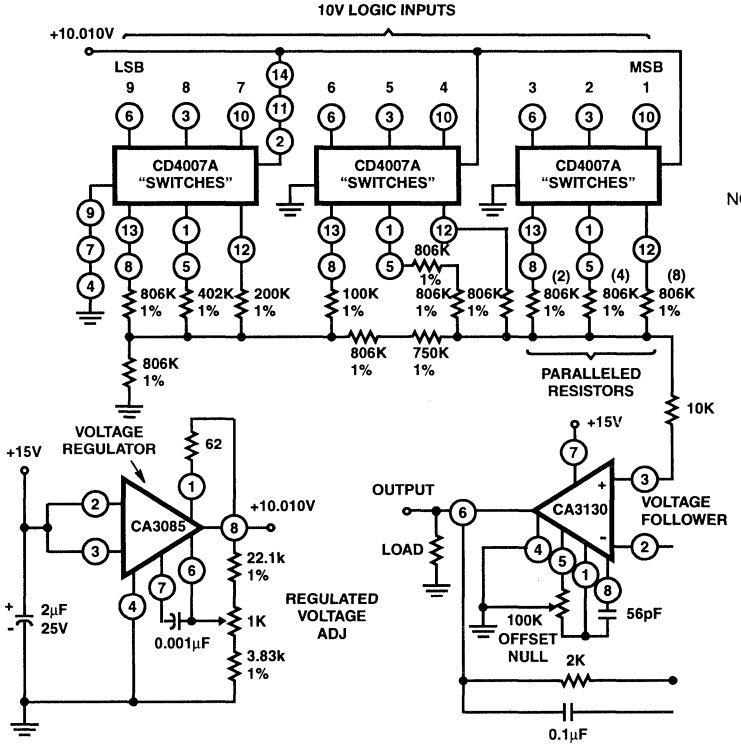
FIGURE 9A. OUTPUT WAVEFORM WITH INPUT SIGNAL RAMPING (2V/DIV., 500µs/DIV.)



Top Trace:Output; 5V/Div., 200µs/Div.
Bottom Trace:Input Signal; 5V/Div., 200µs/Div.

FIGURE 9B. OUTPUT WAVEFORM WITH GROUND REFERENCE SINE-WAVE INPUT

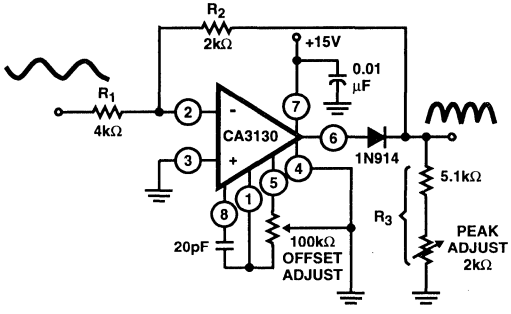
FIGURE 9. SINGLE SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS. (e.g., FOR USE IN SINGLE-SUPPLY D/A CONVERTER; SEE FIGURE 9 IN AN6080)



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS

NOTE: All resistances are in ohms.

FIGURE 10. 9-BIT DAC USING CMOS DIGITAL SWITCHES AND CA3130



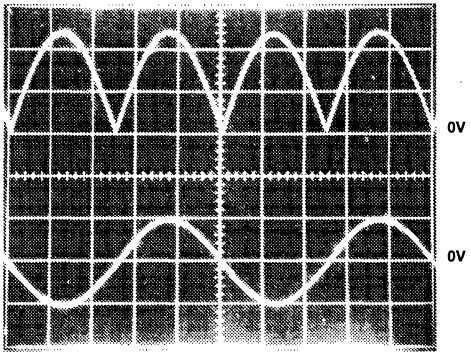
$$\text{Gain} = \frac{R_2}{R_1} = X = \frac{R_3}{R_1 + R_2 + R_3}$$

$$R_3 = R_1\left(\frac{X + X^2}{1 - X}\right)$$

For X = 0.5: $\frac{2K\Omega}{4k\Omega} = \frac{R_2}{R_1}$

$R_3 = 4k\Omega\left(\frac{0.75}{0.5}\right) = 6k\Omega$

$20V_{P-P}$ Input: BW(-3dB) = 230kHz, DC Output (Avg) = 3.2V
$1V_{P-P}$ Input: BW(-3dB) = 130kHz, DC Output (Avg) = 160mV



Top Trace: Output Signal; 2V/Div.
Bottom Trace: Input Signal; 10V/Div.
Time base on both traces: 0.2ms/Div.

FIGURE 11. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL-WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS

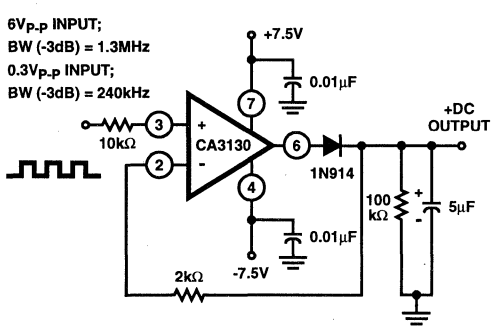


FIGURE 12A. PEAK POSITIVE DETECTOR CIRCUIT

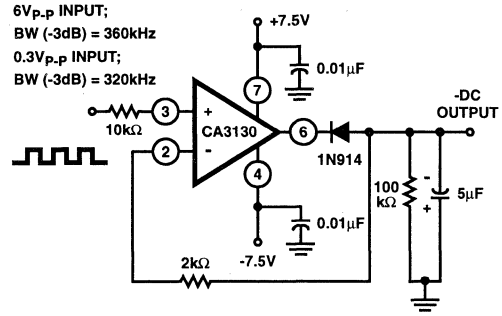
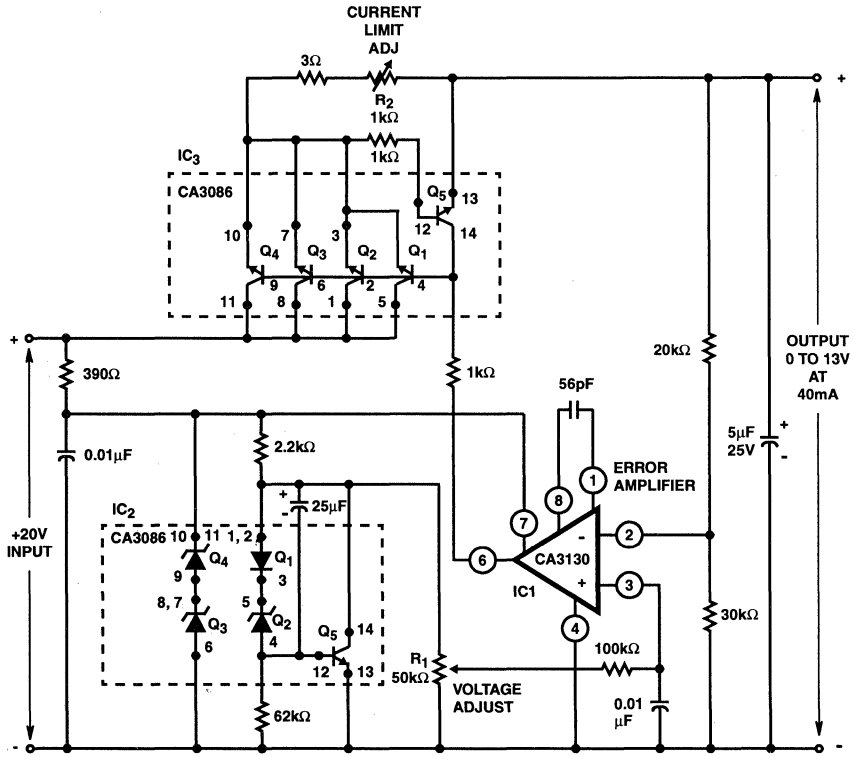


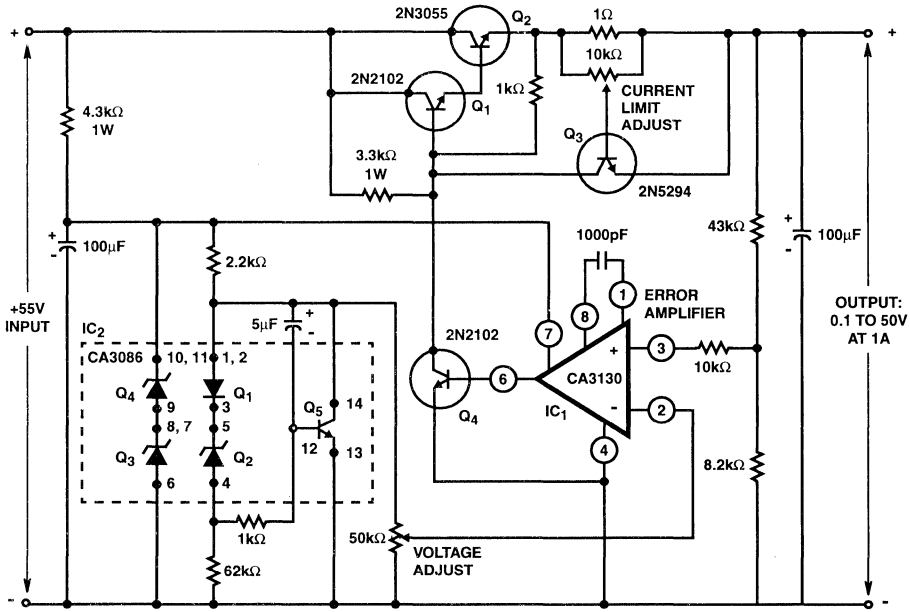
FIGURE 12B. PEAK NEGATIVE DETECTOR CIRCUIT

FIGURE 12. PEAK-DETECTOR CIRCUITS



REGULATION (NO LOAD TO FULL LOAD): <0.01%
INPUT REGULATION: 0.02%/V
HUM AND NOISE OUTPUT: <25µV UP TO 100kHz

FIGURE 13. VOLTAGE REGULATOR CIRCUIT (0V TO 13V AT 40mA)



REGULATION (NO LOAD TO FULL LOAD): <0.005%
INPUT REGULATION: 0.01%/V
HUM AND NOISE OUTPUT: <250μV_{RMS} UP TO 100kHz

FIGURE 14. VOLTAGE REGULATOR CIRCUIT (0.1V TO 50V AT 1A)

Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Figure 13 shows the schematic diagram of a 40mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0V to 13V. Q_3 and Q_4 in IC_2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC_1). Q_1, Q_2, and Q_5 in IC_2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q_1, Q_2, Q_3, and Q_4 in IC_3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q_5 in IC_3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R_2.

Figure 14 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1V to 50V and currents up to 1A. The error amplifier (IC_1) and circuitry associated with IC_2 function as previously described, although the output of IC_1 is boosted by a discrete transistor (Q_4) to provide adequate base drive for the Darlington-connected series-pass transistors Q_1, Q_2. Transistor Q_3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Figure 15. Resistors R_1 and R_2 are used to bias the CA3130 to the mid-point of the supply-voltage and R_3 is the feedback resistor. The pulse repetition rate is selected by positioning S_1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

Figure 16 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1Hz to 100kHz) by means of a single control, R_1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA) (see Note 10), IC_1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C_1, in the feedback loop of the integrator IC_2, using a CA3130, to provide the triangular-wave output. Potentiometer R_2 is used

to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC_3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C_2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R_3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R_4 to the input of IC_1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

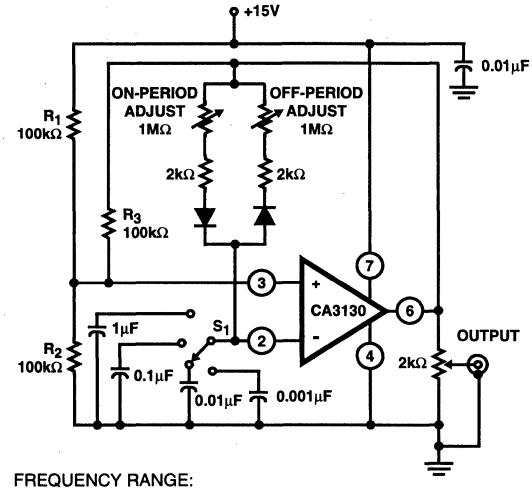
Operation with Output-Stage Power-Booster

The current-sourcing and-sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Figure 17, three CMOS transistor-pairs in a single CA3600E (see Note 12) IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20mA of supply current at 15V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Figure 17 employs feedback to establish a closed-loop gain of 48dB. The typical large-signal bandwidth (-3dB) is 50kHz.

NOTE:

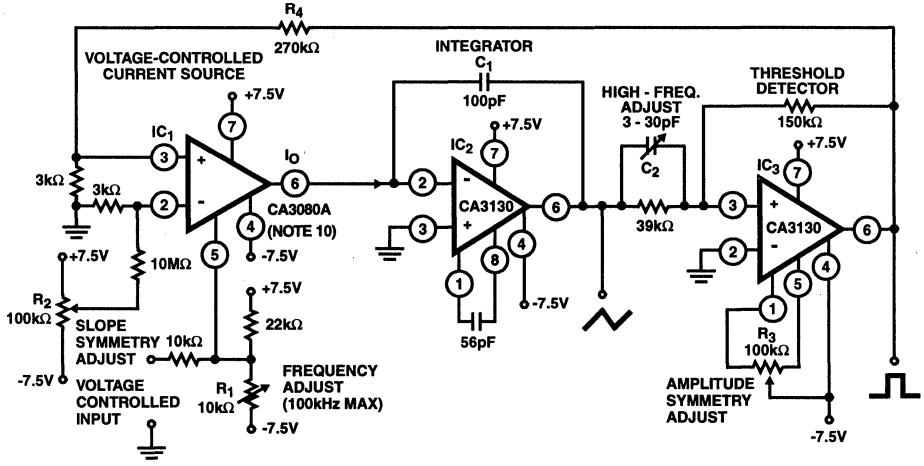
9. See file number 619 for technical information.



FREQUENCY RANGE:

POSITION OF S_1	PULSE PERIOD
0.001µF	4µs to 1ms
0.01µF	40µs to 10ms
0.1µF	0.4ms to 100ms
1µF	4ms to 1s

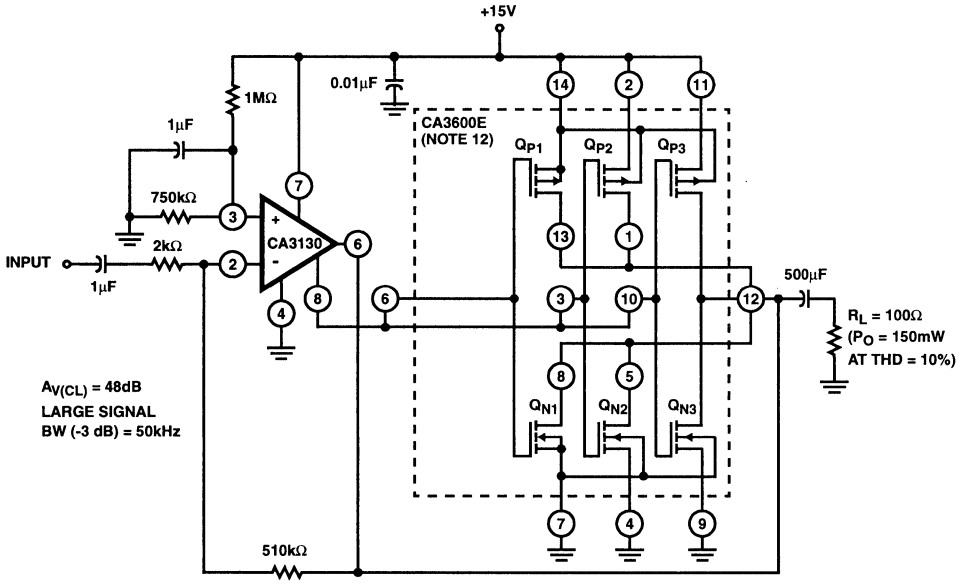
FIGURE 15. PULSE GENERATOR (ASTABLE MULTIVIBRATOR) WITH PROVISIONS FOR INDEPENDENT CONTROL OF "ON" AND "OFF" PERIODS



NOTE:

10. See file number 475 and AN6668 for technical information.

FIGURE 16. FUNCTION GENERATOR (FREQUENCY CAN BE VARIED 1,000,000/1 WITH A SINGLE CONTROL)



NOTES:

11. Transistors Q_{P1}, Q_{P2}, Q_{P3} and Q_{N1}, Q_{N2}, Q_{N3} are parallel connected with Q_8 and Q_{12}, respectively, of the CA3130.
12. See file number 619.

FIGURE 17. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA3130

Typical Performance Curves

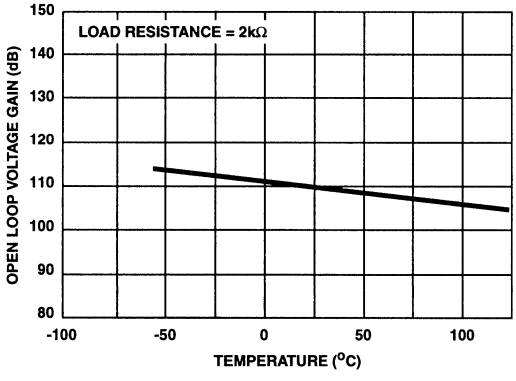
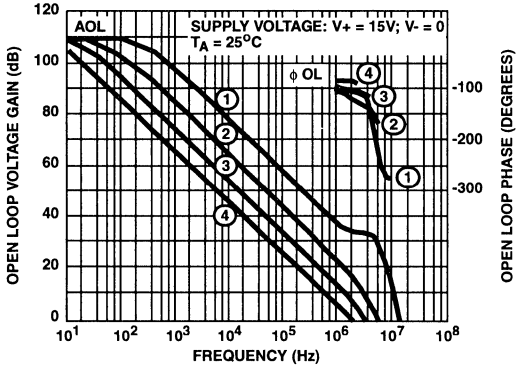


FIGURE 18. OPEN LOOP GAIN vs TEMPERATURE



1 - C_L = 9pF, C_C = 0pF, R_L = ∞
2 - C_L = 30pF, C_C = 15pF, R_L = 2kΩ
3 - C_L = 30pF, C_C = 47pF, R_L = 2kΩ
4 - C_L = 30pF, C_C = 150pF, R_L = 2kΩ

FIGURE 19. OPEN-LOOP RESPONSE

Typical Performance Curves (Continued)

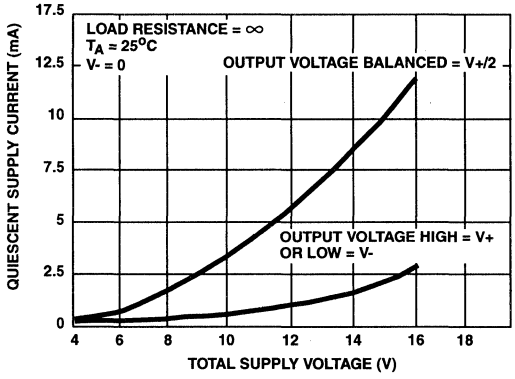


FIGURE 20. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

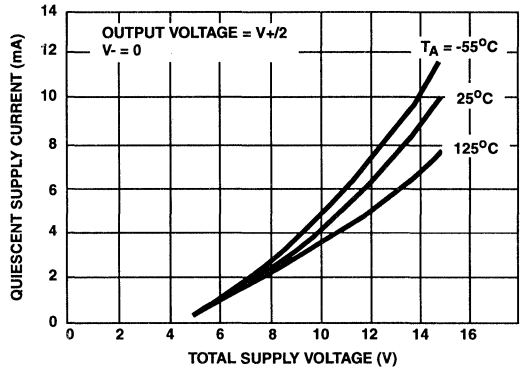


FIGURE 21. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

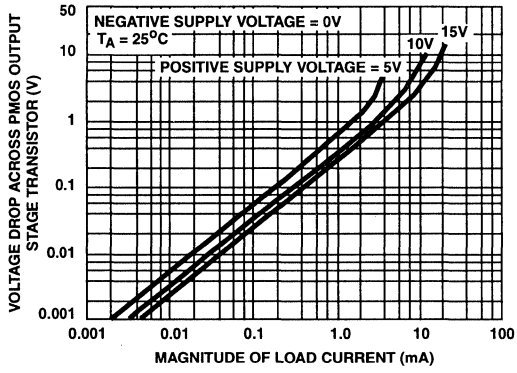


FIGURE 22. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q_8) vs LOAD CURRENT

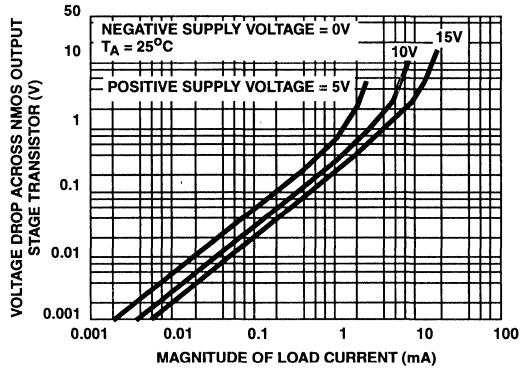


FIGURE 23. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q_{12}) vs LOAD CURRENT

CA3140, CA3140A

4.5MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar Output

November 1996

Features

- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}) -1.5TΩ (Typ)
  - Very Low Input Current (I_I) -10pA (Typ) at ±15V
  - Wide Common Mode Input Voltage Range (V_{ICR}) - Can be Swung 0.5V Below Negative Supply Voltage Rail
  - Output Swing Complements Input Common Mode Range
- Directly Replaces Industry Type 741 in Most Applications

Applications

- Ground-Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (μseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Peak Detectors
- Active Filters
- Comparators
- Interface in 5V TTL Systems and Other Low Supply Voltage Systems
- All Standard Operational Amplifier Applications
- Function Generators
- Tone Controls
- Power Supplies
- Portable Instruments
- Intrusion Alarm Systems

Description

The CA3140A and CA3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The CA3140A and CA3140 operate at supply voltage from 4V to 36V (either single or dual supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

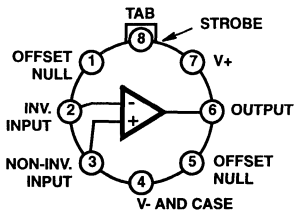
The CA3140 Series has the same 8-lead pinout used for the "741" and other industry standard op amps. The CA3140A and CA3140 are intended for operation at supply voltages up to 36V (±18V).

Ordering Information

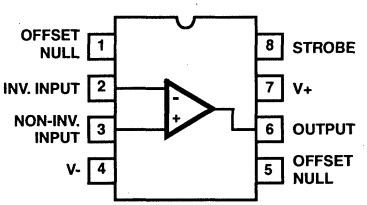
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3140AE	-55 to 125	8 Ld PDIP	E8.3
CA3140AM (3140A)	-55 to 125	8 Ld SOIC	M8.15
CA3140AS	-55 to 125	8 Pin Metal Can	T8.C
CA3140AT	-55 to 125	8 Pin Metal Can	T8.C
CA3140E	-55 to 125	8 Ld PDIP	E8.3
CA3140M (3140)	-55 to 125	8 Ld SOIC	M8.15
CA3140M96 (3140)	-55 to 125	8 Ld SOIC Tape and Reel	
CA3140T	-55 to 125	8 Pin Metal Can	T8.C

Pinouts

CA3140 (METAL CAN)
TOP VIEW



CA3140 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **957.3**

Absolute Maximum Ratings

DC Supply Voltage (Between V+ and V- Terminals) 36V
Differential Mode Input Voltage 8V
DC Input Voltage . . . . . (V+ +8V) To (V- -0.5V)
Input Terminal Current 1mA
Output Short Circuit Duration (Note 2) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	100	N/A
SOIC Package	160	N/A
Metal Can Package	170	85

Maximum Junction Temperature (Metal Can Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Short circuit may be applied to ground or to either supply.

Electrical Specifications $V_{SUPPLY} = \pm 15V$, $T_A = 25°C$

PARAMETER	SYMBOL	TEST CONDITIONS		TYPICAL VALUES CA3140	TYPICAL VALUES CA3140A	UNITS
Input Offset Voltage Adjustment Resistor		Typical Value of Resistor Between Terminals 4 and 5 or 4 and 1 to Adjust Max V_{IO}		4.7	18	kΩ
Input Resistance	R_I			1.5	1.5	TΩ
Input Capacitance	C_I			4	4	pF
Output Resistance	R_O			60	60	Ω
Equivalent Wideband Input Noise Voltage, (See Figure 27)	e_N	BW = 140kHz, R_S = 1MΩ		48	48	μV
Equivalent Input Noise Voltage (See Figure 35)	e_N	R_S = 100Ω	f = 1kHz	40	40	nV/√Hz
			f = 10kHz	12	12	nV/√Hz
Short Circuit Current to Opposite Supply	I_{OM^+}		Source	40	40	mA
	I_{OM^-}		Sink	18	18	mA
Gain-Bandwidth Product, (See Figures 6, 30)	f_T			4.5	4.5	MHz
Slew Rate, (See Figure 31)	SR			9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	220	μA
Transient Response (See Figure 28)	t_r	R_L = 2kΩ, C_L = 100pF	Rise Time	0.08	0.08	μs
	OS		Overshoot	10	10	%
Settling Time at $10V_{P-P}$, (See Figure 5)	t_S	R_L = 2kΩ, C_L = 100pF, Voltage Follower	To 1mV	4.5	4.5	μs
			To 10mV	1.4	1.4	μs

Electrical Specifications For Equipment Design, at $V_{SUPPLY} = \pm 15V$, $T_A = 25°C$, Unless Otherwise Specified

PARAMETER	SYMBOL	CA3140 MIN	CA3140 TYP	CA3140 MAX	CA3140A MIN	CA3140A TYP	CA3140A MAX	UNITS
Input Offset Voltage	$\lvert V_{IO} \rvert$	-	5	15	-	2	5	mV
Input Offset Current	$\lvert I_{IO} \rvert$	-	0.5	30	-	0.5	20	pA
Input Current	I_I	-	10	50	-	10	40	pA
Large Signal Voltage Gain (Note 3) (See Figures 6, 29)	A_{OL}	20	100	-	20	100	-	kV/V
		86	100	-	86	100	-	dB
Common Mode Rejection Ratio (See Figure 34)	CMRR	-	32	320	-	32	320	μV/V
		70	90	-	70	90	-	dB
Common Mode Input Voltage Range (See Figure 8)	V_{ICR}	-15	-15.5 to +12.5	11	-15	-15.5 to +12.5	12	V

Electrical Specifications For Equipment Design, at $V_{SUPPLY} = \pm 15V$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	CA3140			CA3140A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$ (See Figure 36)	PSRR	-	100	150	-	100	150	µV/V
		76	80	-	76	80	-	dB
Max Output Voltage (Note 4) (See Figures 2, 8)	V_{OM+}	+12	13	-	+12	13	-	V
	V_{OM-}	-14	-14.4	-	-14	-14.4	-	V
Supply Current (See Figure 32)	I+	-	4	6	-	4	6	mA
Device Dissipation	P_D	-	120	180	-	120	180	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	8	-	-	6	-	µV/°C

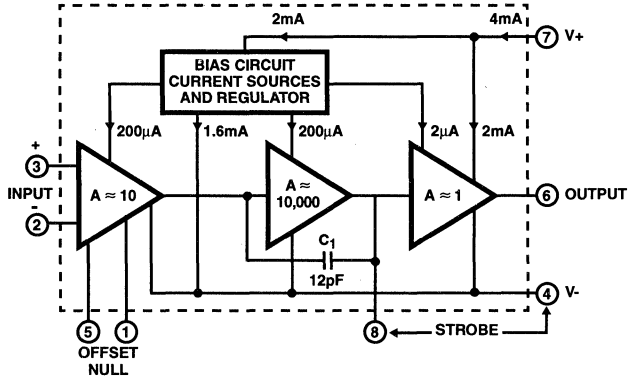
NOTES:

3. At $V_O = 26V_{P-P}$, +12V, -14V and $R_L = 2k\Omega$.
4. At $R_L = 2k\Omega$.

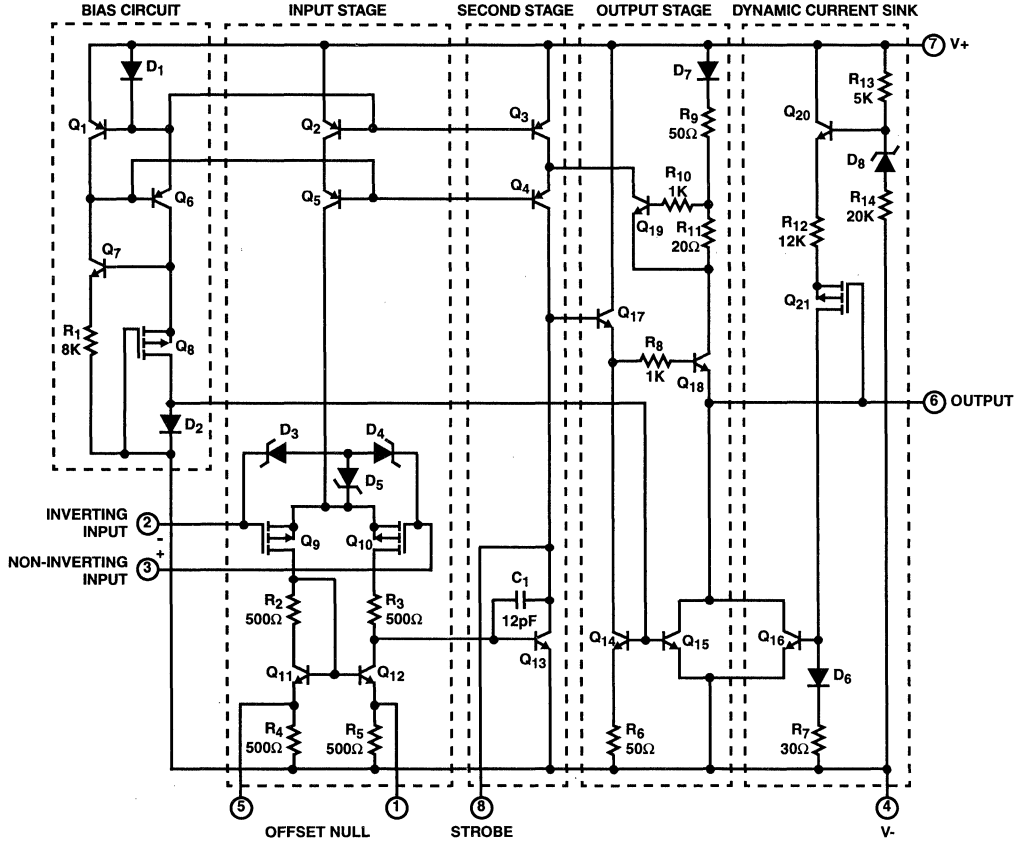
Electrical Specifications For Design Guidance At V+ = 5V, V- = 0V, $T_A = 25^oC$

PARAMETER		SYMBOL	TYPICAL VALUES		UNITS
			CA3140	CA3140A	
Input Offset Voltage		$\lvert V_{IO}\rvert$	5	2	mV
Input Offset Current		$\lvert I_{IO}\rvert$	0.1	0.1	pA
Input Current		I_I	2	2	pA
Input Resistance		R_I	1	1	TΩ
Large Signal Voltage Gain (See Figures 6, 29)		A_{OL}	100	100	kV/V
			100	100	dB
Common Mode Rejection Ratio		CMRR	32	32	µV/V
			90	90	dB
Common Mode Input Voltage Range (See Figure 8)		V_{ICR}	-0.5	-0.5	V
			2.6	2.6	V
Power Supply Rejection Ratio		PSRR $\Delta V_{IO}/\Delta V_S$	100	100	µV/V
			80	80	dB
Maximum Output Voltage (See Figures 2, 8)		V_{OM+}	3	3	V
		V_{OM-}	0.13	0.13	V
Maximum Output Current:	Source	I_{OM+}	10	10	mA
	Sink	I_{OM-}	1	1	mA
Slew Rate (See Figure 31)		SR	7	7	V/µs
Gain-Bandwidth Product (See Figure 30)		f_T	3.7	3.7	MHz
Supply Current (See Figure 32)		I+	1.6	1.6	mA
Device Dissipation		P_D	8	8	mW
Sink Current from Terminal 8 to Terminal 4 to Swing Output Low			200	200	µA

Block Diagram



Schematic Diagram



NOTE: All resistance values are in ohms.

Application Information

Circuit Description

As shown in the block diagram, the input terminals may be operated down to 0.5V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant current flow circuits in the first and second stages. The CA3140 includes an on chip phase compensating capacitor that is sufficient for the unity gain voltage follower configuration.

Input Stage

The schematic diagram consists of a differential input stage using PMOS field-effect transistors (Q_9, Q_{10}) working into a mirror pair of bipolar transistors (Q_{11}, Q_{12}) functioning as load resistors together with resistors R_2 through R_5. The mirror pair transistors also function as a differential-to-single-ended converter to provide base current drive to the second stage bipolar transistor (Q_{13}). Offset nulling, when desired, can be effected with a 10kΩ potentiometer connected across Terminals 1 and 5 and with its slider arm connected to Terminal 4. Cascode-connected bipolar transistors Q_2, Q_5 are the constant current source for the input stage. The base biasing circuit for the constant current source is described subsequently. The small diodes D_3, D_4, D_5 provide gate oxide protection against high voltage transients, e.g., static electricity.

Second Stage

Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q_{13} and its cascode connected load resistance provided by bipolar transistors Q_3, Q_4. On-chip phase compensation, sufficient for a majority of the applications is provided by C_1. Additional Miller-Effect compensation (roll off) can be accomplished, when desired, by simply connecting a small capacitor between Terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output Terminal 6 swings low, i.e., approximately to Terminal 4 potential.

Output Stage

The CA3140 Series circuits employ a broad band output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q_{17}, Q_{18}) is established by transistors (Q_{14}, Q_{15}) whose base currents are "mirrored" to current flowing through diode D_2 in the bias circuit section. When the CA3140 is operating such that output Terminal 6 is sourcing current, transistor Q_{18} functions as an emitter-follower to source current from the V+ bus (Terminal 7), via D_7, R_9, and R_{11}. Under these conditions, the collector potential of Q_{13} is sufficiently high to permit the necessary flow of base current to emitter follower Q_{17} which, in turn, drives Q_{18}.

When the CA3140 is operating such that output Terminal 6 is sinking current to the V- bus, transistor Q_{16} is the current sinking element. Transistor Q_{16} is mirror connected to D_6, R_7, with current fed by way of Q_{21}, R_{12}, and Q_{20}. Transistor Q_{20}, in turn, is biased by current flow through R_{13}, zener D_8, and R_{14}. The dynamic current sink is controlled by voltage level sensing. For purposes of explanation, it is assumed that output Terminal 6 is quiescently established at the potential midpoint between the V+ and V- supply rails. When output current sinking mode operation is required, the collector potential of transistor Q_{13} is driven below its quiescent level, thereby causing Q_{17}, Q_{18} to decrease the output voltage at Terminal 6. Thus, the gate terminal of PMOS transistor Q_{21} is displaced toward the V- bus, thereby reducing the channel resistance of Q_{21}. As a consequence, there is an incremental increase in current flow through Q_{20}, R_{12}, Q_{21}, D_6, R_7, and the base of Q_{16}. As a result, Q_{16} sinks current from Terminal 6 in direct response to the incremental change in output voltage caused by Q_{18}. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q_{18}. Short circuit protection of the output circuit is provided by Q_{19}, which is driven into conduction by the high voltage drop developed across R_{11} under output short circuit conditions. Under these conditions, the collector of Q_{19} diverts current from Q_4 so as to reduce the base current drive from Q_{17}, thereby limiting current flow in Q_{18} to the short circuited load terminal.

Bias Circuit

Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R_1. The function of the bias circuit is to establish and maintain constant current flow through D_1, Q_6, Q_8 and D_2. D_1 is a diode connected transistor mirror connected in parallel with the base emitter junctions of Q_1, Q_2, and Q_3. D_1 may be considered as a current sampling diode that senses the emitter current of Q_6 and automatically adjusts the base current of Q_6 (via Q_1) to maintain a constant current through Q_6, Q_8, D_2. The base currents in Q_2, Q_3 are also determined by constant current flow D_1. Furthermore, current in diode connected transistor Q_2 establishes the currents in transistors Q_{14} and Q_{15}.

Typical Applications

Wide dynamic range of input and output characteristics with the most desirable high input impedance characteristics is achieved in the CA3140 by the use of an unique design based upon the PMOS Bipolar process. Input common mode voltage range and output swing capabilities are complementary, allowing operation with the single supply down to 4V.

The wide dynamic range of these parameters also means that this device is suitable for many single supply applications, such as, for example, where one input is driven below the potential of Terminal 4 and the phase sense of the output signal must be maintained – a most important consideration in comparator applications.

Output Circuit Considerations

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2V zener diode connected to Terminal 8 as shown in Figure 1. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

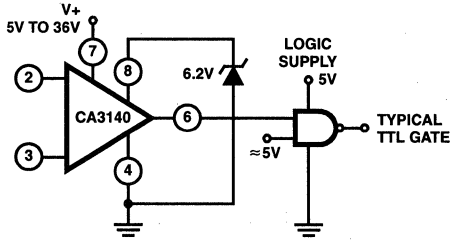


FIGURE 1. ZENER CLAMPING DIODE CONNECTED TO TERMINALS 8 AND 4 TO LIMIT CA3140 OUTPUT SWING TO TTL LEVELS

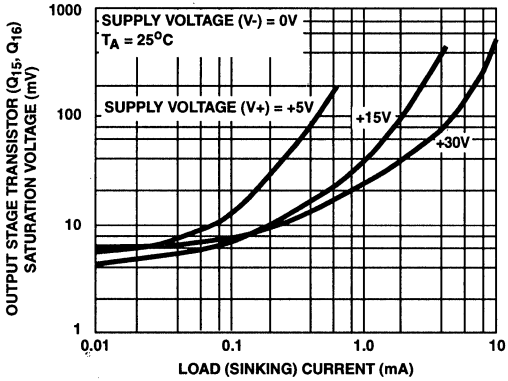


FIGURE 2. VOLTAGE ACROSS OUTPUT TRANSISTORS (Q_{15} AND Q_{16}) vs LOAD CURRENT

Figure 2 shows output current sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 4 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

Offset Voltage Nulling

The input offset voltage can be nulled by connecting a 10kΩ potentiometer between Terminals 1 and 5 and returning its wiper arm to terminal 4, see Figure 3A. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors (R) that may be placed at either end of the potentiometer, see Figure 3B, to optimize its utilization range are given in the Electrical Specifications table.

An alternate system is shown in Figure 3C. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to 0Ω at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

Low Voltage Operation

Operation at total supply voltages as low as 4V is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low voltage limitation occurs when the upper extreme of the input common mode voltage range extends down to the voltage at Terminal 4. This limit is reached at a total supply voltage just below 4V. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Figure 8 shows these characteristics and shows that with 2V dual supplies, the lower extreme of the input common mode voltage range is below ground potential.

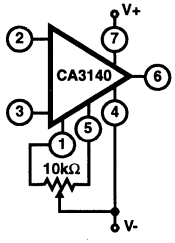


FIGURE 3A. BASIC

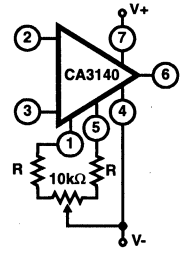


FIGURE 3B. IMPROVED RESOLUTION

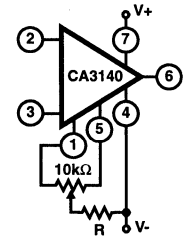


FIGURE 3C. SIMPLER IMPROVED RESOLUTION

FIGURE 3. THREE OFFSET VOLTAGE NULLING METHODS

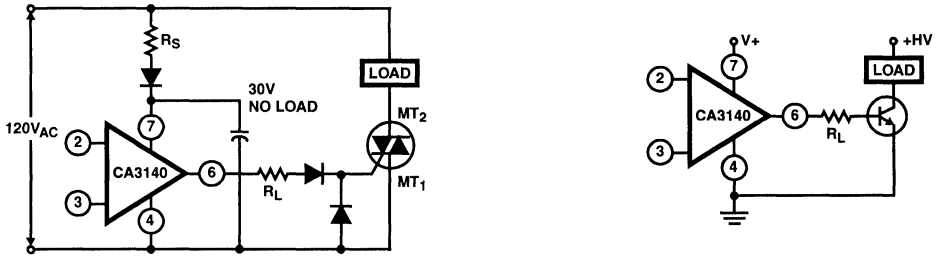


FIGURE 4. METHODS OF UTILIZING THE $V_{CE(SAT)}$ SINKING CURRENT CAPABILITY OF THE CA3140 SERIES

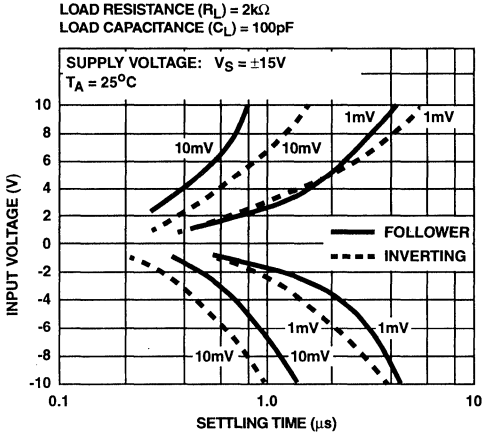


FIGURE 5A. WAVEFORM

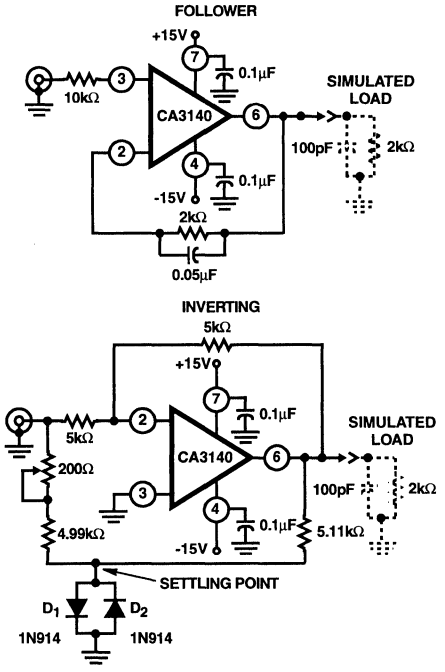


FIGURE 5B. TEST CIRCUITS

FIGURE 5. SETTLING TIME vs INPUT VOLTAGE

Bandwidth and Slew Rate

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between Terminals 1 and 8 can reduce the open loop -3dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Figure 5 shows the typical settling time required to reach 1mV or 10mV of the final value for various levels of large signal inputs for the voltage follower and inverting unity gain amplifiers. The exceptionally fast settling time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Figure 6.

Input Circuit Considerations

As mentioned previously, the amplifier inputs can be driven below the Terminal 4 potential, but a series current limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity gain voltage follower. This resistance prevents the possibility of extremely large input signal transients from forcing a signal through the input protection network and directly driving the internal constant current source which could result in positive feedback via the output terminal. A 3.9kΩ resistor is sufficient.

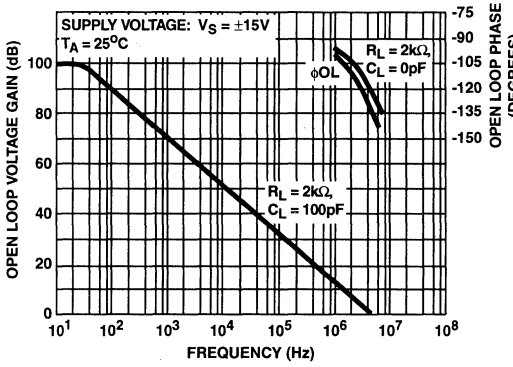


FIGURE 6. OPEN LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY

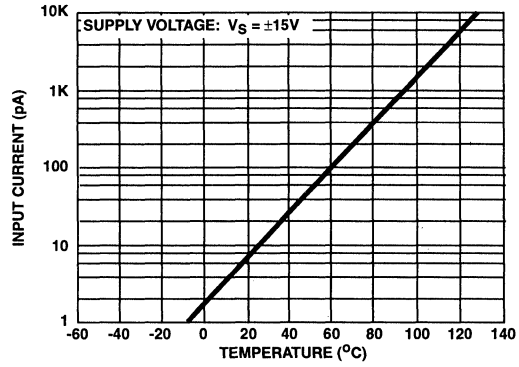


FIGURE 7. INPUT CURRENT vs TEMPERATURE

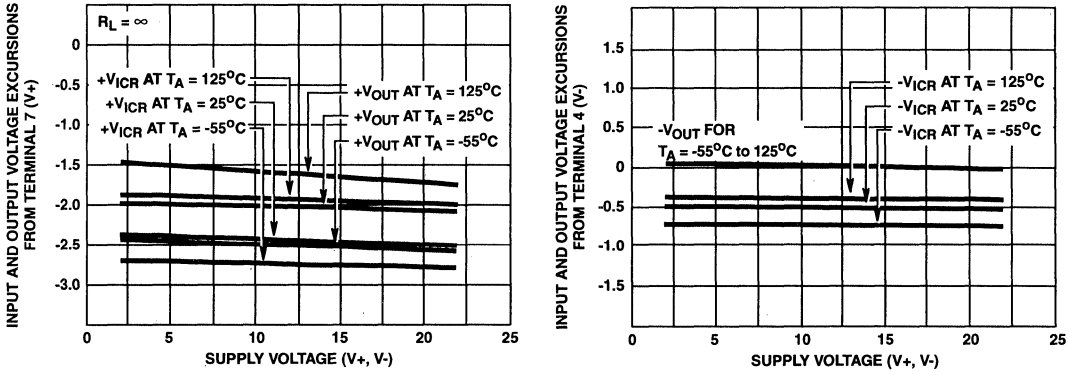


FIGURE 8. OUTPUT VOLTAGE SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

The typical input current is on the order of 10pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Figure 7 shows typical input terminal current versus ambient temperature for the CA3140.

It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Figure 9 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for metal can); at lower temperatures (metal can and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

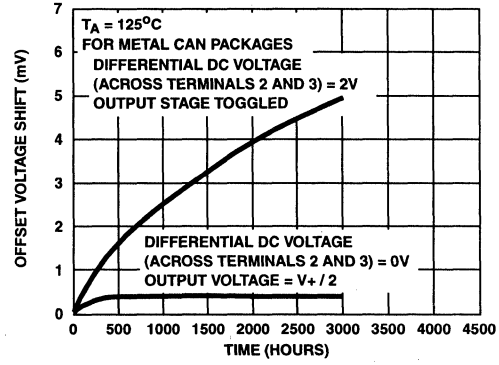


FIGURE 9. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

Super Sweep Function Generator

A function generator having a wide tuning range is shown in Figure 10. The 1,000,000/1 adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting readout amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

Buffered triangular output signals are then applied to a second CA3080 functioning as a high speed hysteresis switch. Output from the switch is returned directly back to the input of the CA3080A current source, thereby, completing the positive feedback loop

The triangular output level is determined by the four 1N914 level limiting diodes of the second CA3080 and the resistor divider network connected to Terminal No. 2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High frequency ramp linearity is adjusted by the single 7pF to 60pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA3080A is characterized for maximum output linearity in the current generator function.

Meter Driver and Buffer Amplifier

Figure 11 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generator's frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60mV change in the applied voltage, V_{ABC} (voltage between Terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necessary. Two adjustments are used for the meter. The meter sensitivity control sets the meter scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects $^1/_6$ of full scale for each decade change in frequency.

Sine Wave Shaper

The circuit shown in Figure 12 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero crossing slope is established by the 10kΩ potentiometer connected between Terminals 2 and 6 of the CA3140 and the 9.1kΩ resistor and 10kΩ potentiometer from Terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

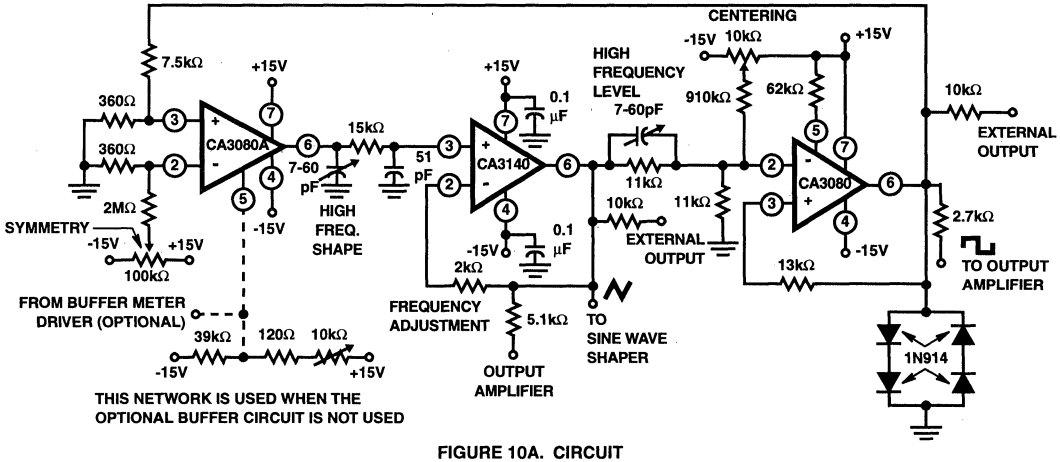
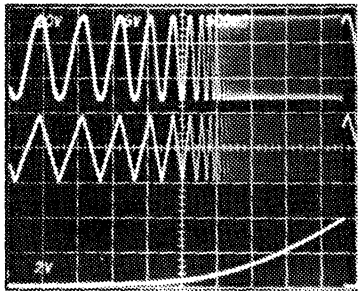


FIGURE 10A. CIRCUIT

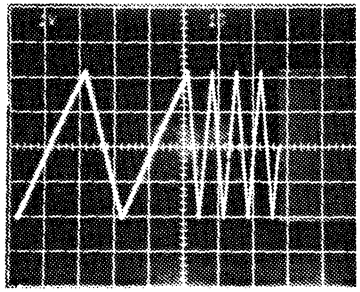


Top Trace: Output at junction of 2.7Ω and 51Ω resistors; 5V/Div., 500ms/Div.

Center Trace: External output of triangular function generator; 2V/Div., 500ms/Div.

Bottom Trace: Output of "Log" generator; 10V/Div., 500ms/Div.

FIGURE 10B. FIGURE FUNCTION GENERATOR SWEEPING



1V/Div., 1s/Div.

Three tone test signals, highest frequency ≥0.5MHz. Note the slight asymmetry at the three second/cycle signal. This asymmetry is due to slightly different positive and negative integration from the CA3080A and from the PC board and component leakages at the 100pA level.

FIGURE 10C. FUNCTION GENERATOR WITH FIXED FREQUENCIES

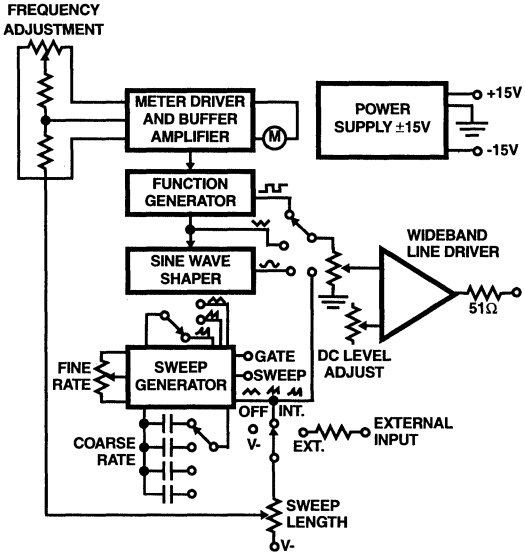


FIGURE 10D. INTERCONNECTIONS

FIGURE 10. FUNCTION GENERATOR

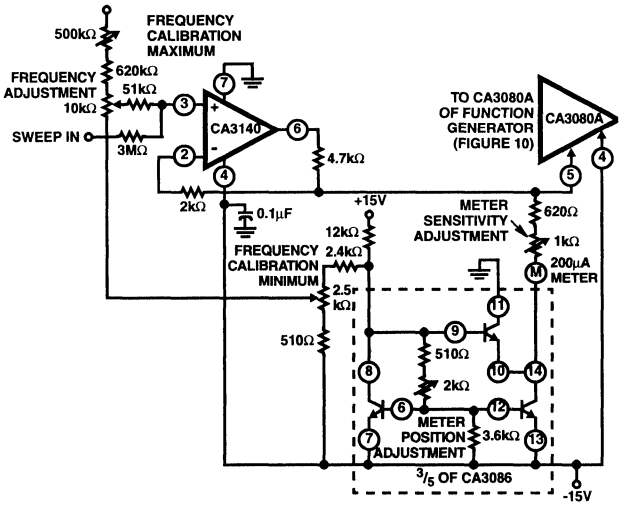


FIGURE 11. METER DRIVER AND BUFFER AMPLIFIER

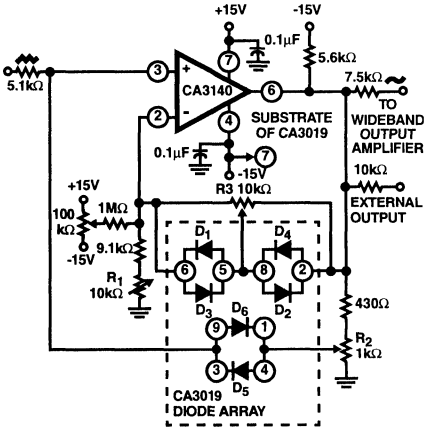


FIGURE 12. SINE WAVE SHAPER

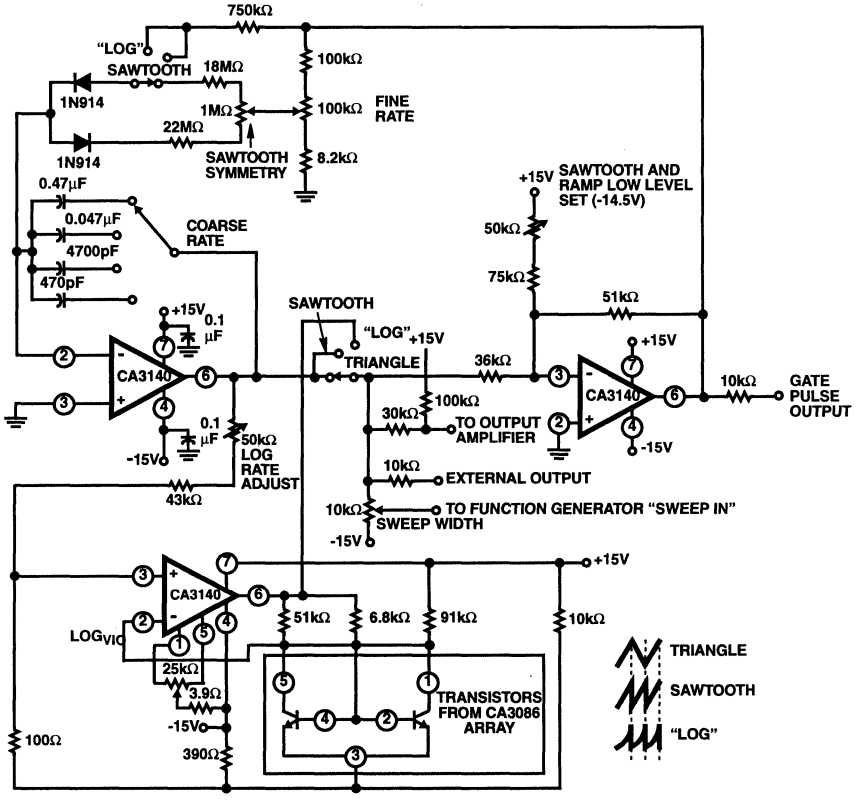


FIGURE 13. SWEEPING GENERATOR

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary.

Sweeping Generator

Figure 13 shows a sweeping generator. Three CA3140s are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

Wideband Output Amplifier

Figure 14 shows a high slew rate, wideband amplifier suitable for use as a 50Ω transmission line driver. This circuit, when used in conjunction with the function generator and sine wave shaper circuits shown in Figures 10 and 12 provides $18V_{P-P}$ output open circuited, or $9V_{P-P}$ output when terminated in 50Ω. The slew rate required of this amplifier is 28V/μs ($18V_{P-P} \times \pi \times 0.5MHz$).

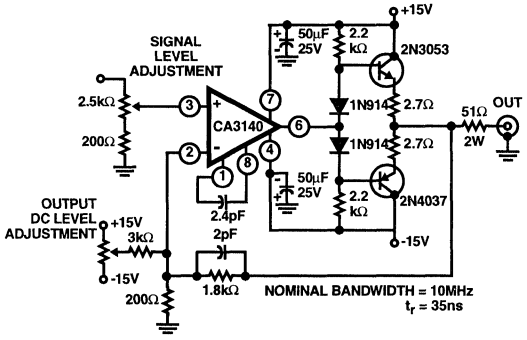


FIGURE 14. WIDEBAND OUTPUT AMPLIFIER

Power Supplies

High input impedance, common mode capability down to the negative supply and high output drive current capability are key factors in the design of wide range output voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0V to 24V.

Unlike many regulator systems using comparators having a bipolar transistor input stage, a high impedance reference voltage divider from a single supply can be used in connection with the CA3140 (see Figure 15).

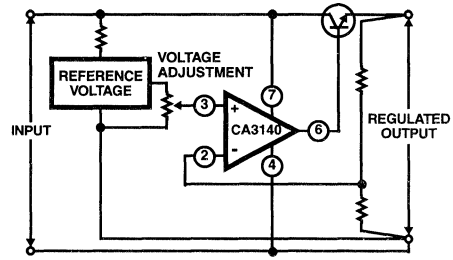


FIGURE 15. BASIC SINGLE SUPPLY VOLTAGE REGULATOR SHOWING VOLTAGE FOLLOWER CONFIGURATION

Essentially, the regulators, shown in Figures 16 and 17, are connected as non inverting power operational amplifiers with a gain of 3.2. An 8V reference input yields a maximum output voltage slightly greater than 25V. As a voltage follower, when the reference input goes to 0V the output will be 0V. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CESAT}) across the output of the CA3140 (see Figure 2). This saturation voltage level may indeed set the lowest voltage obtainable.

The high impedance presented by Terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply rail.

Figures 16 and 17, show circuits in which a D2201 high speed diode is used for the current sensor. This diode was chosen for its slightly higher forward voltage drop characteristic, thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1A at 1V forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small signal reference amplifier in the proximity of the current sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10mA to 1A with a single adjustment potentiometer. If the temperature stability of the current limiting system is a serious consideration, the more usual current sampling resistor type of circuitry should be employed.

A power Darlington transistor (in a metal can with heatsink), is used as the series pass element for the conventional current limiting system, Figure 16, because high power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat sink VERSAWATT transistor is used as the series pass element in the fold back current system, Figure 17, since dissipation levels will only approach 10W. In this system, the D2201 diode is used for current sampling. Fold-

back is provided by the 3kΩ and 100kΩ divider network connected to the base of the current sensing transistor.

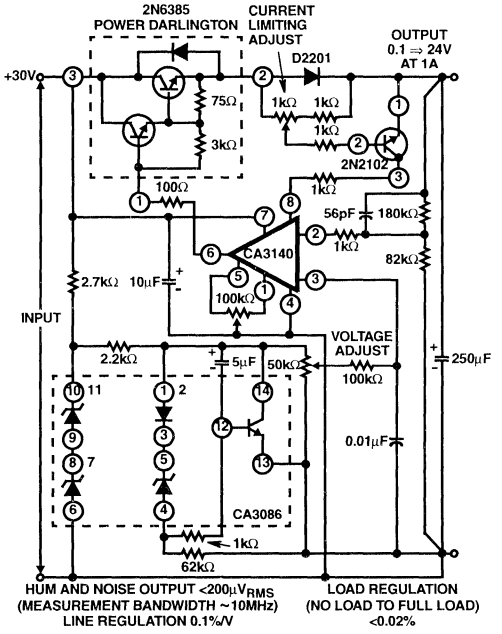


FIGURE 16. REGULATED POWER SUPPLY

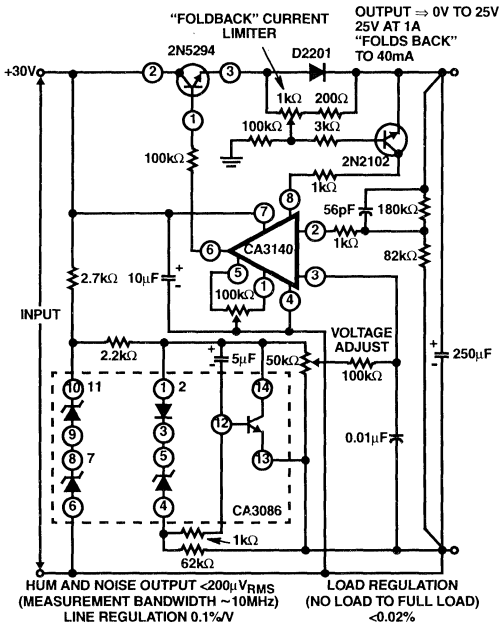
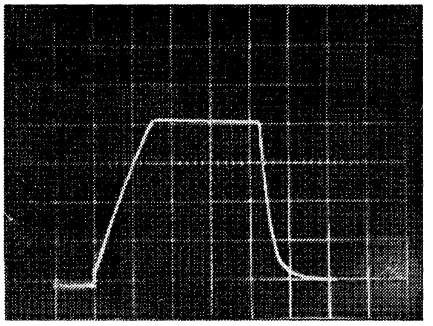


FIGURE 17. REGULATED POWER SUPPLY WITH "FOLDBACK" CURRENT LIMITING

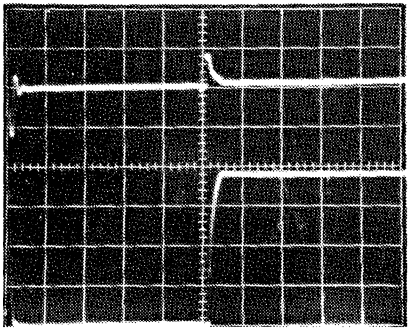
Both regulators provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200μV as read with a meter having a 10MHz bandwidth.

Figure 18A shows the turn ON and turn OFF characteristics of both regulators. The slow turn on rise is due to the slow rate of rise of the reference voltage. Figure 18B shows the transient response of the regulator with the switching of a 20Ω load at 20V output.



5V/Div., 1s/Div.

FIGURE 18A. SUPPLY TURN-ON AND TURNOFF CHARACTERISTICS



Top Trace: Output Voltage;
200mV/Div., 5μs/Div.

Bottom Trace: Collector of load switching transistor, load = 1A;
5V/Div., 5μs/Div.

FIGURE 18B. TRANSIENT RESPONSE

FIGURE 18. WAVEFORMS OF DYNAMIC CHARACTERISTICS OF POWER SUPPLY CURRENTS SHOWN IN FIGURES 16 AND 17

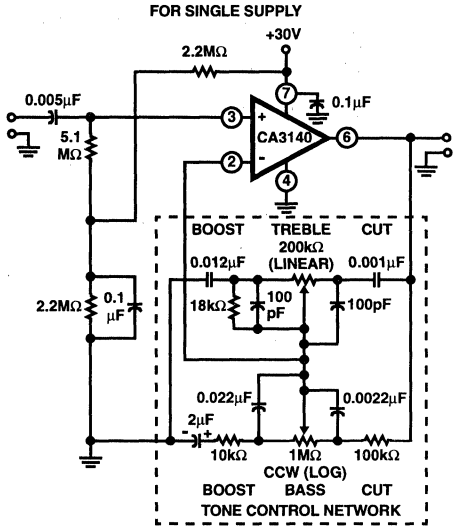
Tone Control Circuits

High slew rate, wide bandwidth, high output voltage capability and high input impedance are all characteristics required of tone control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figures 19 and 20.

The first circuit, shown in Figure 20, is the Baxandall tone control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ±15dB at 100Hz and 10kHz, respectively. Full peak-to-peak output is available up to at least 20kHz due to the high slew rate of the CA3140. The amplifier gain is 3dB down from its "flat" position at 70kHz.

Figure 19 shows another tone control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from Terminal No. 3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No. 3, August, 1972.



NOTES:

5. 20dB Flat Position Gain.
6. ±15dB Bass and Treble Boost and Cut at 100Hz and 10kHz, respectively.
7. $25V_{P-P}$ output at 20kHz.
8. -3dB at 24kHz from 1kHz reference.

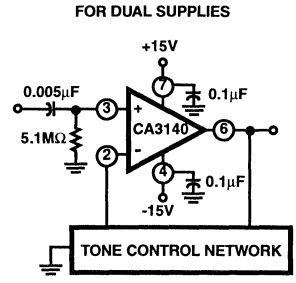
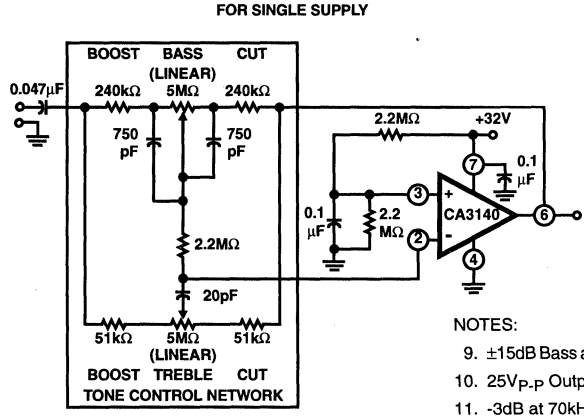
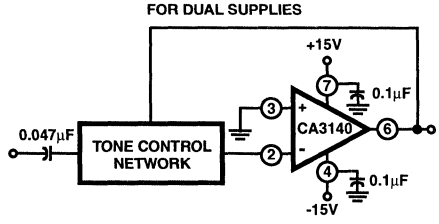


FIGURE 19. TONE CONTROL CIRCUIT USING CA3130 SERIES (20dB MIDBAND GAIN)





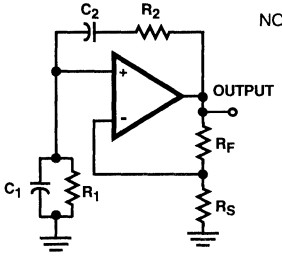
NOTES:

9. ±15dB Bass and Treble Boost and Cut at 100Hz and 10kHz, Respectively.
10. $25V_{P-P}$ Output at 20kHz.
11. -3dB at 70kHz from 1kHz Reference.
12. 0dB Flat Position Gain.

FIGURE 20. BAXANDALL TONE CONTROL CIRCUIT USING CA3140 SERIES

Wien Bridge Oscillator

Another application of the CA3140 that makes excellent use of its high input impedance, high slew rate, and high voltage qualities is the Wien Bridge sine wave oscillator. A basic Wien Bridge oscillator is shown in Figure 21. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/(2\pi RC)$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain bandwidth product of the CA3140.



NOTES:

$$f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

$$A_{OSC} = 1 + \frac{C_1}{C_2} + \frac{R_2}{R_1}$$

$$A_{CL} = 1 + \frac{R_F}{R_S}$$

FIGURE 21. BASIC WIEN BRIDGE OSCILLATOR CIRCUIT USING AN OPERATIONAL AMPLIFIER

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance increases as the output amplitude is increased are a few of the elements often utilized.

Figure 22 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_F of Figure 21). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1µF polycarbonate capacitors and 22MΩ for the frequency determining network, the operating frequency is 0.007Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180kHz will reach a slew rate of approximately 9V/µs when its amplitude is $16V_{P-P}$.

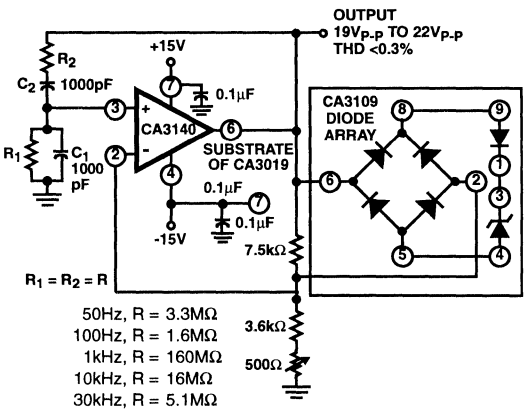


FIGURE 22. WIEN BRIDGE OSCILLATOR CIRCUIT USING CA3140

Simple Sample-and-Hold System

Figure 23 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch (see Note 13). System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2kΩ and 30pF is shown in the schematic.

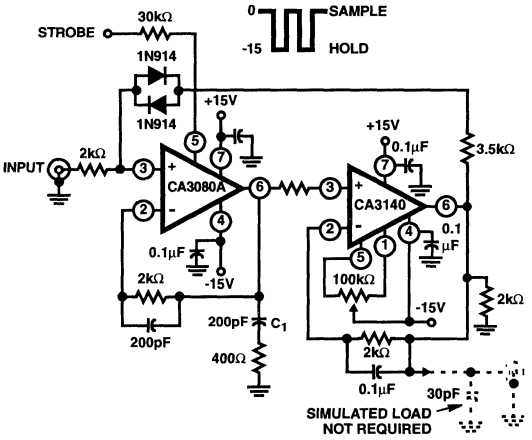


FIGURE 23. SAMPLE AND HOLD CIRCUIT

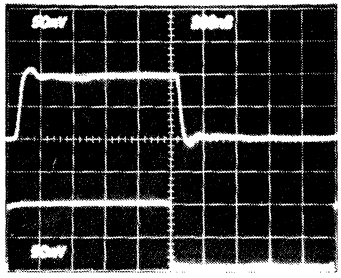
In this circuit, the storage compensation capacitance (C_1) is only 200pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate is:

$$\frac{dv}{dt} = \frac{I}{C} = 0.5mA/200pF = 2.5V/\mu s$$

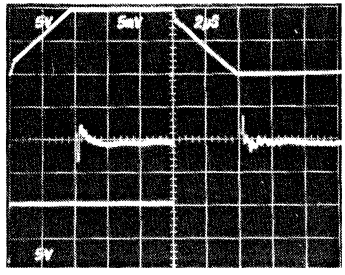
NOTE:

13. AN6668 "Applications of the CA3080 and CA 3080A High Performance Operational Transconductance Amplifiers".

Pulse "droop" during the hold interval is 170pA/200pF which is 0.85μV/μs; (i.e., 170pA/200pF). In this case, 170pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000pF, the "hold-droop" rate will decrease to 0.085μV/μs, but the slew rate would decrease to 0.25V/μs. The parallel diode network connected between Terminal 3 of the CA3080A and Terminal 6 of the CA3140 prevents large input signal feedthrough across the input terminals of the CA3080A to the 200pF storage capacitor when the CA3080A is strobed off. Figure 24 shows dynamic characteristic waveforms of this sample-and-hold system.

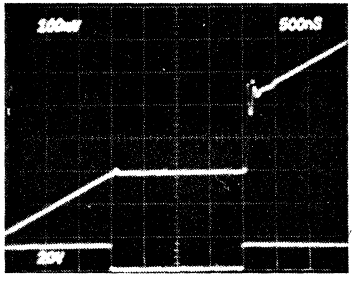


Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.



Top Trace: Output Signal; 5V/Div, 2μs/Div.
Center Trace: Difference of Input and Output Signals through Tektronix Amplifier 7A13; 5mV/Div., 2μs/Div.
Bottom Trace: Input Signal; 5V/Div., 2μs/Div.

LARGE SIGNAL RESPONSE AND SETTLING TIME



SAMPLING RESPONSE

Top Trace: Output; 100mV/Div., 500ns/Div.
Bottom Trace: Input; 20V/Div., 500ns/Div.

FIGURE 24. SAMPLE AND HOLD SYSTEM DYNAMIC CHARACTERISTICS WAVEFORMS

Current Amplifier

The low input terminal current needed to drive the CA3140 makes it ideal for use in current amplifier applications such as the one shown in Figure 25 (see Note 14). In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R_2/R_1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100nA, with values shown, the load current presented to the supply will be 100μA; a much easier current to measure in many systems.

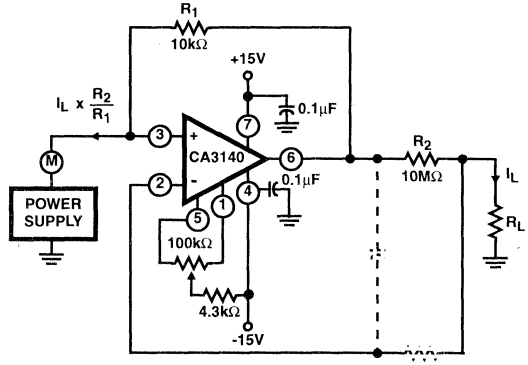


FIGURE 25. BASIC CURRENT AMPLIFIER FOR LOW CURRENT MEASUREMENT SYSTEMS

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

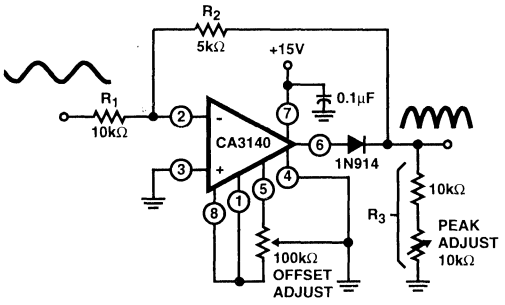
The dotted components show a method of decoupling the circuit from the effects of high output load capacitance and the potential oscillation in this situation. Essentially, the necessary high frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

Full Wave Rectifier

Figure 26 shows a single supply, absolute value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to $-R_2/R_1$. When the equality of the two equations shown in Figure 26 is satisfied, the full wave output is symmetrical.

NOTE:

14. "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308, "Negative Immittance Converter Circuits".



$$GAIN = \frac{R_2}{R_1} = X = \frac{R_3}{R_1R_2 + R_3}$$

$$R_3 = \left(\frac{X + X^2}{1 - X}\right)R_1$$

$$\text{FOR } X = 0.5 \quad \frac{5k\Omega}{10k\Omega} = \frac{R_2}{R_1}$$

$$R_3 = 10k\Omega\left(\frac{0.75}{0.5}\right) = 15k\Omega$$

$20V_{P-P}$ Input BW (-3dB) = 290kHz, DC Output (Avg) = 3.2V

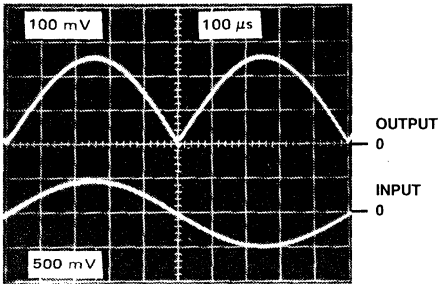


FIGURE 26. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS

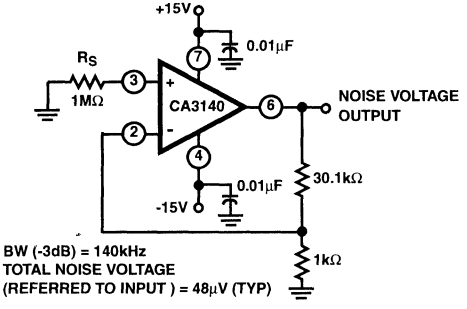


FIGURE 27. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT

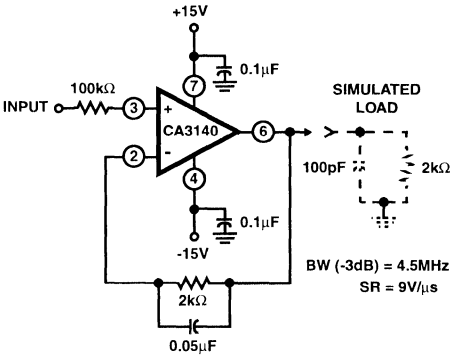
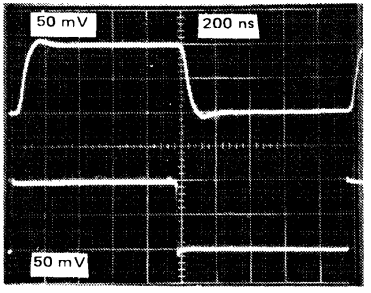
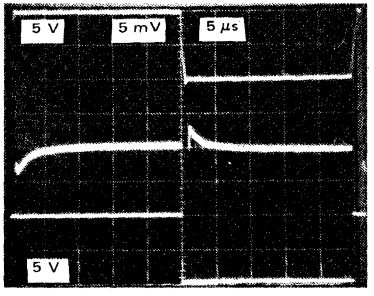


FIGURE 28A. TEST CIRCUIT



Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.

FIGURE 28B. SMALL SIGNAL RESPONSE



(Measurement made with Tektronix 7A13 differential amplifier.)

Top Trace: Output Signal; 5V/Div., 5μs/Div.
Center Trace: Difference Signal; 5mV/Div., 5μs/Div.
Bottom Trace: Input Signal; 5V/Div., 5μs/Div.

FIGURE 28C. INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME

FIGURE 28. SPLIT SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS

Typical Performance Curves

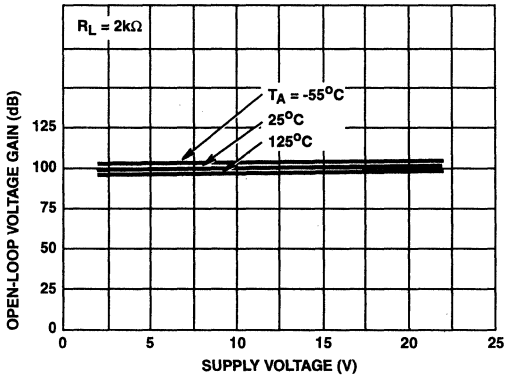


FIGURE 29. OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE AND TEMPERATURE

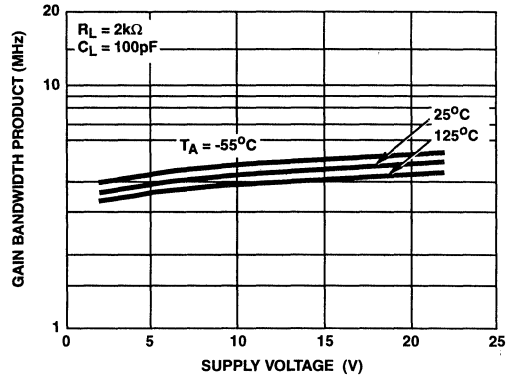


FIGURE 30. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE AND TEMPERATURE

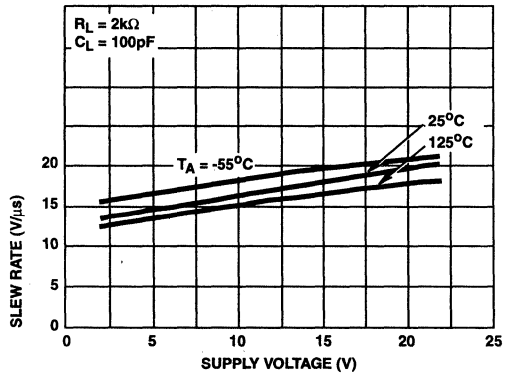


FIGURE 31. SLEW RATE vs SUPPLY VOLTAGE AND TEMPERATURE

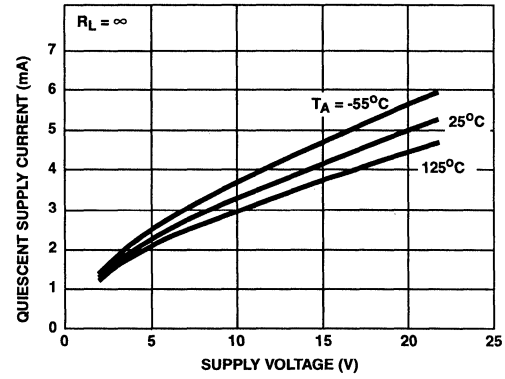


FIGURE 32. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE AND TEMPERATURE

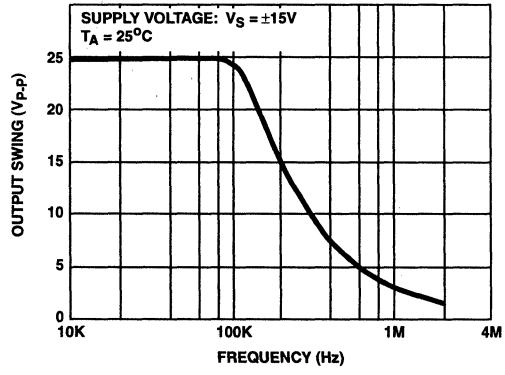


FIGURE 33. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

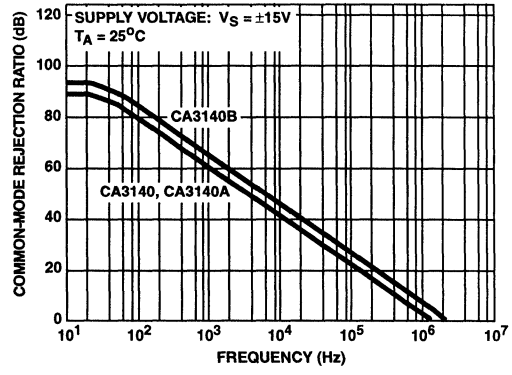


FIGURE 34. COMMON MODE REJECTION RATIO vs FREQUENCY

Typical Performance Curves (Continued)

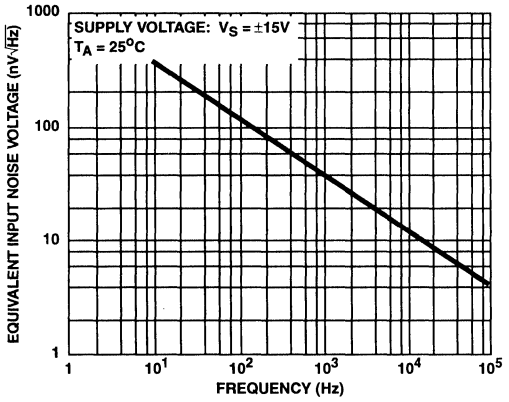


FIGURE 35. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

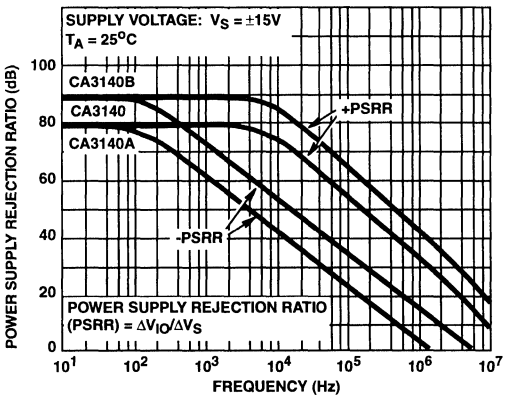
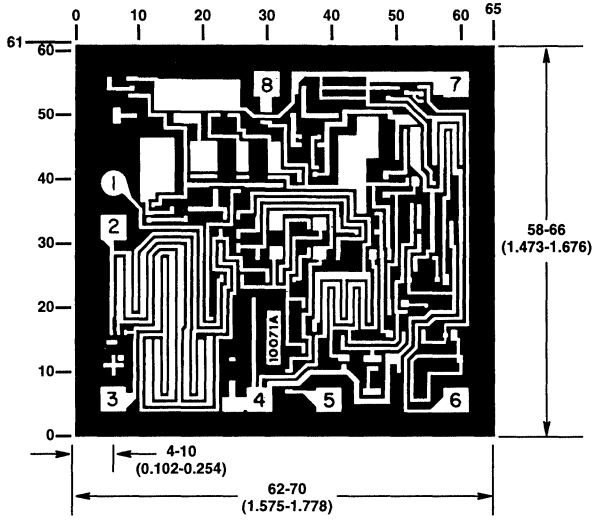


FIGURE 36. POWER SUPPLY REJECTION RATIO vs FREQUENCY

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^o instead of 90^o with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

HARRIS SEMICONDUCTOR

CA3160, CA3160A

4MHz, BiMOS Operational Amplifier with MOSFET Input/CMOS Output

November 1996

Features

- MOSFET Input Stage Provides:
  - Very High Z_I = 1.5TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I = 5pA (Typ) at 15V Operation
    = 2pA (Typ) at 5V Operation
- Common-Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can Be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample Hold Amplifiers
- Long Duration Timers/Monostables
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g., Follower for Single Supply D/A Converter)
- Wien-Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3160AE	-55 to 125	8 Ld PDIP	E8.3
CA3160AT	-55 to 125	8 Pin Metal Can	T8.C
CA3160E	-55 to 125	8 Ld PDIP	E8.3
CA3160T	-55 to 125	8 Pin Metal Can	T8.C

Description

The CA3160A and CA3160 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA3160 series are frequency compensated versions of the popular CA3130 series.

Gate protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common-mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

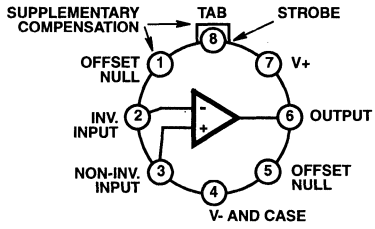
A complementary symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3160 Series circuits operate at supply voltages ranging from 5V to 16V, or ±2.5V to ±8V when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset null capability. Terminal provisions are also made to permit strobing of the output stage.

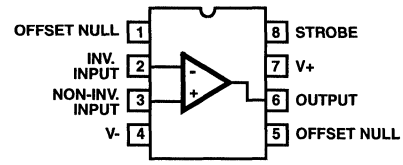
The CA3160A offers superior input characteristics over those of the CA3160.

Pinouts

CA3160
(METAL CAN)
TOP VIEW



CA3160
(PDIP)
TOP VIEW



NOTE: CA3160 Series devices have an on-chip frequency compensation network. Supplementary phase compensation or frequency roll-off (if desired) can be connected externally between Terminals 1 and 8.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **976.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) . . . . . +16V
Differential Mode Input Voltage 8V
Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 2) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . $-55^{o}C$ to $125^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
PDIP Package	110	N/A
Metal Can Package	170	85

Maximum Junction Temperature (Metal Can) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Short Circuit may be applied to ground or to either supply.

Electrical Specifications $T_A = 25^{o}C$, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3160			CA3160A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$	$V_S = \pm 7.5V$	-	6	15	-	2	5	mV
Input Offset Current	$\|I_{IO}\|$	$V_S = \pm 7.5V$	-	0.5	30	-	0.5	20	pA
Input Current	I_I	$V_S = \pm 7.5V$	-	5	50	-	5	30	pA
Large-Signal Voltage Gain	A_{OL}	$V_O = 10V_{P-P}$, $R_L = 2k\Omega$	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common-Mode Rejection Ratio	CMRR		70	90	-	80	95	-	dB
Common-Mode Input-Voltage Range	V_{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power-Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V_S$, $V_S = \pm 7.5V$	-	32	320	-	32	150	µV/V
Maximum Output Voltage	V_{OM+}	$R_L = 2k\Omega$	12	13.3	-	12	13.3	-	V
	V_{OM-}		-	0.002	0.01	-	0.002	0.01	V
	V_{OM+}	$R_L = \infty$	14.99	15	-	14.99	15	-	V
	V_{OM-}		-	0	0.01	-	0	0.01	V
Maximum Output Current	I_{OM+}	V_O = 0V (Source)	12	22	45	12	22	45	mA
	I_{OM-}	V_O = 15V (Sink)	12	20	45	12	20	45	mA
Supply Current (Note 3)	I+	$V_O = 7.5V$, $R_L = \infty$	-	10	15	-	10	15	mA
		V_O = 0V, $R_L = \infty$	-	2	3	-	2	3	mA
Input Offset Voltage Temperature Drift		$\Delta V_{IO}/\Delta T$	-	8	-	-	6	-	µV/°C

Electrical Specifications For Design Guidance, $V_{SUPPLY} = \pm 7.5V$, $T_A = 25^{o}C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		CA3160	CA3160A	UNITS
				TYP	TYP	
Input Offset Voltage Adjustment Range		10kΩ Across Terminals 4 and 5 or Terminals 4 and 1		±22	±22	mV
Input Resistance	R_I			1.5	1.5	TΩ
Input Capacitance	C_I	f = 1MHz		4.3	4.3	pF
Equivalent Input Noise Voltage	e_N	BW = 0.2MHz	$R_S = 1M\Omega$	40	40	µV
			$R_S = 10M\Omega$	50	50	µV
Equivalent Input Noise Voltage	e_N	$R_S = 100\Omega$	1kHz	72	72	$nV\sqrt{Hz}$
			10kHz	30	30	$nV\sqrt{Hz}$
Unity Gain Crossover Frequency	f_T			4	4	MHz
Slew Rate	SR			10	10	V/µs

Electrical Specifications For Design Guidance, V_{SUPPLY} = ±7.5V, T_A = 25°C, Unless Otherwise Specified **(Continued)**

PARAMETER		SYMBOL	TEST CONDITIONS	CA3160 TYP	CA3160A TYP	UNITS
Transient Response	Rise and Fall Time	t_r	C_L = 25pF, R_L = 2kΩ, (Voltage Follower)	0.09	0.09	µs
	Overshoot	OS		10	10	%
Settling Time		t_S	C_L = 25pF, R_L = 2kΩ, (Voltage Follower) To <0.1%, V_{IN} = $4V_{P-P}$	1.8	1.8	µs

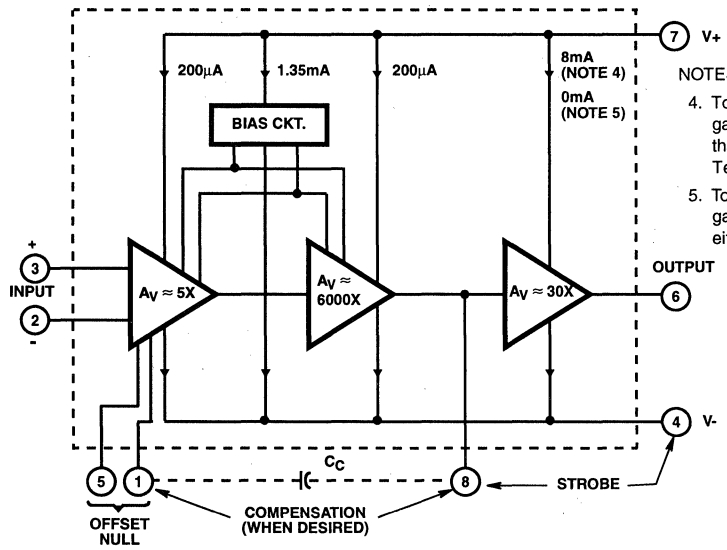
Electrical Specifications For Design Guidance, V+ = +5V, V- = 0V, T_A = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3160 TYP	CA3160A TYP	UNITS
Input Offset Voltage	V_{IO}		6	2	mV
Input Offset Current	I_{IO}		0.1	0.1	pA
Input Current	I_I		2	2	pA
Common-Mode Rejection Ratio	CMRR		80	90	dB
Large Signal Voltage Gain	A_{OL}	V_O = $4V_{P-P}$, R_L = 5kΩ	100	100	kV/V
			100	100	dB
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current	I+	V_O = 5V, R_L = ∞	300	300	µA
		V_O = 2.5V, R_L = ∞	500	500	µA
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V+$	200	200	µV/V

NOTE:

3. I_{CC} typically increases by 1.5mA/MHz during operation.

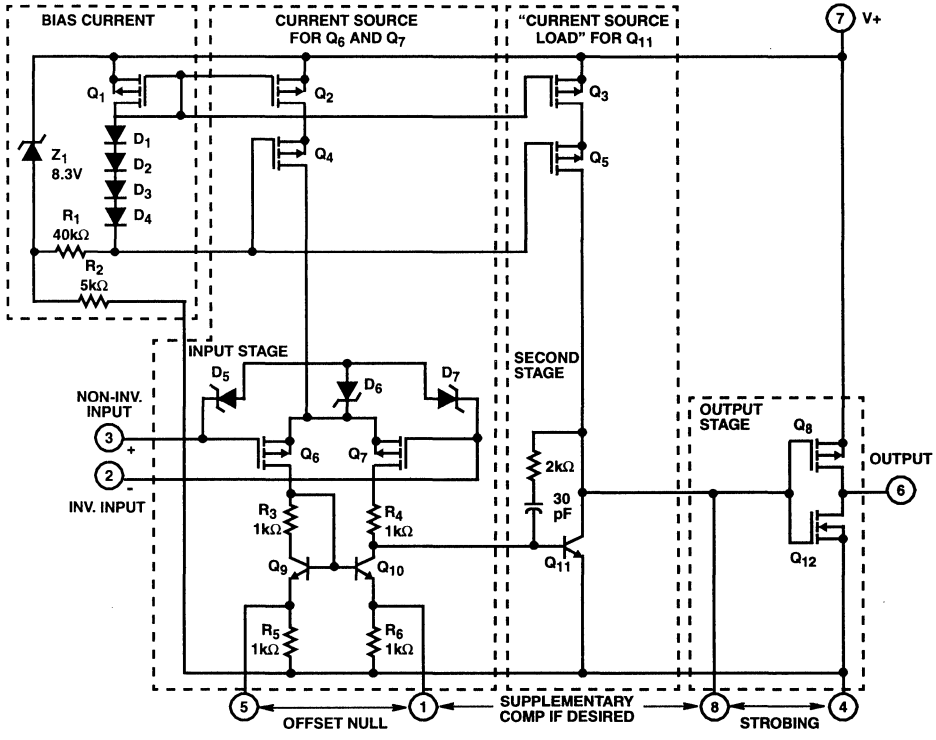
Block Diagram



NOTES:

4. Total supply voltage (for indicated voltage gains) = 15V with input terminals biased so that Terminal 6 potential is +7.5V above Terminal 4.
5. Total supply voltage (for indicated voltage gains) = 15V with output terminal driven to either supply rail.

Schematic Diagram



NOTE: Diodes D_5 Through D_7 Provide Gate Oxide Protection For MOSFET Input Stage.

Application Information

Circuit Description

Refer to the Block Diagram of the CA3160 series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3160 series circuits are ideal for single supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in the Block Diagram provide the total gain of the CA3160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive MOS digital circuits in comparator applications).

Input Stage - The circuit of the CA3160 is shown in the Schematic Diagram. It consists of a differential-input stage using PMOS field-effect transistors (Q_6, Q_7) working into a mirror-pair of bipolar transistors (Q_9, Q_{10}) functioning as load resistors together with resistors R_3 through R_6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q_{11}). Offset nulling, when desired, can be effected by connecting a 100,000Ω potentiometer across Terminals 1 and 5 and the potentiometer slider arm to Terminal 4. Cascode-connected PMOS transistors Q_2, Q_4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D_5 through D_7 provide gate-oxide protection against high-voltage transients, including static electricity during handling for Q_6 and Q_7.

Second-Stage - Most of the voltage gain in the CA3160 is provided by the second amplifier stage, consisting of bipolar transistor Q_{11} and its cascode-connected load resistance provided by PMOS transistors Q_3 and Q_5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30pF capacitor and 2kΩ resistor connected between the base and collector of transistor Q_{11}. These internal components

provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit - At total supply voltages, somewhat above 8.3V, resistor R_2 and zener diode Z_1 serve to establish a voltage of 8.3V across the series-connected circuit, consisting of resistor R_1, diodes D_1 through D_4, and PMOS transistor Q_1. A tap at the junction of resistor R_1 and diode D_4 provides a gate-bias potential of about 4.5V for PMOS transistors Q_4 and Q_5 with respect to Terminal 7. A potential of about 2.2V is developed across diode-connected PMOS transistor Q_1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q_2 and Q_3. It should be noted that Q_1 is "mirror-connected" to both Q_2 and Q_3. Since transistors Q_1, Q_2, Q_3 are designed to be identical, the approximately 200μA current in Q_1 establishes a similar current in Q_2 and Q_3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3V, zener diode Z_1 becomes nonconductive and the potential, developed across series-connected R_1, D_1 - D_4, and Q_1, varies directly with variations in supply voltage. Consequently, the gate bias for Q_4, Q_5 and Q_2, Q_3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3V. Operation at total supply voltages below about 4.5V results in seriously degraded performance.

Output Stage - The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 17. Typical op amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01% accuracy levels, including the negative supply rail.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000Ω potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input Current Variation with Common Mode Input Voltage

As shown in the Electrical Specifications, the input current for the CA3160 Series Op Amps is typically 5pA at $T_A = 25^oC$ when Terminals 2 and 3 are at a common-mode potential of +7.5V with respect to negative supply Terminal 4. Figure 23 contains data showing the variation of input current as a function of common-mode input voltage at $T_A = 25^oC$. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common-mode input voltage does not exceed 2V. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the metal can package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the metal can case of the CA3160 is also internally tied to Terminal 4, input Terminal 3 is essentially "guarded" from spurious leakage currents.

Input-Current Variation with Temperature

The input current of the CA3160 Series circuits is typically 5pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Figure 24 provides data on the typical variation of input bias current as a function of temperature in the CA3160.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input Offset Voltage (V_{IO}) Variation with DC Bias vs Device Operating Life

It is well known that the characteristics of a MOSFET device can change slightly when a DC gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential DC bias voltage applied across Terminals 2 and 3. Figure 25 shows typical data pertinent to shifts in offset voltage encountered with CA3160 devices in metal can packages during life testing. At lower temperatures (metal can and plastic) for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The 2V differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

Power Supply Considerations

Because the CA3160 is very useful in single supply applications, it is pertinent to review some considerations relating to power supply current consumption under both single and dual supply service. Figures 1A and 1B show the CA3160 connected for both dual and single supply operation.

Dual-supply operation: When the output voltage at Terminal 6 is 0V, the currents supplied by the two power supplies are equal. When the gate terminals of Q_8 and Q_{12} are driven

increasingly positive with respect to ground, current flow through Q_{12} (from the negative supply) to the load is increased and current flow through Q_8 (from the positive supply) decreases correspondingly. When the gate terminals of Q_8 and Q_{12} are driven increasingly negative with respect to ground, current flow through Q_8 is increased and current flow through Q_{12} is decreased accordingly.

Single supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage-drops across Q_8 and Q_{12} are of equal magnitude. Figure 18 shows typical quiescent supply-current vs supply voltage for the CA3160 operated under these conditions.

Since the output stage is operating as a Class A amplifier, the supply current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Figure 17). If either Q_8 or Q_{12} are swung out of their linear regions toward cutoff (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q_{12} is completely cut off and the supply current to series connected transistors Q_8, Q_{12} goes essentially to zero. The two preceding stages in the CA3160, however, continue to draw modest supply-current (see the lower curve in Figure 18) even though the output stage is strobed off. Figure 1A shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now-be assumed that a load resistance of nominal value (e.g., 2kΩ) is connected between Terminal 6 and ground in the circuit of Figure 1B. Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2. Since PMOS transistor Q_8 must now supply quiescent current to both R_L and transistor Q_{12}, it should be apparent that under these conditions the supply current must increase as an inverse function of the R_L magnitude. Figure 20 shows the voltage-drop across PMOS transistor Q_8 as a function of load current at several supply voltages. Figure 17 shows the voltage transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3160 is most advantageous in applications where in the source resistance of the input signal is on the order of 1MΩ or more. In this case, the total input-referred noise voltage is typically only 40μV when the test circuit amplifier of Figure 2 is operated at a total supply voltage of 15V. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1MΩ, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

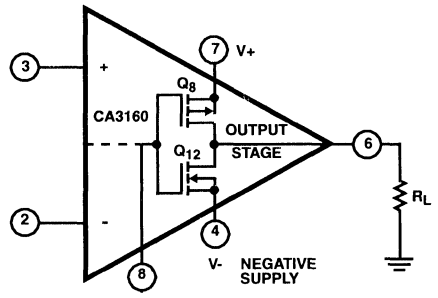


FIGURE 1A. DUAL POWER SUPPLY OPERATION

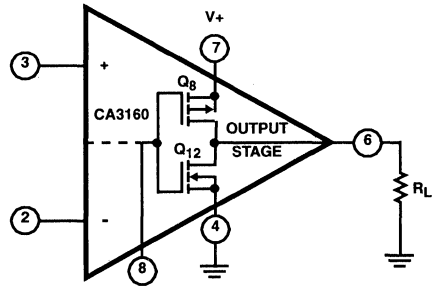


FIGURE 1B. SINGLE POWER SUPPLY OPERATION

FIGURE 1. CA3160 OUTPUT STAGE IN DUAL AND SINGLE POWER SUPPLY OPERATION

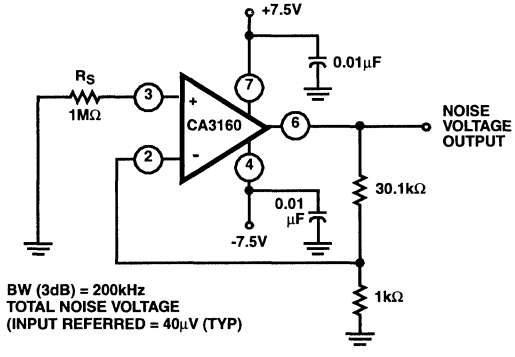


FIGURE 2. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENTS

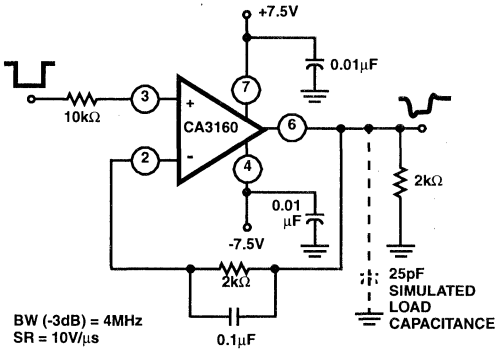
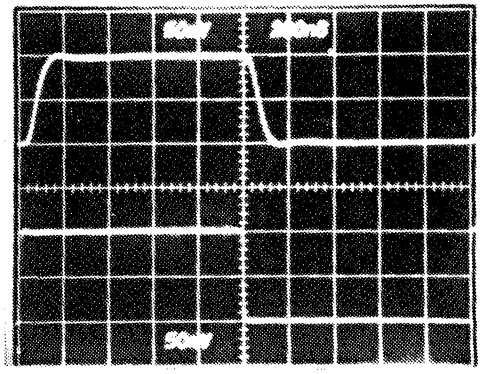
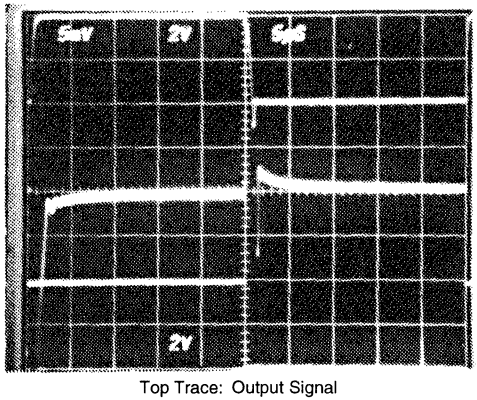


FIGURE 3A.



Top Trace: Output
Bottom Trace: Input

FIGURE 3B. SMALL SIGNAL RESPONSE



Top Trace: Output Signal
Center Trace: Difference Signal 5mV/Div.
Bottom Trace: Input Signal

FIGURE 3C. INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME

FIGURE 3. DUAL SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS

Typical Applications

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3160, are particularly suited to service as voltage followers. Figure 3 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3160 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Figure 4 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 4B with input-signal ramping. The waveforms in Figure 4C show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5V below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 4C also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3160 in a single supply voltage follower application.

9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC) (see Note 6) is shown in Figure 5. This system combines the concepts of multiple-switch CMOS ICs, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10V logic levels are used in the circuit of Figure 5.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power supply terminal. Each CD4007A contains three inverters, each inverter functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of 1% tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000Ω resistors from the same manufacturing lot.

A single 15V supply provides a positive bus for the CA3160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10V level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

NOTE:

6. "Digital-to-Analog Conversion Using the Harris CD4007A COS/MOS IC", Application Note AN6080.

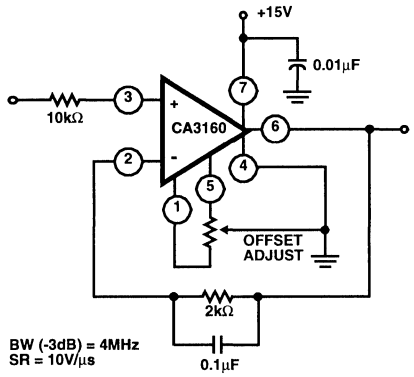
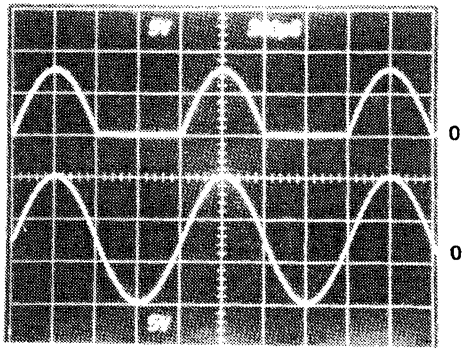


FIGURE 4A.



Top Trace: Output
Bottom Trace: Input

FIGURE 4B. OUTPUT WAVEFORM WITH GROUND REFERENCE SINE WAVE INPUT

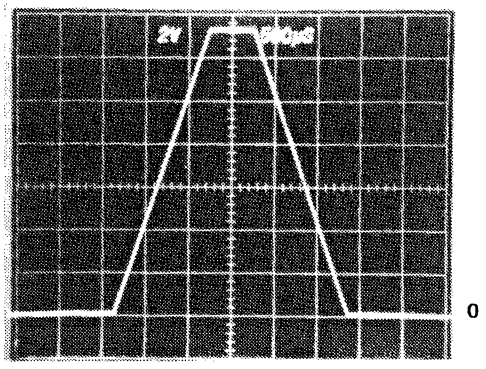


FIGURE 4C. OUTPUT SIGNAL WITH INPUT SIGNAL RAMPING

FIGURE 4. SINGLE SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS. (e.g., FOR USE IN SINGLE SUPPLY D/A CONVERTER; SEE FIGURE 9 IN AN6080)

Error-Amplifier in Regulated Power Supplies

The CA3160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Figure 6 uses a CA3160 as an error amplifier in a continuously adjustable 1A power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of 0V with only one DC power supply input.

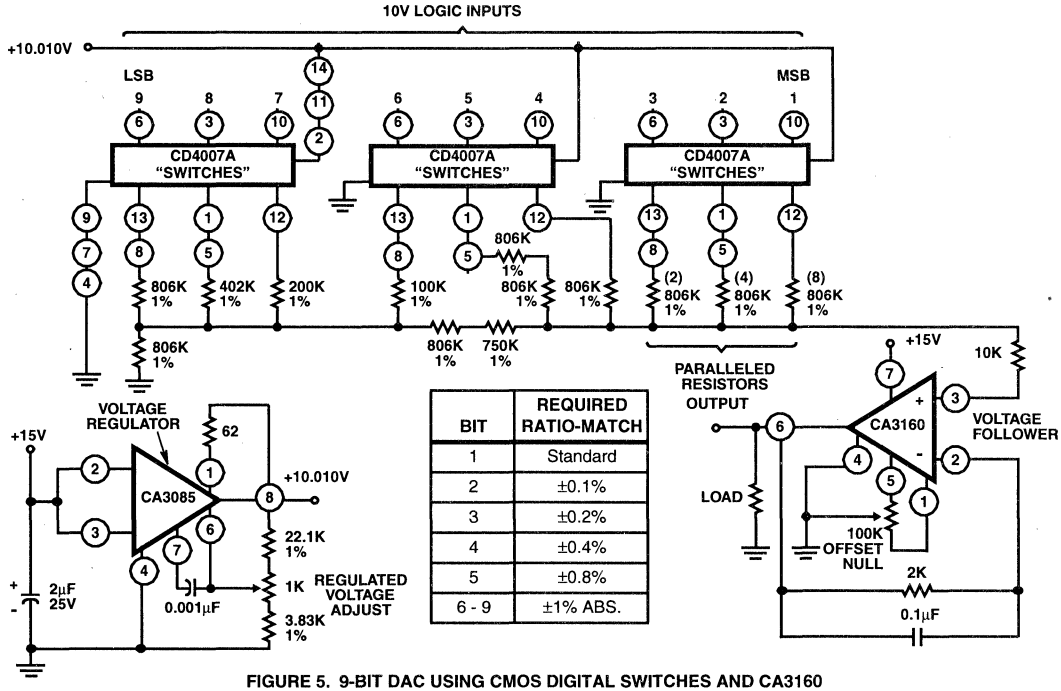
An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Figure 7. The oscillator operates with a tracking error in the order of 0.02% and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (Terminal 6) of A_1 (a CA3130) can swing within about 10mV of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{AVG} = V\ T_2/T_1$) is applied to the non-inverting Input terminal of comparator A_2 via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{AVG} = V_1$. This circuit condition is accomplished by feeding an output signal from Terminal 6 of A_2 through R_4, D_4 to the inverting terminal (Terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

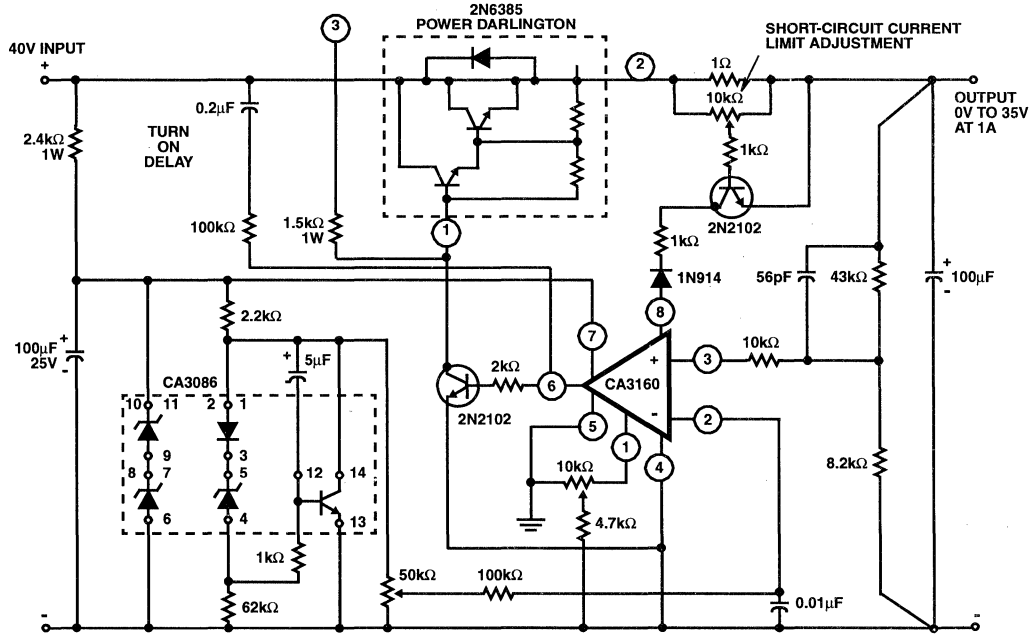
Voltmeter With High Input Resistance

The voltmeter circuit shown in Figure 8 illustrates an application in which a number of the CA3160 characteristics are exploited. Range-switch SW_1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10kΩ current-limiting resistor. The circuit is powered by a single 8.4V mercury battery. With zero input signal, the circuit consumes somewhat less than 500µA plus the meter current required to indicate a given voltage. Thus, at full scale input, the total supply current rises to slightly more than 1500µA.



BIT	REQUIRED RATIO-MATCH
1	Standard
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS.

FIGURE 5. 9-BIT DAC USING CMOS DIGITAL SWITCHES AND CA3160



Hum and Noise Output <250µV_{RMS}; Regulation (No Load to Full Load) <0.005%; Input Regulation <0.01%/V

FIGURE 6. VOLTAGE REGULATOR CIRCUIT (0.1V TO 35V AT 1A)

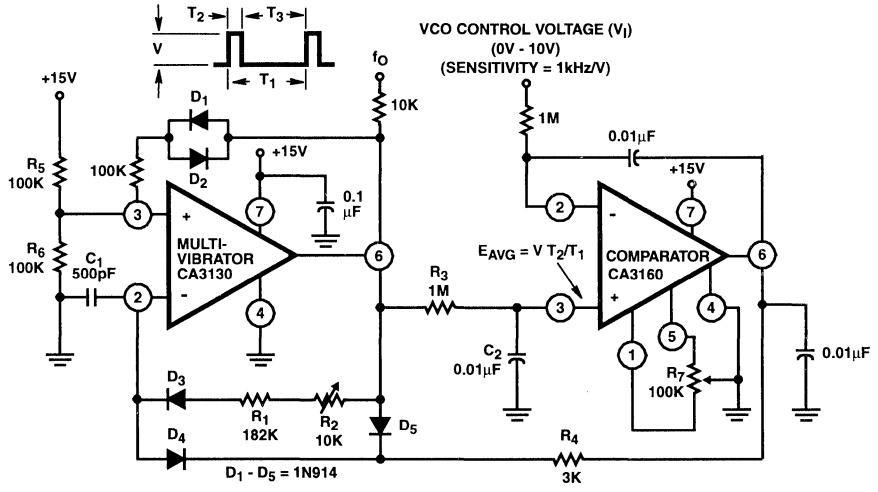


FIGURE 7. VOLTAGE CONTROLLED OSCILLATOR

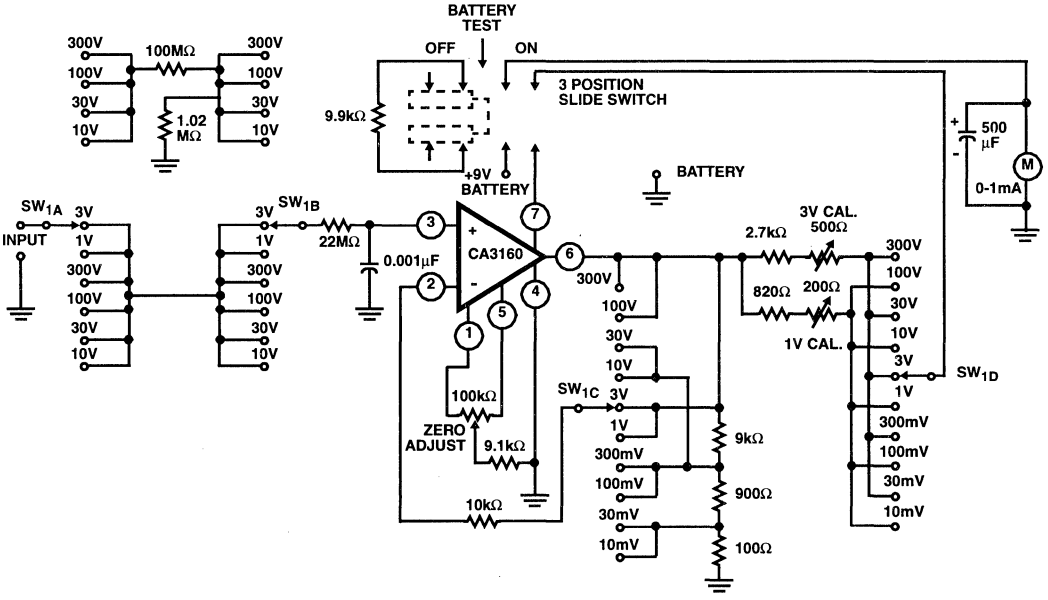


FIGURE 8. HIGH INPUT RESISTANCE DC VOLTMETER

Function Generator

A function generator having a wide tuning range is shown in Figure 9. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA3160 as a voltage follower, a CA3080 as a high speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C_1, C_2, and C_3 shape the triangular signal between 500kHz and 1MHz. Capacitors C_4, C_5, and the trimmer potentiometer in series with C_5 maintain essentially constant (+10%) amplitude up to 1MHz.

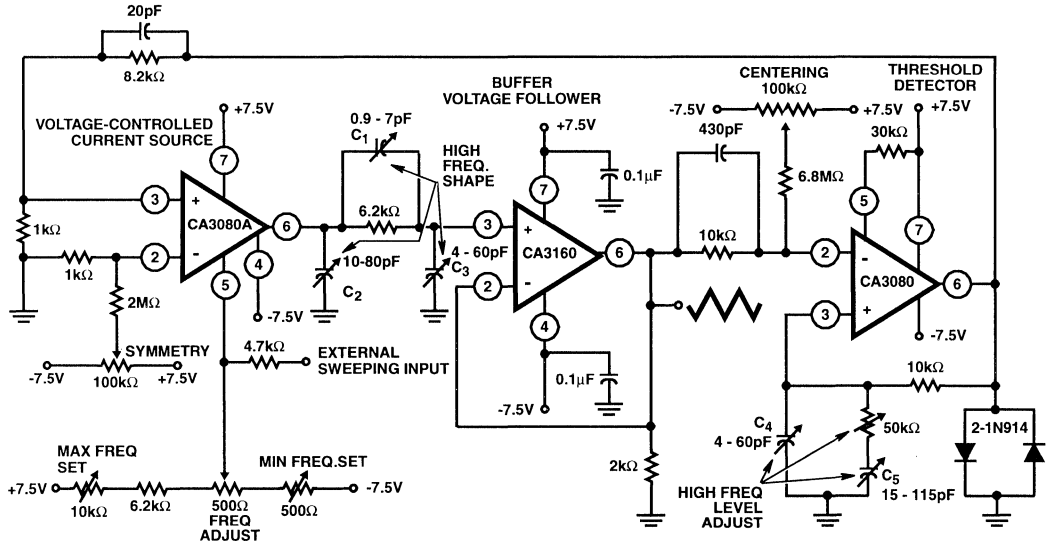
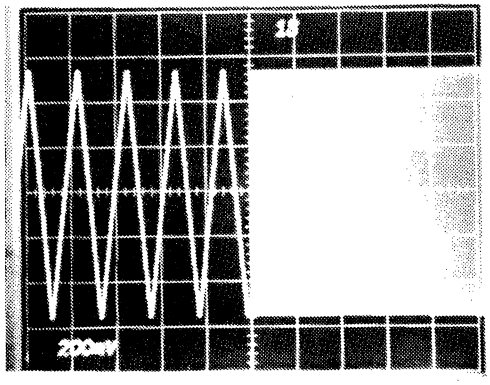
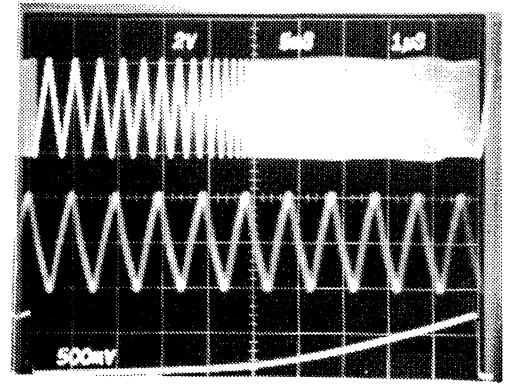


FIGURE 9A. HIGH INPUT RESISTANCE DC VOLTMETER



NOTE: A square wave signal modulates the external sweeping input to produce 1Hz and 1MHz, showing the 1,000,000/1 frequency range of the Function Generator.

FIGURE 10. TWO-TONE OUTPUT SIGNAL FROM THE FUNCTION GENERATOR



NOTE: The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1MHz signal via delayed oscilloscope triggering of the upper swept output signal.

FIGURE 10A. TRIPLE-TRACE OF THE FUNCTION GENERATOR SWEEPING TO 1MHz

FIGURE 10. 1,000,000/1 SINGLE CONTROL FUNCTION GENERATOR: 1Hz to 1MHz

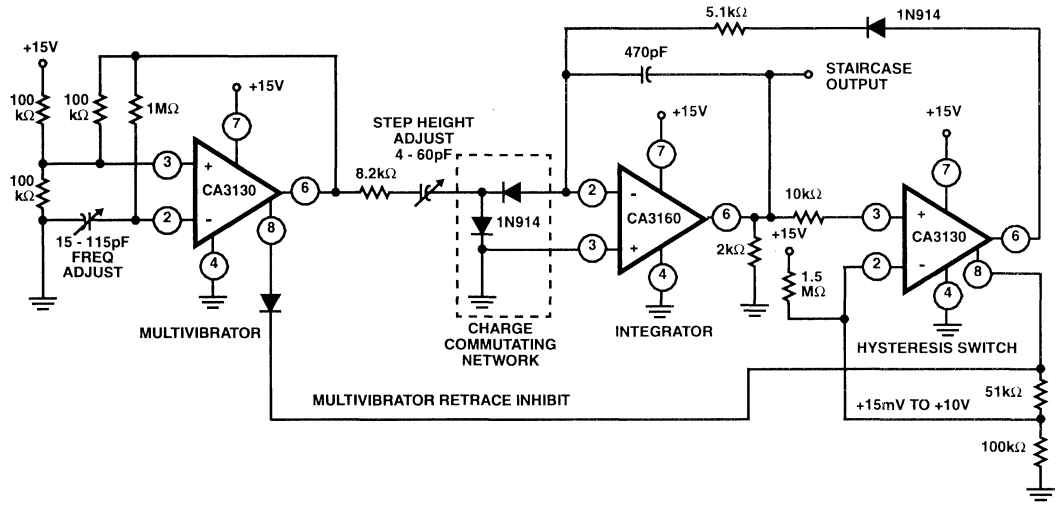


FIGURE 11A.

Staircase Generator

Figure 10 shows a staircase generator circuit utilizing three CMOS operational amplifiers. Two CA3130s are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA3160, is used as a linear staircase generator.

Picoammeter Circuit

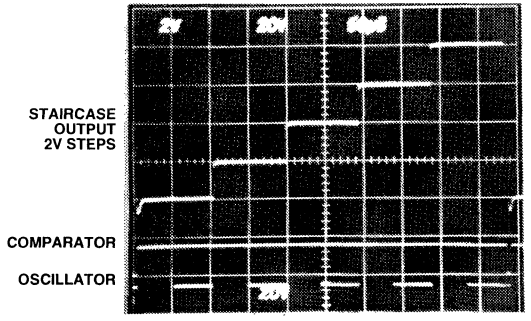
Figure 11 is a current-to-voltage converter configuration utilizing a CA3160 and CA3140 to provide a picoampere meter for 13pA full scale meter deflection. By placing Terminals 2 and 4 of the CA3160 at ground potential, the CA3160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA3160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Figure 23.

To further enhance the stability of this circuit, the CA3160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9kΩ resistor in series with a 100Ω resistor sets the voltage at the 10GΩ resistor (in series with Terminal 3) to ±30mV full-scale deflection. This 30mV signal results from ±3V appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9kΩ and 100Ω network similar to that used in voltmeter circuit shown in Figure 8, a current range of 3pA to 1nA full scale can be handled with the single 10GΩ resistor.



Top Trace: Staircase Output 2V Steps
Center Trace: Comparator
Bottom Trace: Oscillator

FIGURE 11B. STAIRCASE GENERATOR WAVEFORM

FIGURE 11. STAIRCASE GENERATOR CIRCUIT

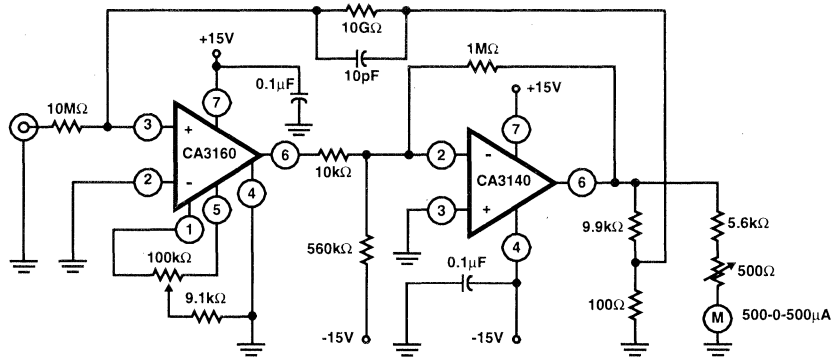


FIGURE 12. CURRENT-TO-VOLTAGE CONVERTER TO PROVIDE A PICOAMMETER WITH ±3pA FULL SCALE DEFLECTION

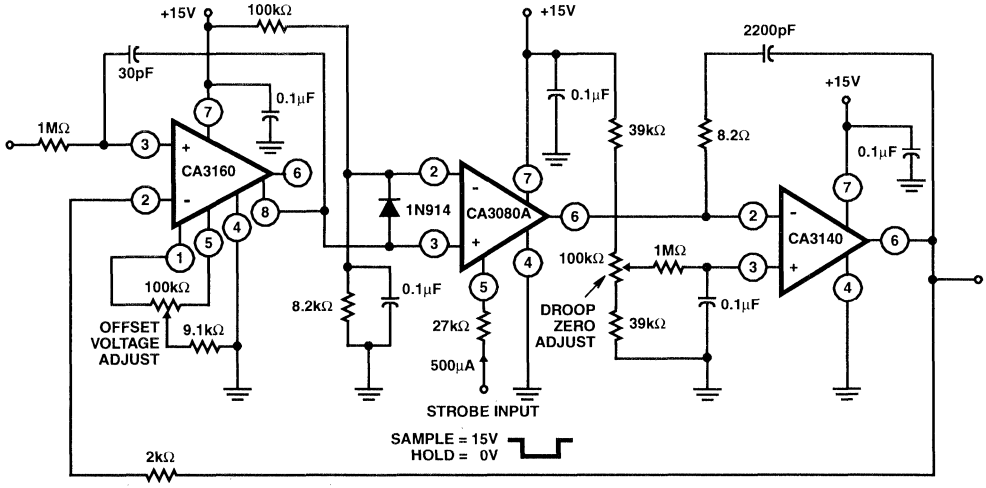
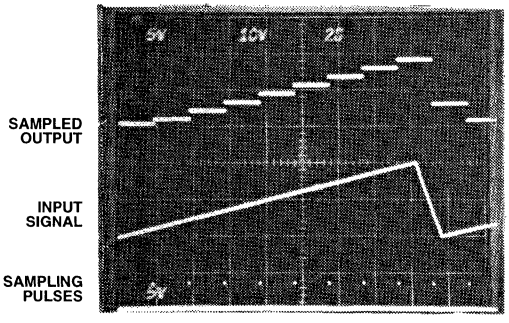
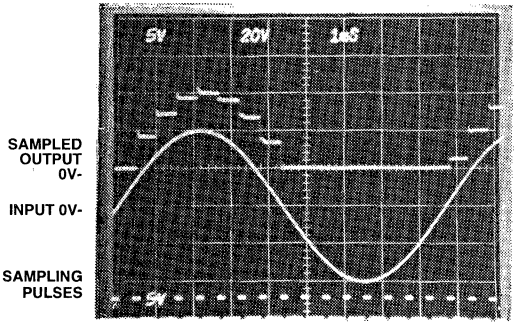


FIGURE 13A.



Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses

FIGURE 13B. SAMPLE AND HOLD WAVEFORM



Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses

FIGURE 13C. SAMPLE AND HOLD WAVEFORM

FIGURE 13. SINGLE SUPPLY SAMPLE AND HOLD SYSTEM, INPUT 0V TO 10V

Single Supply Sample-and-Hold System

Figure 12 shows a single supply sample-and-hold system using a CA3160 to provide a high input impedance and an input voltage range of 0V to 10V. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100kΩ bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320mV at the amplifier bias circuit terminal (5) at least 1100pA of output current will be available.

Wien Bridge Oscillator

A simple, single supply Wien Bridge oscillator using a CA3160 is shown in Figure 13. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1V. The 500Ω potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

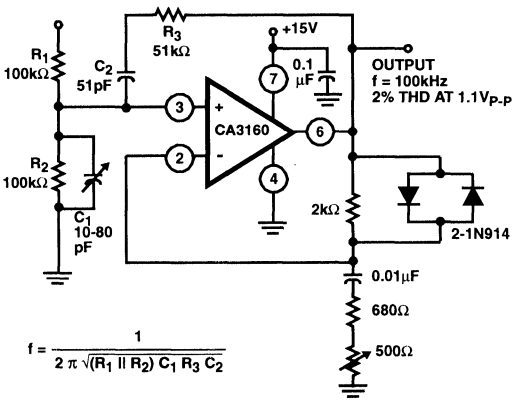


FIGURE 14. SINGLE SUPPLY WEIN BRIDGE OSCILLATOR

Operation with Output Stage Power Booster

The current sourcing and sinking capability of the CA3160 output stage is easily supplemented to provide power-boost capability. In the circuit of Figure 14, three CMOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA3160. In the Class A mode of CA3600E shown, a typical device consumes 20mA of supply current at 15V operation. This arrangement boosts the current-handling capability of the CA3160 output stage by about 2.5X.

The amplifier circuit in Figure 14 employs feedback to establish a closed-loop gain of 20dB. The typical large-signal-bandwidth (-3dB) is 190kHz.

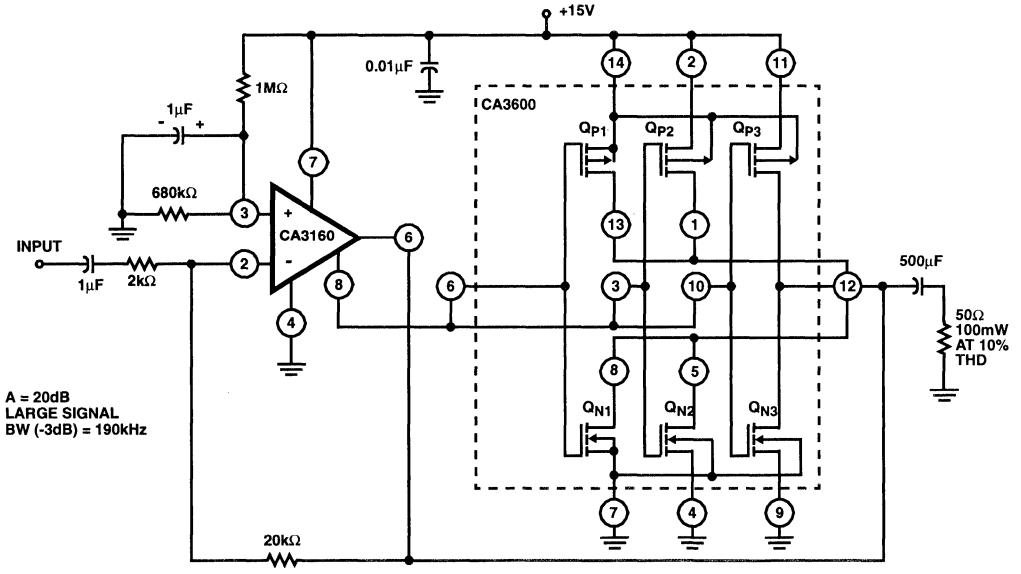


FIGURE 15. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA3160

Typical Performance Curves

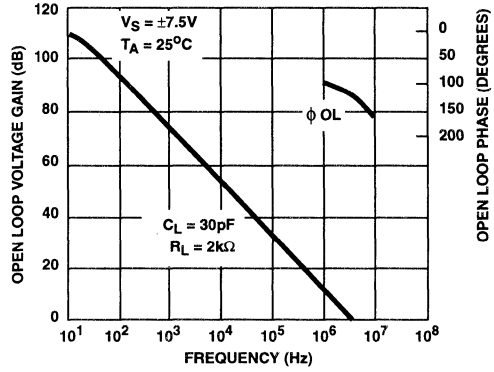


FIGURE 16. OPEN LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY

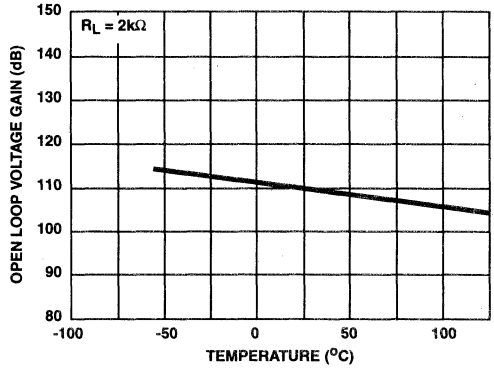


FIGURE 17. OPEN LOOP GAIN vs TEMPERATURE

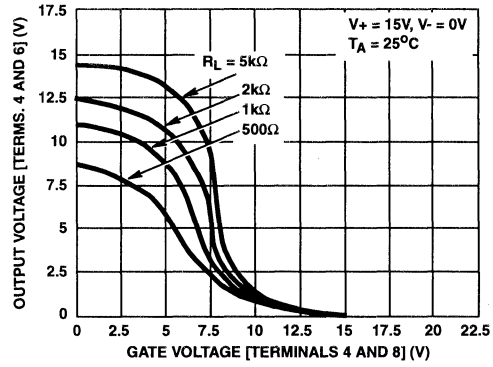


FIGURE 18. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS OUTPUT STAGE

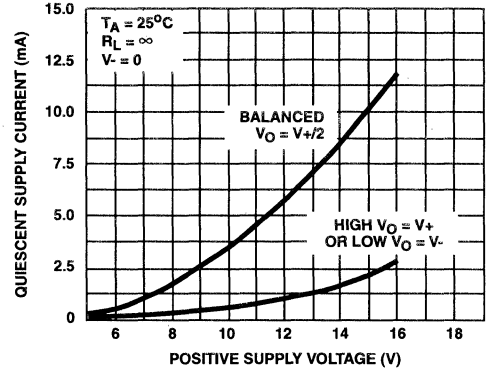


FIGURE 19. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

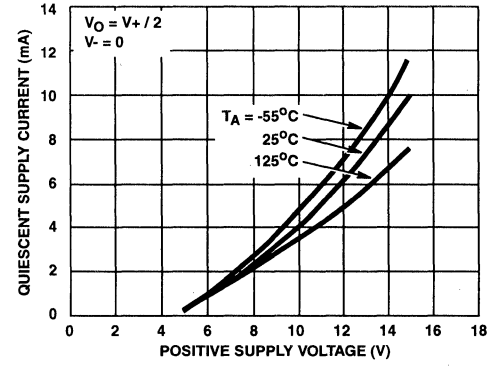


FIGURE 20. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

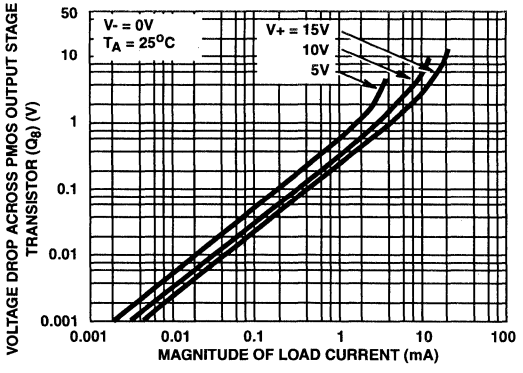


FIGURE 21. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q_8) vs LOAD CURRENT

Typical Performance Curves (Continued)

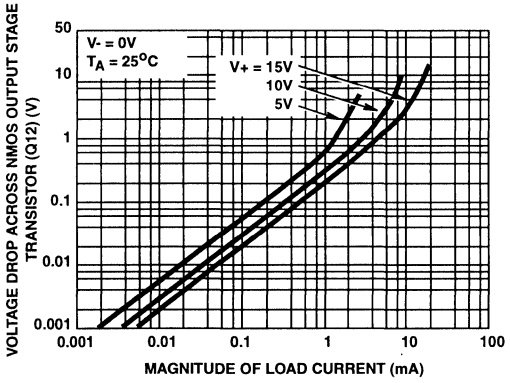


FIGURE 22. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q_{12}) vs LOAD CURRENT

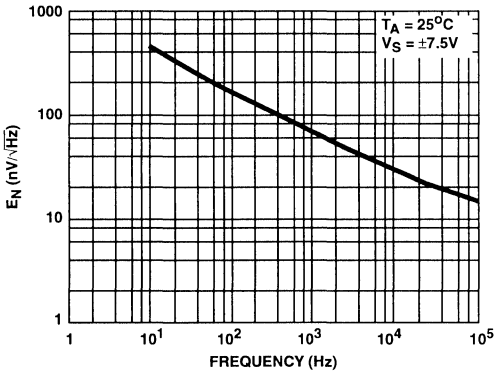


FIGURE 23. EQUIVALENT NOISE VOLTAGE vs FREQUENCY

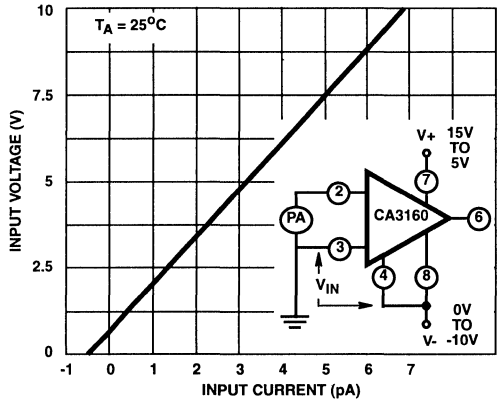


FIGURE 24. INPUT CURRENT vs COMMON MODE VOLTAGE

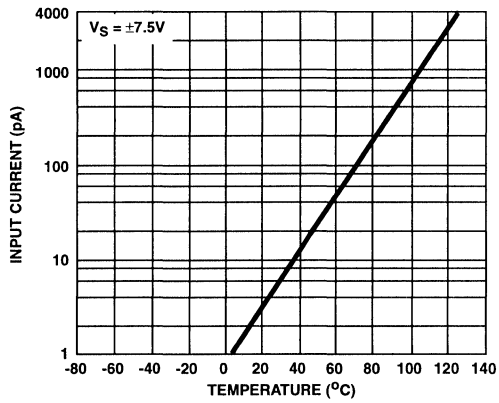


FIGURE 25. INPUT CURRENT vs TEMPERATURE

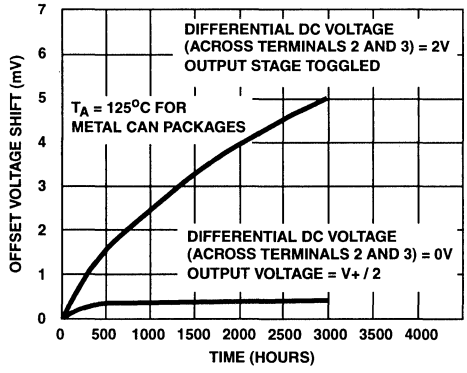


FIGURE 26. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

CA3193, CA3193A

November 1996

1.2MHz, BiCMOS Precision Operational Amplifiers

Features

- Low V_{IO}
  - CA3193A ..... 200μV (Max)
  - CA3193 ..... 500μV (Max)
- Low $\Delta V_{IO}/\Delta T$
  - CA3193A ..... 3μV/°C (Max)
  - CA3193 ..... 5μV/°C (Max)
- Low I_{IO} and I_I
- Low $\Delta I_{IO}/\Delta T$: CA3193..... 150pA/°C (Max)
- Low $\Delta I_I/\Delta T$: CA3193 ..... 3.7nA/°C (Max)

Applications

- Thermocouple Preamplifiers
- Strain Gauge Bridge Amplifiers
- Summing Amplifiers
- Differential Amplifiers
- Bilateral Current Sources
- Log Amplifiers
- Differential Voltmeters
- Precision Voltage References
- Active Filters
- Buffers
- Integrators
- Sample-and-Hold Circuits
- Low Frequency Filters

Description

The CA3193A and CA3193 are ultra-stable, precision instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3193A and CA3193 amplifiers are internally phase compensated and provide a gain bandwidth product of 1.2MHz. They are pin compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741 series types in most applications.

The CA3193A and CA3193 can also be used as functional replacements for op amp types 725, 108A, OP-5, OP-7, LM11 and LM714 in many applications where nulling is not employed. Because of their low offset voltage and low offset voltage vs temperature coefficient the CA3193A and CA3193 amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high gain filters, buffer, strain gauge bridge amplifiers and precision voltage references.

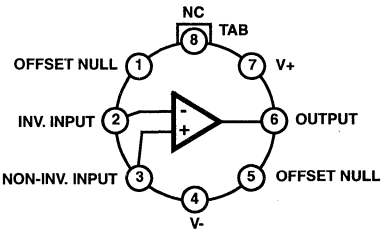
The two types in the CA3193 series are functionally identical. The CA3193A and CA3193 operate from supply voltages of ±3.5V to ±18V.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3193AE	-25 to 85	8 Ld PDIP	E8.3
CA3193AT	-25 to 85	8 Pin Metal Can	T8.C
CA3193E	0 to 70	8 Ld PDIP	E8.3
CA3193T	0 to 70	8 Pin Metal Can	T8.C

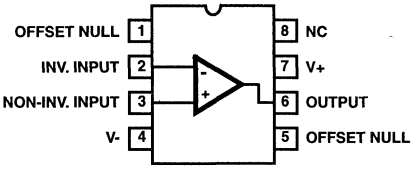
Pinouts

CA3193
(METAL CAN)
TOP VIEW



NOTE: Pin 4 is connected to case on S and T suffix.

CA3193
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1249.2**

CA3240, CA3240A

Dual, 4.5MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar Output

November 1996

Features

- Dual Version of CA3140
- Internally Compensated
- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}) 1.5TΩ (Typ)
  - Very Low Input Current (I_I) 10pA Typ. at ±15V
  - Wide Common-Mode Input Voltage Range (V_{ICR}): Can Be Swung 0.5V Below Negative Supply Voltage Rail
- Directly Replaces Industry Type 741 in Most Applications

Applications

- Ground Referenced Single Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (Microseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Intrusion Alarm System
- Comparators
- Instrumentation Amplifiers
- Active Filters
- Function Generators
- Power Supplies

Description

The CA3240A and CA3240 are dual versions of the popular CA3140 series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOSFET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

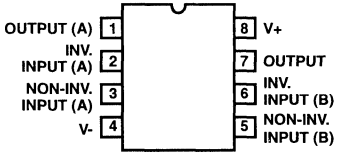
The CA3240A and CA3240 are compatible with the industry standard 1458 operational amplifiers in similar packages. The offset null feature is available only when these types are supplied in the 14 lead PDIP package (E1 suffix).

Ordering Information

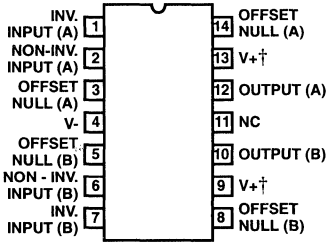
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3240AE	-40 to 85	8 Ld PDIP	E8.3
CA3240AE1	-40 to 85	14 Ld PDIP	E14.3
CA3240E	-40 to 85	8 Ld PDIP	E8.3
CA3240E1	-40 to 85	14 Ld PDIP	E14.3

Pinouts

CA3240, CA3240A, (PDIP)
TOP VIEW

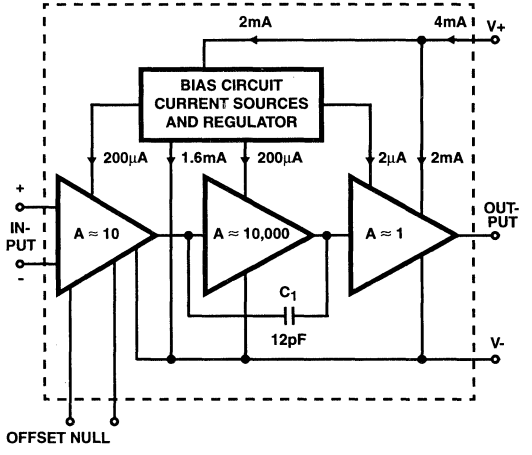


CA3240, CA3240A, (PDIP)
TOP VIEW



† Pins 9 and 13 internally connected through approximately 3Ω.

Functional Diagram



NOTE: Only available with 14 lead DIP (E1 Suffix).

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **1050.3**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V-) 36V
Differential Input Voltage. 8V
Input Voltage. . . . . (V+ +8V) to (V- -0.5V)
Input Current. 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Voltage Range . . . . . 4V to 36V or ±2V to ±18V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
8 Lead PDIP Package	100
14 Lead PDIP Package	100

Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

For Equipment Design, V_{SUPPLY} = ±15V, T_A = $25^{o}C$, Unless Otherwise Specified

PARAMETER	SYMBOL	CA3240			CA3240A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	-	5	15	-	2	5	mV
Input Offset Current	I_{IO}	-	0.5	30	-	0.5	20	pA
Input Current	I_I	-	10	50	-	10	40	pA
Large-Signal Voltage Gain (See Figures 13, 28) (Note 3)	A_{OL}	20	100	-	20	100	-	kV/V
		86	100	-	86	100	-	dB
Common Mode Rejection Ratio (See Figure 18)	CMRR	-	32	320	-	32	320	µV/V
		70	90	-	70	90	-	dB
Common Mode Input Voltage Range (See Figure 25)	V_{ICR}	-15	-15.5 to +12.5	11	-15	-15.5 to +12.5	12	V
Power Supply Rejection Ratio (See Figure 20)	PSRR	-	100	150	-	100	150	µV/V
	($\Delta V_{IO}/\Delta V\pm$)	76	80	-	76	80	-	dB
Maximum Output Voltage (Note 4) (See Figures 24, 25)	$V_{OM}+$	12	13	-	12	13	-	V
	$V_{OM}-$	-14	-14.4	-	-14	-14.4	-	V
Maximum Output Voltage (Note 5)	$V_{OM}-$	0.4	0.13	-	0.4	0.13	-	V
Total Supply Current (See Figure 16) For Both Amps	I+	-	8	12	-	8	12	mA
Total Device Dissipation	P_D	-	240	360	-	240	360	mW

NOTES:

3. At V_O = $26V_{P-P}$, +12V, -14V and R_L = 2kΩ.
4. At R_L = 2kΩ.
5. At V+ = 5V, V- = GND, I_{SINK} = 200µA.

Electrical Specifications

For Equipment Design, V_{SUPPLY} = ±15V, T_A = $25^{o}C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS
			CA3240A	CA3240	
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typical Value of Resistor Between Terminals 4 and 3(5) or Between 4 and 14(8) to Adjust Maximum V_{IO}	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Figure 2)	e_N	BW = 140kHz, R_S = 1MΩ	48	48	µV

Electrical Specifications For Equipment Design, $V_{SUPPLY} = \pm 15V$, $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Equivalent Input Noise Voltage (See Figure 19)	e_N	f = 1kHz, $R_S = 100\Omega$		40	40	$nV/\sqrt{Hz}$
		f = 10kHz, $R_S = 100\Omega$		12	12	$nV/\sqrt{Hz}$
Short-Circuit Current to Opposite Supply	I_{OM+}	Source		40	40	mA
	I_{OM-}	Sink		11	11	mA
Gain Bandwidth Product (See Figures 14, 28)	f_T			4.5	4.5	MHz
Slew Rate (See Figure 15)	SR			9	9	V/µs
Transient Response (See Figure 1)	t_r	$R_L = 2k\Omega$, $C_L = 100pF$	Rise Time	0.08	0.08	µs
	OS	$R_L = 2k\Omega$, $C_L = 100pF$	Overshoot	10	10	%
Settling Time at 10 V_{P-P} (See Figure 26)	t_S	$A_V = +1$, $R_L = 2k\Omega$, $C_L = 100pF$, Voltage Follower	To 1mV	4.5	4.5	µs
			To 10mV	1.4	1.4	µs
Crosstalk (See Figure 23)		f = 1kHz		120	120	dB

Electrical Specifications For Equipment Design, at $V_{SUPPLY} = \pm 15V$, $T_A = -40$ to 85^oC, Unless Otherwise Specified

PARAMETER	SYMBOL	TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Input Offset Voltage	$\|V_{IO}\|$	3	10	mV
Input Offset Current (Note 8)	$\|I_{IO}\|$	32	32	pA
Input Current (Note 8)	I_I	640	640	pA
Large Signal Voltage Gain (See Figures 13, 28), (Note 6)	A_{OL}	63	63	kV/V
		96	96	dB
Common Mode Rejection Ratio (See Figure 18)	CMRR	32	32	µV/V
		90	90	dB
Common Mode Input Voltage Range (See Figure 25)	V_{ICR}	-15 to +12.3	-15 to +12.3	V
Power Supply Rejection Ratio (See Figure 20)	PSRR	150	150	µV/V
	$(\Delta V_{IO}/\Delta V\pm)$	76	76	dB
Maximum Output Voltage (Note 7) (See Figures 24, 25)	V_{OM+}	12.4	12.4	V
	V_{OM-}	-14.2	-14.2	V
Supply Current (See Figure 16) Total For Both Amps	I+	8.4	8.4	mA
Total Device Dissipation	P_D	252	252	mW
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	15	15	$\mu V/^oC$

NOTES:

6. At $V_O = 26V_{P-P}$, +12V, -14V and $R_L = 2k\Omega$.
7. At $R_L = 2k\Omega$.
8. At $T_A = 85^oC$.

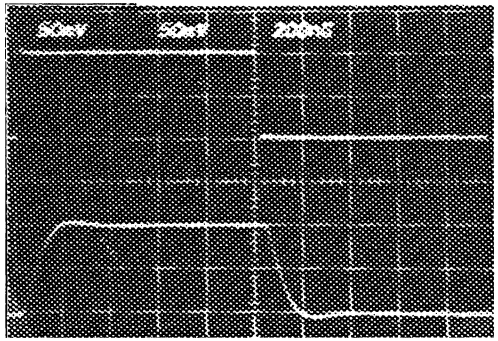
Electrical Specifications For Equipment Design, at V+ = 5V, V- = 0V, $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Input Offset Voltage	$\|V_{IO}\|$	2	5	mV
Input Offset Current	$\|I_{IO}\|$	0.1	0.1	pA
Input Current	I_I	2	2	pA
Input Resistance	R_{IN}	1	1	TΩ
Large Signal Voltage Gain (See Figures 13, 28)	A_{OL}	100	100	kV/V
		100	100	dB

Electrical Specifications For Equipment Design, at V+ = 5V, V- = 0V, T_A = 25°C, Unless Otherwise Specified **(Continued)**

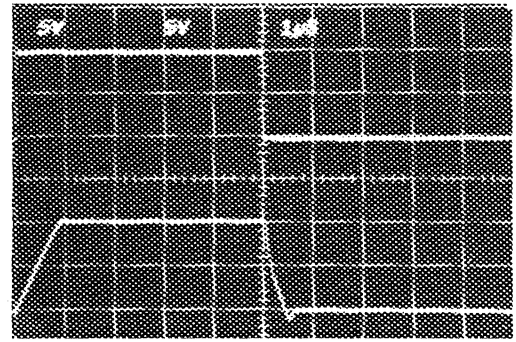
PARAMETER		SYMBOL	TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Common-Mode Rejection Ratio		CMRR	32	32	µV/V
			90	90	dB
Common-Mode Input Voltage Range (See Figure 25)		V_{ICR}	-0.5	-0.5	V
			2.6	2.6	V
Power Supply Rejection Ratio		PSRR	31.6	31.6	µV/V
			90	90	dB
Maximum Output Voltage (See Figures 24, 25)		V_{OM+}	3	3	V
		V_{OM-}	0.3	0.3	V
Maximum Output Current	Source	I_{OM+}	20	20	mA
	Sink	I_{OM-}	1	1	mA
Slew Rate (See Figure 15)		SR	7	7	V/µs
Gain Bandwidth Product (See Figure 14)		f_T	4.5	4.5	MHz
Supply Current (See Figure 16)		I+	4	4	mA
Device Dissipation		P_D	20	20	mW

Test Circuits and Waveforms



50mV/Div., 200ns/Div.
Top Trace: Input, Bottom Trace: Output

FIGURE 1A. SMALL SIGNAL RESPONSE



5V/Div., 1µs/Div.
Top Trace: Input, Bottom Trace: Output

FIGURE 1B. LARGE SIGNAL RESPONSE

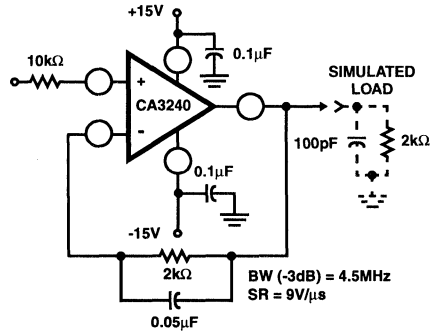


FIGURE 1C. TEST CIRCUIT

FIGURE 1. SPLIT-SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS

Test Circuits and Waveforms (Continued)

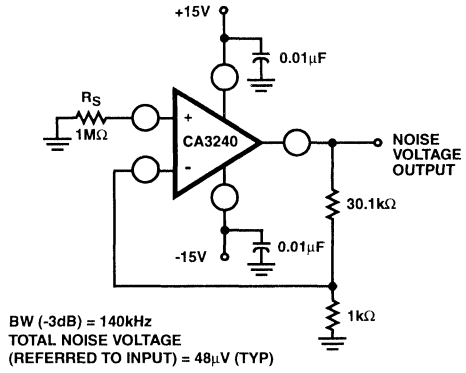
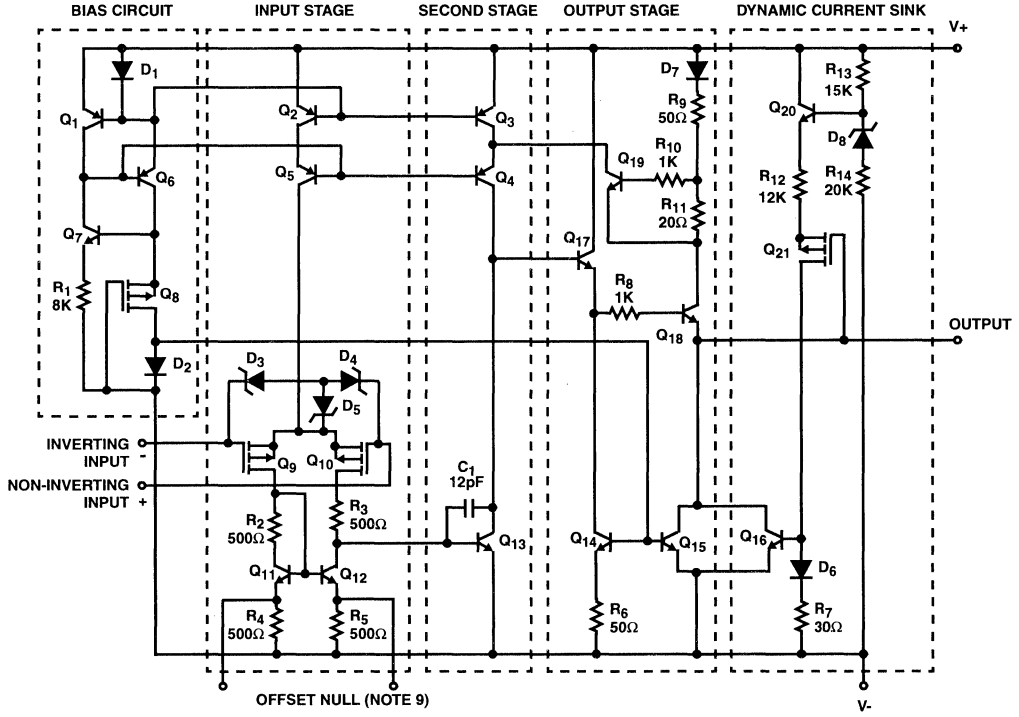


FIGURE 2. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT

Schematic Diagram (One Amplifier of Two)



NOTES:

9. Only available with 14 Lead DIP (E1 Suffix).
10. All resistance values are in ohms.

Application Information

Circuit Description

The schematic diagram details one amplifier section of the CA3240. It consists of a differential amplifier stage using PMOS transistors (Q_9 and Q_{10}) with gate-to-source protection against static discharge damage provided by zener diodes D_3, D_4, and D_5. Constant current bias is applied to the differential amplifier from transistors Q_2 and Q_5 connected as a constant current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q_{13} by means of an NPN current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14 lead plastic package (E1 suffix) is provided through the use of this current mirror.

The gain stage transistor Q_{13} has a high impedance active load (Q_3 and Q_4) to provide maximum open-loop gain. The collector of Q_{13} directly drives the base of the compound emitter-follower output stage. Pulldown for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q_{14} and Q_{15} and (2) dynamic current-sink transistor Q_{16} and its associated circuitry. *The level of pulldown current is constant at about 1mA for Q_{15} and varies from 0 to 18mA for Q_{16} depending on the magnitude of the voltage between the output terminal and V+.* The dynamic current sink becomes active whenever the output terminal is more negative than V+ by about 15V. When this condition exists, transistors Q_{21} and Q_{16} are turned on causing Q_{16} to sink current from the output terminal to V-. This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q_{18} if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2V (V_{CE} (sat)) of V- with a 2kΩ load to ground. *When the load is returned to V+, it may be necessary to supplement the 1mA of current from Q_{15} in order to turn on the dynamic current sink (Q_{16}).* This may be accomplished by placing a resistor (Approx. 2kΩ) between the output and V-.

Output Circuit Considerations

Figure 24 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 3 shows some typical configurations. Note that a series resistor, RL, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as 0.5V below V-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9kW resistor is sufficient.

The typical input current is on the order of 10pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, rasing the chip temperature and resulting in increased input current. Figure 4 shows typical input-terminal current versus ambient temperature for the CA3240.

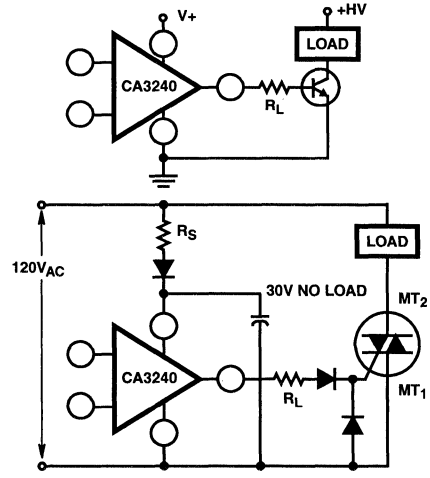


FIGURE 3. METHODS OF UTILIZING THE V_{CE} (SAT) SINKING CURRENT CAPABILITY OF THE CA3240 SERIES

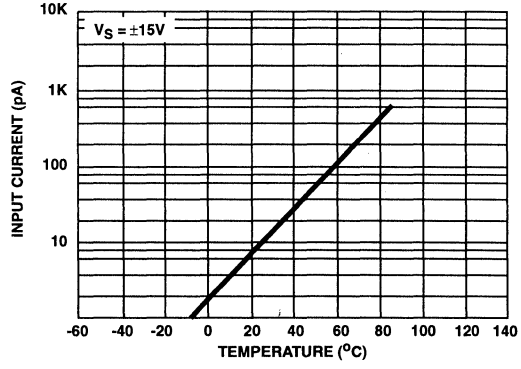


FIGURE 4. INPUT CURRENT vs TEMPERATURE

It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

Offset-Voltage Nulling

The input offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10kΩ potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Figure 5A. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Figure 5B, to optimize its utilization range are given in the table "Electrical Specifications for Equipment Design" shown on third page of this data sheetAn alternate system is shown in Figure 5C. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to 0Ω at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

Typical Applications

On/Off Touch Switch

The on/off touch switch shown in Figure 6 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Terminal 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing TRIAC driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the TRIAC is turned on and held on by the CA3059 and its associated positive feedback circuitry (51kΩ resistor and 36kΩ/42kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the TRIAC is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

Dual Level Detector (Window Comparator)

Figure 7 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Figure 6. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor..

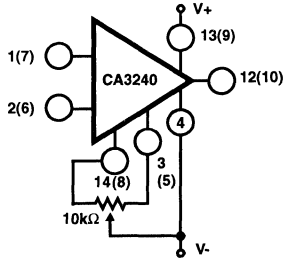


FIGURE 5A. BASIC

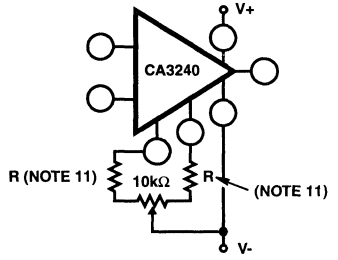


FIGURE 5B. IMPROVED RESOLUTION

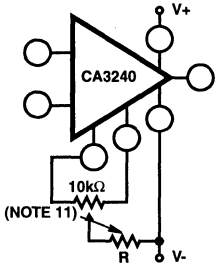
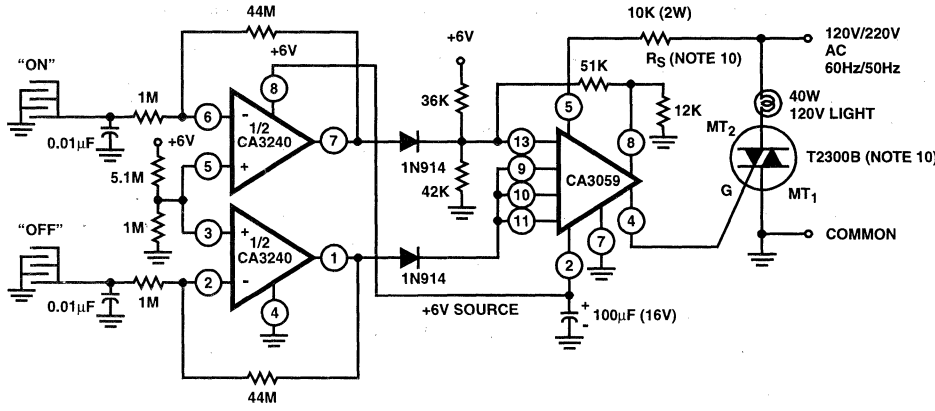


FIGURE 5C. SIMPLER IMPROVED RESOLUTION

NOTE:

11. See Electrical Specification Table on Third page of this data sheet for value of R.

FIGURE 5. THREE OFFSET-VOLTAGE NULLING METHODS, (CA3240AE1, CA3240E1 ONLY)



NOTE:

12. At 220V operation, TRIAC should be T2300D, R_S = 18K, 5W.

FIGURE 6. ON/OFF TOUCH SWITCH

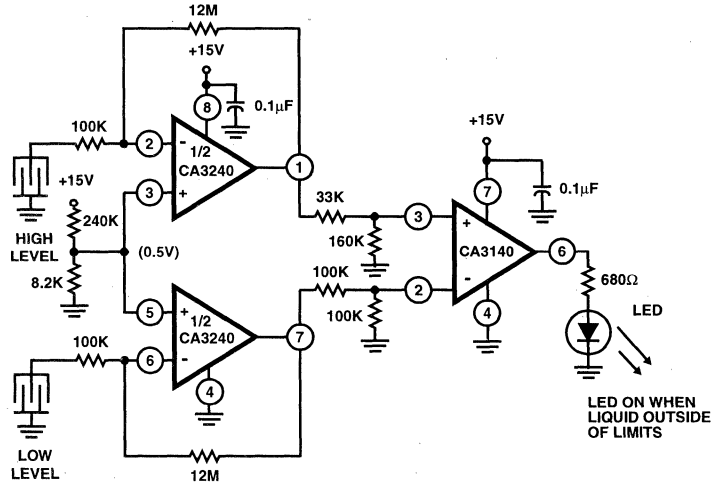


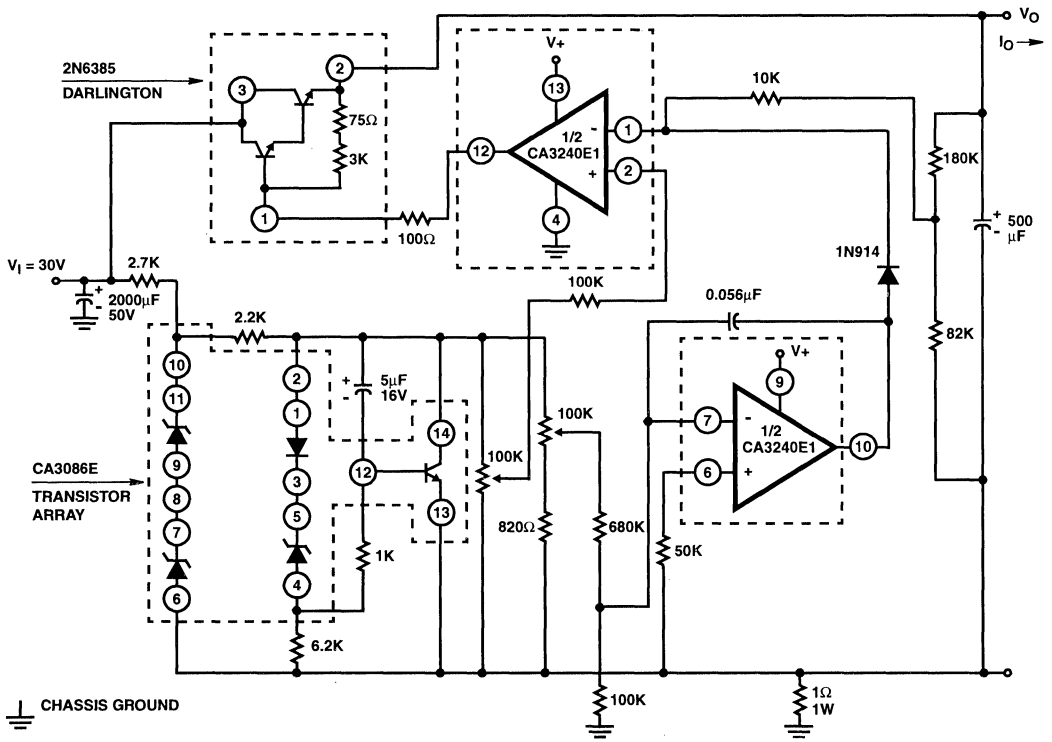
FIGURE 7. DUAL LEVEL DETECTER

Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Figure 8 uses the CA3240E1 as a voltage-error and current-sensing amplifier. The CA3240E1 is ideal for this application because its input common-mode voltage range includes ground, allowing the supply to adjust from 20mV to 25V without requiring a negative supply voltage. Also, the ground reference capability of the CA3240E1 allows it to sense the voltage across the 1Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40W. Figure 9 shows the transient response of the supply during a 100mA to 1A load transition.

Precision Differential Amplifier

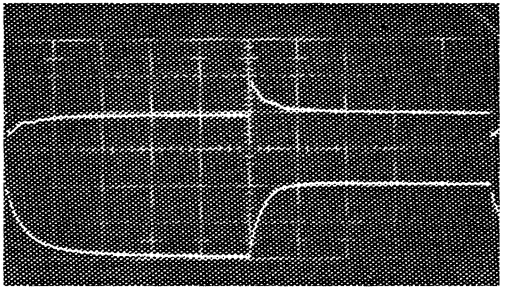
Figure 10 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10MΩ resistors have been used to limit the current to less than 2μA without affecting the performance of the circuit. Figure 11 shows a typical electrocardiogram waveform obtained with this circuit.



V_O RANGE = 20mV TO 25V
LOAD REGULATION:
VOLTAGE <0.08%
CURRENT <0.05%

OUTPUT HUM AND NOISE ≤ 150μV_{RMS}
(10MHz BANDWIDTH)
SINE REGULATION ≤ 0.1%/V_O
I_O RANGE = 10mA - 1.3A

FIGURE 8. CONSTANT-VOLTAGE/CONSTANT-CURRENT POWER SUPPLY



Top Trace: Output Voltage;
500mV/Div., 5μs/Div.

Bottom Trace: Collector Of Load Switching Transistor
Load = 100mA to 1A; 5V/Div., 5μs/Div.

FIGURE 9. TRANSIENT RESPONSE

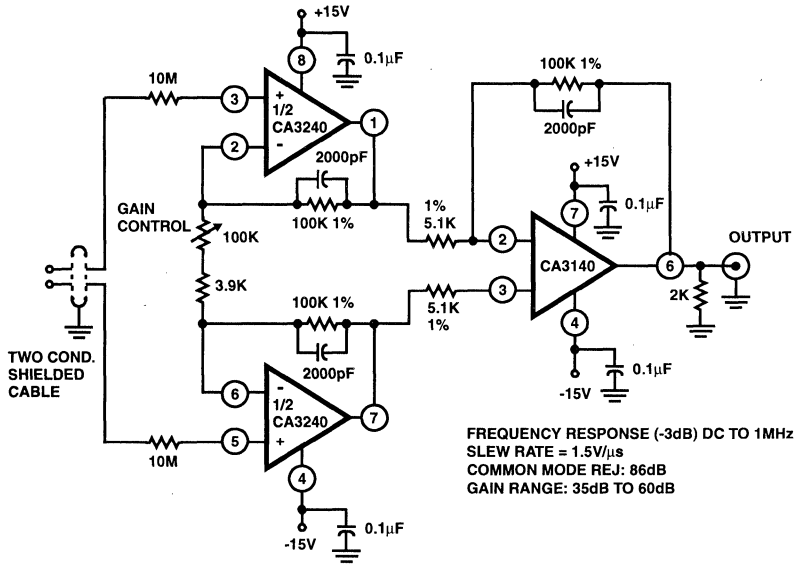
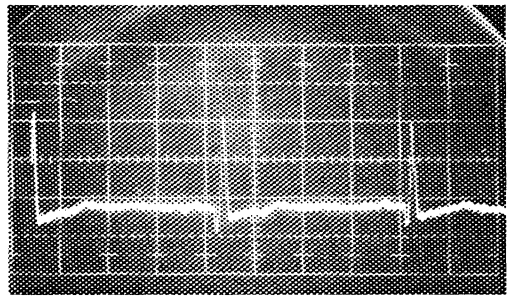


FIGURE 10. PRECISION DIFFERENTIAL AMPLIFIER



Vertical: 1.0mV/Div.
Amplifier Gain = 100X
Scope Sensitivity = 0.1V/Div.

Horizontal: >0.2s/Div. (Uncal)

FIGURE 11. TYPICAL ELECTROCARIOGRAM WAVEFORM

Differential Light Detector

In the circuit shown in Figure 12, the CA3240E converts the current from two photo diodes to voltage, and applies 1V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

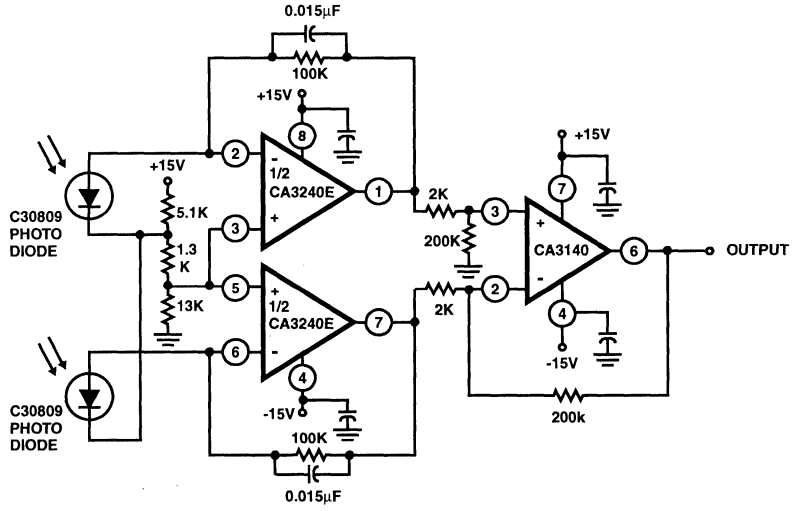


FIGURE 12. DIFFERENTIAL LIGHT DETECTOR

Typical Performance Curves

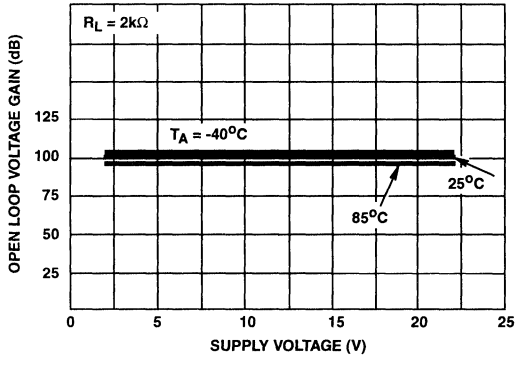


FIGURE 13. OPEN LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE

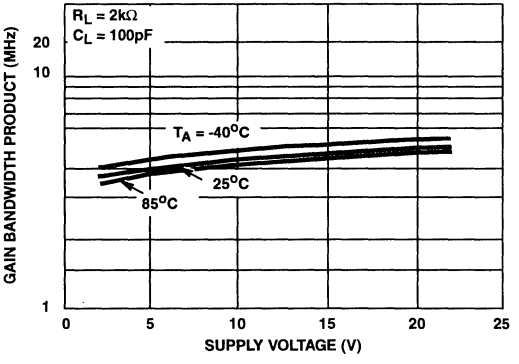


FIGURE 14. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

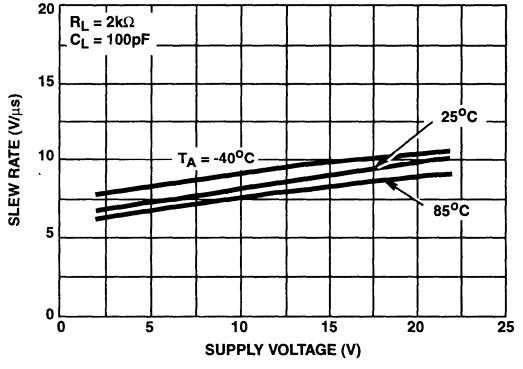


FIGURE 15. SLEW RATE vs SUPPLY VOLTAGE

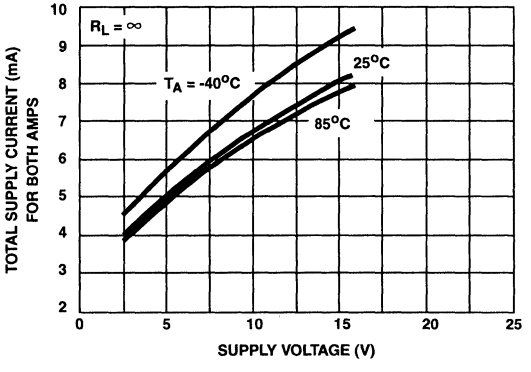


FIGURE 16. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

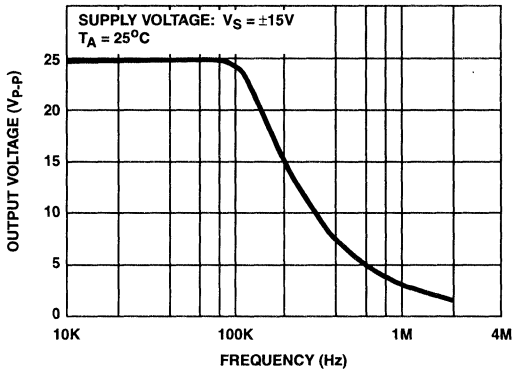


FIGURE 17. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

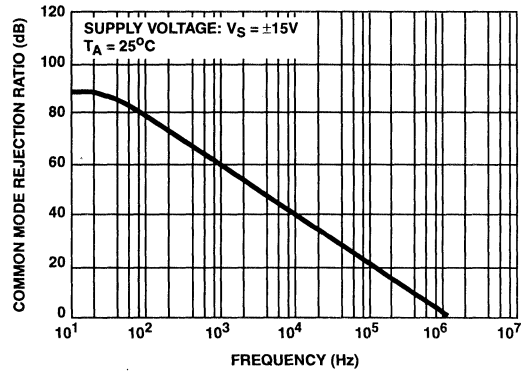


FIGURE 18. COMMON MODE REJECTION RATIO vs FREQUENCY

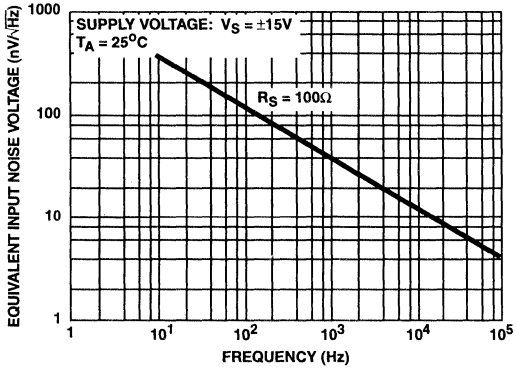


FIGURE 19. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

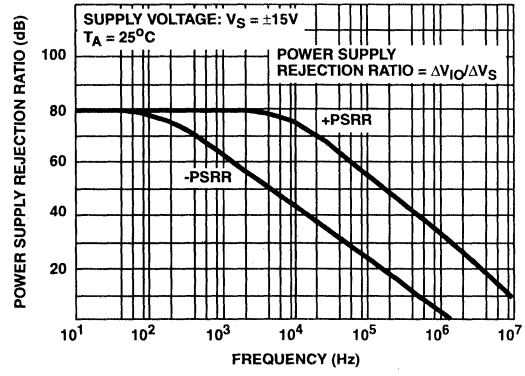


FIGURE 20. POWER SUPPLY REJECTION RATIO vs FREQUENCY

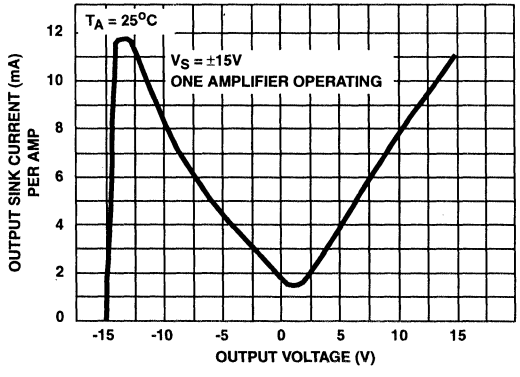


FIGURE 21. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

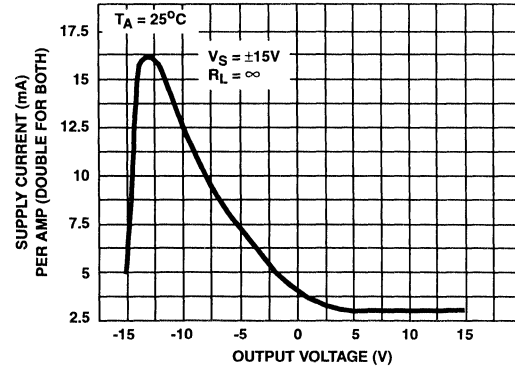


FIGURE 22. SUPPLY CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

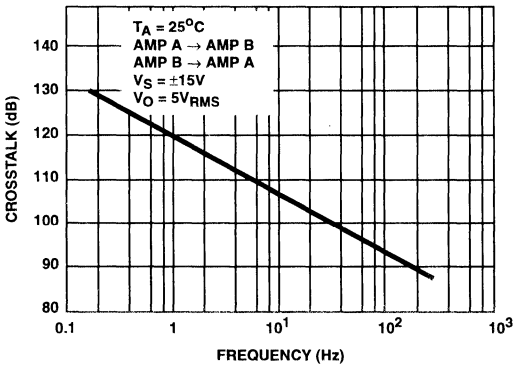


FIGURE 23. CROSSTALK vs FREQUENCY

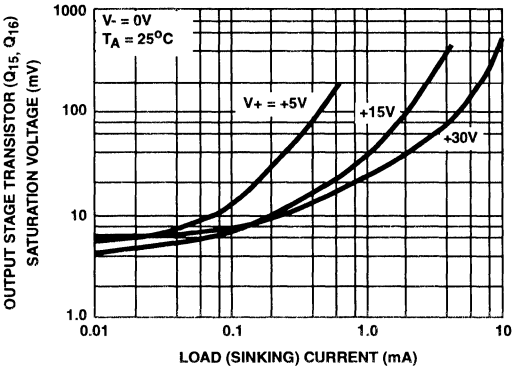


FIGURE 24. VOLTAGE ACROSS OUTPUT TRANSISTORS Q_{15} AND Q_{16} vs LOAD CURRENT

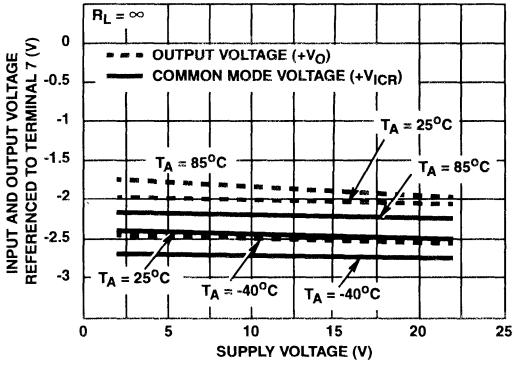


FIGURE 25A.

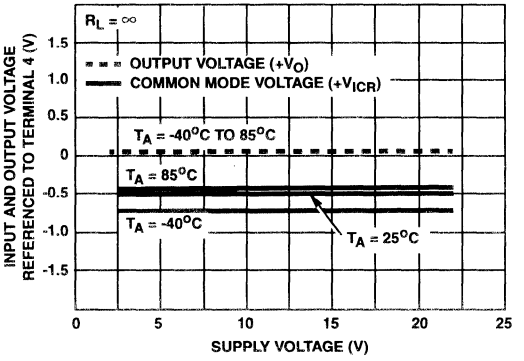


FIGURE 25B.

FIGURE 25. OUTPUT VOLTAGE SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

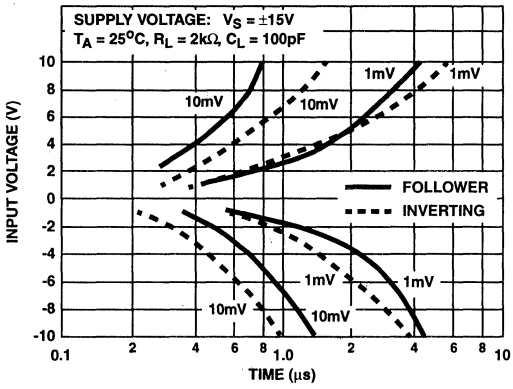


FIGURE 26A. SETTLING TIME vs INPUT VOLTAGE

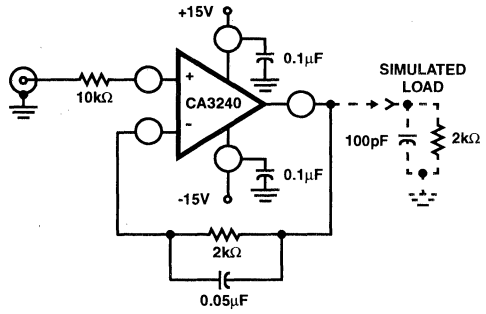


FIGURE 26B. TEST CIRCUIT (FOLLOWER)

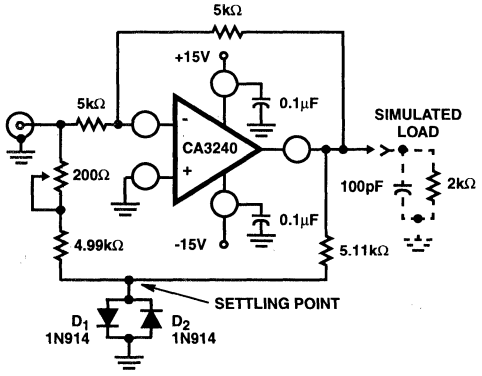


FIGURE 26C. TEST CIRCUIT (INVERTING)

FIGURE 26. INPUT VOLTAGE vs SETTLING TIME

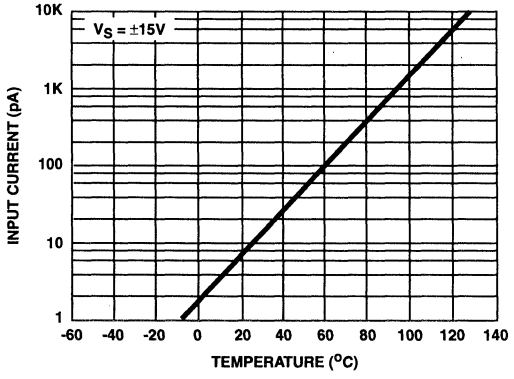


FIGURE 27. INPUT CURRENT vs TEMPERATURE

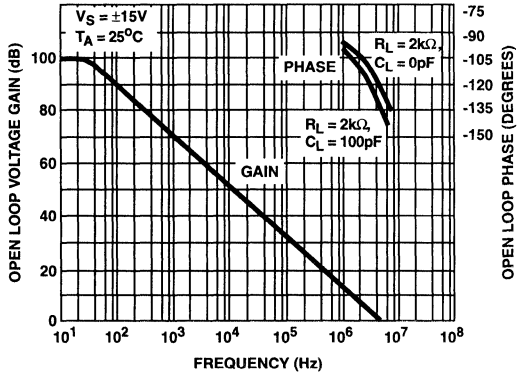


FIGURE 28. OPEN LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY

CA3260, CA3260A

4MHz, BiMOS Operational Amplifier with MOSFET Input/CMOS Output

November 1996

Features

- MOSFET Input Stage provides
  - Very High Z_I = 1.5TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I = 5pA (Typ) at 15V Operation
    = 2pA (Typ) at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (Or Both) Supply Rails

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface with Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Wien Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers

Description

CA3260A and CA3260 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

Gate protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

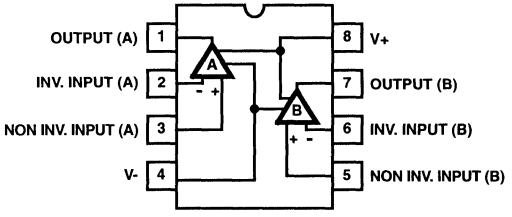
The CA3260 Series circuits operate at supply voltages ranging from 4V to 16V, or ±2V to ±8V when using split supplies. The CA3260A offers superior input characteristics over those of the CA3260.

Ordering Information

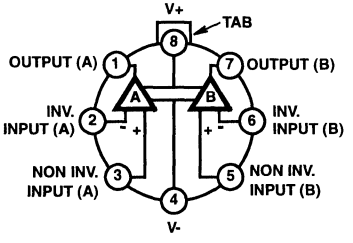
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3260E	-55 to 125	8 Ld PDIP	E8.3
CA3260T	-55 to 125	8 Pin Metal Can	T8.C
CA3260AE	-55 to 125	8 Ld PDIP	E8.3
CA3260AT	-55 to 125	8 Pin Metal Can	T8.C

Pinouts

CA3260, CA3260A (PDIP)
TOP VIEW



CA3260, CA3260A (METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number **1266.3**

Absolute Maximum Ratings

DC Supply Voltage (V+ to V-) 16V
DC Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Differential Input Voltage. 8V
Input Terminal Current 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . $-55^{o}C$ to $125^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
PDIP Package	100	N/A
Metal Can Package	165	75

Maximum Junction Temperature (Metal Can Package) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^{o}C$, Typical Values Intended Only for Design Guidance

PARAMETER		SYMBOL	TEST CONDITIONS	TYPICAL VALUES CA3260A	TYPICAL VALUES CA3260	UNITS
Input Resistance		R_I	$V_S = \pm 7.5V$	1.5	1.5	TΩ
Input Capacitance		C_I	f = 1MHz, $V_S = \pm 7.5V$	4.3	4.3	pF
Unity Gain Crossover Frequency		f_T	$V_S = \pm 7.5V$	4	4	MHz
Slew Rate		SR	$V_S = \pm 7.5V$	10	10	V/µs
Transient Response	Rise Time	t_r	C_L = 25pF, R_L = 2kΩ, A_V = +1, $V_S = \pm 7.5V$	0.09	0.09	µs
	Overshoot	OS		10	10	%
Settling Time (to <0.1%, $V_{IN} = 4V_{P-P}$)		t_S	C_L = 25pF, R_L = 2kΩ, A_V = +1, $V_S = \pm 7.5V$	1.8	1.8	µs
Input Offset Voltage		V_{IO}	V+ = 5V, V- = 0V	2	6	mV
Input Offset Current		I_{IO}	V+ = 5V, V- = 0V	0.1	0.1	pA
Input Current		I_I	V+ = 5V, V- = 0V	2	2	pA
Common Mode Rejection Ratio		CMRR	V+ = 5V, V- = 0V	70	60	dB
Large Signal Voltage Gain		A_{OL}	$V_O = 4V_{P-P}$, R_L = 20kΩ, V+ = 5V, V- = 0V	100	100	kV/V
				100	100	dB
Common Mode Input Voltage Range		V_{ICR}	V+ = 5V, V- = 0V	0 to 2.5	0 to 2.5	V
Supply Current		I+	V_O = 5V, $R_L = \infty$, V+ = 5V, V- = 0V	1	1	mA
			V_O = 2.5V, $R_L = \infty$, V+ = 5V, V- = 0V	1.2	1.2	mA
Power Supply Rejection Ratio		PSRR	$\Delta V_{IO}/\Delta V+$, V+ = 5V, V- = 0V	200	200	µV/V

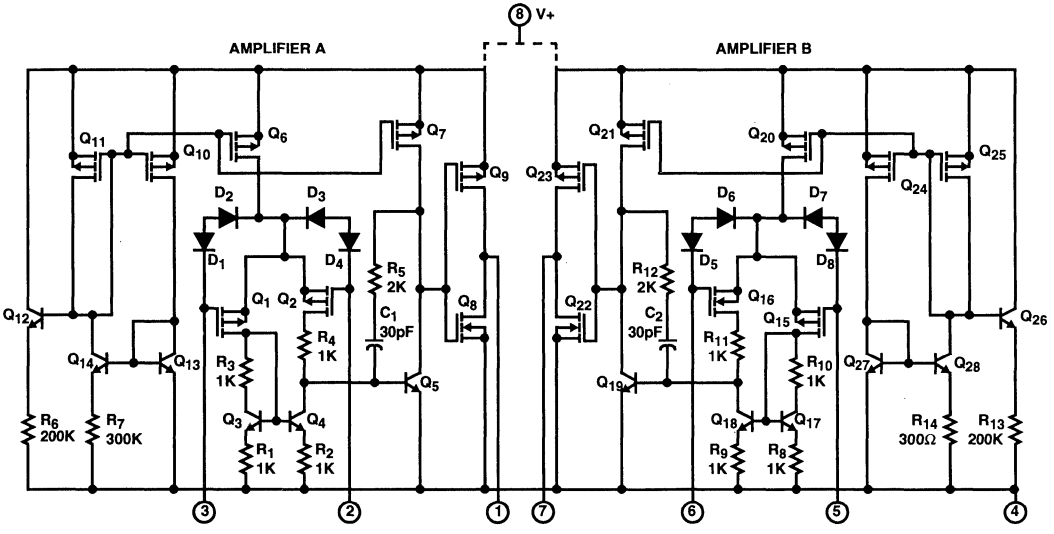
Electrical Specifications For Each Amplifier at $T_A = 25^{o}C$, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3260A MIN	CA3260A TYP	CA3260A MAX	CA3260 MIN	CA3260 TYP	CA3260 MAX	UNITS
Input Offset Voltage	$\lvert V_{IO} \rvert$	$V_S = \pm 7.5V$	-	2	5	-	6	15	mV
Input Offset Current	$\lvert I_{IO} \rvert$	$V_S = \pm 7.5V$	-	0.5	20	-	0.5	30	pA
Input Current	I_I	$V_S = \pm 7.5V$	-	5	30	-	5	50	pA
Large Signal Voltage Gain	A_{OL}	$V_O = 10V_{P-P}$, R_L = 10kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		80	95	-	70	90	-	dB

Electrical Specifications For Each Amplifier at $T_A = 25^oC$, V+ = 15V, V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA3260A			CA3260			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Common Mode Input Voltage Range	V_{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V+$ V+ = 17.5V	-	32	150	-	32	320	µV/V
Maximum Output Voltage	$V_{OM}+$	$R_L = 10k\Omega$	11	13.3	-	11	13.3	-	V
	$V_{OM}-$		-	0.002	0.01	-	0.002	0.01	V
	$V_{OM}+$	$R_L = \infty$	14.99	15	-	14.99	15	-	V
	$V_{OM}-$		-	0	0.01	-	0	0.01	V
Maximum Output Current	$I_{OM}+$ Source	$V_O = 7.5V$	12	22	45	12	22	45	mA
	$I_{OM}-$ Sink		12	20	45	12	20	45	mA
Total Supply Current	I+	$R_L = \infty$							
V_O (Amplifier A) = 7.5V V_O (Amplifier B) = 7.5V			-	9	15.5	-	9	15.5	mA
V_O (Amplifier A) = 0V V_O (Amplifier B) = 0V			-	1.2	3	-	1.2	3	mA
V_O (Amplifier A) = 0V V_O (Amplifier B) = 7.5V			-	5	8.5	-	5	8.5	mA
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	6	-	-	8	-	µV/°C
Crosstalk		f = 1kHz	-	120	-	-	120	-	dB

Schematic Diagram



CA3280, CA3280A

Dual, 9MHz, Operational Transconductance Amplifier (OTA)

November 1996

Features

- **Low Initial Input Offset Voltage: 500μV (Max) (CA3280A)**
- **Low Offset Voltage Change vs I_{ABC}: <500μV (Typ) for All Types**
- **Low Offset Voltage Drift: 5μV/°C (Max) (CA3280A)**
- **Excellent Matching of the Two Amplifiers for All Characteristics**
- **Internal Current-Driven Linearizing Diodes Reduce the External Input Current to an Offset Component**
- **Flexible Supply Voltage Range..... ±2V to ±15V**

Applications

- **Voltage Controlled Amplifiers**
- **Voltage Controlled Oscillators**
- **Multipliers**
- **Demodulators**
- **Sample and Hold**
- **Instrumentation Amplifiers**
- **Function Generators**
- **Triangle Wave-to-Sine Wave Converters**
- **Comparators**
- **Audio Preamplifier**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3280AE	-55 to 125	16 Ld PDIP	E16.3
CA3280E	0 to 70	16 Ld PDIP	E16.3
CA3280AF3	-55 to 125	16 Ld CERDIP	F16.3

Description

he CA3280 and CA3280A types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset voltage variation with respect to changes in programming current. This design results in reduced "AGC thump," an objectionable characteristic of many AGC systems. Interdigitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier except that the forward transfer characteristics is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced in 1969 (see Note 1), and it has since gained wide acceptance as a gateable, gain controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and high speed comparators.

For additional application information on this device and on OTAs in general, please refer to Application Notes: AN6818, AN6668, and AN6077.

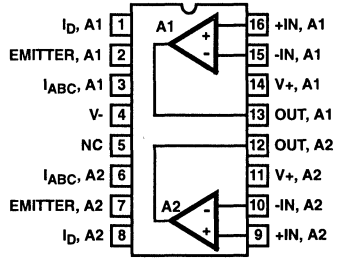
"OTA Obsoletes Op Amp", by C. F. Wheatley and H. A. Wittlinger, NEC Proceedings, December 1969.

NOTE:

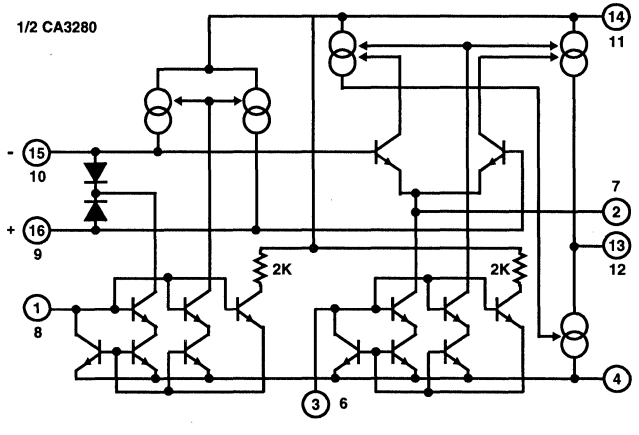
1. "OTA Obsoletes Op Amp", by C. F. Wheatley and H. A. Wittlinger, NEC Proceedings, December 1969

Pinout

CA3280
(PDIP, CERDIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1174.3**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V-) . . . . . +36V
Differential Input Voltage 5V
Input Voltage Range . . . . . V+ to V-
Input Current at $I_D = 0$ 100µA
Amplifier Bias Current (I_{ABC}) 10mA
Output Short Circuit Duration (Note 3) . . . . . Indefinite
Linearizing Diode Bias Current, I_D 5mA
Peak Input Current with Linearizing Diode . . . . . $\pm I_D$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	65	16
PDIP Package	100	N/A

Maximum Junction Temperature (CERDIP Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range
CA3280 . . . . . 0°C to 70°C
CA3280A . . . . . -55°C to 125°C
Supply Voltage Range (Typ) . . . . . ±2V to ±15V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Short circuit may be applied to ground or to either supply.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

For Equipment Design, at $T_A = 25°C$, $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		CA3280 MIN	CA3280 TYP	CA3280 MAX	CA3280A MIN	CA3280A TYP	CA3280A MAX	UNITS
Input Offset Voltage	V_{IO}	I_{ABC} = 1mA		-	-	3	-	-	0.5	mV
		I_{ABC} = 100µA		-	0.7	3	-	0.25	0.5	mV
		I_{ABC} = 10µA		-	-	3	-	-	0.5	mV
		I_{ABC} = 1mA to 10µA, T_A = Full Temp. Range		-	0.8	4	-	0.8	1.5	mV
Input Offset Voltage Drift	$\lvert\Delta V_{IO}\rvert$	I_{ABC} = 1µA to 1mA		-	0.5	1	-	0.5	1	mV
		I_{ABC} = 100µA, T_A = Full Temperature Range		-	5	-	-	3	5	µV/°C
Amplifier Bias Voltage	V_{ABC}	I_{ABC} = 100µA		-	1.2	-	-	1.2	-	V
Peak Output Voltage	V_{OM+}	IABC = 500mA		12	13.7	-	12.5	13.7	-	V
	V_{OM-}			12	-14.3	-	-13.3	-14.3	-	V
	V_{OM+}	I_{ABC} = 5µA		12	13.9	-	12.5	13.9	-	V
	V_{OM-}			12	-14.5	-	-13.5	-14.5	-	V
Common Mode Input Voltage Range	V_{ICR}	I_{ABC} = 100µA		-13	-	13	-13	-	13	V
Noise Voltage	e_N	I_{ABC} = 500µA	10Hz	-	20	-	-	20	-	nV/√Hz
			1kHz	-	8	-	-	8	-	nV/√Hz
			10kHz	-	7	-	-	7	-	nV/√Hz
Input Offset Current	I_{IO}	I_{ABC} = 500µA		-Z	0.3	0.7	-	0.3	0.7	µA
Input Bias Current	I_{IB}	I_{ABC} = 500µA		-	1.8	5	-	1.8	5	µA
		I_{ABC} = 500µA, T_A = Full Temperature Range		-	3	8	-	3	8	µA
Peak Output Current	I_{OM+}	I_{ABC} = 500µA	Source	350	410	650	350	410	650	µA
	I_{OM-}		Sink	-350	-410	-650	-350	-410	-650	µA
	I_{OM+}	I_{ABC} = 5µA	Source	3	4.1	7	3	4.1	7	µA
	I_{OM-}		Sink	-3	-4.1	-7	-3	-4.1	-7	µA

Electrical Specifications For Equipment Design, at $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA3280			CA3280A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Peak Output Current Sink and Source	I_{OM^-}, I_{OM+}	$I_{ABC} = 500\mu A$, T_A = Full Temperature Range	350	450	550	350	450	550	µA
Linearization Diodes		$I_D = 100\mu A$	-	10	-	-	10	-	µA
Offset Current		$I_D = 10\mu A$	-	0.5	1	-	0.5	1	µA
Dynamic Impedance		$I_D = 100\mu A$	-	700	-	-	700	-	Ω
Diode Network Supply Current		$I_{ABC} = 100\mu A$	250	400	800	250	400	800	µA
Amplifier Supply Current (Per Amplifier)	I+	$I_{ABC} = 500\mu A$	-	2	2.4	-	2	2.4	mA
Amplifier Output Leakage Current	I_{OL}	$I_{ABC} = 0$, $V_O = 0V$	-	0.015	0.1	-	0.015	0.1	nA
		$I_{ABC} = 0$, $V_O = 30V$	-	0.15	1	-	0.15	1	nA
Common Mode Rejection Ratio	CMRR	$I_{ABC} = 100\mu A$	80	100	-	94	100	-	dB
Power Supply Rejection Ratio	PSRR	$I_{ABC} = 100\mu A$	86	105	-	94	105	-	dB
Open Loop Voltage Gain	A_{OL}	$I_{ABC} = 100\mu A$, $R_L = \infty$ $V_O = 20V_{P-P}$	94	100	-	94	100	-	dB
			50	100	-	50	100	-	kV/V
Forward Transconductance	G_M	$I_{ABC} = 50\mu A$, Large Signal	-	0.8	1.2	-	0.8	1.2	mS
	g_M	$I_{ABC} = 1mA$, Small Signal	-	16	22	-	16	22	mS
Input Resistance	R_I	$I_{ABC} = 10\mu A$	0.5	-	-	0.5	-	-	MΩ
Channel Separation		f = 1kHz	-	94	-	-	94	-	dB
Open Loop Total Harmonic Distortion	THD	f = 1kHz, $I_{ABC} = 1.5mA$, $R_L = 15k\Omega$, $V_O = 20V_{P-P}$	-	0.4	-	-	0.4	-	%
Bandwidth	f_T	$I_{ABC} = 1mA$, $R_L = 100\Omega$	-	9	-	-	9	-	MHz
Slew Rate, Open Loop	SR	$I_{ABC} = 1mA$	-	125	-	-	125	-	V/µs
Capacitance	C_I	$I_{ABC} = 100\mu A$ Input	-	4.5	-	-	4.5	-	pF
	C_O	Output	-	7.5	-	-	7.5	-	pF
Output Resistance	R_O	$I_{ABC} = 100\mu A$	-	63	-	-	63	-	MΩ

Test Circuits and Waveforms

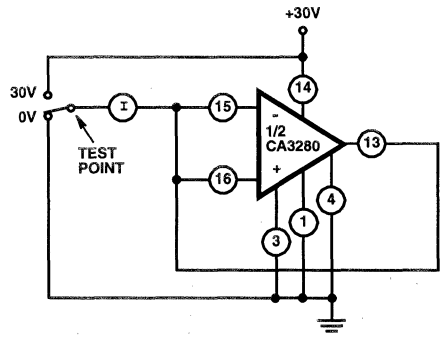


FIGURE 1. LEAKAGE CURRENT TEST CIRCUIT

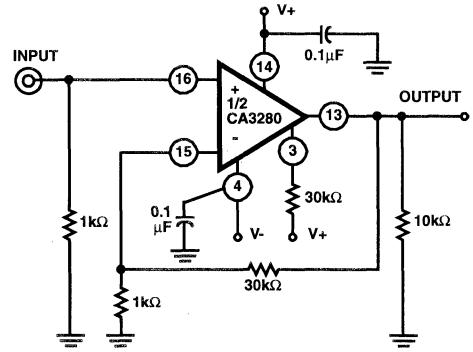
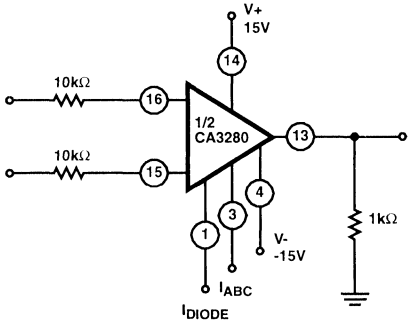
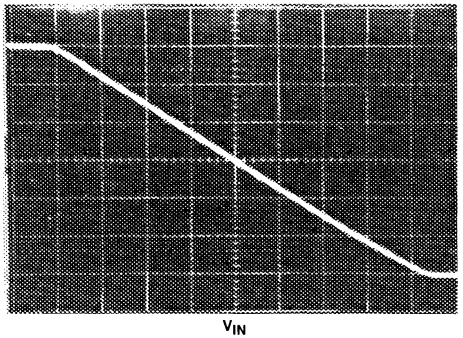


FIGURE 2. CHANNEL SEPARATION TEST CIRCUIT

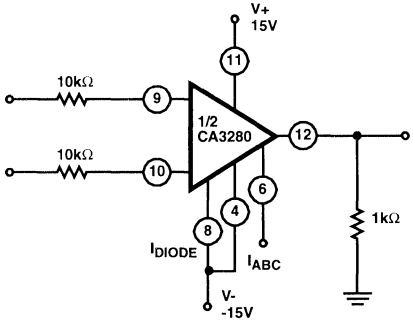
Test Circuits and Waveforms (Continued)

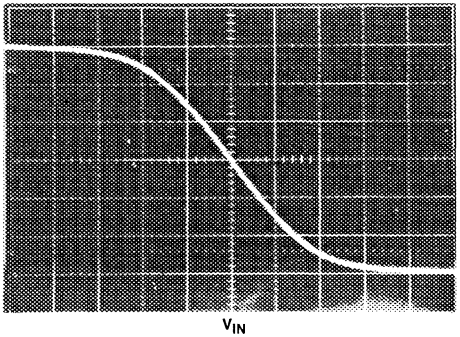




I_{ABC} = 650µA, I_D = 200µA; Vertical = 200µA/Div.; Horizontal = 1V/Div.

FIGURE 3A. EFFECTS OF DIODE LINEARIZATION, WITH DIODE PROGRAMMING TERMINAL ACTIVE





I_{ABC} = 650µA; I_D = 0; Vertical = 200µA/Div.; Horizontal = 25mV/Div.

FIGURE 3B. WITH DIODE PROGRAMMING TERMINAL CUTOFF

FIGURE 3. CA3280 TRANSFER CHARACTERISTICS

Application Information

Figures 4 and 5 show the equivalent circuits for the current source and linearization diodes in the CA3280. The current through the linearization network is approximately equal to the programming current. There are several advantages to driving these diodes with a current source. First, only the offset current from the biasing network flows through the input resistor. Second, another input is provided to extend the gain control dynamic range. And third, the input is truly differential and can accept signals within the common mode range of the CA3280.

Typical Applications

The structure of the variable operational amplifier eliminates the need for matched resistor networks in differential to single ended converters, as shown in Figure 6. A matched resistor network requires ratio matching of 0.01% or trimming for 80dB of common-mode rejection. The CA3280, with its excellent common mode rejection ratio, is capable of converting a small (±25mV) differential input signal to a single-ended output without the need for a matched resistor network.

Figure 7 shows the CA3280 in a typical gain control application. Gain control can be performed with the amplifier bias current (I_{ABC}). With no diode bias current, the gain is merely $g_M R_L$. For example, with an I_{ABC} of 1mA, the g_M is approximately 16mS. With the CA3280 operating into a 5kΩ resistor, the gain is 80.

The need for external buffers can be eliminated by the use of low value load resistors, but the resulting increase in the required amplifier bias current reduces the input impedance of the CA3280. The linearization diode impedance also decreases as the diode bias current increases, which further loads the input. The diodes, in addition to acting as a linearization network, also operate as an additional attenuation system to accommodate input signals in the volt range when they are applied through appropriate input resistors.

Figure 10 shows a triangle wave to sine wave converter using the CA3280. Two 100kΩ resistors are connected between the differential amplifier emitters and V+ to reduce the current flow through the differential amplifier. This allows the amplifier to fully cut off during peak input signal excursions. THD is appropriately 0.37% for this circuit.

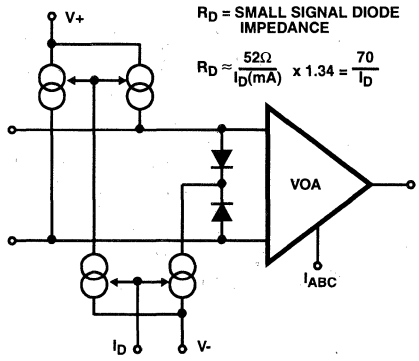


FIGURE 4. VOA SHOWING LINEARIZATION DIODES AND CURRENT DRIVE

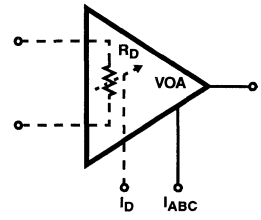


FIGURE 5. BLOCK DIAGRAM OF LINEARIZED VOA

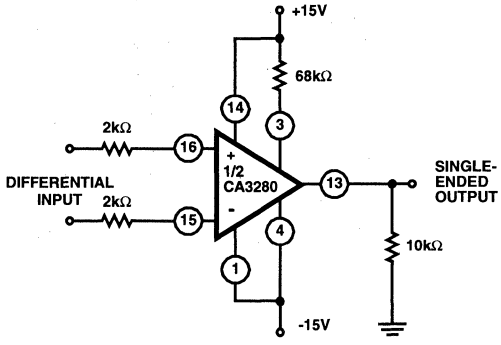


FIGURE 6. DIFFERENTIAL TO SINGLE ENDED CONVERTER

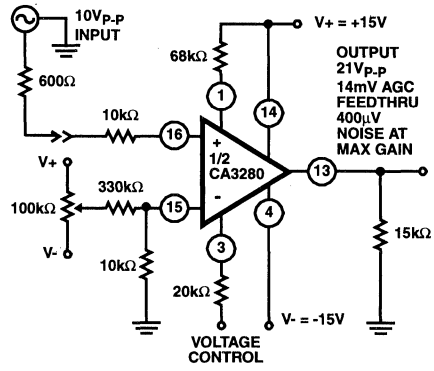
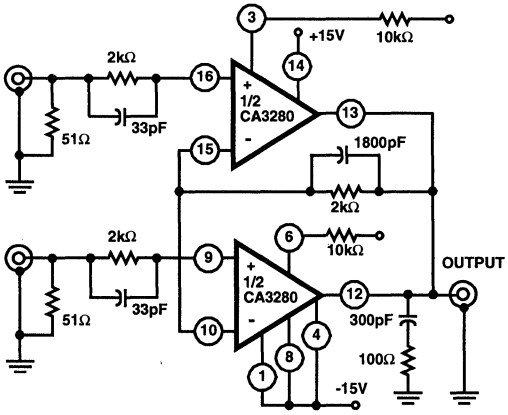


FIGURE 7. TYPICAL GAIN CONTROL CIRCUIT



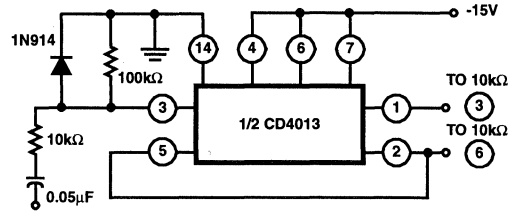


FIGURE 8. TWO CHANNEL LINEAR MULTIPLEXER

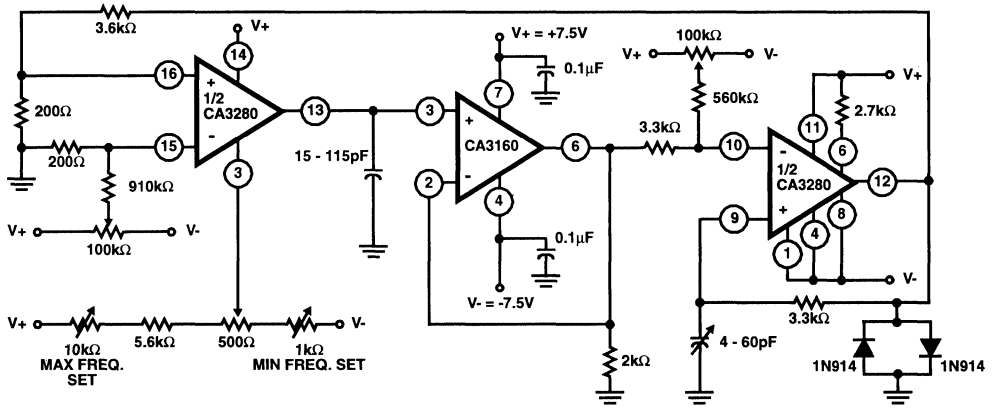


FIGURE 9. CA3280 USED IN CONJUNCTION WITH A CA3160 TO PROVIDE A FUNCTION GENERATOR WITH A TUNABLE RANGE OF 2Hz TO 1MHz

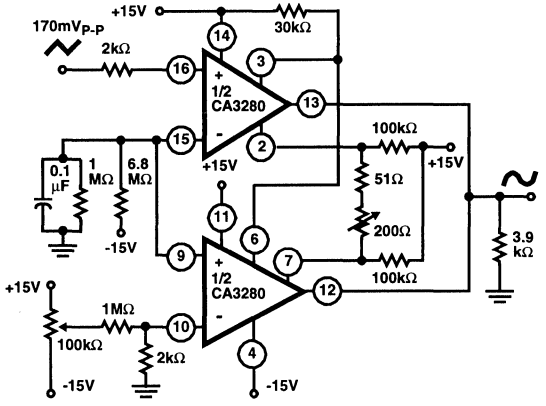


FIGURE 10. TRIANGLE WAVE-TO-SINE WAVE CONVERTER

Typical Performance Curves

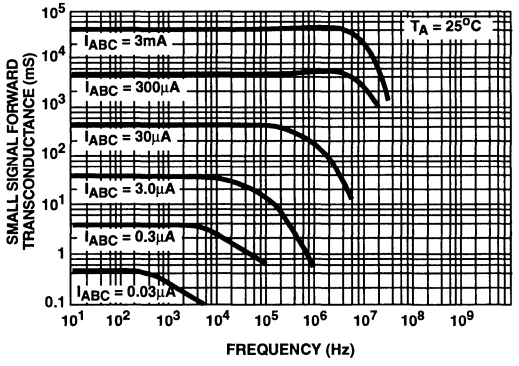


FIGURE 11. AMPLIFIER GAIN vs FREQUENCY

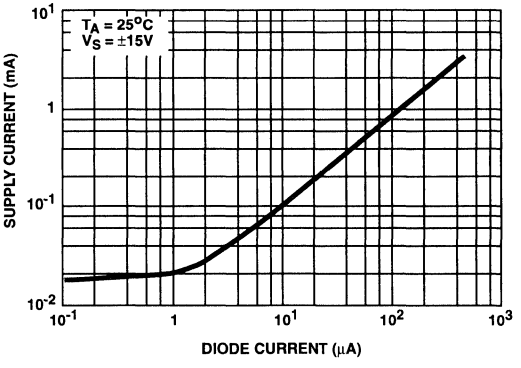


FIGURE 12. SUPPLY CURRENT vs DIODE CURRENT

Typical Performance Curves (Continued)

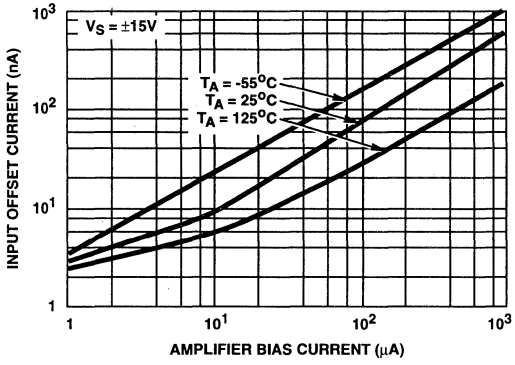


FIGURE 13. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT

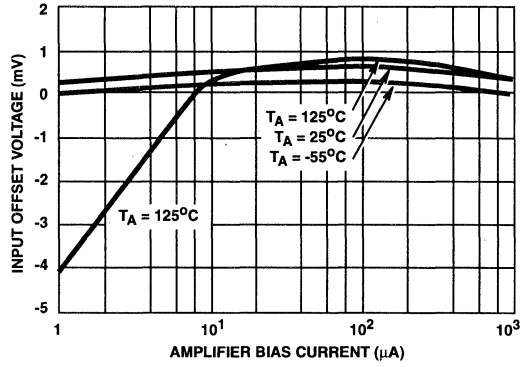


FIGURE 14. INPUT OFFSET VOLTAGE vs AMPLIFIER BIAS CURRENT

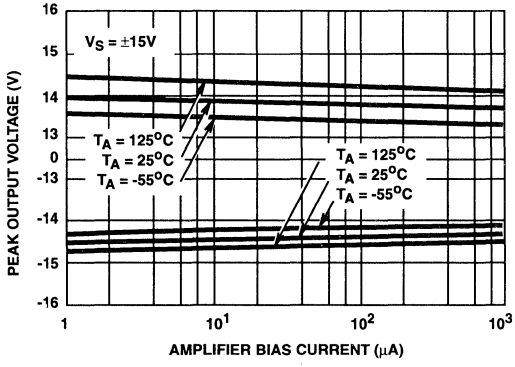


FIGURE 15. PEAK OUTPUT VOLTAGE vs AMPLIFIER BIAS CURRENT

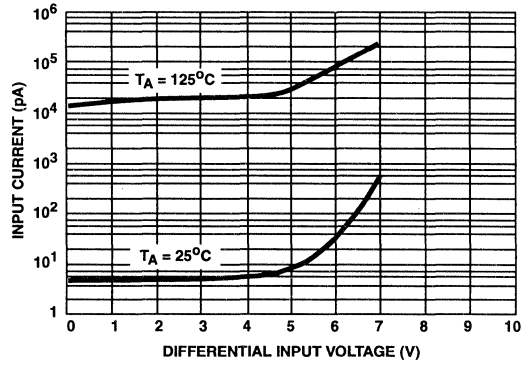


FIGURE 16. INPUT CURRENT vs INPUT DIFFERENTIAL VOLTAGE

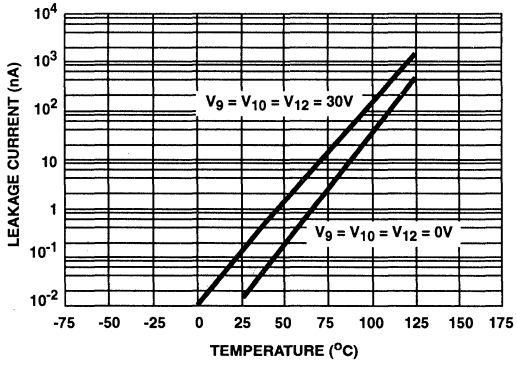


FIGURE 17. LEAKAGE CURRENT vs TEMPERATURE

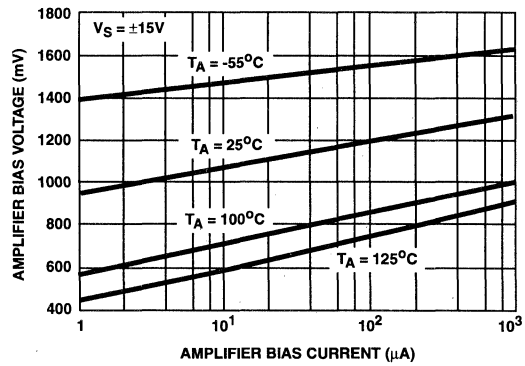


FIGURE 18. AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT

Typical Performance Curves (Continued)

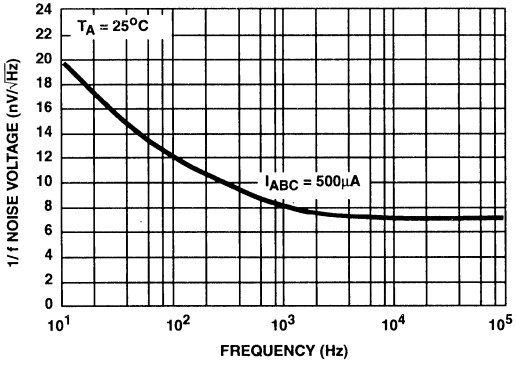


FIGURE 19. 1/f NOISE vs FREQUENCY

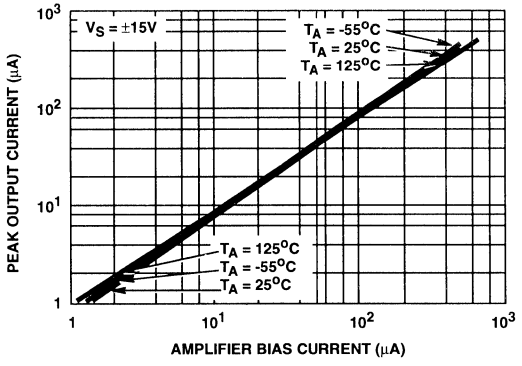


FIGURE 20. PEAK OUTPUT CURRENT vs AMPLIFIER BIAS CURRENT

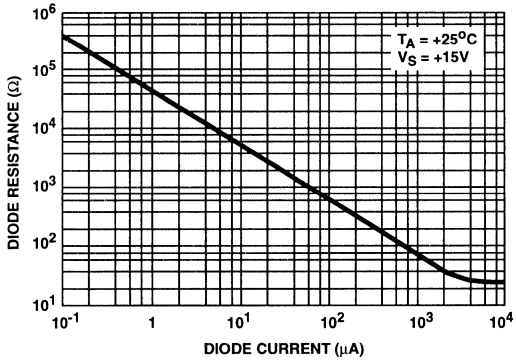


FIGURE 21. DIODE RESISTANCE vs DIODE CURRENT

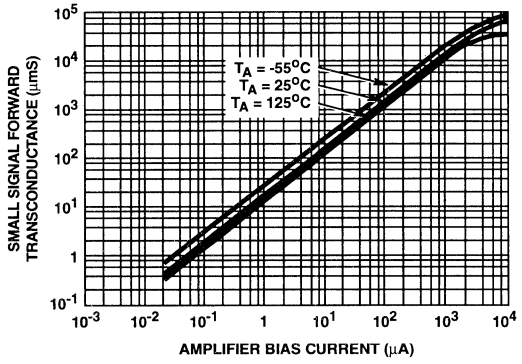


FIGURE 22. AMPLIFIER GAIN vs AMPLIFIER BIAS CURRENT

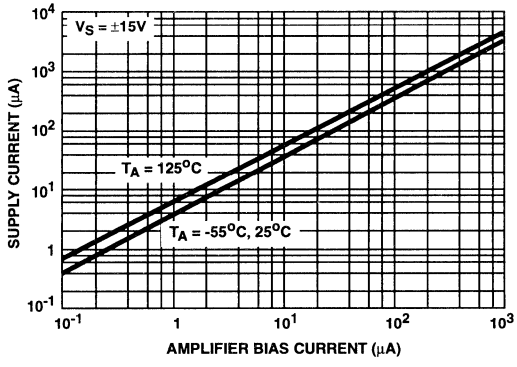


FIGURE 23. SUPPLY CURRENT vs AMPLIFIER BIAS CURRENT

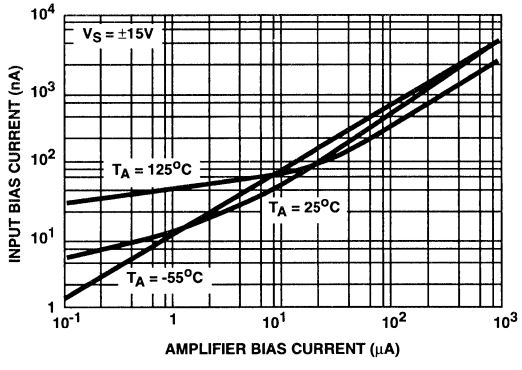
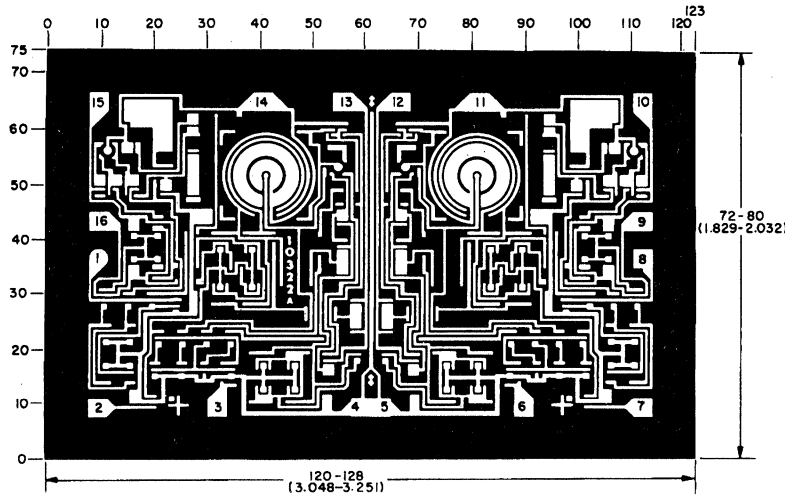


FIGURE 24. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT

3 OPERATIONAL AMPLIFIERS

Metallization Mask Layout



Dimensions in parentheses are in millimeters and derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

CA3420, CA3420A

NOT RECOMMENDED FOR NEW DESIGN
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section

November 1996

0.5MHz, Low Supply Voltage, Low Input Current BiMOS Operational Amplifiers

Features

- 2V Supply at 300μA Supply Current
- 1pA Input Current (Typ) (Essentially Constant to 85°C)
- Rail-to-Rail Output Swing (Drive ±2mA into 1kΩ Load)
- Pin Compatible with 741 Operational Amplifiers

Applications

- pH Probe Amplifiers
- Picoammeters
- Electrometer (High Z) Instruments
- Portable Equipment
- Inaccessible Field Equipment
- Battery-Dependent Equipment (Medical and Military)

Ordering Information

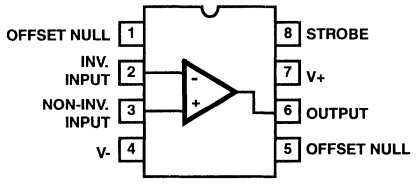
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3420AE	-55 to 125	8 Ld PDIP	E8.3
CA3420AT	-55 to 125	8 Pin Metal Can	T8.C
CA3420E	-55 to 125	8 Ld PDIP	E8.3
CA3420T	-55 to 125	8 Pin Metal Can	T8.C

Description

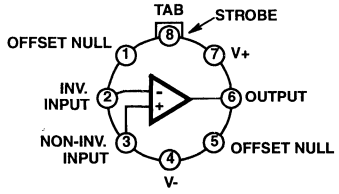
The CA3420A and CA3420 are integrated circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. The CA3420A and CA3420 BiMOS operational amplifiers feature gate protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10°C increase in temperature. The CA3420 series operates at total supply voltages from 2V to 20V either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common mode input voltage capability down to 0.45V below the negative supply terminal, an important attribute for single supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.5mA (Min) is provided by using nonlinear current mirrors.

Pinouts

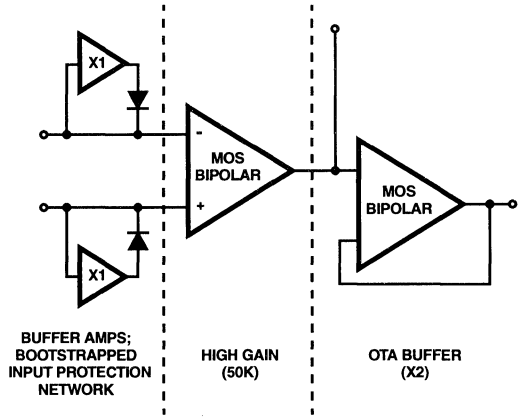
CA3420 (PDIP)
TOP VIEW



CA3420 (METAL CAN)
TOP VIEW



Functional Diagram



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or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

CA3440, CA3440A

63kHz, Nanopower, BiMOS Operational Amplifiers

November 1996

Features

- **High Input Resistance . . . . . 2TΩ (Typ)**
- **Standby Power at V+ = 5V . . . . . 300nW (Typ)**
- **Supply Current, BW, Slew Rate Programmable Using External Resistor**
- **Input Current . . . . . 10pA (Typ)**
- **5V to 15V Supply**
- **Output Drives Typical Bipolar Type Loads**

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3440AE	-55 to 125	8 Ld PDIP	E8.3
CA3440E	-55 to 125	8 Ld PDIP	E8.3
CA3440M (3440)	-55 to 125	8 Ld SOIC	M8.15

Description

The CA3440A and CA3440 (see Note) are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

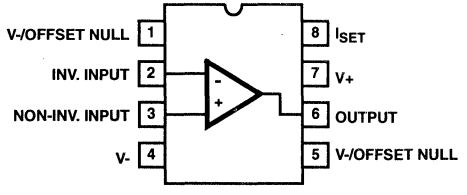
The CA3440A and CA3440 BiMOS op amps feature gate protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 10pA). These devices operate at total supply voltage from 5V to 15V and can be operated over the temperature range from -55^{o}C to 125^{o}C. Their virtues are programmability and very low standby power consumption (300nW). These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminals, an important attribute for single supply applications. The output stage uses MOS complementary source follower form which permits moderate load driving capability (10kΩ) at very low standby currents (50nA).

The CA3440A and CA3440 have the same 8 pin terminal pinout as the "741" and other industry standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

NOTE: Formerly Developmental Type No. TA10590.

Pinout

CA3440, CA3440A
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1318.3**

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A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

CA3450

220MHz, Video Line Driver, High Speed Operational Amplifier

November 1996

Features

- High Open Loop Gain at Video Frequencies
  - A_{OL} .....>40dB at f = 5MHz
- Power Bandwidth of 10MHz ..... A_{CL} = 5; V_O = ±3.5V
- Slew Rate at Full Load..... 330V/µs ($A_V \geq 10$)
- f_T = 220MHz; C_C = 0pF With a Load of 50Ω ll20pFll 1MΩ (Scope Input)
- V_{OUT} = ±4.1V Into 75Ω
- Offset Null Terminals

Applications

- Video Line Driver
- High Frequency Unity Gain Buffer
- Pulse Amplifier
- High Speed Comparator
- High Frequency Oscillator and Video Amplifiers
- Driver for A/Ds in Video Applications .....10MHz BW

Description

The CA3450 (see Note) is a large signal video line driver and high speed operational amplifier capable of driving 50Ω transmission lines and flash A/Ds. The uncompensated unity gain crossing occurs at 230MHz without load. It can operate at dual or single supplies of ±7.25V or 14.5V, respectively. The CA3450 can be compensated with a single capacitor network. It has output drive capability of 75mA SINK or SOURCE. The CA3450 is capable of driving Flash A/Ds in video or high speed instrumentation (accurate) applications with bandwidth up to 10MHz. Offset voltage nulling terminals are also available.

NOTE: Formerly Developmental Type No. TA11371A.

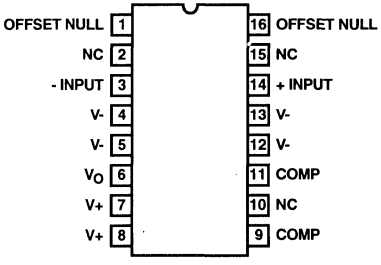
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3450E	-40 to 85	16 Ld PDIP	E16.3

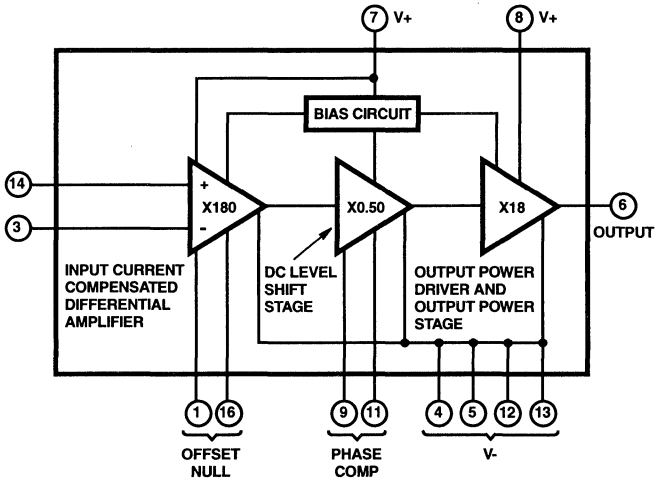
3 OPERATIONAL AMPLIFIERS

Pinout

CA3450
(PDIP)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1732.3**

NOT RECOMMENDED FOR NEW DESIGN
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

CA5130, CA5130A

November 1996

15MHz, BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output

Features

- MOSFET Input Stage
  - Very High Z_I . . . . . 1.5TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I . . . . . 5pA (Typ) at 15V Operation
    2pA (Typ) at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can Be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5130A, CA5130 Have Full Military Temperature Range Guaranteed Specifications for V+ = 5V
- CA5130A, CA5130 Are Guaranteed to Operate Down to V+ = 4.5V for A_{OL}
- CA5130A, CA5130 Are Guaranteed to Operate at ±7.5V CA3130A, CA3130 Specifications

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- High Input Impedance Comparators (Ideal Interface with Digital CMOS)
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g., Follower for Single-Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Peak Detectors
- Single Supply Full Wave Precision Rectifiers
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

Description

CA5130A and CA5130 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. They are designed and guaranteed to operate in microprocessors or logic systems that use +5V supplies.

Gate protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5130 Series circuits operate at supply voltages ranging from 4V to 16V, or ±2V to ±8V when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset null capability. Terminal provisions are also made to permit strobing of the output stage.

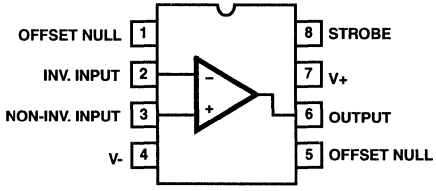
The CA5130A, CA5130 have guaranteed specifications for 5V operation over the full military temperature range of -55°C to 125°C.

Ordering Information

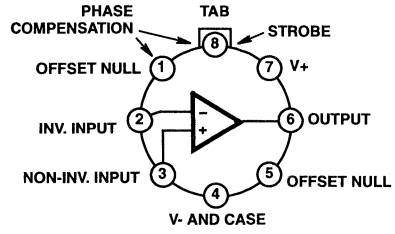
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA5130AE	-55 to 125	8 Ld PDIP	E8.3
CA5130AM (5130A)	-55 to 125	8 Ld SOIC	M8.15
CA5130AT	-55 to 125	8 Pin Metal Can	T8.C
CA5130E	-55 to 125	8 Ld PDIP	E8.3
CA5130M (5130)	-55 to 125	8 Ld SOIC	M8.15
CA5130T	-55 to 125	8 Pin Metal Can	T8.C

Pinouts

CA5130 (PDIP, SOIC)
TOP VIEW



CA5130 (METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1923.3**

CA5160, CA5160A

NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris Home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 10

4MHz, BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output

November 1996

Features

- MOSFET Input Stage
  - Very High Z_I; 1.5TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I; 5pA (Typ) at 15V Operation
    2pA (Typ) at 5V Operation
- Common-Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5160A, CA5160 Have Full Military Temperature Range Guaranteed Specifications for V+ = 5V
- CA5160A, CA5160 Are Guaranteed to Operate Down to 4.5V for A_{OL}
- CA5160A, CA5160 Are Guaranteed Up to ±7.5V

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface With Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g., Follower for Single Supply D/A Converter)
- Wien-Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

Description

CA5160A and CA5160 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5160 series circuits are frequency compensated versions of the popular CA5130 series. They are designed and guaranteed to operate in microprocessor or logic systems that use +5V supplies.

Gate-protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common-mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

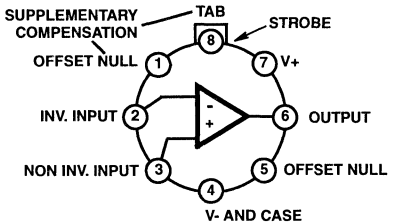
The CA5160 Series circuits operate at supply voltages ranging from +5V to +16V, or ±2.5V to ±8V when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage. They have guaranteed specifications for 5V operation over the full military temperature range of -55°C to 125°C.

Ordering Information

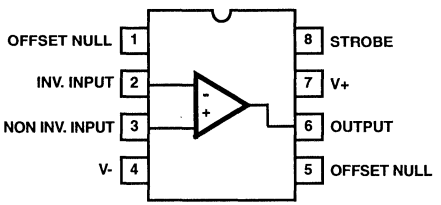
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA5160AE	-55 to 125	8 Ld PDIP	E8.3
CA5160AM (5160A)	-55 to 125	8 Ld SOIC	M8.15
CA5160M (5160)	-55 to 125	8 Ld SOIC	M8.15
CA5160E	-55 to 125	8 Ld PDIP	E8.3
CA5160T	-55 to 125	8 Pin Metal Can	T8.C

Pinouts

CA5160 (METAL CAN)
TOP VIEW



CA5160A, CA5160 (PDIP, SOIC)
TOP VIEW



NOTE: CA5160 Series devices have an on-chip frequency compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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HARRIS SEMICONDUCTOR

CA5260, CA5260A

3MHz, BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output

November 1996

Features

- MOSFET Input Stage provides
  - Very High Z_I = 1.5TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I = 5pA (Typ) at 15V Operation
    = 2pA (Typ) at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5260A, CA5260 Have Full Military Temperature Range Guaranteed Specifications for V+ = 5V
- CA5260A, CA5260 are Guaranteed to Operate Down to 4.5V for A_{OL}
- Fully Guaranteed to Operate from -55°C to 125°C at V+ = 5V, V- = GND

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface with Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g., Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Wien Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

Description

The CA5260A and CA5260 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5260 series circuits are dual versions of the popular CA5160 series. They are designed and guaranteed to operate in microprocessor or logic systems that use +5V supplies.

Gate-protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5V below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5260 Series circuits operate at supply voltages ranging from 4.5V to 16V, or ±2.25V to ±8V when using split supplies.

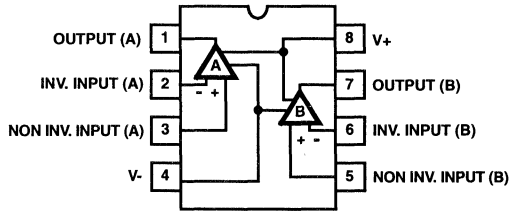
The CA5260, CA5260A have guaranteed specifications for 5V operation over the full military temperature range of -55°C to 125°C.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA5260AE	-55 to 125	8 Ld PDIP	E8.3
CA5260AM (5260A)	-55 to 125	8 Ld SOIC	M8.15
CA5260AM96 (5260A)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA5260E	-55 to 125	8 Ld PDIP	E8.3
CA5260M (5260)	-55 to 125	8 Ld SOIC	M8.15
CA5260M96 (5260)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15

Pinout

CA5260 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1929.3**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 16V
Differential Input Voltage 8V
Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . $-55^{o}C$ to $125^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
PDIP Package	96
SOIC Package	157
Maximum Junction Temperature (Die)	$175^{o}C$
Maximum Junction Temperature (Plastic Package)	$150^{o}C$
Maximum Storage Temperature Range	$-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	$300^{o}C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Typical Values Intended Only for Design Guidance, V+ = 5V, V- = 0V, $T_A = 25^{o}C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES CA5260	TYPICAL VALUES CA5260A	UNITS
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	4.3	pF
Unity Gain Crossover Frequency	f_T		3	3	MHz
Slew Rate	SR	$V_{OUT} = 2.5V_{P-P}$	5	5	V/μs
Transient Response Rise Time	t_r	$C_L = 25pF$, $R_L = 2k\Omega$ (Voltage Follower)	0.09	0.09	μs
Overshoot	OS		10	10	%
Settling Time (To <0.1%, $V_{IN} = 4V_{P-P}$)	t_S	$C_L = 25pF$, $R_L = 2k\Omega$ (Voltage Follower)	1.8	1.8	μs

Electrical Specifications

$T_A = 25^{o}C$, V+ = 5V, V- = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260 MIN	CA5260 TYP	CA5260 MAX	CA5260A MIN	CA5260A TYP	CA5260A MAX	UNITS
Input Offset Voltage	V_{IO}	$V_O = 2.5V$	-	2	15	-	1.5	4	mV
Input Offset Current	I_{IO}	$V_O = 2.5V$	-	1	10	-	1	10	pA
Input Current	I_I	$V_O = 2.5V$	-	2	15	-	2	15	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 1V	70	85	-	80	85	-	dB
		V_{CM} = 0 to 2.5V	50	55	-	50	55	-	dB
Common Mode Input Voltage Range	V_{ICR+}		2.5	3	-	2.5	3	-	V
	V_{ICR-}		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	70	84	-	75	84	-	dB
Large Signal Voltage Gain (Note 3)	A_{OL}	$R_L = \infty$, V_O = 0.5 to 4V	105	111	-	107	113	-	dB
		$R_L = 10k\Omega$, V_O = 0.5 to 3.6V	80	86	-	83	86	-	dB
Source Current	I_{SOURCE}	$V_O = 0V$	1.75	2.2	-	1.75	2.2	-	mA
Sink Current	I_{SINK}	$V_O = 5V$	1.70	2	-	1.70	2	-	mA
Output Voltage	V_{OM+}	$R_L = \infty$	4.99	5	-	4.99	5	-	V
	V_{OM-}		-	0	0.01	-	0	0.01	V
	V_{OM+}	$R_L = 10k\Omega$	4.4	4.7	-	4.4	4.7	-	V
	V_{OM-}		-	0	0.01	-	0	0.01	V
	V_{OM+}	$R_L = 2k\Omega$	3	3.4	-	3	3.4	-	V
	V_{OM-}		-	0	0.01	-	0	0.01	V

Electrical Specifications $T_A = 25^oC$, V+ = 5V, V- = 0V **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I_{SUPPLY}	V_O = 0V	-	1.60	2.0	-	1.60	2.0	mA
		V_O = 2.5V	-	1.80	2.25	-	1.80	2.25	mA

NOTE:

3. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ.

Electrical Specifications $T_A = -55^oC$ to 125^oC, V+ = 5V, V- = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	3	20	-	2	15	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	1	10	-	1	10	nA
Input Current	I_I	V_O = 2.5V	-	2	15	-	2	15	nA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 1V	60	78	-	65	78	-	dB
		V_{CM} = 0 to 2.5V	50	60	-	50	60	-	dB
Common Mode Input Voltage Range	V_{ICR}+		2.5	3	-	2.5	3	-	V
	V_{ICR}-		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	60	65	-	62	65	-	dB
Large Signal Voltage Gain (Note 4)	A_{OL}	$R_L = \infty$, V_O = 0.5 to 4V	70	78	-	70	78	-	dB
		R_L = 10kΩ, V_O = 0.5 to 3.6V	60	65	-	60	65	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1.3	1.6	-	1.3	1.6	-	mA
Sink Current	I_{SINK}	V_O = 5V	1.2	1.4	-	1.2	1.4	-	mA
Output Voltage	V_{OM}+	$R_L = \infty$	4.99	5	-	4.99	5	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
	V_{OM}+	R_L = 10kΩ	4.2	4.4	-	4.2	4.4	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
	V_{OM}+	R_L = 2kΩ	2.5	2.7	-	2.5	2.7	-	V
	V_{OM}-		-	0	0.01	-	0	0.01	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	1.65	2.2	-	1.65	2.2	mA
		V_O = 2.5V	-	1.95	2.35	-	1.95	2.35	mA

NOTE:

4. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ.

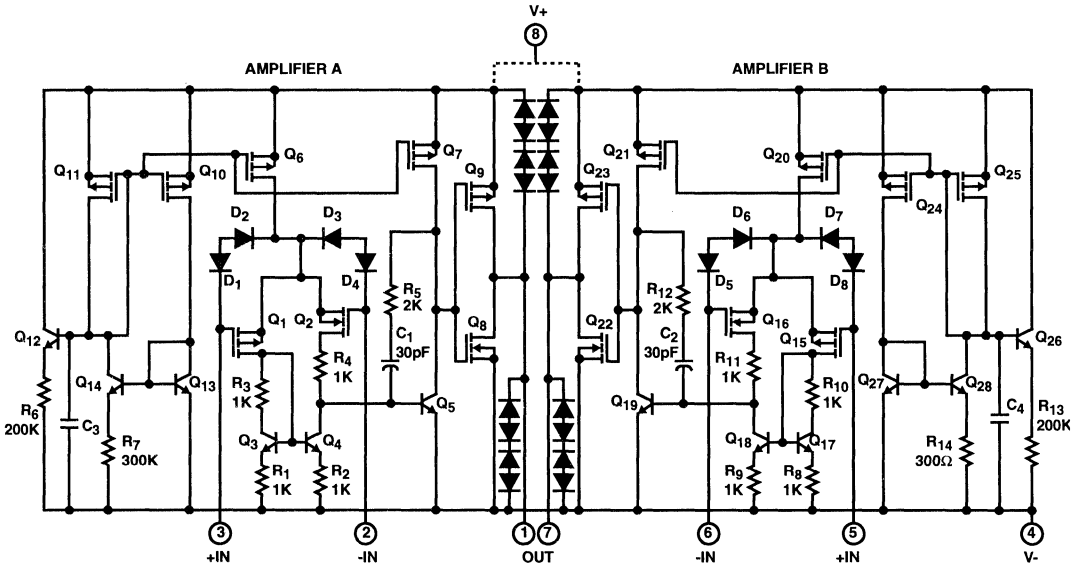
Electrical Specifications Each Amplifier at $T_A = 25^oC$, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_S = ±7.5	-	6	15	-	2	5	mV
Input Offset Current	I_{IO}	V_S = ±7.5	-	0.5	30	-	0.5	20	pA
Input Current	I_I	V_S = ±7.5	-	5	50	-	5	30	pA
Large Signal Voltage Gain	A_{OL}	$V_O = 10V_{P-P}$, R_L = 10kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		70	90	-	80	95	-	dB

Electrical Specifications Each Amplifier at $T_A = 25^oC$, V+ = 15V, V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Common Mode Input Voltage Range	V_{ICR}		10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V\pm$	PSRR	$V_S = \pm 7.5$	-	32	320	-	32	150	µV/V
Maximum Output Voltage	$V_{OM}+$	$R_L = 10k\Omega$	11	13.3	-	11	13.3	-	V
	$V_{OM}-$		-	0.002	0.01	-	0.002	0.01	V
	$V_{OM}+$	$R_L = \infty$	14.99	15	-	14.99	15	-	V
	$V_{OM}-$		-	0	0.01	-	0	0.01	V
Maximum Output Current	$I_{OM}+$ (Source)	$V_O = 7.5V$	12	22	45	12	22	45	mA
	$I_{OM}-$ (Sink)		12	20	45	12	20	45	mA
Total Supply Current, $R_L = \infty$	I+	V_O (Amp A) = 7.5V V_O (Amp B) = 7.5V	-	9	16.5	-	9	16.5	mA
		V_O (Amp A) = 0V V_O (Amp B) = 0V	-	1.2	4	-	1.2	4	mA
		V_O (Amp A) = 0V V_O (Amp B) = 7.5V	-	5	9.5	-	5	9.5	mA
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	8	-	-	6	-	µV/°C
Crosstalk		f = 1kHz	-	120	-	-	120	-	dB

Schematic Diagram



HARRIS SEMICONDUCTOR

CA5420, CA5420A

0.5MHz, Low Supply Voltage, Low Input Current BiMOS Operational Amplifiers

November 1996

Features

- **CA5420A, CA5420 at 5V Supply Voltage with Full Military Temperature Range Guaranteed Specifications**
- **CA5420A, CA5420 Guaranteed to Operate from ±1V to ±10V Supplies**
- **2V Supply at 300μA Supply Current**
- **1pA (Typ) Input Current (Essentially Constant to 85°C)**
- **Rail-to-Rail Output Swing (Drive ±2mA Into 1kΩ Load)**
- **Pin Compatible with 741 Op Amp**

Applications

- **pH Probe Amplifiers**
- **Picoammeters**
- **Electrometer (High Z) Instruments**
- **Portable Equipment**
- **Inaccessible Field Equipment**
- **Battery Dependent Equipment (Medical and Military)**
- **5V Logic Systems**
- **Microprocessor Interface**

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA5420AM (5420A)	-55 to 125	8 Ld SOIC	M8.15
CA5420AT	-55 to 125	8 Pin Metal Can	T8.C
CA5420E	-55 to 125	8 Ld PDIP	E8.3
CA5420M (5420)	-55 to 125	8 Ld SOIC	M8.15
CA5420T	-55 to 125	8 Pin Metal Can	T8.C

Description

The CA5420A and CA5420 (see Note) are integrated circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. They are designed and guaranteed to operate in microprocessor logic systems that use V+ = 5V, V- = GND, since they can operate down to ±1V supplies. They will also be suitable for 3.3V logic systems.

The CA5420A and CA5420 BiMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10°C increase in temperature. The CA5420 series operates at total supply voltages from 2V to 20V either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45V below the negative supply terminal, an important attribute for single supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.0mA (Min) is provided by using nonlinear current mirrors.

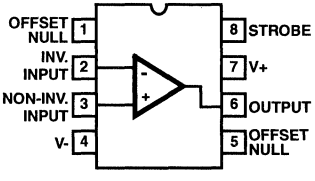
These devices have guaranteed specifications for 5V operation over the full military temperature range of -55°C to 125°C.

The CA5420 series has the same 8 lead pinout used for the industry standard 741.

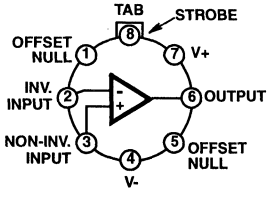
NOTE: Formerly Development Type No. TA10841.

Pinouts

CA5420 (PDIP, SOIC)
TOP VIEW



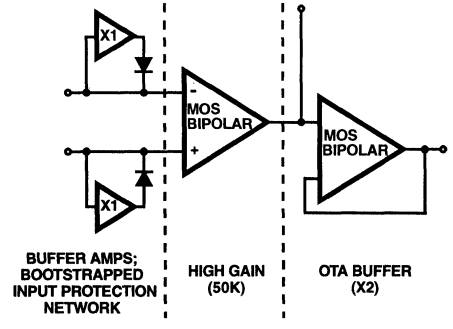
CA5420 (METAL CAN)
TOP VIEW



NOTE: Pin is connected to Case.

Functional Diagram

CA5420



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **1925.3**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 22V
Differential Input Voltage 15V
Input Voltage . . . . . (V+ + 8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . $-55^{o}C$ to $125^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
PDIP Package	96	N/A
SOIC Package	157	N/A
Metal Can Package	165	80

Maximum Junction Temperature (Metal Can) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range (All Types) . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Typical Values Intended Only for Design Guidance. V+ = +5V; V- = GND, $T_A = 25^{o}C$

PARAMETER		SYMBOL	TEST CONDITIONS		CA5420	CA5420A	UNITS
Input Resistance		R_I			150	150	TΩ
Input Capacitance		C_I			4.9	4.9	pF
Output Resistance		R_O			300	300	Ω
Equivalent Input Noise Voltage		e_N	f = 1kHz	$R_S = 100Ω$	62	62	$nV/\sqrt{Hz}$
			f = 10kHz		38	38	$nV/\sqrt{Hz}$
Short-Circuit Current	Source	I_{OM+}			2.6	2.6	mA
To Opposite Supply	Sink	I_{OM-}			2.4	2.4	mA
Gain Bandwidth Product		f_T			0.5	0.5	MHz
Slew Rate		SR			0.5	0.5	V/µs
Transient Response	Rise Time	t_r	$R_L = 2kΩ$, $C_L = 100pF$		0.7	0.7	µs
	Overshoot	OS			15	15	%
Current from Terminal 8 To V-		I_{8+}			20	20	µA
Current from Terminal 8 To V+		I_{8-}			2	2	mA
Settling Time		0.01%	$A_V = 1$	$2V_{P-P}$ Input	8	8	µs
		0.10%	$A_V = 1$	$2V_{P-P}$ Input	4.5	4.5	µs

Electrical Specifications

$T_A = 25^{o}C$, V+ = 5V, V- = 0, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420			CA5420A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	$V_O = 2.5V$	-	1.5	10	-	1	5	mV
Input Offset Current	I_{IO}	$V_O = 2.5V$	-	0.02	1	-	0.02	0.5	pA
Input Current	I_I	$V_O = 2.5V$	-	0.02	2	-	0.02	1	pA
Common Mode Rejection Ratio	CMRR	$V_{CM} = 0$ to 3.7V, $V_O = 2.5V$	70	80	-	75	83	-	dB
Common Mode Input Voltage Range	V_{ICR+}	$V_O = 2.5V$	3.7	4	-	3.7	4	-	V
	V_{ICR-}		-	-0.3	0	-	-0.3	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	70	80	-	75	83	-	dB

Electrical Specifications $T_A = 25^oC$, V+ = 5V, V- = 0, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420			CA5420A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Voltage Gain	A_{OL}								
V_O = 0.5 to 4V		$R_L = \infty$	85	87	-	85	87	-	dB
V_O = 0.5 to 4V		R_L = 10kΩ	85	87	-	85	87	-	dB
V_O = 0.7 to 3V		R_L = 2kΩ	80	85	-	80	85	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1.2	2.7	-	1.2	2.7	-	mA
Sink Current	I_{SINK}	V_O = 5V	1.2	2.1	-	1.2	2.1	-	mA
Output Voltage	V_{OM+}	$R_L = \infty$	4.9	4.94	-	4.9	4.94	-	V
	V_{OM-}		-	0.13	0.15	-	0.13	0.15	V
	V_{OM+}	R_L = 10kΩ	4.7	4.9	-	4.7	4.9	-	V
	V_{OM-}		-	0.12	0.15	-	0.12	0.15	V
	V_{OM+}	R_L = 2kΩ	3.5	4.6	-	3.5	4.6	-	V
	V_{OM-}		-	0.1	0.15	-	0.1	0.15	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	400	500	-	400	500	µA
		V_O = 2.5V	-	430	550	-	430	550	µA

Electrical Specifications $T_A = -55^oC$ to 125^oC, V+ = 5V, V- = 0, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420			CA5420A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	3	15	-	2	10	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	1.5	3	-	1.5	3	nA
Up to $T_A = 85^oC$	I_{IO}		-	2	10	-	2	10	pA
Input Current	$\|I_I\|$	V_O = 2.5V	-	2	5	-	2	5	nA
Up to $T_A = 85^oC$	$\|I_I\|$		-	15	25	-	10	15	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.7V, V_O = 2.5V	65	75	-	70	80	-	dB
Common Mode Input Voltage Range	V_{ICR+}	V_O = 2.5V	3.7	4	-	3.7	4	-	V
	V_{ICR-}		-	-0.3	0	-	-0.3	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	65	80	-	70	83	-	dB
Large Signal Voltage Gain	A_{OL}								
V_O = 0.5 to 4V		$R_L = \infty$	80	85	-	85	87	-	dB
V_O = 0.7 to 4V		R_L = 10kΩ	80	85	-	80	87	-	dB
V_O = 0.7 to 2.5V		R_L = 2kΩ	75	80	-	75	80	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1	2.7	-	1	2.7	-	mA
Sink Current	I_{SINK}	V_O = 5V	1	2.1	-	1	2.1	-	mA
Output Voltage	V_{OM+}	$R_L = \infty$	4.8	4.9	-	4.8	4.9	-	V
	V_{OM-}		-	0.16	0.2	-	0.16	0.2	V
	V_{OM+}	R_L = 10kΩ	4.7	4.9	-	4.7	4.9	-	V
	V_{OM-}		-	0.15	0.20	-	0.15	0.2	V
	V_{OM+}	R_L = 2kΩ	3	4	-	3	4	-	V
	V_{OM-}		-	0.14	0.2	-	0.14	0.2	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	430	550	-	430	550	µA
		V_O = 2.5V	-	480	600	-	480	600	µA

Electrical Specifications For Equipment Design at V_{SUPPLY} = ±1V, T_A = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420			CA5420A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}		-	5	10	-	2	5	mV
Input Offset Current	$\|I_{IO}\|$		-	0.01	4 (Note 3)	-	0.01	4 (Note 3)	pA
Input Current	$\|I_I\|$		-	0.02	5 (Note 3)	-	0.02	5 (Note 3)	pA
Large Signal Voltage Gain	A_{OL}	R_L = 10kΩ	10	100	-	20	100	-	kV/V
			80	100	-	86	100	-	dB
Common Mode Rejection Ratio	CMRR		-	560	1800	-	560	1000	µV/V
			55	65	-	60	65	-	dB
Common Mode Input Voltage Range	V_{ICR+}		0.2	0.5	-	0.2	0.5	-	V
	V_{ICR-}		-	-1.3	-	-1	-1.3	-	V
Power Supply Rejection Ratio	PSRR		-	100	1000	-	32	320	µV/V
			60	80	-	70	90	-	dB
Maximum Output Voltage	V_{OM+}	R_L = ∞	0.9	0.95	-	0.9	0.95	-	V
	V_{OM-}		-0.85	-0.91	-	-0.85	-0.91	-	V
Supply Current	I_{SUPPLY}		-	350	650	-	350	650	µA
Device Dissipation	P_D		-	0.7	1.1	-	0.7	1.1	mW
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$		-	4	-	-	4	-	µV/°C

Electrical Specifications For Equipment Design at V_{SUPPLY} = ±10V, T_A = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5420			CA5420A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}		-	5	10	-	2	5	mV
Input Offset Current	$\|I_{IO}\|$		-	0.03	4 (Note 3)	-	0.03	4 (Note 3)	pA
Input Current	$\|I_I\|$		-	0.05	5 (Note 3)	-	0.05	5 (Note 3)	pA
Large Signal Voltage Gain	A_{OL}	R_L = 10kΩ	10	100	-	20	100	-	kV/V
			80	100	-	86	100	-	dB
Common Mode Rejection Ratio	CMRR		-	100	320	-	100	320	µV/V
			70	80	-	70	80	-	dB
Common Mode Input Voltage Range	V_{ICR+}		8.5	9.3	-	9	9.3	-	V
	V_{ICR-}		-10	-10.3	-	-10	-10.3	-	V
Power Supply Rejection Ratio	PSRR		-	32	320	-	32	320	µV/V
			70	90	-	70	90	-	dB
Maximum Output Voltage	V_{OM+}	R_L = ∞	9.7	9.9	-	9.7	9.9	-	V
	V_{OM-}		-9.7	-9.85	-	-9.7	-9.85	-	V
Supply Current	I_{SUPPLY}		-	450	1000	-	450	1000	µA
Device Dissipation	P_D		-	9	14	-	9	14	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	4	-	-	4	-	µV/°C

NOTE:

3. The maximum limit represents the levels obtainable on high-speed automatic test equipment. Typical values are obtained under laboratory conditions.

Typical Applications

Picoammeter Circuit

The exceptionally low input current (typically 0.2pA) makes the CA5420 highly suited for use in a picoammeter circuit. With only a single 10GΩ resistor, this circuit covers the range from ±1.5pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1MΩ resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10MΩ resistor connected to pin 2 of the CA5420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

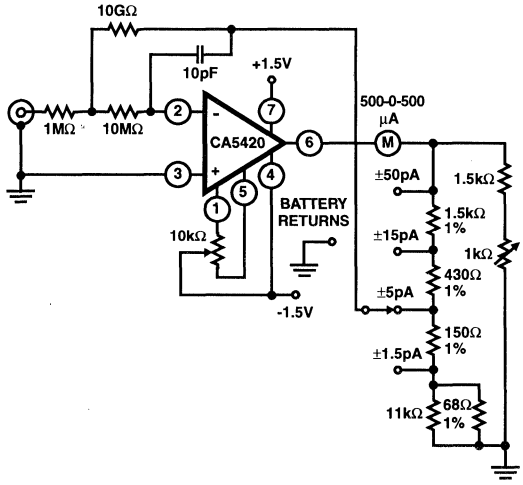


FIGURE 1. PICOAMMETER CIRCUIT

High Input Resistance Voltmeter

Advantage is taken of the high input impedance of the CA5420 in a high input resistance DC voltmeter. Only two 1.5V "AA" type penlite batteries power this exceedingly high-input resistance (>1,000,000MΩ) DC voltmeter. Full-scale deflection is ±500mV, ±150mV, and ±15mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300µA. At full-scale deflection this current rises to 800µA. Carbon-zinc battery life should be in excess of 1,000 hours.

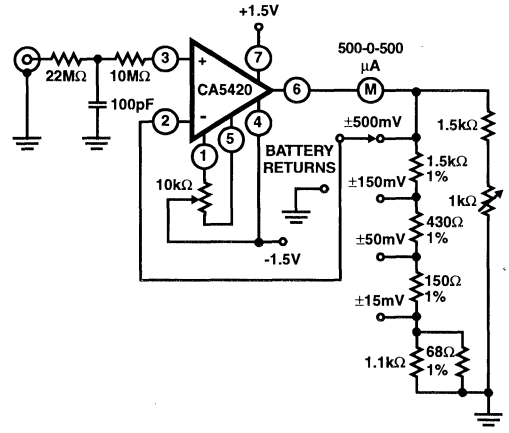


FIGURE 2. HIGH INPUT RESISTANCE VOLTMETER

Typical Performance Curves

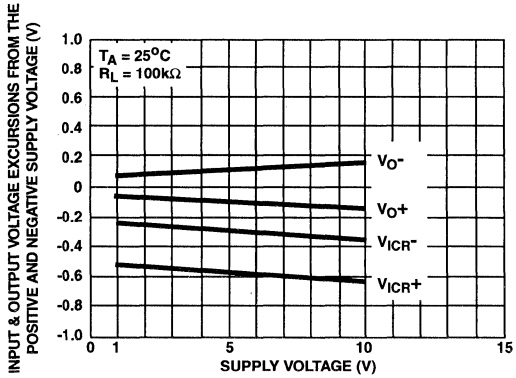


FIGURE 3. OUTPUT VOLTAGE SWING AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

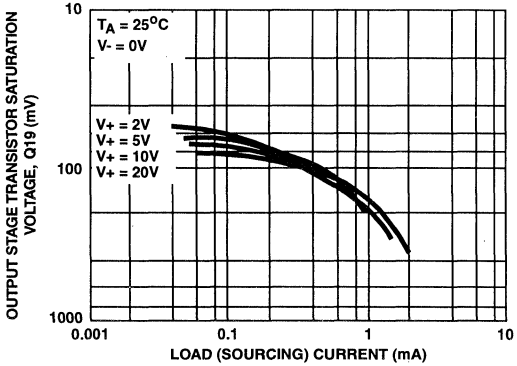


FIGURE 4. OUTPUT VOLTAGE vs LOAD SOURCING CURRENT

Typical Performance Curves (Continued)

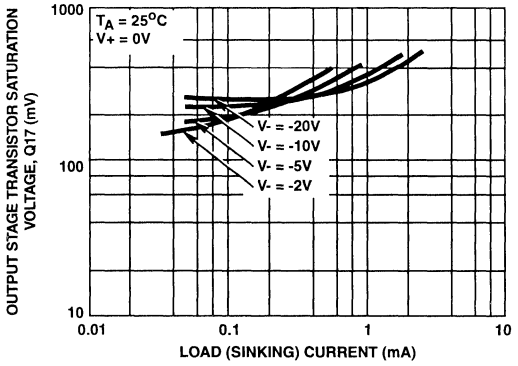


FIGURE 5. OUTPUT VOLTAGE vs LOAD SINKING CURRENT

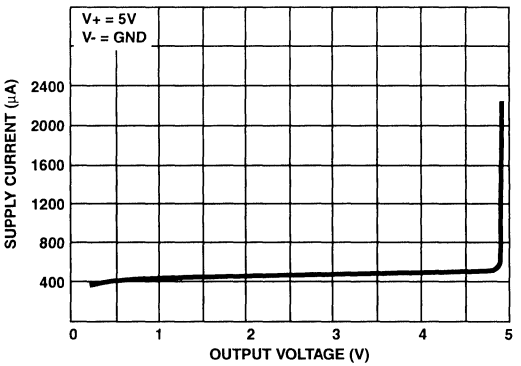


FIGURE 6. SUPPLY CURRENT vs OUTPUT VOLTAGE

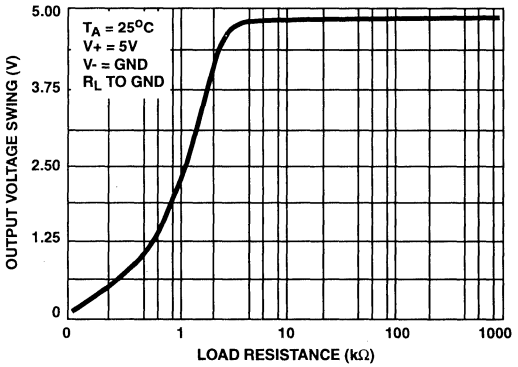


FIGURE 7. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

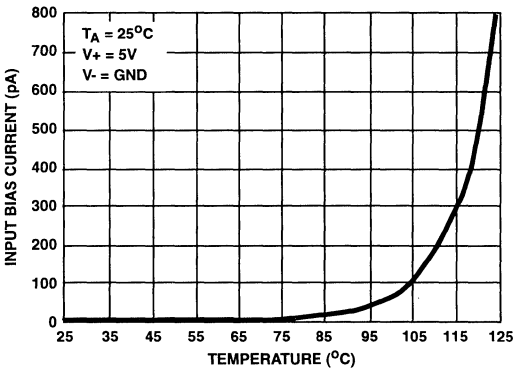


FIGURE 8. INPUT BIAS CURRENT DRIFT ($\Delta I_B/\Delta T$)

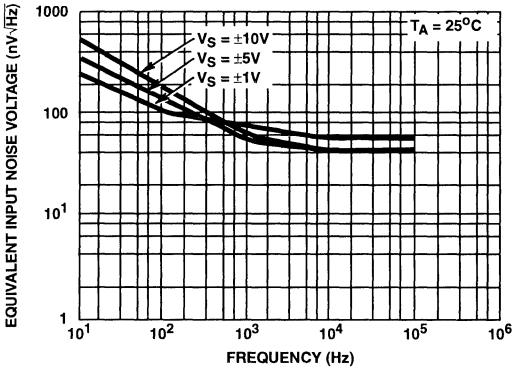


FIGURE 9. INPUT NOISE VOLTAGE vs FREQUENCY

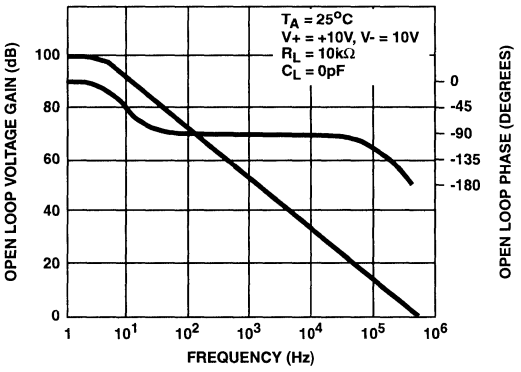


FIGURE 10. OPEN LOOP GAIN AND PHASE SHIFT RESPONSE

HARRIS SEMICONDUCTOR

CA5470

Quad, 14MHz, Microprocessor BiMOS-E Operational Amplifier with MOSFET Input/Bipolar Output

November 1996

Features

- High Speed CMOS Input Stage Provides
  - Very High Z_I . . . . . 5TΩ (5 x 10^{12}Ω) (Typ)
  - Very Low I_I . . . . . 0.5pA (Typ) at 5V Operation
  - Very Low I_{IO} . . . . . 0.5pA (Typ) at 5V Operation
- ESD Protection to 2000V
- 3V to 16V Power Supply Operation
- Fully Guaranteed Specifications Over Full Military Range
- Wide BW (14MHz); High SR (5V/μs) at 5V Supply
- Wide V_{ICR} Range From -0.5V to 3.7V (Typ) at 5V Supply
- Ideally Suited for CMOS and HCMOS Applications

Applications

- Bar Code Readers
- Photodiode Amplifiers (IR)
- Microprocessor Buffering
- Ground Reference Single Supply Amplifiers
- Fast Sample and Hold
- Timers
- Voltage Controlled Oscillators
- Voltage Followers
- V to I Converters
- Peak Detectors
- Precision Rectifiers
- 5V Logic Systems
- 3V Logic Systems

Description

The CA5470 is an operational amplifier that combines the advantages of both high speed CMOS and bipolar transistors on a single monolithic chip. It is constructed in the BiMOS-E process which adds drain-extension implants to 3μm polygate CMOS, enhancing both the voltage capability and providing vertical bipolar transistors for broadband analog/digital functions. This process lends itself easily to high speed operational amplifiers, comparators, analog switches and interface peripherals, resulting in twice the speed of the conventional CMOS transistors having similar feature size.

BiMOS-E are broadbased bipolar transistors that have high transconductance, gains more constant with current level, stable "precision" base-emitter offset voltages and superior drive capability. Excellent interface with environmental potentials enable use in 5V logic systems and future 3.3V logic systems. Refer to Application Note AN8811.

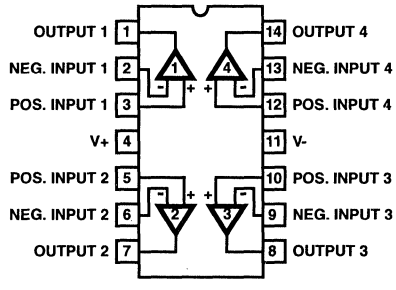
ESD capability exceeds the standard 2000V level. The CA5470 series can operate with single supply voltages from 3V to 16V or ±1.5V to ±8V. They have guaranteed specifications at both 5V and ±7.5V at room temperature as well as over the full -55°C to 125°C military range.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA5470E	-55 to 125	14 Ld PDIP	E14.3
CA5470M (5470)	-55 to 125	14 Ld SOIC	M14.15
CA5470M96 (5470)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinout

CA5470 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1946.3**

Absolute Maximum Ratings

DC Supply Voltage (Between V+ And V- Terminals) 16V
Differential Input Voltage. 8V
Input Voltage. . . . . (V+ +8V) to (V- -0.5V)
Input Current. 1mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . $-55^{o}C$ to $125^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{o}C/W$)
PDIP Package	80
SOIC Package	175

Maximum Junction Temperature (Die) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Typical Values Intended Only for Design Guidance at V+ = 5V, V- = 0V, $T_A = 25^{o}C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
Input Resistance	R_I		5	TΩ
Input Capacitance	C_I	f = 1MHz	3.1	pF
Unity Gain Crossover Frequency	f_T		14	MHz
Slew Rate	SR	$V_{OUT} = 3.65V_{P-P}$	5	V/µs
Transient Response:		$C_L = 25pF$, $R_L = 2k\Omega$ (Voltage Follower)		
Rise Time/Fall Time	t_r		27/25	ns
Overshoot	OS		20	%
Settling Time (To <0.1%, $V_{IN} = 4V_{P-P}$)	t_S	$C_L = 25pF$, $R_L = 2k\Omega$ (Voltage Follower)	1	µs
Full Power BW, SR = 5V/µs	FPBW	$A_V = 1$, $V_{OUT} = 3.65V_{P-P}$	436	kHz

Electrical Specifications

$T_A = 25^{o}C$, V+ = 5V, V- = GND

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$\lvert V_{IO}\rvert$		-	6	22	mV
Input Offset Current	$\lvert I_{IO}\rvert$		-	0.5	50 (Note 3)	pA
Input Current	I_I		-	0.5	50 (Note 3)	pA
Common Mode Input Range	V_{ICR}		3.5	-0.5 to 3.7	0	V
Common Mode Rejection Ratio	CMRR	V_{ICR} = 0V to 3.5V	55	70	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = 2V	60	75	-	dB
Positive Output Voltage Swing	V_{OM+}	$R_L = 2k\Omega$ to GND	4	4.4	-	V
Negative Output Voltage Swing	V_{OM-}	$R_L = 2k\Omega$ to GND	-	0.06	0.10	V
Total Supply Current	I_{SUPPLY}	$V_{OUT} = 2.5V$, $R_L = \infty$	-	6	7	mA
Unity Gain Bandwidth Product	f_T		10	14	-	MHz
Slew Rate	SR		4	5	-	V/µs
Output Current						
Source to opposite supply	I_{SOURCE}		4	5.5	-	mA
Sink to opposite supply	I_{SINK}		1.0	1.2	-	mA
Open Loop Gain	A_{OL}	0.5V to 3.5V, $R_L = 10k\Omega$	80	90	-	dB

NOTE:

3. This is the lowest value that can be tested reliably. Almost all devices will be <10pA.

Electrical Specifications T_A = -55°C to 125°C, V+ = 5V, V- = GND

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$\|V_{IO}\|$		-	6	25	mV
Input Offset Current	$\|I_{IO}\|$		-	550	5500	pA
Input Current	I_I		-	550	11000	pA
Common Mode Input Range	V_{ICR}		3.5	-0.5 to 3.7	0	V
Common Mode Rejection Ratio	CMRR	V_{ICR} = 0V to 3.5V	50	65	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = 2V	58	75	-	dB
Positive Output Voltage Swing	V_{OM+}	R_L = 2kΩ to GND	3.8	4.2	-	V
Negative Output Voltage Swing	V_{OM-}	R_L = 2kΩ to GND	-	0.08	0.11	V
Total Supply Current	I_{SUPPLY}	V_{OUT} = 2.5V	-	9	11	mA
Unity Gain Bandwidth Product	f_T		8	12	-	MHz
Slew Rate	SR		3	5	-	V/µs
Output Current						
Source to opposite supply	I_{SOURCE}		4	5.5	-	mA
Sink to opposite supply	I_{SINK}		0.8	1.2	-	mA
Open Loop Gain	A_{OL}	0.5V to 3.5V, R_L = 10kΩ	80	90	-	dB

Electrical Specifications T_A = 25°C, V_{SUPPLY} = ±7.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$\|V_{IO}\|$		-	5	25	mV
Input Offset Current	$\|I_{IO}\|$		-	0.5	50 (Note 4)	pA
Input Current	I_I		-	1	50 (Note 4)	pA
Common Mode Input Range	V_{ICR}		5.8	-7.8 to 6.0	-7.5	V
Common Mode Rejection Ratio	CMRR	V_{ICR} = 0V to 13.3V	60	70	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = 1V	60	76	-	dB
Positive Output Voltage Swing	V_{OM+}					
		R_L = 2kΩ to GND	6.3	6.5	-	V
		R_L = 10kΩ to GND	6.4	6.6	-	V
Negative Output Voltage Swing	V_{OM-}					
		R_L = 2kΩ to GND	-	-2.6	-2	V
		R_L = 10kΩ to GND	-	-7.3	-7.1	V
Total Supply Current	I_{SUPPLY}	V_{OUT} = GND, R_L = ∞	-	10	12	mA
Unity Gain Bandwidth Product	f_T		12	16	-	MHz
Slew Rate	SR		4	7	-	V/µs
Output Current						
Source to opposite supply	I_{SOURCE}		6.2	6.8	-	mA
Sink to opposite supply	I_{SINK}		1	1.4	-	mA
Open Loop Gain	A_{OL}	-5V to +5V, R_L = 10kΩ	80	90	-	dB

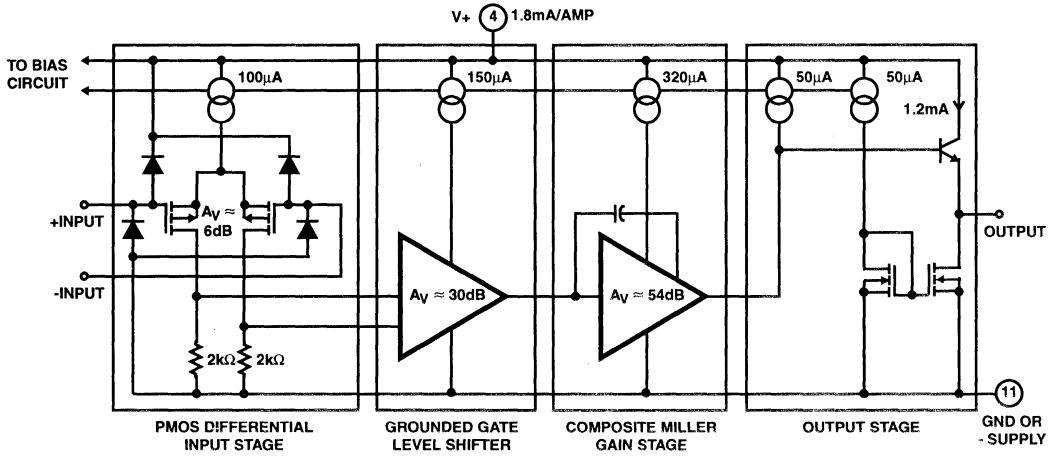
NOTE:

4. This is the lowest value that can be tested reliably. Almost all devices will be <10pA.

Electrical Specifications T_A = -55°C to 125°C, V_{SUPPLY} = ±7.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$\|V_{IO}\|$		-	5	30	mV
Input Offset Current	$\|I_{IO}\|$		-	550	5500	pA
Input Current	I_I		-	1100	11000	pA
Common Mode Input Range	V_{ICR}		5.8	-7.8 to 6.0	-7.5	V
Common Mode Rejection Ratio	CMRR	V_{ICR} = 0V to 3.5V	58	70	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = 1V	60	76	-	dB
Positive Output Voltage Swing	V_{OM+}					
		R_L = 2kΩ to GND	4.75	5.5	-	V
		R_L = 10kΩ to GND	6.1	6.4	-	V
Negative Output Voltage Swing	V_{OM-}					
		R_L = 2kΩ to GND	-	-2.6	-2	V
		R_L = 10kΩ to GND	-	-7.3	-7.1	V
Total Supply Current	I_{SUPPLY}	V_{OUT} = GND, R_L = ∞	-	12	18	mA
Unity Gain Bandwidth Product	f_T		10	15	-	MHz
Slew Rate	SR		3	7	-	V/μs
Output Current						
Source to opposite supply	I_{SOURCE}		6.2	6.8	-	mA
Sink to opposite supply	I_{SINK}		1	1.4	-	mA
Open Loop Gain	A_{OL}	-5V to +5V, R_L = 10kΩ	80	90	-	dB

Block Diagram ($^1/_4$ of CA5470)



Typical Performance Curve

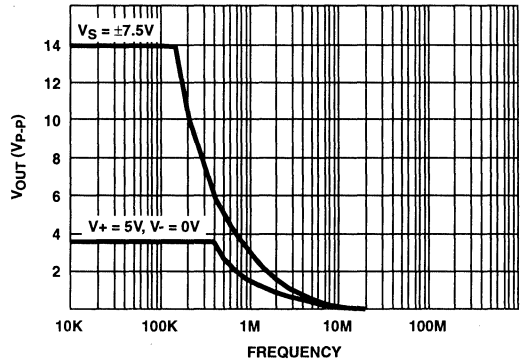
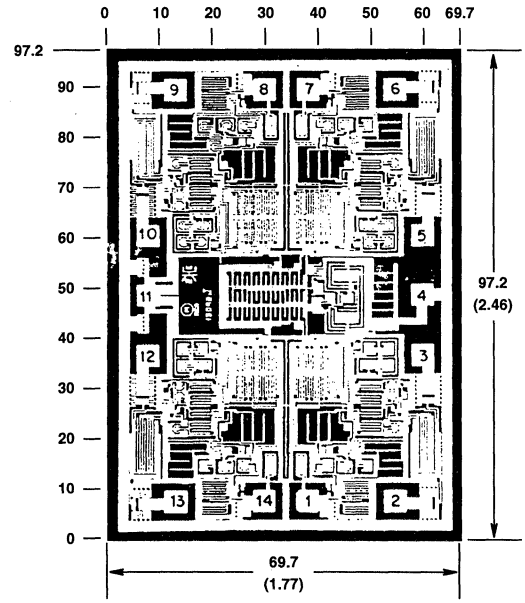


FIGURE 1. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

Metallization Mask Layout

Dimensions in parentheses are in millimeters and derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.



HA-2400, HA-2404, HA-2405

40MHz, PRAM Four Channel Programmable Amplifiers

November 1996

Features

- Programmability
- High Rate Slew 30V/µs
- Wide Gain Bandwidth 40MHz
- High Gain 150kV/V
- Low Offset Current 5nA
- High Input Impedance 30MΩ
- Single Capacitor Compensation
- DTL/TTL Compatible Inputs

Applications

- Thousands of Applications; Program
  - Signal Selection/Multiplexing
  - Operational Amplifier Gain
  - Oscillator Frequency
  - Filter Characteristics
  - Add-Subtract Functions
  - Integrator Characteristics
  - Comparator Levels

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-2400-2	-55 to 125	16 Ld CERDIP	F16.3
HA1-2404-4	-25 to 85	16 Ld CERDIP	F16.3
HA1-2405-5	0 to 75	16 Ld CERDIP	F16.3
HA3-2405-5	0 to 75	16 Ld PDIP	E16.3

Description

THA-2400/04/05 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

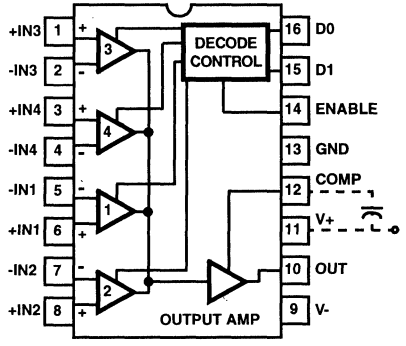
Each channel of the HA-2400/04/05 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing signal selection and mathematical function designs. With 30V/µs slew rate, 40MHz gain bandwidth and 30MΩ input impedance these devices are ideal building blocks for signal generators, active filters and data acquisition designs. Programmability, coupled with 4mV typical offset voltage and 5nA offset current, makes these amplifiers outstanding components for signal conditioning circuits.

During Disable Mode V_{OUT} goes to V-. For high output impedance during Disable, see HA2444.

For further design ideas, see Application Note AN514.

Pinout

HA-2400/04 (CERDIP)
HA-2405 (CERDIP, PDIP)
TOP VIEW



TRUTH TABLE

D1	D0	EN	SELECTED CHANNEL	D1
L	L	H	1	L
L	H	H	2	L
H	L	H	3	H
H	H	H	4	H
X	X	L	None, V_{OUT} goes to V-	X

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2891.2**

Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage. . . . . V_{SUPPLY}
Digital Input Voltage . . . . . -0.76V to +10.0V
Output Current . . . . . Short Circuit Protected, I_{SC} <±33mA)
Internal Power Dissipation (Note 1)

Operating Conditions

Temperature Range
HA-2400-2. . . . . -55^oC to 125^oC
HA-2404-4. . . . . -25^oC to 85^oC
HA-2405-5. . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	80	N/A
CERDIP Package	90	35

Maximum Junction Temperature (Ceramic Package). . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s). . . . . 300^oC)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation including output load, must be designed to maintain the junction temperature below 175^oC for the ceramic package, and below 150^oC for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified. Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4$. Limits apply to each of the four channels, when addressed

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	HA-2400/04			HA-2405			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	4	9	-	4	9	mV
		Full	-	-	11	-	-	11	mV
Bias Current (Note 8)		25	-	50	200	-	50	250	nA
		Full	-	-	400	-	-	500	nA
Offset Current (Note 8)		25	-	5	50	-	5	50	nA
		Full	-	-	100	-	-	100	nA
Input Resistance (Note 8)		25	-	30	-	-	30	-	MΩ
Common Mode Range		Full	±9.0	-	-	±9.0	-	-	V
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$R_L = 2k\Omega$	25	50	150	-	50	150	-	kV/V
	$V_{OUT} = 20V_{P-P}$	Full	25	-	-	25	-	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm5V$	Full	80	100	-	74	100	-	dB
Gain Bandwidth (Notes 3, 9)		25	20	40	-	20	40	-	MHz
Gain Bandwidth (Notes 4, 9)		25	4	8	-	4	8	-	MHz
Minimum Stable Gain	($C_{COMP} = 0$)		10	-	-	10	-	-	V/V
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 2k\Omega$	Full	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current		25	10	20	-	10	20	-	mA
Full Power Bandwidth (Notes 3, 10)	$V_{OUT} = 20V_{P-P}$	25	640	950	-	640	950	-	kHz
Full Power Bandwidth (Notes 4, 10)	$V_{OUT} = 20V_{P-P}$	25	200	250	-	200	250	-	kHz
TRANSIENT RESPONSE (Note 11)									
Rise Time (Note 4)	$V_{OUT} = 200mV_{PEAK}$	25	-	20	45	-	20	50	ns
Overshoot (Note 4)	$V_{OUT} = 200mV_{PEAK}$	25	-	25	40	-	25	40	%
Slew Rate (Note 3)	$V_{OUT} = 10V_{P-P}$	25	20	30	-	20	30	-	V/µs
Slew Rate (Notes 4, 9)	$V_{OUT} = 10V_{P-P}$	25	6	8	-	6	8	-	V/µs

Electrical Specifications Test Conditions: $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified. Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4$. Limits apply to each of the four channels, when addressed **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-2400/04			HA-2405			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time (Notes 4, 5, 9)	$V_{OUT} = 10V_{P-P}$	25	-	1.5	2.5	-	1.5	2.5	µs
CHANNEL SELECT CHARACTERISTICS									
Digital Input Current	$V_{IN} = 0V$	Full	-	1	1.5	-	1	1.5	mA
Digital Input Current	$V_{IN} = +5.0V$	Full	-	5	-	-	5	-	nA
Output Delay (Notes 6, 9)		25	-	100	250	-	100	250	ns
Crosstalk (Note 7)		25	-80	-110	-	-74	-110	-	dB
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	4.8	6.0	-	4.8	6.0	mA
Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$	Full	74	90	-	74	90	-	dB

NOTES:

3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.
5. To 0.1% of final value.
6. To 10% of final value; output then slews at normal rate to final value.
7. Unselected input to output; $V_{IN} = \pm 10V_{DC}$.
8. Unselected channels have approximately the same input parameters.
9. Guaranteed by design.
10. Full Power Bandwidth based on slew rate measurement using: $FPBW = \frac{SR}{2\pi V_{PEAK}}$; $V_{PEAK} = 5V$.
11. See Figure 13 for test circuit.

Schematic Diagram

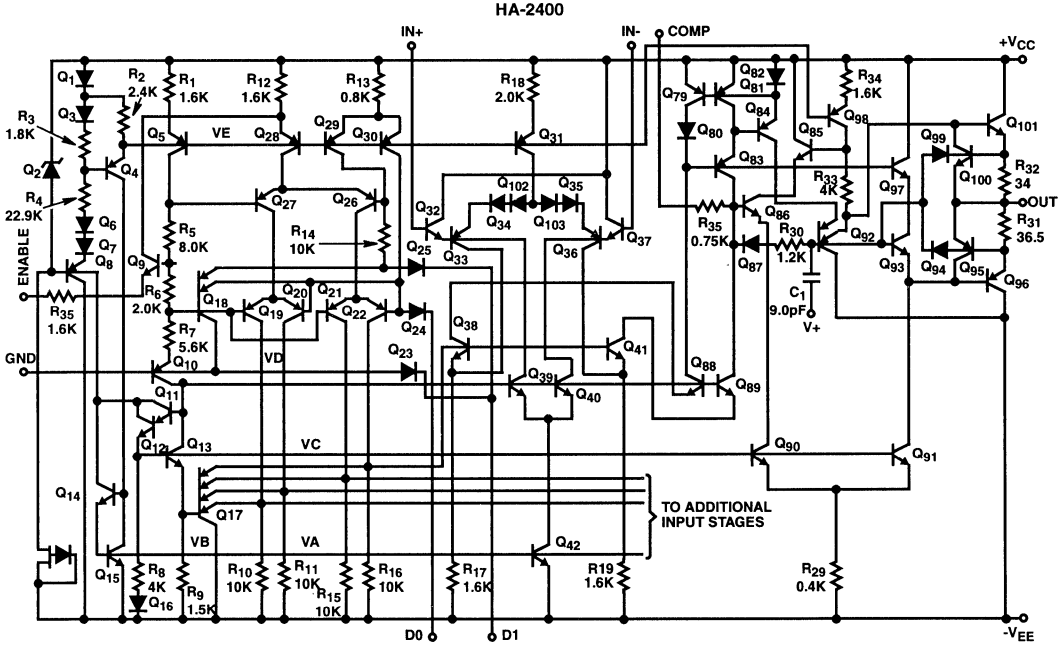


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stage

Typical Applications

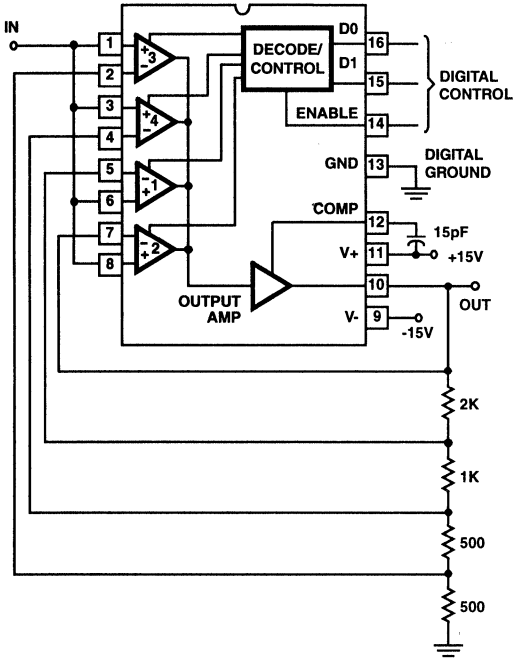
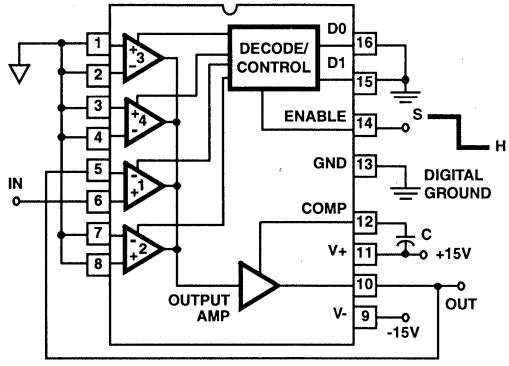


FIGURE 1. HA-2400 AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN



Sample Charging Rate = $\frac{I_1}{C}$ V/s

Hold Drift Rate = $\frac{I_2}{C}$ V/s

Switch Pedestal Error = $\frac{Q}{C}$ V

$I_1 \approx 150 \times 10^{-6}$A

$I_2 \approx 200 \times 10^{-9}$A at 25°C

$\approx 600 \times 10^{-9}$A at -55°C

$\approx 100 \times 10^{-9}$A at 125°C

$Q \approx 2 \times 10^{-12}$C

FIGURE 2. HA-2400 SAMPLE AND HOLD

For more examples, see Harris Application Note AN514.

Typical Performance Curves

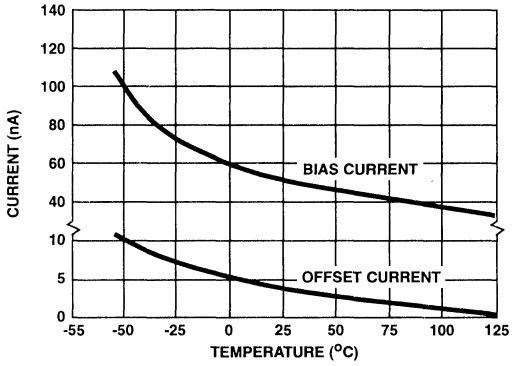


FIGURE 3. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

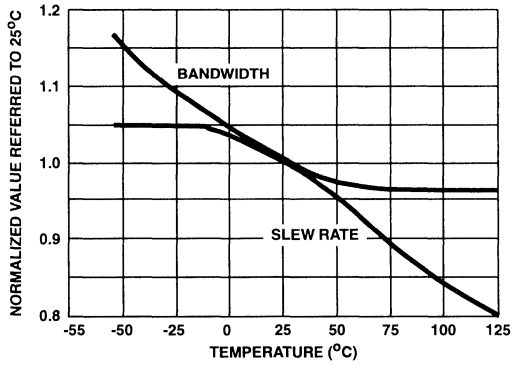


FIGURE 4. NORMALIZED AC PARAMETERS vs TEMPERATURE

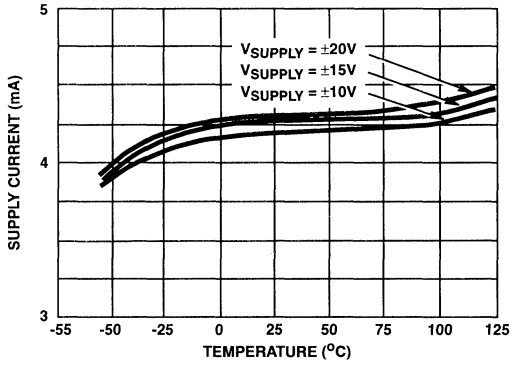


FIGURE 5. POWER SUPPLY CURRENT vs TEMPERATURE

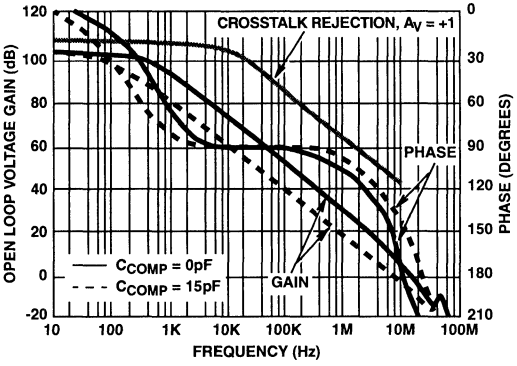


FIGURE 6. OPEN LOOP FREQUENCY AND PHASE RESPONSE

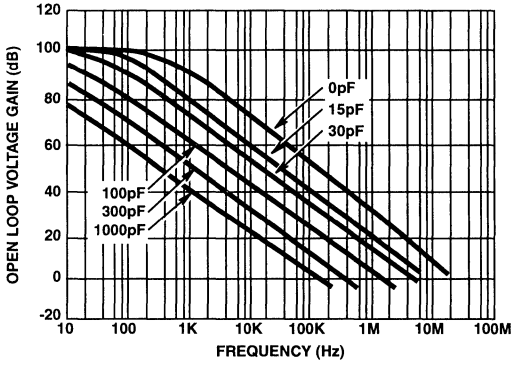


FIGURE 7. FREQUENCY RESPONSE vs C_{COMP}

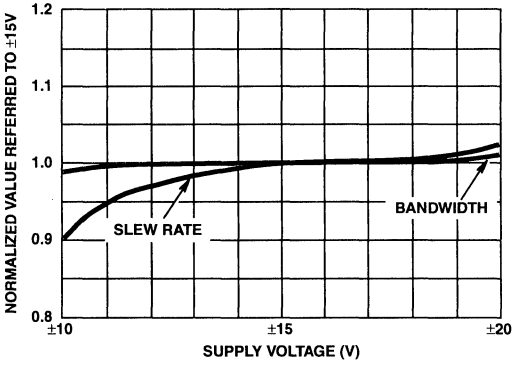


FIGURE 8. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

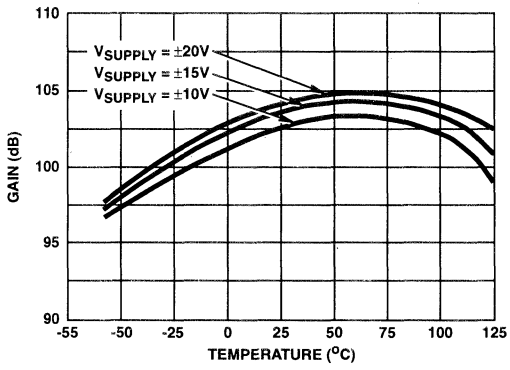


FIGURE 9. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

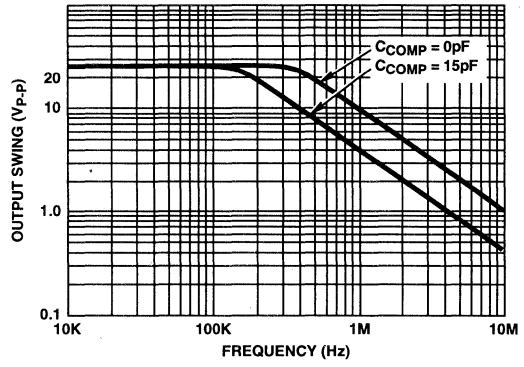


FIGURE 10. OUTPUT VOLTAGE SWING vs FREQUENCY

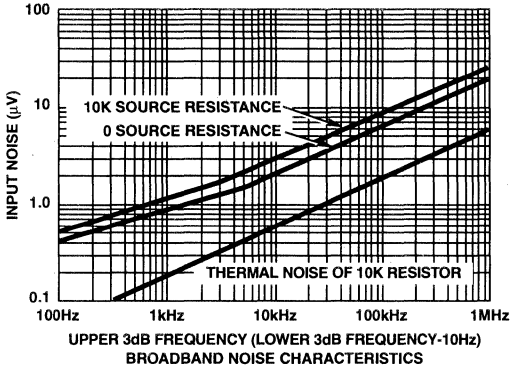


FIGURE 11. EQUIVALENT INPUT NOISE vs BANDWIDTH

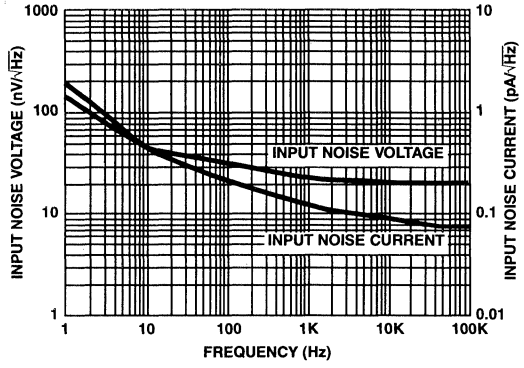


FIGURE 12. INPUT NOISE vs FREQUENCY

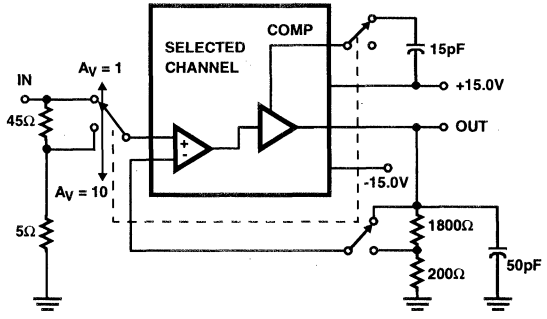


FIGURE 13. SLEW RATE AND TRANSIENT RESPONSE

HARRIS SEMICONDUCTOR

HA-2406

30MHz, Digitally Selectable Four Channel Operational Amplifier

November 1996

Features

- TTL Compatible Inputs
- Single Capacitor Compensation
- Low Crosstalk ..... -110dB
- High Slew Rate 20V/μs
- Low Offset Current 5nA
- Offset Voltage 7mV
- High Gain-Bandwidth 30MHz
- High Input Impedance 30MΩ

Applications

- Digital Control Of
  - Analog Signal Multiplexing
  - Op Amp Gains
  - Oscillator Frequencies
  - Filter Characteristics
  - Comparator Levels

Ordering Information

PART NO.	TEMP RANGE (°C)	PACKAGE	PKG. NO.
HA1-2406-5	0 to 75	16 Ld CERDIP	F16.3
HA3-2406-5	0 to 75	16 Ld PDIP	E16.3
HA9P2406-5	0 to 75	16 Ld SOIC	M16.3
HA9P2406-9	-40 to 85	16 Ld SOIC	M16.3

Description

The HA-2406 is a monolithic device consisting of four op amp input stages that can be individually connected to one output stage by decoding two TTL lines into four channel select signals. In addition to allowing each channel to be addressed, an enable control disconnects all input stages from the output stage when asserted low.

Each input-output combination of the HA-2406 is designed to be a 20V/μs, 30MHz gain-bandwidth amplifier that is stable at a gain of ten. By connecting one external 15pF capacitor all amplifiers are compensated for unity gain operation. The compensation lead may also be used to limit the output swing to TTL levels through suitable clamping diodes and divider networks (see Application Note AN514).

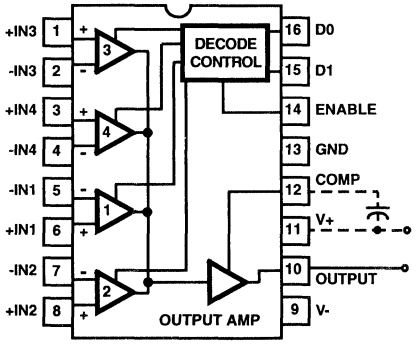
Dielectric isolation and short-circuit protected output stages contribute to the quality and durability of the HA-2406. When used as a simple amplifier, its dynamic performance is very good and when its added versatility is considered, the HA-2406 is unmatched in the analog world. It can replace a number of individual components in analog signal conditioning circuits for digital signal processing systems. Its advantages include saving board space and reducing power supply requirements.

During Disable Mode V_{OUT} goes to V-. For high output impedance during Disable, see HA2444.

For further design ideas, see Application Note AN514.

Pinout

HA-2406
(PDIP, CERDIP, SOIC)
TOP VIEW)



TRUTH TABLE

D1	D0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	None, V_{OUT} goes to V-

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2892.2**

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage Between V+ and V- Terminals 45V
Differential Input Voltage. . . . . V_{SUPPLY}
Output Current . . . . . Short Circuit Protected ($I_{SC} < \pm 33mA$)

Operating Conditions

Temperature Range
HA-2406-5. . . . . 0^oC to 75^oC
HA-2406-9. . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	80	N/A
SOIC Package	96	N/A
CERDIP Package	90	35

Maximum Junction Temperature (Ceramic Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: $V_{SUPPLY} = 15.0V$, Unless Otherwise Specified. Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Limits apply to each of the four channels, when addressed.

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HA-2406-5, -9			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Offset Voltage		25	-	7	10	mV
		Full	-	-	12	mV
Bias Current (Note 7)		25	-	50	250	nA
		Full	-	-	500	nA
Offset Current (Note 7)		25	-	5	50	nA
		Full	-	-	100	nA
Input Resistance (Note 7)		25	-	30	-	MΩ
Common Mode Range		Full	±9.0	-	-	V
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_{OUT} = 20V_{P-P}$	25	40	150	-	kV/V
		Full	20	-	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm 5V$	Full	74	80	-	dB
Gain Bandwidth Product (Notes 2, 9)		25	15	30	-	MHz
Gain Bandwidth Product (Notes 3, 9)		25	3	6	-	MHz
Minimum Stable Gain	$C_{COMP} = 0$		10	-	-	V/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing	$R_L = 2k\Omega$	Full	±10.0	±12.0	-	V
Output Current	$V_{OUT} = \pm 10V$	25	10	15	-	mA
Full Power Bandwidth (Notes 2, 8, 9)	$V_{OUT} = 20V_{P-P}$	25	240	320	-	kHz
Full Power Bandwidth (Notes 3, 8)	$V_{OUT} = 20V_{P-P}$	25	64	95	-	kHz
TRANSIENT RESPONSE (Note 10)						
Rise Time (Note 3)	$V_{OUT} = 200mV_{PEAK}$	25	-	30	100	ns
Overshoot (Note 3)	$V_{OUT} = 200mV_{PEAK}$	25	-	25	40	%
Slew Rate (Notes 2, 9)	$V_{OUT} = 10V_{P-P}$	25	15	20	-	V/µs
Slew Rate (Note 3)	$V_{OUT} = 10V_{P-P}$	25	4	6	-	Vµs
Settling Time (Notes 3, 4)	$V_{OUT} = 10V_{P-P}$	25	-	2.0	3.5	µs
CHANNEL SELECT CHARACTERISTICS						
Digital Input Current	$V_{IN} = 0V$	Full	-	1	1.5	mA

Electrical Specifications Test Conditions: V_{SUPPLY} = 15.0V, Unless Otherwise Specified. Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V. Limits apply to each of the four channels, when addressed. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2406-5, -9			UNITS
			MIN	TYP	MAX	
Digital Input Current	V_{IN} = +5.0V	Full	-	15	-	nA
Output Delay (Notes 5, 9)		25	-	150	300	ns
Crosstalk (Note 6)		25	-74	-110	-	dB
POWER SUPPLY CHARACTERISTICS						
Supply Current		25	-	4.8	7.0	mA
Power Supply Rejection Ratio	V_S = ±10V to ±20V	Full	74	90	-	dB

NOTES:

2. A_V = +10, C_{COMP} = 0, R_L = 2kΩ, C_L = 50pF.
3. A_V = +1, C_{COMP} = 15pF, R_L = 2kΩ, C_L = 50pF.
4. To 0.1% of final value.
5. To 10% of final value; output then slews at normal rate to final value.
6. Unselected input to output; V_{IN} = ±10V
7. Unselected channels have approximately the same input parameters.
8. Full power Bandwidth based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
9. Sample tested.
10. See Figure 11 for test circuit.

Schematic Diagram

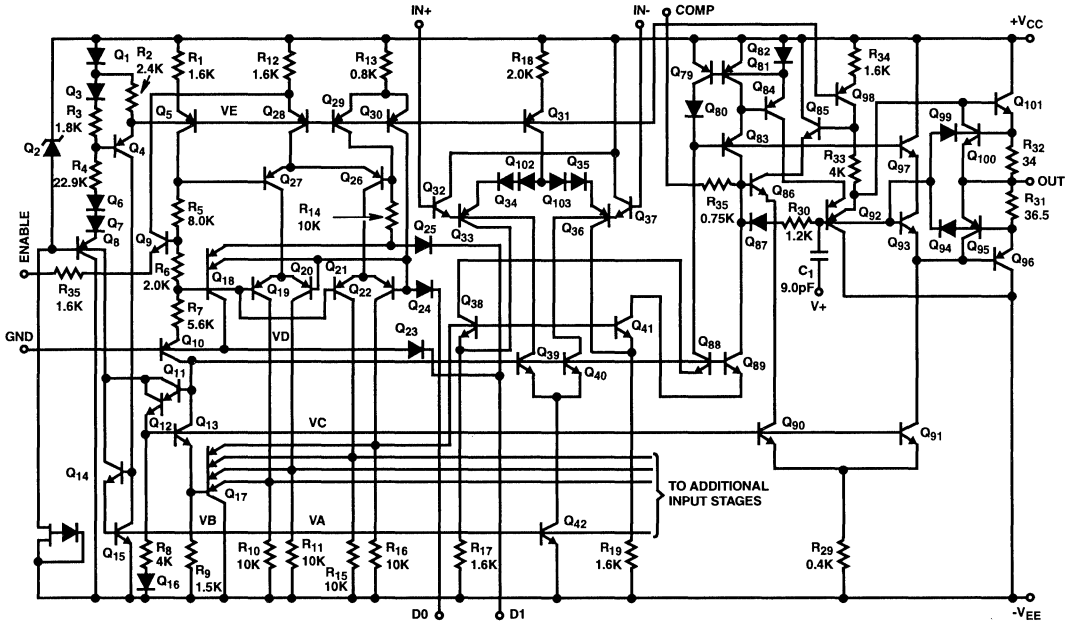


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stag

Typical Applications

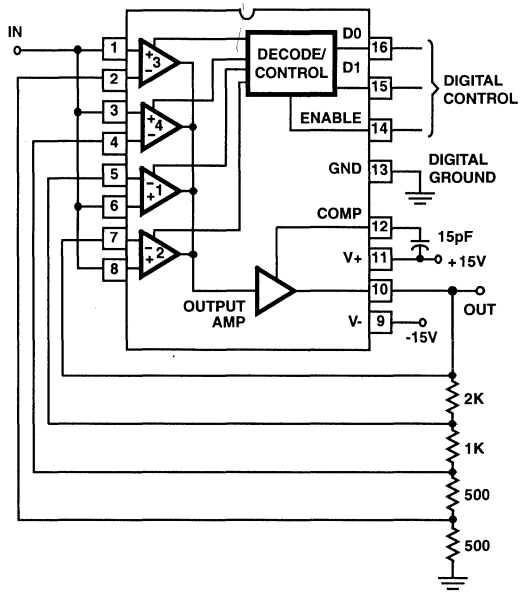
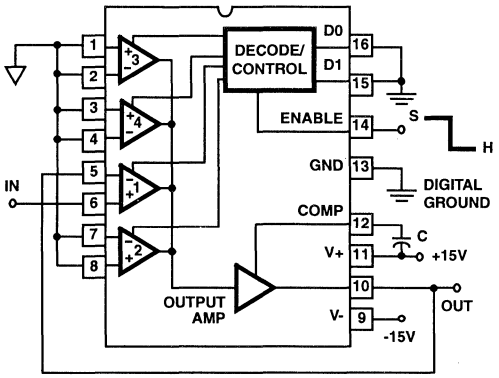


FIGURE 1. HA-2406 AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN



Sample Charging Rate $= \frac{I_1}{C} V/s$

Hold Drift Rate $= \frac{I_2}{C} V/s$

Switch Pedestal Error $= \frac{Q}{C} V$

$I_1 \approx 150 \times 10^{-6} A$

$I_2 \approx 200 \times 10^{-9} A$ at $25^{o}C$

$\approx 600 \times 10^{-9} A$ at $-55^{o}C$

$\approx 100 \times 10^{-9} A$ at $125^{o}C$

$Q \approx 2 \times 10^{-12} C$

FIGURE 2. HA-2406 SAMPLE AND HOLD

For more examples, see Harris Application Note AN514.

Typical Performance Curves

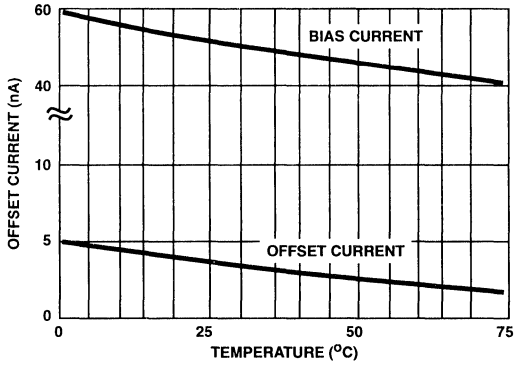


FIGURE 3. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

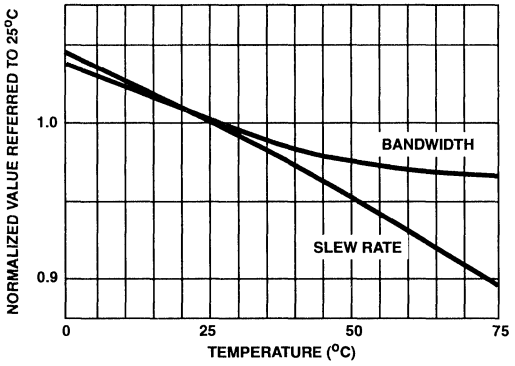


FIGURE 4. NORMALIZED AC PARAMETERS vs TEMPERATURE

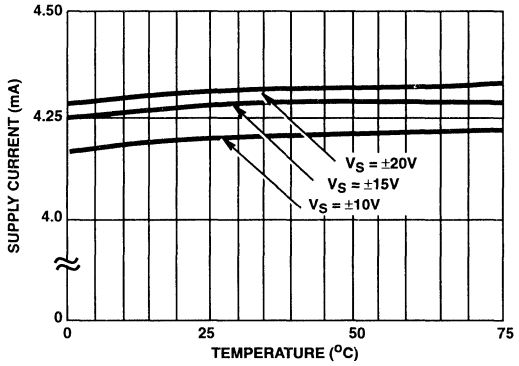


FIGURE 5. POWER SUPPLY CURRENT vs TEMPERATURE

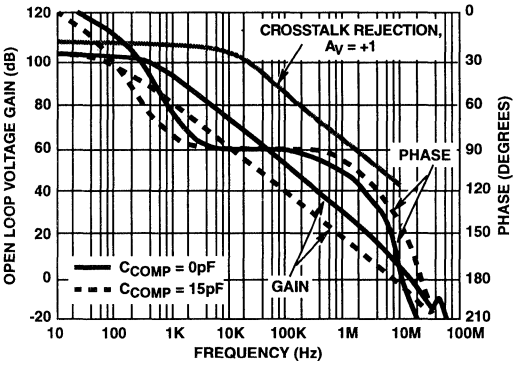


FIGURE 6. OPEN LOOP FREQUENCY AND PHASE RESPONSE

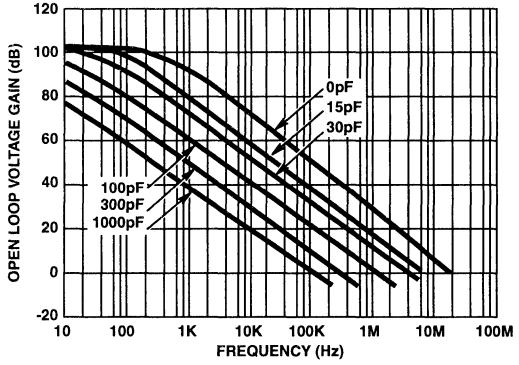


FIGURE 7. FREQUENCY RESPONSE vs C_{COMP}

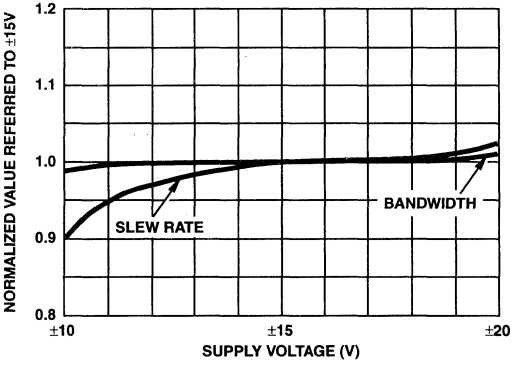


FIGURE 8. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

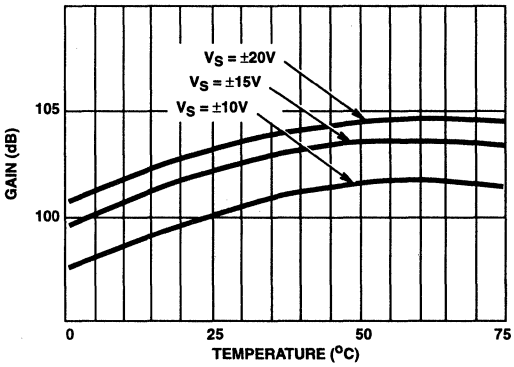


FIGURE 9. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

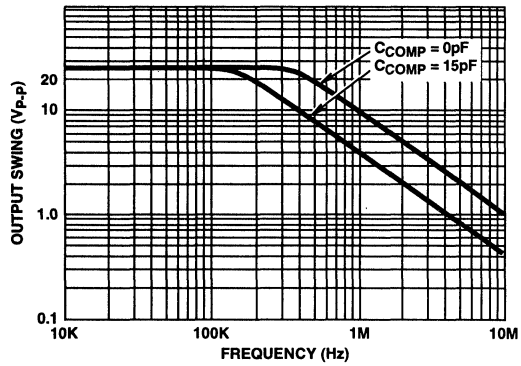


FIGURE 10. OUTPUT VOLTAGE SWING vs FREQUENCY

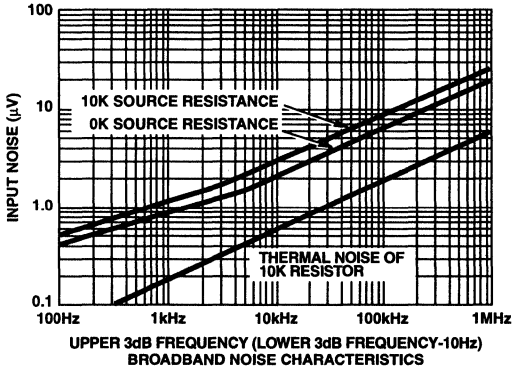


FIGURE 11. EQUIVALENT INPUT NOISE vs BANDWIDTH

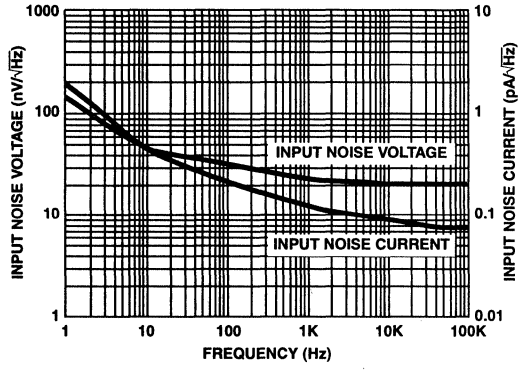


FIGURE 12. INPUT NOISE vs FREQUENCY

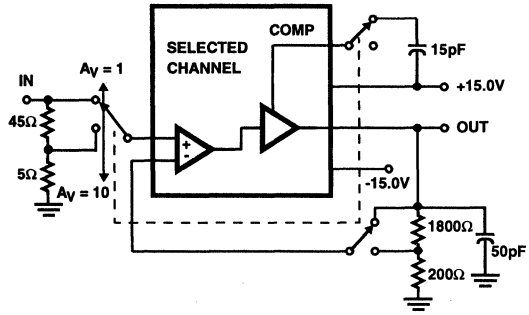


FIGURE 13. SLEW RATE AND TRANSIENT RESPONSE

Complete data sheet available via web, Harris' home page: http://www.semi.harris.com/ Or via Harris AnswerFAX, see Section 12

HA-2444

50MHz, Selectable, Four Channel Video Operational Amplifier

November 1996

Features

- Digital Selection of Input Channel
- Unity Gain Stability
- Gain Flatness to 10MHz. 0.1dB
- Differential Gain 0.03%
- Differential Phase. . . . . 0.03 Degrees
- Fast Channel Selection 60ns
- Crosstalk Rejection 60dB

Applications

- Video Multiplexer
- Programmable Gain Amplifier
- Special Effects Processors
- Video Distribution Systems
- Heads-up/Night Vision Displays
- Medical Imaging Systems
- Radar Video

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HA3-2444-5	0 to 75	16 Ld PDIP	E16.3
HA3-2444-9	-40 to 85	16 Ld PDIP	E16.3
HA9P2444-5	0 to 75	16 Ld SOIC	M16.3
HA9P2444-9	-40 to 85	16 Ld SOIC	M16.3

Description

The HA-2444 is a channel-selectable video op amp consisting of four differential inputs, a single-ended output, and digital control circuitry allowing two digital inputs to activate one of the four differential inputs. The HA-2444 also includes a high impedance output state allowing the outputs of multiple HA-2444s to be wire-OR'd. Functionally, the HA-2444 is equivalent to four wideband video op amps and a wideband multiplexer.

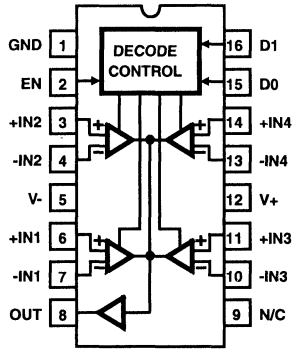
Unlike similar competitor devices, the HA-2444 is not restricted to multiplexing. Any op amp configuration can be used with any of the inputs. Signal amplification, addition, integration, and more can be put under digital control with broadcast quality performance.

The key video parameters of the HA-2444 have been optimized without compromising DC performance. Gain Flatness to 10MHz is only 0.1dB. Differential gain and phase are typically 0.03% and 0.03 degrees, respectively. Laser trimming allows offset voltages in the 4.0mV range and a unique common current source design assures minimal channel-to-channel mismatch, while maintaining 60dB of crosstalk rejection at 5MHz. Open loop gain of 76dB and low input offset and bias currents enhance the performance of this versatile device.

For information about military grade devices, please refer to the HA-2444/883 data sheet.

Pinout

HA-2444
(PDIP, SOIC)
TOP VIEW



Logic Operation

TRUTH TABLE

EN	D1	D0	SELECTED CHANNEL
H	L	L	1
H	L	H	2
H	H	L	3
H	H	H	4
L	X	X	NONE-OUT is set to a high impedance state.

L = Low State (0.8V Max)
H = High State (2.4V Min)
X = Don't Care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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HARRIS SEMICONDUCTOR

HA-2500, HA-2502, HA-2505

12MHz, High Input Impedance, Operational Amplifiers

November 1996

Features

- Slew Rate 30V/µs
- Fast Settling 330ns
- Full Power Bandwidth 500kHz
- Gain Bandwidth 12MHz
- High Input Impedance 50MΩ
- Low Offset Current 10nA
- Internally Compensated For Unity Gain Stability

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators

Ordering Information

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. NO.
HA2-2500-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2502-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2505-5	0 to 75	8 Pin Metal Can	T8.C
HA3-2505-5	0 to 75	8 Ld PDIP	E8.3
HA7-2500-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2505-5	0 to 75	8 Ld CERDIP	F8.3A

Description

HA-2500, HA-2502, HA-2505 comprises a series of operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

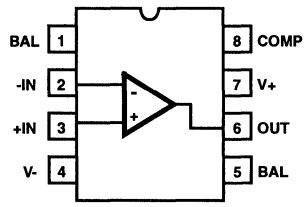
These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, RF, video, and pulse conditioning circuits. Slew rates of ±30V/µs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12MHz small signal bandwidth and 500kHz power bandwidth make these devices well suited to RF and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500, HA-2502, HA-2505 are particularly useful components in signal conditioning designs.

The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

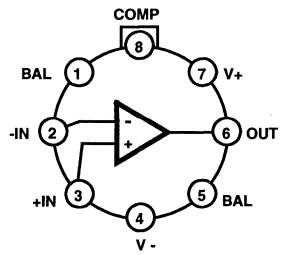
MIL-STD-883 product and data sheets are available upon request.

Pinouts

HA-2500/02 (CERDIP)
HA-2505 (PDIP, CDIP)
TOP VIEW



HA-2500/02/05
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2890.2**

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 40V
Differential Input Voltage. 15V
Peak Output Current. 50mA

Operating Conditions

Temperature Range
HA-2500/2502-2 . . . . . -55°C to 125°C
HA-2505-5. . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	165	80
PDIP Package	96	N/A
CERDIP Package	135	50

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_S = \pm 15V$

PARAMETER	TEMP (°C)	HA-2500-2			HA-2502-2			HA-2505-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	25	-	2	5	-	4	8	-	4	8	mV
	Full	-	-	8	-	-	10	-	-	10	mV
Offset Voltage Average Drift	Full	-	20	-	-	20	-	-	20	-	µV/°C
Bias Current	25	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	25	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 2)	25	25	50	-	20	50	-	20	50	-	MΩ
Common Mode Range	Full	±10	-	-	±10	-	-	±10	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 3, 6)	25	20	30	-	15	25	-	15	25	-	kV/V
	Full	15	-	-	10	-	-	10	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth Product (Note 5)	25	-	12	-	-	12	-	-	12	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 6)	25	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Notes 6, 11)	25	350	500	-	300	500	-	300	500	-	kHz
TRANSIENT RESPONSE											
Rise Time (Notes 3, 7, 8, 9)	25	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 3, 7, 8, 9)	25	-	25	40	-	25	50	-	25	50	%
Slew Rate (Notes 3, 7, 9, 12)	25	±25	±30	-	±20	±30	-	±20	±30	-	V/µs
Settling Time to 0.1% (Notes 3, 7, 9, 12)	25	-	0.33	-	-	0.33	-	-	0.33	-	µs

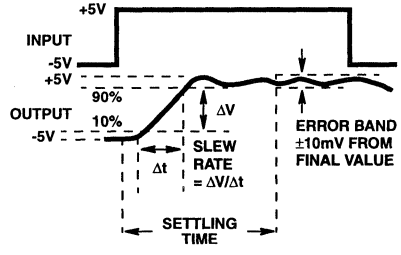
Electrical Specifications $V_S = \pm15V$ (Continued)

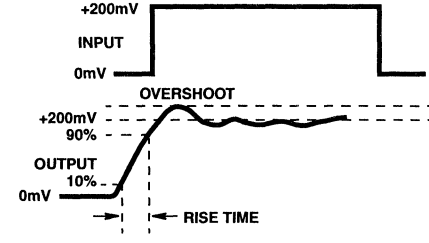
PARAMETER	TEMP (°C)	HA-2500-2			HA-2502-2			HA-2505-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS											
Supply Current	25	-	4	6	-	4	6	-	4	6	mA
PSRR (Note 10)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

2. This parameter value is based on design calculations.
3. $R_L = 2k\Omega$.
4. $V_{CM} = \pm10V$.
5. $A_V > 10$.
6. $V_O = \pm10V$.
7. $C_L = 50pF$.
8. $V_O = \pm200mV$.
9. See Transient Response Test Circuits and Waveforms.
10. $\Delta V = \pm5V$.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/$2\pi V_{PEAK}$.
12. $V_{OUT} = \pm5V$.

Test Circuits and Waveforms

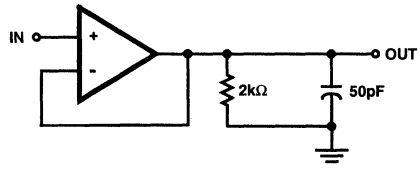




NOTE: Measured on both positive and negative transitions from 0V to +200mv and 0V to -200mV at the output.

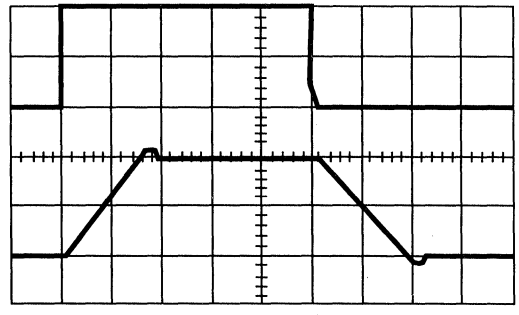
FIGURE 1. SLEW RATE AND SETTLING TIME

FIGURE 2. TRANSIENT RESPONSE



NOTE: Measured on both positive and negative transitions from 0V to +200mv and 0V to -200mV at the output.

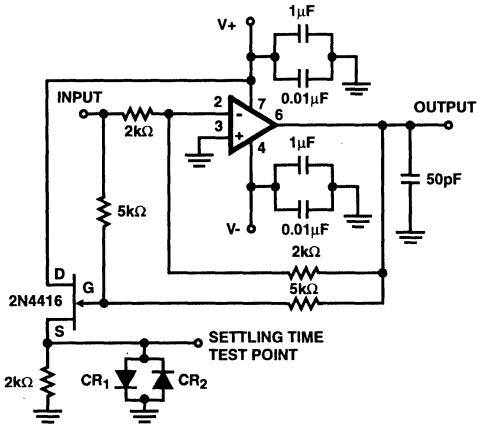
FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE



$R_L = 2k\Omega$, $C_L = 50pF$ Vertical = 5V/Div.
Upper Trace: Input Horizontal = 200ns/Div.
Lower Trace: Output $T_A = 25°C$, $V_S = \pm15V$

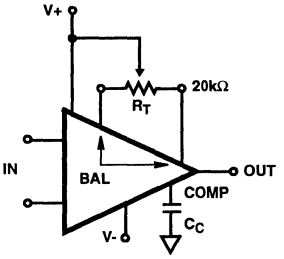
FIGURE 4. VOLTAGE FOLLOWER PULSE RESPONSE

Test Circuits and Waveforms (Continued)



13. $A_V = -1$.
14. Feedback and Summing Resistor Ratios should be 0.1% matched.
15. Clipping Diodes CR_1 and CR_2 are optional. HP5082-2810 recommended.

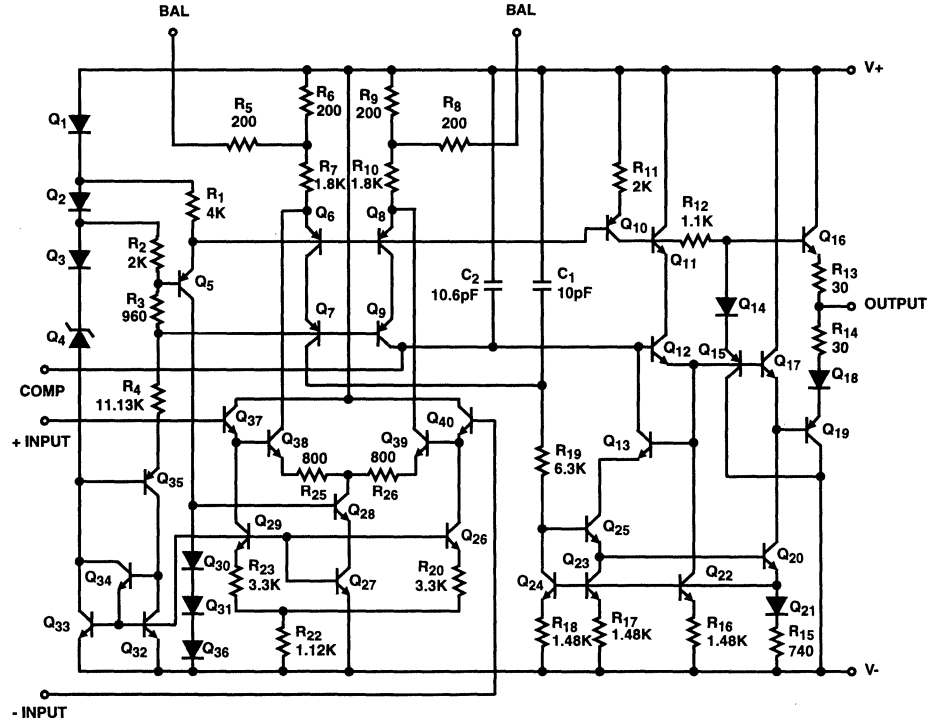
FIGURE 5. SETTLING TIME TEST CIRCUIT



NOTE: Tested offset adjustment range is $|V_{OS}| + 1mV|$ minimum referred to output. Typical ranges are ±6mV with $R_T = 20k\Omega$.

FIGURE 6. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Schematic



Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$, Unless Otherwise Specified

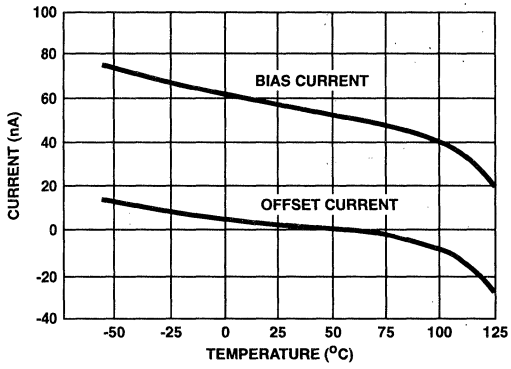


FIGURE 7. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

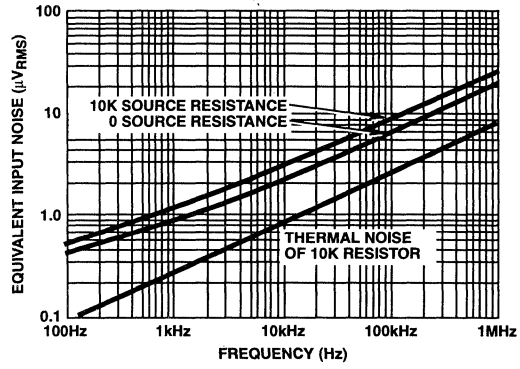


FIGURE 8. EQUIVALENT INPUT NOISE vs BANDWIDTH (WITH 10Hz HIGH PASS FILTER)

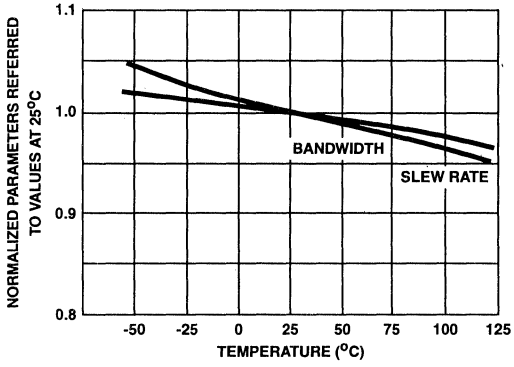


FIGURE 9. NORMALIZED AC PARAMETERS vs TEMPERATURE

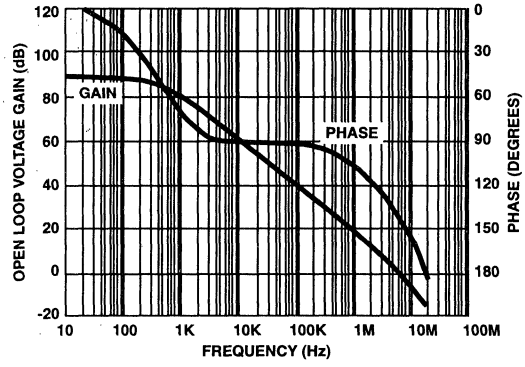


FIGURE 10. OPEN LOOP FREQUENCY AND PHASE RESPONSE

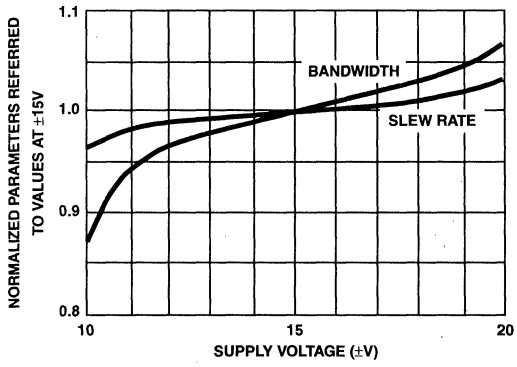
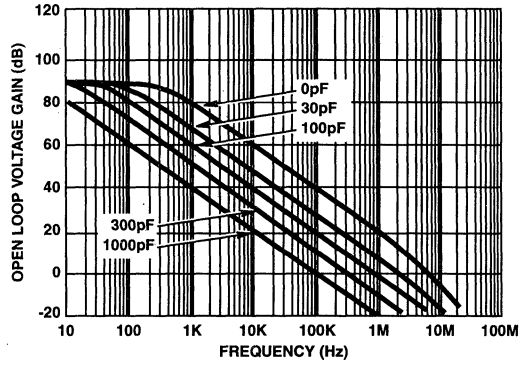


FIGURE 11. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE



NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

FIGURE 12. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

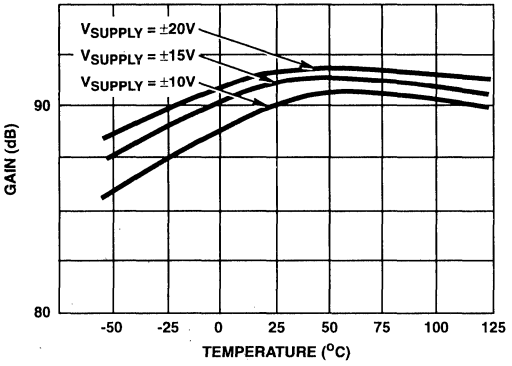


FIGURE 13. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

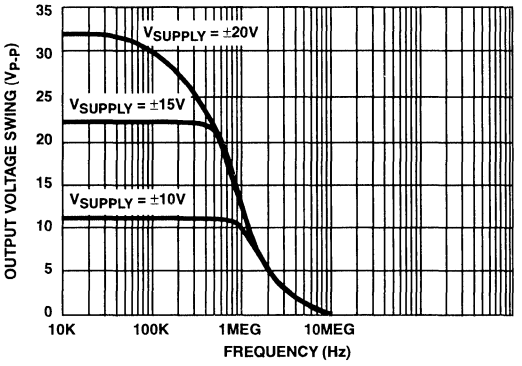


FIGURE 14. OUTPUT VOLTAGE SWING vs FREQUENCY

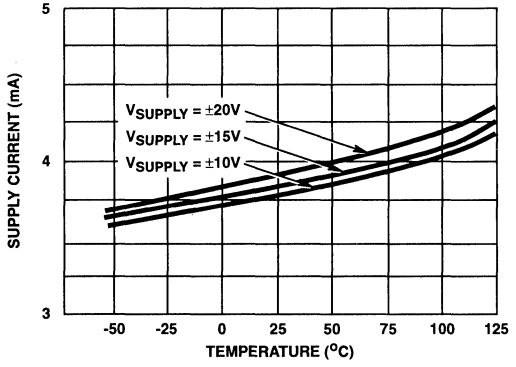


FIGURE 15. POWER SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

57 mils x 65 mils x 19 mils
1450µm x 1650µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

PASSIVATION:

Type: Nitride (Si3N4) over Silox (SiO2, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

TRANSISTOR COUNT:

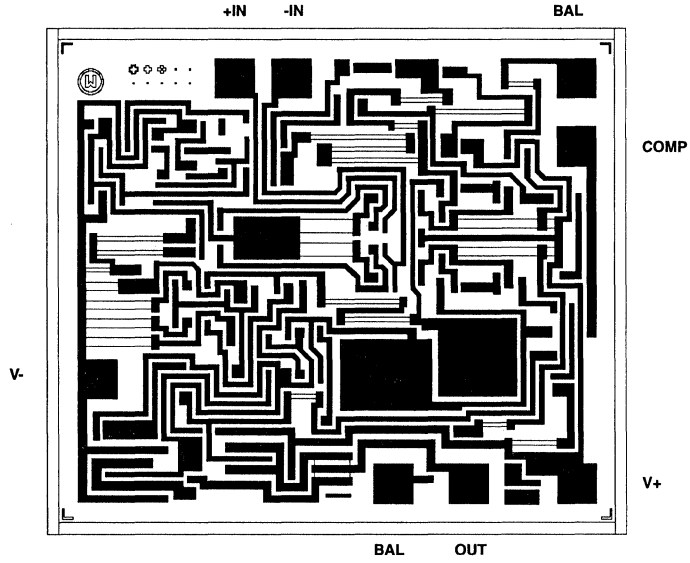
40

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2500, HA-2502



HA-2510, HA-2512, HA-2515

12MHz, High Input Impedance, Operational Amplifiers

November 1996

Features

- Slew Rate 60V/µs
- Fast Settling 250ns
- Full Power Bandwidth 1MHz
- Gain Bandwidth 12MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA
- Internally Compensated for Unity Gain Stability

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

HA-2510/12/15 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidths for internally compensated devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The ±60V/µs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/12/15's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in RF and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

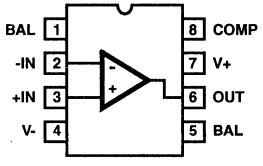
MIL-STD-883 product and data sheets available upon request.

Ordering Information

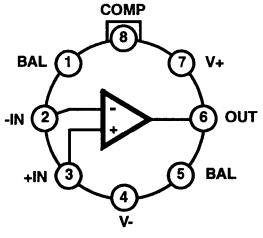
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2510-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2512-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2515-5	0 to 75	8 Pin Metal Can	T8.C
HA3-2515-5	0 to 75	8 Ld PDIP	E8.3
HA7-2510-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2512-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2515-5	0 to 75	8 Ld CERDIP	F8.3A

Pinouts

HA-2510/12 (CERDIP)
HA-2515 (PDIP, CERDIP)
TOP VIEW



HA-2510/12/15
(METAL CAN)
TOP VIEW



3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **2893.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage. 15V
Peak Output Current. 50mA

Operating Conditions

Temperature Range
HA-2510/12-2 . . . . . -55°C to 125°C
HA-2515-5. . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	165	80
PDIP Package	96	N/A
CERDIP Package	135	50

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 15V$

PARAMETER	TEMP (°C)	HA-2510-2			HA-2512-2			HA-2515-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	25	-	4	8	-	5	10	-	5	10	mV
	Full	-	-	11	-	-	14	-	-	14	mV
Offset Voltage Average Drift	Full	-	20	-	-	25	-	-	30	-	µV/°C
Bias Current	25	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	25	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 2)	25	50	100	-	40	100	-	40	100	-	MΩ
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 3, 6)	25	10	15	-	7.5	15	-	7.5	15	-	kV/V
	Full	7.5	-	-	5	-	-	5	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth Product (Note 5)	25	-	12	-	-	12	-	-	12	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3)	Full	±10.0	±12.0	-	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current (Note 6)	25	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Notes 6, 11)	25	750	1000	-	600	1000	-	600	1000	-	kHz
TRANSIENT RESPONSE											
Rise Time (Notes 3, 7, 8, 9)	25	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 3, 7, 8, 9)	25	-	25	40	-5	25	50	-	25	50	%
Slew Rate (Notes 3, 7, 9, 12)	25	±50	±65	-	±40	±60	-	±40	±60	-	V/µs
Settling Time to 0.1% (Notes 3, 7, 9, 12)	25	-	0.25	-	-	0.25	-	-	0.25	-	µs

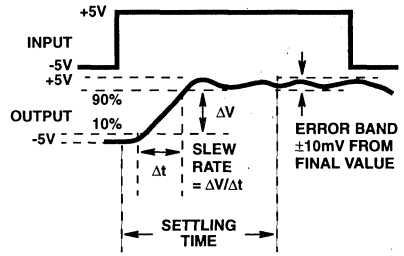
Electrical Specifications $V_{SUPPLY} = \pm15V$ (Continued)

PARAMETER	TEMP (°C)	HA-2510-2			HA-2512-2			HA-2515-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS											
Supply Current	25	-	4	6	-	4	6	-	4	6	mA
Power Supply Rejection Ratio (Note 10)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

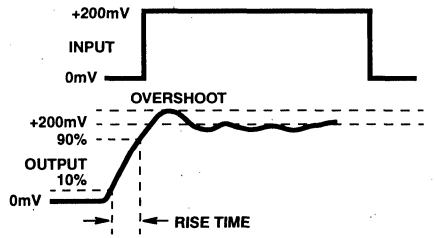
2. This parameter value is based on design calculations.
3. $R_L = 2k\Omega$.
4. $V_{CM} = \pm10V$
5. $A_V > 10$.
6. $V_O = \pm10V$.
7. $C_L = 50pF$.
8. $V_O = \pm200mV$.
9. See Transient Response Test Circuits and Waveforms.
10. $\Delta V = \pm5V$.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/$2\pi V_{PEAK}$.
12. $V_{OUT} = \pm5V$.

Test Circuits and Waveforms



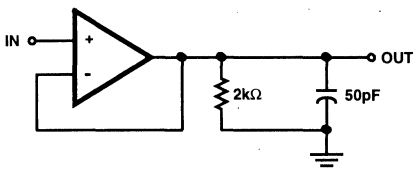
NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 1. SLEW RATE AND SETTLING TIME



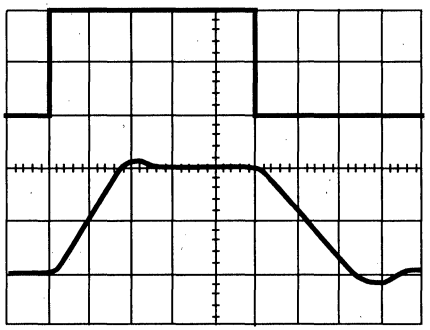
NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 2. TRANSIENT RESPONSE



NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

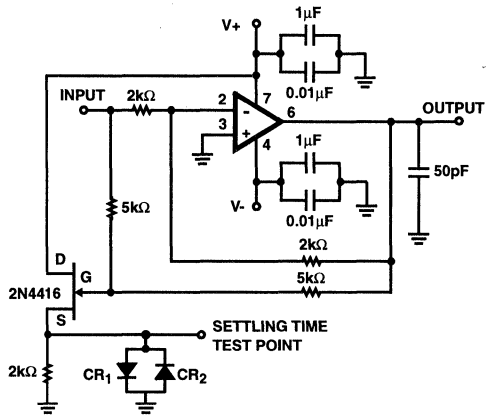
FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE

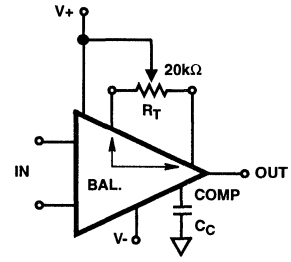


$R_L = 2k\Omega$, $C_L = 50pF$ Vertical = 5V/Div.
Upper Trace: Input Horizontal = 200ns/Div.
Lower Trace: Output $T_A = 25°C$, $V_S = \pm15V$

FIGURE 4. VOLTAGE FOLLOWER PULSE RESPONSE

Test Circuits and Waveforms (Continued)





NOTES:

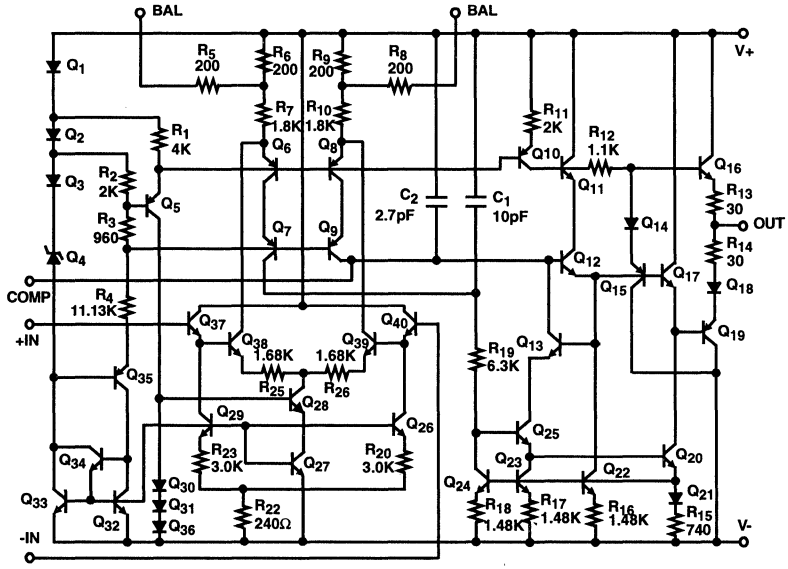
13. $A_V = -1$.
14. Feedback and summing resistor ratios should be 0.1% matched.
15. Clipping diodes CR_1 and CR_2 are optional. HP5082-2810 recommended.

FIGURE 5. SETTLING TIME TEST CIRCUIT

NOTE: Tested offset adjustment range is IVOS + 1mVI minimum referred to output. Typical ranges are ±6mV with $R_T = 20k\Omega$.

FIGURE 6. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Schematic



Typical Performance Curves

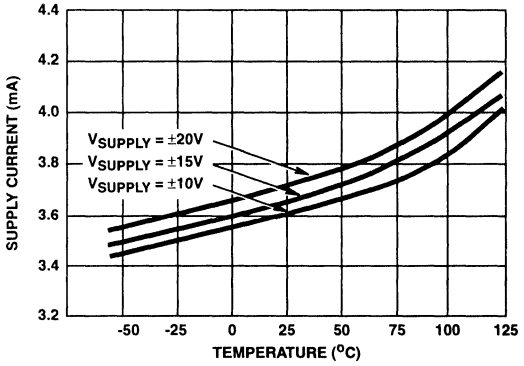


FIGURE 7. POWER SUPPLY CURRENT vs TEMPERATURE

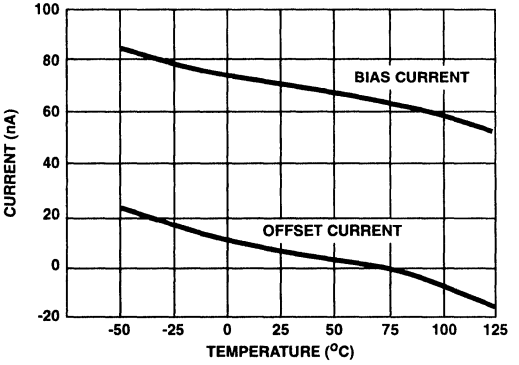


FIGURE 8. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

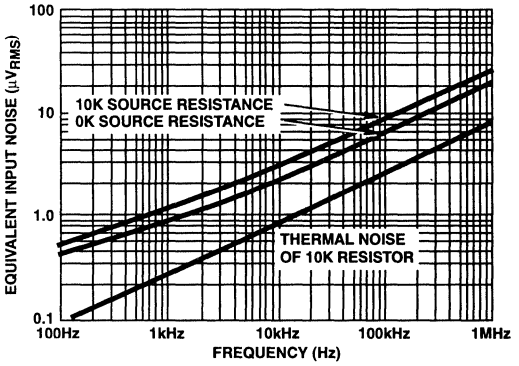


FIGURE 9. EQUIVALENT INPUT NOISE vs BANDWIDTH (WITH 10Hz HIGH PASS FILTER)

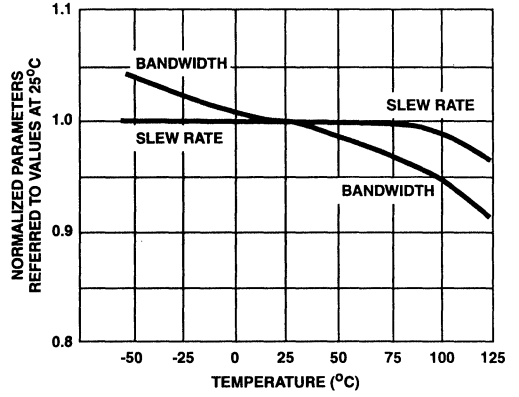


FIGURE 10. NORMALIZED AC PARAMETERS vs TEMPERATURE

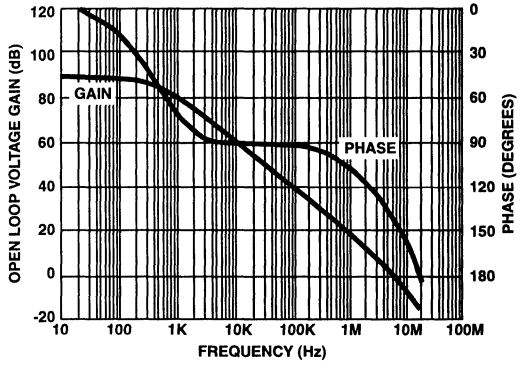


FIGURE 11. OPEN LOOP GAIN AND PHASE RESPONSE

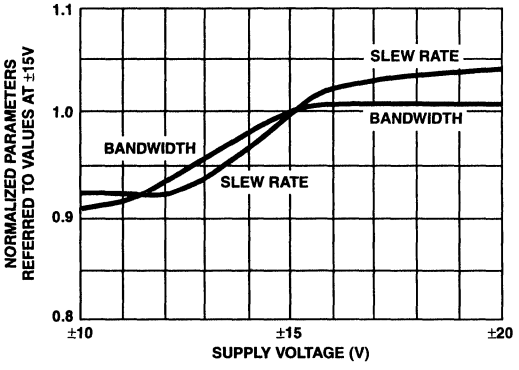


FIGURE 12. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT 25°C

Typical Performance Curves (Continued)

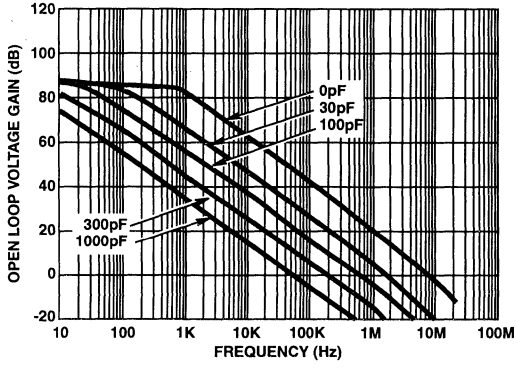


FIGURE 13. OPEN LOOP GAIN RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

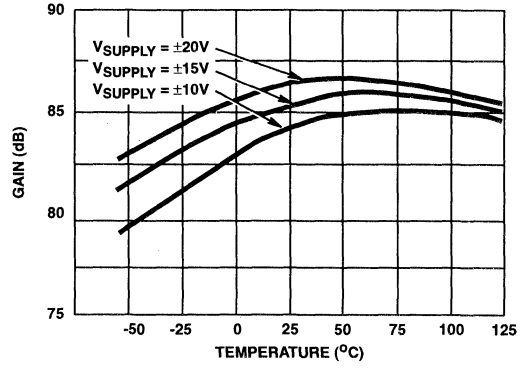


FIGURE 14. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

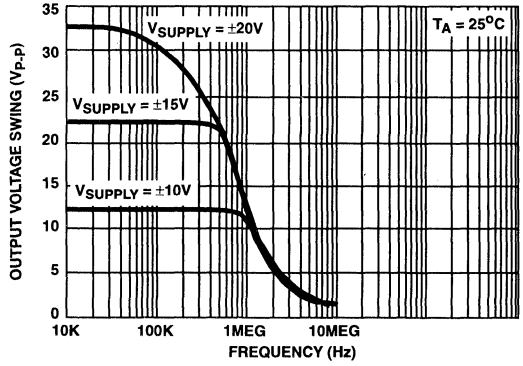


FIGURE 15. OUTPUT VOLTAGE SWING vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

65 mils x 57 mils x 19 mils
1650µm x 1450µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

TRANSISTOR COUNT:

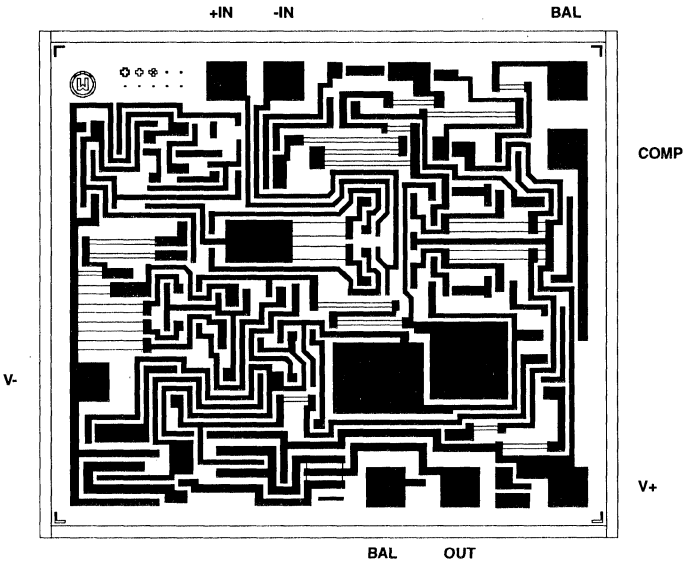
40

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2510, HA-2512, HA-2515



HARRIS SEMICONDUCTOR

HA-2520, HA-2522, HA-2525

20MHz, High Slew Rate, Uncompensated, High Input Impedance, Operational Amplifiers

November 1996

Features

- High Slew Rate 120V/µs
- Fast Settling 200ns
- Full Power Bandwidth 2MHz
- Gain Bandwidth ($A_V \geq 3$) 20MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

HA-2520/2522/2525 comprise a series of operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at close loop gains greater than 3 without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

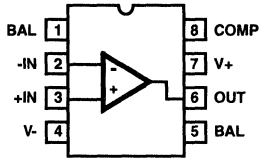
120V/µs slew rate and 200ns (0.2%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for RF and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complemented by 10nA offset current, 100MΩ input impedance and offset trim capability. MIL-STD-883 product and data sheets are available upon request.

Ordering Information

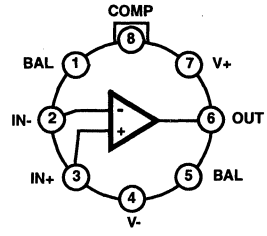
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2520-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2522-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2525-5	0 to 75	8 Pin Metal Can	T8.C
HA3-2525-5	0 to 75	8 Ld PDIP	E8.3
HA4P2525-5	0 to 75	20 Ld PLCC	N20.35
HA7-2520-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2522-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2525-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P2525-5 (H25255)	0 to 75	8 Ld SOIC	M8.15

Pinouts

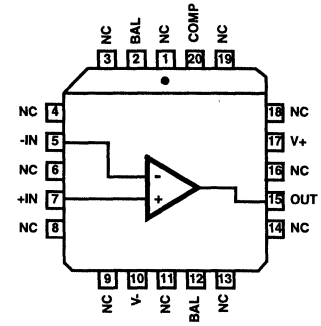
HA-2520/22 (CERDIP)
HA-2525 (PDIP, CERDIP, SOIC)
TOP VIEW



HA-2520/22/25
(METAL CAN)
TOP VIEW



HA-2525
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2894.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 40V
Differential Input Voltage 15V
Output Current 50mA

Operating Conditions

Temperature Range
HA-2520/2522-2 . . . . . -55°C to 125°C
HA-2525-5 . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	165	80
PDIP Package	96	N/A
CERDIP Package	135	50
PLCC Package	74	N/A
SOIC Package	157	N/A

Maximum Junction Temperature (Hermetic Packages) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 15V$

PARAMETER	TEMP (°C)	HA-2520-2			HA-2522-2			HA-2525-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	25	-	4	8	-	5	10	-	5	10	mV
	Full	-	-	11	-	-	14	-	-	14	mV
Offset Voltage Drift	Full	-	20	-	-	25	-	-	30	-	µV/°C
Bias Current	25	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	25	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 2)	25	50	100	-	40	100	-	40	100	-	MΩ
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 3, 6)	25	10	15	-	7.5	15	-	7.5	15	-	kV/V
	Full	7.5	-	-	5	-	---	5	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth (Notes 2, 5)	25	10	20	-	10	20	-	10	20	-	MHz
Minimum Stable Gain	25	3	-	-	3	-	-	3	-	-	V/V
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3)	Full	±10.0	±12.0	-	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current (Note 6)	25	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Notes 6, 11)	25	1.5	2.0	-	1.2	2.0	-	1.2	2.0	-	MHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 3, 7, 8, 10)	25	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 3, 7, 8, 10)	25	-	25	40	-	25	50	-	25	50	%
Slew Rate (Notes 3, 7, 10, 12)	25	±100	±120	-	±80	±120	-	±80	±120	-	V/µs
Settling Time (Notes 3, 7, 10, 12)	25	-	0.20	-	-	0.20	-	-	0.20	-	µs

Electrical Specifications $V_{SUPPLY} = \pm15V$ (Continued)

PARAMETER	TEMP (°C)	HA-2520-2			HA-2522-2			HA-2525-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS											
Supply Current	25	-	4	6	-	4	6	-	4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

2. This parameter value is based on design calculations.
3. $R_L = 2k\Omega$.
4. $V_{CM} = \pm10V$.
5. $A_V > 10$.
6. $V_O = \pm10.0V$.
7. $C_L = 50pF$.
8. $V_O = \pm200mV$.
9. $\Delta V = \pm5.0V$.
10. See Transient Response Test Circuits and Waveforms.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
12. $V_{OUT} = \pm5V$.

Test Circuits and Waveforms

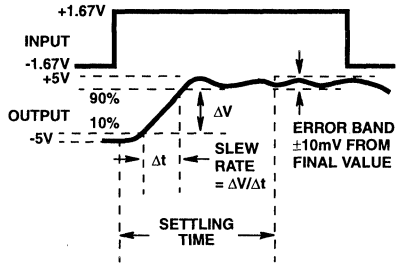
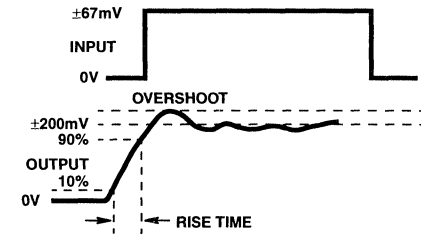


FIGURE 1. SLEW RATE AND SETTLING TIME



NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 2. TRANSIENT RESPONSE

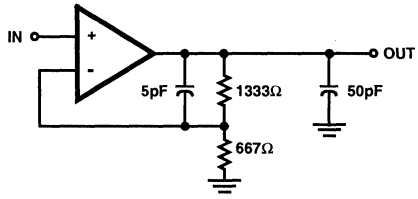
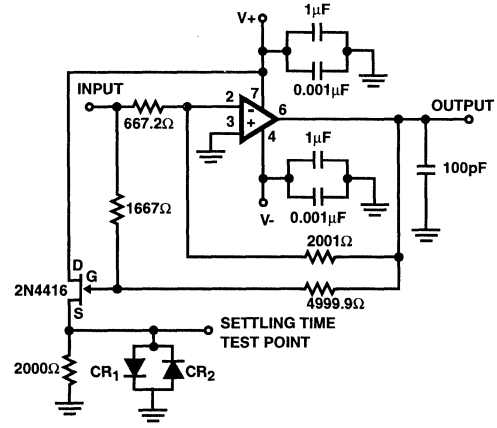


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE

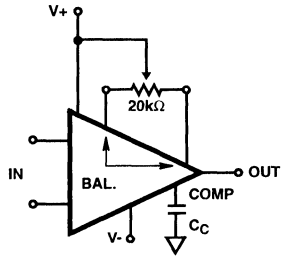


NOTES:

13. $A_V = -3$.
14. Feedback and summing resistor ratios should be 0.1% matched.
15. Clipping diodes CR_1 and CR_2 are optional. HP5082-2810 recommended.

FIGURE 4. SETTLING TIME TEST CIRCUIT

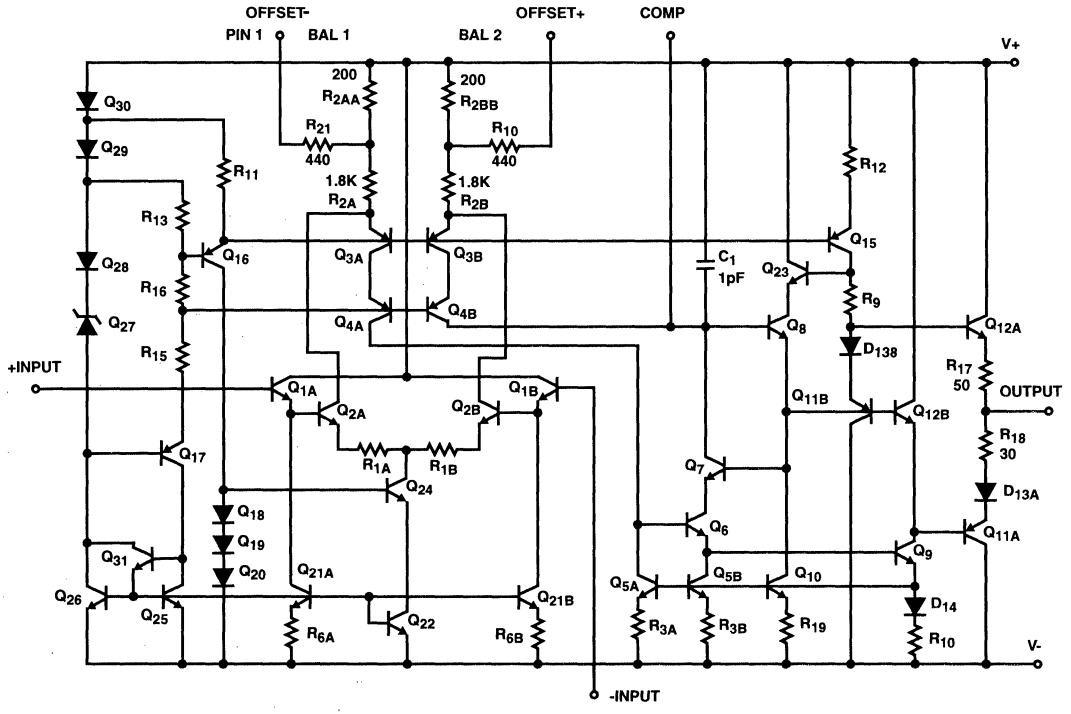
Test Circuits and Waveforms (Continued)



NOTE: Tested offset adjustment range is $|V_{OS}|$ + 1mV| minimum referred to output. Typical ranges are ±20mV with R_T = 20kΩ.

FIGURE 5. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP

Schematic Diagram



Typical Application

Inverting Unity Gain Circuit

Figure 6 shows a Compensation Circuit for an inverting unity gain amplifier. The circuit was tested for functionality with supply voltages from ±4V to ±15V, and the performance as tested was: Slew Rate ≈ 120V/µs; Bandwidth ≈ 10MHz; and Settling Time (0.1%) ≈ 500ns. Figure 7 illustrates the amplifier's frequency response, and it is important to note that capacitance at pin 8 must be minimized for maximum bandwidth.

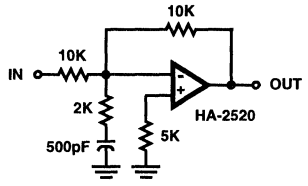


FIGURE 6. INVERTING UNITY GAIN CIRCUIT

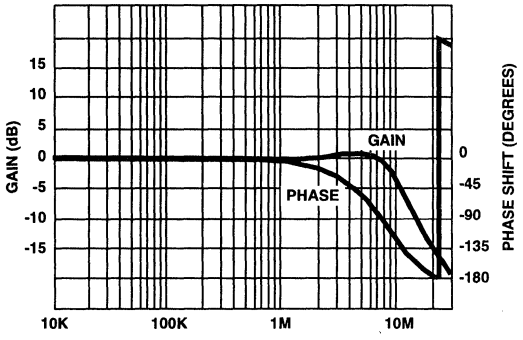


FIGURE 7. FREQUENCY RESPONSE FOR INVERTING UNITY GAIN CIRCUIT

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified

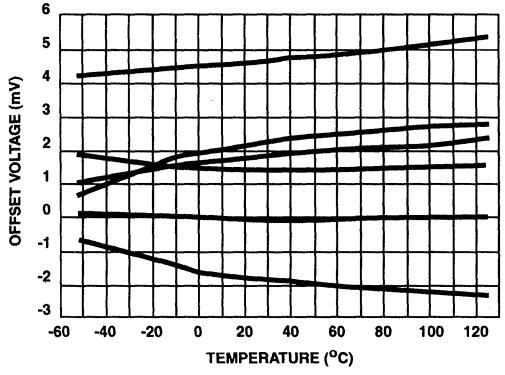


FIGURE 8. OFFSET VOLTAGE vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS)

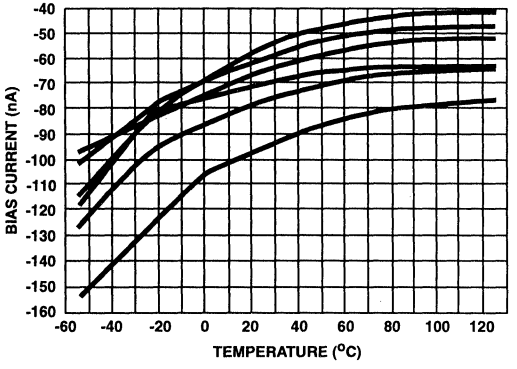


FIGURE 9. BIAS CURRENT vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS)

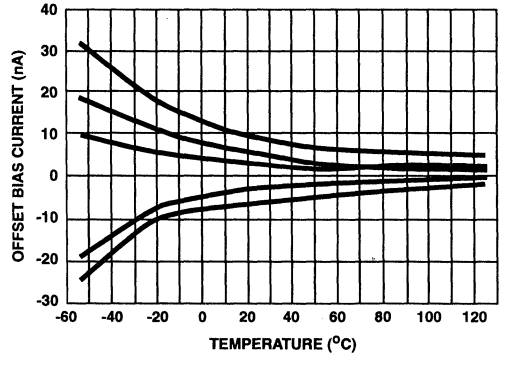


FIGURE 10. OFFSET CURRENT vs TEMPERATURE (5 TYPICAL UNITS FROM 3 LOTS)

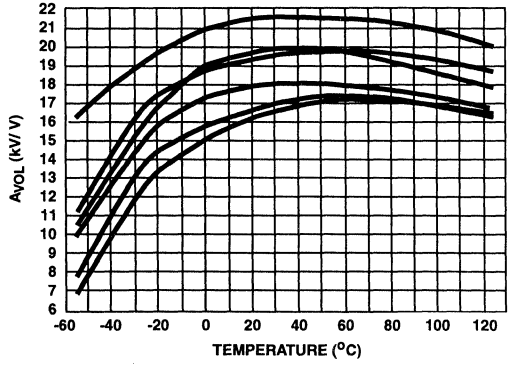


FIGURE 11. OPEN LOOP GAIN vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS)

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

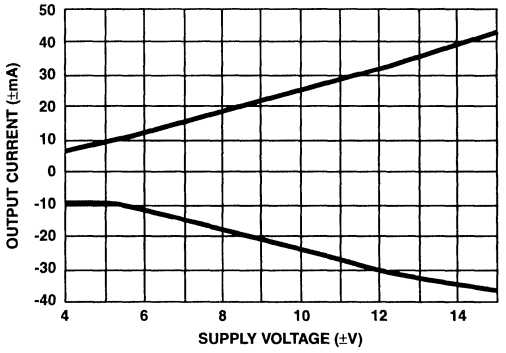


FIGURE 12. OUTPUT CURRENT vs SUPPLY VOLTAGE

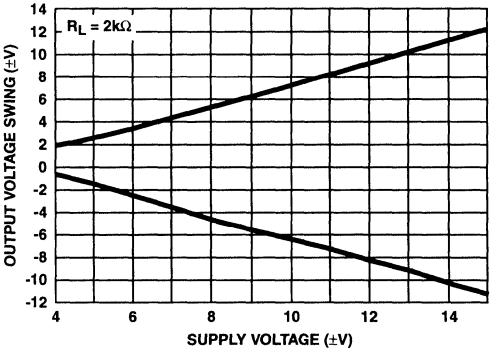


FIGURE 13. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

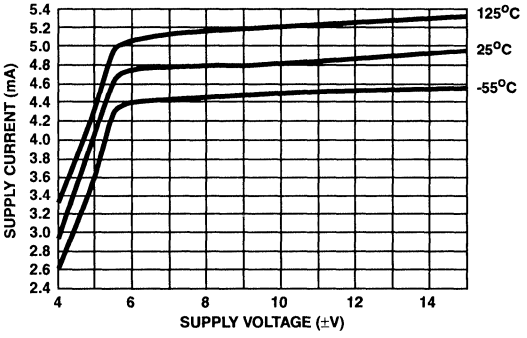


FIGURE 14. SUPPLY CURRENT vs SUPPLY VOLTAGE

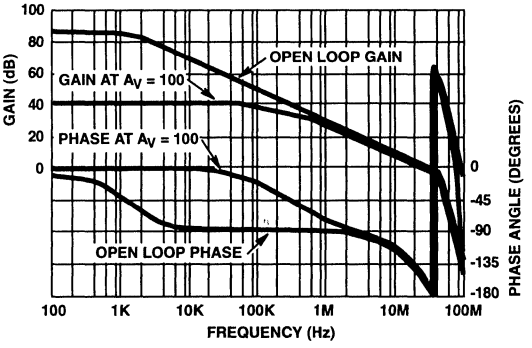


FIGURE 15. FREQUENCY RESPONSE

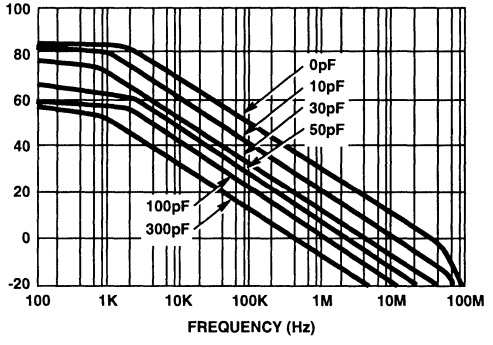


FIGURE 16. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMP PIN TO GROUND

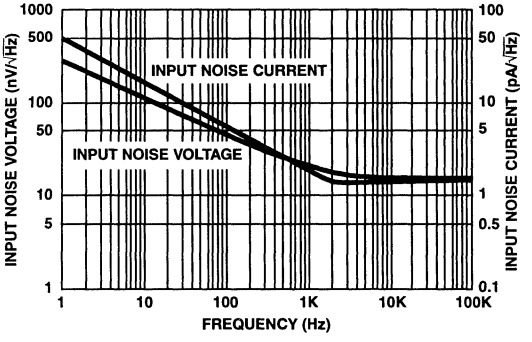


FIGURE 17. INPUT NOISE CHARACTERISTICS

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

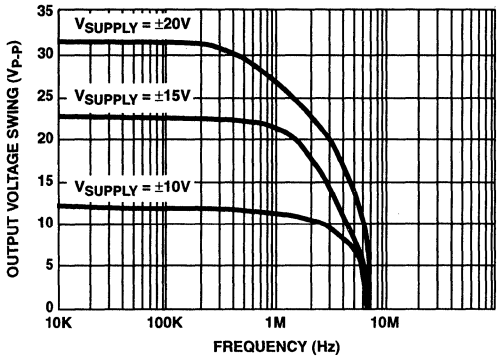


FIGURE 18. OUTPUT VOLTAGE SWING vs FREQUENCY

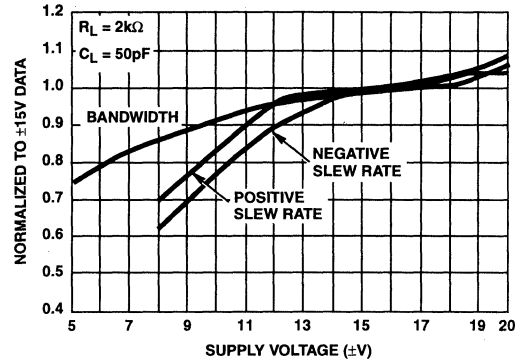


FIGURE 19. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

67 mils x 57 mils x 19 mils
(1700µm x 1440µm x 483µm)

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

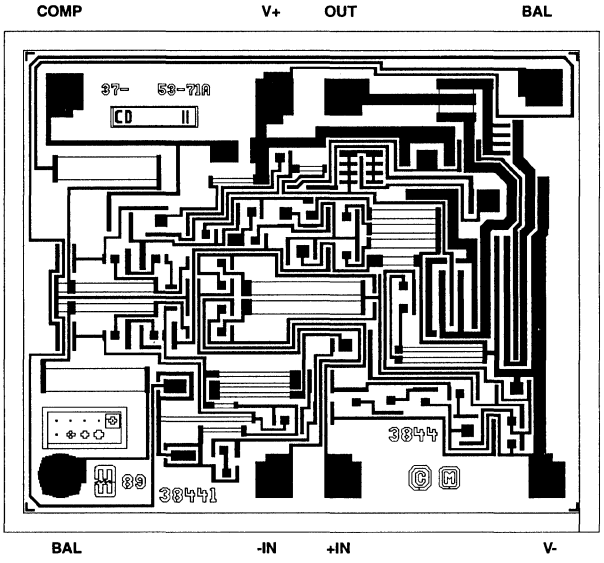
40

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2520, HA-2522, HA-2525



NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

HA-2529

November 1996

20MHz, High Input Impedance, High Slew Rate Operational Amplifier

Features

- High Slew Rate 150V/μs
- Fast Settling 200ns
- Full Power Bandwidth 2MHz
- Gain Bandwidth ($A_V \geq 3$) 20MHz
- High Input Impedance 130MΩ
- Low Offset Current 5nA
- High Output Current . . . . . ±30mA

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2529-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2529-5	0 to 75	8 Pin Metal Can	T8.C
HA3-2529-5	0 to 75	8 Ld PDIP	E8.3
HA7-2529-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P2529-5 (H25295)	0 to 75	8 Ld SOIC	M8.15

Description

The HA-2529 is a monolithic operational amplifier which typifies excellence of design. With a design based on years of experience coupled with the reliable dielectric isolation process, this amplifier provides an outstanding combination of DC and AC parameters at closed loop gains greater than 3.

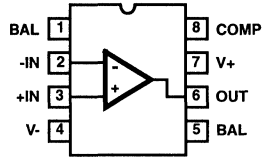
The HA-2529 offers 150V/μs slew rate and fast settling time (200ns), while consuming a mere 6mA of quiescent current, making this amplifier ideal for video circuitry and data acquisition designs. With 20MHz gain bandwidth combined with 7.5kV/V open loop gain, the HA-2529 is an ideal component for demanding signal conditioning designs. This device provides ±30mA output current drive with an output voltage swing of ±10V making it suited for pulse amplifier and RF amplifier components.

The HA-2529 will upgrade output current, slew rate, offset voltage drift and offset current drift in systems presently using the HA-2520/22/25 or EHA-2520/22/25.

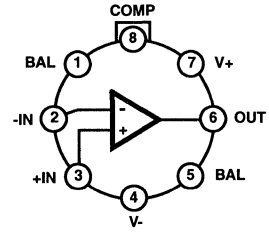
MIL-STD-883 product and data sheets are available upon request.

Pinouts

HA-2529
(PDIP, CERDIP, SOIC)
TOP VIEW



HA-2529
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2895.2**

HARRIS SEMICONDUCTOR

HA-2539

600MHz, Very High Slew Rate Operational Amplifier

November 1996

Features

- Very High Slew Rate 600V/μs
- Open Loop Gain 15kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Power Bandwidth 9.5MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... ±10V
- Monolithic Bipolar Dielectric Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-2539-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-2539-5	0 to 75	14 Ld CERDIP	F14.3
HA3-2539-5	0 to 75	14 Ld PDIP	E14.3
HA3-2539C-5	0 to 75	14 Ld PDIP	E14.3
HA9P2539-5	0 to 75	14 Ld SOIC	M14.15
HA9P2539-9	-40 to 85	14 Ld SOIC	M14.15

Description

The Harris HA-2539 represents the ultimate in high slew rate, wideband, monolithic operational amplifiers. It has been designed and constructed with the Harris High Frequency Bipolar Dielectric Isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/μs slew rate and a 600MHz gain bandwidth product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full ±10V swing coupled with outstanding AC parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

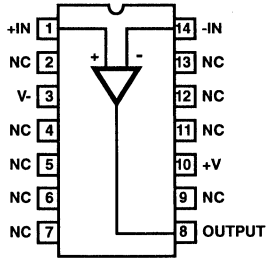
For further design assistance please refer to Application Note AN541 (Using the HA-2539 Very High Slew Rate Wideband Operational Amplifiers) and Application Note AN556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers.

For military grade product information, the HA-2539/883 data sheet is available upon request.

For a lower power version of this product, please see the HA-2839 and HA-2840 data sheets.

Pinout

HA-2539
(PDIP, CERDIP, SOIC)
TOP VIEW



NOTE: No-Connection (NC) leads may be tied to a ground plane for better isolation and heat dissipation.

3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number **2896.2**

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Peak Output Current 50mA
Continuous Output Current . . . . . $33mA_{RMS}$

Operating Conditions

Temperature Range
HA-2539-2 . . . . . -55^oC to 125^oC
HA-2539/2539C-5 . . . . . 0^oC to 75^oC
HA-2539-9 . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20
PDIP Package	107	N/A
SOIC Package	119	N/A

Maximum Internal Quiescent Power Dissipation (Note 1)
Maximum Junction Temperature (Ceramic Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Packages) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below 175^oC for the ceramic package and below 150^oC for the plastic packages. By using Application Note AN556 on Safe Operating Area equations, along with the thermal resistances, proper load conditions can be determined. Heat sinking is recommended above 75^oC.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

PARAMETER	TEMP. (^oC)	HA-2539-2			HA-2539-5, -9			HA-2539C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	25	-	8	10	-	8	15	-	8	15	mV
	Full	-	13	15	-	13	20	-	13	20	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	-	20	-	µV/°C
Bias Current	25	-	5	20	-	5	20	-	5	20	µA
	Full	-	-	25	-	-	25	-	-	25	µA
Offset Current	25	-	1	6	-	1	6	-	1	6	µA
	Full	-	-	8	-	-	8	-	-	8	µA
Input Resistance	25	-	10	-	-	10	-	-	10	-	kΩ
Input Capacitance	25	-	1	-	-	1	-	-	1	-	pF
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
Input Current Noise ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	25	-	6	-	-	6	-	-	6	-	pA/√Hz
Input Voltage Noise ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	25	-	6	-	-	6	-	-	6	-	nV/√Hz
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	25	10	15	-	10	15	-	7	10	-	kV/V
	Full	5	-	-	5	-	--	5	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	60	72	-	60	72	-	60	72	-	dB
Minimum Stable Gain	25	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth (Notes 5, 6)	25	-	600	-	-	600	-	-	600	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Notes 3, 10)	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
Output Current (Note 3)	25	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Resistance	25	-	30	-	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	25	8.7	9.5	-	8.7	9.5	-	8.7	9.5	-	MHz

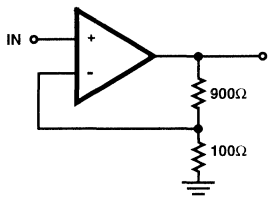
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

PARAMETER	TEMP. (°C)	HA-2539-2			HA-2539-5, -9			HA-2539C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 8)											
Rise Time	25	-	7	-	-	7	-	-	7	-	ns
Overshoot	25	-	15	-	-	15	-	-	15	-	%
Slew Rate	25	550	600	-	550	600	-	550	600	-	V/µs
Settling Time: 10V Step to 0.1%	25	-	180	-	-	180	-	-	200	-	ns
POWER REQUIREMENTS											
Supply Current	Full	-	20	25	-	20	25	-	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	-	60	70	-	60	70	-	dB

NOTES:

3. $R_L = 1k\Omega$, $V_O = \pm10V$.
4. $V_{CM} = \pm10.0V$.
5. $V_O = 90mV$.
6. $A_V = 10$.
7. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of data sheet.
9. $V_{SUPPLY} = +5V, -15V$ and $+15V, -5V$.
10. Guaranteed range for output voltage is $\pm10V$. Functional operation outside of this range is not guaranteed.

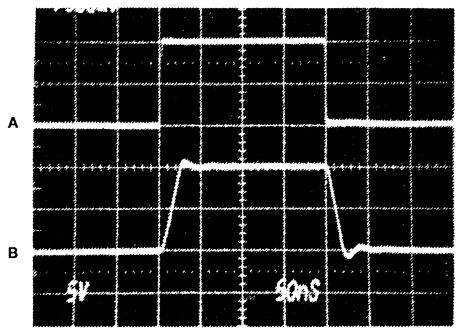
Test Circuits and Waveforms



NOTES:

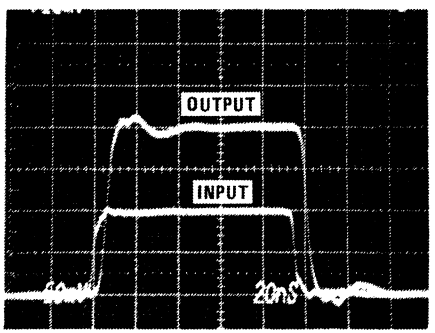
11. $V_S = \pm15V$.
12. $A_V = +10$.
13. $C_L \leq 10pF$.

FIGURE 1. TEST CIRCUIT



Vertical Scale: A = 0.5V/Div., B = 5.0V/Div.
Horizontal Scale: 50ns/Div.

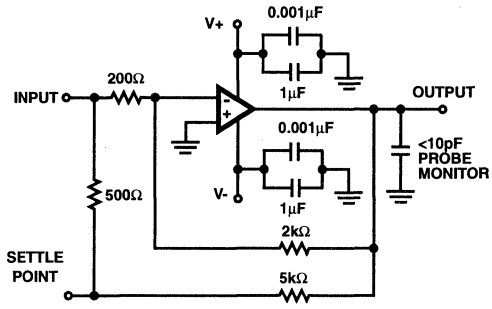
FIGURE 2. LARGE SIGNAL RESPONSE



Vertical Scale: Input = 10mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.

FIGURE 3. SMALL SIGNAL RESPONSE

Test Circuits and Waveforms (Continued)

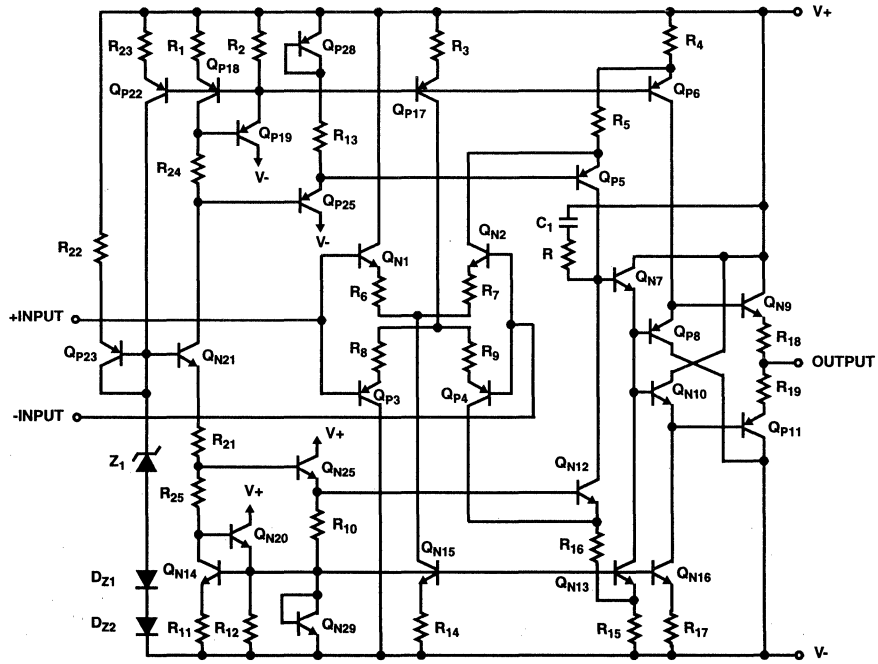


NOTES:

14. $A_V = -10$.
15. Load Capacitance should be less than 10pF.
16. It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
17. SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FIGURE 4. SETTLING TIME CIRCUIT

Schematic Diagram



Typical Applications

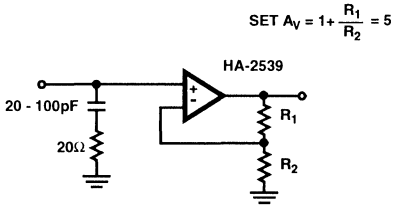


FIGURE 5. FREQUENCY COMPENSATION BY OVERDAMPING

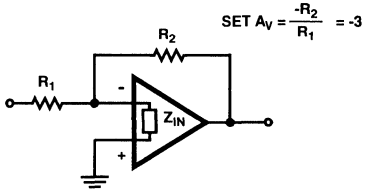


FIGURE 6. STABILIZATION USING Z_{IN}

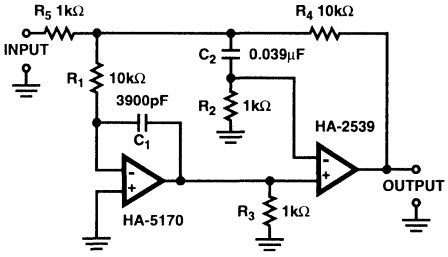


FIGURE 7. REDUCING DC ERRORS; COMPOSITE AMPLIFIER

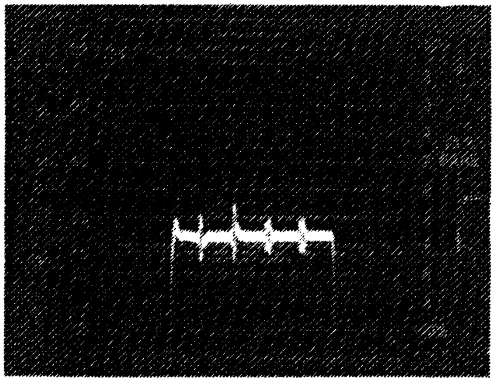


FIGURE 8. DIFFERENTIAL GAIN ERROR (3%) HA-2539 20dB VIDEO GAIN BLOCK

Typical Performance Curves

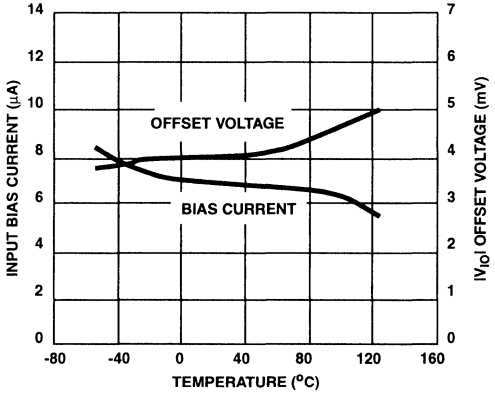


FIGURE 9. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

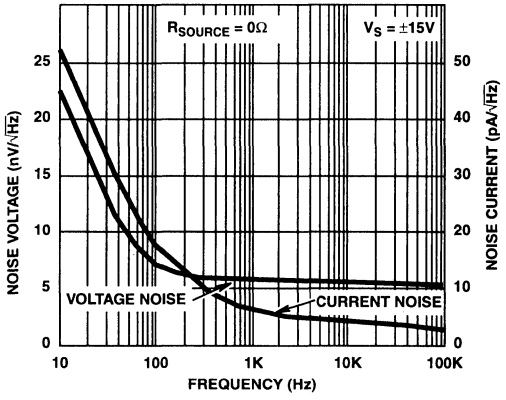


FIGURE 10. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

Typical Performance Curves (Continued)

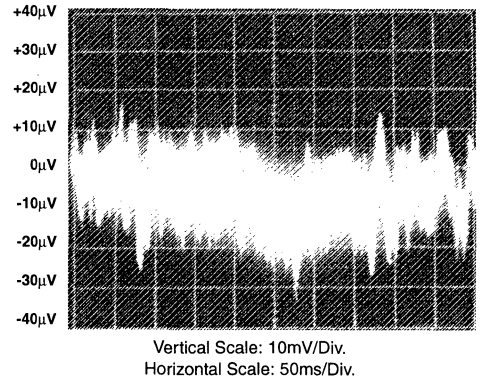


FIGURE 11. BROADBAND NOISE (0.1Hz TO 1MHz)

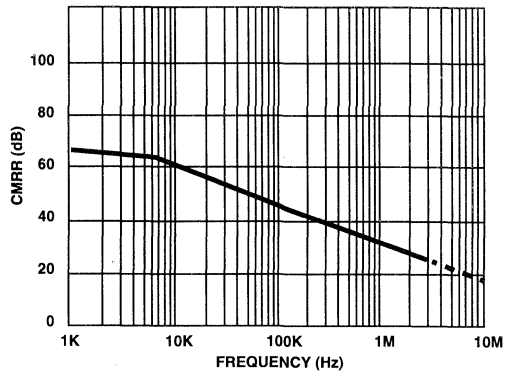


FIGURE 12. COMMON MODE REJECTION RATIO vs FREQUENCY

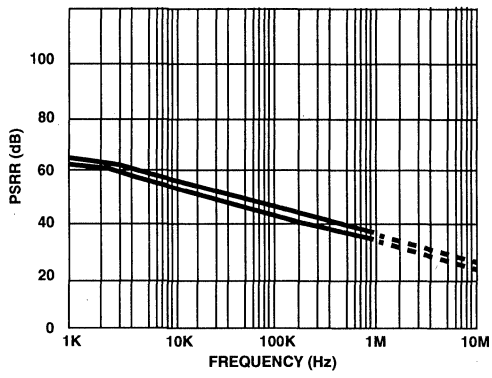


FIGURE 13. POWER SUPPLY REJECTION RATIO vs FREQUENCY

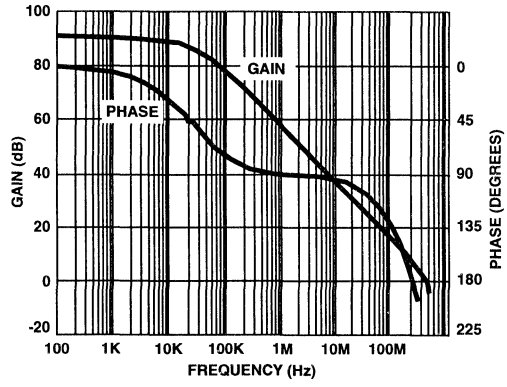


FIGURE 14. OPEN LOOP GAIN/PHASE vs FREQUENCY

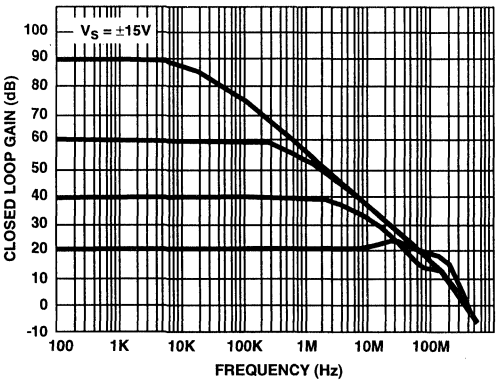


FIGURE 15. CLOSED LOOP FREQUENCY RESPONSE

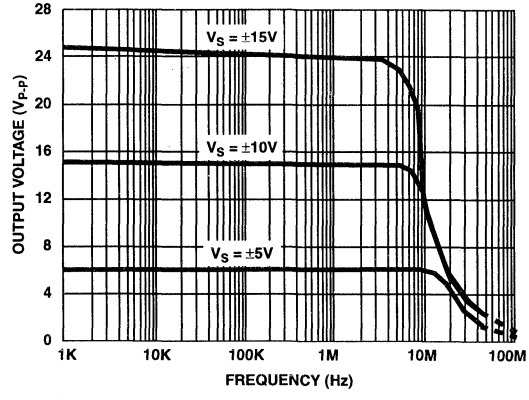


FIGURE 16. OUTPUT VOLTAGE SWING vs FREQUENCY

Typical Performance Curves (Continued)

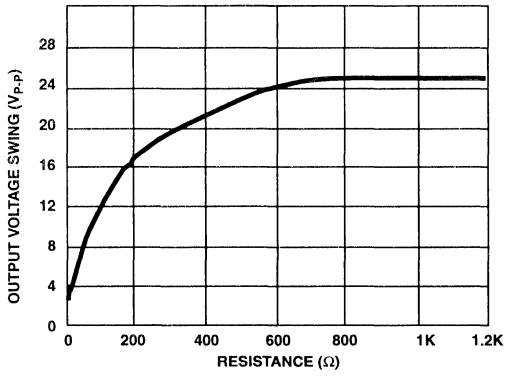


FIGURE 17. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

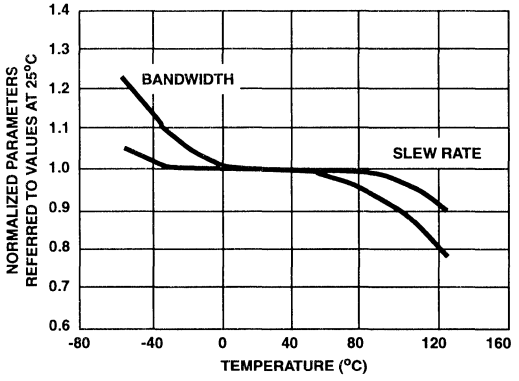


FIGURE 18. NORMALIZED AC PARAMETERS vs TEMPERATURE

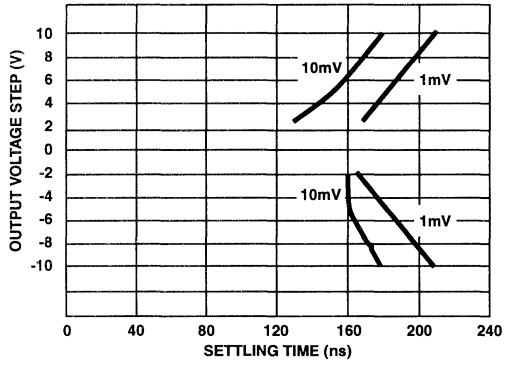


FIGURE 19. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

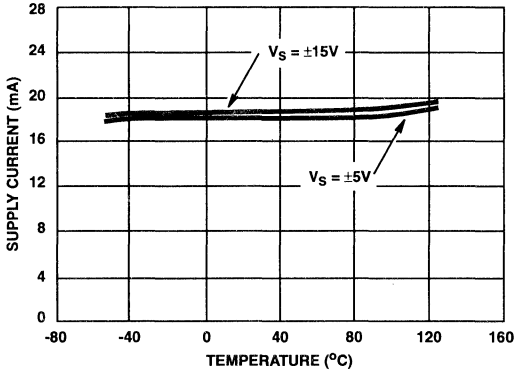


FIGURE 20. POWER SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

62 mils x 76 mils x 19 mils
1575µm x 1930µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

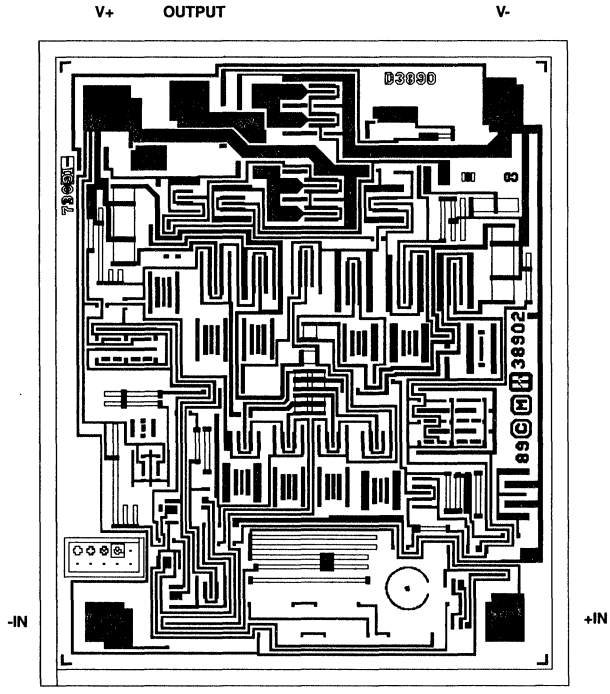
30

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2539



HARRIS SEMICONDUCTOR

HA-2540

400MHz, Fast Settling Operational Amplifier

November 1996

Features

- Very High Slew Rate 400V/µs
- Fast Settling Time 140ns
- Wide Gain Bandwidth ($A_V \geq 10$) 400MHz
- Power Bandwidth 6MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... ±10V
- Monolithic Bipolar Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-2540-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-2540-5	0 to 75	14 Ld CERDIP	F14.3
HA3-2540-5	0 to 75	14 Ld PDIP	E14.3
HA3-2540C-5	0 to 75	14 Ld PDIP	E14.3
HA9P2540-5	0 to 75	14 Ld SOIC	M14.15

Description

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of ±10V into a 1kΩ load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

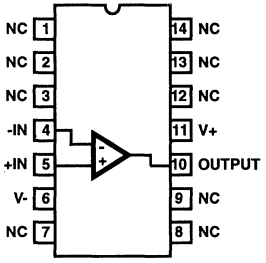
A 400V/µs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth product is ideally suited for wideband signal amplification. A settling time of 140ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

Refer to Application Note AN541 and Application Note AN556 for more information on High Speed Op Amp applications. HA-2540/883 MIL-STD-883 data sheet is available on request.

For a lower power version of this product, please see the HA-2840 and HA-2850 datasheets.

Pinout

HA-2540
(CERDIP, PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage. 6V
Output Current . . . . . $33mA_{RMS}$ Continuous, $50mA_{PEAK}$

Operating Conditions

Temperature Range
HA-2540-2. . . . . -55°C to 125°C
HA-2540/2540C-5. . . . . 0°C to 75°C
HA-2540/2540C-9. . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
PDIP Package	107	N/A
SOIC Package	119	N/A

Maximum Internal Power Dissipation (Note 1)
Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Packages). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below 175°C for the ceramic package, and below 150°C for the plastic package. By using Application Note AN556 on Safe Operating Area Equations, along with the thermal resistances, proper load conditions can be determined. Heat sinking is recommended above 75°C.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

PARAMETER	TEMP (°C)	HA-2540-2			HA-2540-5, -9			HA-2540C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	25	-	8	10	-	8	15	-	8	15	mV
	Full	-	13	15	-	13	20	-	13	20	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	-	20	-	µV/°C
Bias Current	25	-	5	20	-	5	20	-	5	20	µA
	Full	-	-	25	-	-	25	-	-	25	µA
Offset Current	25	-	1	6	-	1	6	-	1	6	µA
	Full	-	-	8	-	-	8	-	-	8	µA
Input Resistance	25	-	10	-	-	10	-	-	10	-	kΩ
Input Capacitance	25	-	1	-	-	1	-	-	1	-	pF
Common Mode Range	Full	±10	-	-	±10	-	-	±10	-	-	V
Input Noise Current ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	25	-	6	-	-	6	-	-	6	-	$pA/\sqrt{Hz}$
Input Noise Voltage ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	25	-	6	-	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	25	10	15	-	10	15	-	7	10	-	kV/V
	Full	5	-	-	5	-	-	5	-	-	kV/V
Common-Mode Rejection Ratio (Note 4)	Full	60	72	-	60	72	-	60	72	-	dB
Minimum Stable Gain	25	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth Product (Notes 5, 6)	25	-	400	-	-	400	-	-	400	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Notes 3, 10)	Full	±10	-	-	±10	-	-	±10	-	-	V
Output Current (Note 3)	25	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Resistance	25	-	30	-	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	25	5.5	6	-	5.5	6	-	5.5	6	-	MHz

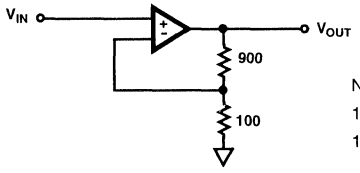
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP (°C)	HA-2540-2			HA-2540-5, -9			HA-2540C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 8)											
Rise Time	25	-	14	-	-	14	-	-	14	-	ns
Overshoot	25	-	5	-	-	5	-	-	5	-	%
Slew Rate	25	320	400	-	320	400	-	320	400	-	V/µs
Settling Time: 10V Step to 0.1%	25	-	140	-	-	140	-	-	140	-	ns
POWER REQUIREMENTS											
Supply Current	Full	-	20	25	-	20	25	-	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	-	60	70	-	60	70	-	dB

NOTES:

3. $R_L = 1k\Omega$, $V_O = \pm10V$.
4. $V_{CM} = \pm10V$.
5. $V_O = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of the data sheet.
9. $V_{SUPPLY} = +5V, -15V$ and $+15V, -5V$.
10. Guaranteed range for output voltage is $\pm10V$. Functional operation outside of this range is not guaranteed.

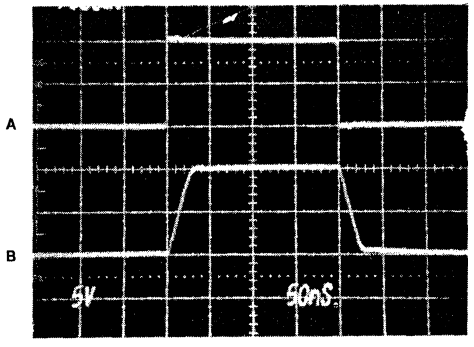
Test Circuits and Waveforms



NOTES:

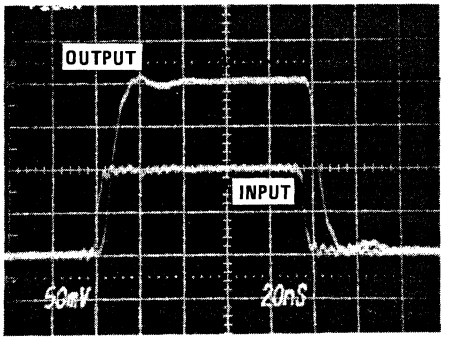
11. $A_V = +10$.
12. $C_L \leq 10pF$.

FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



Vertical Scale: A = 0.5V/Div., B = 5.0V/Div.
Horizontal Scale: 50ns/Div.

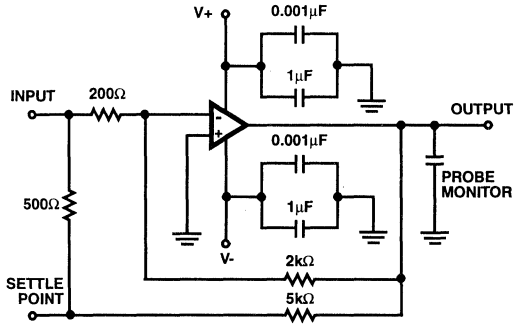
LARGE SIGNAL RESPONSE



Vertical Scale: Input = 10mV/Div.; Output = 50mV/Div.
Horizontal Scale: 20ns/Div.

SMALL SIGNAL RESPONSE

Test Circuits and Waveforms (Continued)

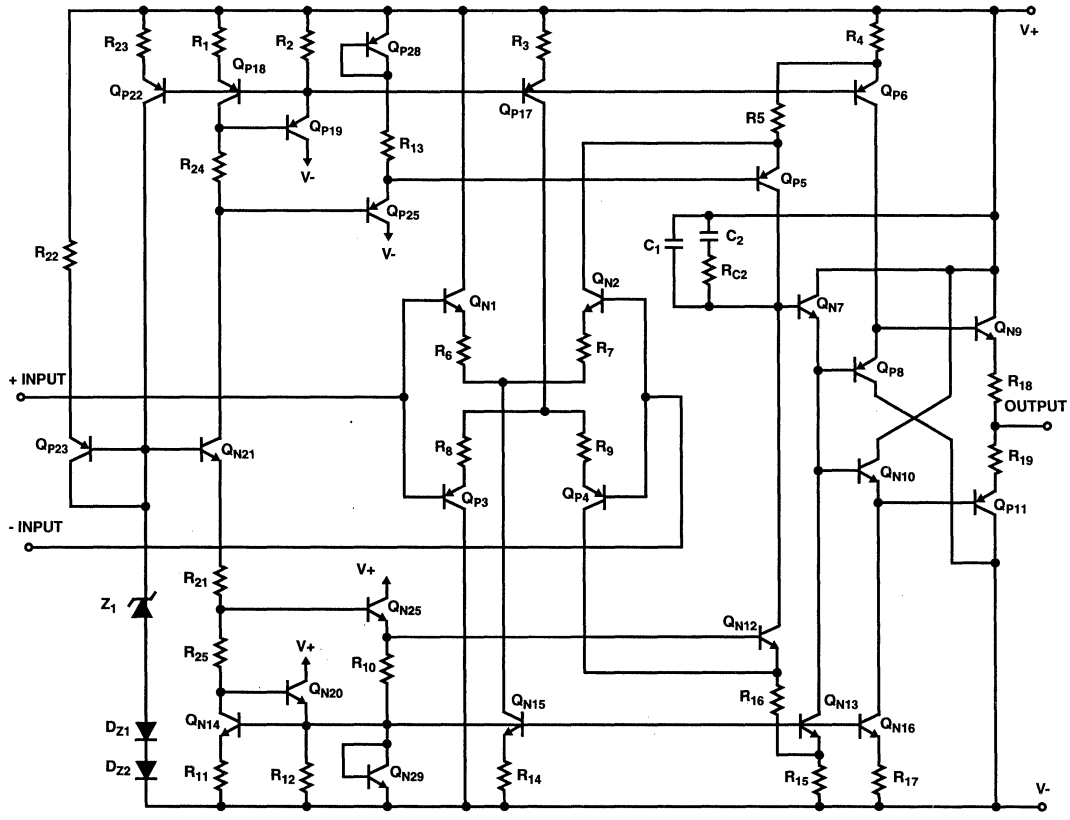


NOTES:

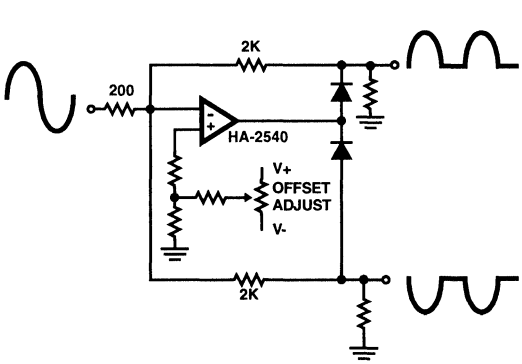
13. $A_V = -10$.
14. Load Capacitance should be less than 10pF. Turn on time delay typically 4ns.
15. It is recommended that resistors be carbon composition and the feedback and summing network ratios be matched to 0.1%.
16. SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram

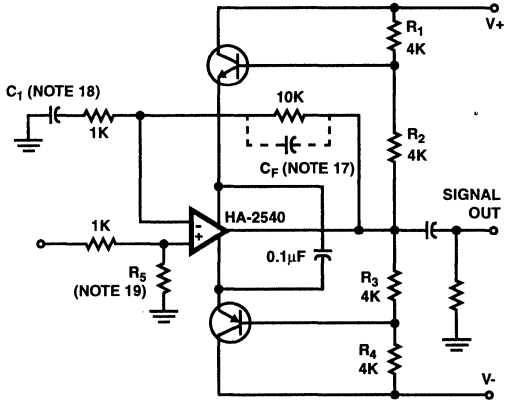


Typical Applications



NOTE: With one HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be separated. This circuit is most useful for full wave rectification, AM detectors or sync generation.

FIGURE 3. WIDEBAND SIGNAL SPLITTER



NOTES:

17. Used for experimental purposes. $C_F \cong 3pF$.
18. C_1 is optional (0.001μF → 0.01μF ceramic).
19. R_5 is optional and can be utilized to reduce input signal amplitude and/or balance input conditions. $R_5 = 500\Omega$ to $1k\Omega$.

FIGURE 4. BOOTSTRAPPING FOR MORE OUTPUT CURRENT AND VOLTAGE SWING

Refer to Application Note AN541 For Further Application Information.

Typical Performance Curves

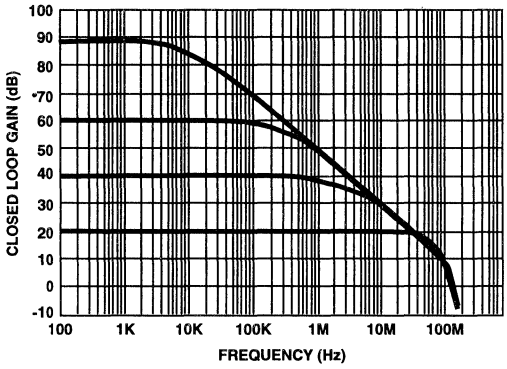


FIGURE 5. CLOSED LOOP FREQUENCY RESPONSE

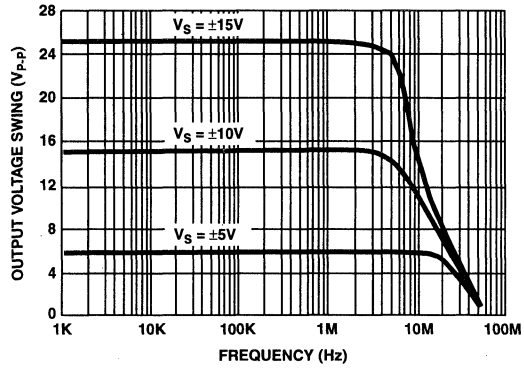


FIGURE 6. OUTPUT VOLTAGE SWING vs FREQUENCY

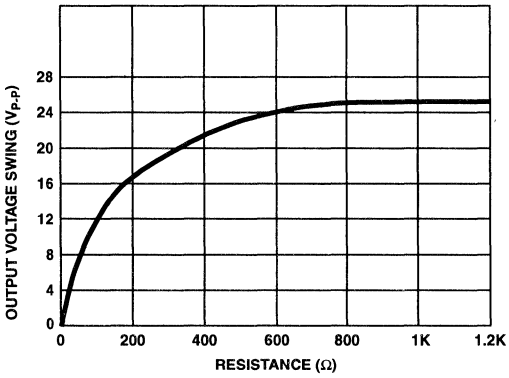


FIGURE 7. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

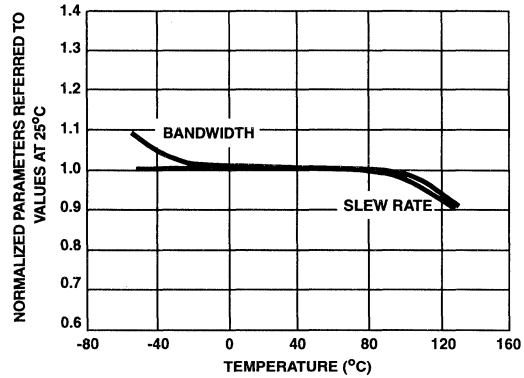


FIGURE 8. NORMALIZED AC PARAMETERS vs TEMPERATURE

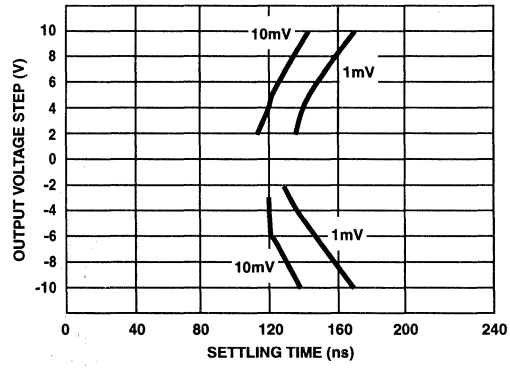


FIGURE 9. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

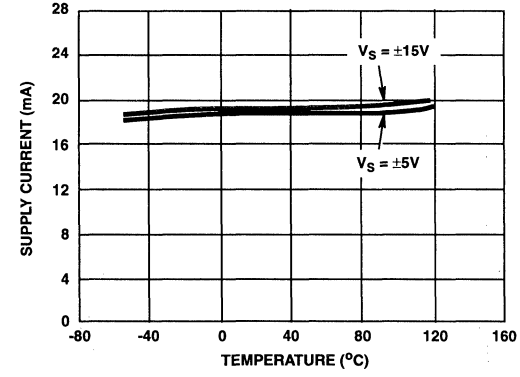


FIGURE 10. POWER SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

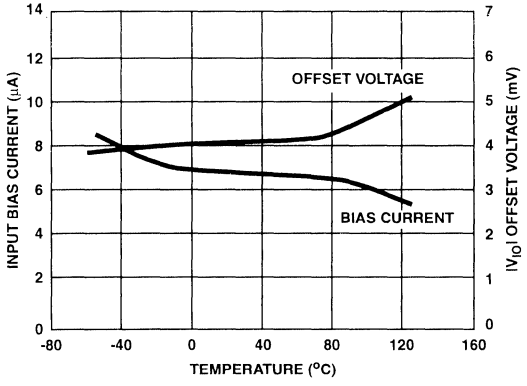


FIGURE 11. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

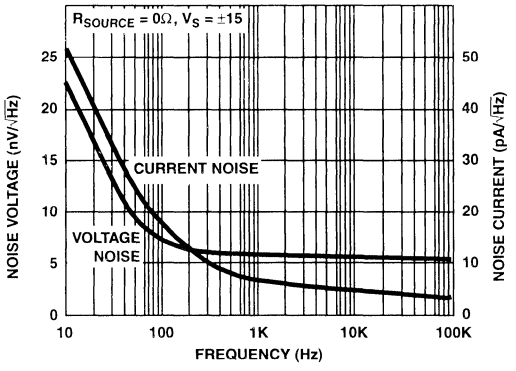


FIGURE 12. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

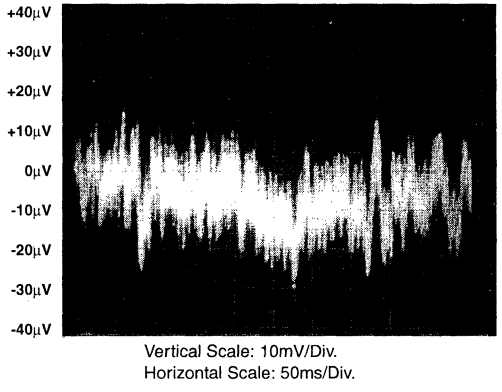


FIGURE 13. BROADBAND NOISE (0.1Hz TO 1MHz)

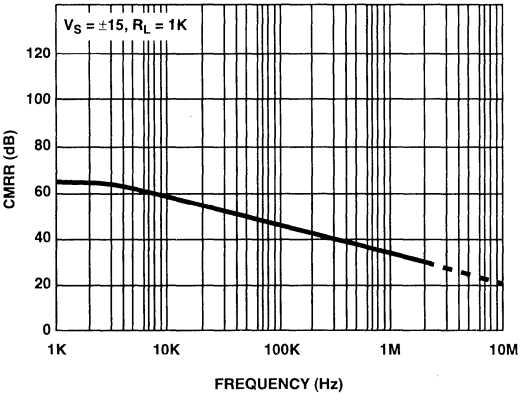


FIGURE 14. COMMON MODE REJECTION RATIO vs FREQUENCY

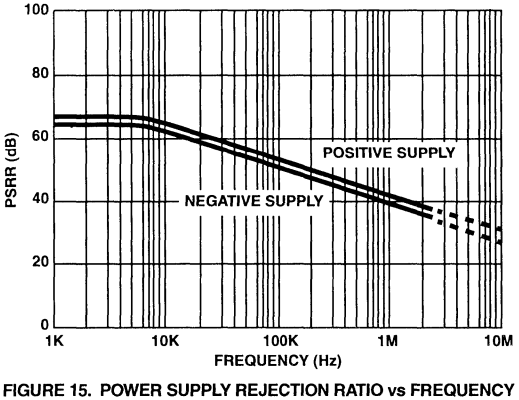


FIGURE 15. POWER SUPPLY REJECTION RATIO vs FREQUENCY

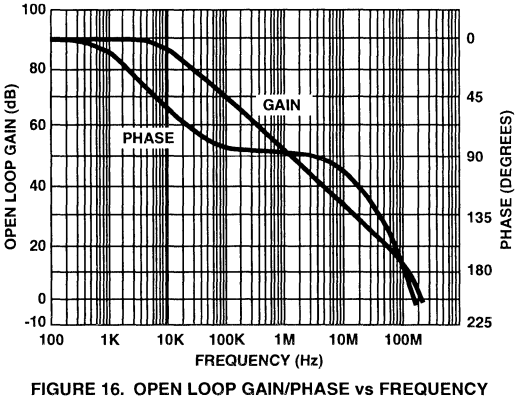


FIGURE 16. OPEN LOOP GAIN/PHASE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

62 mils x 76 mils x 19 mils
1575 µmx 1930µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

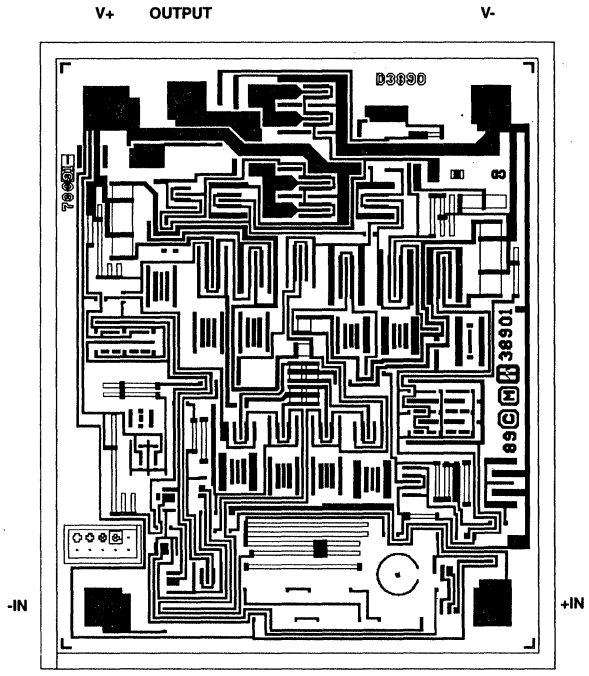
30

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2540



HARRIS SEMICONDUCTOR

HA-2541

40MHz, Fast Settling, Unity Gain Stable, Operational Amplifier

November 1996

Features

- Unity Gain Bandwidth 40MHz
- High Slew Rate 250V/μs
- Low Offset Voltage 0.8mV
- Fast Settling Time (0.1%) 90ns
- Power Bandwidth 4MHz
- Output Voltage Swing (Min) ..... ±10V
- Unity Gain Stability
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

For a lower power version of this product, please see the HA-2841 data sheet.

Description

The HA-2541 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Harris series of high speed, wideband op amps, the HA-2541 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

The uniqueness of the HA-2541 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 250V/μs slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541. These features, along with 90ns settling time to 0.1%, make this product an excellent choice for high speed data acquisition systems.

MIL-STD-883 product and data sheets are available upon request, Harris AnswerFAX (407-724-7800) document #3698.

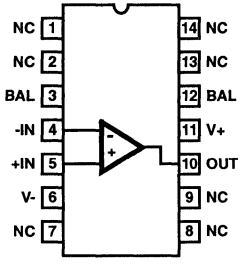
For further application suggestions on the HA-2541, please refer to Application Note AN550 (Using the HA-2541), and Application Note AN556 (Thermal Safe Operating Areas for High Current Operational Amplifiers), Harris AnswerFAX (407-724-7800) document #9550 and 9556. Also see 'Applications' in this data sheet.

Ordering Information

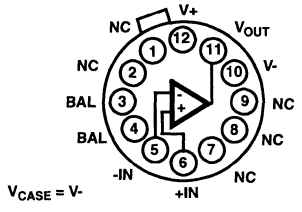
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-2541-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-2541-5	0 to 75	14 Ld CERDIP	F14.3
HA2-2541-2	-55 to 125	12 Pin Metal Can	T12.C
HA2-2541-5	0 to 75	12 Pin Metal Can	T12.C

Pinouts

HA1-2541
(CERDIP)
TOP VIEW



HA2-2541
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage. 6V
Peak Output Current. 50mA
Continuous Output Current. . . . . $28mA_{RMS}$

Operating Conditions

Temperature Range
HA-2541-2. . . . . -55°C to 125°C
HA-2541-5. . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
Can Package	65	34

Maximum Junction Temperature (Note 1) . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below 175°C. By using Application Note AN556 on Safe Operating Area equations, along with the thermal resistances, proper load conditions can be determined. Heat sinking is recommended above 75°C.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2541-2 -55°C to 125°C			HA-2541-5 0°C to 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	0.8	2	-	1	2	mV
		Full	-	-	6	-	-	6	mV
Average Offset Voltage Drift		Full	-	9	-	-	9	-	µV/°C
Bias Current		25	-	11	35	-	11	35	µA
		Full	-	-	50	-	-	50	µA
Average Bias Current Drift		Full	-	85	-	-	85	-	nA/°C
Offset Current		25	-	1	7	-	1	7	µA
		Full	-	-	9	-	-	9	µA
Input Resistance		25	-	100	-	-	100	-	kΩ
Input Capacitance		25	-	1	-	-	1	-	pF
Common Mode Range		Full	±10	±11	-	±10	±11	-	V
Input Noise Voltage	f = 1kHz, $R_g = 0\Omega$	25	-	10	-	-	10	-	$nV/\sqrt{Hz}$
Input Noise Current	f = 1kHz, $R_g = 0\Omega$	25	-	4	-	-	4	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$V_O = \pm10V$	25	10	16	-	10	16	-	kV/V
		Full	5	-	-	5	-	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	Full	70	90	-	70	90	-	dB
Minimum Stable Gain		25	1	-	-	1	-	-	V/V
Unity Gain Bandwidth	$V_O = 90mV$	25	-	40	-	-	40	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 1k\Omega$	Full	±10	±11	-	±10	±11	-	V
Output Current	$R_L = 1k\Omega$	25	±10	±15	-	±10	±15	-	mA
Output Resistance		25	-	2	-	-	2	-	Ω
Full Power Bandwidth (Note 3)	$V_P = 10V$	25	3	4	-	3	4	-	MHz
Differential Gain	Note 4	25	-	0.1	-	-	0.1	-	%
Differential Phase	Note 4	25	-	0.2	-	-	0.2	-	Degrees

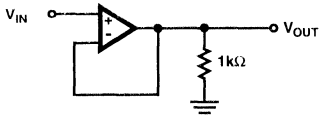
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2541-2 -55°C to 125°C			HA-2541-5 0°C to 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Harmonic Distortion	Note 6	25	-	<0.01	-	-	<0.01	-	%
TRANSIENT RESPONSE (Note 5)									
Rise Time		25	-	4	-	-	4	-	ns
Overshoot		25	-	40	-	-	40	-	%
Slew Rate		25	200	250	-	200	250	-	V/µs
Settling Time	10V Step To 0.1%	25	-	90	-	-	90	-	ns
	10V Step To 0.01%	25	-	175	-	-	175	-	ns
POWER REQUIREMENTS									
Supply Current		25	-	29	-	-	29	-	mA
		Full	-	-	40	-	-	40	mA
Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	Full	70	80	-	70	78	-	dB

NOTES:

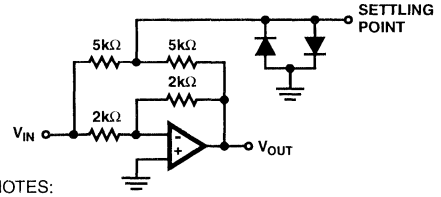
3. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
4. Differential Gain and Phase are measured with a 1V differential voltage at 5MHz.
5. Refer to Test Circuits section of this data sheet.
6. f = 10kHz; $A_V = 5$; $V_O = 14V_{P-P}$.

Test Circuits and Waveforms



NOTES:

7. $V_S = \pm15V$.
8. $A_V = +1$.
9. $C_L \leq 10pF$.

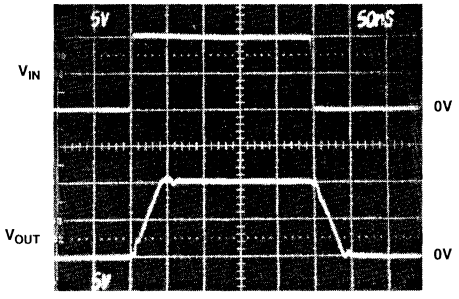


NOTES:

10. $A_V = -1$.
11. Feedback and summing resistor ratios should be 0.1% matched.
12. HP5082-2810 clipping diodes recommended.
13. Tektronix P6201 FET probe used at settling point.

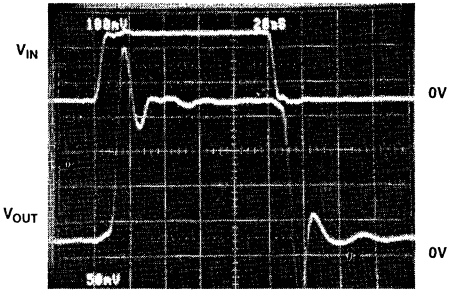
FIGURE 1. TRANSIENT RESPONSE TEST CIRCUIT

FIGURE 2. SETTLING TIME TEST CIRCUIT



Vertical Scale: 5V/Div.
Horizontal Scale: 50ns/Div.

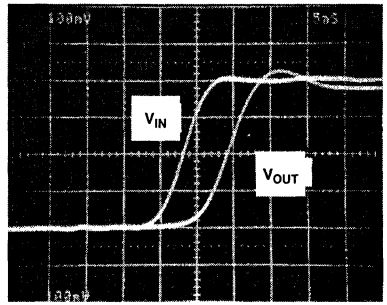
LARGE SIGNAL RESPONSE



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 50mV/Div.
Horizontal Scale: 20ns/Div.

SMALL SIGNAL RESPONSE

Test Circuits and Waveforms (Continued)



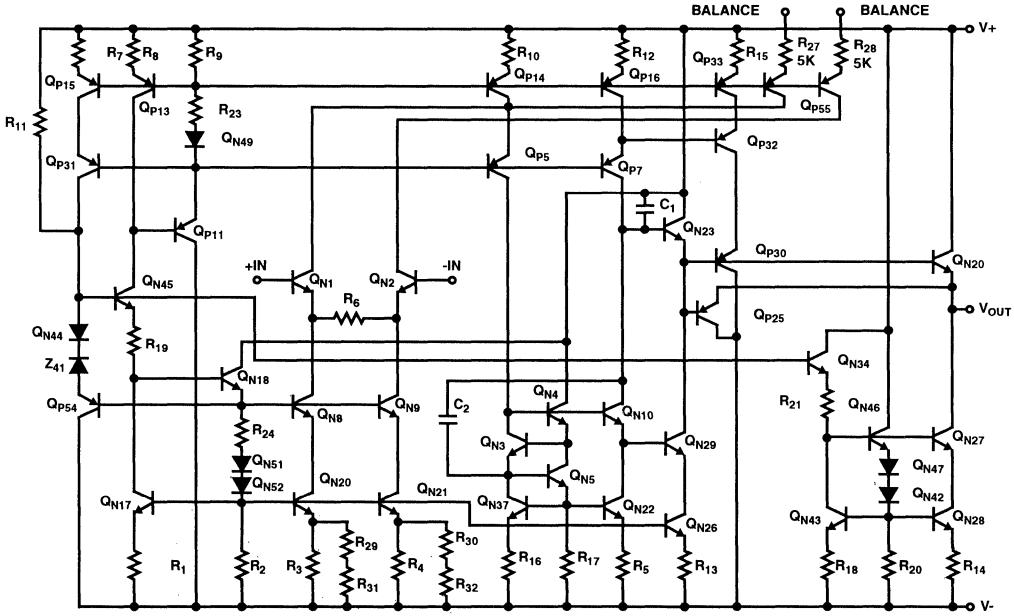
Vertical Scale: 100mV/Div.
Horizontal Scale: 5ns/Div.

PROPAGATION DELAY

NOTES:

14. $V_S = \pm 15V$, $R_L = 1k\Omega$.
15. $T_A = 25^oC$.
16. Propagation delay variance is negligible over full temperature range.

Schematic Diagram



Typical Applications (Also see Application Note AN550)

Application 1

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2541, with its 10mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Figure 3.

The HA-2541 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50Ω coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6Ω and 6000pF capacitance.

Application 2

Video

One of the primary uses of the HA-2541 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2541 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores DC levels at the output of an amplifier stage. The circuit shown in Figure 4 utilizes the HA-5320 sample and hold amplifier as the DC clamp. Also shown is a 3.57MHz trap in series, which will block the color burst portion of the video signal and allow the DC level to be amplified and restored.

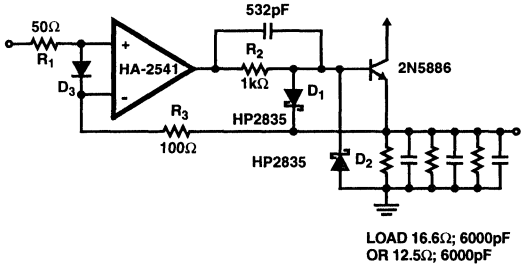


FIGURE 3. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

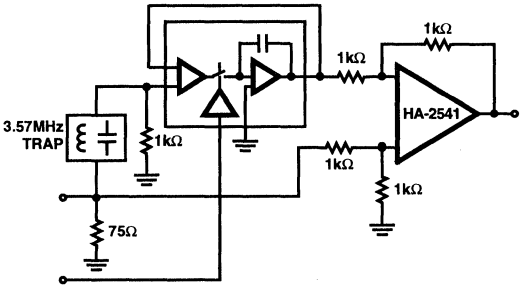
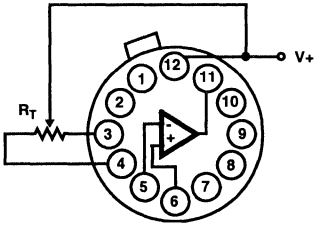


FIGURE 4. VIDEO DC RESTORER

Suggested Offset Voltage Adjustment



NOTE: Tested Offset Adjustment Range is $|V_{OS}| + 1mV|$ minimum referred to output. Typical range is ±15mV for $R_T = 5k\Omega$.

Typical Performance Curves

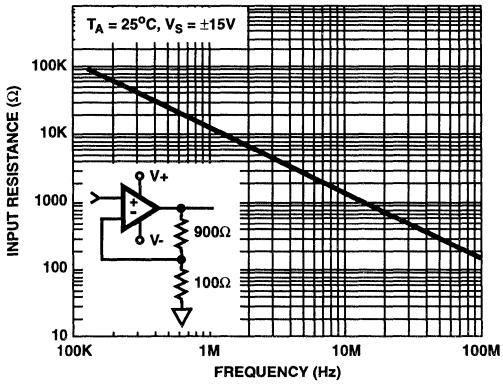


FIGURE 5. INPUT RESISTANCE vs FREQUENCY

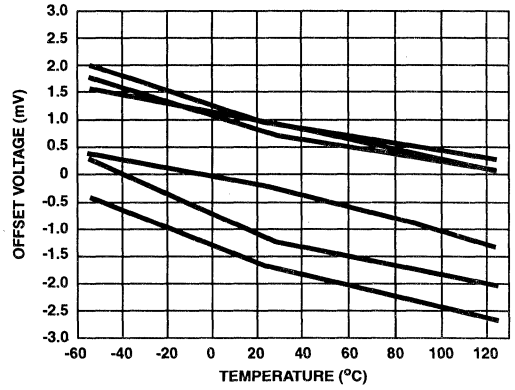


FIGURE 6. OFFSET VOLTAGE vs TEMPERATURE (6 REPRESENTATIVE UNITS)

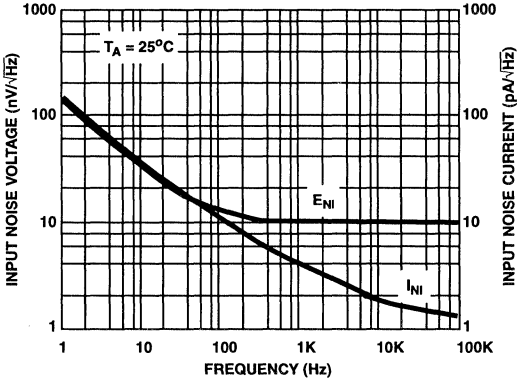


FIGURE 7. NOISE DENSITY vs FREQUENCY

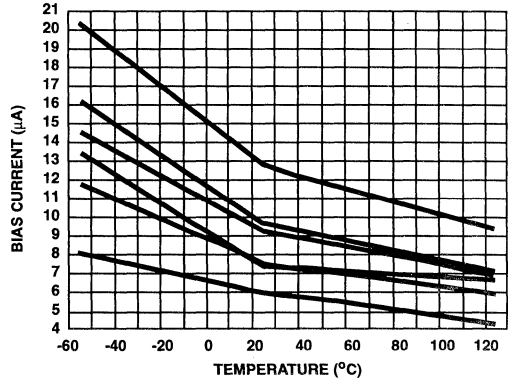


FIGURE 8. BIAS CURRENT vs TEMPERATURE (6 REPRESENTATIVE UNITS)

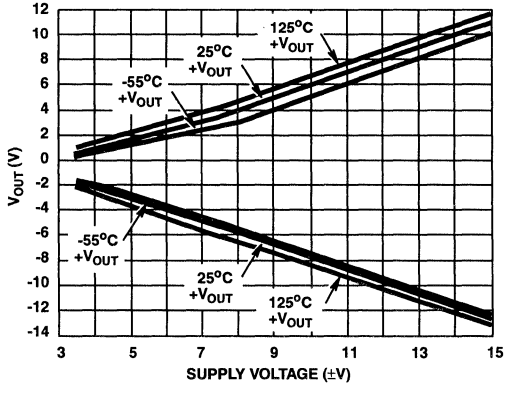


FIGURE 9. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

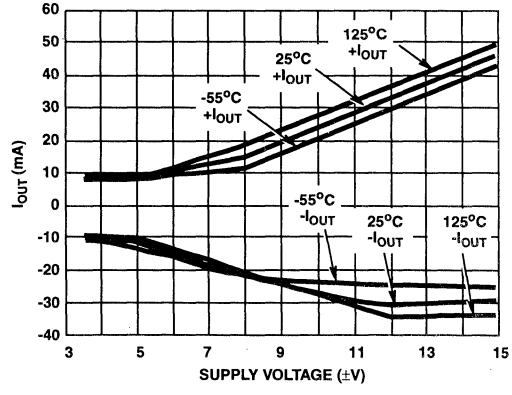


FIGURE 10. OUTPUT CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

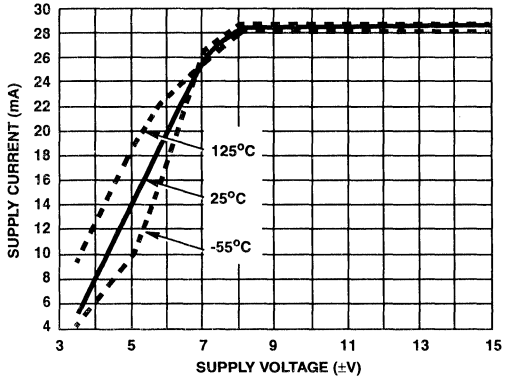


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE

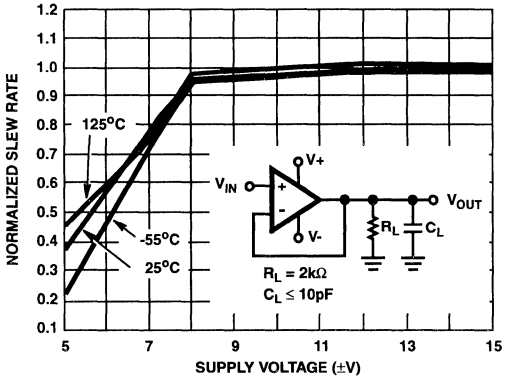


FIGURE 12. SLEW RATE vs SUPPLY VOLTAGE (NORMALIZED WITH V_S = ±15V AT 25°C)

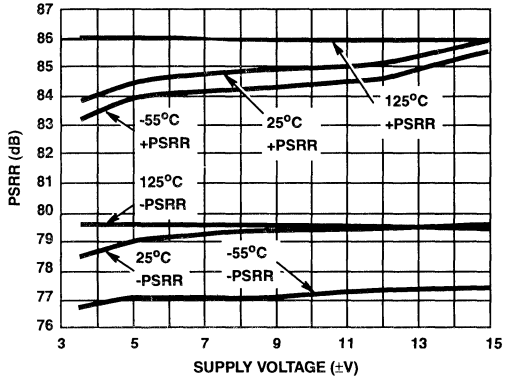


FIGURE 13. PSRR vs SUPPLY VOLTAGE (AVERAGE OF 3 LOTS)

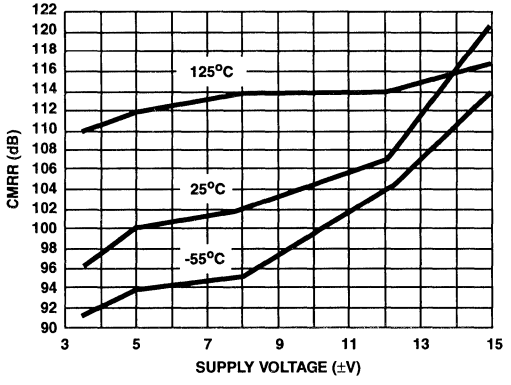


FIGURE 14. CMRR vs SUPPLY VOLTAGE (AVERAGE OF 3 LOTS)

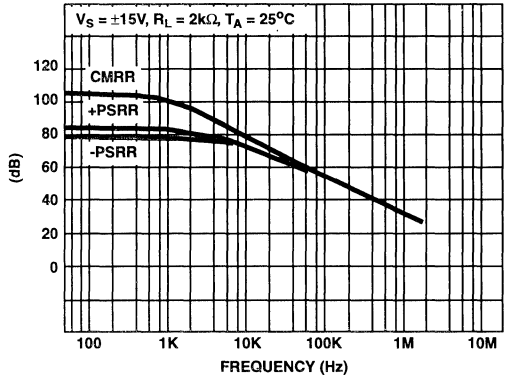


FIGURE 15. REJECTION RATIOS vs FREQUENCY

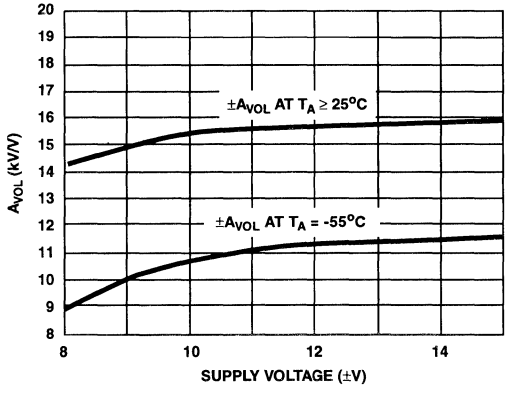


FIGURE 16. OPEN LOOP GAIN vs SUPPLY VOLTAGE (AVERAGE OF 3 LOTS)

Typical Performance Curves (Continued)

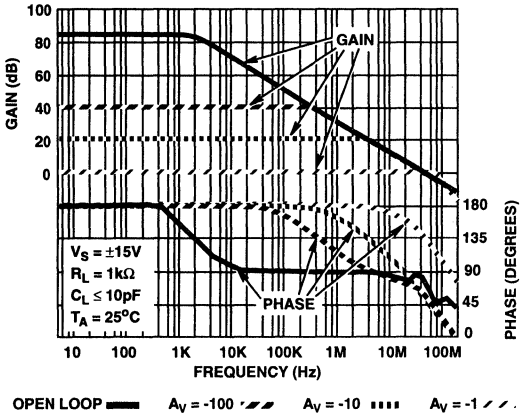


FIGURE 17. GAIN AND PHASE FREQUENCY RESPONSE

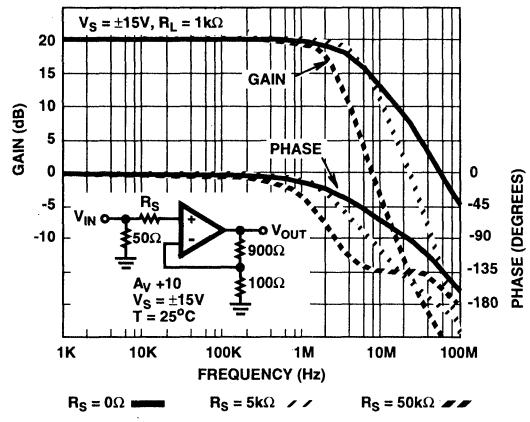


FIGURE 18. SMALL SIGNAL BANDWIDTH vs SOURCE RESISTANCE

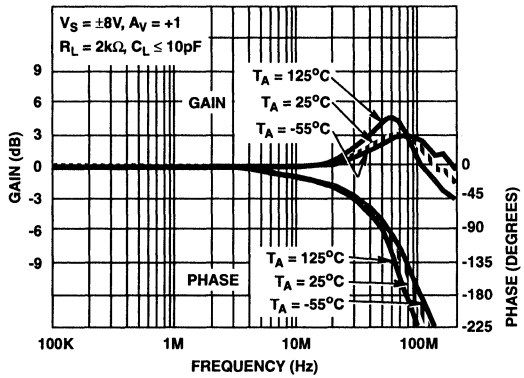


FIGURE 19. CLOSED LOOP FREQUENCY RESPONSE

Die Characteristics

DIE DIMENSIONS:

80 mils x 90 mils x 19 mils
2020µm x 2280µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride(Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

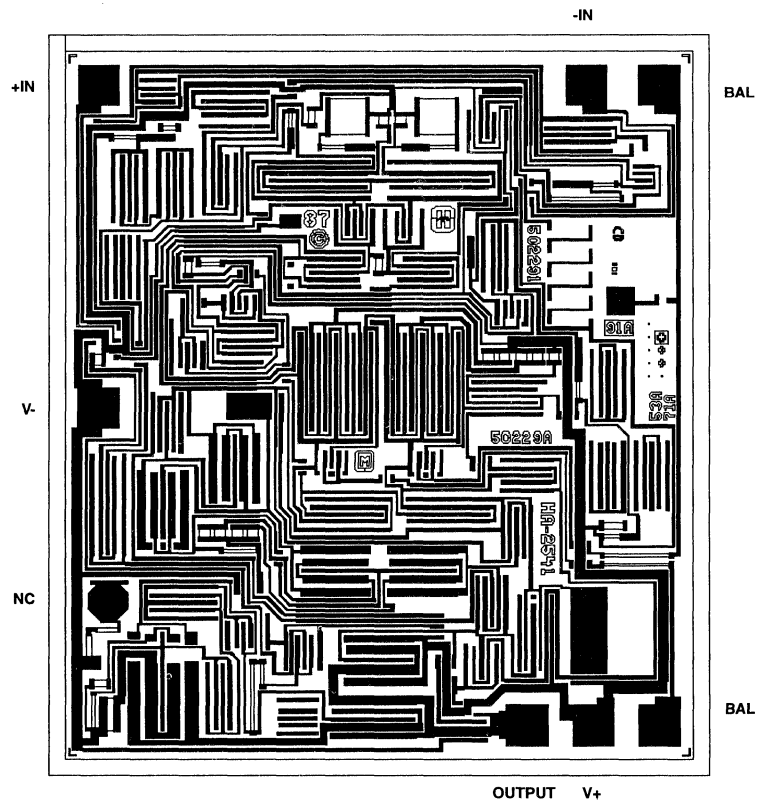
41

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2541



HARRIS SEMICONDUCTOR

HA-2542

70MHz, High Slew Rate, High Output Current Operational Amplifier

November 1996

Features

- Stable at Gains of 2 or Greater
- Gain Bandwidth 70MHz
- High Slew Rate ..... 300V/μs (Min)
- High Output Current ..... 100mA (Min)
- Power Bandwidth ..... 5.5MHz (Typ)
- Output Voltage Swing ..... ±10V (Min)
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-2542-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-2542-5	0 to 75	14 Ld CERDIP	F14.3
HA2-2542-2	-55 to 125	12 Pin Metal Can	T12.C
HA2-2542-5	0 to 75	12 Pin Metal Can	T12.C
HA3-2542-5	0 to 75	14 Ld PDIP	E14.3

Description

The HA-2542 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D.I. technology this amplifier offers 350V/μs slew rate, 70MHz gain bandwidth, and ±100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

For additional flexibility, offset null and frequency compensation controls are included in the HA-2542 pinout.

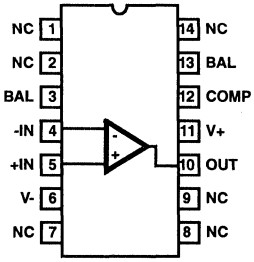
The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse video amplifiers. Other applications utilizing the HA-2542 advantages include wideband amplifiers and fast sample-hold circuits.

For more information on the HA-2542, please refer to Application Note AN552 (Using the HA-2542), or Application Note AN556 (Thermal Safe-Operating-Areas for High Current Op Amps).

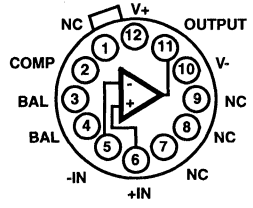
For a lower power version of this product, please see the HA-2842 data sheet.

Pinouts

HA-2542
(PDIP, CERDIP)
TOP VIEW



HA-2542
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2899.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 35V
Differential Input Voltage 6V
Output Current . . . . . 50mA Continuous, $125mA_{PEAK}$

Operating Conditions

Temperature Range
HA-2542-2 . . . . . -55^oC to 125^oC
HA-2542-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20
PDIP Package	100	N/A
Metal Can Package	65	34

Maximum Junction Temperature (Note 1, Hermetic Packages) . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below 175^oC for ceramic and can packages, and below 150^oC for plastic packages. By using Application Note AN556 on Safe Operating Area equations, along with the thermal resistances, proper load conditions can be determined. Heatsinking will be required in many applications. See the "Application Information" section to determine if heat sinking is required for your application.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	HA-2542-2 -55^oC to 125^oC			HA-2542-5 0^oC to 75^oC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	5	10	-	5	10	mV
		Full	-	8	20	-	8	20	mV
Average Offset Voltage Drift		Full	-	14	-	-	14	-	$\mu V/^oC$
Bias Current		25	-	15	35	-	15	35	μA
		Full	-	26	50	-	26	50	μA
Average Bias Current Drift		Full	-	66	-	-	45	-	$nA/^oC$
Offset Current		25	-	1	7	-	1	7	μA
		Full	-	-	9	-	-	9	μA
Input Resistance		25	-	100	-	-	100	-	$k\Omega$
Input Capacitance		25	-	1	-	-	1	-	pF
Common Mode Range		Full	±10	-	-	±10	-	-	V
Input Noise Voltage	0.1Hz to 100Hz	25	-	2.2	-	-	2.2	-	μV_{P-P}
Input Noise Density	$f = 1kHz$, $R_G = 0\Omega$	25	-	10	-	-	10	-	$nV/\sqrt{Hz}$
Input Noise Current Density	$f = 1kHz$, $R_G = 0\Omega$	25	-	3	-	-	3	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$V_O = \pm10V$	25	10	30	-	10	30	-	kV/V
		Full	5	15	-	5	20	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	Full	70	100	-	70	100	-	dB
Minimum Stable Gain		25	2	-	-	2	-	-	V/V
Gain Bandwidth Product	$A_V = 100$	25	-	70	-	-	70	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing		Full	±10	±11	-	±10	±11	-	V
Output Current (Note 3)		25	100	-	-	100	-	-	mA
Output Resistance		25	-	5	-	-	5	-	Ω

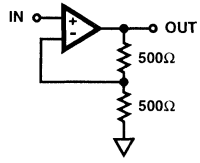
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-2542-2 -55°C to 125°C			HA-2542-5 0°C to 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Full Power Bandwidth (Note 4)	$V_{PEAK} = 10V$	25	4.7	5.5	-	4.7	5.5	-	MHz
Differential Gain (Note 5)		25	-	0.1	-	-	0.1	-	%
Differential Phase (Note 5)		25	-	0.2	-	-	0.2	-	Degree
Harmonic Distortion (Note 7)		25	-	<0.04	-	-	<0.04	-	%
TRANSIENT RESPONSE (Note 6)									
Rise Time		25	-	4	-	-	4	-	ns
Overshoot		25	-	25	-	-	25	-	%
Slew Rate		25	300	350	-	300	350	-	V/µs
Settling Time	10V Step to 0.1%	25	-	100	-	-	100	-	ns
	10V Step to 0.01%	25	-	200	-	-	200	-	ns
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	30	-	-	30	-	mA
		Full	-	31	34.5	-	31	40	mA
Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	Full	70	79	-	70	79	-	dB

NOTES:

3. $R_L = 50\Omega$, $V_O = \pm5V$, Output duty cycle must be reduced for $I_{OUT} > 50mA$ (e.g. ≤50% duty cycle for 100mA).
4. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
5. Differential gain and phase are measured at 5MHz with a 1V differential input voltage.
6. Refer to Test Circuits section of this data sheet.
7. $V_{IN} = 1V_{RMS}$; f = 10kHz; $A_V = 10$.

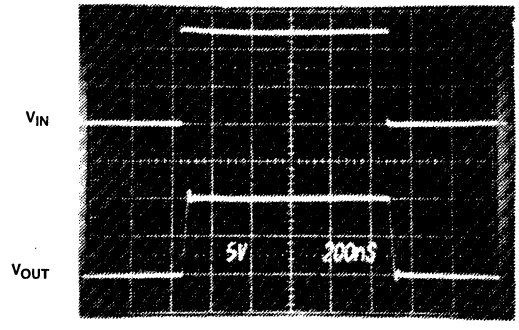
Test Circuits and Waveforms



NOTES:

8. $V_S = \pm15V$.
9. $A_V = +2$.
10. $C_L \leq 10pF$.

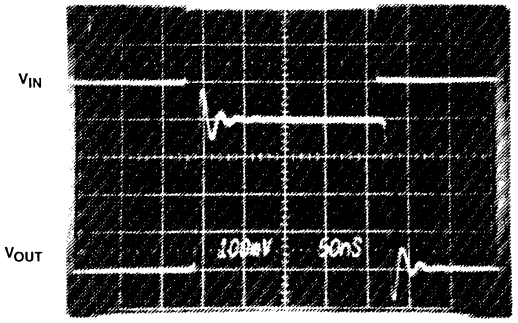
TEST CIRCUIT



Vertical Scale: $V_{IN} = 2.0V/Div.$, $V_{OUT} = 5.0V/Div.$
Horizontal Scale: 200ns/Div.

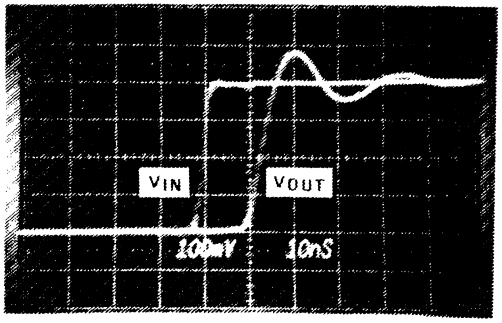
LARGE SIGNAL RESPONSE

Test Circuits and Waveforms (Continued)



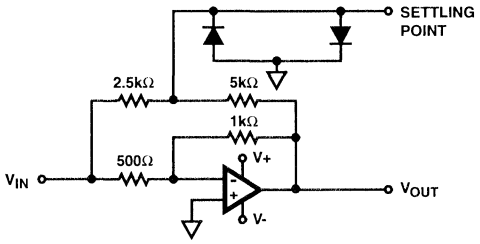
Vertical Scale: 100mV/Div.
Horizontal Scale: 50ns/Div.

SMALL SIGNAL RESPONSE



Vertical Scale: 100mV/Div.
Horizontal Scale: 10ns/Div.
$V_S = \pm 15V$, $R_L = 1k\Omega$. Propagation delay variance is negligible over full temperature range.

PROPAGATION DELAY

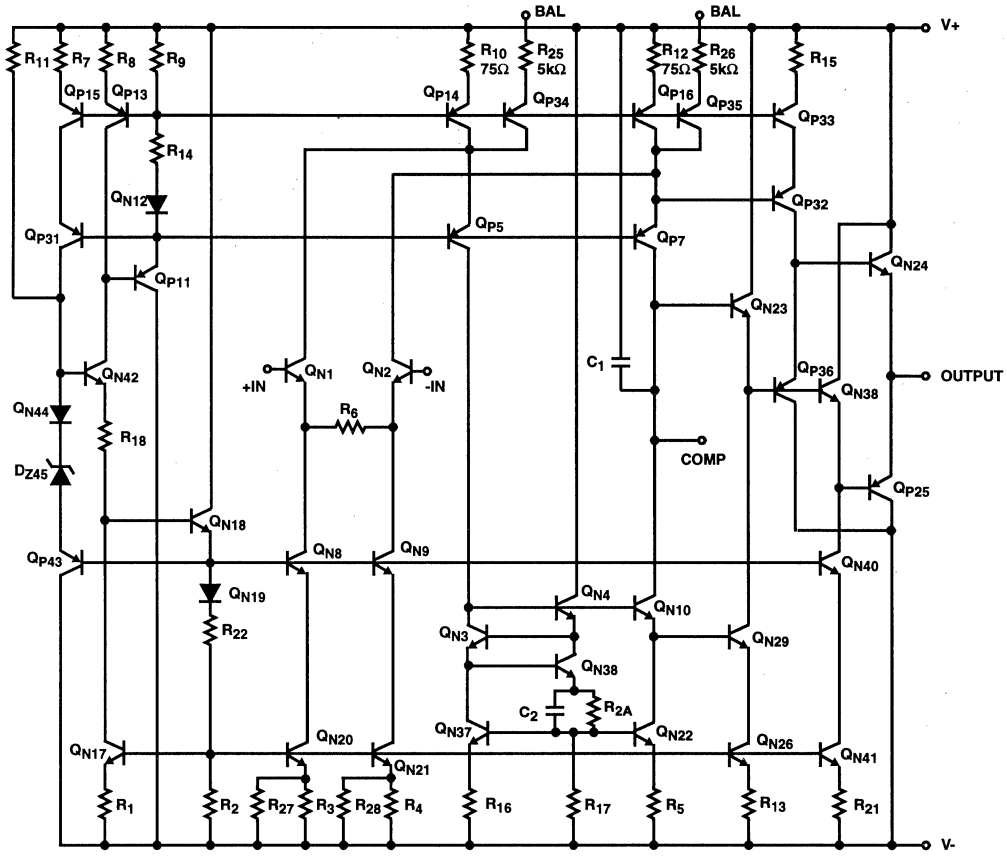


SETTLING TIME TEST CIRCUIT (See Notes 11 - 15.)

NOTES:

11. $A_V = -2$.
12. Feedback and summing resistors must be matched (0.1%).
13. HP5082-2810 clipping diodes recommended.
14. Tektronix P6201 FET probe used at settling point.
15. For 0.01% settling time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.

Schematic Diagram



Application Information (Refer to Application Note AN552 for Further Information)

The Harris HA-2542 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

The applications shown in Figures 2 through Figure 4 demonstrate the HA-2542 at gains of +100 and +2 and as a video cable driver for small signals.

Power Dissipation Considerations

At high output currents, especially with the PDIP package, care must be taken to ensure that the Maximum Junction Temperature (T_J, see "Absolute Maximum Ratings" table) is not exceeded. As an example consider the HA-2542 in the PDIP package, with a required output current of 20mA at V_{OUT} = 5V. The power dissipation is the quiescent power (1.2W = 30V x 40mA) plus the power dissipated in the output stage (P_{OUT} = 200mW = 20mA x (15V - 5V)), or a total of 1.4W. The thermal resistance (θ_{JA}) of the PDIP package is 100°C/W, which increases the junction temperature by 140°C over the ambient temperature (T_A). Remaining below T_{JMAX} requires that T_A be restricted to ≤ 10°C (150°C - 140°C). Heatsinking would be required for operation at ambient temperatures greater than 10°C.

Note that the problem isn't as severe with either the CERDIP or Can packages due to their lower thermal resistances, and higher T_{JMAX}. Nevertheless, it is recommended that Figure 1 be used to ensure that heat sinking is not required.

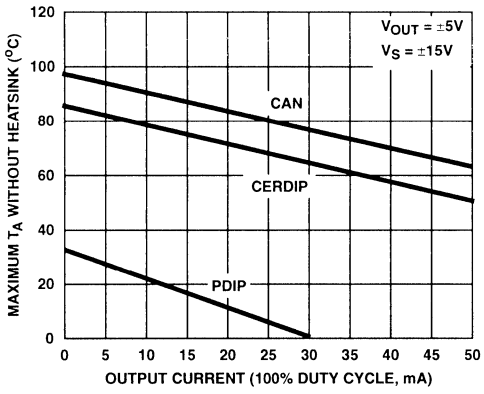


FIGURE 1. MAXIMUM OPERATING TEMPERATURE vs OUTPUT CURRENT

Allowable output power can be increased by decreasing the quiescent dissipation via lower supply voltages.

For more information please refer to Application Note AN556, "Thermal Safe Operating Areas for High Current Op Amps".

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane: 2) connecting unused pins (NC) to the ground: 3) mounting feedback components on Teflon standoffs and or locating these components as close to the device as possible: 4) placing power supply decoupling capacitors from device supply pins to ground.

As a result of speed and bandwidth optimization. the HA-2542 can's case potential, when powered-up, is equal to the V- potential. Therefore, contact with other circuitry or ground should be avoided.

Frequency Compensation

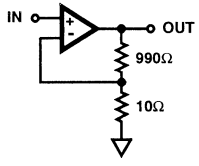
The HA-2542 may be externally compensated with a single capacitor to ground. This provides the user the additional flexibility in tailoring the frequency response of the amplifier. A guideline to the response is demonstrated on the typical performance curve showing the normalized AC parameters versus compensation capacitance. It is suggested that the user check and tailor the accurate compensation value for each application. As shown additional phase margin is achieved at the loss of slew rate and bandwidth.

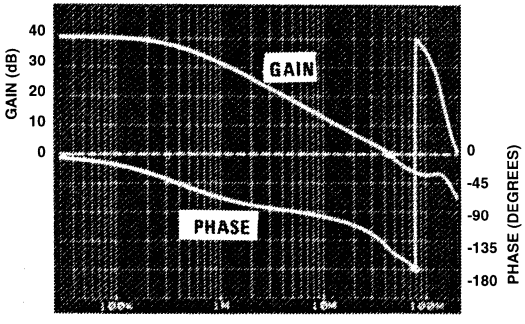
For example, for a voltage gain of +2 (or -1) and a load of 500pF/2kΩ, 20pF is needed for compensation to give a small signal bandwidth of 30MHz with 40° of phase margin. If a full power output voltage of ±10V is needed, this same configuration will provide a bandwidth of 5MHz and a slew rate of 200V/µs.

If maximum bandwidth is desired and no compensation is needed, care must be given to minimize parasitic capacitance at the compensation pin. In some cases where minimum gain applications are desired, bending up or totally removing this pin may be the solution. In this case, care must also be given to minimize load capacitance.

For wideband positive unity gain applications, the HA-2542 can also be over-compensated with capacitance greater than 30pF to achieve bandwidths of around 25MHz. This over-compensation will also improve capacitive load handling or lower the noise bandwidth. This versatility along with the ±100mA output current makes the HA-2542 an excellent high speed driver for many power applications.

Typical Applications



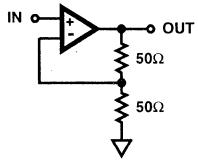


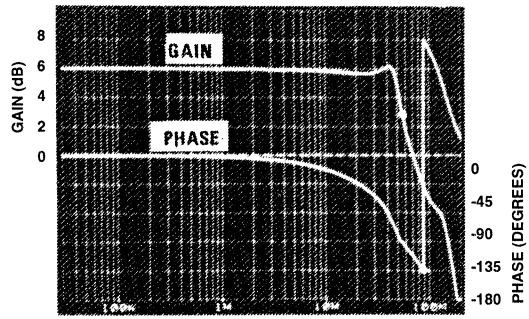
Frequency (0dB) = 44.9MHz,
Phase Margin (0dB) = 40°

FREQUENCY RESPONSE

FIGURE 2. NONINVERTING CIRCUIT (A_{VCL} = 100)

Typical Applications (Continued)

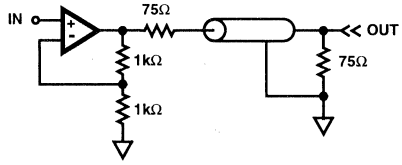


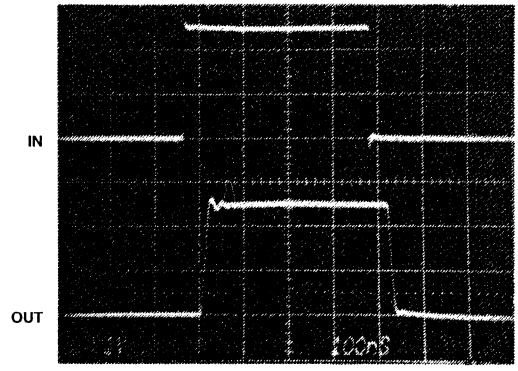


Frequency (dB) = 56MHz, Phase Margin (3dB) = 40°

FREQUENCY RESPONSE

FIGURE 3. NONINVERTING CIRCUIT (A_{VCL} = 2)

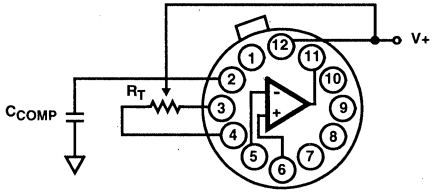




1V/Div.; 100ns/Div.

PULSE RESPONSE

FIGURE 4. VIDEO CABLE DRIVER (A_{VCL} = 2)



NOTES:

16. Suggested compensation scheme 5pF - 20pF.
17. Tested Offset Adjustment Range is $|V_{OS}$ +1mV| minimum referred to output.
18. Typical range is ±20mV with R_T = 5kΩ.

FIGURE 5. SUGGESTED OFFSET VOLTAGE ADJUSTMENT AND FREQUENCY COMPENSATION

Typical Performance Curves

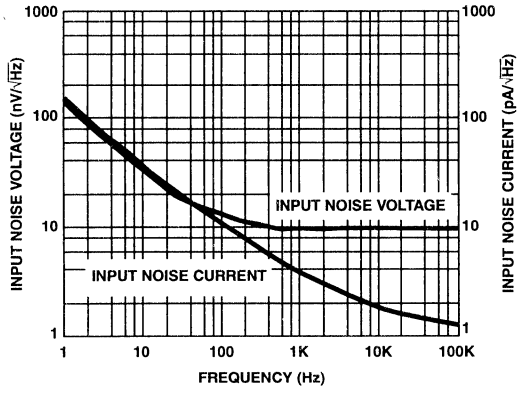


FIGURE 6. INPUT NOISE VOLTAGE AND INPUT NOISE CURRENT vs FREQUENCY

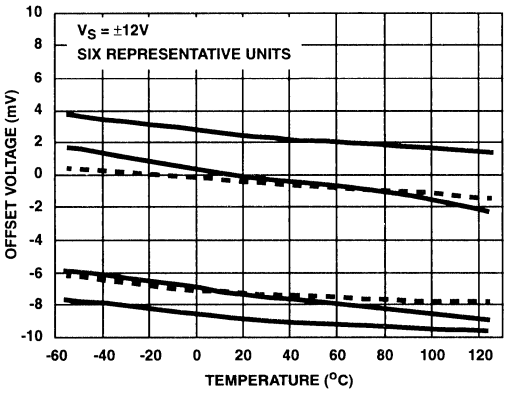


FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE

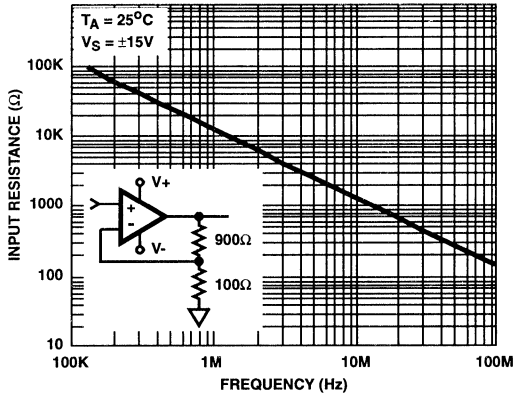


FIGURE 8. INPUT RESISTANCE vs FREQUENCY

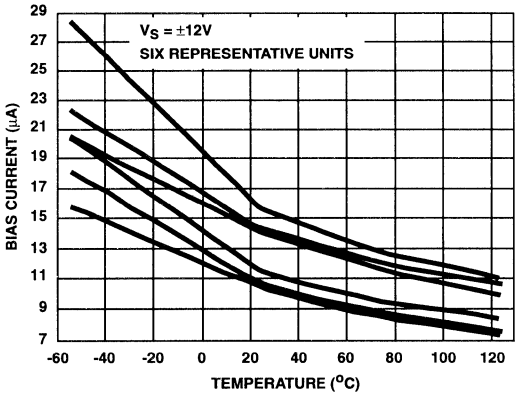


FIGURE 9. BIAS CURRENT vs TEMPERATURE

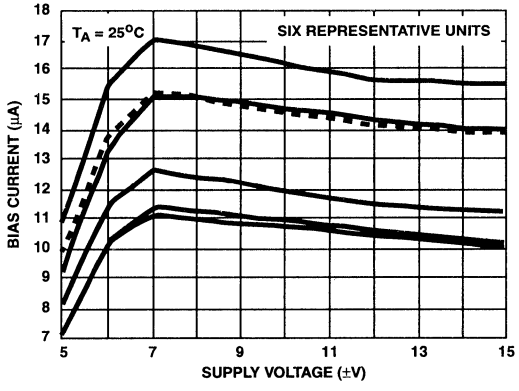


FIGURE 10. BIAS CURRENT vs SUPPLY VOLTAGE

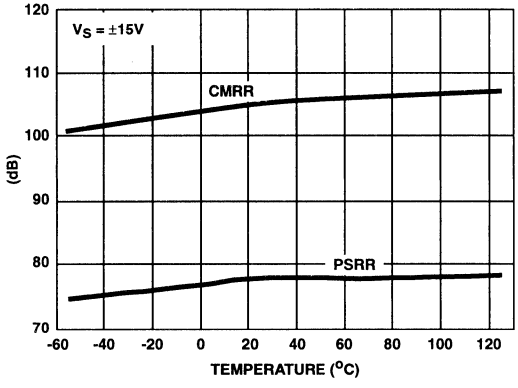


FIGURE 11. PSRR AND CMRR vs TEMPERATURE

Typical Performance Curves (Continued)

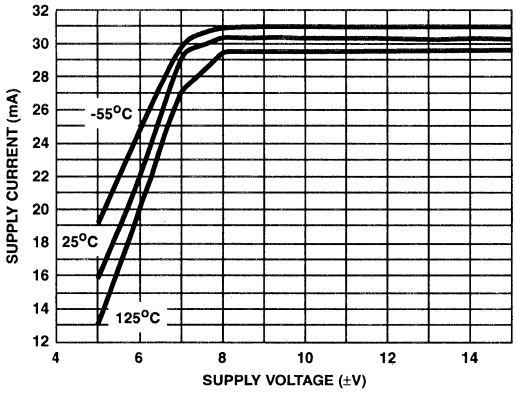


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE, AT VARIOUS TEMPERATURES

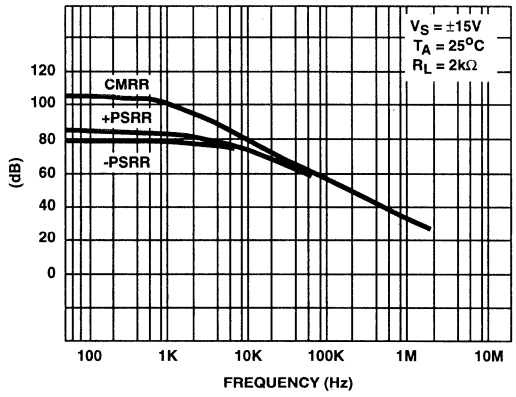


FIGURE 13. PSRR AND CMRR vs FREQUENCY

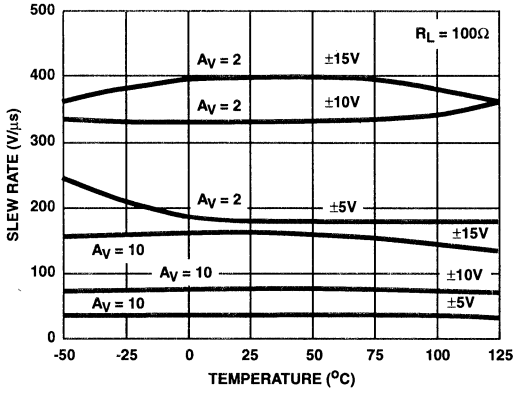


FIGURE 14. SLEW RATE vs TEMPERATURE AT VARIOUS SUPPLY VOLTAGES

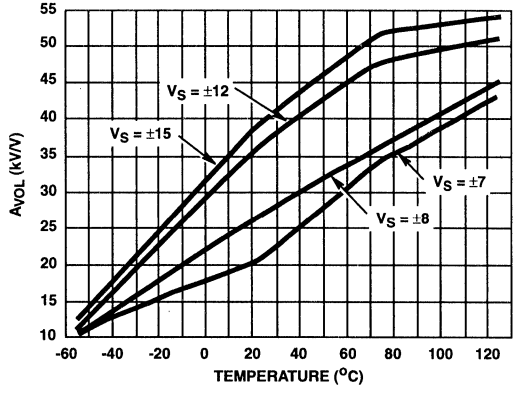


FIGURE 15. OPEN LOOP GAIN vs TEMPERATURE, AT VARIOUS SUPPLY VOLTAGES

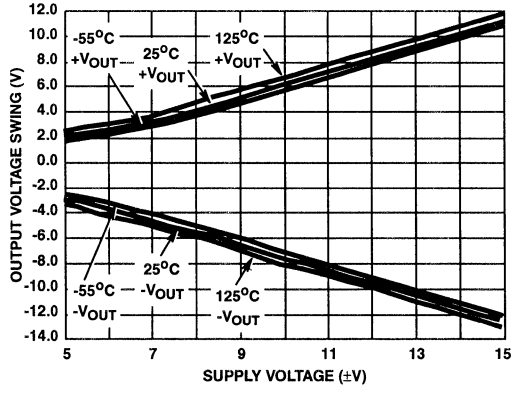


FIGURE 16. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE, AT VARIOUS TEMPERATURES

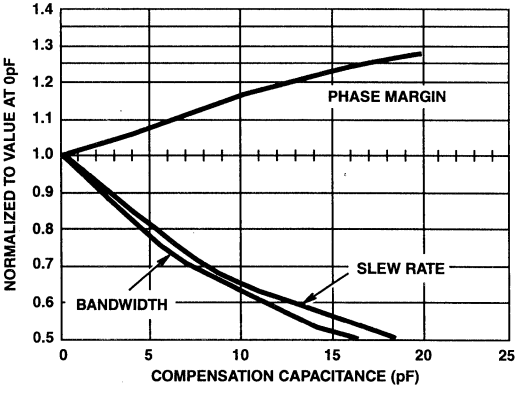


FIGURE 17. NORMALIZED AC PARAMETERS vs COMPENSATION CAPACITANCE

Typical Performance Curves (Continued)

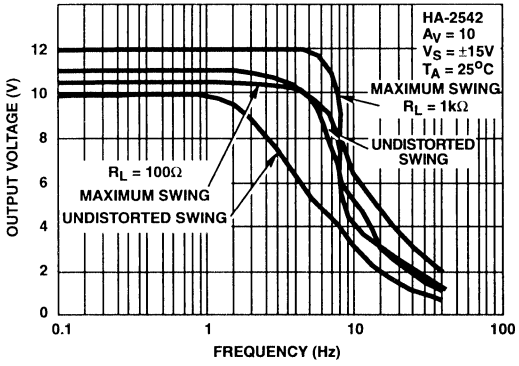


FIGURE 18. OUTPUT VOLTAGE SWING vs FREQUENCY

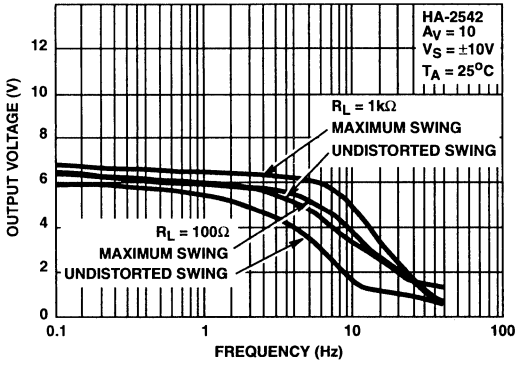


FIGURE 19. OUTPUT VOLTAGE SWING vs FREQUENCY

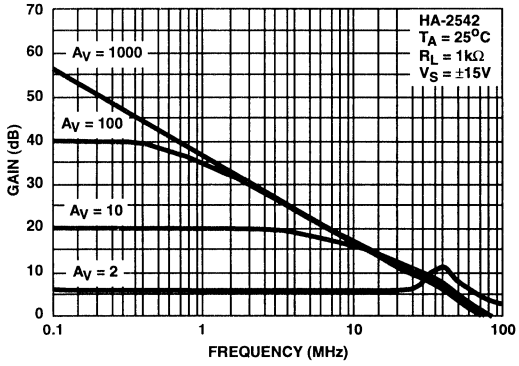


FIGURE 20. FREQUENCY RESPONSE CURVES

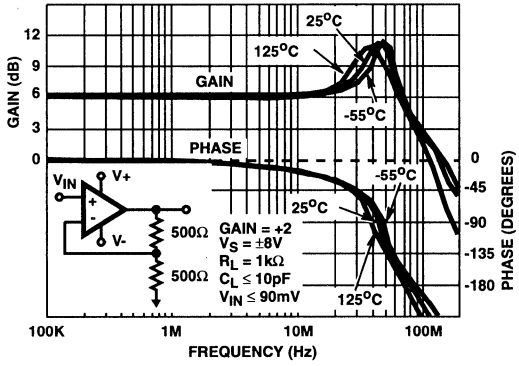


FIGURE 21. HA-2542 CLOSED LOOP GAIN vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

106 mils x 73 mils x 19 mils
2700µm x 1850µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

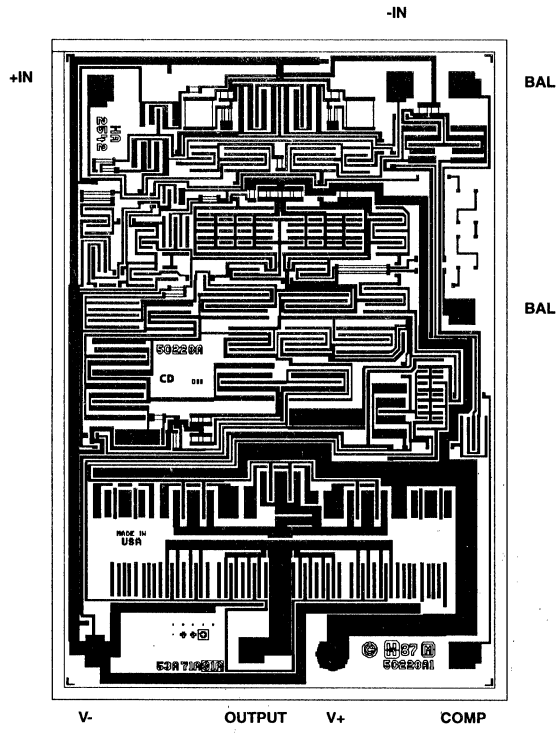
43

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2542



HARRIS SEMICONDUCTOR

HA-2544

November 1996

50MHz, Video Operational Amplifier

Features

- Gain Bandwidth 50MHz
- High Slew Rate 150V/µs
- Low Supply Current 10mA
- Differential Gain Error 0.03%
- Differential Phase Error . . . . . 0.03 Degrees
- Gain Flatness at 10MHz 0.12dB

Applications

- Video Systems
- Video Test Equipment
- Radar Displays
- Data Acquisition Systems
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2544-2	-55 to 125	8 Pin Metal Can	T8.C
HA3-2544-5	0 to 75	8 Ld PDIP	E8.3
HA3-2544C-5	0 to 75	8 Ld PDIP	E8.3
HA7-2544-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2544-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P2544-5 (H25445)	0 to 75	8 Ld SOIC	M8.15
HA9P2544-9 (H25449)	-40 to 85	8 Ld SOIC	M8.15
HA9P2544C-5 (H2544C5)	0 to 75	8 Ld SOIC	M8.15
HA9P2544C-9 (H2544C9)	-40 to 85	8 Ld SOIC	M8.15

Description

The HA-2544 is a fast, unity gain stable, monolithic op amp designed to meet the needs required for accurate reproduction of video or high speed signals. It offers high voltage gain (6kV/V) and high phase margin (65 degrees) while maintaining tight gain flatness over the video bandwidth. Built from high quality Dielectric Isolation, the HA-2544 is another addition to the Harris series of high speed, wideband op amps, and offers true video performance combined with the versatility of an op amp.

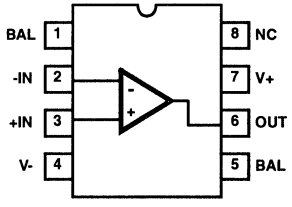
The primary features of the HA-2544 include 50MHz Gain Bandwidth, 150V/µs slew rate, 0.03% differential gain error and gain flatness of just 0.12dB at 10MHz. High performance and low power requirements are met with a supply current of only 10mA.

Uses of the HA-2544 range from video test equipment, guidance systems, radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544 will also be used in non-video systems requiring high speed signal conditioning such as data acquisition systems, medical electronics, specialized instrumentation and communication systems.

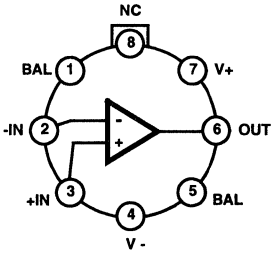
Military (/883) product and data sheets are available upon request.

Pinouts

HA-2544 (PDIP, CERDIP, SOIC)
HA-2544C (PDIP, SOIC)
TOP VIEW



HA-2544
(METAL CAN)
TOP VIEW



3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number **2900.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage (Note 1) 6V
Peak Output Current . . . . . ±40mA

Operating Conditions

Temperature Range
HA-2544/2544C-5 . . . . . 0°C to 75°C
HA-2544/2544C-9 . . . . . -40°C to 85°C
HA-2544-2 . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	160	75
PDIP Package	92	N/A
CERDIP Package	135	50
SOIC Package	157	N/A

Maximum Junction Temperature (Hermetic Packages) . . . . . 175°C
Maximum Junction Temperature (Plastic Packages) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. To achieve optimum AC performance, the input stage was designed without protective diode clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of the input transistors and probable degradation of the input parameters especially V_{OS}, I_{OS} and Noise.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15V, C_L ≤10pF, R_L = 1kΩ, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2544-2, -5, -9			HA-2544C-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	6	15	-	15	25	mV
		-2, -5	-	-	20	-	-	40	mV
		-9	-	-	25	-	-	40	mV
Average Offset Voltage Drift (Note 7)		Full	-	10	-	-	10	-	µV/°C
Bias Current		25	-	7	15	-	9	18	µA
		Full	-	-	20	-	-	30	µA
Average Bias Current Drift (Note 7)		Full	-	0.04	-	-	0.04	-	µA/°C
Offset Current		25	-	0.2	2	-	0.8	2	µA
		Full	-	-	3	-	-	3	µA
Offset Current Drift		Full	-	10	-	-	10	-	nA/°C
Common Mode Range		Full	±10	±11.5	-	±10	±11.5	-	V
Differential Input Resistance		25	50	90	-	50	90	-	kΩ
Differential Input Capacitance		25	-	3	-	-	3	-	pF
Input Noise Voltage	f = 1kHz	25	-	20	-	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current	f = 1kHz	25	-	2.4	-	-	2.4	-	$pA/\sqrt{Hz}$
Input Noise Voltage (Note 7)	0.1Hz to 10Hz	25	-	1.5	-	-	1.5	-	μV_{P-P}
	0.1Hz to 1MHz	25	-	4.6	-	-	4.6	-	μV_{RMS}
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Note 7)	V_O = ±5V	25	3.5	6	-	3	6	-	kV/V
		Full	2.5	-	-	2	-	-	kV/V
Common Mode Rejection Ratio (Note 7)	ΔV_{CM} = ±10V	-2, -5	75	89	-	70	89	-	dB
		-9	75	89	-	65	89	-	dB
Minimum Stable Gain		25	+1	-	-	+1	-	-	V/V
Unity Gain Bandwidth (Note 7)	V_O = ±100mV	25	-	45	-	-	45	-	MHz
Gain Bandwidth Product (Note 7)	V_O = ±100mV	25	-	50	-	-	50	-	MHz
Phase Margin		25	-	65	-	-	65	-	Degrees

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L \leq 10pF$, $R_L = 1k\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2544-2, -5, -9			HA-2544C-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS									
Output Voltage Swing		Full	±10	±11	-	±10	±11	-	V
Full Power Bandwidth (Note 6)		25	3.2	4.2	-	3.2	4.2	-	MHz
Peak Output Current (Note 7)		25	±25	±35	-	±25	±35	-	mA
Continuous Output Current (Note 7)		25	±10	-	-	±10	-	-	mA
Output Resistance	Open Loop	25	-	20	-	-	20	-	Ω
TRANSIENT RESPONSE									
Rise Time (Note 4)		25	-	7	-	-	7	-	ns
Overshoot (Note 4)		25	-	10	-	-	10	-	%
Slew Rate		25	100	150	-	100	150	-	V/µs
Settling Time (Note 5)		25	-	120	-	-	120	-	ns
VIDEO PARAMETERS $R_L = 1k\Omega$ (Note 8)									
Differential Phase (Note 9)		25	-	0.03	-	-	0.03	-	Degree
Differential Gain (Notes 3, 9)		25	-	0.0026	-	-	0.0026	-	dB
		25	-	0.03	-	-	0.03	-	%
Gain Flatness	5MHz	25	-	0.10	-	-	0.10	-	dB
	10MHz	25	-	0.12	-	-	0.12	-	dB
Chrominance to Luminance Gain (Note 10)		25	-	0.1	-	-	0.1	-	dB
Chrominance to Luminance Delay (Note 10)		25	-	7	-	-	7	-	ns
POWER SUPPLY CHARACTERISTICS									
Supply Current		Full	-	10	12	-	10	15	mA
Power Supply Rejection Ratio (Note 7)	$V_S = \pm10V$ to $\pm20V$	-2, -5	70	80	-	70	80	-	dB
		-9	65	80	-	65	80	-	dB

NOTES:

3. $A_D(\%) = \left[10^{\frac{A_D(dB)}{20}} - 1\right] \times 100.$

4. For Rise Time and Overshoot testing, V_{OUT} is measured from 0 to +200mV and 0 to -200mV.

5. Settling Time is specified to 0.1% of final value for a 10V step and $A_V = -1$.

6. Full Power Bandwidth is guaranteed by equation: Full Power Bandwidth $= \frac{\text{Slew Rate}}{2\pi V_{PEAK}} (V_{PEAK} = 5V)$.

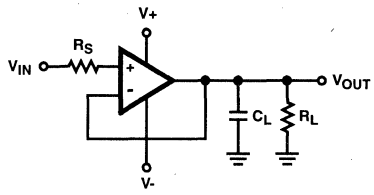
7. Refer to typical performance curve in Data Sheet.

8. The video parameter specifications will degrade as the output load resistance decreases.

9. Tested with a VM700A video tester, using a NTC-7 Composite input signal. For adequate test repeatability, a minimum warm-up of 2 minutes is suggested. $A_V = +1$.

10. C-L Gain and C-L Delay was less than the resolution of the test equipment used which is 0.1dB and 7ns, respectively.

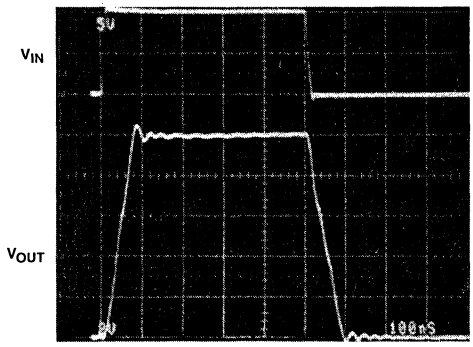
Test Circuits and Waveforms



NOTES:

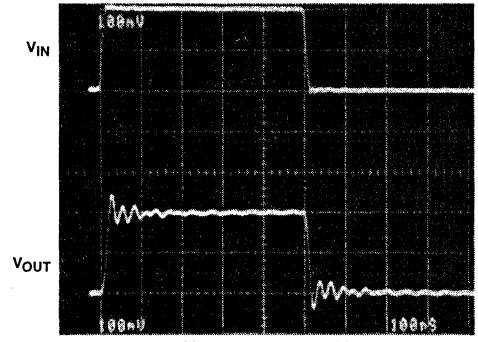
11. $V_S = \pm 15V$.
12. $A_V = +1$.
13. $R_S = 50\Omega$ or 75Ω (Optional).
14. $R_L = 1k\Omega$.
15. $C_L < 10pF$.
16. V_{IN} for Large Signal = $\pm 5V$.
17. V_{IN} for Small Signal = 0 to +200mV and 0 to -200mV.

FIGURE 1. TRANSIENT RESPONSE



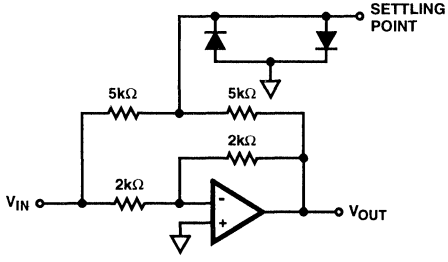
V_{OUT} = 0 to +10V
Vertical Scale: V_{IN} = 5V/Div.; V_{OUT} = 2V/Div.
Horizontal Scale: 100ns/Div.

LARGE SIGNAL RESPONSE



V_{OUT} = 0 to +200mV
Vertical Scale: V_{IN} = 100mV/Div.; V_{OUT} = 100mV/Div.
Horizontal Scale: 100ns/Div.

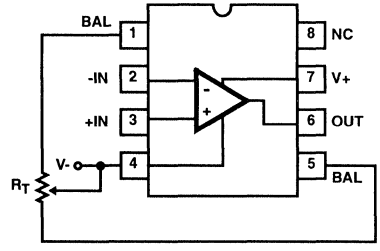
SMALL SIGNAL RESPONSE



NOTES:

18. $A_V = -1$.
19. Feedback and summing resistor ratios should be 0.1% matched.
20. HP5082-2810 clipping diodes recommended.
21. Tektronix P6201 FET probe used at settling point.

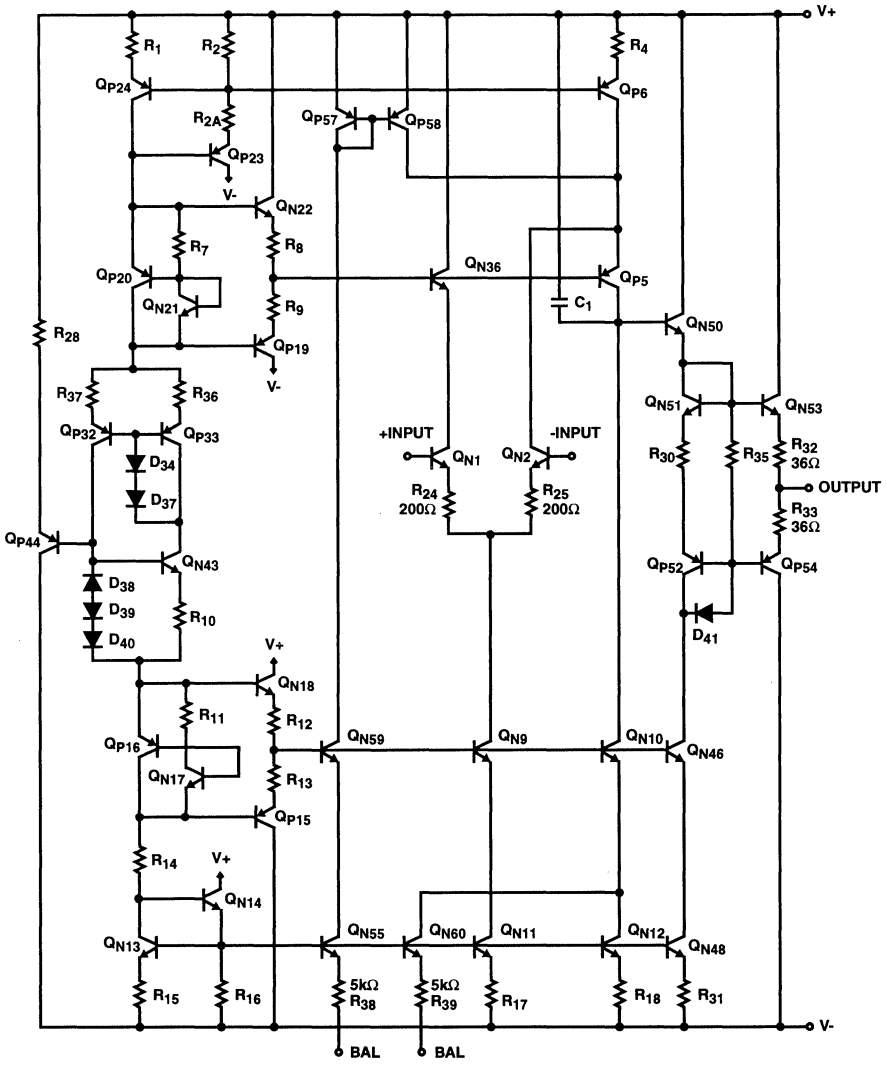
FIGURE 2. SETTLING TIME TEST CIRCUIT



NOTE: Tested offset adjustment range is $|V_{OS}| + 1mV|$ minimum referred to output. Typical range for $R_T = 20k\Omega$ is approximately $\pm 30mV$.

FIGURE 3. OFFSET VOLTAGE ADJUSTMENT

Schematic Diagram



Application Information

The HA-2544 is a true differential op amp that is as versatile as any op amp but offers the advantages of high unity gain bandwidth, high speed and low supply current. More important than its general purpose applications is that the HA-2544 was especially designed to meet the requirements found in a video amplifier system. These requirements include fine picture resolution and accurate color rendition, and must meet broadcast quality standards.

In a video signal, the video information is carried in the amplitude and phase as well as in the DC level. The amplifier must pass the 30Hz line rate luminance level and the 3.58MHz (NTSC) or 4.43MHz (PAL) color band without altering phase or gain. The HA-2544's key specifications aimed at meeting this include high bandwidth (50MHz), very low gain flatness (0.12dB at 10MHz), near unmeasurable differential gain and differential phase (0.03% and 0.03 degrees), and low noise (20nV/√Hz). The HA-2544 meets these quidelines.

The HA-2544 also offers the advantage of a full output voltage swing of ±10V into a 1kΩ load. This equates to a full power bandwidth of 2.4MHz for this ±10V signal. If video signal levels of ±2V maximum is used (with R_L = 1kΩ), the full power bandwidth would be 11.9MHz without clipping distortion. Another usage might be required for a direct 50Ω or 75Ω load where the HA-2544 will still swing this ±2V signal as shown in the above display. One important note that must be realized is that as load resistance decreases the video parameters are also degraded. For optimal video performance a 1kΩ load is recommended.

If lower supply voltages are required, such as ±5V, many of the characterization curves indicate where the parameters vary. As shown the bandwidth, slew rate and supply current are still very well maintained.

Prototyping and PC Board Layout

When designing with the HA-2544 video op amp as with any high performance device, care should be taken to use high frequency layout techniques to avoid unwanted parasitic effects. Short lead lengths, low source impedance and lower value feedback resistors help reduce unwanted poles or zeros. This layout would also include ground plane construction and power supply decoupling as close to the supply pins with suggested parallel capacitors of 0.1µF and 0.001µF ceramic to ground.

In the noninverting configuration, the amplifier is sensitive to stray capacitance (<40pF) to ground at the inverting input. Therefore, the inverting node connections should be kept to a minimum. Phase shift will also be introduced as load parasitic capacitance is increased. A small series resistor (20Ω to 100Ω) before the capacitance effectively decouples this effect.

Stability/Phase Margin/Compensation

The HA-2544 has not sacrificed unity gain stability in achieving its superb AC performance. For this device, the phase margin exceeds 60 degrees at the unity crossing point of the open loop frequency response. Large phase margin is critical in order to reduce the differential phase and differential gain errors caused by most other op amps. Because this part is unity gain stable, no compensation pin is brought out. If compensation is desired to reduce the noise bandwidth, most standard methods may be used. One method suggested for an inverting scheme would be a series R-C from the inverting node to ground which will reduce bandwidth, but not effect slew rate. If the user wishes to achieve even higher bandwidth (>50MHz), and can tolerate some slight gain peaking and lower phase margin, experimenting with various load capacitance can be done.

Shown in Application 1 is an excellent Differential Input, Unity Gain Buffer which also will terminate a cable to 75Ω and reject common mode voltages. Application 2 is a method of separating a video signal up into the Sync only signal and the Video and Blanking signal. Application 3 shows the HA-2544 being used as a 100kHz High Pass 2-Pole Butterworth Filter. Also shown is the measured frequency response curves.

Typical Applications

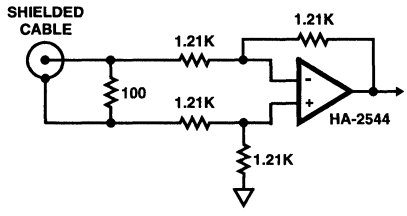


FIGURE 4. APPLICATION 1, 75Ω DIFFERENTIAL INPUT BUFFER

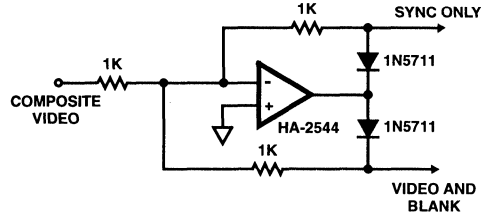


FIGURE 5. APPLICATION 2, COMPOSITE VIDEO SYNC SEPARATOR

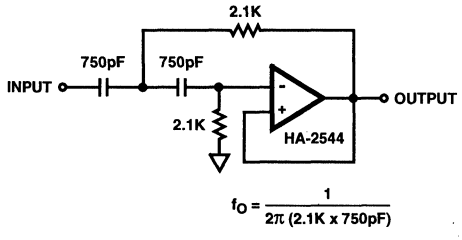


FIGURE 6. APPLICATION 3, 100kHz HIGH PASS 2-POLE BUTTERWORTH FILTER

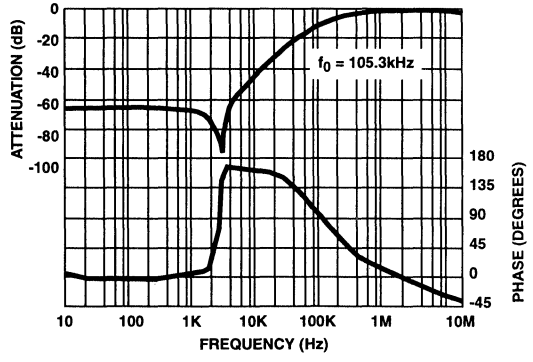


FIGURE 7. MEASURED FREQUENCY RESPONSE OF APPLICATION 3

Typical Performance Curves

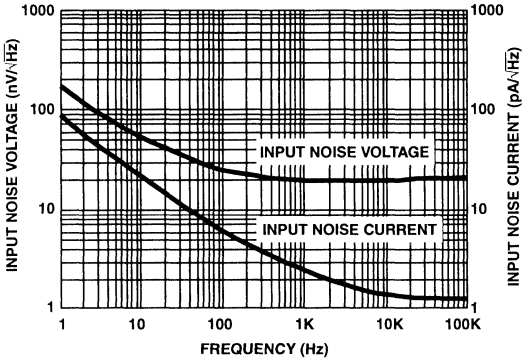


FIGURE 8. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

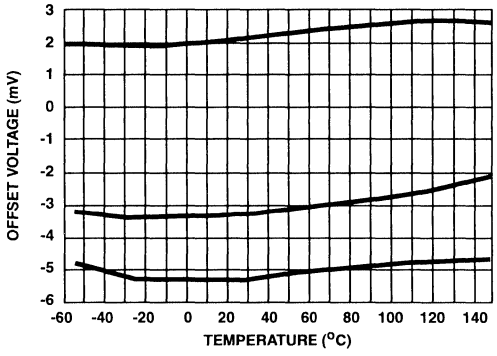
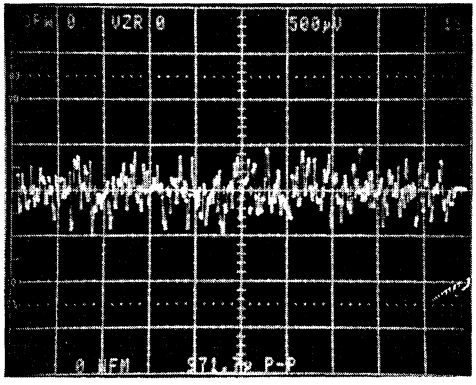


FIGURE 9. INPUT OFFSET VOLTAGE vs TEMPERATURE (3 TYPICAL UNITS)



0.1Hz to 10Hz, Noise Voltage = 0.97μV_{P-P}

FIGURE 10. NOISE VOLTAGE (A_V = 1000)

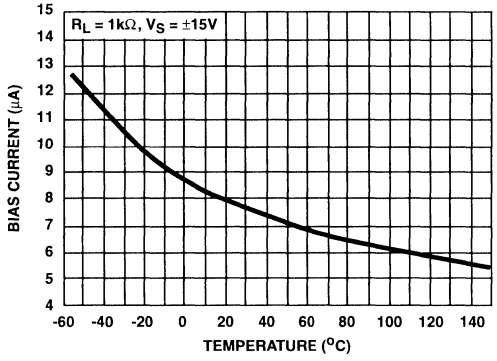


FIGURE 11. INPUT BIAS CURRENT vs TEMPERATURE

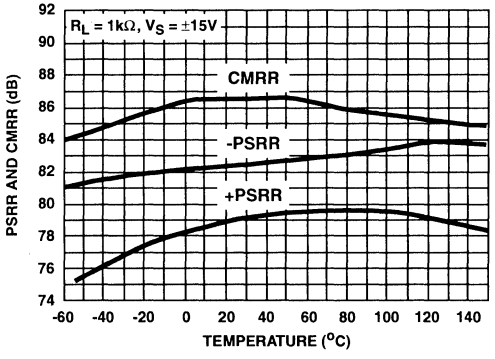


FIGURE 12. PSRR AND CMRR vs TEMPERATURE

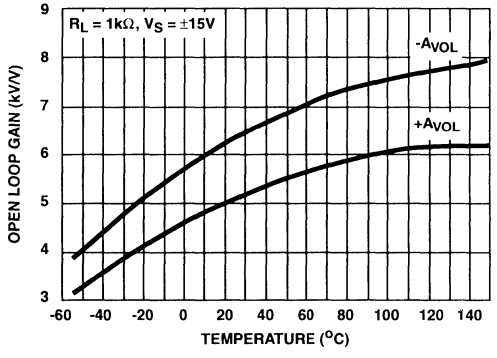


FIGURE 13. OPEN LOOP GAIN vs TEMPERATURE

Typical Performance Curves (Continued)

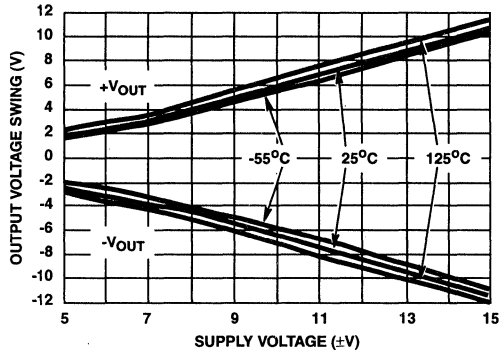


FIGURE 14. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

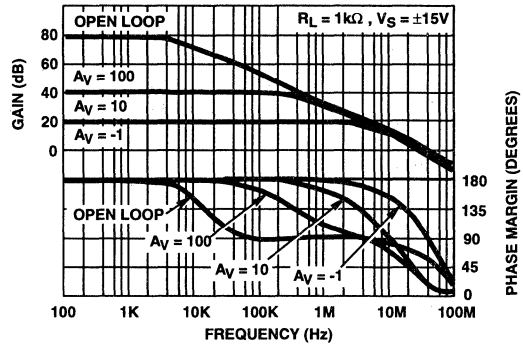


FIGURE 15. FREQUENCY RESPONSE AT VARIOUS GAINS

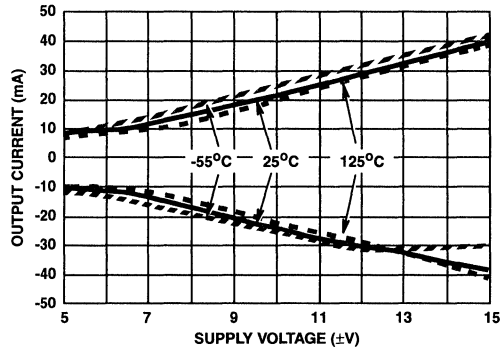


FIGURE 16. OUTPUT CURRENT vs SUPPLY VOLTAGE

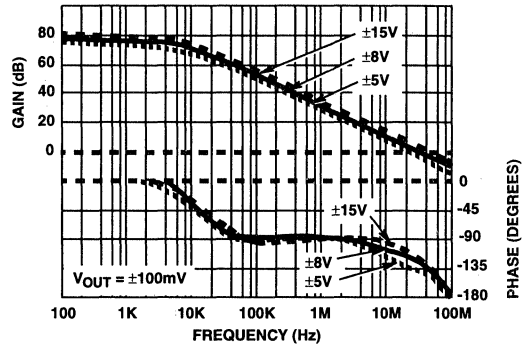


FIGURE 17. OPEN LOOP RESPONSE

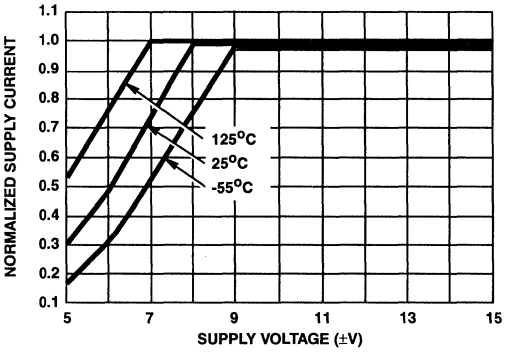


FIGURE 18. SUPPLY CURRENT vs SUPPLY VOLTAGE (NORMALIZED TO V_S = ±15V AT 25°C)

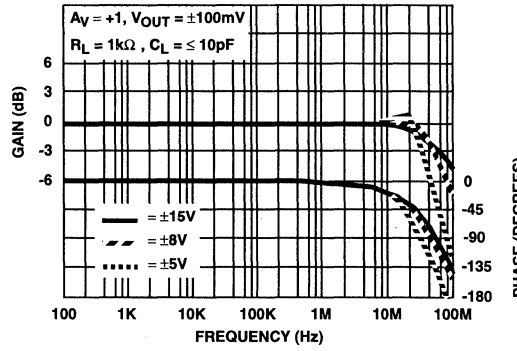


FIGURE 19. VOLTAGE FOLLOWER RESPONSE

Typical Video Performance Curves

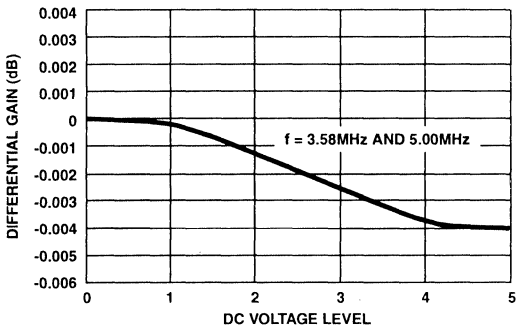


FIGURE 20. AC GAIN VARIATION vs DC OFFSET LEVELS (DIFFERENTIAL GAIN)

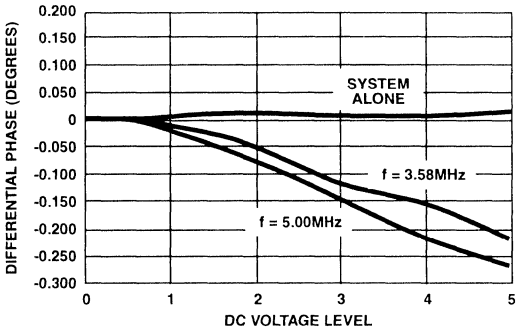
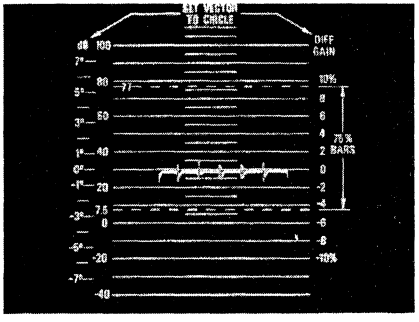
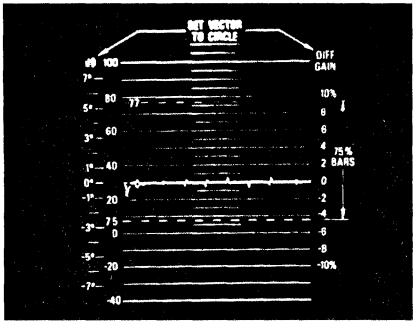


FIGURE 21. AC PHASE VARIATION vs DC OFFSET LEVELS (DIFFERENTIAL PHASE)



NTSC Method, R_L = 1kΩ, Differential Gain <0.05% at T_A = 75°C
No Visual Difference at T_A = -55°C or 125°C

FIGURE 22. DIFFERENTIAL GAIN



NTSC Method, R_L = 1kΩ,
Differential Phase < 0.05 Degree at T_A = 75°C
No Visual Difference at T_A = -55°C or 125°C

FIGURE 23. DIFFERENTIAL PHASE

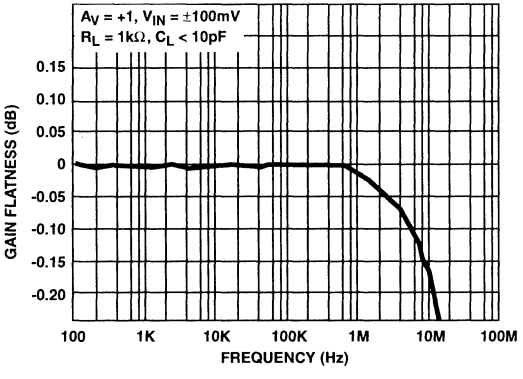
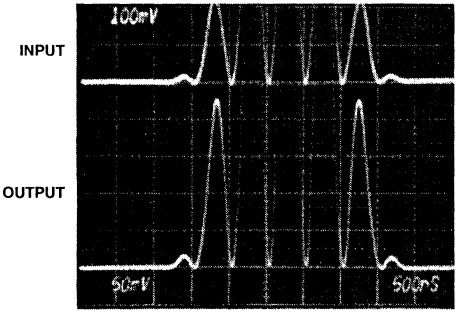


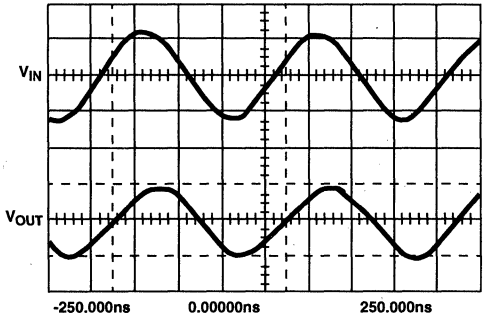
FIGURE 24. GAIN FLATNESS



NTSC Method, R_L = 1kΩ, C-L Delay <7ns at T_A = 75°C
No Visual Difference at T_A = -55°C or 125°C
Vertical Scale: Input = 100mV/Div., Output = 50mV/Div.
Horizontal Scale: 500ns/Div.

FIGURE 25. CHROMINANCE TO LUMINANCE DELAY

Typical Video Performance Curves (Continued)



V_{IN} = 2.0V/Div., V_{OUT} = 2.0V/Div., Timebase = 50ns

FIGURE 26. ±2V OUTPUT SWING (WITH R_{LOAD} = 75Ω, FREQUENCY = 5.00MHz)

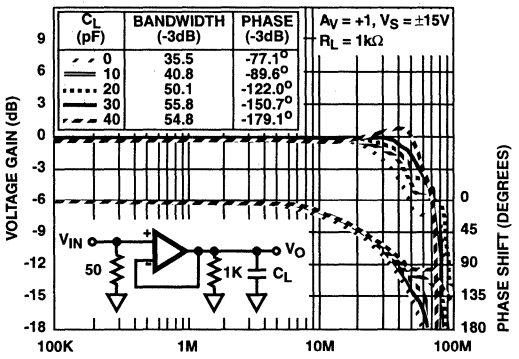


FIGURE 27. BANDWIDTH vs LOAD CAPACITANCE

Die Characteristics

DIE DIMENSIONS:

80 mils x 64 mils x 19 mils
2030µm x 1630µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

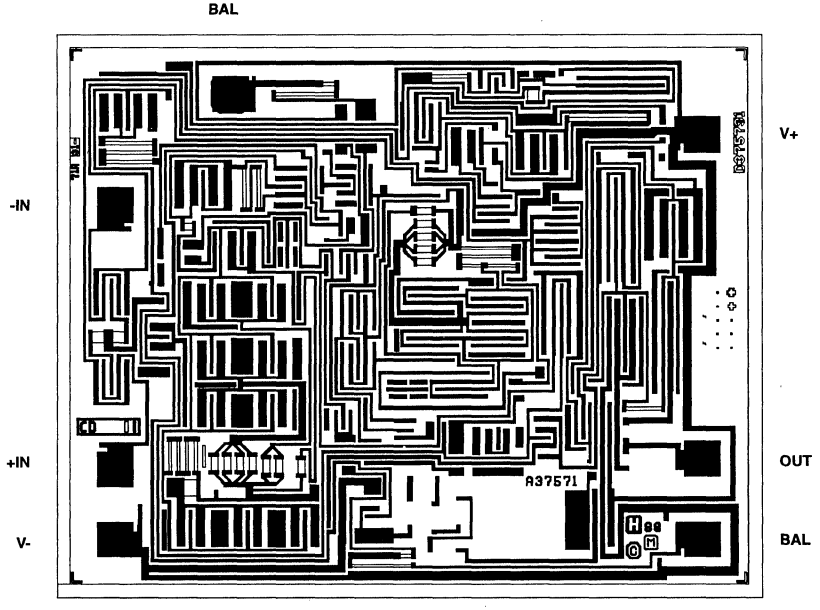
44

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2544



NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

November 1996

HA-2548

150MHz, High Slew Rate, Precision Operational Amplifier

Features

- High Slew Rate 120V/µs
- Low Offset Voltage 300µV
- High Open Loop Gain 130dB
- Gain Bandwidth Product 150MHz
- Low Noise Voltage at 1kHz ..... 8.3nV/√Hz
- Minimum Gain Stability ..... ≥5

Applications

- High Speed Instrumentation
- Data Acquisition Systems
- Analog Signal Conditioning
- Precision, Wideband Amplifiers
  - Pulse/RF Amplifiers

Description

The HA-2548 is an op amp that offers a unique combination of bandwidth, slew rate, and precision specifications. These features can eliminate the need for composite op amp designs and external calibration circuitry.

Optimized for gains ≥5, the HA-2548 has a gain-bandwidth product of 150MHz and a slew rate of 120V/µs while maintaining extremely high open loop gain (130dB Typ) and low offset voltage (300µV Typ). These specifications are achieved through uniquely designed input circuitry and a single ultra-high gain stage that minimizes the AC signal path. Capable of delivering over 30mA of output current, the HA-2548 is ideal for precision, high speed applications such as signal conditioning, instrumentation, video/pulse amplifiers and buffers.

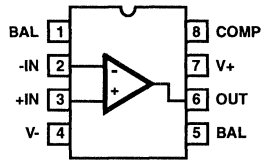
For information on the military version of this device please refer to the HA-2548/883 datasheet.

Ordering Information

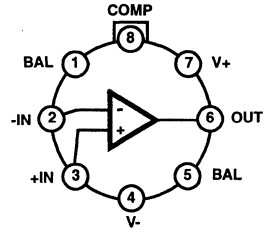
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2548-5	0 to 75	8 Pin Metal Can	T8.C
HA2-2548-9	-40 to 85	8 Pin Metal Can	T8.C
HA3-2548-5	0 to 75	8 Ld PDIP	E8.3
HA7-2548-5	0 to 75	8 Ld SBDIP	D8.3
HA9P2548-5	0 to 75	16 Ld SOIC	M16.3

Pinouts

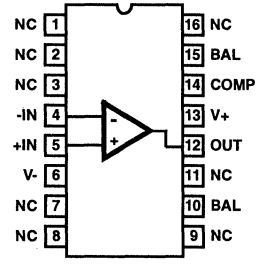
HA-2548 (PDIP, SBDIP) TOP VIEW



HA-2548 (METAL CAN) TOP VIEW



HA-2548 (SOIC) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2901.2**

HA-2600, HA-2602, HA-2605

12MHz, High Input Impedance Operational Amplifiers

November 1996

Features

- Bandwidth 12MHz
- High Input Impedance 500MΩ
- Low Input Bias Current 1nA
- Low Input Offset Current 1nA
- Low Input Offset Voltage 0.5mV
- High Gain 150kV/V
- Slew Rate 7V/μs
- Output Short Circuit Protection
- Unity Gain Stable

Applications

- Video Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High-Speed Comparators
- Low Distortion Oscillators

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2600-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2602-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2605-5	0 to 75	8 Pin Metal Can	T8.C
HA3-2605-5	0 to 75	8 Ld PDIP	E8.3
HA7-2600-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2602-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2605-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P2605-5 (H26055)	0 to 75	8 Ld SOIC	M8.15

Description

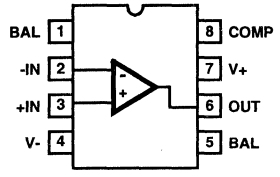
HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth, 7V/μs slew rate and 150kV/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 are particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Note AN515.

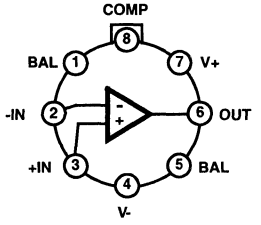
The HA-2600 and HA-2602 are offered as /883 Military Grade; product and data sheets are available upon request.

Pinouts

HA-2600/02 (CERDIP)
HA-2605 (PDIP, CERDIP, SOIC)
TOP VIEW



HA-2600/02/05
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2902.2**

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 45V
Differential Input Voltage 12V
Peak Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-2600/HA-2602-2 . . . . . -55°C to 125°C
HA-2605-5 . . . . . 0°C to 75°C
HA-2605-9 . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	165	80
PDIP Package	96	N/A
CERDIP Package	135	50
SOIC Package	157	N/A

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified

PARAMETER	TEMP. (°C)	HA-2600-2			HA-2602-2			HA-2605-9 HA-2605-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	25	-	0.5	4	-	3	5	-	3	5	mV
	Full	-	2	6	-	-	7	-	-	7	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	-	5	-	µV/°C
Bias Current (Note 2)	25	-	1	10	-	15	25	-	5	25	nA
	Full	-	10	30	-	-	60	-	-	40	nA
Offset Current (Note 2)	25	-	1	10	-	5	25	-	5	25	nA
	Full	-	5	30	-	-	60	-	-	40	nA
Differential Input Resistance (Note 12)	25	100	500	-	40	300	-	40	300	-	MΩ
Input Noise Voltage Density (f = 1kHz)	25	-	11	-	-	11	-	-	11	-	nV/√Hz
Input Noise Current Density (f = 1kHz)	25	-	0.16	-	-	0.16	-	-	0.16	-	pA/√Hz
Common Mode Range	Full	±11	±12	-	±11	±12	-	±11	±12	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 3, 6)	25	100	150	-	80	150	-	80	150	-	kV/V
	Full	70	-	-	60	-	-	70	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	80	100	-	74	100	-	74	100	-	dB
Minimum Stable Gain	25	1	-	-	1	-	-	1	-	-	V/V
Gain Bandwidth Product (Note 5)	25	-	12	-	-	12	-	-	12	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 6)	25	±15	±22	-	±10	±18	-	±10	±18	-	mA
Full Power Bandwidth (Notes 6, 13)	25	50	75	-	50	75	-	50	75	-	kHz
TRANSIENT RESPONSE (Note 10)											
Rise Time (Notes 3, 7, 8, 9)	25	-	30	60	-	30	60	-	30	60	ns
Overshoot (Notes 3, 7, 8, 9)	25	-	25	40	-	25	40	-	25	40	%
Slew Rate (Notes 3, 7, 9, 14)	25	±4	±7	-	±4	±7	-	±4	±7	-	V/µs
Settling Time (Notes 3, 7, 15)	25	-	1.5	-	-	1.5	-	-	1.5	-	µs

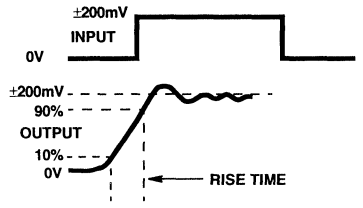
Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP. (°C)	HA-2600-2			HA-2602-2			HA-2605-9 HA-2605-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS											
Supply Current	25	-	3	3.7	-	3	4	-	3	4	mA
Power Supply Rejection Ratio (Note 11)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

2. Typical and minimum specifications for -9 are identical to those of -5. All maximum specifications for -9 are identical to those of -5 except for Full Temperature Bias and Offset Currents, which are 70nA Max.
3. R_L = 2kΩ.
4. V_{CM} = ±10V.
5. V_{OUT} < 90mV.
6. V_{OUT} = ±10V.
7. C_L = 100pF.
8. V_{OUT} = ±200mV.
9. A_V = +1.
10. See Transient Response Test Circuits and Waveforms.
11. ΔV_S = ±5V.
12. This parameter value guaranteed by design calculations.
13. Full Power Bandwidth guaranteed by slew rate measurement: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
14. V_{OUT} = ±5V
15. Settling time is characterized at A_V = -1 to 0.1% of a 10V step.

Test Circuits and Waveforms



NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 1. TRANSIENT RESPONSE

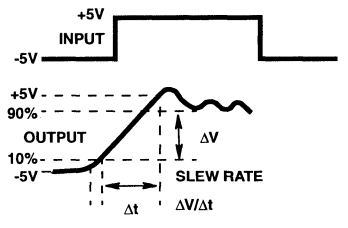


FIGURE 2. SLEW RATE

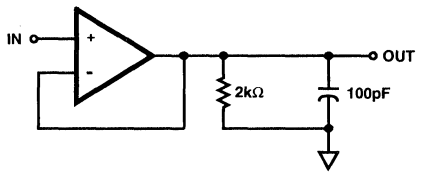
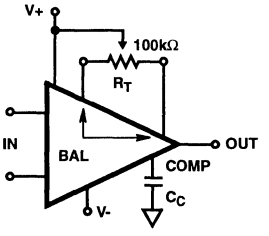


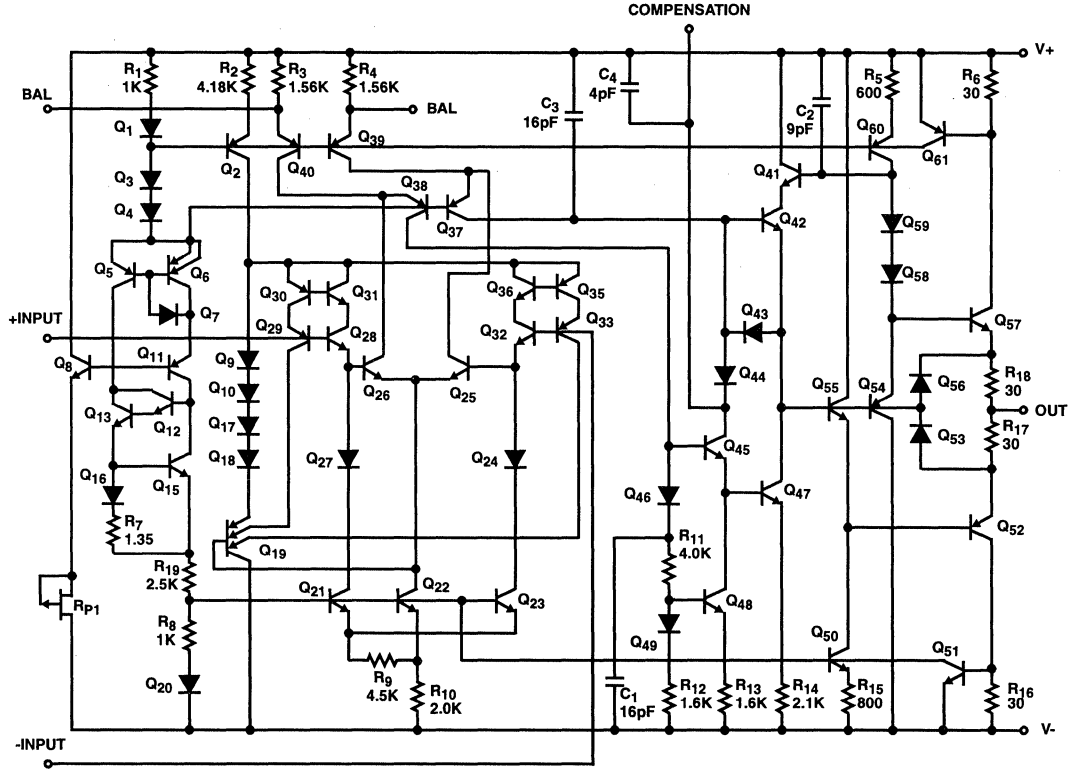
FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



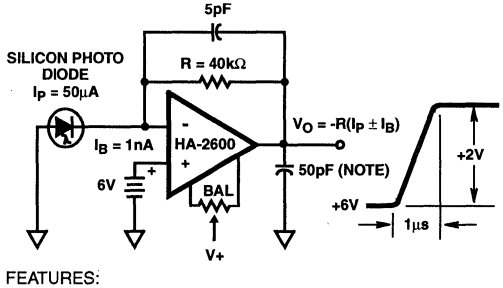
NOTE: Tested offset adjustment range is $|V_{OS}$ + 1mV| minimum referred to output. Typical ranges are ±10mV with R_T = 100kΩ.

FIGURE 4. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Schematic Diagram

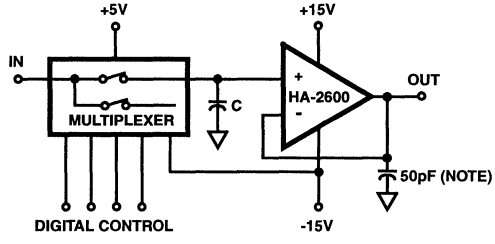


Typical Applications



FEATURES:

1. Constant cell voltage.
2. Minimum bias current error.



$$\text{DRIFT RATE} = \frac{I_{BIAS}}{C}$$

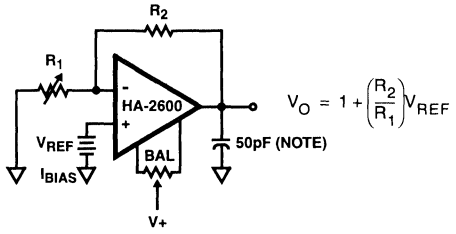
If C = 1000pF
Then DRIFT = 0.01V/µs (Max)

NOTE: A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

FIGURE 5. PHOTO CURRENT TO VOLTAGE CONVERTER

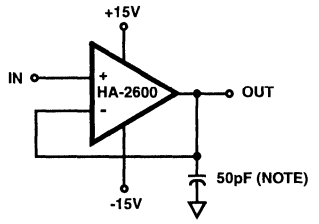
FIGURE 6. SAMPLE AND HOLD

Typical Applications (Continued)



FEATURES:
1. Minimum bias current in reference cell.
2. Short Circuit Protection.

FIGURE 7. REFERENCE VOLTAGE AMPLIFIER



FEATURES
1. $Z_{IN} = 10^{12}\Omega$ (Min).
2. $Z_{OUT} = 0.01\Omega$ (Max), B.W. = 12MHz (Typ).
3. Slew Rate = 4V/µs (Min), Output Swing = ±10V (Min) to 50kHz.

FIGURE 8. VOLTAGE FOLLOWER

NOTE: A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$, Unless Otherwise Specified

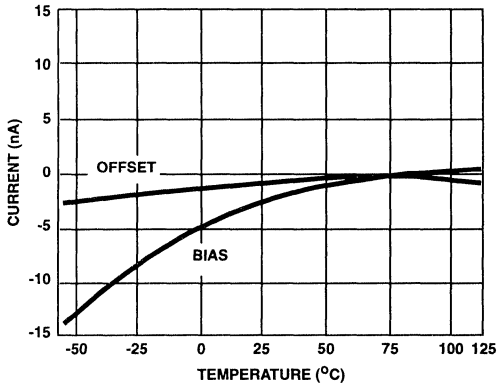


FIGURE 9. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

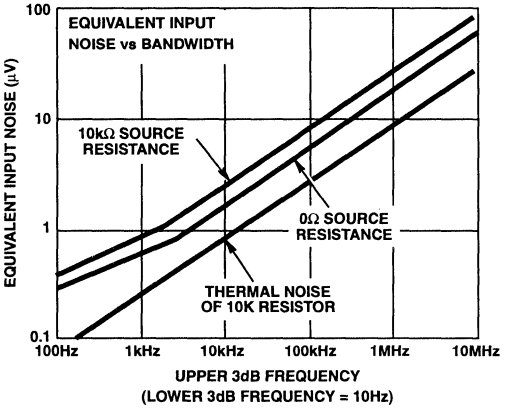


FIGURE 10. BROADBAND NOISE CHARACTERISTICS

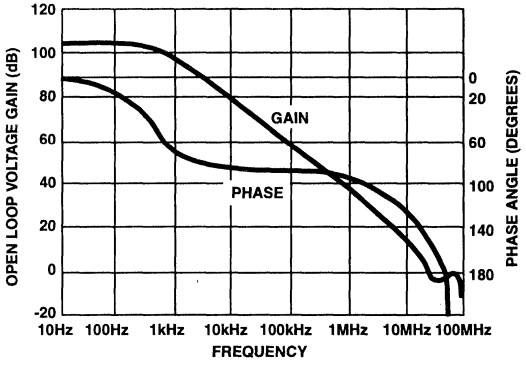


FIGURE 11. OPEN LOOP FREQUENCY RESPONSE

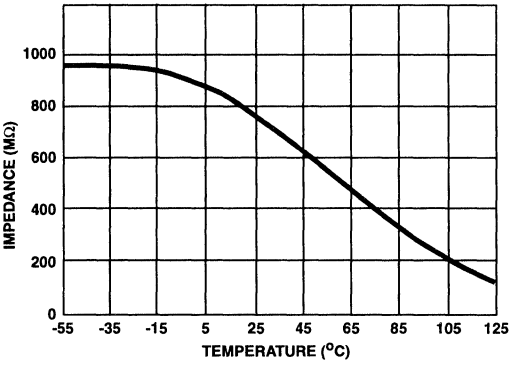


FIGURE 12. INPUT IMPEDANCE vs TEMPERATURE (100Hz)

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

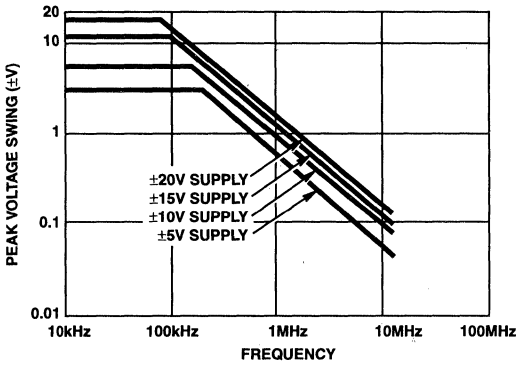
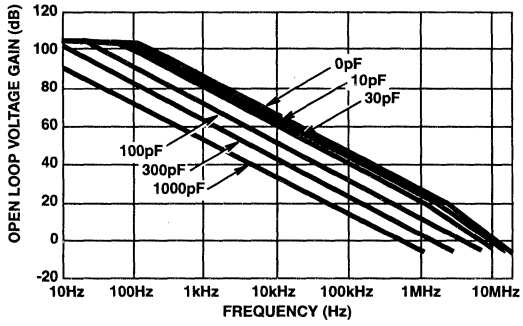


FIGURE 13. OUTPUT VOLTAGE SWING vs FREQUENCY



NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired. If External Compensation is used, also connect 100pF capacitor from output to ground.

FIGURE 14. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

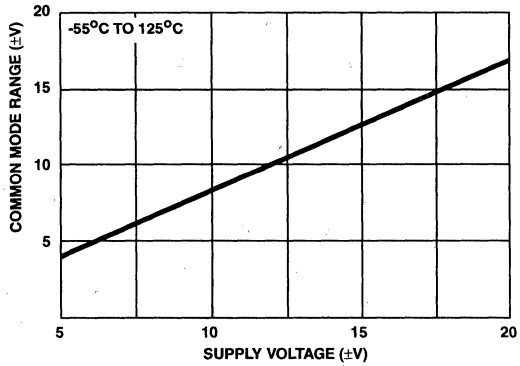


FIGURE 15. COMMON MODE VOLTAGE RANGE vs SUPPLY VOLTAGE

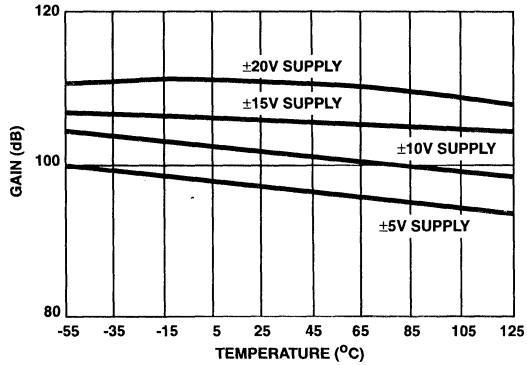


FIGURE 16. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

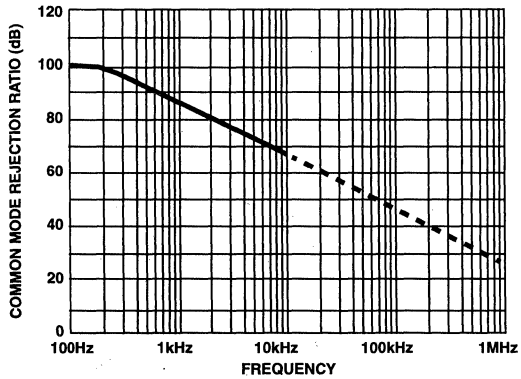


FIGURE 17. COMMON MODE REJECTION RATIO vs FREQUENCY

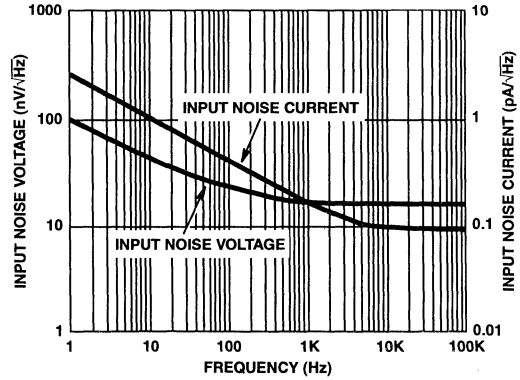


FIGURE 18. NOISE DENSITY vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

69 mils x 56 mils x 19 mils
1750µm x 1420µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

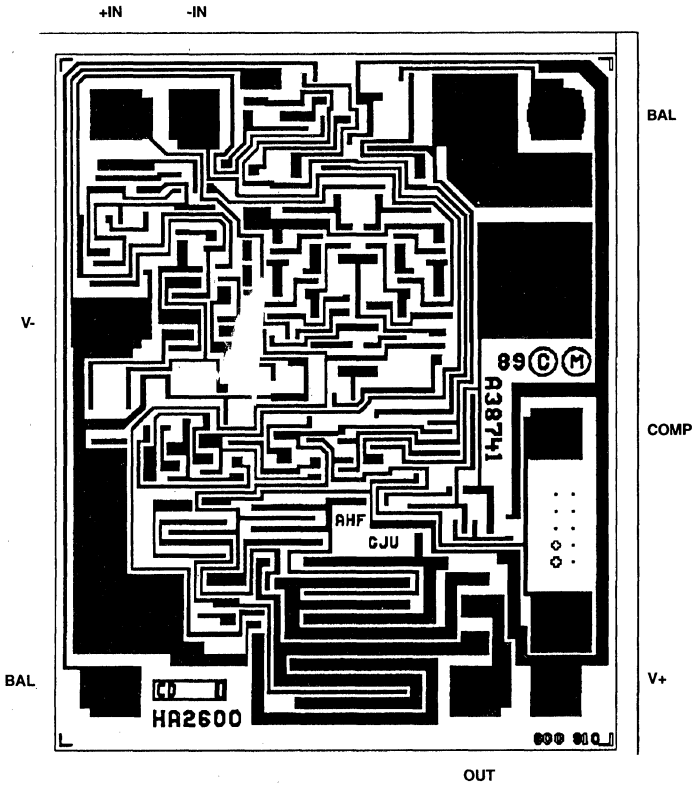
140

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2600, HA-2602, HA-2605



HARRIS SEMICONDUCTOR

HA-2620, HA-2622, HA-2625

100MHz, High Input Impedance, Very Wideband, Uncompensated Operational Amplifiers

November 1996

Features

- Gain Bandwidth Product ($A_V \geq 5$) 100MHz
- High Input Impedance 500MΩ
- Low Input Bias Current 1nA
- Low Input Offset Current 1nA
- Low Input Offset Voltage 0.5mV
- High Gain 150kV/V
- Slew Rate 35V/μs
- Output Short Circuit Protection

Applications

- Video and RF Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High Speed Comparators
- Low Distortion Oscillator

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2620-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2622-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2625-5	0 to 75	8 Pin Metal Can	T8.C
HA3-2625-5	0 to 75	8 Ld PDIP	E8.3
HA7-2620-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2622-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2625-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P2625-5 (H26255)	0 to 75	8 Ld SOIC	M8.15
HA9P2625-9 (H26259)	-40 to 85	8 Ld SOIC	M8.15

Description

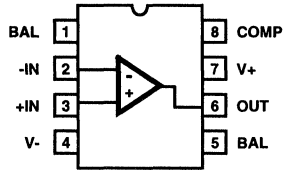
HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. The 100MHz gain bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/μs slew rate and 150kV/V open loop gain enables HA-2620/2622/2625 to perform high gain amplification of very fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g., video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor connected from the Comp pin to GND.

In addition to its application in pulse and video amplifier designs, HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Notes AN509, AN519 and AN546.

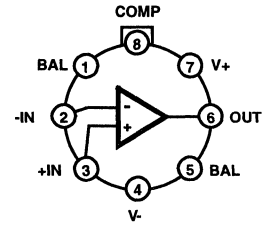
The HA-2620 and HA-2622 are both offered as /883 Military Grade with the HA-2622 also available in CLCC packages. MIL-STD-883 data sheets are available upon request. Harris AnswerFAX (407-724-7800) Document #3701.

Pinouts

HA-2620/22 (CERDIP)
HA-2625 (CERDIP, PDIP, SOIC)
TOP VIEW



HA-2620, HA-2622, HA-2625
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2903.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 45V
Differential Input Voltage 12V
Peak Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-2620/HA-2622-2 . . . . . -55°C to 125°C
HA-2625-5 . . . . . 0°C to 75°C
HA-2625-9 . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	96	N/A
CERDIP Package	135	50
SOIC Package	157	N/A
Metal Can Package	165	80

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15V, Unless Otherwise Specified

PARAMETER	TEMP. (°C)	HA-2620-2			HA-2622-2			HA-2625-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 3)	25	-	0.5	4	-	3	5	-	3	5	mV
	Full	-	2	6	-	-	7	-	-	7	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	-	5	-	µV/°C
Bias Current	25	-	1	15	-	5	25	-	5	25	nA
	Full	-	10	35	-	-	60	-	-	40	nA
Offset Current	25		1	15	-	5	25	-	5	25	nA
	Full	-	5	35	-	-	60	-	-	40	nA
Differential Input Resistance (Note 2)	25	65	500	-	40	300	-	40	300	-	MΩ
Input Noise Voltage Density (f = 1kHz)	25	-	11	-	-	11	-	-	11	-	$nV/\sqrt{Hz}$
Input Noise Current Density (f = 1kHz)	25	-	0.16	-	-	0.16	-	-	0.16	-	$pA/\sqrt{Hz}$
Common Mode Range	Full	±11	±12	-	±11	±12	-	±11	±12	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 4, 5)	25	100	150	-	80	150	-	80	150	-	kV/V
	Full	70	-	-	60	-	-	70	-	-	kV/V
Common Mode Rejection Ratio (Note 6)	Full	80	100	-	74	100	-	74	100	-	dB
Minimum Stable Gain	25	5	-	-	5	-	-	5	-	-	V/V
Gain Bandwidth Product (Notes 4, 7, 8)	25	-	100	-	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 4)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 5)	25	±15	±22	-	±10	±18	-	±10	±18	-	mA
Full Power Bandwidth (Notes 4, 5, 9, 13)	25	400	600	-	320	600	-	320	600	-	kHz
TRANSIENT RESPONSE (Note 8)											
Rise Time (Notes 4, 9, 10)	25	-	17	45	-	17	45	-	17	45	ns

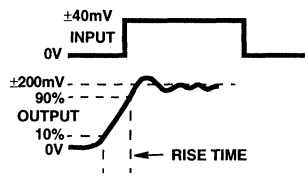
Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

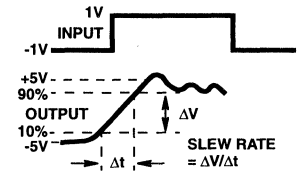
PARAMETER	TEMP. (°C)	HA-2620-2			HA-2622-2			HA-2625-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate (Notes 4, 9, 10, 12)	25	±25	±35	-	±20	±35	-	±20	±35	-	V/µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	25	-	3	3.7	-	3	4	-	3	4	mA
Power Supply Rejection Ratio (Note 11)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

2. This parameter value guaranteed by design calculations.
3. Offset may be externally adjusted to zero.
4. R_L = 2kΩ.
5. V_{OUT} = ±10V.
6. V_{CM} = ±10V.
7. V_{OUT} < 90mV.
8. 40dB Gain.
9. See Transient Response Test Circuits and Waveforms.
10. A_V = 5 (The HA-2620 family is not stable at unity gain without external compensation).
11. ΔV_S = ±5V.
12. V_{OUT} = ±5V.
13. Full Power Bandwidth guaranteed by slew rate measurement: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.

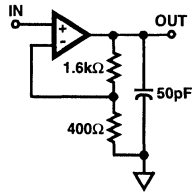
Test Circuits and Waveforms

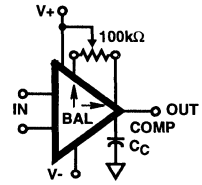




NOTE: Measured on both positive and negative transistions from 0V to +200mV and 0V to -200mV at output.

TRANSIENT RESPONSE **SLEW RATE**

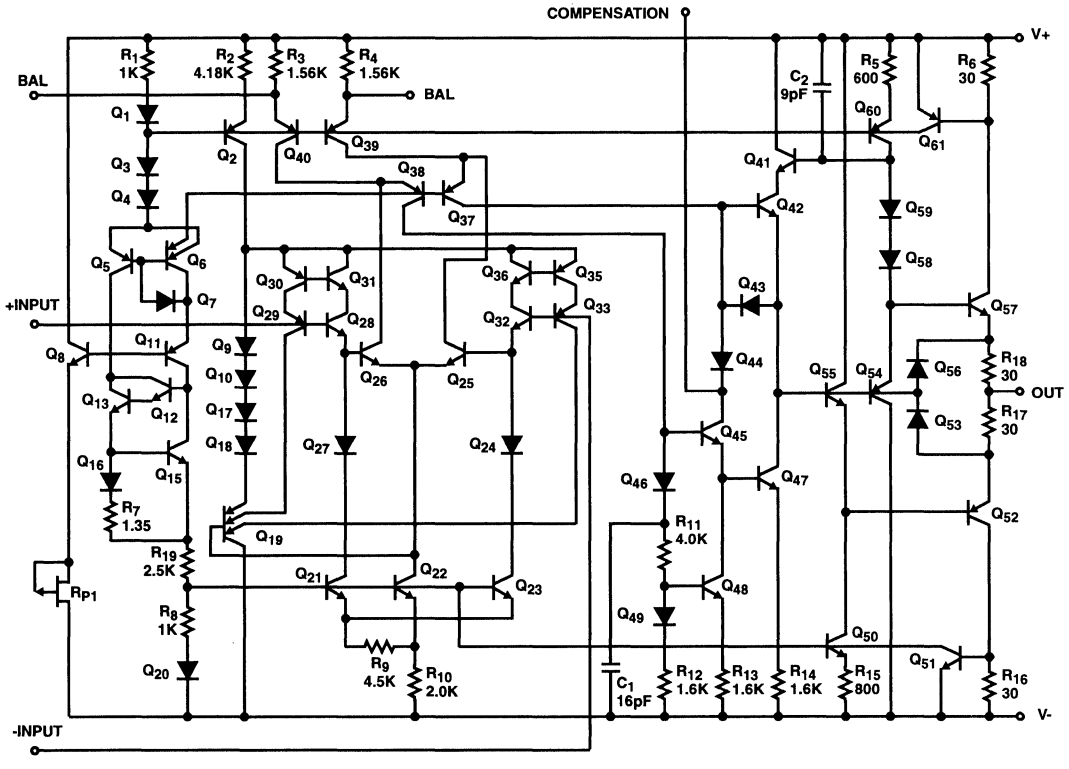




NOTE: Tested Offset Adjustment is $|V_{OS}|$ + 1mV| minimum referred to output. Typical range is ±10mV with R_T = 100kΩ.

SLEW RATE AND TRANSIENT RESPONSE **SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP**

Schematic Diagram



Typical Applications

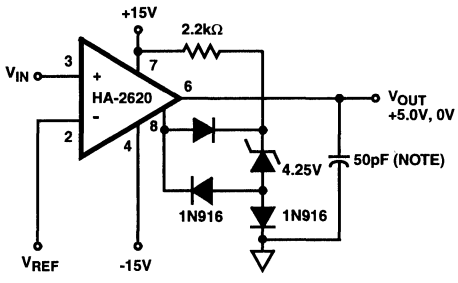


FIGURE 1. HIGH INPUT IMPEDANCE COMPARATOR

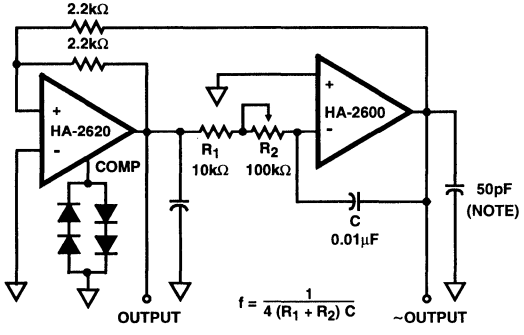
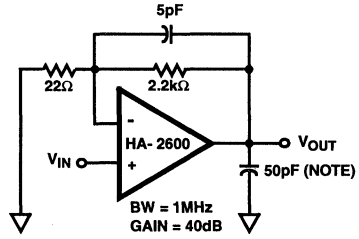


FIGURE 2. FUNCTION GENERATOR

Typical Applications (Continued)



NOTE: A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

FIGURE 3. VIDEO AMPLIFIER

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$, Unless Otherwise Specified

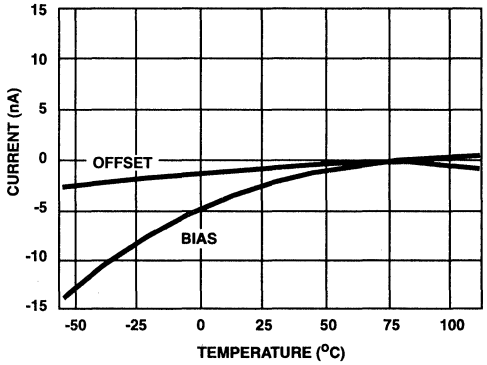


FIGURE 4. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

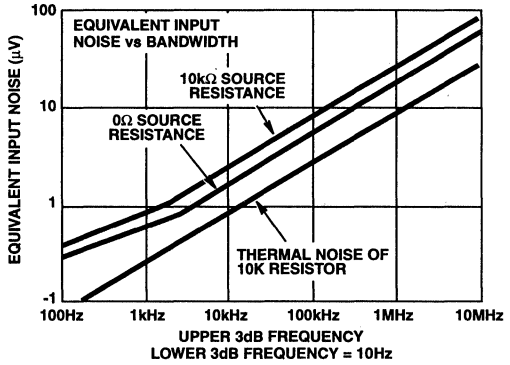


FIGURE 5. BROADBAND NOISE CHARACTERISTICS

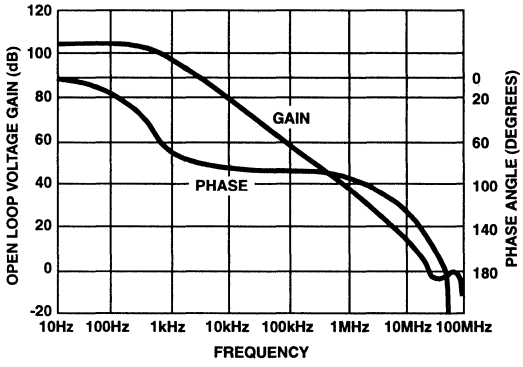


FIGURE 6. OPEN LOOP FREQUENCY RESPONSE

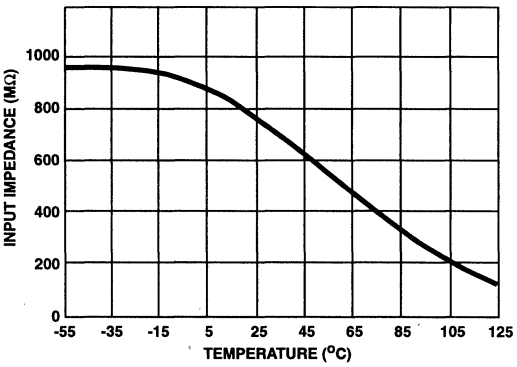


FIGURE 7. INPUT IMPEDANCE vs TEMPERATURE, 100Hz

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

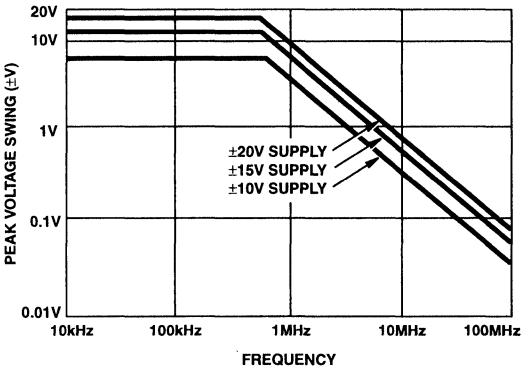
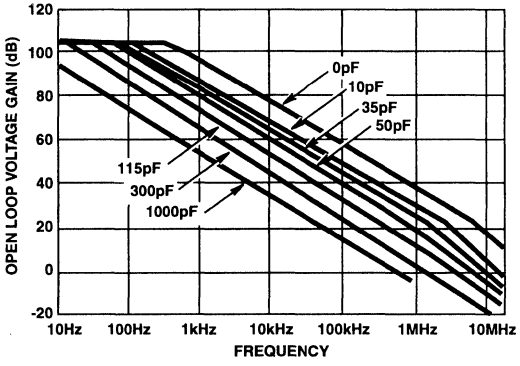


FIGURE 8. OUTPUT VOLTAGE SWING vs FREQUENCY



NOTE: External Compensation is required for closed loop gain < 5. If external compensation is used, also connect 100pF capacitor from output to ground.

FIGURE 9. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMP. PIN TO GND

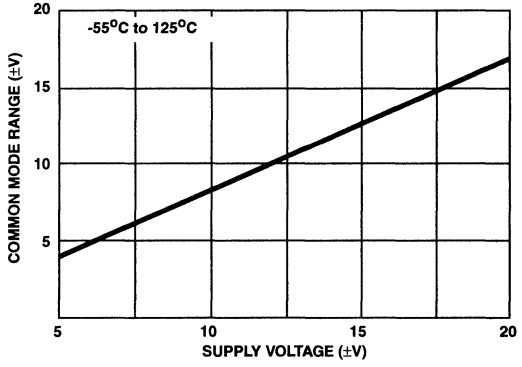


FIGURE 10. COMMON MODE VOLTAGE RANGE vs SUPPLY VOLTAGE

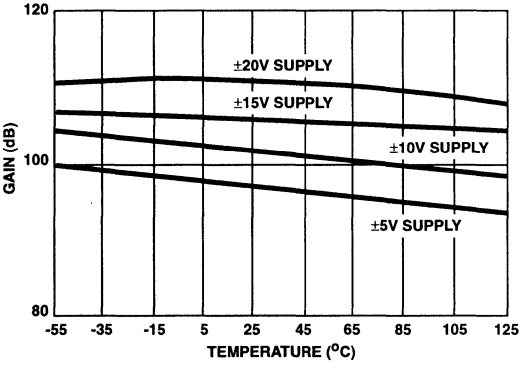


FIGURE 11. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

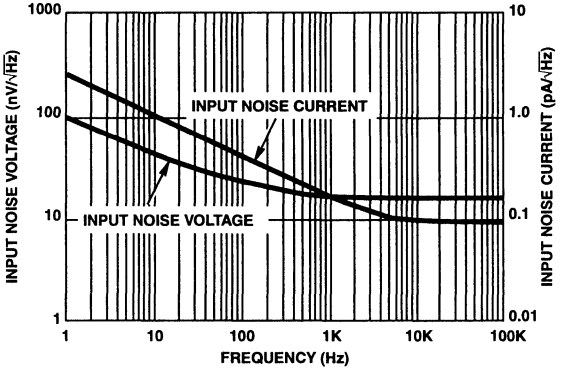


FIGURE 12. NOISE DENSITY vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

69 mils x 56 mils x 19 mils
1750µm x 1420µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up)

Unbiased

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

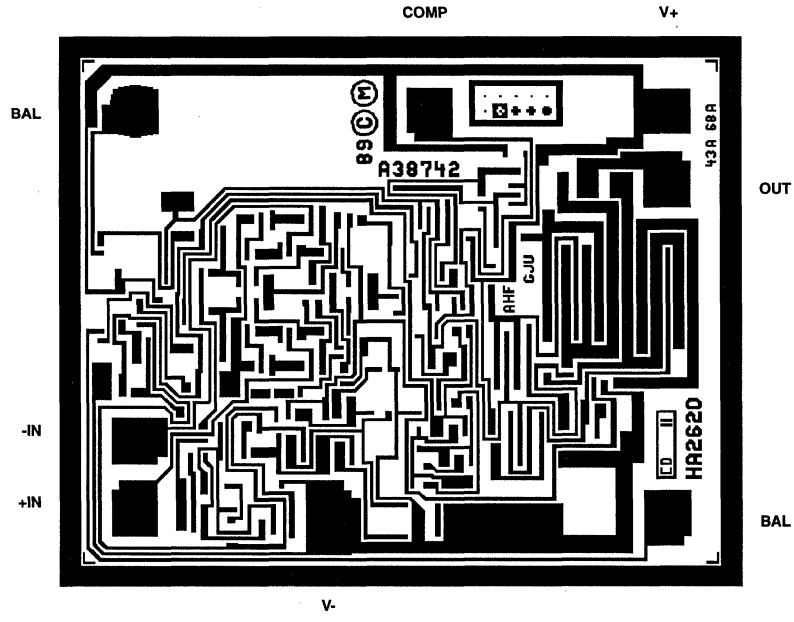
140

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2620, HA-2622, HA-2625



HA-2640, HA-2645

November 1996

4MHz, High Supply Voltage Operational Amplifiers

Features

- Output Voltage Swing ..... ±35V
- Supply Voltage ..... ±10V to ±40V
- Offset Current 5nA
- Bandwidth 4MHz
- Slew Rate 5V/µs
- Common Mode Input Voltage Range ..... ±35V
- Output Overload Protection

Applications

- Industrial Control Systems
- Power Supplies
- High Voltage Regulators
- Resolver Excitation
- Signal Conditioning

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2640-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2645-5	0 to 75	8 Pin Metal Can	T8.C
HA7-2640-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2645-5	0 to 75	8 Ld CERDIP	F8.3A

Description

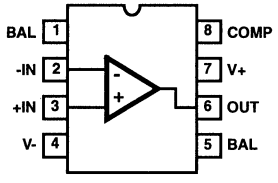
HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

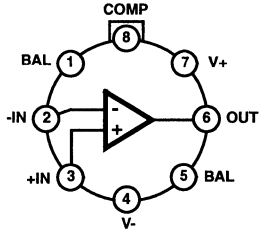
These amplifiers deliver ±35V common mode input voltage range, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/µs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excitation designs.

Pinouts

HA-2640/2645 (CERDIP)
TOP VIEW



HA-2640/2645 (METAL CAN)
TOP VIEW



(TO-99 CASE VOLTAGE = FLOATING)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 100V
Differential Input Voltage Range 37V
Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-2640-2 . . . . . -55°C to 125°C
HA-2645-5 . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	135	50
Metal Can Package	165	80

Maximum Junction Temperature . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

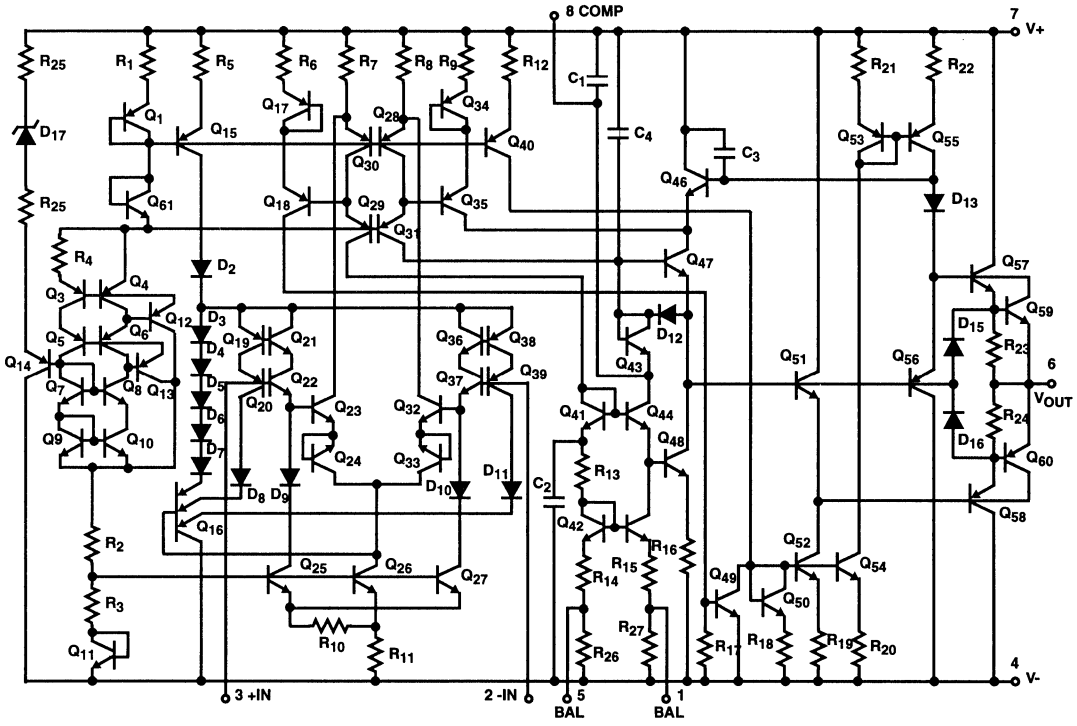
$V_{SUPPLY} = \pm 40V$, $R_L = 5k\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2640-2 -55°C TO 125°C			HA-2645-5 0°C TO 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	2	4	-	2	6	mV
		Full		-	6	-	-	7	mV
Average Offset Voltage Drift		Full	-	15	-	-y	15	-	µV/°C
Bias Current		25	-	10	25	-	12	30	nA
		Full	-	-	50	-	-	50	nA
Offset Current		25	-	5	12	-	15	30	nA
		Full	-	-	35	-	-	50	nA
Input Resistance (Note 2)		25	50	250	-	40	200	-	MΩ
Common Mode Range		Full	±35	-	-	±35	-	-	V
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$V_{OUT} = \pm 30V$	25	100	200	-	100	200	-	kV/V
		Full	75	-	-	75	-	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm 20V$	Full	80	100	-	74	100	-	dB
Minimum Stable Gain		25	1	-	-	1	-	-	V/V
Unity Gain Bandwidth	$V_{OUT} = 90mV$	25	-	4	-	-	4	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing		Full	±35	-	-	±35	-	-	V
Output Current	$R_L = 1k\Omega$	25	±12	±15	-	±10	±12	-	mA
Output Resistance	Open Loop	25	-	500	-	-	500	-	Ω
Full Power Bandwidth (Note 3)	$V_{OUT} = \pm 35V$	25	-	23	-	-	23	-	kHz
TRANSIENT RESPONSE $A_V = +1$, $C_L = 50pF$, $R_L = 5k\Omega$									
Rise Time	$V_{OUT} = \pm 200mV$	25	-	60	135	-	60	135	ns
Overshoot	$V_{OUT} = \pm 200mV$	25	-	15	30		15	40	%
Slew Rate		25	±3	±5	-	±2.5	±5	-	V/µs
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	3.2	3.8	-	3.2	4.5	mA
Supply Voltage Range		Full	±10	-	±40	±10	-	±40	V
Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 40V$	Full	80	90	-	74	90	-	dB

NOTES:

2. This parameter is based upon design calculations.
3. Full Power Bandwidth guaranteed based upon slew rate measurement: $FPBW = S.R./2\pi V_{PEAK}$; $V_{PEAK} = 35V$.

Schematic Diagram



Test Circuits and Waveform

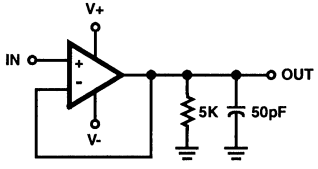
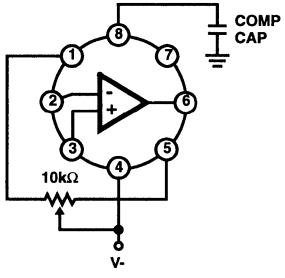


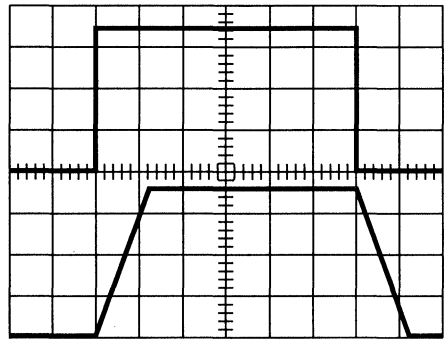
FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



NOTE: Tested offset adjustment range is $|V_{OS}|$ +1mV| minimum referred to output. Typical range is ±20mV with R_T = 10kΩ.

FIGURE 2. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Test Circuits and Waveform (Continued)



Vertical = 10V/Div., Horizontal = 5µs/Div.

NOTE: $R_L = 5k\Omega$, $C_L = 50pF$, $T_A = 25^oC$, $V_S = \pm 40V$

FIGURE 3. VOLTAGE FOLLOWER PULSE RESPONSE

Typical Performance Curves $V_S = \pm 40V$, $T_A = 25^oC$, Unless Otherwise Specified

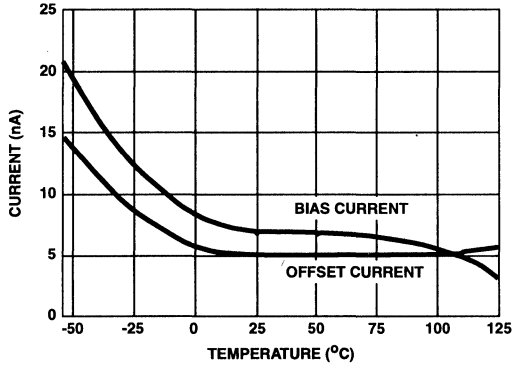


FIGURE 4. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

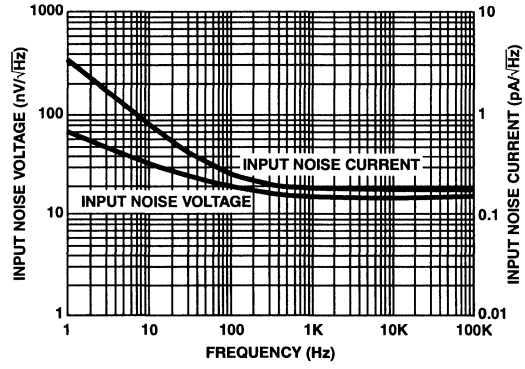


FIGURE 5. INPUT NOISE CHARACTERISTICS

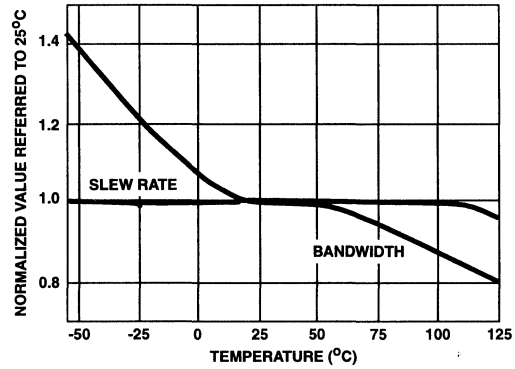


FIGURE 6. NORMALIZED AC PARAMETERS vs TEMPERATURE

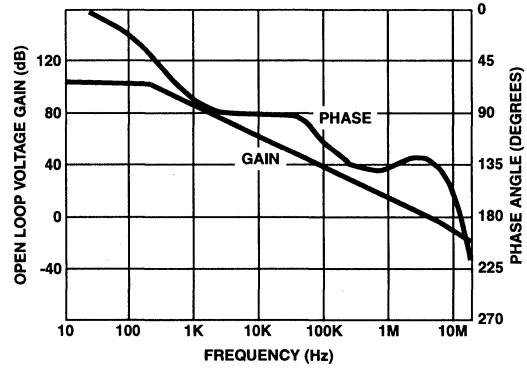


FIGURE 7. OPEN LOOP FREQUENCY RESPONSE

Typical Performance Curves $V_S = \pm 40V$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

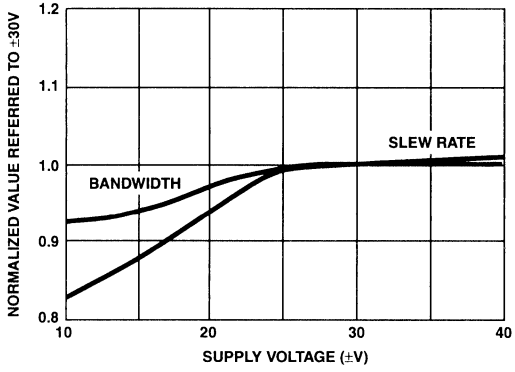


FIGURE 8. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT 25°C

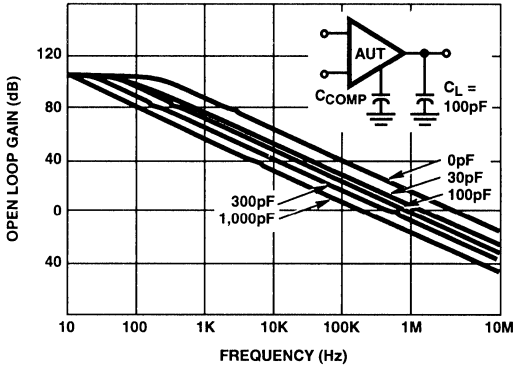


FIGURE 9. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

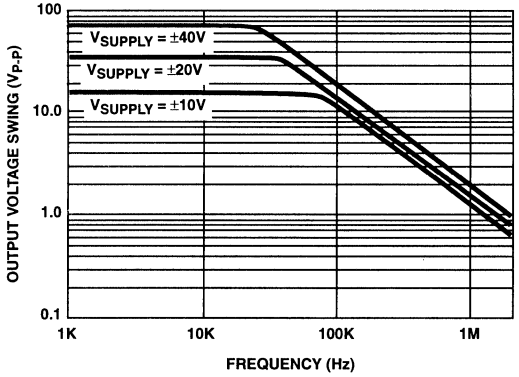


FIGURE 10. OUTPUT VOLTAGE SWING vs FREQUENCY

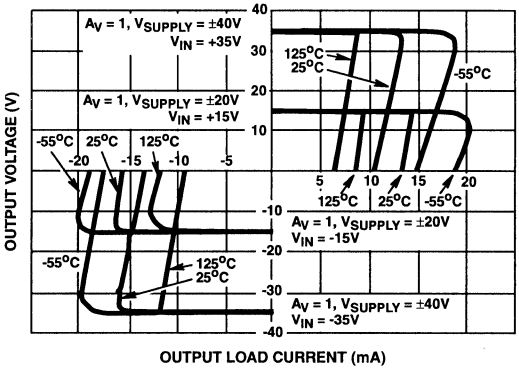


FIGURE 11. OUTPUT CURRENT CHARACTERISTIC

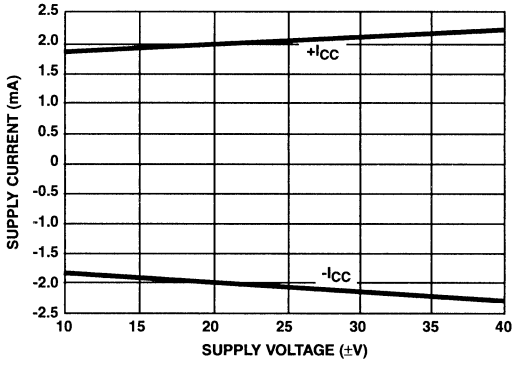


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

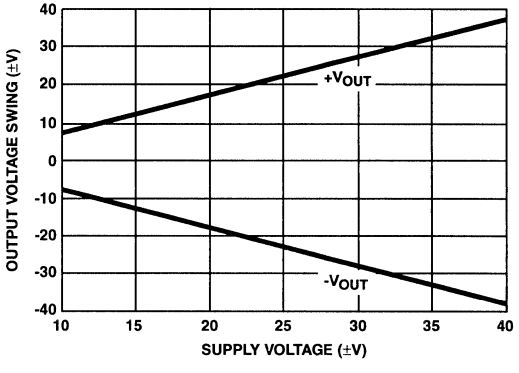


FIGURE 13. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

93 mils x 68 mils x 19 mils
2360µm x 1720µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

TRANSISTOR COUNT:

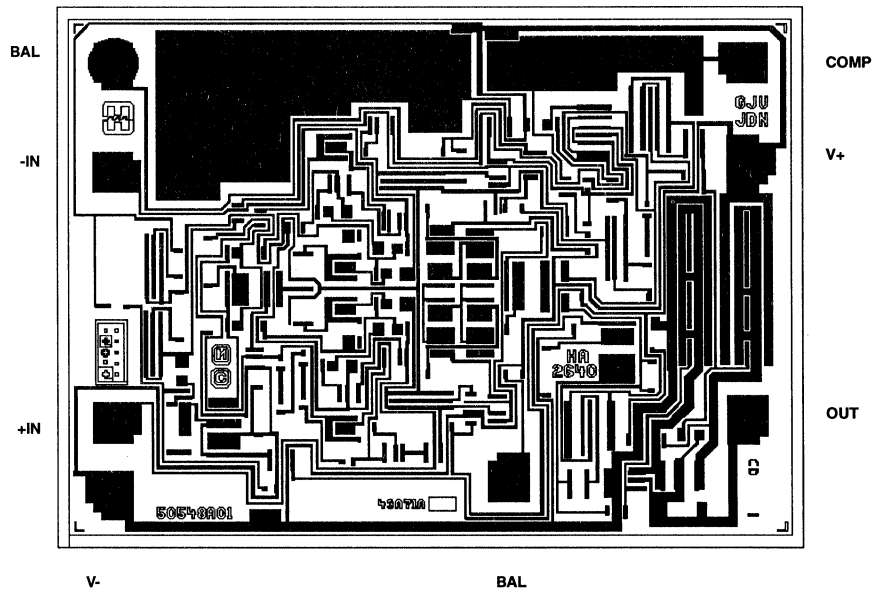
76

PROCESS:

HV200 Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2640, HA-2645



Complete data sheet available via web, Harris' home page: http://www.semi.harris.com/ or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

HA-2839

600MHz, Very High Slew Rate Operational Amplifier

November 1996

Features

- Low Supply Current 13mA
- Very High Slew Rate 625V/µs
- Open Loop Gain 25kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Full Power Bandwidth 10MHz
- Low Offset Voltage 0.6mV
- Differential Gain/Phase . . . . . 0.03%/0.03 Degrees
- Enhanced Replacement for EL2039

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Description

The HA-2839 is a wideband, very high slew rate, operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction, coupled with dielectric isolation, delivers outstanding performance in circuits with a closed loop gain of 10 or greater.

A 625V/µs slew rate and a 600MHz gain bandwidth product ensure high performance in video and RF amplifier designs. Differential gain and phase are a low 0.03% and 0.03 degrees respectively, making the HA-2839 ideal for video applications. A full ±10V output swing, high open loop gain, and outstanding AC parameters, make the HA-2839 an excellent choice for high speed Data Acquisition Systems.

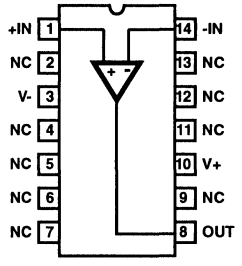
The HA-2839 is available in commercial and industrial temperature ranges, and a choice of packages. For military grade product, refer to the HA-2839/883 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-2839-5	0 to 75	14 Ld CERDIP	F14.3
HA3-2839-5	0 to 75	14 Ld PDIP	E14.3
HA3-2839-9	-40 to 85	14 Ld PDIP	E14.3

Pinout

HA-2839
(CERDIP, PDIP)
TOP VIEW



NOTE: No Connection (NC) pins may be tied to a ground plane for better isolation and heat dissipation.

3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 2841.2

HARRIS SEMICONDUCTOR

HA-2840

600MHz, Very High Slew Rate Operational Amplifier

November 1996

Features

- Low Supply Current 13mA
- Very High Slew Rate 625V/μs
- Open Loop Gain 25kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Full Power Bandwidth 10MHz
- Low Offset Voltage 0.6mV
- Differential Gain/Phase . . . . . 0.03%/0.03 Degrees
- Enhanced Replacement for EL2039

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Description

The HA-2840 is a wideband, very high slew rate, operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction, coupled with dielectric isolation, delivers outstanding performance in circuits with a closed loop gain of 10 or greater.

A 625V/μs slew rate and a 600MHz gain bandwidth product ensure high performance in video and RF amplifier designs. Differential gain and phase are a low 0.03% and 0.03 degrees respectively, making the HA-2840 ideal for video applications. A full ±10V output swing, high open loop gain, and outstanding AC parameters, make the HA-2840 an excellent choice for high speed Data Acquisition Systems.

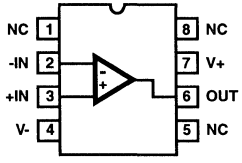
The HA-2840 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" below for more information. For military grade product, refer to the HA-2840/883 data sheet.

Ordering Information

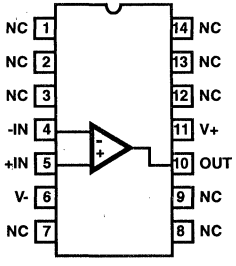
PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA3B2840-5	0 to 75	14 Ld PDIP	E14.3
HA3-2840-5	0 to 75	8 Ld PDIP	E8.3
HA9P2840-5 (H28405)	0 to 75	8 Ld SOIC	M8.15
HA3B2840-9	-40 to 85	14 Ld PDIP	E14.3
HA7-2840-9	-40 to 85	8 Ld CERDIP	F8.3A
HA3-2840-9	-40 to 85	8 Ld PDIP	E8.3

Pinouts

HA-2840
(CERDIP, PDIP, SOIC)
TOP VIEW



HA-2840
(PDIP)
TOP VIEW



NOTE: No Connection (NC) pins may be tied to a ground plane for better isolation and heat dissipation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **2842.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage. 6V
Output Current 50mA

Operating Conditions

Temperature Range
HA-2840-5. . . . . $0^{o}C$ to $75^{o}C$
HA-2840-9. . . . . $-40^{o}C$ to $85^{o}C$
Recommended Supply Voltage Range. . . . . ±7V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
14 Lead PDIP Package	80	N/A
8 Lead CERDIP Package	135	50
8 Lead PDIP Package	96	N/A
8 Lead SOIC Package	157	N/A

Maximum Internal Quiescent Power Dissipation (Note 1)
Maximum Junction Temperature (Ceramic Package) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below $175^{o}C$ for ceramic packages and below $150^{o}C$ for plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, $C_L \leq$ 10pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	HA-2840-5, -9			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Offset Voltage (Note 8)		25	-	0.6	2	mV
		Full	-	2	6	mV
Average Offset Voltage Drift		Full	-	20	-	µV/^{o}C
Bias Current (Note 8)		25	-	5	14.5	µA
		Full	-	8	20	µA
Offset Current		25	-	1	4	µA
		Full	-	-	8	µA
Input Resistance		25	-	10	-	kΩ
Input Capacitance		25	-	1	-	pF
Common Mode Range		Full	±10	-	-	V
Input Noise Voltage (Note 8)	f = 1kHz, R_{SOURCE} = 0Ω	25	-	6	-	nV/$\sqrt{Hz}$
Input Noise Current (Note 8)	f = 1kHz, R_{SOURCE} = 10kΩ	25	-	6	-	pA/$\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	Note 3	25	20	25	-	kV/V
		Full	15	20	-	kV/V
Common-Mode Rejection Ratio (Note 8)	V_{CM} = ±10V	Full	75	80	-	dB
Minimum Stable Gain		25	10	-	-	V/V
Gain Bandwidth Product (Note 8)	V_O = 90mV, A_V = +100	25	-	600	-	MHz
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 8)	Note 3	Full	±10	-	-	V
Output Current (Note 8)	Note 3	Full	±10	±20	-	mA
Output Resistance		25	-	30	-	Ω
Full Power Bandwidth (Note 4)	Note 3	25	8.7	10	-	MHz
Differential Gain (Note 7)	A_V = 10	25	-	0.03	-	%

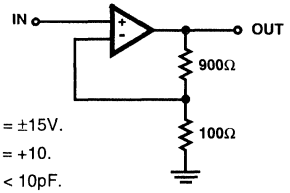
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2840-5, -9			UNITS
			MIN	TYP	MAX	
Differential Phase (Note 7)	$A_V = 10$	25	-	0.03	-	Degrees
Harmonic Distortion (Note 8)	$A_V = 10$, $V_O = 2V_{P-P}$, f = 1MHz	25	-	-79	-	dBc
TRANSIENT RESPONSE (Note 5)						
Rise Time		25	-	4	-	ns
Overshoot		25	-	20	-	%
Slew Rate (Notes 6, 8)	Note 3	25	550	625	-	V/µs
Settling Time	10V Step to 0.1%	25	-	180	-	ns
POWER REQUIREMENTS						
Supply Current (Note 8)		Full	-	13	15	mA
Power Supply Rejection Ratio (Note 8)	$V_S = \pm10V$ to $\pm20V$	Full	75	90	-	dB

NOTES:

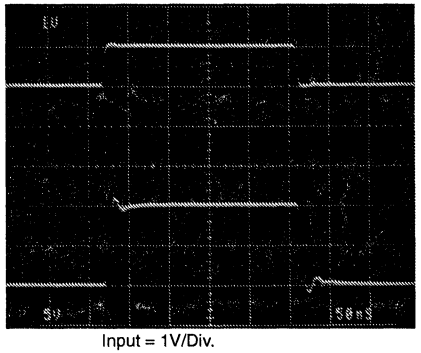
3. $R_L = 1k\Omega$, $V_O = \pm10V$, 0V to $\pm10V$ for slew rate.
4. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; ($V_{PEAK} = 10V$).
5. Refer to Test Circuit section of data sheet.
6. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
7. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS.
8. See "Typical Performance Curves" for more information.

Test Circuits and Waveforms



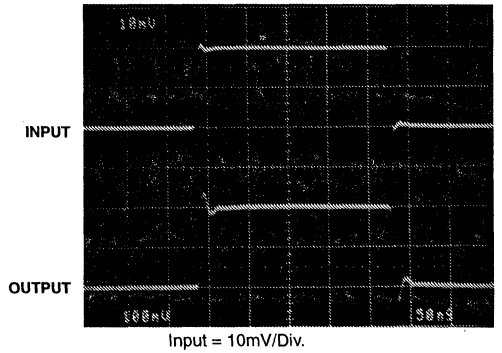
9. $V_S = \pm15V$.
10. $A_V = +10$.
11. $C_L < 10pF$.

TEST CIRCUIT



Input = 1V/Div.
Output = 5V/Div.
50ns/Div.

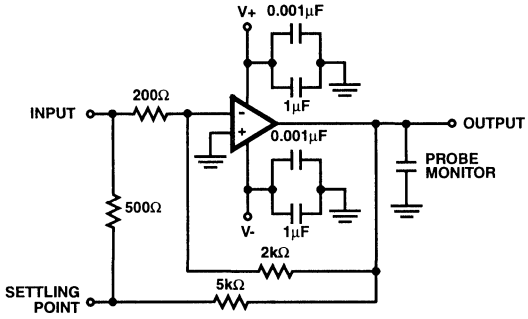
LARGE SIGNAL RESPONSE



Input = 10mV/Div.
Output = 100mV/Div.
50ns/Div.

SMALL SIGNAL RESPONSE

Test Circuits and Waveforms (Continued)



SETTLING TIME TEST CIRCUIT

NOTES:

12. A_V = -10.
13. Load Capacitance should be less than 10pF.
14. It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
15. SETTLING POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

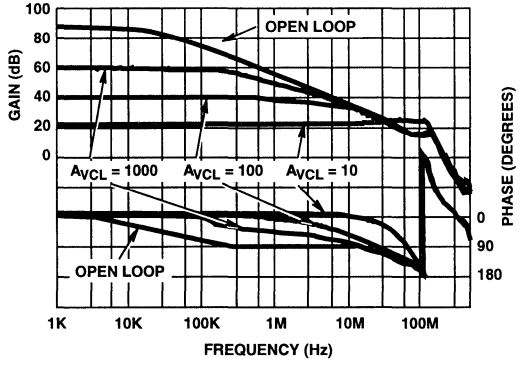


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS GAINS

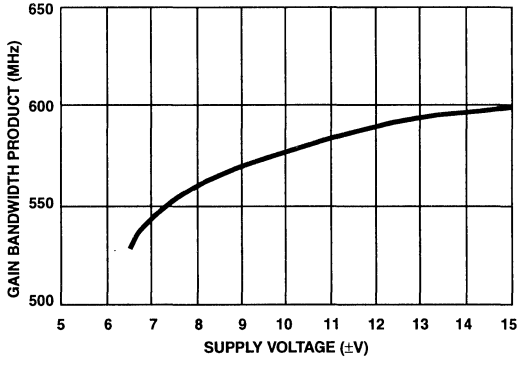


FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

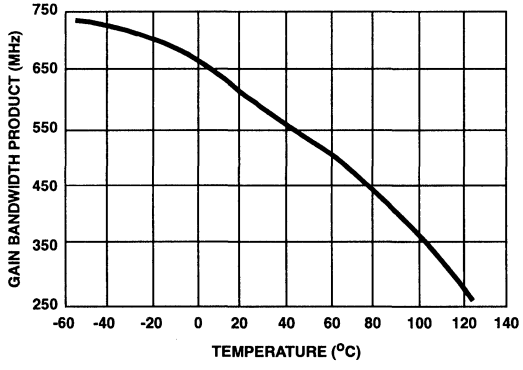


FIGURE 3. GAIN BANDWIDTH PRODUCT vs TEMPERATURE

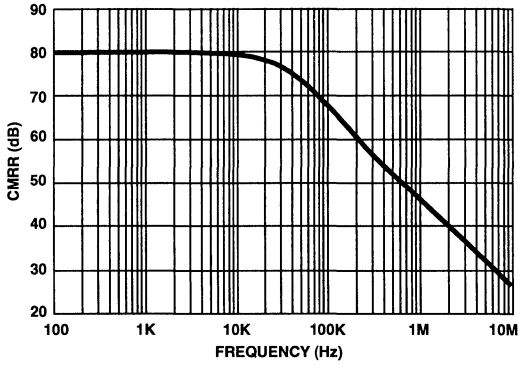


FIGURE 4. CMRR vs FREQUENCY

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

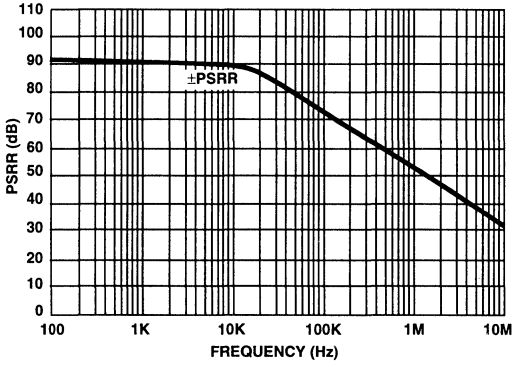


FIGURE 5. PSRR vs FREQUENCY

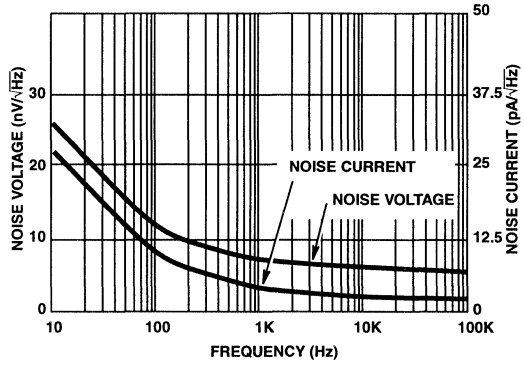


FIGURE 6. INPUT NOISE vs FREQUENCY

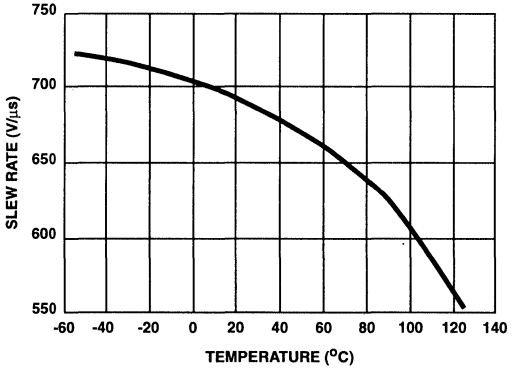


FIGURE 7. SLEW RATE vs TEMPERATURE

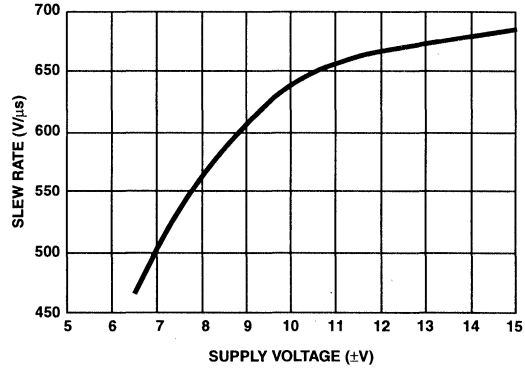


FIGURE 8. SLEW RATE vs SUPPLY VOLTAGE

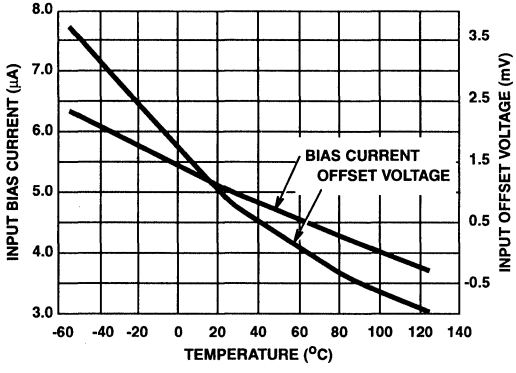


FIGURE 9. INPUT OFFSET VOLTAGE AND INPUT BIAS CURRENT vs TEMPERATURE

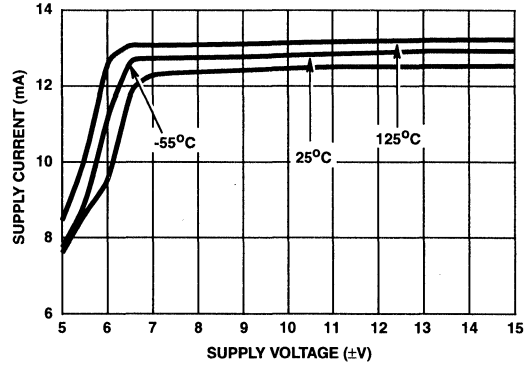


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

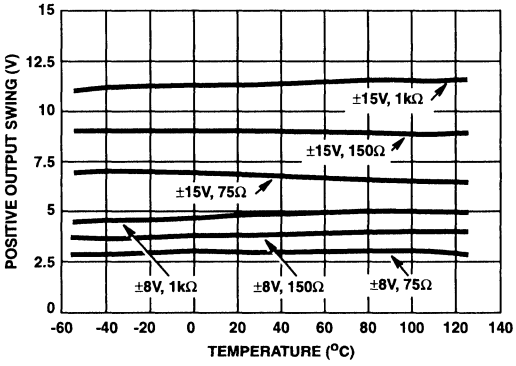


FIGURE 11. POSITIVE OUTPUT SWING vs TEMPERATURE

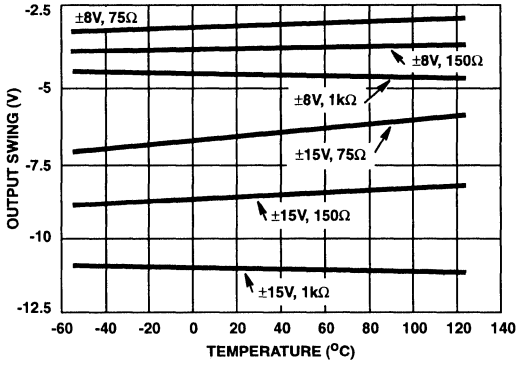


FIGURE 12. NEGATIVE OUTPUT SWING vs TEMPERATURE

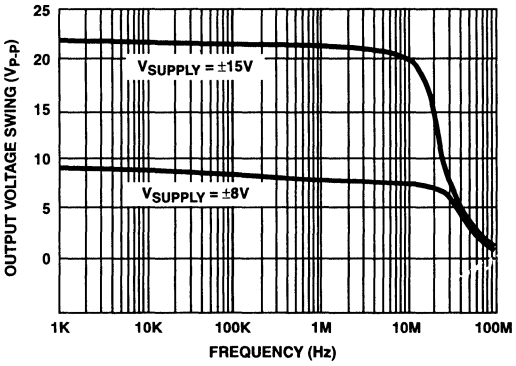


FIGURE 13. MAXIMUM UNDISTORTED OUTPUT SWING vs FREQUENCY

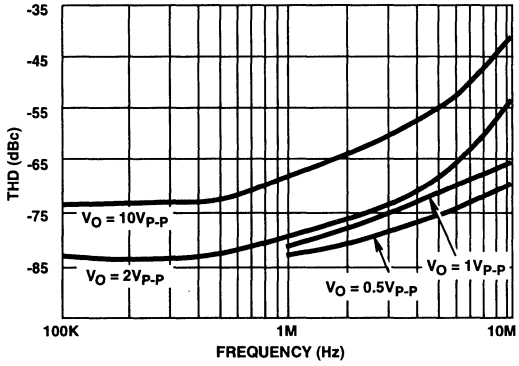


FIGURE 14. TOTAL HARMONIC DISTORTION vs FREQUENCY

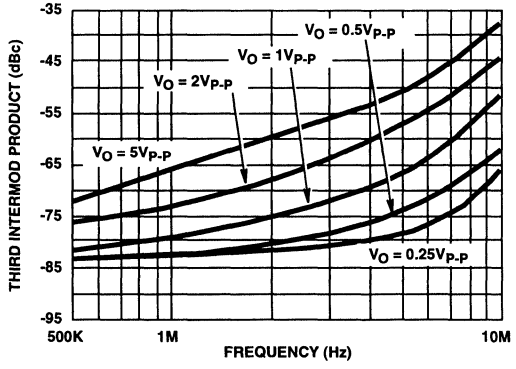


FIGURE 15. INTERMODULATION DISTORTION vs FREQUENCY (TWO TONE)

Die Characteristics

DIE DIMENSIONS:

65 mils x 52 mils x 19 mils
1650µm x 1310µm x 483µm

METALLIZATION:

Type: Aluminum, 1% Copper
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride thickness: 3.5kÅ ±1kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

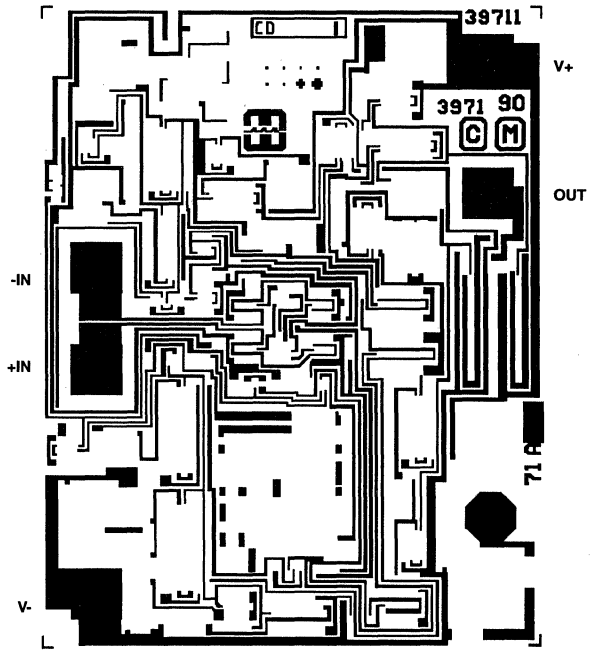
34

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2840



HARRIS SEMICONDUCTOR

HA-2841

50MHz, Fast Settling, Unity Gain Stable, Video Operational Amplifier

November 1996

Features

- Low Supply Current 10mA
- Low AC Variability Over Process and Temperature
- Unity Gain Bandwidth 50MHz
- Gain Flatness to 10MHz. 0.05dB
- High Slew Rate. 240V/ms
- Low Offset Voltage. 1mV
- Fast Settling Time (0.1%) 90ns
- Differential Gain/Phase . . . . . 0.03%/0.03 Degrees
- Enhanced Replacement for AD841 and EL2041

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HA3B2841-5	0 to 75	14 Ld PDIP	E14.3
HA3-2841-5	0 to 75	8 Ld PDIP	E8.3
HA9P2841-5 (H28415)	0 to 75	8 Ld SOIC	M8.15
HA3B2841-9	-40 to 85	14 Ld PDIP	E14.3
HA3-2841-9 (H28415)	-40 to 85	8 Ld PDIP	E8.3

Description

The HA-2841 is a wideband, unity gain stable, operational amplifier featuring a 50MHz unity gain bandwidth, and excellent DC specifications. This amplifier's performance is further enhanced through stable operation down to closed loop gains of +1, the inclusion of offset null controls, and by its excellent video performance.

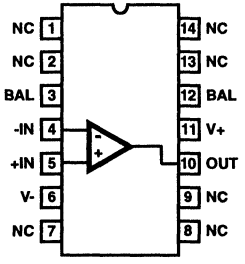
The capabilities of the HA-2841 are ideally suited for high speed pulse and video amplifier circuits, where high slew rates and wide bandwidth are required. Gain flatness of 0.05dB, combined with differential gain and phase specifications of 0.03%, and 0.03 degrees, respectively, make the HA-2841 ideal for component and composite video applications.

A zener/nichrome based reference circuit, coupled with advanced laser trimming techniques, yields a supply current with a low temperature coefficient and low lot-to-lot variability. Tighter I_{CC} control translates to more consistent AC parameters ensuring that units from each lot perform the same way, and easing the task of designing systems for wide temperature ranges. Critical AC parameters, Slew Rate and Bandwidth, each vary by less than ±5% over the industrial temperature range (see characteristic curves).

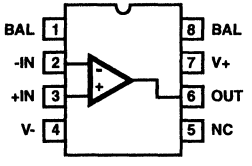
For military grade product, refer to the HA-2841/883 data sheet. Harris AnswerFAX (407 724-7800), document number 3621.

Pinouts

HA-2841
(PDIP)
TOP VIEW



HA-2841
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2843.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage. 6V
Output Current (Note 3) 50mA
10mA (50% Duty Cycle)

Operating Conditions

Temperature Range
HA-2841-5. . . . . $0^{o}C$ to $75^{o}C$
HA-2841-9. . . . . $-40^{o}C$ to $85^{o}C$
Recommended Supply Voltage Range. . . . . ±6.5V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
14 Lead PDIP Package	89
8 Lead PDIP Package	92
8 Lead SOIC Package	157

Maximum Junction Temperature (Die, Note 1). . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s). . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below $150^{o}C$ for plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. $V_O = \pm10V$, R_L unconnected. Output duty cycle must be reduced if $I_{OUT} > 10mA$.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	HA-2841-5, -9			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Offset Voltage (Note 10)		25	-	1	3	mV
		Full	-	-	6	mV
Average Offset Voltage Drift		Full	-	14	-	$\mu V/^{o}C$
Bias Current (Note 10)		25	-	5	10	µA
		Full	-	8	15	µA
Average Bias Current Drift		Full	-	45	-	$nA/^{o}C$
Offset Current		25	-	0.5	1.0	µA
		Full	-	-	1.5	µA
Input Resistance		25	-	170	-	kΩ
Input Capacitance		25	-	1	-	pF
Common Mode Range		Full	±10	-	-	V
Input Noise Voltage	10Hz to 1MHz	25	-	16	-	μV_{RMS}
Input Noise Voltage (Note 10)	f = 1kHz, $R_{SOURCE} = 0\Omega$	25	-	16	-	$nV/\sqrt{Hz}$
Input Noise Current (Note 10)	f = 1kHz, $R_{SOURCE} = 10k\Omega$	25	-	2	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	$V_O = \pm10V$	25	25	50	-	kV/V
		Full	10	30	-	kV/V
Common-Mode Rejection Ratio (Note 10)	$V_{CM} = \pm10V$	Full	80	95	-	dB
Minimum Stable Gain		25	1	-	-	V/V
Gain Bandwidth Product (Notes 5, 10)		25	-	50	-	MHz
Gain Flatness to 5MHz (Note 10)	$R_L \geq 75\Omega$	25	-	±0.015	-	dB
Gain Flatness to 10MHz (Note 10)	$R_L \geq 500\Omega$	25	-	±0.05	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 10)		Full	±10	±10.5	-	V
Output Current (Note 10)	Note 3	Full	15	30	-	mA
Output Resistance		25	-	8.5	-	Ω
Full Power Bandwidth (Note 6)	$V_O = \pm10V$	25	3.2	3.8	-	MHz

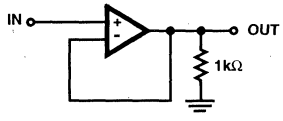
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-2841-5, -9			UNITS
			MIN	TYP	MAX	
Differential Gain (Note 10)	Note 4	25	-	0.03	-	%
Differential Phase (Note 10)	Note 4	25	-	0.03	-	Degrees
Harmonic Distortion (Note 10)	$V_O = 2V_{P-P}$, f = 1MHz, $A_V = +1$	25	-	>83	-	dBc
TRANSIENT RESPONSE (Note 7)						
Rise Time		25	-	3	-	ns
Overshoot		25	-	33	-	%
Slew Rate (Notes 9, 10)	$A_V = +1$	25	200	240	-	V/µs
Settling Time	10V Step to 0.1%	25	-	90	-	ns
POWER REQUIREMENTS						
Supply Current (Note 10)		25	-	10	-	mA
		Full	-	10	11	mA
Power Supply Rejection Ratio (Note 10)	Note 8	Full	70	80	-	dB

NOTES:

4. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS. $R_F = R_1 = 1k\Omega$, $R_L = 700\Omega$.
5. $A_{VCL} = 1000$, Measured at unity gain crossing.
6. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$ $(V_{PEAK} = 10V)$.
7. Refer to Test Circuit section of data sheet.
8. $V_{SUPPLY} = \pm10V$ to $\pm20V$.
9. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
10. See "Typical Performance Curves" for more information.

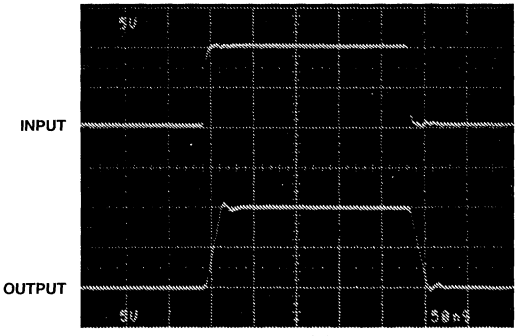
Test Circuits and Waveforms



NOTES:

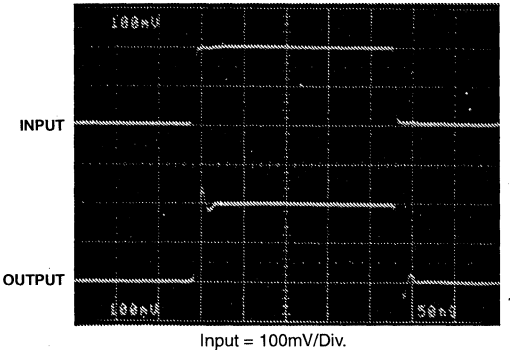
11. $V_S = \pm15V$.
12. $A_V = +1$.
13. $C_L < 10pF$.

TEST CIRCUIT



Input = 5V/Div.
Output = 5V/Div.
50ns/Div.

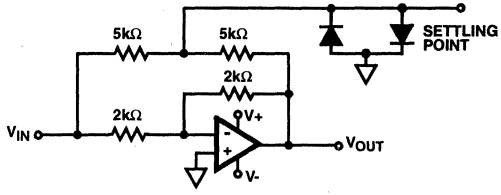
LARGE SIGNAL RESPONSE



Input = 100mV/Div.
Output = 100mV/Div.
50ns/Div.

SMALL SIGNAL RESPONSE

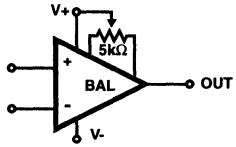
Test Circuits and Waveforms (Continued)



SETTLING TIME TEST CIRCUIT

NOTES:

14. $A_V = -1$.
15. Load Capacitance should be less than 10pF.
16. Feedback and summing resistors must be matched to 0.1%.
17. Tektronix P6201 FET probe used at settling point.
18. HP5082-2810 clipping diodes recommended.



SUGGESTED OFFSET VOLTAGE ADJUSTMENT

Typical Applications (Also see Application Note AN550)

Application 1 - High Power Amplifiers and Buffers

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2841, with its 15mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Figure 1.

The HA-2841 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50Ω coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6Ω and 6000pF capacitance.

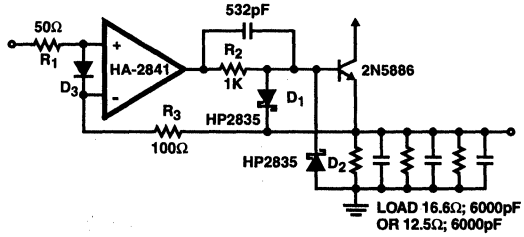


FIGURE 1. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

Application 2 - Video

One of the primary uses of the HA-2841 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2841 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores DC levels at the output of an amplifier stage. The circuit shown in Figure 2 utilizes the HA-5320 sample and hold amplifier as the DC clamp. Also shown is a 3.57MHz trap in series, which will block the color burst portion of the video signal and allow the DC level to be amplified and restored.

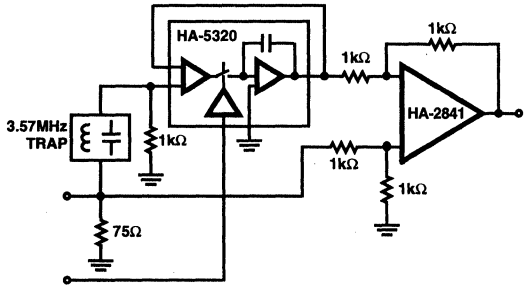


FIGURE 2. VIDEO DC RESTORER

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include:

1. Mounting the device through a ground plane.
2. Connecting unused pins (NC) to the ground plane.
3. Mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible.
4. Placing power supply decoupling capacitors from device supply pins to ground.

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

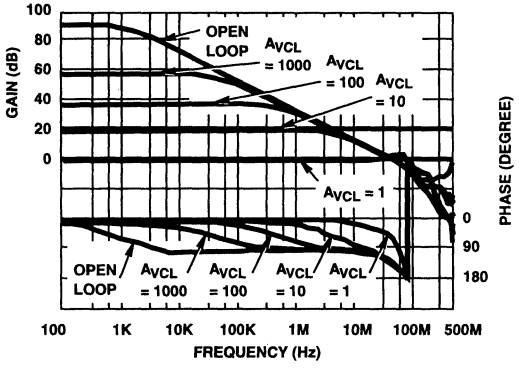


FIGURE 3. FREQUENCY RESPONSE FOR VARIOUS GAINS

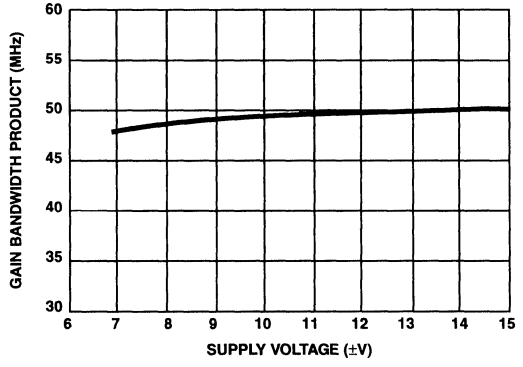


FIGURE 4. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

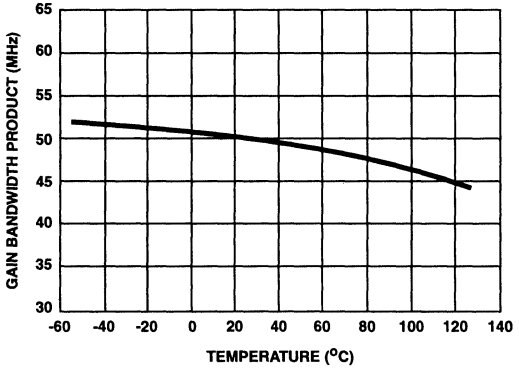


FIGURE 5. GAIN BANDWIDTH PRODUCT vs TEMPERATURE

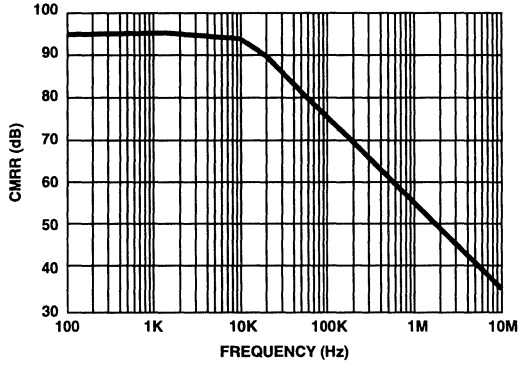


FIGURE 6. CMRR vs FREQUENCY

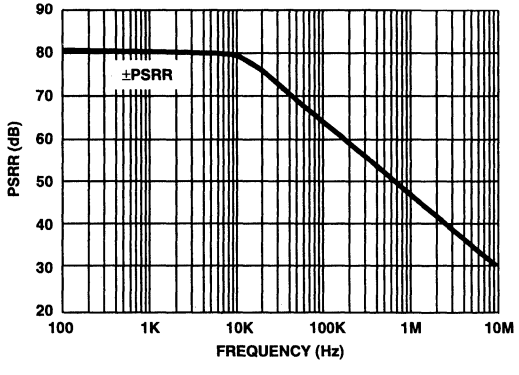


FIGURE 7. PSRR vs FREQUENCY

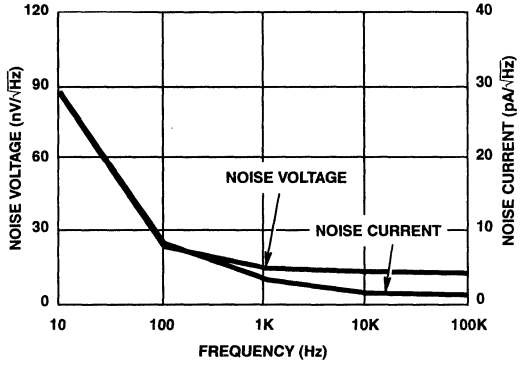


FIGURE 8. INPUT NOISE vs FREQUENCY

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

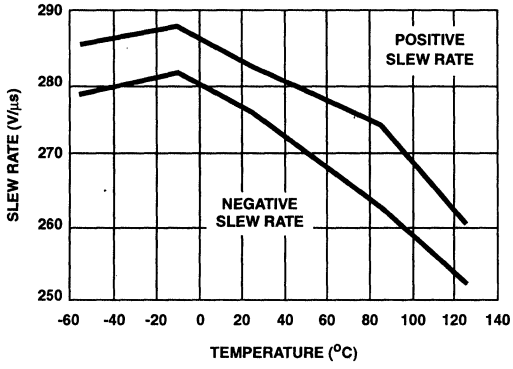


FIGURE 9. SLEW RATE vs TEMPERATURE

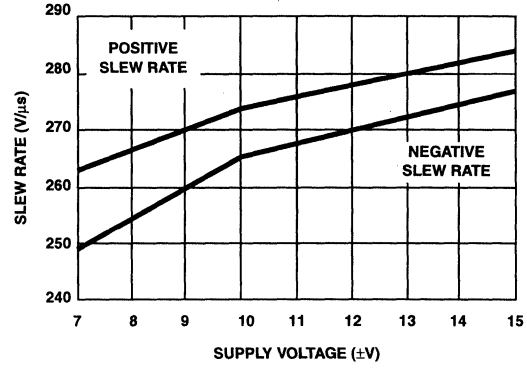


FIGURE 10. SLEW RATE vs SUPPLY VOLTAGE

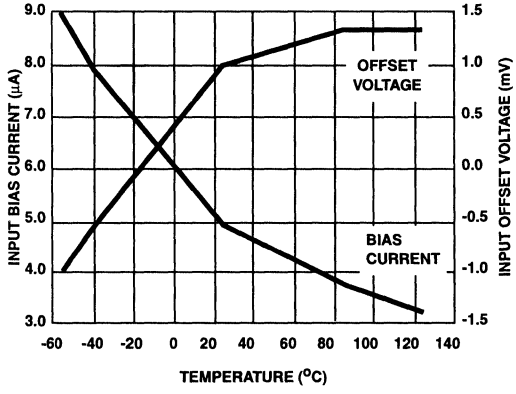


FIGURE 11. INPUT OFFSET VOLTAGE AND INPUT BIAS CURRENT vs TEMPERATURE

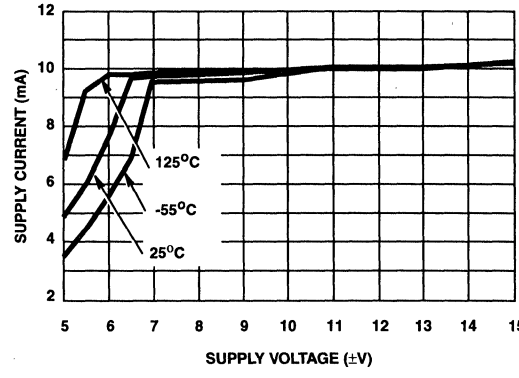


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

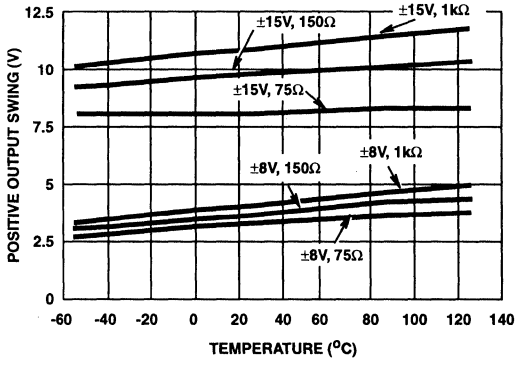


FIGURE 13. POSITIVE OUTPUT SWING vs TEMPERATURE

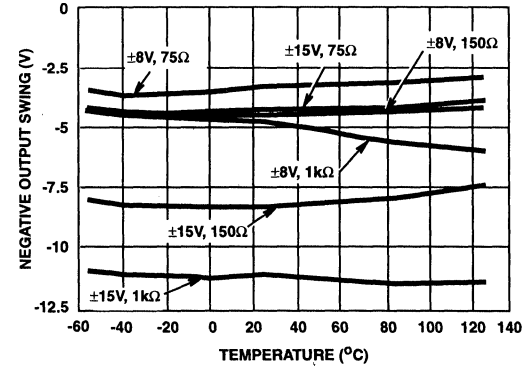


FIGURE 14. NEGATIVE OUTPUT SWING vs TEMPERATURE

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

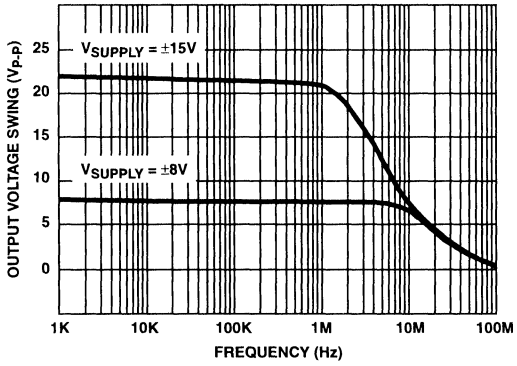


FIGURE 15. MAXIMUM UNDISTORTED OUTPUT SWING vs FREQUENCY

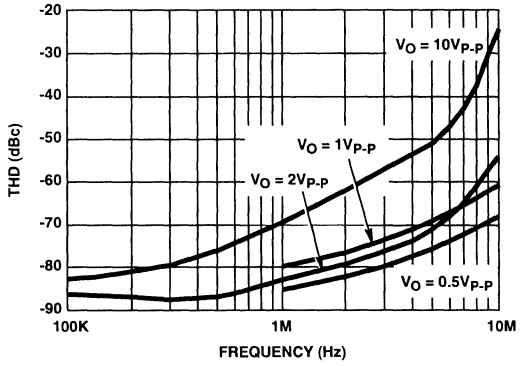


FIGURE 16. TOTAL HARMONIC DISTORTION vs FREQUENCY

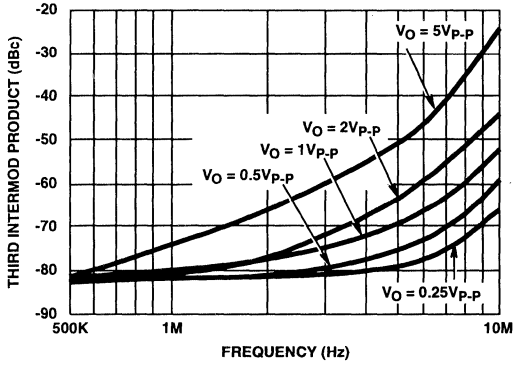


FIGURE 17. INTERMODULATION DISTORTION vs FREQUENCY (TWO TONE)

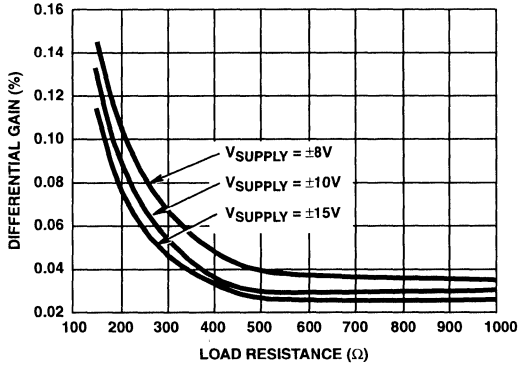


FIGURE 18. DIFFERENTIAL GAIN vs LOAD RESISTANCE

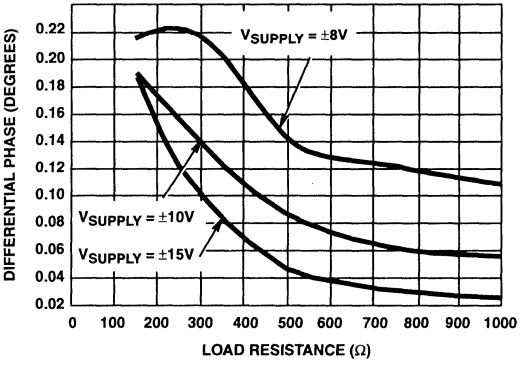


FIGURE 19. DIFFERENTIAL PHASE vs LOAD RESISTANCE

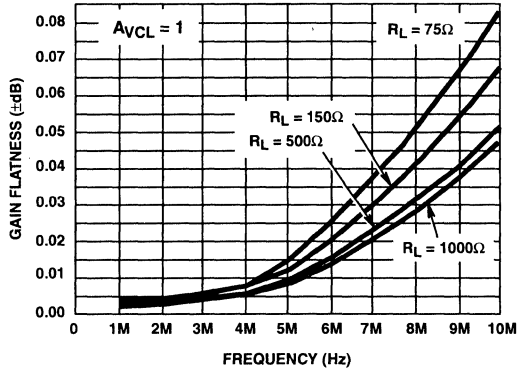


FIGURE 20. GAIN FLATNESS vs FREQUENCY

3 OPERATIONAL AMPLIFIERS

Die Characteristics

DIE DIMENSIONS:

77 mils x 81 mils x 19 mils
1960µm x 2060µm x 483µm

METALLIZATION:

Type: Aluminum, 1% Copper
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride thickness: 3.5kÅ ±1kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

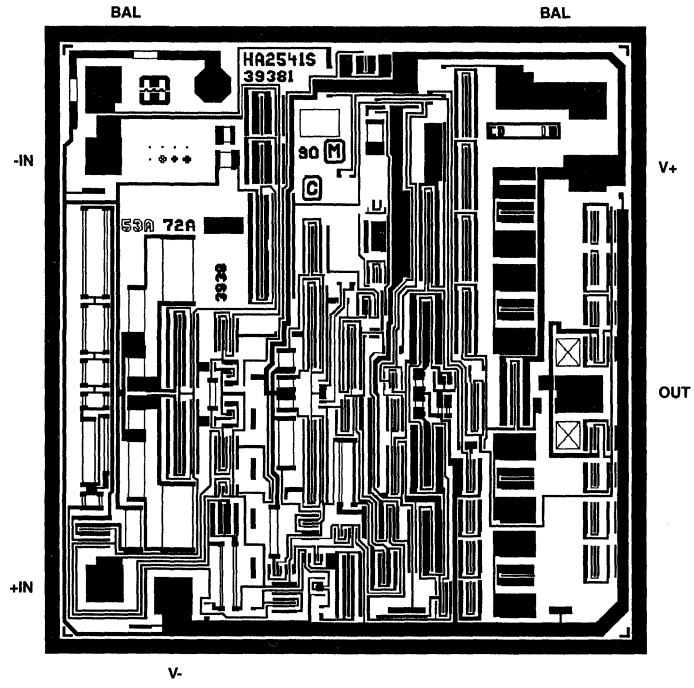
43

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2841



HARRIS SEMICONDUCTOR

HA-2842

80MHz, High Slew Rate, High Output Current, Video Operational Amplifier

November 1996

Features

- Stable at Gains of 2 or Greater
- Low AC Variability Over Process and Temperature
- Gain Bandwidth 80MHz
- Gain Flatness to 10MHz..... 0.035dB
- High Slew Rate..... 400V/µs
- High Output Current (Min)..... 100mA
- Differential Gain/Phase ..... 0.02%/0.03 Degrees
- Low Supply Current (Max) 15mA
- Enhanced Replacement for AD842

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HA3B2842-5	0 to 75	14 Ld PDIP	E14.3
HA3-2842-5	0 to 75	8 Ld PDIP	E8.3
HA9P2842-5 (H2842F5)	0 to 75	8 Ld SOIC	M8.15
HA3-2842C-5	0 to 75	8 Ld PDIP	E8.3
HA9P2842C-5 (H2842C5)	0 to 75	8 Ld SOIC	M8.15
HA3B2842-9	-40 to 85	14 Ld PDIP	E14.3
HA3-2842-9	-40 to 85	8 Ld PDIP	E8.3

Description

The HA-2842 is a wideband, high slew rate, operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability. This amplifier's performance is further enhanced through stable operation down to closed loop gains of +2, the inclusion of offset null controls, and by its excellent video performance.

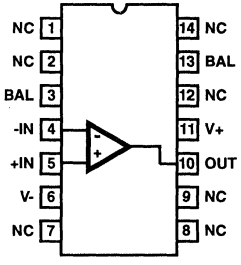
The capabilities of the HA-2842 are ideally suited for high speed cable driver circuits, where low closed loop gains and high output drive are required. With a 6MHz full power bandwidth, this amplifier is well suited for high frequency signal conditioning circuits and video amplifiers. Gain flatness of 0.035dB, combined with differential gain and phase specifications of 0.02%, and 0.03 degrees, respectively, make the HA-2842 ideal for component and composite video applications.

A zener/nichrome based reference circuit, coupled with advanced laser trimming techniques, yields a supply current with a low temperature coefficient and low lot-to-lot variability. For example, the average I_{CC} variation from 85^{o}C to -40^{o}C is <600µA (±2%), while the standard deviation of the I_{CC} distribution is <0.1mA (0.8%) at 25^{o}C. Tighter I_{CC} control translates to more consistent AC parameters ensuring that units from each lot perform the same way, and easing the task of designing systems for wide temperature ranges. Critical AC parameters, Slew Rate and Bandwidth, each vary by less than ±5% over the industrial temperature range (see Typical Performance Curves).

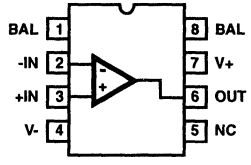
The HA-2842C is the same amplifier with a compensation pin available to the user. By connecting a capacitor from pin 8 to GND, the HA-2842C can be compensated for unity gain operation, or the bandwidth can be limited to reduce total noise.

Pinouts

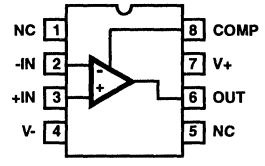
HA-2842 (PDIP) TOP VIEW



HA-2842 (PDIP, SOIC) TOP VIEW



HA-2842C (PDIP, SOIC) TOP VIEW



NOTE: No Connection (NC) pins may be tied to a ground plane for better isolation and heat dissipation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **2766.4**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage. 6V
Output Current (Notes 3, 4) 125mA
100mA (50% Duty Cycle)

Operating Conditions

Temperature Range
HA-2842-5. . . . . $0^{o}C$ to $75^{o}C$
HA-2842-9. . . . . $-40^{o}C$ to $85^{o}C$
Recommended Supply Voltage Range. . . . . ±6.5V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
14 Lead PDIP Package	89
8 Lead PDIP Package	92
8 Lead SOIC Package	157

Maximum Junction Temperature (Die). . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package, Note 1) . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s). . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below $150^{o}C$ for plastic packages. By using Application Note AN556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Operating Conditions section, proper load conditions can be determined.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. $V_O = \pm5V$, R_L Unconnected, Duty cycle ≤ 50%. For information about using high output current amplifiers, please refer to Application Note AN556 (Thermal Safe-Operating-Areas For High Current Op Amps), and the "Power Dissipation Considerations" section in the "Application Information" section of this datasheet.
4. Maximum continuous (100% Duty Cycle) output current is 50mA. For currents >50mA, Duty Cycle must be derated accordingly.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	HA-2842-5, -9			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Offset Voltage (Note 10)		25	-	1	3	mV
		Full	-	-	6	mV
Average Offset Voltage Drift		Full	-	13	-	$\mu V/^{o}C$
Bias Current (Note 10)		25	-	5	10	µA
		Full	-	-	15	µA
Average Bias Current Drift		Full	-	20	-	$nA/^{o}C$
Offset Current		25	-	0.5	1.0	µA
		Full	-	-	1.5	µA
Average Offset Current Drift		Full	-	1.3	-	$nA/^{o}C$
Input Resistance		25	-	170	-	kΩ
Input Capacitance		25	-	1	-	pF
Common Mode Range		Full	±10	-	-	V
Input Noise Voltage	10Hz to 1MHz	25	-	16	-	μV_{RMS}
Input Noise Voltage Density	f = 1kHz, $R_{SOURCE} = 0\Omega$	25	-	16	-	$nV/\sqrt{Hz}$
Input Noise Current (Note 10)	f = 1kHz, $R_{SOURCE} = 100k\Omega$	25	-	2	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	$V_O = \pm10V$	25	50	100	-	kV/V
		Full	30	60	-	kV/V
Common-Mode Rejection Ratio (Note 10)	$V_{CM} = \pm10V$	Full	80	110	-	dB
Minimum Stable Gain		25	2	-	-	V/V
Gain Bandwidth Product (Note 10)	$A_{VCL} = 100$	25	-	80	-	MHz
Gain Flatness to 10MHz (Note 10)	$R_L \geq 75\Omega$	25	-	±0.035	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note, 10)	$V_O = \pm10V$	Full	±10	±11	-	V
Output Current (Note 10)	Note 3	Full	100	-	-	mA

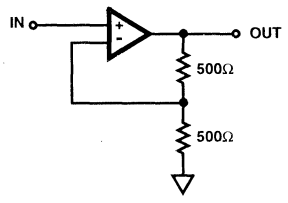
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2842-5, -9			UNITS
			MIN	TYP	MAX	
Output Resistance		25	-	8.5	-	Ω
Full Power Bandwidth (Note 6)	$V_O = \pm10V$	25	5.2	6	-	MHz
Differential Gain (Note 10)	Note 5	25	-	0.02	-	%
Differential Phase (Note 10)	Note 5	25	-	0.03	-	Degrees
Harmonic Distortion (Note 10)	$V_O = 2V_{P-P}$, f = 1MHz, $A_V = 2$	25	-	>81	-	dBc
TRANSIENT RESPONSE (Note 7)						
Rise Time		25	-	4	-	ns
Overshoot		25	-	25	-	%
Slew Rate (Notes 9, 10)	$A_V = +2$	25	325	400	-	V/µs
Settling Time	10V Step to 0.1%	25	-	100	-	ns
POWER REQUIREMENTS						
Supply Current (Note 10)		25	-	14.2	-	mA
		Full	-	14.3	15	mA
Power Supply Rejection Ratio (Note 10)	Note 8	Full	70	80	-	dB

NOTES:

5. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS. $R_F = R_1 = 1k\Omega$, $R_L = 700\Omega$.
6. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 10V$.
7. Refer to Test Circuits section of this data sheet.
8. $V_{SUPPLY} = \pm10V$ to $\pm20V$.
9. This parameter is not tested. The limits are guaranteed based on lab characterization and reflect lot-to-lot variation.
10. See "Typical Performance Curves" for more information.

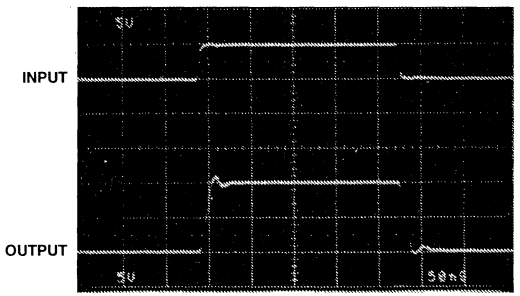
Test Circuits and Waveforms



TEST CIRCUIT

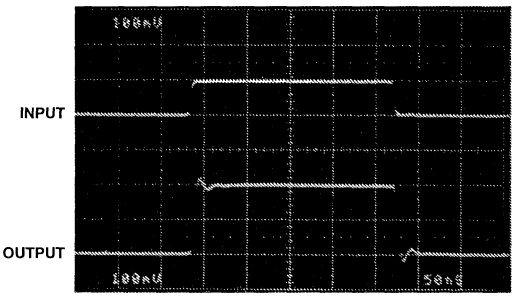
NOTES:

11. $V_S = \pm15V$.
12. $A_V = +2$.
13. $C_L \leq 10pF$



Input = 5V/Div., Output = 5V/Div., 50ns/Div.

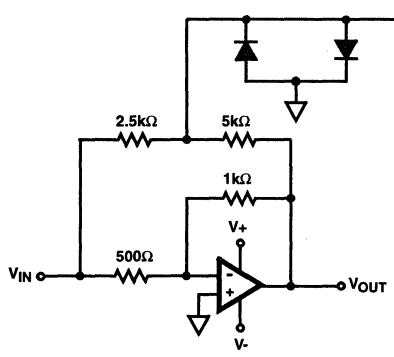
LARGE SIGNAL RESPONSE



Input = 100mV/Div., Output = 100mV/Div., 50ns/Div.

SMALL SIGNAL RESPONSE

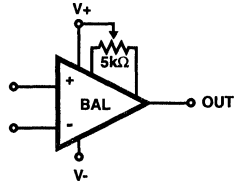
Test Circuits and Waveforms (Continued)



SETTLING TIME TEST CIRCUIT

NOTES:

14. $A_V = -2$.
15. Feedback and summing resistors must be matched (0.1%).
16. HP5082-2810 clipping diodes recommended.
17. Tektronix P6201 FET probe used at settling point.
18. For 0.01% settling time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.



SUGESTED OFFSET VOLTAGE ADJUSTMENT

Application Information

The Harris HA-2842 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2842 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include:

1. Mounting the device through a ground plane.
2. Connecting unused pins (NC) to the ground plane.
3. Mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible.
4. Placing power supply decoupling capacitors from device supply pins to ground.

Power Dissipation Considerations

At high output currents, especially with the 8 lead SOIC package, care must be taken to ensure that the Maximum Junction Temperature (T_J, see "Absolute Maximum Ratings" table) isn't exceeded. As an example consider the HA-2842 in the SOIC package, with a required output current of 50mA at $V_{OUT} = 10V$ with ±15V supplies. The power dissipation is the quiescent power (450mW = 30V x 15mA) plus the power dissipated in the output stage ($P_{OUT} = 250mW = 50mA \times (15V - 10V)$), or a total of 700mW. The thermal resistance (θ_{JA}) of the SOIC package is 157°C/W, which increases the junction temperature by 110°C over the ambient temperature (T_A). Remaining below T_{JMAX} requires that T_A be restricted to ≤ 40°C (150°C - 110°C). Heatsinking would be required for operation at ambient temperatures greater than 40°C.

Note that the problem isn't as severe with either of the PDIP packages due to their lower thermal resistances, however it is recommended that the above analysis be performed for any package if operating outside the conditions listed below:

MAX P_{OUT} WITHOUT HEATSINK (V_S = ±15V)

T_A	14 LEAD PDIP (θ_{JA} = 89°C/W)	8 LEAD PDIP (θ_{JA} = 92°C/W)	8 LEAD SOIC (θ_{JA} = 157°C/W)
85°C	280mW	260mW	Heatsink Required
70°C	450mW	420mW	60mW
25°C	950mW	910mW	350mW

Allowable output power can be increased by decreasing the quiescent dissipation via lower supply voltages.

For more information please refer to Application Note AN556, Thermal Safe Operating Areas for High Current Op Amps.

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

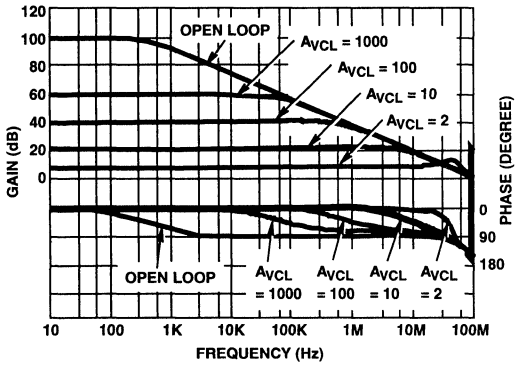


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS GAINS

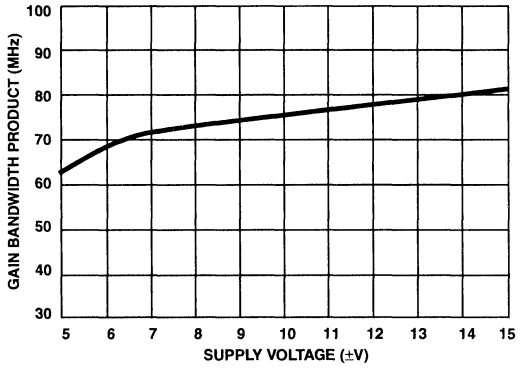


FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

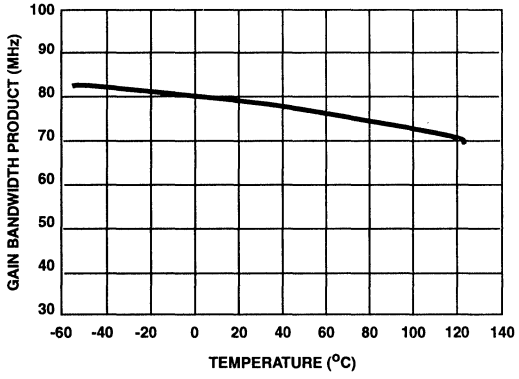


FIGURE 3. GAIN BANDWIDTH PRODUCT vs TEMPERATURE

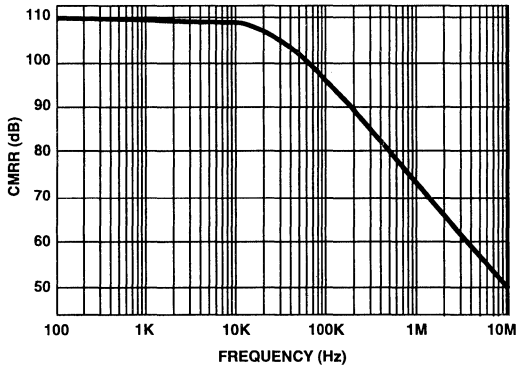


FIGURE 4. CMRR vs FREQUENCY

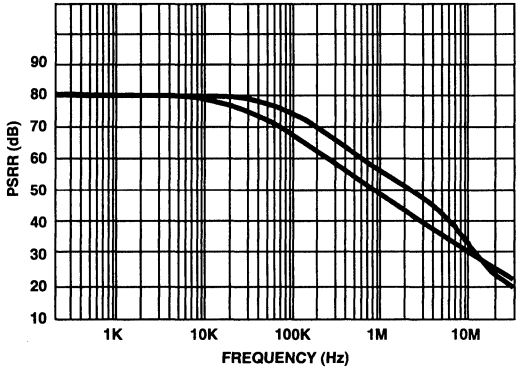


FIGURE 5. PSRR vs FREQUENCY

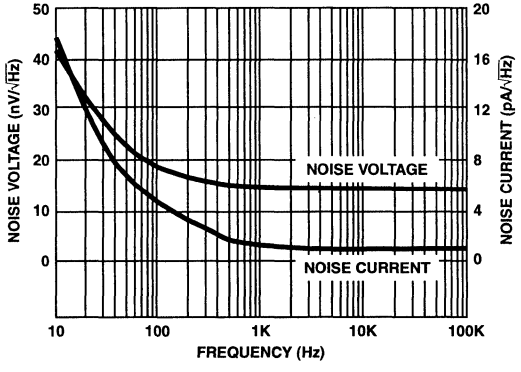


FIGURE 6. INPUT NOISE vs FREQUENCY

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified **(Continued)**

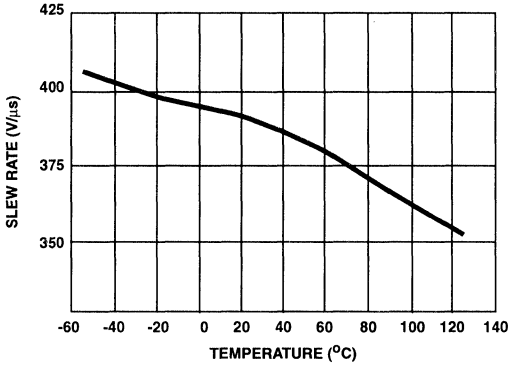


FIGURE 7. SLEW RATE vs TEMPERATURE

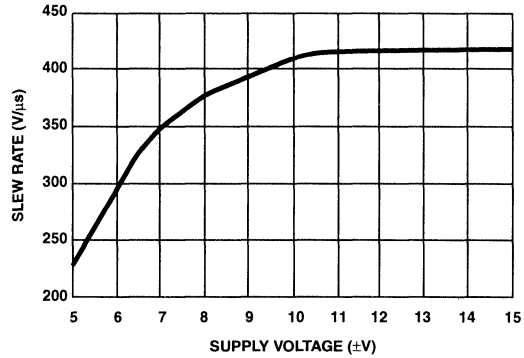


FIGURE 8. SLEW RATE vs SUPPLY VOLTAGE

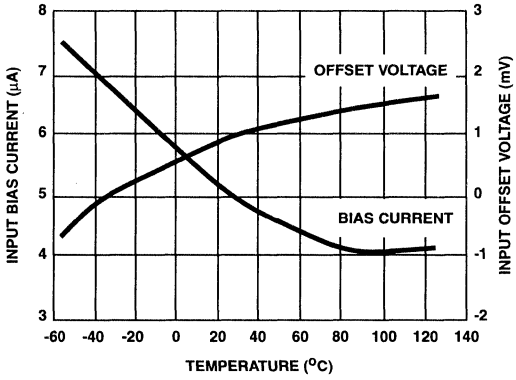


FIGURE 9. INPUT OFFSET VOLTAGE AND INPUT BIAS CURRENT vs TEMPERATURE

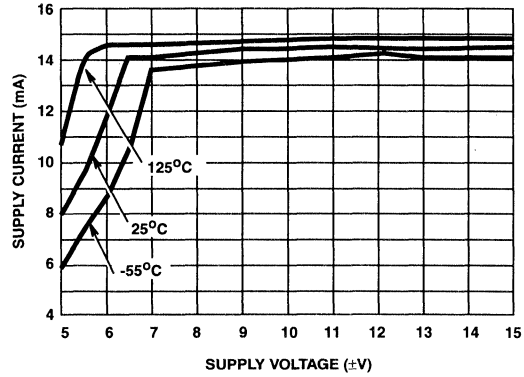


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

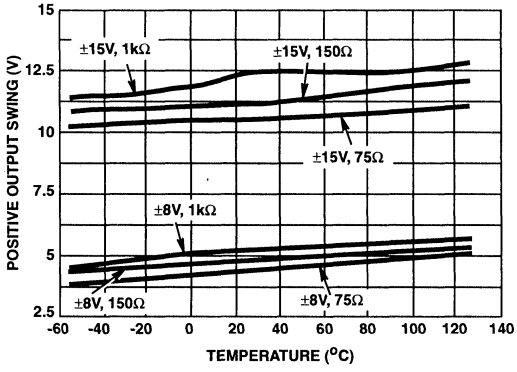


FIGURE 11. POSITIVE OUTPUT SWING vs TEMPERATURE

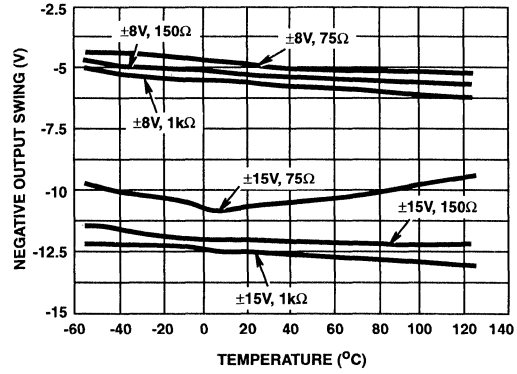


FIGURE 12. NEGATIVE OUTPUT SWING vs TEMPERATURE

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified **(Continued)**

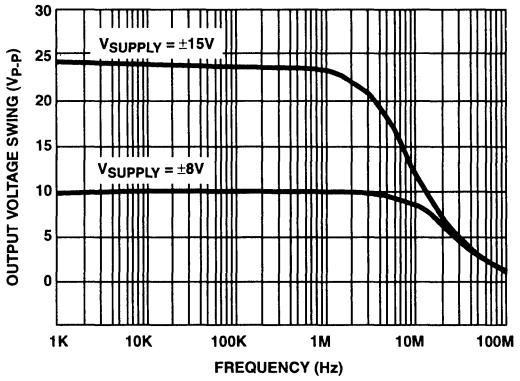


FIGURE 13. MAXIMUM UNDISTORTED OUTPUT SWING vs FREQUENCY

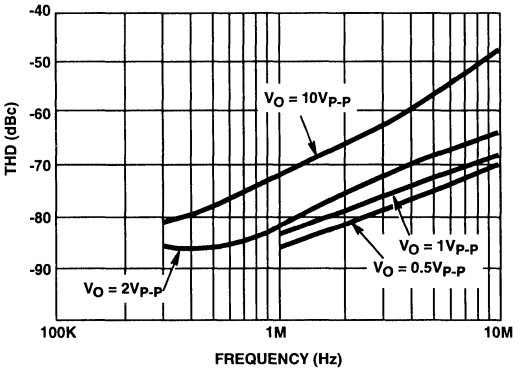


FIGURE 14. TOTAL HARMONIC DISTORTION vs FREQUENCY

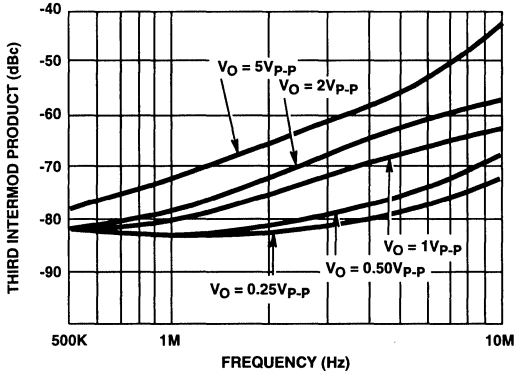


FIGURE 15. INTERMODULATION DISTORTION vs FREQUENCY (TWO TONE)

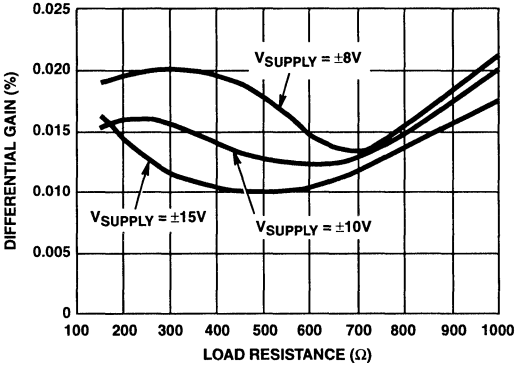


FIGURE 16. DIFFERENTIAL GAIN vs LOAD RESISTANCE

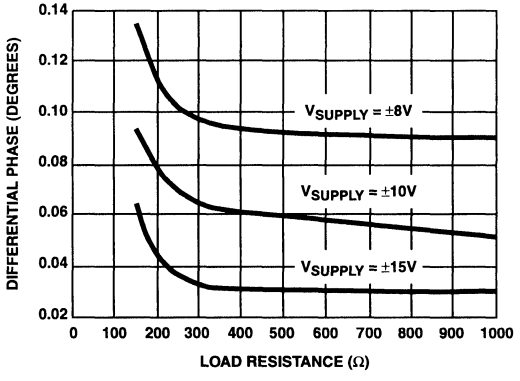


FIGURE 17. DIFFERENTIAL PHASE vs LOAD RESISTANCE

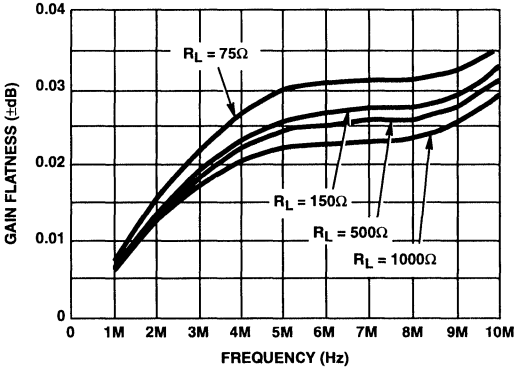


FIGURE 18. GAIN FLATNESS vs FREQUENCY ($A_{VCL} = 2$)

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified (Continued)

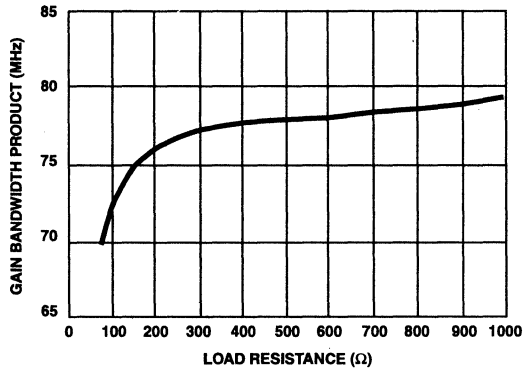


FIGURE 19. GAIN BANDWIDTH PRODUCT vs LOAD RESISTANCE

Metallization Topology

DIE DIMENSIONS:

77 mils x 81 mils x 19 mils
1960µm x 2060µm x 483µm

METALLIZATION:

Type: Aluminum, 1% Copper
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride thickness: 3.5kÅ ±1kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

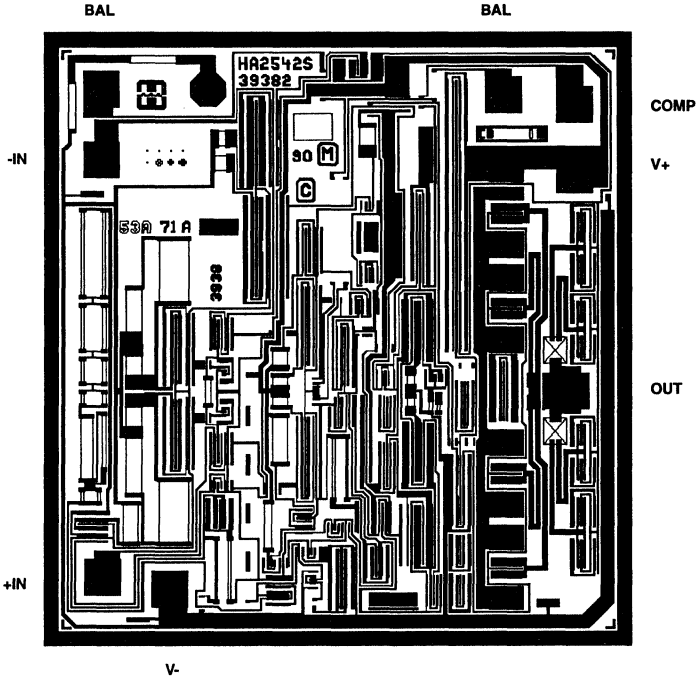
58

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2842



Complete data sheet available via web, Harris' home page: http://www.semi.harris.com/ or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

HA-2850

470MHz, Low Power, High Slew Rate Operational Amplifier

November 1996

Features

- Low Supply Current 7.5mA
- High Slew Rate 340V/μs
- Open Loop Gain 25kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 470MHz
- Full Power Bandwidth 5.4MHz
- Low Offset Voltage 0.6mV
- Input Noise Voltage . . . . . $11nV/\sqrt{Hz}$
- Differential Gain/Phase . . . . . 0.04%/0.04 Degrees
- Lower Power Enhanced Replacement for AD840 and EL2040

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

Description

The HA-2850 is a wideband, high slew rate, operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction, coupled with dielectric isolation, delivers outstanding performance in circuits with a closed loop gain of 10 or greater.

A 340V/μs slew rate and a 470MHz gain bandwidth product ensure high performance in video and wideband amplifier designs. Differential gain and phase are a low 0.04% and 0.04 degrees respectively, making the HA-2850 ideal for video applications. A full ±10V output swing, high open loop gain, and outstanding AC parameters, make the HA-2850 an excellent choice for high speed Data Acquisition Systems.

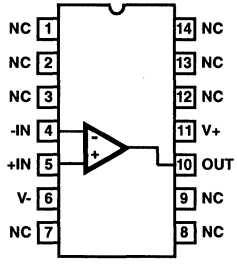
The HA-2850 is available in commercial and industrial temperature ranges, and a choice of packages. For military grade product, refer to the HA-2850/883 data sheet. Harris AnswerFAX (407-724-7800) Document #3595.

Ordering Information

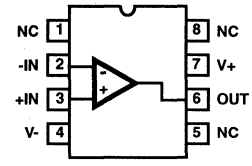
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3B2850-5	0 to 75	14 Ld PDIP	E14.3
HA3-2850-5	0 to 75	8 Ld PDIP	E8.3
HA9P2850-5 (H28505)	0 to 75	8 Ld SOIC	M8.15
HA3B2850-9	-40 to 85	14 Ld PDIP	E14.3
HA3-2850-9	-40 to 85	8 Ld PDIP	E8.3

Pinouts

HA-2850 (PDIP) TOP VIEW



HA-2850 (PDIP, SOIC) TOP VIEW



NOTE: No Connection (NC) pins may be tied to a ground plane for better isolation and heat dissipation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2844.3**

HARRIS SEMICONDUCTOR

HA-4741

November 1996

Quad, 3.5MHz, Operational Amplifier

Features

- Slew Rate 1.6V/μs
- Bandwidth. 3.5MHz
- Input Voltage Noise . . . . . 9nV/√Hz
- Input Offset Voltage 0.5mV
- Input Bias Current 60nA
- Supply Range. . . . . ±2V to ±20V
- No Crossover Distortion
- Standard Quad Pinout

Applications

- Universal Active Filters
- D3 Communications Filters
- Audio Amplifiers
- Battery-Powered Equipment

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-4741-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-4741-5	0 to 75	14 Ld CERDIP	F14.3
HA3-4741-5	0 to 75	14 Ld PDIP	E14.3
HA9P4741-9	-40 to 85	16 Ld SOIC	M16.3

Description

HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/√Hz at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion.

These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (69dB at 10kHz).

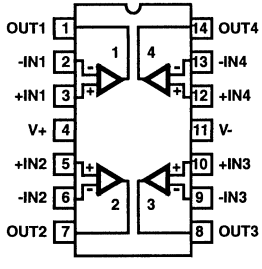
A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

HA-4741/883 product and data sheets available upon request.

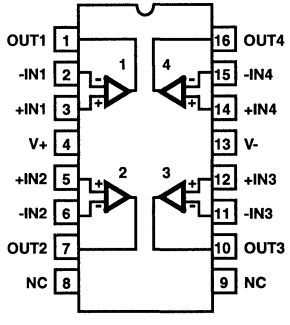
3 OPERATIONAL AMPLIFIERS

Pinouts

HA-4741
(PDIP, CERDIP)
TOP VIEW



HA-4741
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **2922.2**

Absolute Maximum Ratings

T_A = 25°C Unless Otherwise Stated
Supply Voltage Between V+ and V- Terminals 40V
Differential Input Voltage. 30V
Input Voltage. . . . . V_{SUPPLY}
Output Short Circuit Duration (Note 3) . . . . . Indefinite

Operating Conditions

Temperature Range:
HA-4741-2. . . . . -55°C to 125°C
HA-4741-5. . . . . 0°C to 75°C
HA-4741-9. . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	90	35
PDIP Package	107	N/A
SOIC Package	96	N/A

Maximum Junction Temperature (Ceramic Package, Note 1) . . . . . 175°C
Maximum Junction Temperature (Plastic Packages, Note 1) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175°C for the ceramic package, and below 150°C for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. One amplifier may be shorted to ground indefinitely.

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-4741-2			HA-4741-5			(NOTE 4) HA-4741-9	UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MAX	
INPUT CHARACTERISTICS										
Offset Voltage		25	-	0.5	3	-	1	5	5	mV
		Full	-	4	5	-	4	6.5	8.5	mV
Average Offset Voltage Drift		Full	-	5	-	-	5	-		µV/°C
Bias Current		25	-	60	200	-	60	300	300	nA
		Full	-	-	325	-	-	400	400	nA
Offset Current		25	-	15	30	-	30	50	50	nA
		Full	-	-	75	-	-	100	100	nA
Common Mode Range		Full	±12	-	-	±12	-	-	-	V
Differential Input Resistance		25	-	0.5	-	-	0.5	-	-	MΩ
Input Voltage Noise	f = 1kHz	25	-	9	-	-	9	-	-	nV/√Hz
TRANSFER CHARACTERISTICS										
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2kΩ	25	50	100	-	25	50	-	-	kV/V
		Full	25	-	-	15	-	-	-	kV/V
Common Mode Rejection Ratio		25	80	95	-	80	95	-	-	dB
		Full	74	-	-	74	-	-	-	dB
Channel Separation (Note 5)		25	66	69	-	66	69	-	-	dB
Small Signal Bandwidth		25	2.5	3.5	-	2.5	3.5	-		MHz
OUTPUT CHARACTERISTICS										
Output Voltage Swing	R_L = 10kΩ	Full	±12	±13.7	-	±12	±13.7	-	-	V
Output Voltage Swing	R_L = 2kΩ	Full	±10	±12.5	-	±10	±12.5	-	-	V
Full Power Bandwidth (Notes 6, 7)		25	-	25	-	-	25	-	-	kHz
Output Current	V_{OUT} = ±10V	Full	±5	±15	-	±5	±15	-	-	mA
Output Resistance		25	-	300	-	-	300	-	-	Ω
TRANSIENT RESPONSE R_L = 2kΩ, C_L = 50pF										
Rise Time	V_{OUT} = ±200mV	25	-	75	140	-	75	140	140	ns
Overshoot		25	-	25	40	-	25	40	40	%

Electrical Specifications $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-4741-2			HA-4741-5			(NOTE 4) HA-4741-9	UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MAX	
Slew Rate	$V_{OUT} = \pm5V$	25	-	±1.6	-	-	±1.6	-	-	V/µs
POWER SUPPLY CHARACTERISTICS										
Supply Current		25	-	4.5	5	-	5	7	7	mA
Power Supply Rejection Ratio	$\Delta V_S = \pm5V$	Full	80	95	-	80	95	-	-	dB

NOTES:

4. Typical and Minimum specifications for the -9 version are the same as those for the -5 version.
5. Referred to input; f = 10kHz, $R_S = 1k\Omega$, $V_{IN} = 100mV_{PEAK}$.
6. $V_{OUT} = \pm10V$, $R_L = 2k\Omega$.
7. Full power bandwidth guaranteed based upon slew rate measurement: FPBW = S.R./2π V_{PEAK}.

Test Circuit and Waveforms

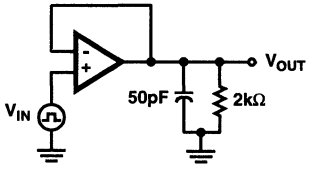
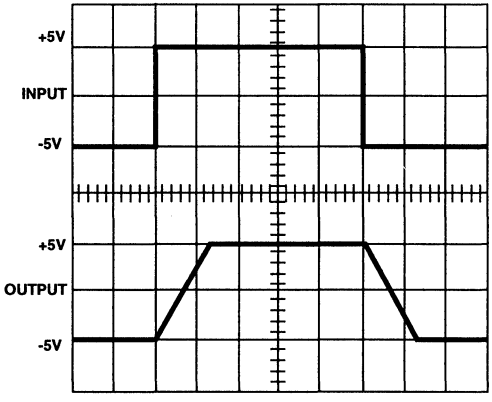
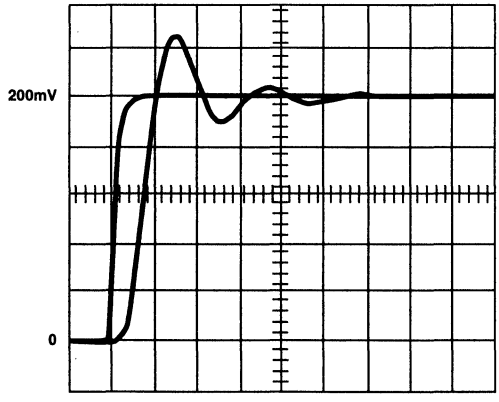


FIGURE 1. SMALL AND LARGE SIGNAL TEST CIRCUIT



Volts = 5V/Div., Time = 5µs/Div.

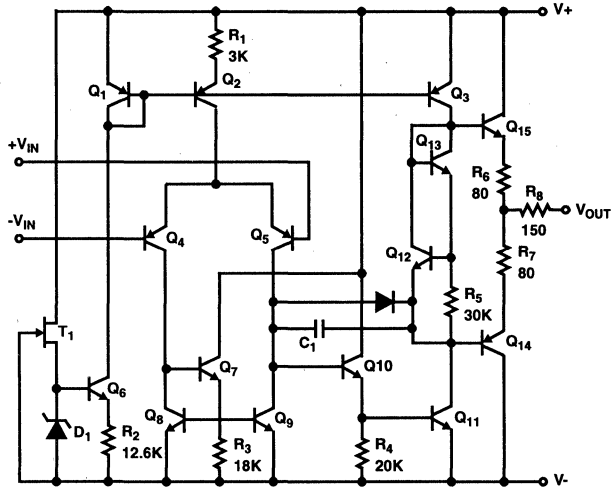
FIGURE 2. LARGE SIGNAL RESPONSE



Volts = 40mV/Div., Time = 100ns/Div.

FIGURE 3. SMALL SIGNAL RESPONSE

Schematic Diagram



Typical Performance Curves $V_{SUPPLY} = \pm 15V$, $T_A = 25^oC$, Unless Otherwise Specified

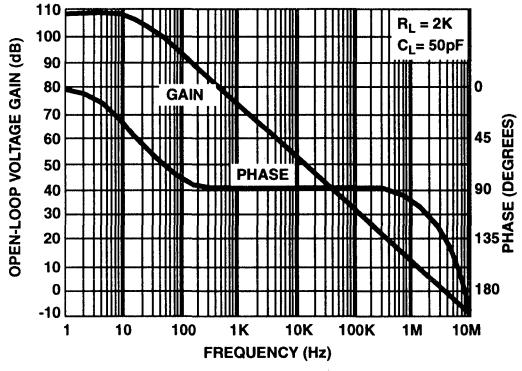


FIGURE 4. OPEN LOOP FREQUENCY RESPONSE

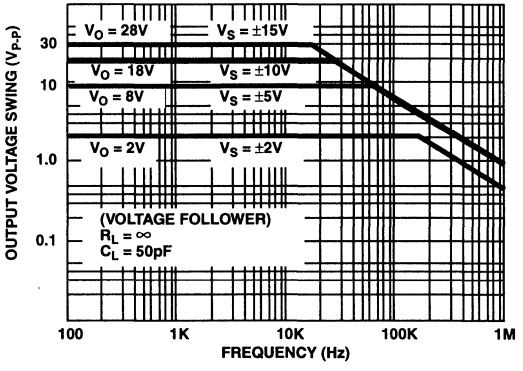


FIGURE 5. OUTPUT VOLTAGE SWING vs FREQUENCY

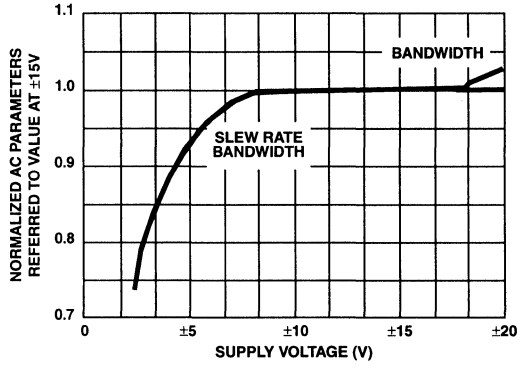


FIGURE 6. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

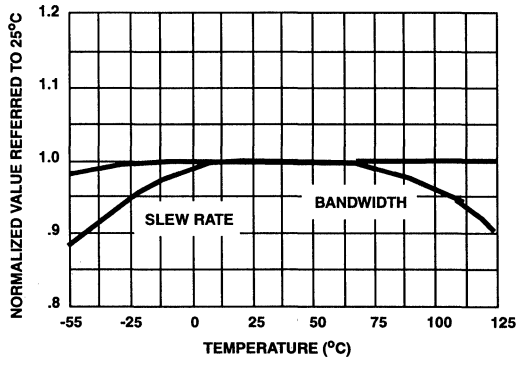


FIGURE 7. NORMALIZED AC PARAMETERS vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

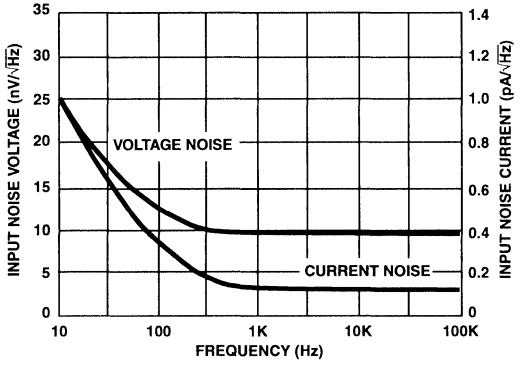


FIGURE 8. INPUT NOISE vs FREQUENCY

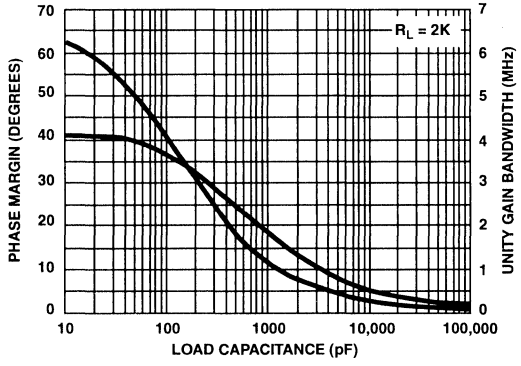


FIGURE 9. SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

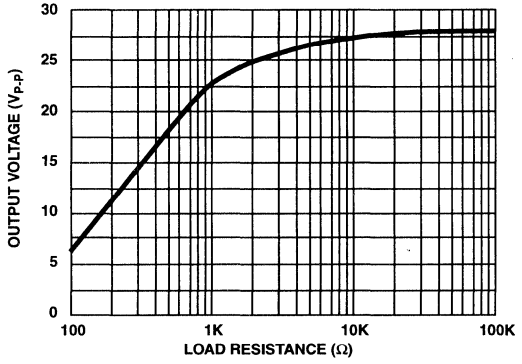


FIGURE 10. MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

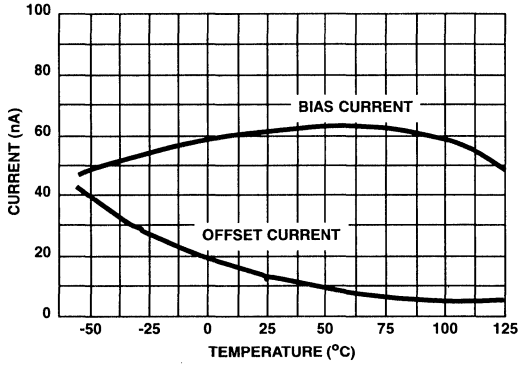


FIGURE 11. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

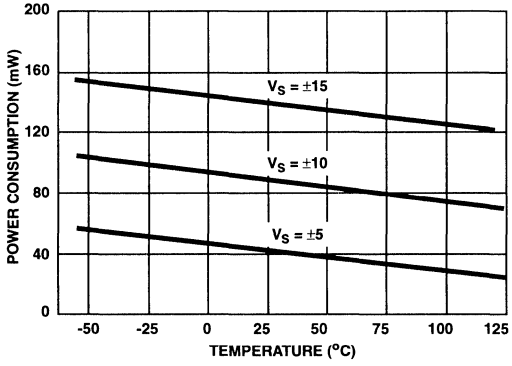


FIGURE 12. POWER CONSUMPTION vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

87 mils x 75 mils x 19 mils
2210µm x 1910µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride
Thickness: 7kÅ ±0.7kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

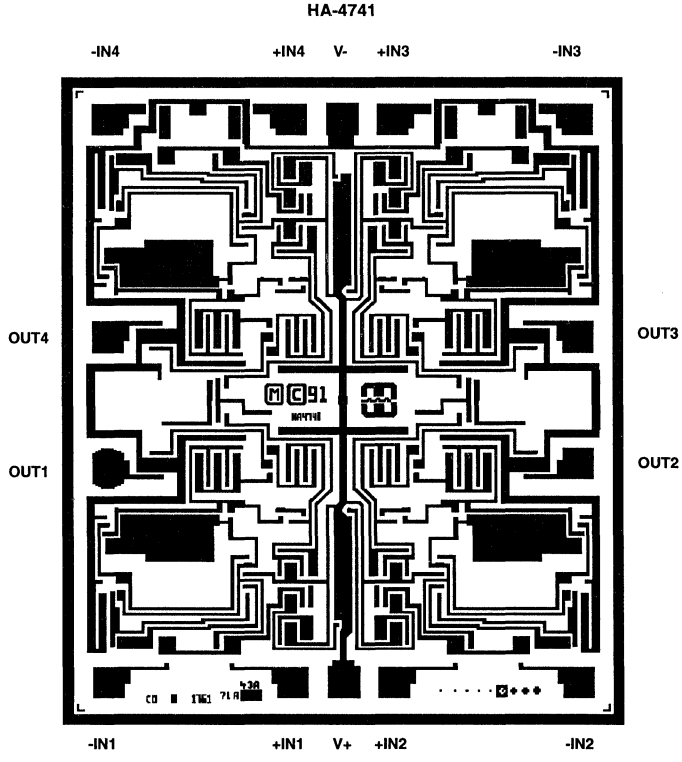
TRANSISTOR COUNT:

72

PROCESS:

Junction Isolated Bipolar/JFET

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HA-5002

110MHz, High Slew Rate, High Output Current Buffer

November 1996

Features

- Voltage Gain 0.995
- High Input Impedance 3000kΩ
- Low Output Impedance 3Ω
- Very High Slew Rate 1300V/μs
- Very Wide Bandwidth 110MHz
- High Output Current ..... ±200mA
- Pulsed Output Current 400mA
- Monolithic Construction

Applications

- Line Driver
- Data Acquisition
- 110MHz Buffer
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Radar Cable Driver
- Video Products

Description

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Harris D.I. technologies, the HA-5002 current buffer offers 1300V/μs slew rate with 110MHz of bandwidth. The ±200mA output current capability is enhanced by a 3Ω output impedance.

The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000kΩ input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

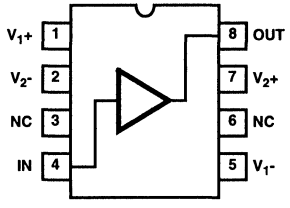
For the military grade product, refer to the HA-5002/883 datasheet.

Ordering Information

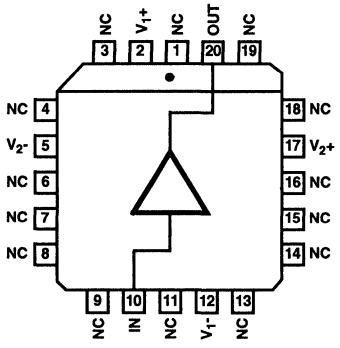
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-5002-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-5002-5	0 to 75	8 Pin Metal Can	T8.C
HA3-5002-5	0 to 75	8 Ld PDIP	E8.3
HA4P5002-5	0 to 75	20 Ld PLCC	N20.35
HA7-5002-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5002-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P5002-5 (H50025)	0 to 75	8 Ld SOIC	M8.15
HA9P5002-9 (H50029)	-40 to 85	8 Ld SOIC	M8.15

Pinouts

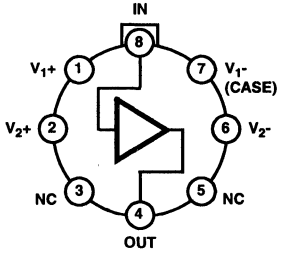
HA-5002 (PDIP, CERDIP, SOIC)
TOP VIEW



HA-5002 (PLCC)
TOP VIEW



HA-5002 (METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2921.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Input Voltage. . . . . V_1+ to V_1-
Output Current (Continuous) . . . . . ±200mA
Output Current (50ms On, 1s Off) . . . . . ±400mA

Operating Conditions

Temperature Range
HA-5002-2. . . . . -55°C to 125°C
HA-5002-5. . . . . 0°C to 75°C
HA-5002-9. . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	115	28
PDIP Package	92	N/A
Metal Can Package	155	67
PLCC Package	74	N/A
SOIC Package	157	N/A

Maximum Junction Temperature (Hermetic Packages, Note 1) . . . 175°C
Maximum Junction Temperature (Plastic Packages, Note 1) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC and SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below 175°C for the ceramic and can packages, and below 150°C for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5002-2			HA-5002-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	5	20	-	5	20	mV
		Full	-	10	30	-	10	30	mV
Average Offset Voltage Drift		Full	-	30	-	-	30	-	µV/°C
Bias Current		25	-	2	7	-	2	7	µA
		Full	-	3.4	10	-	2.4	10	µA
Input Resistance		Full	1.5	3	-	1.5	3	-	MΩ
Input Noise Voltage	10Hz-1MHz	25	-	18	-	-	18	-	μV_{P-P}
TRANSFER CHARACTERISTICS									
Voltage Gain (V_{OUT} = ±10V)	R_L = 50Ω	25	-	0.900	-	-	0.900	-	V/V
	R_L = 100Ω	25	-	0.971	-	-	0.971	-	V/V
	R_L = 1kΩ	25	-	0.995	-	-	0.995	-	V/V
	R_L = 1kΩ	Full	0.980	-	-	0.980	-	-	V/V
-3dB Bandwidth	V_{IN} = $1V_{P-P}$	25	-	110	-	-	110	-	MHz
AC Current Gain		25	-	40	-	-	40	-	A/mA
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 100Ω	25	±10	±10.7	-	±10	±11.2	-	V
	R_L = 1kΩ, V_S = ±15V	Full	±10	±13.5	-	±10	±13.9	-	V
	R_L = 1kΩ, V_S = ±12V	Full	±10	±10.5	-	±10	±10.5	-	V
Output Current	V_{IN} = ±10V, R_L = 40Ω	25	-	220	-	-	220	-	mA
Output Resistance		Full	-	3	10	-	3	10	Ω
Harmonic Distortion	V_{IN} = $1V_{RMS}$, f = 10kHz	25	-	<0.005	-	-	<0.005	-	%
TRANSIENT RESPONSE									
Full Power Bandwidth (Note 3)		25	-	20.7	-	-	20.7	-	MHz
Rise Time		25	-	3.6	-	-	3.6	-	ns
Propagation Delay		25	-	2	-	-	2	-	ns
Overshoot		25	-	30	-	-	30	-	%
Slew Rate		25	1.0	1.3	-	1.0	1.3	-	V/ns
Settling Time	To 0.1%	25	-	50	-	-	50	-	ns
Differential Gain	R_L = 500Ω	25	-	0.06	-	-	0.06	-	%
Differential Phase	R_L = 500Ω	25	-	0.22	-	-	0.22	-	Degrees

Electrical Specifications $V_{SUPPLY} = \pm12V$ to $\pm15V$, $R_S = 50\Omega$, $R_L = 1k\Omega$, $C_L = 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5002-2			HA-5002-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER REQUIREMENTS									
Supply Current		25	-	8.3	-	-	8.3	-	mA
		Full	-	-	10	-	-	10	mA
Power Supply Rejection Ratio	$A_V = 10V$	Full	54	64	-	54	64	-	dB

NOTE:

3. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_P = 10V$.

Test Circuit and Waveforms

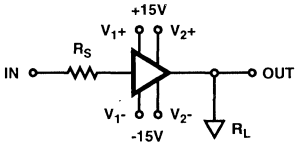
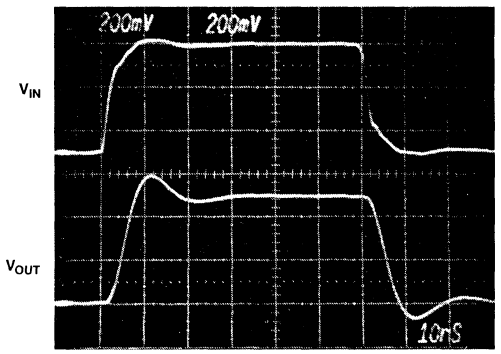
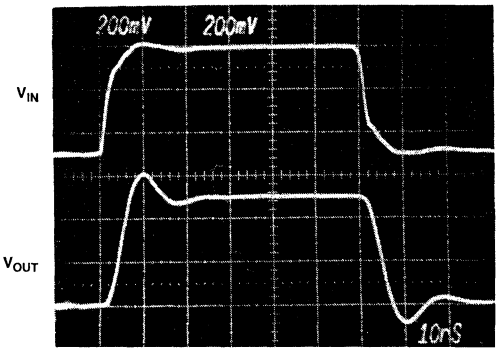


FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE



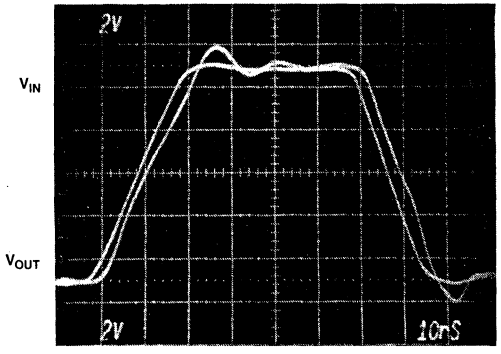
$R_S = 50\Omega$, $R_L = 100\Omega$

SMALL SIGNAL WAVEFORMS



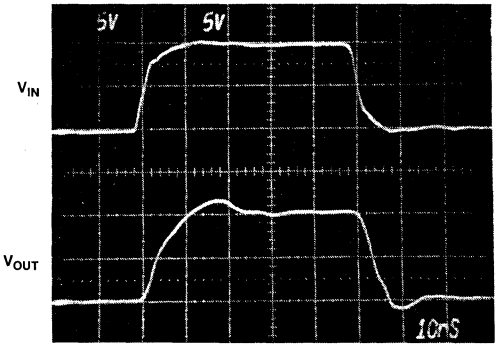
$R_S = 50\Omega$, $R_L = 1k\Omega$

SMALL SIGNAL WAVEFORMS



$R_S = 50\Omega$, $R_L = 100\Omega$

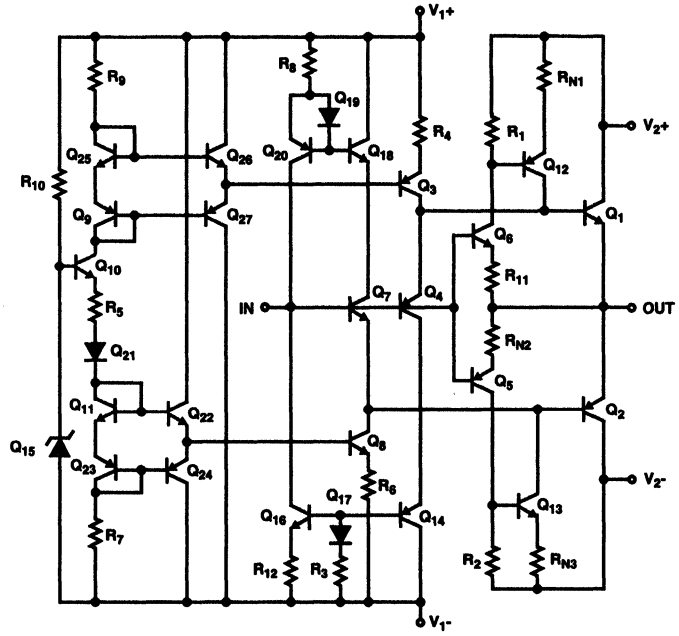
LARGE SIGNAL WAVEFORMS



$R_S = 50\Omega$, $R_L = 1k\Omega$

LARGE SIGNAL WAVEFORMS

Schematic Diagram



Application Information

Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimal device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1µF will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

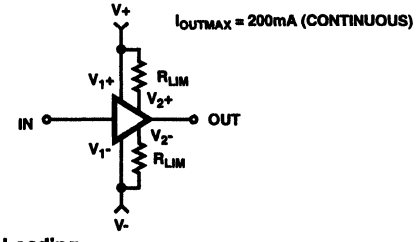
Operation at Reduced Supply Levels

The HA-5002 can operate at supply voltage levels as low as ±5V and lower. Output swing is directly affected as well as slight reductions in slew rate and bandwidth.

Short Circuit Protection

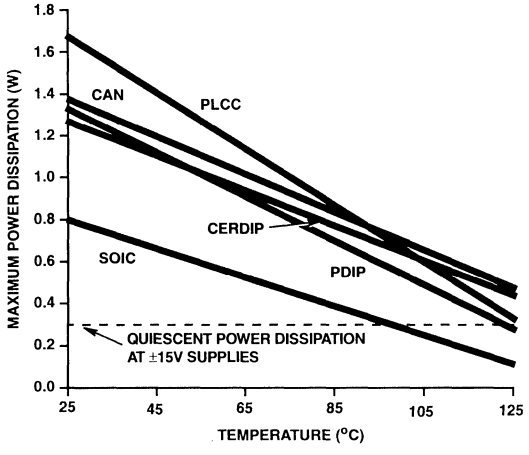
The output current can be limited by using the following circuit:

$$R_{LIM} = \frac{V+}{I_{OUTMAX}} = \frac{V-}{I_{OUTMAX}}$$



Capacitive Loading

The HA-5002 will drive large capacitive loads without oscillation but peak current limits should not be exceeded. Following the formula I = Cdv/dt implies that the slew rate or the capacitive load must be controlled to keep peak current below the maximum or use the current limiting approach as shown. The HA-5002 can become unstable with small capacitive loads (50pF) if certain precautions are not taken. Stability is enhanced by any one of the following: a source resistance in series with the input of 50Ω to 1kΩ; increasing capacitive load to 150pF or greater; decreasing C_{LOAD} to 20pF or less; adding an output resistor of 10Ω to 50Ω; or adding feedback capacitance of 50pF or greater. Adding source resistance generally yields the best results.



$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

Where: T_{JMAX} = Maximum Junction Temperature of the Device

T_A = Ambient

θ_{JC} = Junction to Case Thermal Resistance

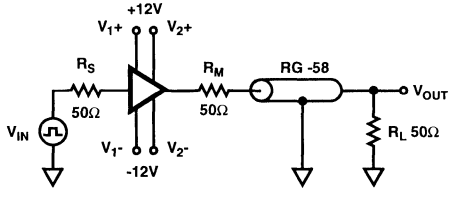
θ_{CS} = Case to Heat Sink Thermal Resistance

θ_{SA} = Heat Sink to Ambient Thermal Resistance

Graph is based on: $P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$

FIGURE 2. FREE AIR POWER DISSIPATION

Typical Application



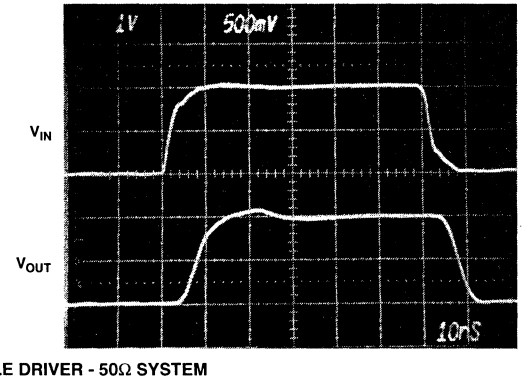


FIGURE 3. COAXIAL CABLE DRIVER - 50Ω SYSTEM

Typical Performance Curves

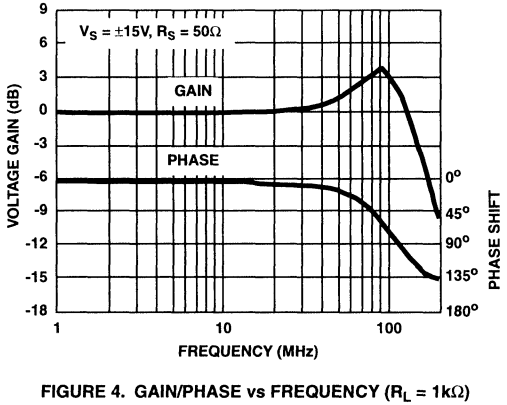


FIGURE 4. GAIN/PHASE vs FREQUENCY (R_L = 1kΩ)

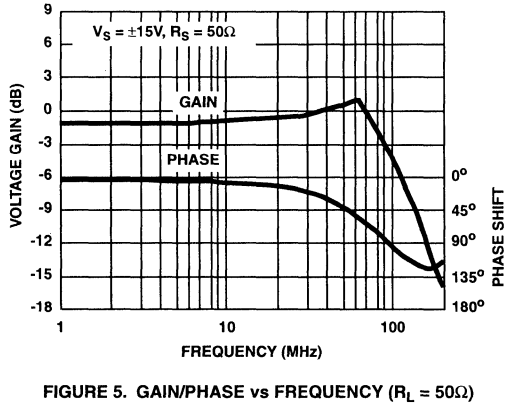


FIGURE 5. GAIN/PHASE vs FREQUENCY (R_L = 50Ω)

Typical Performance Curves (Continued)

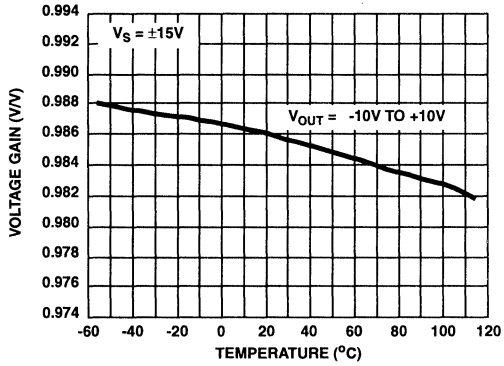


FIGURE 6. VOLTAGE GAIN vs TEMPERATURE (R_L = 100Ω)

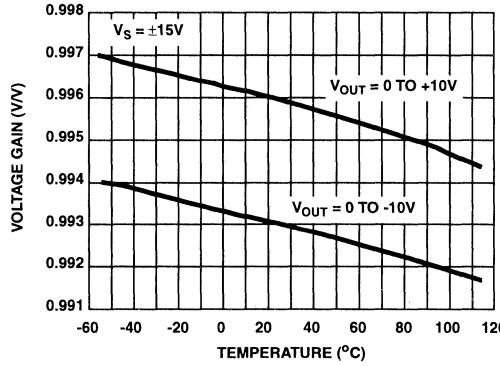


FIGURE 7. VOLTAGE GAIN vs TEMPERATURE (R_L = 1kΩ)

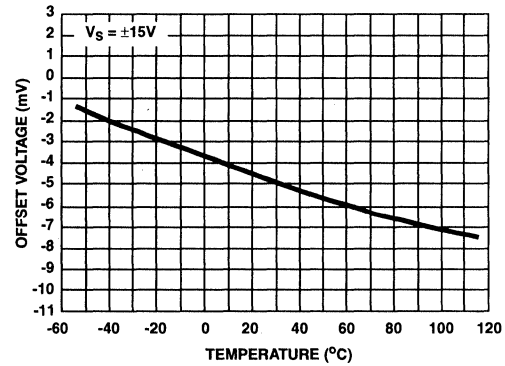


FIGURE 8. OFFSET VOLTAGE vs TEMPERATURE

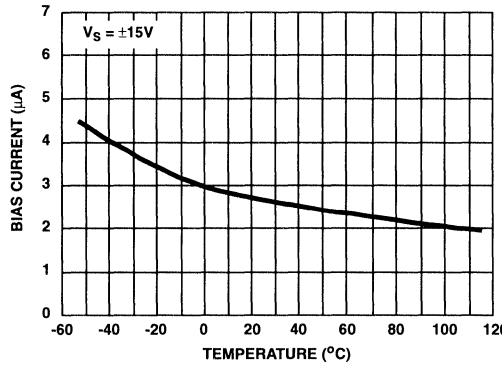


FIGURE 9. BIAS CURRENT vs TEMPERATURE

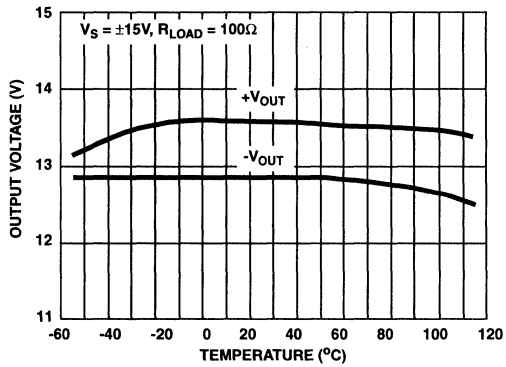


FIGURE 10. MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

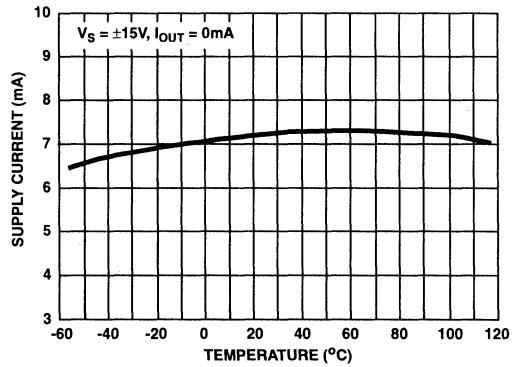


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

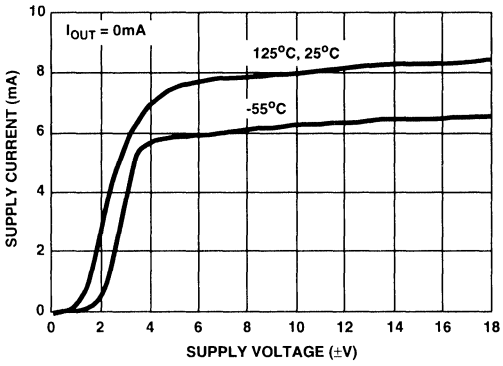


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

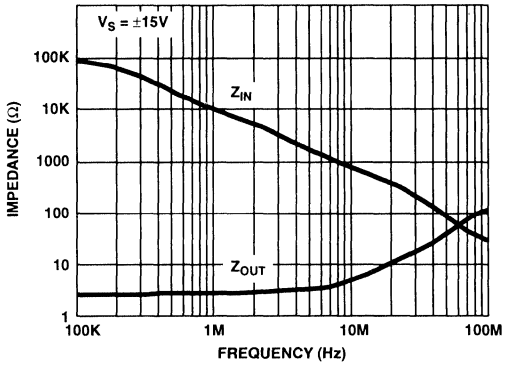


FIGURE 13. INPUT/OUTPUT IMPEDANCE vs FREQUENCY

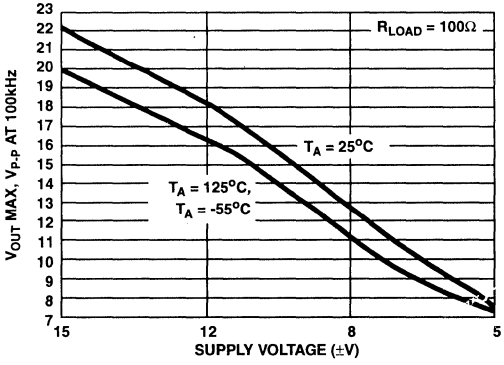


FIGURE 14. V_{OUT} MAXIMUM vs V_{SUPPLY}

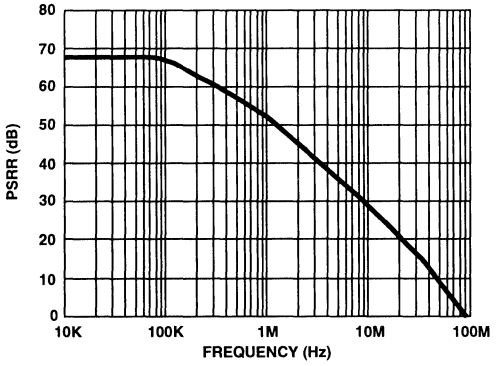


FIGURE 15. PSRR vs FREQUENCY

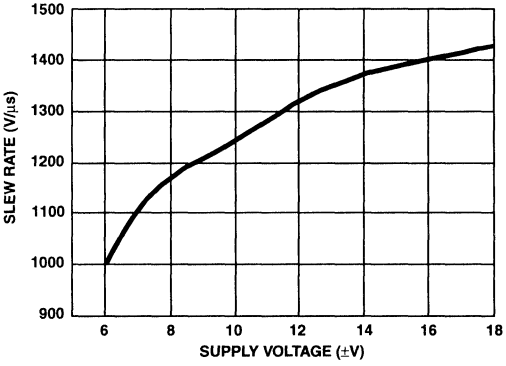


FIGURE 16. SLEW RATE vs SUPPLY VOLTAGE

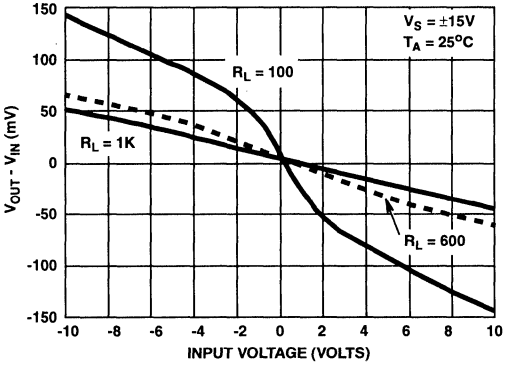


FIGURE 17. GAIN ERROR vs INPUT VOLTAGE

3 OPERATIONAL AMPLIFIERS

Die Characteristics

DIE DIMENSIONS:

81 mils x 80 mils x 19 mils
2050µm x 2030µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 20kÅ ±2kÅ

PASSIVATION:

Type: Nitride
Thickness: 7kÅ ±0.7kÅ

SUBSTRATE POTENTIAL (Powered Up):

V1-

TRANSISTOR COUNT:

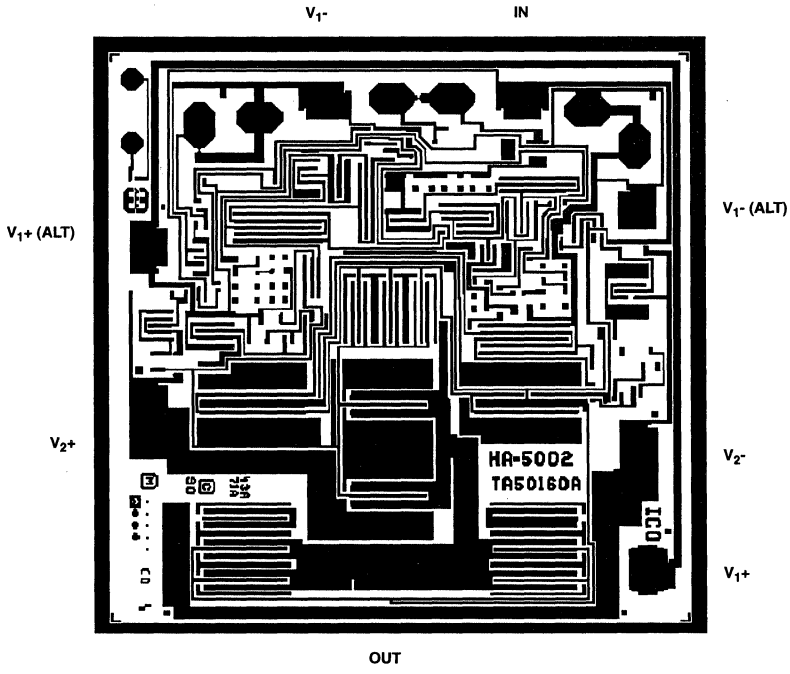
27

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5002



NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HA-5004

November 1996

100MHz Current Feedback Amplifier

Features

- Slew Rate 1200V/µs
- Output Current ..... ±100mA
- Drives ..... ±9V into 100Ω
- V_{SUPPLY} ..... ±5V to ±18V
- Thermal Overload Protection and Output Flag
- Bandwidth Nearly Independent of Gain
- Output Enable/Disable

Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- High Speed Peak Detector
- Fiber Optic Transmitters
- Zero Insertion Loss Transmission Line Drivers
- Current to Voltage Converter
- Radar Systems

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-5004-5	0 to 70	14 Ld CERDIP	F14.3
HA1-5004-9	-40 to 85	14 Ld CERDIP	F14.3

Description

The HA-5004 current feedback amplifier is a video/wideband amplifier optimized for low gain applications. The design is based on current-mode feedback which allows the amplifier to achieve higher closed loop bandwidth than voltage-mode feedback operational amplifiers. Since feedback is employed, the HA-5004 can offer better gain accuracy and lower distortion than open loop buffers. Unlike conventional op amps, the bandwidth and rise time of the HA-5004 are nearly independent of closed loop gain. The 100MHz bandwidth at unity gain reduces to only 65MHz at a gain of 10. The HA-5004 may be used in place of a conventional op amp with a significant improvement in speed power product.

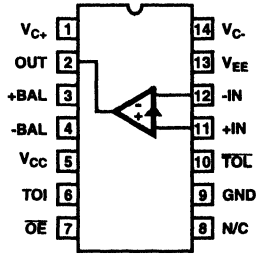
Several features have been designed in for added value. A thermal overload feature protects the part against excessive junction temperature by shutting down the output. If this feature is not needed, it can be inhibited via a TTL input (TOI). A TTL chip enable/disable ($\overline{OE}$) is also provided; when the chip is disabled its output is high impedance. Finally, an open collector output flag ($\overline{TOL}$) is provided to indicate the status of the chip. The status flag goes low to indicate when the chip is disabled due to either the internal Thermal Overload shutdown or the external disable.

In order to maximize bandwidth and output drive capacity, internal current limiting is not provided. However, current limiting may be applied via the V_C+ and V_C- pins which provide power separately to the output stage.

For Military grade product refer to the HA-5004/883 data sheet.

Pinout

HA-5004
(CERDIP)
TOP VIEW



TRUTH TABLE

INPUTS		TEMP	$\overline{TOL}$ OUTPUT (OPEN COLLECTOR)	OPERATION
$\overline{OE}$	TOI	T_J		
0	0	Normal	1	Normal
0	0	High (Note)	0	Auto Shutdown, HI-Z OUT
0	1	X	1	Normal
1	X	X	0	Manual Shutdown, HI-Z OUT

NOTE: >180°C Typical

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2923.2**

HARRIS SEMICONDUCTOR

HA5013

November 1996

Triple, 125MHz Video Amplifier

Features

- Wide Unity Gain Bandwidth 125MHz
- Slew Rate 475V/μs
- Input Offset Voltage 800μV
- Differential Gain 0.03%
- Differential Phase ..... 0.03 Degrees
- Supply Current (Per Amplifier) 7.5mA
- ESD Protection 4000V
- Guaranteed Specifications at ±5V Supplies
- Low Cost

Applications

- PC Add-On Multimedia Boards
- Flash A/D Driver
- Color Image Scanners
- CCD Cameras and Systems
- RGB Cable Driver
- RGB Video Preamp
- PC Video Conferencing

Description

The HA5013 is a low cost triple amplifier optimized for RGB video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor.

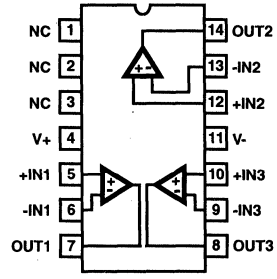
The performance of the HA5013 is very similar to the popular Harris HA-5020 single video amplifier.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA5013IP	-40 to 85	14 Ld PDIP	E14.3
HA5013IB	-40 to 85	14 Ld SOIC	M14.15
HA5025EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HA5013
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number **3654.3**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
DC Input Voltage . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage. 10V
Output Current (Note 2) . . . . . Short Circuit Protected
ESD Rating (Note 4)
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 2000V

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage Range (Typical) . . . . . ±4.5V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	100
SOIC Package	120

Maximum Junction Temperature (Die Only, Note 3) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package, Note 3) . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.
3. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175^oC for die, and below 150^oC for plastic packages. See Application Information section for safe operating area information.
4. The non-inverting input of unused amplifiers must be connected to GND.

Electrical Specifications

V_{SUPPLY} = ±5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤10pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (V_{IO})		A	25	-	0.8	3	mV
		A	Full	-	-	5	mV
Delta V_{IO} Between Channels		A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift		B	Full	-	5	-	µV/^oC
V_{IO} Common Mode Rejection Ratio	V_{CM} = ±2.5V (Note 5)	A	25	53	-	-	dB
		A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio	±3.5V ≤ V_S ≤ ±6.5V	A	25	60	-	-	dB
		A	Full	55	-	-	dB
Input Common Mode Range	V_{CM} = ±2.5V (Note 5)	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current		A	25	-	3	8	µA
		A	Full	-	-	20	µA
+IN Common Mode Rejection ($+I_{BCMR} = \frac{1}{+R_{IN}}$)	V_{CM} = ±2.5V (Note 5)	A	25	-	-	0.15	µA/V
		A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection	±3.5V ≤ V_S ≤ ±6.5V	A	25	-	-	0.1	µA/V
		A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current		A	25, 85	-	4	12	µA
		A	-40	-	10	30	µA
Delta - IN BIAS Current Between Channels		A	25, 85	-	6	15	µA
		A	-40	-	10	30	µA
-IN Common Mode Rejection	V_{CM} = ±2.5V (Note 5)	A	25	-	-	0.4	µA/V
		A	Full	-	-	1.0	µA/V

Electrical Specifications V_{SUPPLY} = ±5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
-IN Power Supply Rejection	±3.5V ≤ V_S ≤ ±6.5V	A	25	-	-	0.2	µA/V
		A	Full	-	-	0.5	µA/V
Input Noise Voltage	f = 1kHz	B	25	-	4.5	-	nV/√Hz
+Input Noise Current	f = 1kHz	B	25	-	2.5	-	pA/√Hz
-Input Noise Current	f = 1kHz	B	25	-	25.0	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Transimpedence	V_{OUT} = ±2.5V (Note 11)	A	25	1.0	-	-	MΩ
		A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain	R_L = 400Ω, V_{OUT} = ±2.5V	A	25	70	-	-	dB
		A	Full	65	-	-	dB
Open Loop DC Voltage Gain	R_L = 100Ω, V_{OUT} = ±2.5V	A	25	50	-	-	dB
		A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing	R_L = 150Ω	A	25	±2.5	±3.0	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	R_L = 150Ω	B	Full	±16.6	±20.0	-	mA
Short Circuit Output Current	V_{IN} = ±2.5V, V_{OUT} = 0V	A	Full	±40	±60	-	mA
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		A	25	5	-	15	V
Quiescent Supply Current		A	Full	-	7.5	10	mA/Op Amp
AC CHARACTERISTICS A_V = +1							
Slew Rate	Note 6	B	25	275	350	-	V/µs
Full Power Bandwidth (Note 7)		B	25	22	28	-	MHz
Rise Time (Note 8)	V_{OUT} = 1V, R_L = 100Ω	B	25	-	6	-	ns
Fall Time (Note 8)	V_{OUT} = 1V, R_L = 100Ω	B	25	-	6	-	ns
Propagation Delay (Note 8)	V_{OUT} = 1V, R_L = 100Ω	B	25	-	6	-	ns
Overshoot		B	25	-	4.5	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	125	-	MHz
Settling Time	To 1%, 2V Output Step	B	25	-	50	-	ns
Settling Time	To 0.25%, 2V Output Step	B	25	-	75	-	ns
AC CHARACTERISTICS A_V = +2, R_F = 681Ω							
Slew Rate	Note 6	B	25	-	475	-	V/µs
Full Power Bandwidth (Note 7)		B	25	-	26	-	MHz
Rise Time (Note 8)	V_{OUT} = 1V, R_L = 100Ω	B	25	-	6	-	ns
Fall Time (Note 8)	V_{OUT} = 1V, R_L = 100Ω	B	25	-	6	-	ns

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Propagation Delay (Note 8)	V_{OUT} = 1V, R_L = 100Ω	B	25	-	6	-	ns
Overshoot		B	25	-	12	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	95	-	MHz
Settling Time	To 1%, 2V Output Step	B	25	-	50	-	ns
Settling Time	To 0.25%, 2V Output Step	B	25	-	100	-	ns
Gain Flatness	5MHz	B	25	-	0.02	-	dB
	20MHz	B	25	-	0.07	-	dB
AC CHARACTERISTICS A_V = +10, R_F = 383Ω							
Slew Rate	Note 6	B	25	350	475	-	V/µs
Full Power Bandwidth (Note 7)		B	25	28	38	-	MHz
Rise Time (Note 8)	V_{OUT} = 1V, R_L = 100Ω	B	25	-	8	-	ns
Fall Time (Note 8)	V_{OUT} = 1V, R_L = 100Ω	B	25	-	9	-	ns
Propagation Delay (Note 8)	V_{OUT} = 1V, R_L = 100Ω	B	25	-	9	-	ns
Overshoot		B	25	-	1.8	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	65	-	MHz
Settling Time	To 1%, 2V Output Step	B	25	-	75	-	ns
	To 0.1%, 2V Output Step	B	25	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain	R_L = 150Ω, (Note 10)	B	25	-	0.03	-	%
Differential Phase	R_L = 150Ω, (Note 10)	B	25	-	0.03	-	Degrees

NOTES:

5. At -40°C Product is tested at $V_{CM} = \pm2.25V$ because Short Test Duration does not allow self heating.
6. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
7. FPBW = $\frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; V_{PEAK} = 2V.
8. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
9. A. Production Tested; B. Typical or Guaranteed Limit based on characterization; C. Design Typical for information only.
10. Measured with a VM700A video tester using an NTC-7 composite VITS.
11. At -40°C Product is tested at $V_{OUT} = \pm2.25V$ because Short Test Duration does not allow self heating.

Test Circuits and Waveforms

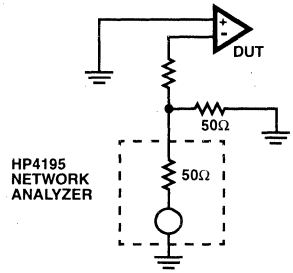


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

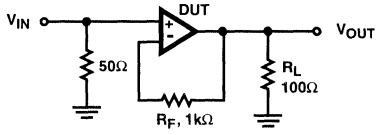


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

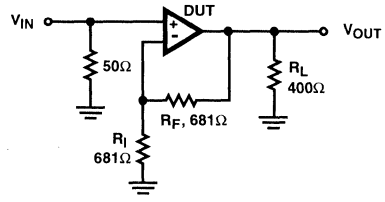
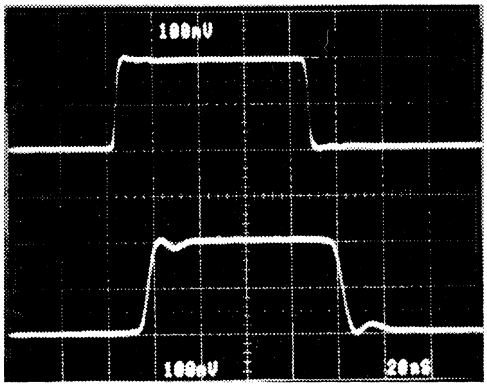
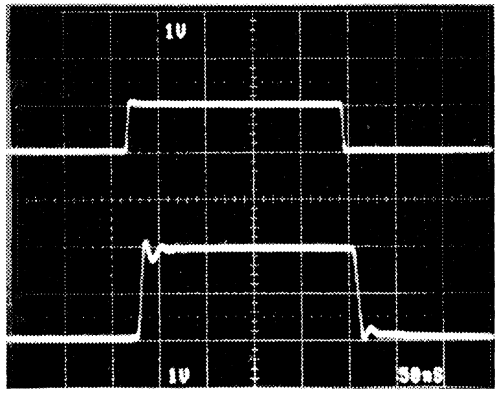


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

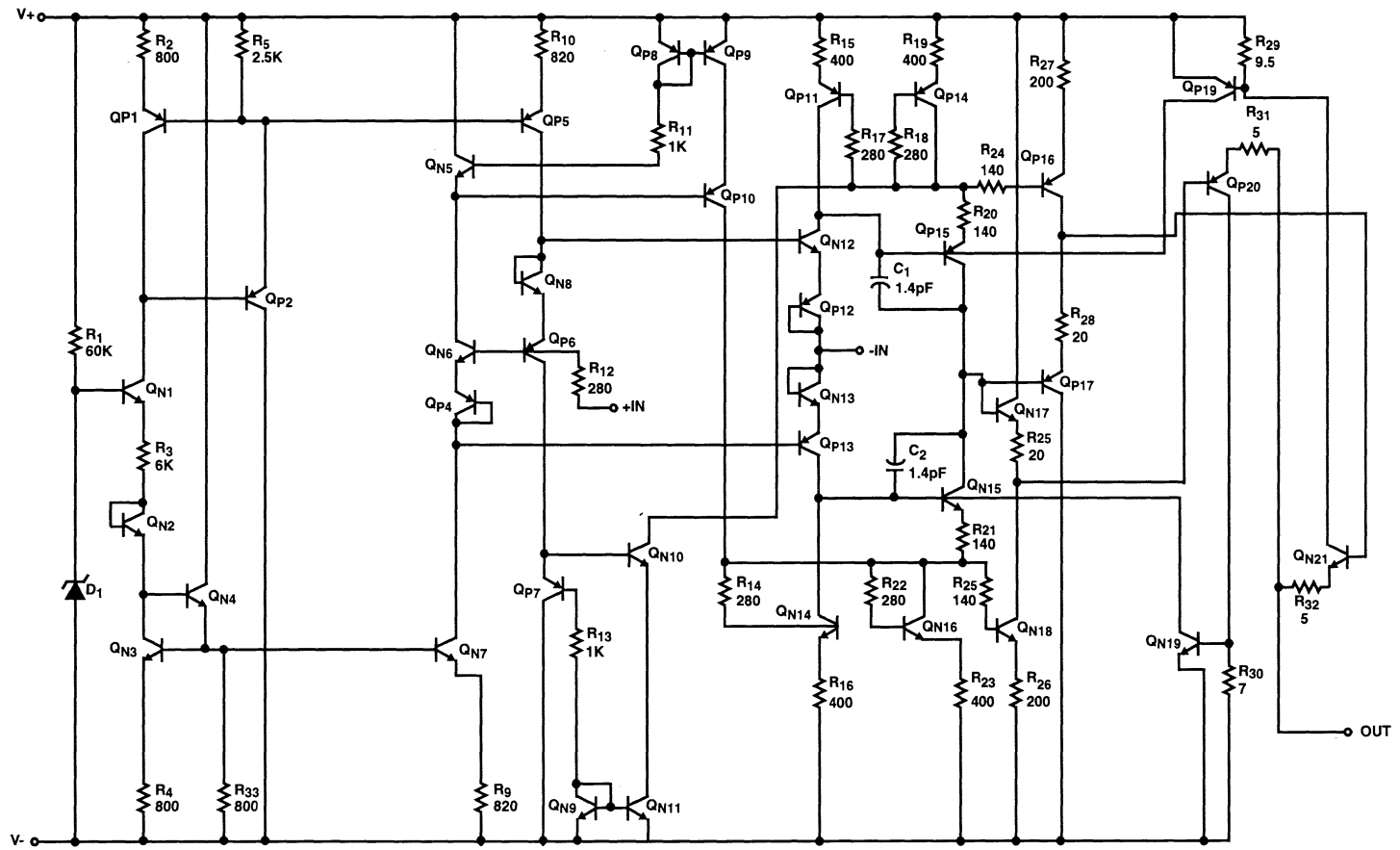
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic (One Amplifier of Three)



Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 8 and Figure 9 in the typical performance section, illustrate the performance of the HA5013 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5013 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10μF) tantalum or electrolytic capacitor in parallel with a small value (0.1μF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

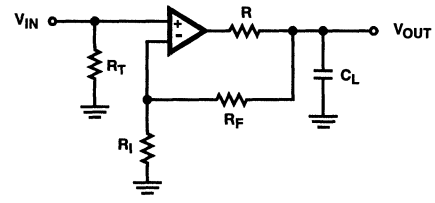


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in triple amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (PDIP, SOIC). At $V_S = \pm 5V$ quiescent operation both package styles may be operated over the full industrial range of -40°C to 85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

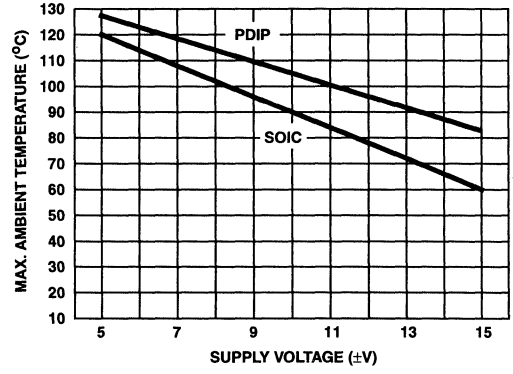


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Typical Performance Curves

$V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

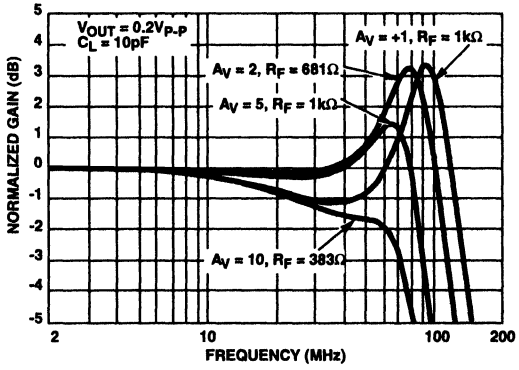


FIGURE 8. NON-INVERTING FREQUENCY RESPONSE

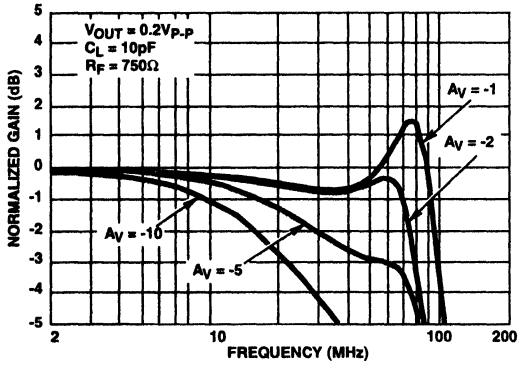


FIGURE 9. INVERTING FREQUENCY RESPONSE

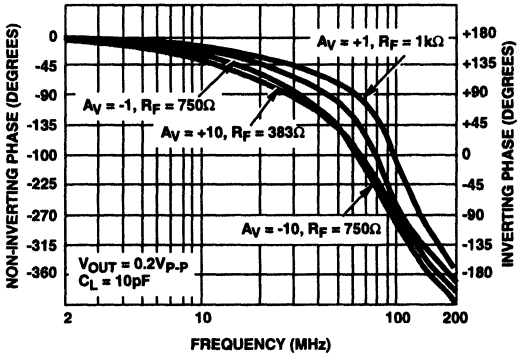


FIGURE 10. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

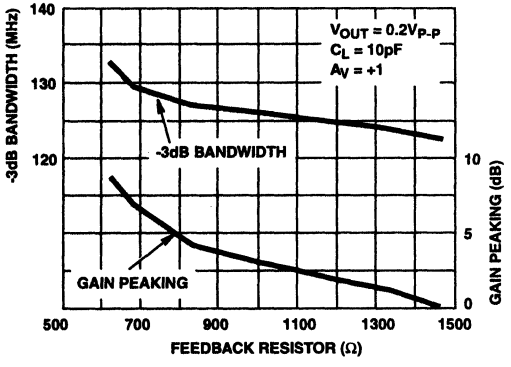


FIGURE 11. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

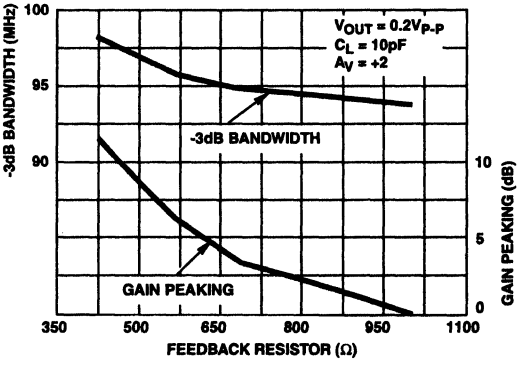


FIGURE 12. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

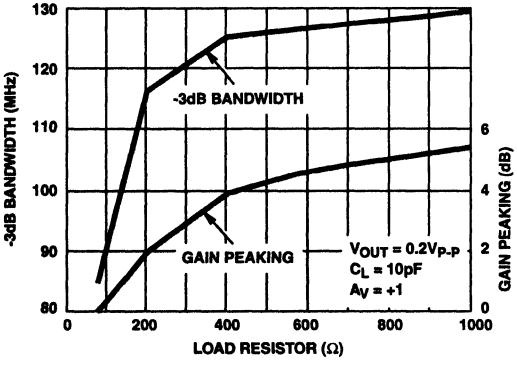


FIGURE 13. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

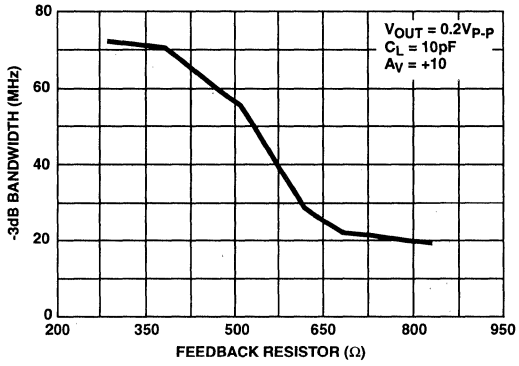


FIGURE 14. BANDWIDTH vs FEEDBACK RESISTANCE

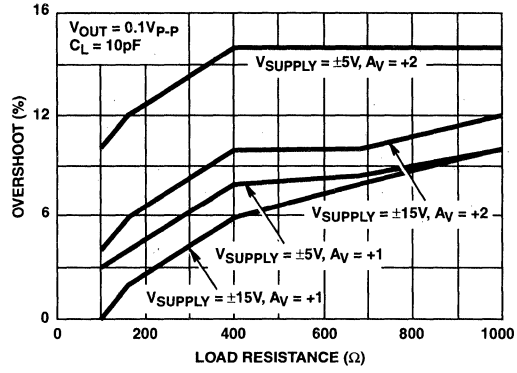


FIGURE 15. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

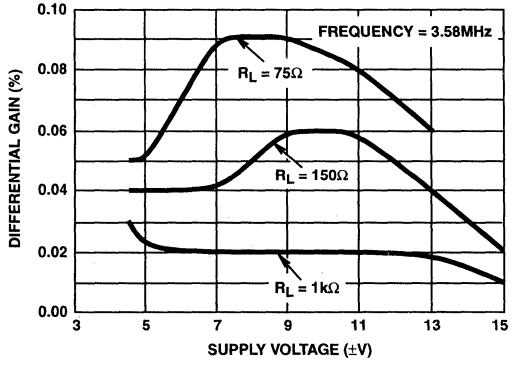


FIGURE 16. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

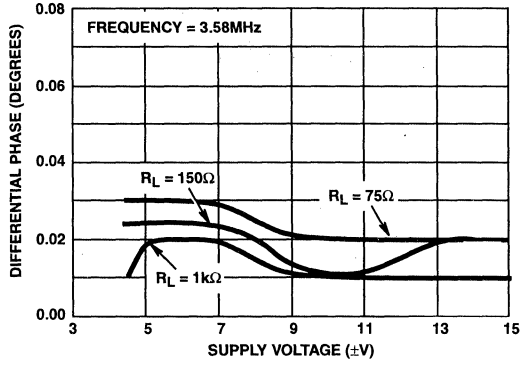


FIGURE 17. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

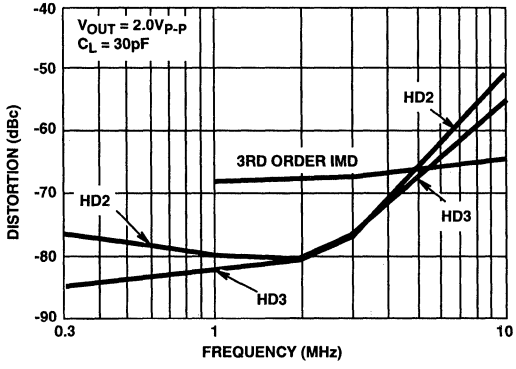


FIGURE 18. DISTORTION vs FREQUENCY

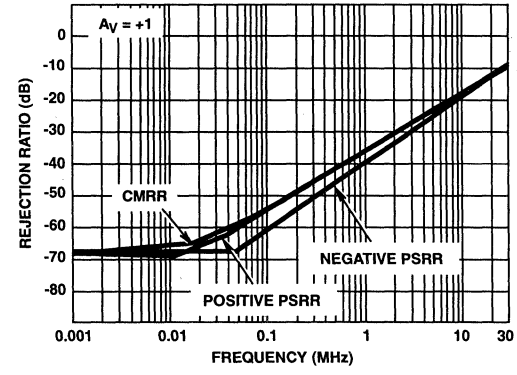


FIGURE 19. REJECTION RATIOS vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

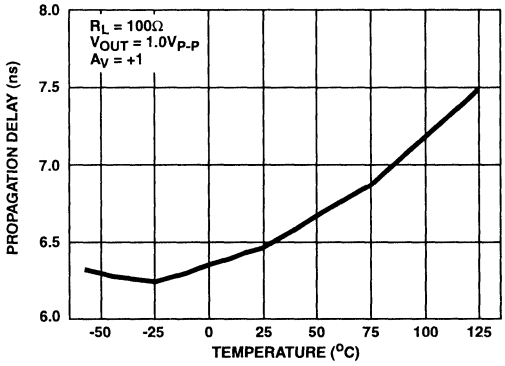


FIGURE 20. PROPAGATION DELAY vs TEMPERATURE

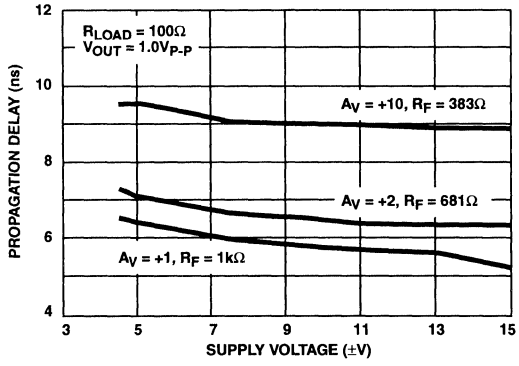


FIGURE 21. PROPAGATION DELAY vs SUPPLY VOLTAGE

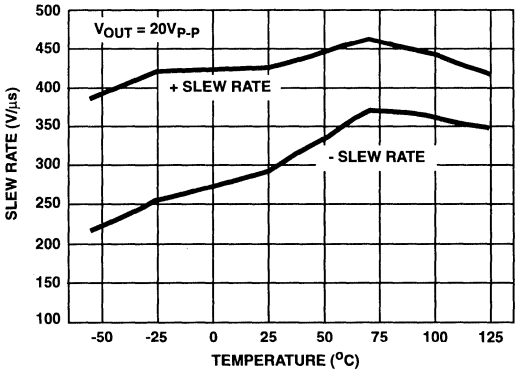


FIGURE 22. SLEW RATE vs TEMPERATURE

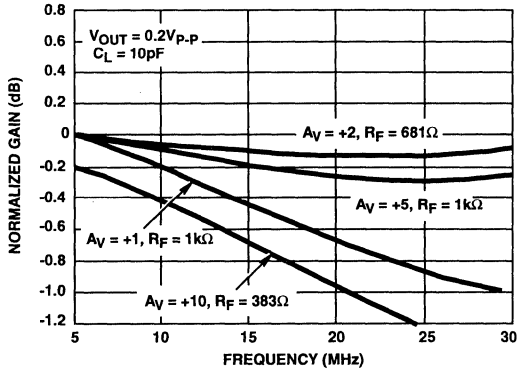


FIGURE 23. NON-INVERTING GAIN FLATNESS vs FREQUENCY

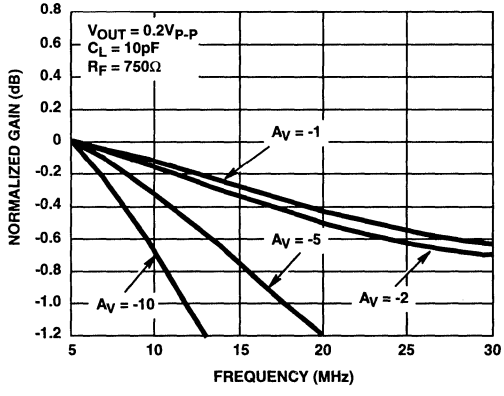


FIGURE 24. INVERTING GAIN FLATNESS vs FREQUENCY

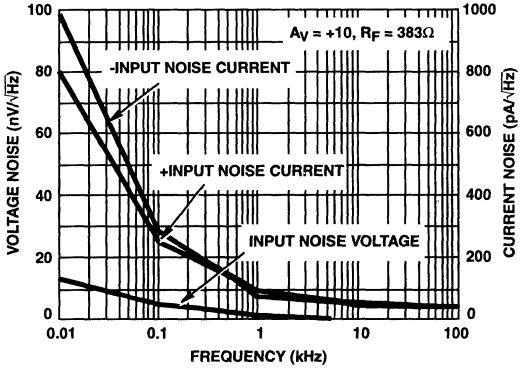


FIGURE 25. INPUT NOISE CHARACTERISTICS

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

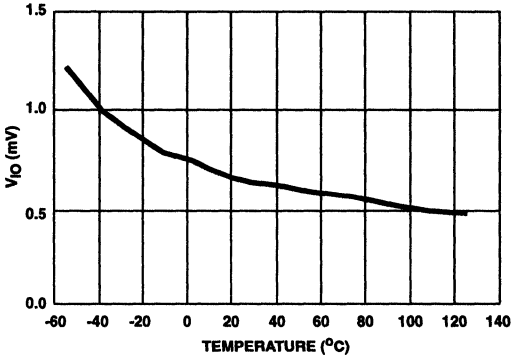


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE

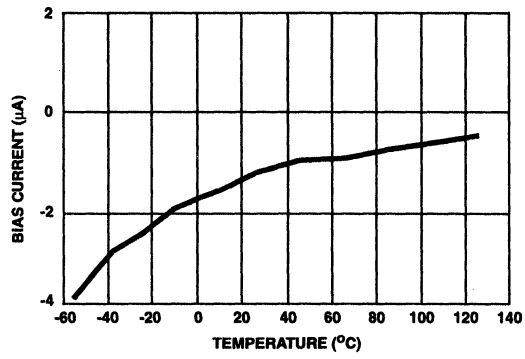


FIGURE 27. +INPUT BIAS CURRENT vs TEMPERATURE

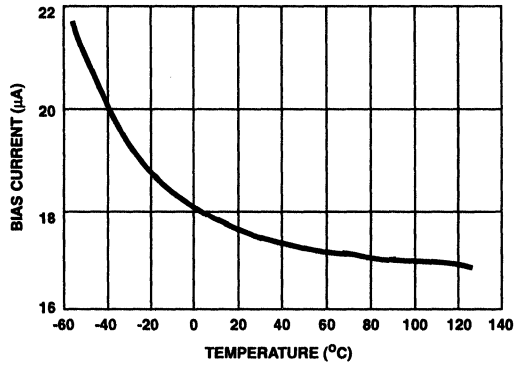


FIGURE 28. -INPUT BIAS CURRENT vs TEMPERATURE

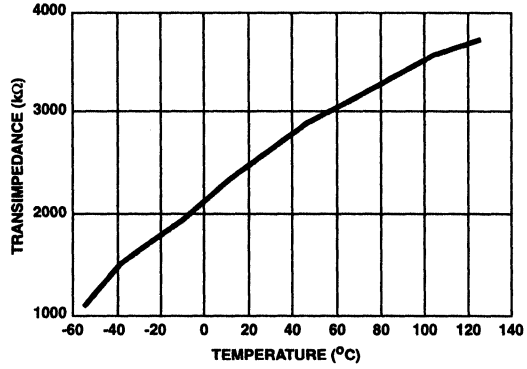


FIGURE 29. TRANSIMPEDANCE vs TEMPERATURE

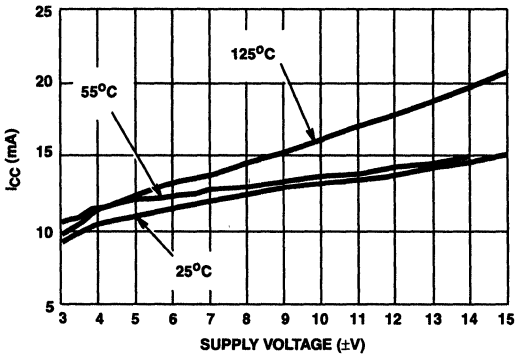


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

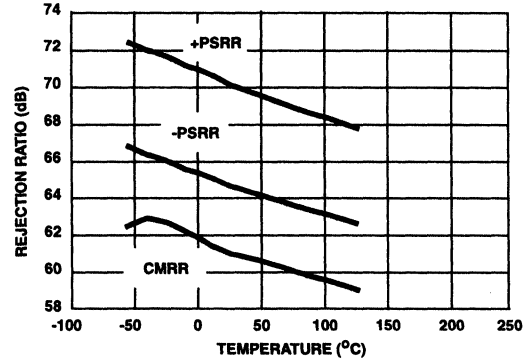


FIGURE 31. REJECTION RATIO vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

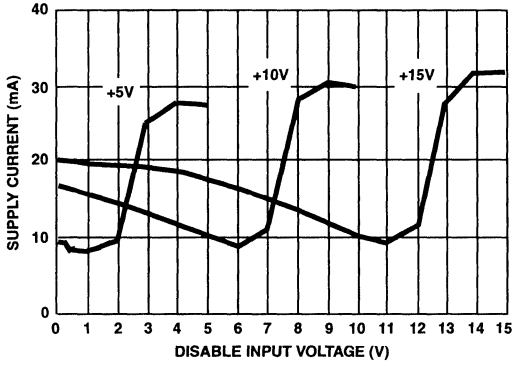


FIGURE 32. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

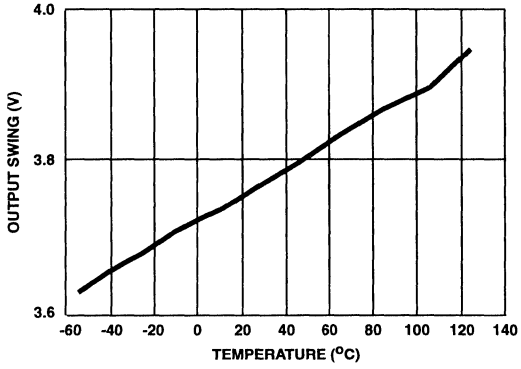


FIGURE 33. OUTPUT SWING vs TEMPERATURE

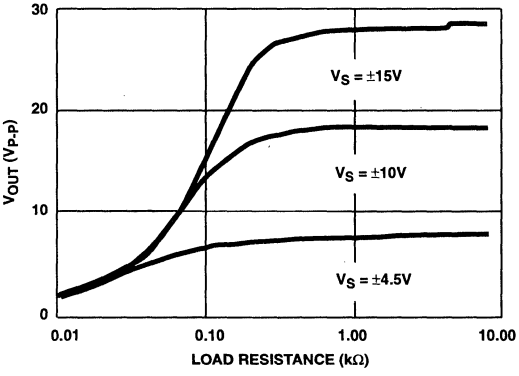


FIGURE 34. OUTPUT SWING vs LOAD RESISTANCE

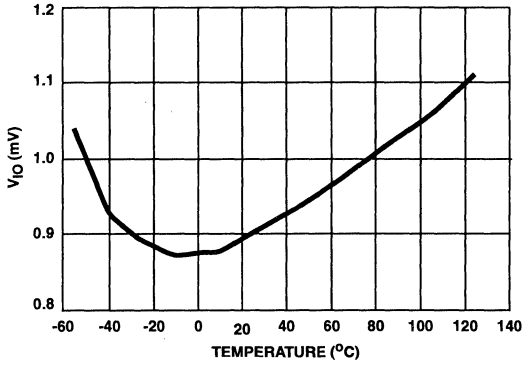


FIGURE 35. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

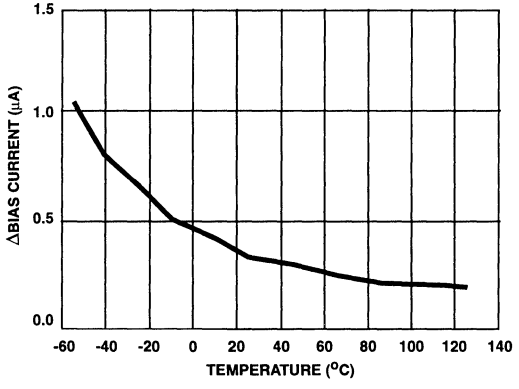


FIGURE 36. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

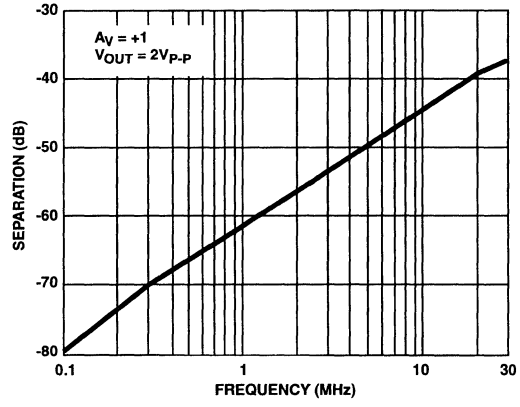


FIGURE 37. CHANNEL SEPARATION vs FREQUENCY

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

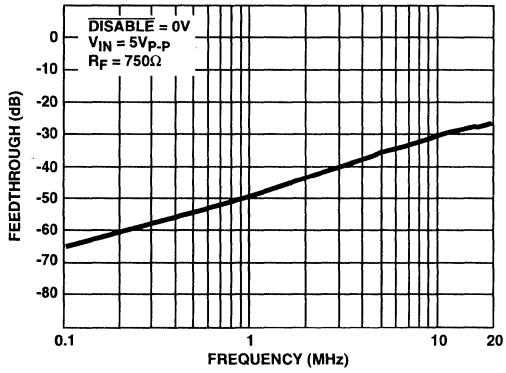


FIGURE 38. DISABLE FEEDTHROUGH vs FREQUENCY

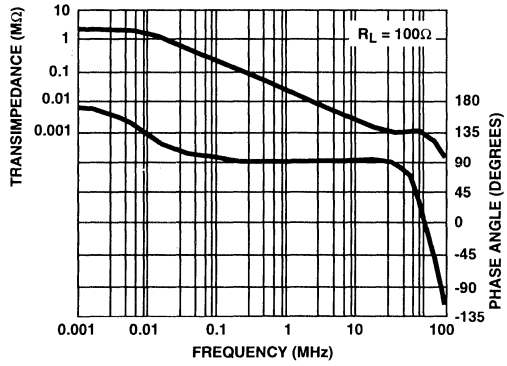


FIGURE 39. TRANSIMPEDANCE vs FREQUENCY

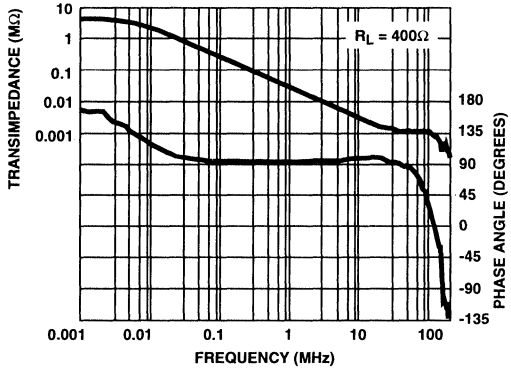


FIGURE 40. TRANSIMPEDENCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

2010µm x 3130µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL

Unbiased

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.4kÅ

TRANSISTOR COUNT:

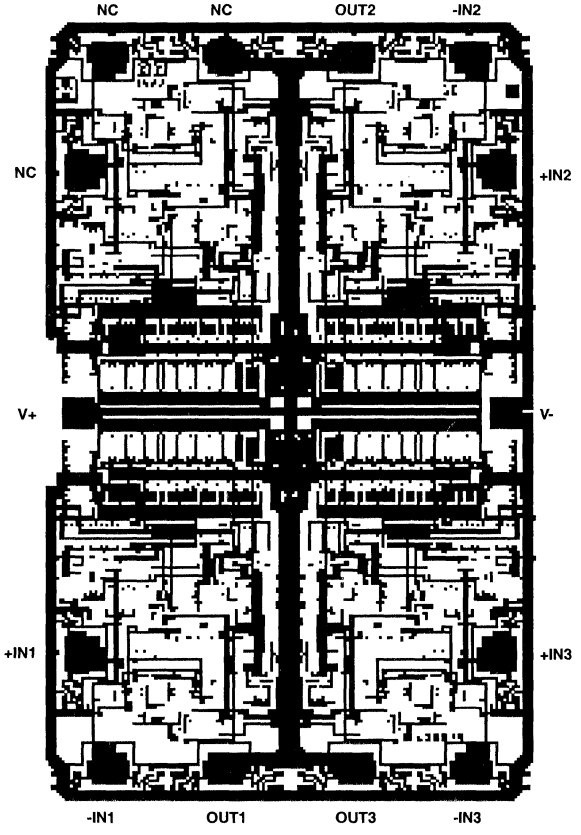
248

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA5013



HARRIS SEMICONDUCTOR

HA-5020

100MHz Current Feedback Video Amplifier With Disable

November 1996

Features

- Wide Unity Gain Bandwidth 100MHz
- Slew Rate 800V/μs
- Output Current ..... ±30mA (Min)
- Drives 3.5V into 75Ω
- Differential Gain 0.03%
- Differential Phase ..... 0.03 Degrees
- Low Input Voltage Noise ..... 4.5nV/√Hz
- Low Supply Current ..... 10mA (Max)
- Wide Supply Range ..... ±5V to ±15V
- Output Enable/Disable
- High Performance Replacement for EL2020

Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- Video Distribution Amp/Coax Cable Driver
- Flash A/D Driver
- Waveform Generator Output Driver
- Current to Voltage Converter; D/A Output Buffer
- Radar Systems
- Imaging Systems

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3-5020-5	0 to 75	8 Ld PDIP	E8.3
HA7-5020-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P5020-5 (H50205)	0 to 75	8 Ld SOIC	M8.15
HA3-5020-9	-40 to 85	8 Ld PDIP	E8.3
HA7-5020-9	-40 to 85	8 Ld CERDIP	F8.3A

Description

The HA-5020 is a wide bandwidth, high slew rate amplifier optimized for video applications and gains between 1 and 10. Manufactured on Harris' Reduced Feature Complementary Bipolar DI process, this amplifier uses current mode feedback to maintain higher bandwidth at a given gain than conventional voltage feedback amplifiers. Since it is a closed loop device, the HA-5020 offers better gain accuracy and lower distortion than open loop buffers.

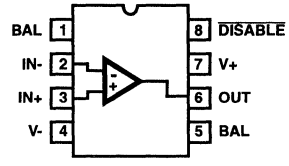
The HA-5020 features low differential gain and phase and will drive two double terminated 75Ω coax cables to video levels with low distortion. Adding a gain flatness performance of 0.1dB makes this amplifier ideal for demanding video applications. The bandwidth and slew rate of the HA-5020 are relatively independent of closed loop gain. The 100MHz unity gain bandwidth only decreases to 60MHz at a gain of 10. The HA-5020 used in place of a conventional op amp will yield a significant improvement in the speed power product. To further reduce power, the HA-5020 has a disable function which significantly reduces supply current, while forcing the output to a true high impedance state. This allows the outputs of multiple amplifiers to be wire-OR'd into multiplexer configurations. The device also includes output short circuit protection and output offset voltage adjustment.

The HA-5020 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" section below for more information. For military grade product, please refer to the HA-5020/883 datasheet.

For multi channel versions of the HA-5020 see the HA5022 dual with disable, HA5023 dual, HA5013 triple, HA5024 quad with disable or HA5025 quad op amp data sheets.

Pinout

HA-5020
(PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **2845.7**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 36V
DC Input Voltage . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage. 10V
Output Current . . . . . Short Circuit Protected

Operating Conditions

Temperature Range
HA-5020-5 . . . . . 0°C to 75°C
HA-5020-9 . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	130	N/A
CERDIP Package	135	50
SOIC Package	170	N/A

Maximum Junction Temperature (Ceramic Package, Note 1) . . . 175°C
Maximum Junction Temperature (Plastic Packages, Note 1) . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175°C for ceramic packages, and below 150°C for plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm 15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5020-5, -9			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Input Offset Voltage (Notes 3, 14)		25	-	2	8	mV
		Full	-	-	10	mV
Average Input Offset Voltage Drift		Full	-	10	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Note 14)	$V_{CM} = \pm 10V$	25	60	-	-	dB
		Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 14)	$\pm 4.5V \leq V_S \leq \pm 18V$	25	64	-	-	dB
		Full	60	-	-	dB
Non-Inverting Input (+IN) Current (Note 14)		25	-	3	8	µA
		Full	-	-	20	µA
+IN Common Mode Rejection	$V_{CM} = \pm 10V$	25	-	-	0.1	µA/V
		Full	-	-	0.5	µA/V
+IN Power Supply Rejection	$4.5V \leq V_S \leq \pm 18V$	25	-	-	0.06	µA/V
		Full	-	-	0.2	µA/V
Inverting Input (-IN) Current (Note 14)		25	-	12	20	µA
		Full	-	25	50	µA
-IN Common Mode Rejection	$V_{CM} = \pm 10V$	25	-	-	0.4	µA/V
		Full	-	-	0.5	µA/V
-IN Power Supply Rejection	$4.5V \leq V_S \leq \pm 18V$	25	-	-	0.2	µA/V
		Full	-	-	0.5	µA/V
TRANSFER CHARACTERISTICS						
Transimpedance (Notes 9, 14)		25	3500	-	-	V/mA
		Full	1000	-	-	V/mA
Open Loop DC Voltage Gain (Note 9)	$R_L = 400\Omega$, $V_{OUT} = \pm 10V$	25	70	-	-	dB
		Full	65	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	25	60	-	-	dB
		Full	55	-	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 14)	$R_L = 150\Omega$	25 to 85	±12	±12.7	-	V
		-40 to 0	±11	±11.8	-	V

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5020-5, -9			UNITS
			MIN	TYP	MAX	
Output Current		25	±30	±31.7	-	mA
(Guaranteed by Output Voltage Test)		Full	±27.5	-	-	mA
POWER SUPPLY CHARACTERISTICS						
Quiescent Supply Current (Note 14)		Full	-	7.5	10	mA
Supply Current, Disabled (Note 14)	$\overline{DISABLE}$ = 0V	Full	-	5	7.5	mA
$\overline{Disable}$ Pin Input Current	$\overline{DISABLE}$ = 0V	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 4)		Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 5)		Full	-	-	20	µA
AC CHARACTERISTICS ($A_V = +1$)						
Slew Rate (Note 6)		25	600	800	-	V/µs
		Full	500	700	-	V/µs
Full Power Bandwidth (Note 7) (Guaranteed by Slew Rate Test)		25	9.6	12.7	-	MHz
		Full	8.0	11.1	-	MHz
Rise Time (Note 8)		25	-	5	-	ns
Fall Time (Note 8)		25	-	5	-	ns
Propagation Delay (Notes 8, 14)		25	-	6	-	ns
-3dB Bandwidth (Note 14)	V_{OUT} = 100mV	25	-	100	-	MHz
Settling Time to 1%	10V Output Step	25	-	45	-	ns
Settling Time to 0.25%	10V Output Step	25	-	100	-	ns
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)						
Slew Rate (Notes 6, 9)		25	900	1100	-	V/µs
		Full	700	-	-	V/µs
Full Power Bandwidth (Note 7) (Guaranteed by Slew Rate Test)		25	14.3	17.5	-	MHz
		Full	11.1	-	-	MHz
Rise Time (Note 8)		25	-	8	-	ns
Fall Time (Note 8)		25	-	8	-	ns
Propagation Delay (Notes 8, 14)		25	-	9	-	ns
-3dB Bandwidth	V_{OUT} = 100mV	25	-	60	-	MHz
Settling Time to 1%	10V Output Step	25	-	55	-	ns
Settling Time to 0.1%	10V Output Step	25	-	90	-	ns
HARRIS VALUE ADDED SPECIFICATIONS						
Input Noise Voltage (Note 14)	f = 1kHz	25	-	4.5	-	nV/√Hz
+Input Noise Current (Note 14)	f = 1kHz	25	-	2.5	-	pA/√Hz
-Input Noise Current (Note 14)	f = 1kHz	25	-	25	-	pA/√Hz
Input Common Mode Range		Full	±10	±12	-	V
$-I_{BIAS}$ Adjust Range (Note 3)		Full	±25	±40	-	µA
Overshoot (Note 14)		25	-	7	-	%
Output Current, Short Circuit (Note 14)	$V_{IN} = \pm10V$, $V_{OUT} = 0V$	Full	±50	±65	-	mA
Output Current, Disabled (Note 14)	$\overline{DISABLE}$ = 0V, $V_{OUT} = \pm10V$	Full	-	-	1	µA
Output Disable Time (Notes 10, 14)		25	-	10	-	µs
Output Enable Time (Notes 11, 14)		25	-	200	-	ns
Supply Voltage Range		25	±5	-	±15	V
Output Capacitance, Disabled (Note 12)	$\overline{DISABLE}$ = 0V	25	-	6	-	pF

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5020-5, -9			UNITS
			MIN	TYP	MAX	
VIDEO CHARACTERISTICS						
Differential Gain (Notes 13, 14)	$R_L = 150\Omega$	25	-	0.03	-	%
Differential Phase (Notes 18, 20, 21)	$R_L = 150\Omega$	25	-	0.03	-	Degrees
Gain Flatness	To 5MHz	25	-	0.1	-	dB

Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation.

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5020-5, -9			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Input Offset Voltage (Notes 3, 14)		25	-	2	8	mV
		Full	-	-	10	mV
Average Input Offset Voltage Drift		Full	-	10	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Notes 14, 15)		25	50	-	-	dB
		Full	35	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 14)	$\pm3.5V \leq V_S \leq \pm6.5V$	25	55	-	-	dB
		Full	50	-	-	dB
Non-Inverting Input (+IN) Current (Note 14)		25	-	3	8	µA
		Full	-	-	20	µA
+IN Common Mode Rejection (Note 15)		25	-	-	0.1	µA/V
		Full	-	-	0.5	µA/V
+IN Power Supply Rejection	$\pm3.5V \leq V_S \leq \pm6.5V$	25	-	-	0.06	µA/V
		Full	-	-	0.2	µA/V
Inverting Input (-IN) Current (Note 14)		25	-	12	20	µA
		Full	-	25	50	µA
-IN Common Mode Rejection (Note 15)		25	-	-	0.4	µA/V
		Full	-	-	0.5	µA/V
-IN Power Supply Rejection	$\pm3.5V \leq V_S \leq \pm6.5V$	25	-	-	0.2	µA/V
		Full	-	-	0.5	µA/V
TRANSFER CHARACTERISTICS						
Transimpedance (Notes 9, 14)		25	1000	-	-	V/mA
		Full	850	-	-	V/mA
Open Loop DC Voltage Gain	$R_L = 400\Omega$, $V_{OUT} = \pm2.5V$	25	65	-	-	dB
		Full	60	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm2.5V$	25	50	-	-	dB
		Full	45	-	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 14)		25 to 85	±2.5	±3.0	-	V
		-40 to 0	±2.5	±3.0	-	V

Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5020-5, -9			UNITS
			MIN	TYP	MAX	
Output Current (Guaranteed by Output Voltage Test)	$R_L = 100\Omega$	25	±16.6	±20	-	mA
		Full	±16.6	±20	-	mA
POWER SUPPLY CHARACTERISTICS						
Quiescent Supply Current (Note 14)		Full	-	7.5	10	mA
Supply Current, Disabled (Note 14)	$\overline{DISABLE} = 0V$	Full	-	5	7.5	mA
$\overline{Disable}$ Pin Input Current	$\overline{DISABLE} = 0V$	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 16)		Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 5)		Full	-	-	20	µA
AC CHARACTERISTICS ($A_V = +1$)						
Slew Rate (Note 17)		25	215	400	-	V/µs
Full Power Bandwidth (Note 18)		25	22	28	-	MHz
Rise Time (Note 8)		25	-	6	-	ns
Fall Time (Note 8)		25	-	6	-	ns
Propagation Delay (Note 8)		25	-	6	-	ns
Overshoot		25	-	4.5	-	%
-3dB Bandwidth (Note 14)	$V_{OUT} = 100mV$	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	25	-	75	-	ns
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)						
Slew Rate (Note 17)		25	-	475	-	V/µs
Full Power Bandwidth (Note 18)		25	-	26	-	MHz
Rise Time (Note 8)		25	-	6	-	ns
Fall Time (Note 8)		25	-	6	-	ns
Propagation Delay (Note 8)		25	-	6	-	ns
Overshoot		25	-	12	-	%
-3dB Bandwidth (Note 14)	$V_{OUT} = 100mV$	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	25	-	100	-	ns
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)						
Slew Rate (Note 17)		25	350	475	-	V/µs
Full Power Bandwidth (Note 18)		25	28	38	-	MHz
Rise Time (Note 8)		25	-	8	-	ns
Fall Time (Note 8)		25	-	9	-	ns
Propagation Delay (Note 8)		25	-	9	-	ns
Overshoot		25	-	1.8	-	%
-3dB Bandwidth (Note 14)	$V_{OUT} = 100mV$	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	25	-	75	-	ns

Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5020-5, -9			UNITS
			MIN	TYP	MAX	
Settling Time to 0.25%	2V Output Step	25	-	130	-	ns
HARRIS VALUE ADDED SPECIFICATIONS						
Input Noise Voltage (Note 14)	f = 1kHz	25	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 14)	f = 1kHz	25	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 14)	f = 1kHz	25	-	25	-	$pA/\sqrt{Hz}$
Input Common Mode Range		Full	±2.5V	–	-	V
Output Current, Short Circuit	$V_{IN} = \pm 2.5V$ $V_{OUT} = 0V$	Full	±40	±60	-	mA
Output Current, Disabled (Note 14)	$\overline{DISABLE} = 0V$, $V_{OUT} = \pm 2.5V$, $V_{IN} = 0V$	Full	-	-	2	µA
Output Disable Time (Notes 14, 20)		25	-	40	-	µs
Output Enable Time (Notes 14, 21)		25	-	40	-	ns
Supply Voltage Range		25	±5	-	±15	V
Output Capacitance, Disabled (Note 19)	$\overline{DISABLE} = 0V$	25	-	6	-	pF
VIDEO CHARACTERISTICS						
Differential Gain (Notes 13, 14)	$R_L = 150\Omega$	25	-	0.03	-	%
Differential Phase (Notes 13, 14)	$R_L = 150\Omega$	25	-	0.03	-	Degrees
Gain Flatness to 5MHz	To 5MHz	25	-	0.1	-	dB

NOTES:

3. Suggested V_{OS} Adjust Circuit: The inverting input current ($-I_{BIAS}$) can be adjusted with an external 10kΩ pot between pins 1 and 5, wiper connected to V+. Since $-I_{BIAS}$ flows through the feedback resistor (R_F), the result is an adjustment in offset voltage. The amount of offset voltage adjustment is determined by the value of R_F ($\Delta V_{OS} = \Delta -I_{BIAS} * R_F$).
4. $R_L = 100\Omega$, $V_{IN} = 10V$. This is the minimum current which must be pulled out of the $\overline{Disable}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
5. $V_{IN} = 0V$. This is the maximum current that can be pulled out of the $\overline{Disable}$ pin with the HA-5020 remaining enabled. The HA-5020 is considered disabled when the supply current has decreased by at least 0.5mA.
6. V_{OUT} switches from -10V to +10V, or from +10V to -10V. Specification is from the 25% to 75% points.
7. $FPBW = \frac{Slew\ Rate}{2\pi V_{PEAK}}$; $V_{PEAK} = 10V$.
8. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
9. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
10. $V_{IN} = +10V$, $\overline{Disable} = +15V$ to 0V. Measured from the 50% point of $\overline{Disable}$ to $V_{OUT} = 0V$.
11. $V_{IN} = +10V$, $\overline{Disable} = 0V$ to +15V. Measured from the 50% point of $\overline{Disable}$ to $V_{OUT} = 10V$.
12. $V_{IN} = 0V$, Force V_{OUT} from 0V to ±10V, $t_R = t_F = 50ns$.
13. Measured with a VM700A video tester using a NTC-7 composite VITS.
14. See "Typical Performance Curves" for more information.
15. $V_{CM} = \pm 2.5V$. At -40°C product is tested at $V_{CM} = \pm 2.25V$ because short test duration does not allow self heating.
16. $R_L = 100\Omega$. $V_{IN} = 2.5V$. This is the minimum current which must be pulled out of the $\overline{Disable}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
17. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
18. $FPBW = \frac{Slew\ Rate}{2\pi V_{PEAK}}$; $V_{PEAK} = 2V$.
19. $V_{IN} = 0V$, Force V_{OUT} from 0V to ±2.5V, $t_R = t_F = 50ns$.
20. $V_{IN} = +2V$, $\overline{Disable} = +5V$ to 0V. Measured from the 50% point of $\overline{Disable}$ to $V_{OUT} = 0V$.
21. $V_{IN} = +2V$, $\overline{Disable} = 0V$ to +5V. Measured from the 50% point of $\overline{Disable}$ to $V_{OUT} = 2V$.

Test Circuits and Waveforms

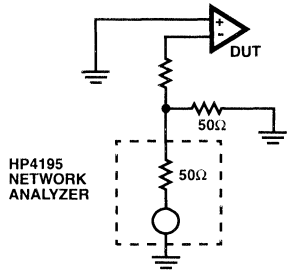


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

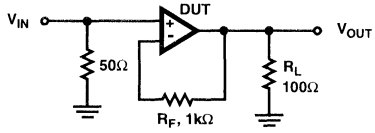


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

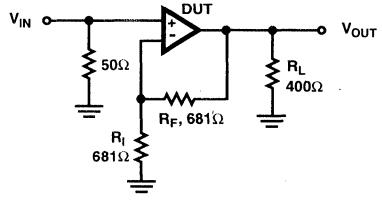
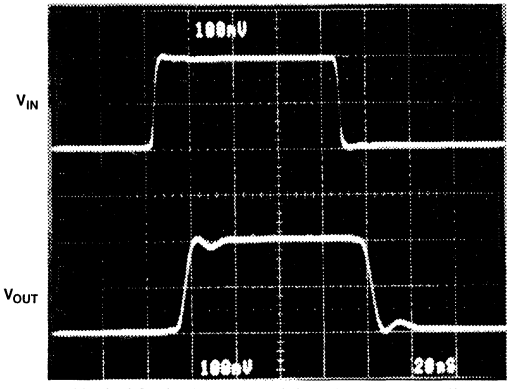
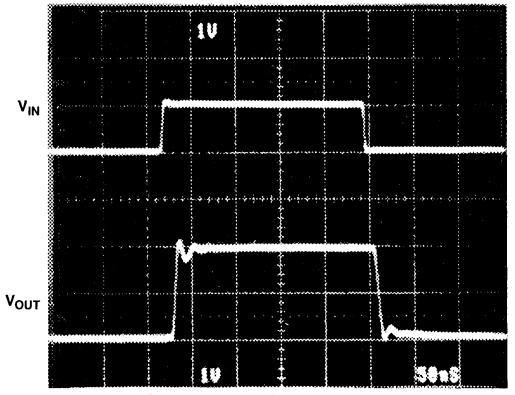


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

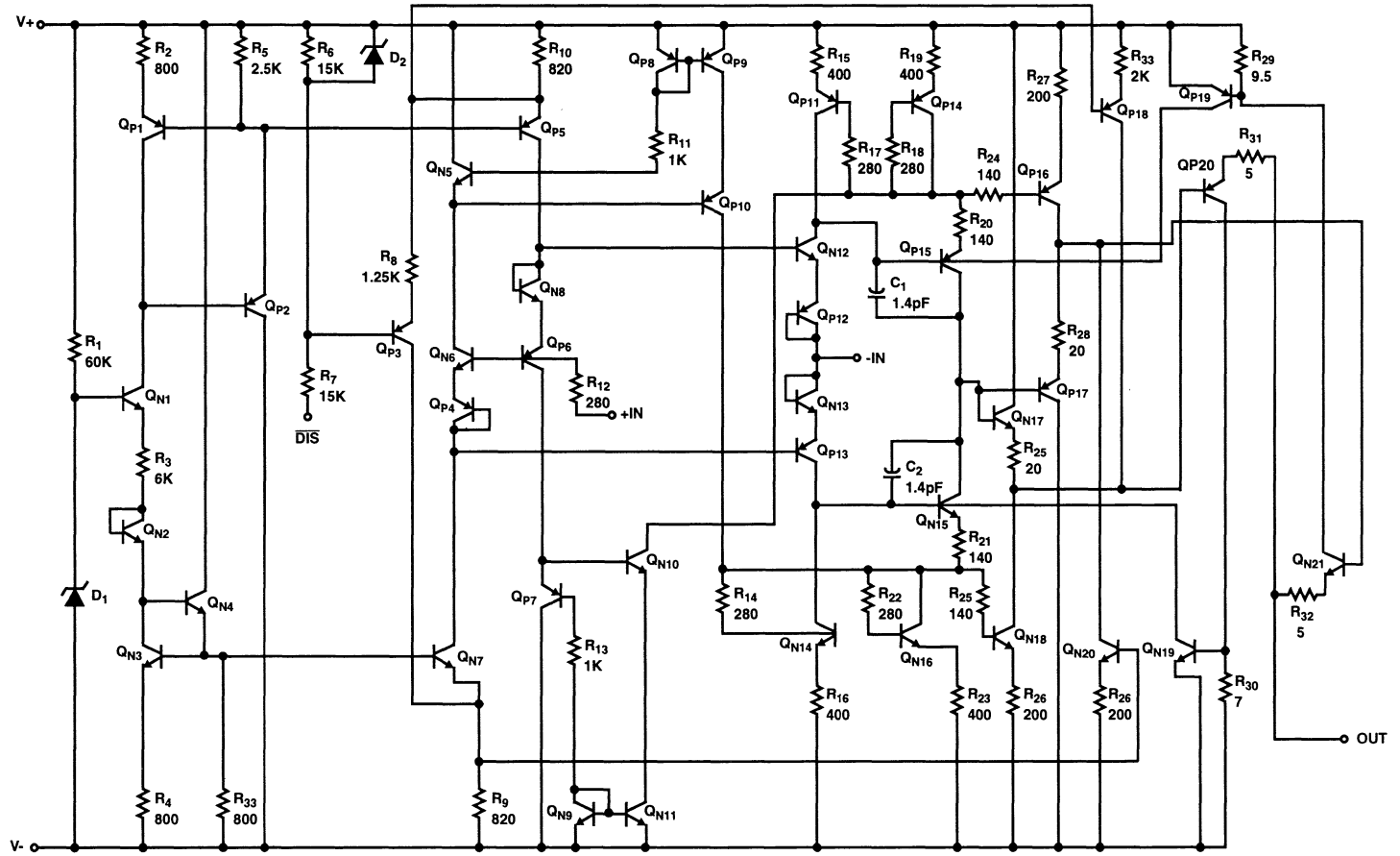
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic Diagram



Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response illustrate the performance of the HA-5020 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA-5020 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10μF) tantalum or electrolytic capacitor in parallel with a small value (0.1μF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

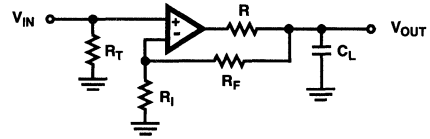


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Enable/Disable Function

When enabled the amplifier functions as a normal current feedback amplifier with all of the data in the electrical specifications table being valid and applicable. When disabled the amplifier output assumes a true high impedance state and the supply current is reduced significantly.

The circuit shown in Figure 7 is a simplified schematic of the enable/disable function. The large value resistors in series with the DISABLE pin makes it appear as a current source to the driver. When the driver pulls this pin low current flows out of the pin and into the driver. This current, which may be as large as 350μA when external circuit and process variables are at their extremes, is required to insure that point "A" achieves the proper potential to disable the output. The driver must have the compliance and capability of sinking all of this current.

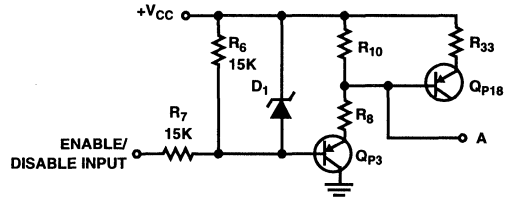


FIGURE 7. SIMPLIFIED SCHEMATIC OF ENABLE/DISABLE FUNCTION

When V_{CC} is +5V the DISABLE pin may be driven with a dedicated TTL gate. The maximum low level output voltage of the TTL gate, 0.4V, has enough compliance to insure that the amplifier will always be disabled even though D_1 will not turn on, and the TTL gate will sink enough current to keep point "A" at its proper voltage. When V_{CC} is greater than +5V the DISABLE pin should be driven with an open collector device that has a breakdown rating greater than V_{CC}.

Referring to Figure 7, it can be seen that R_6 will act as a pull-up resistor to $+V_{CC}$ if the DISABLE pin is left open. In those cases where the enable/disable function is not required on all circuits some circuits can be permanently enabled by letting the DISABLE pin float. If a driver is used to set the enable/disable level, be sure that the driver does not sink more than 20μA when the DISABLE pin is at a high level. TTL gates, especially CMOS versions, do not violate this criteria so it is permissible to control the enable/disable function with TTL.

Typical Applications

Two Channel Video Multiplexer

Referring to the amplifier U_{1A} in Figure 8, R_1 terminates the cable in its characteristic impedance of 75Ω, and R_4 back terminates the cable in its characteristic impedance. The amplifier is set up in a gain configuration of +2 to yield an overall network gain of +1 when driving a double terminated cable. The value of R_3 can be changed if a different network gain is desired. R_5 holds the disable pin at ground thus inhibiting the amplifier until the switch, S_1, is thrown to position 1. At position 1 the switch pulls the disable pin up to the plus supply rail thereby enabling the amplifier. Since all of the actual signal switching takes place within the amplifier, it's differential gain and phase parameters, which are 0.03% and 0.03 degrees respectively, determine the circuit's performance. The other circuit, U_{1B}, operates in a similar manner.

When the plus supply rail is 5V the disable pin can be driven by a dedicated TTL gate as discussed earlier. If a multiplexer IC or its equivalent is used to select channels its logic must be break before make. When these conditions are satisfied the HA-5020 is often used as a remote video multiplexer, and the multiplexer may be extended by adding more amplifier ICs.

Low Impedance Multiplexer

Two common problems surface when you try to multiplex multiple high speed signals into a low impedance source such as an A/D converter. The first problem is the low source impedance which tends to make amplifiers oscillate and causes gain errors. The second problem is the multiplexer which supplies no gain, introduces all kinds of distortion and limits the frequency response. Using op amps which have an enable/disable function, such as the HA-5020, eliminates the multiplexer problems because the external mux chip is not needed, and the HA-5020 can drive low impedance (large capacitance) loads if a series isolation resistor is used.

Referring to Figure 9, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications. Since the drivers usually are terminated in their characteristic impedance the input gain is 0.5, thus the amplifiers, U_2, are configured in a gain of +2 to set the circuit gain equal to one. Resistors R_2 and R_3 determine the amplifier gain, and if a different gain is desired R_2 should be changed according to the equation $G = (1 + R_3/R_2)$. R_3 sets the frequency response of the amplifier so you should refer to the manufacturers data sheet before changing its value. R_5, C_1 and D_1 are an asymmetrical charge/discharge time circuit which configures U_1 as a break before make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels the drive logic must be designed to be break before make. R_4 is enclosed in the feedback loop of the amplifier so that the large open loop amplifier gain of U_2 will present the load with a small closed loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown in Figure 9 was tested for the full range of capacitor values with no oscillations being observed; thus, problem one has been solved. The frequency and gain characteristics of the circuit are now those of the amplifier and independent of any multiplexing action; thus, problem two has been solved. The multiplexer transition time is approximately 15µs with the component values shown.

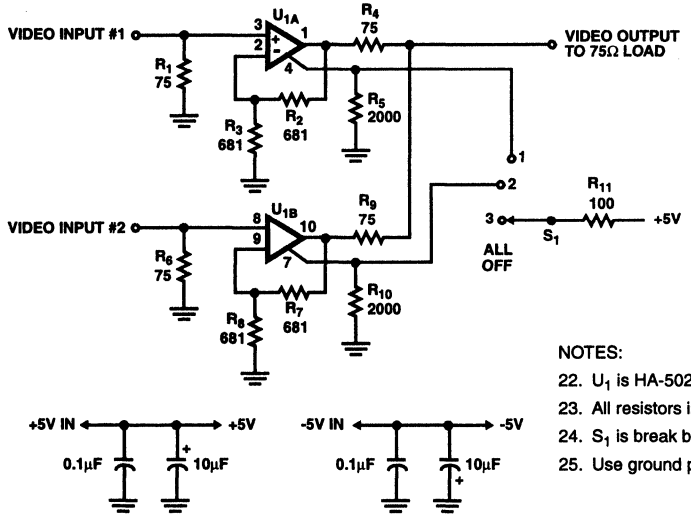
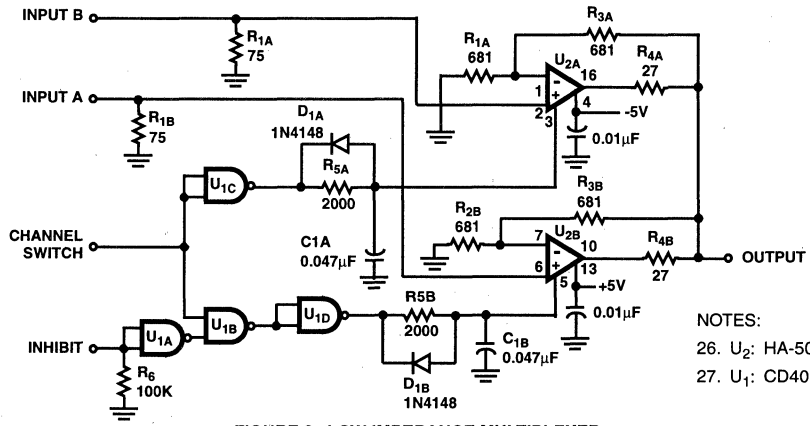


FIGURE 8. TWO CHANNEL HIGH IMPEDANCE MULTIPLEXER



NOTES:
26. U_2: HA-5020.
27. U_1: CD4011.

FIGURE 9. LOW IMPEDANCE MULTIPLEXER

Typical Performance Curves

$V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

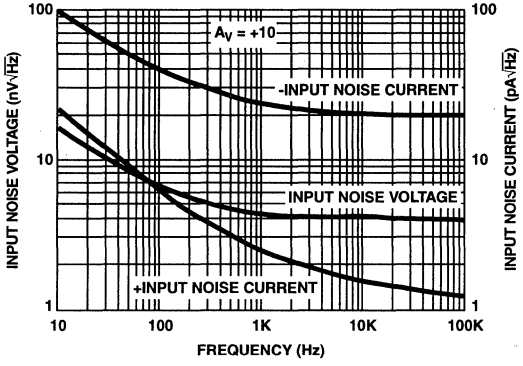


FIGURE 10. INPUT NOISE vs FREQUENCY (AVERAGE OF 18 UNITS FROM 3 LOTS)

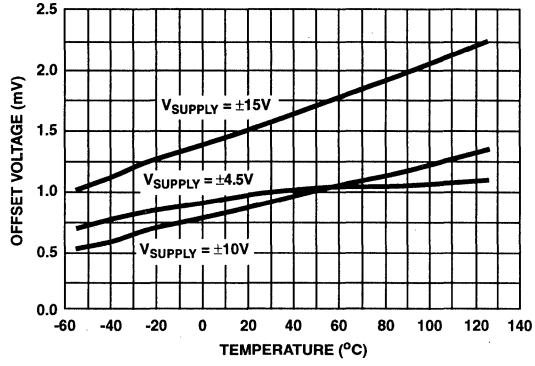


FIGURE 11. INPUT OFFSET VOLTAGE vs TEMPERATURE (ABSOLUTE VALUE AVERAGE OF 30 UNITS FROM 3 LOTS)

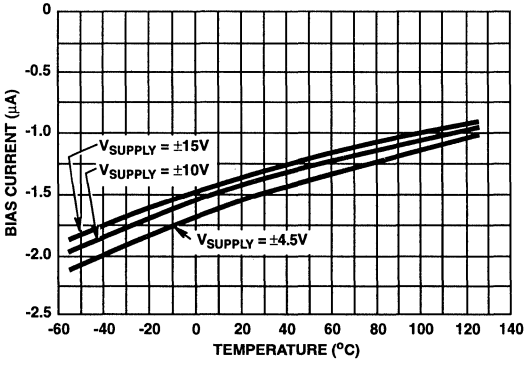


FIGURE 12. +INPUT BIAS CURRENT vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

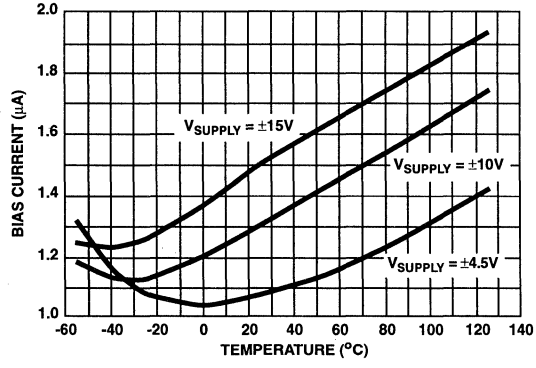


FIGURE 13. -INPUT BIAS CURRENT vs TEMPERATURE (ABSOLUTE VALUE AVERAGE OF 30 UNITS FROM 3 LOTS)

Typical Performance Curves

$V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

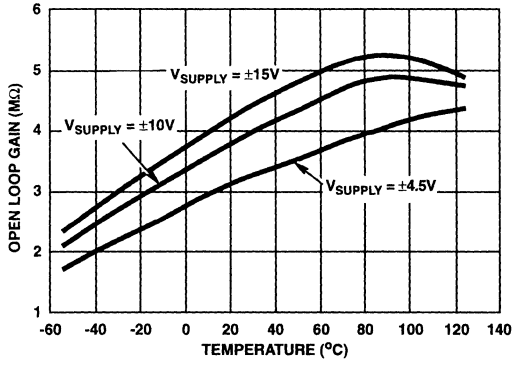


FIGURE 14. TRANSIMPEDANCE vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

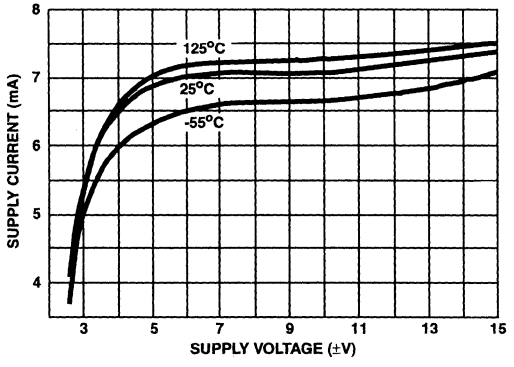


FIGURE 15. SUPPLY CURRENT vs SUPPLY VOLTAGE (AVERAGE OF 30 UNITS FROM 3 LOTS)

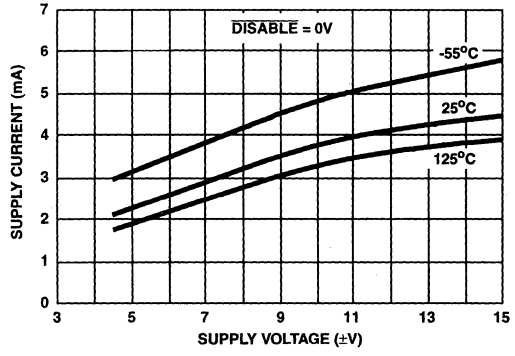


FIGURE 16. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE (AVERAGE OF 30 UNITS FROM 3 LOTS)

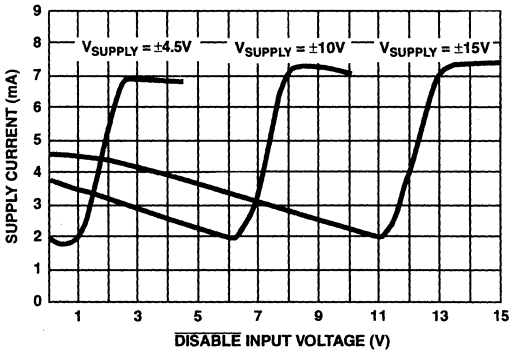


FIGURE 17. SUPPLY CURRENT vs $\overline{DISABLE}$ INPUT VOLTAGE

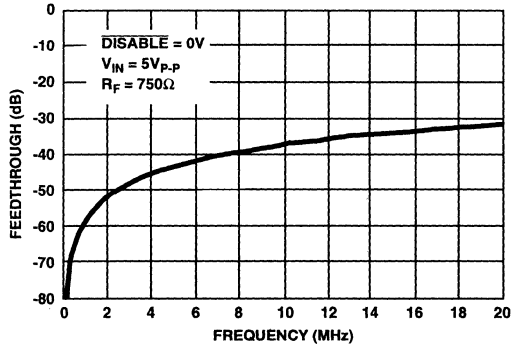


FIGURE 18. DISABLE MODE FEEDTHROUGH vs FREQUENCY

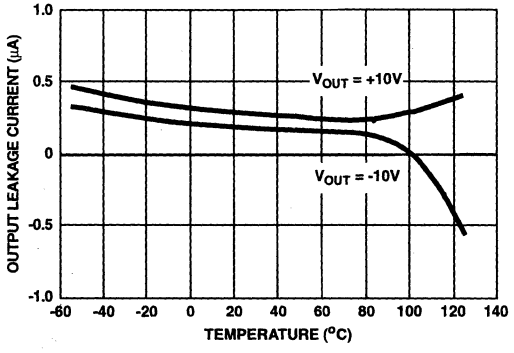


FIGURE 19. DISABLED OUTPUT LEAKAGE vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

Typical Performance Curves

$V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

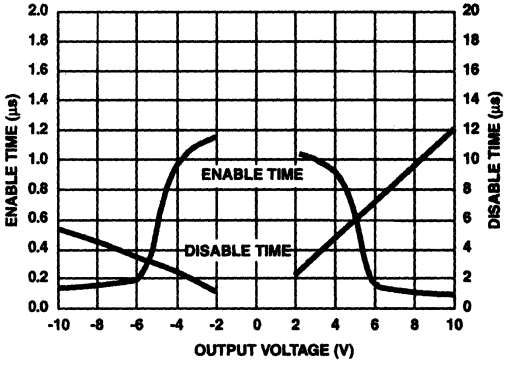


FIGURE 20. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE (AVERAGE OF 9 UNITS FROM 3 LOTS)

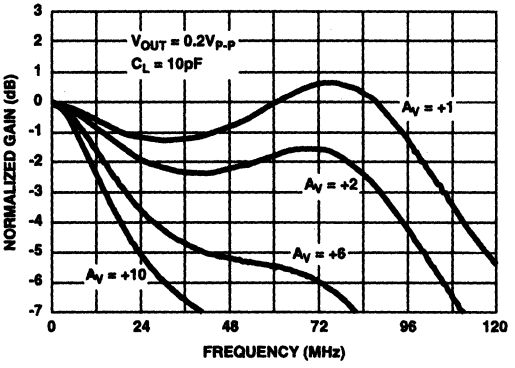


FIGURE 21. NON-INVERTING GAIN vs FREQUENCY

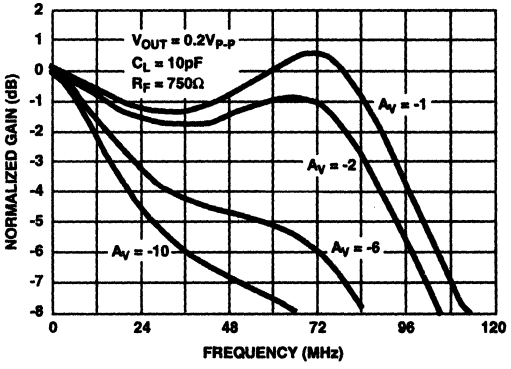


FIGURE 22. INVERTING FREQUENCY RESPONSE

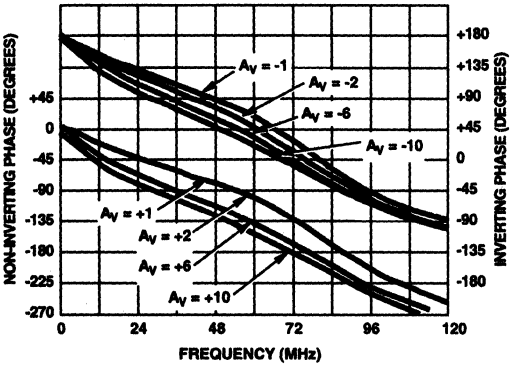


FIGURE 23. PHASE vs FREQUENCY

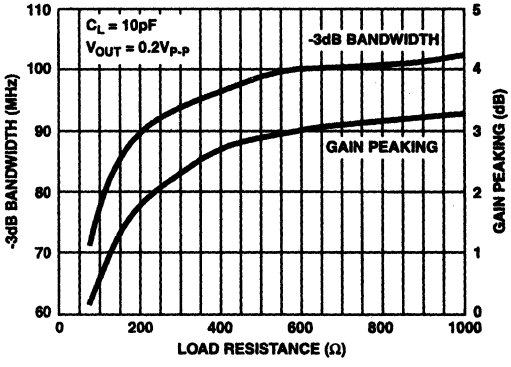


FIGURE 24. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

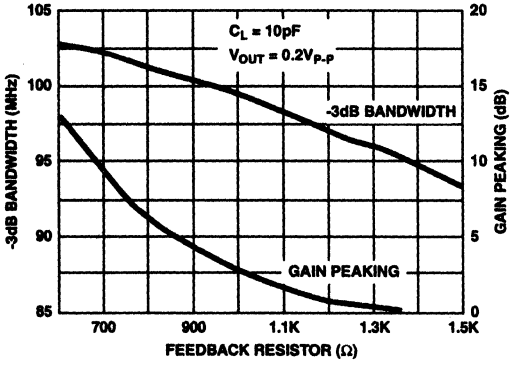


FIGURE 25. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

Typical Performance Curves

$V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

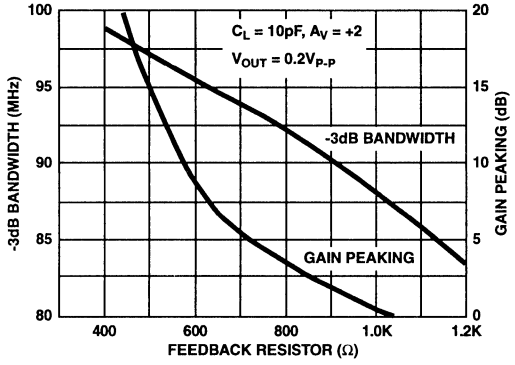


FIGURE 26. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

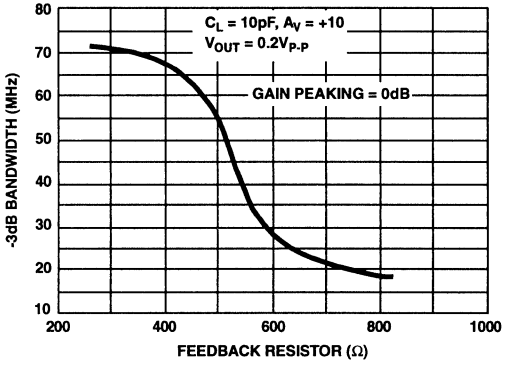


FIGURE 27. BANDWIDTH vs FEEDBACK RESISTANCE

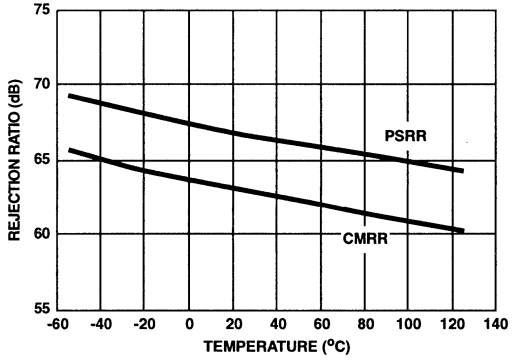


FIGURE 28. REJECTION RATIOS vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

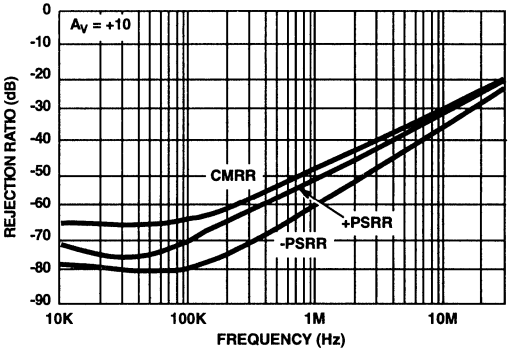


FIGURE 29. REJECTION RATIOS vs FREQUENCY

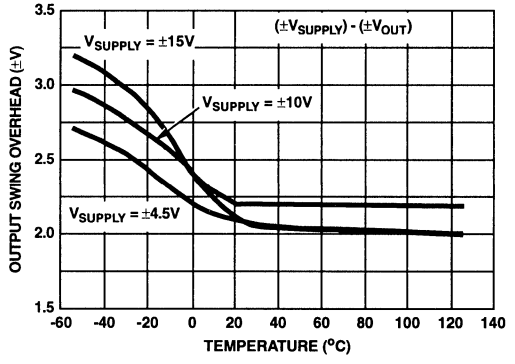


FIGURE 30. OUTPUT SWING OVERHEAD vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

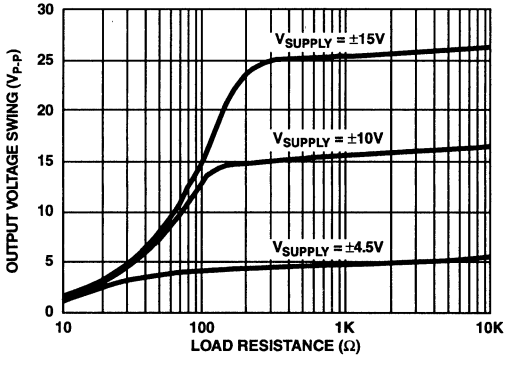


FIGURE 31. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

Typical Performance Curves

$V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

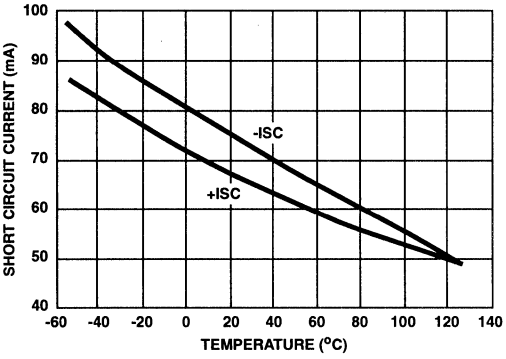


FIGURE 32. SHORT CIRCUIT CURRENT LIMIT vs TEMPERATURE

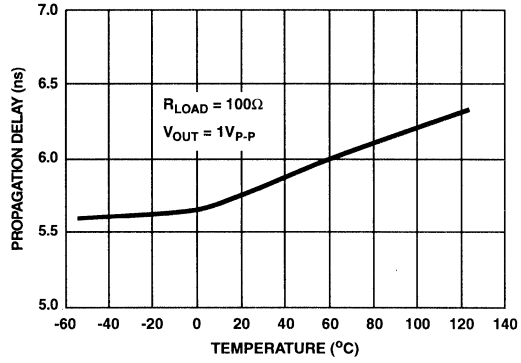


FIGURE 33. PROPAGATION DELAY vs TEMPERATURE (AVERAGE OF 18 UNITS FROM 3 LOTS)

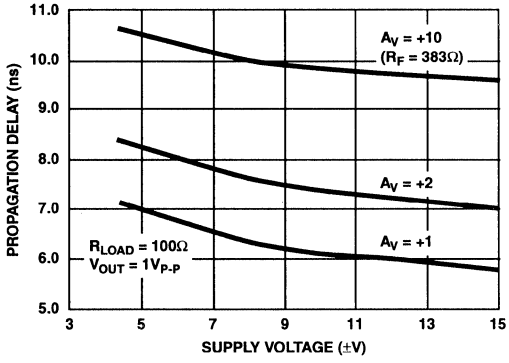


FIGURE 34. PROPAGATION DELAY vs SUPPLY VOLTAGE (AVERAGE OF 18 UNITS FROM 3 LOTS)

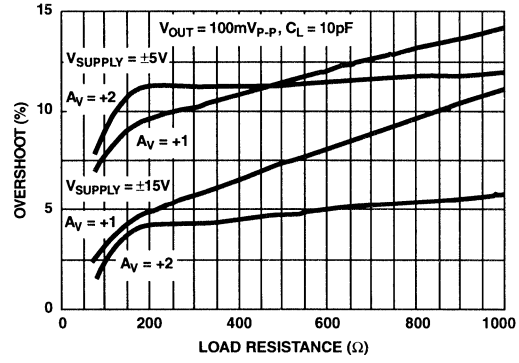


FIGURE 35. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

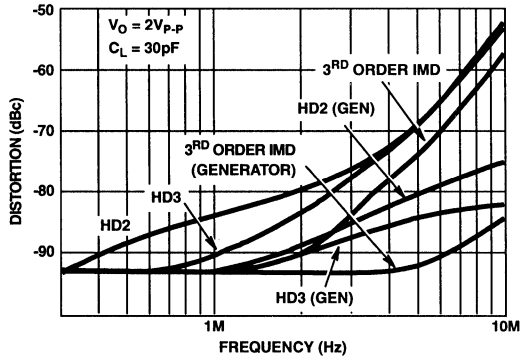


FIGURE 36. DISTORTION vs FREQUENCY

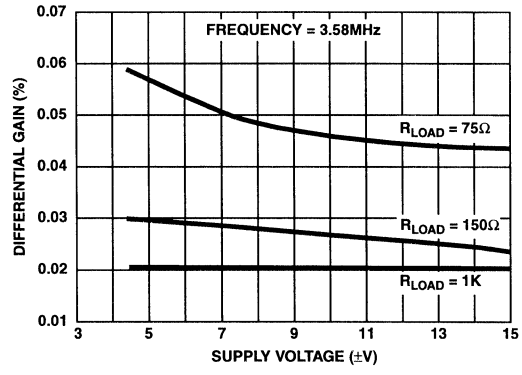


FIGURE 37. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE (AVERAGE OF 18 UNITS FROM 3 LOTS)

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

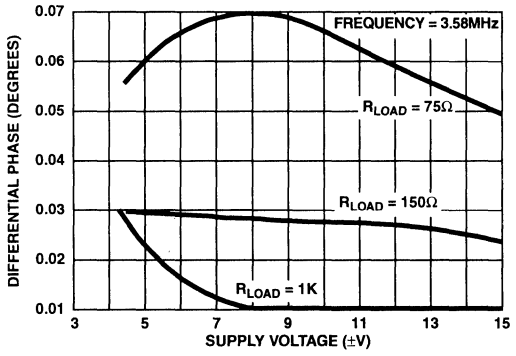


FIGURE 38. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE (AVERAGE OF 18 UNITS FROM 3 LOTS)

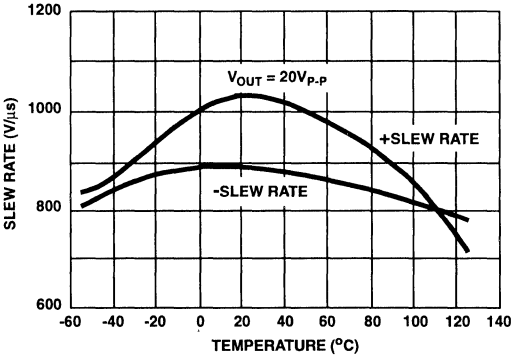


FIGURE 39. SLEW RATE vs TEMPERATURE (AVERAGE OF 30 UNITS FROM 3 LOTS)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

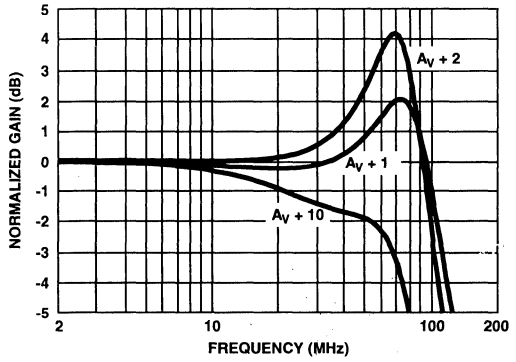


FIGURE 40. NON-INVERTING FREQUENCY RESPONSE

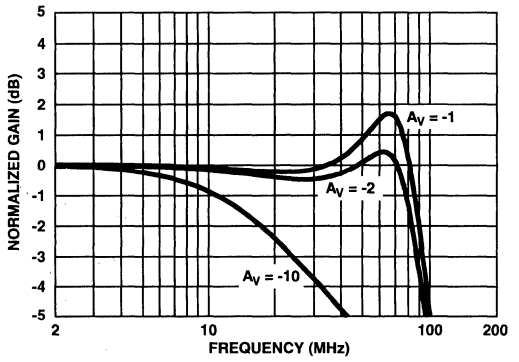


FIGURE 41. INVERTING FREQUENCY RESPONSE

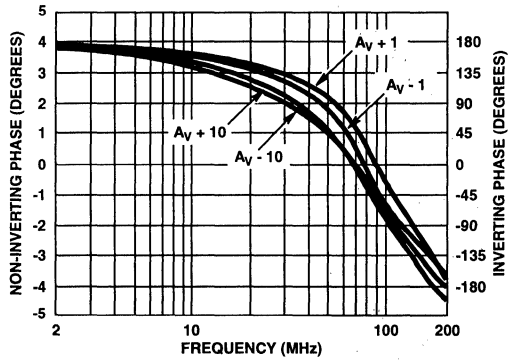


FIGURE 42. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

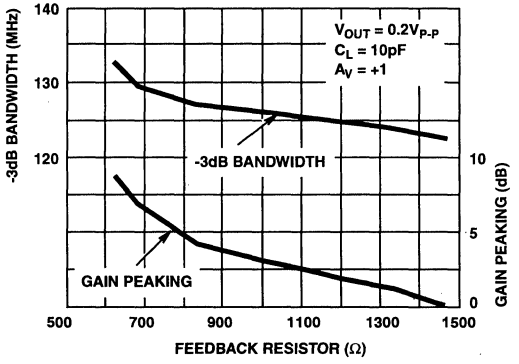


FIGURE 43. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

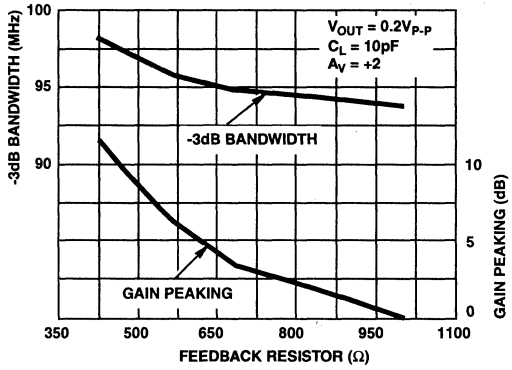


FIGURE 44. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

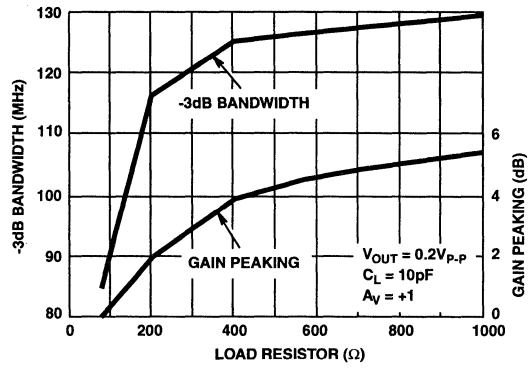


FIGURE 45. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

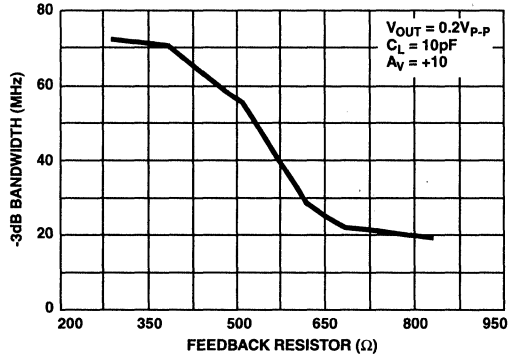


FIGURE 46. BANDWIDTH vs FEEDBACK RESISTANCE

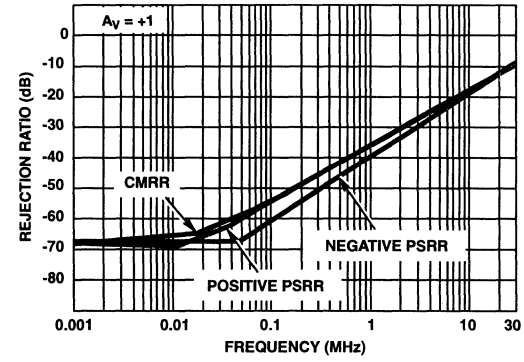


FIGURE 47. REJECTION RATIOS vs FREQUENCY

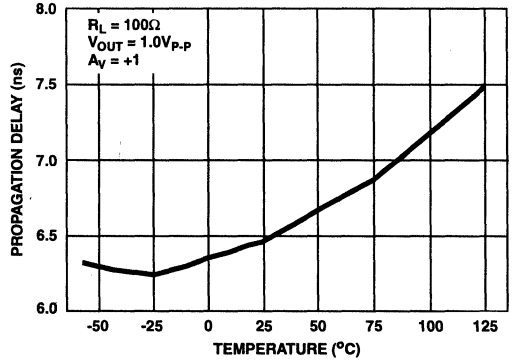


FIGURE 48. PROPAGATION DELAY vs TEMPERATURE

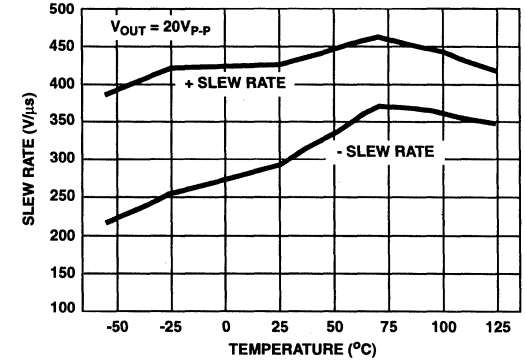


FIGURE 49. SLEW RATE vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

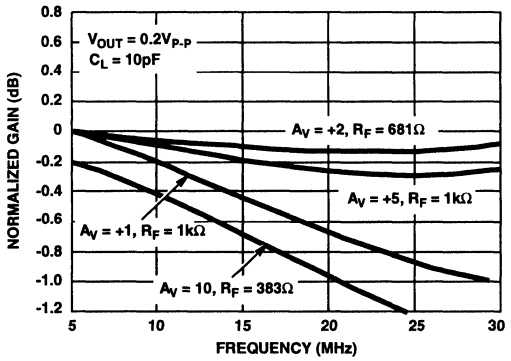


FIGURE 50. NON-INVERTING GAIN FLATNESS vs FREQUENCY

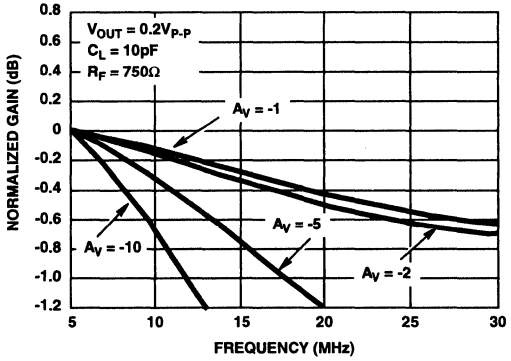


FIGURE 51. INVERTING GAIN FLATNESS vs FREQUENCY

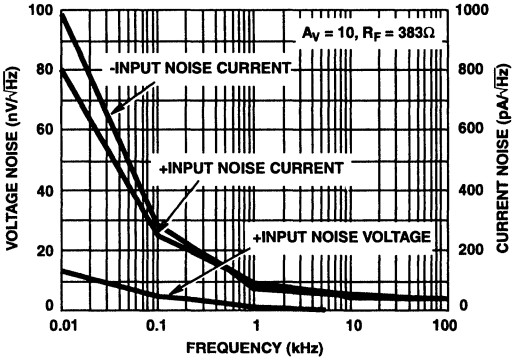


FIGURE 52. INPUT NOISE CHARACTERISTICS

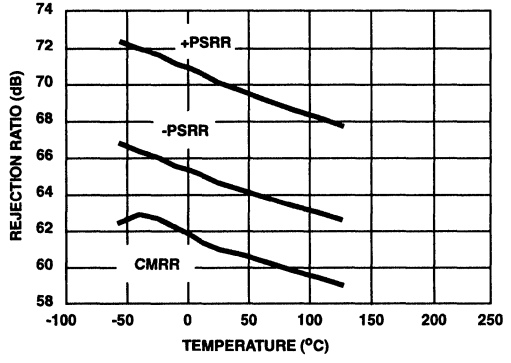


FIGURE 53. REJECTION RATIO vs TEMPERATURE

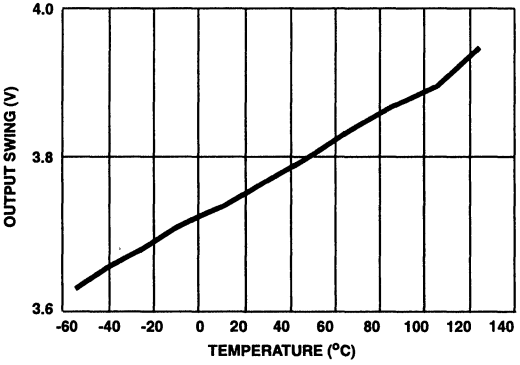


FIGURE 54. OUTPUT SWING vs TEMPERATURE

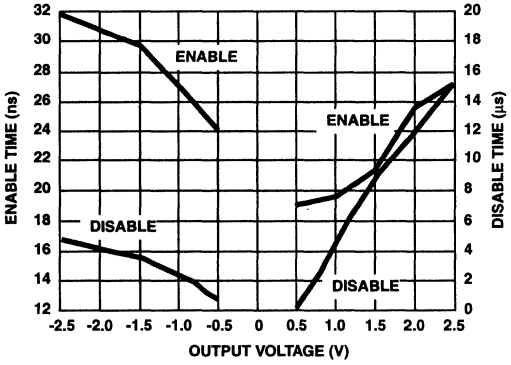


FIGURE 55. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

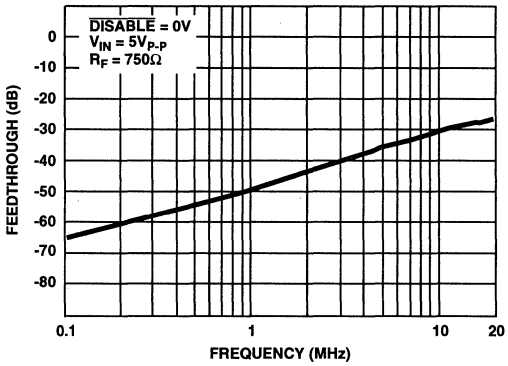


FIGURE 56. DISABLE FEEDTHROUGH vs FREQUENCY

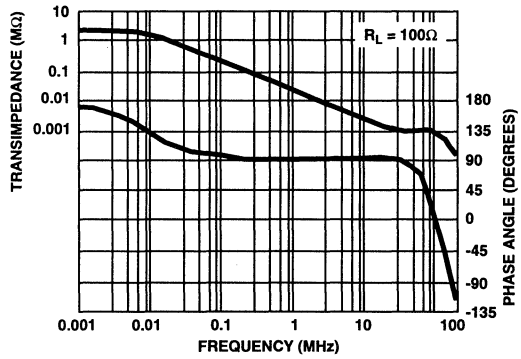


FIGURE 57. TRANSIMPEDANCE vs FREQUENCY

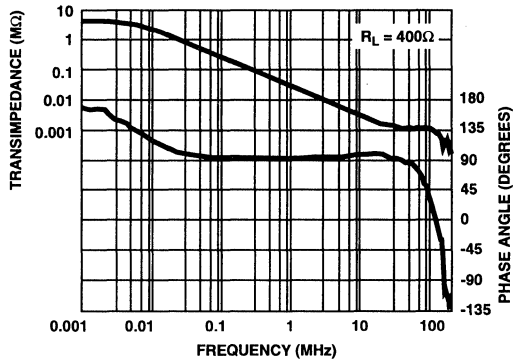


FIGURE 58. TRANSIMPEDENCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

1640µm x 1520µm x 483µm

METALLIZATION:

Type: Aluminum, 1% Copper
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1kÅ

TRANSISTOR COUNT:

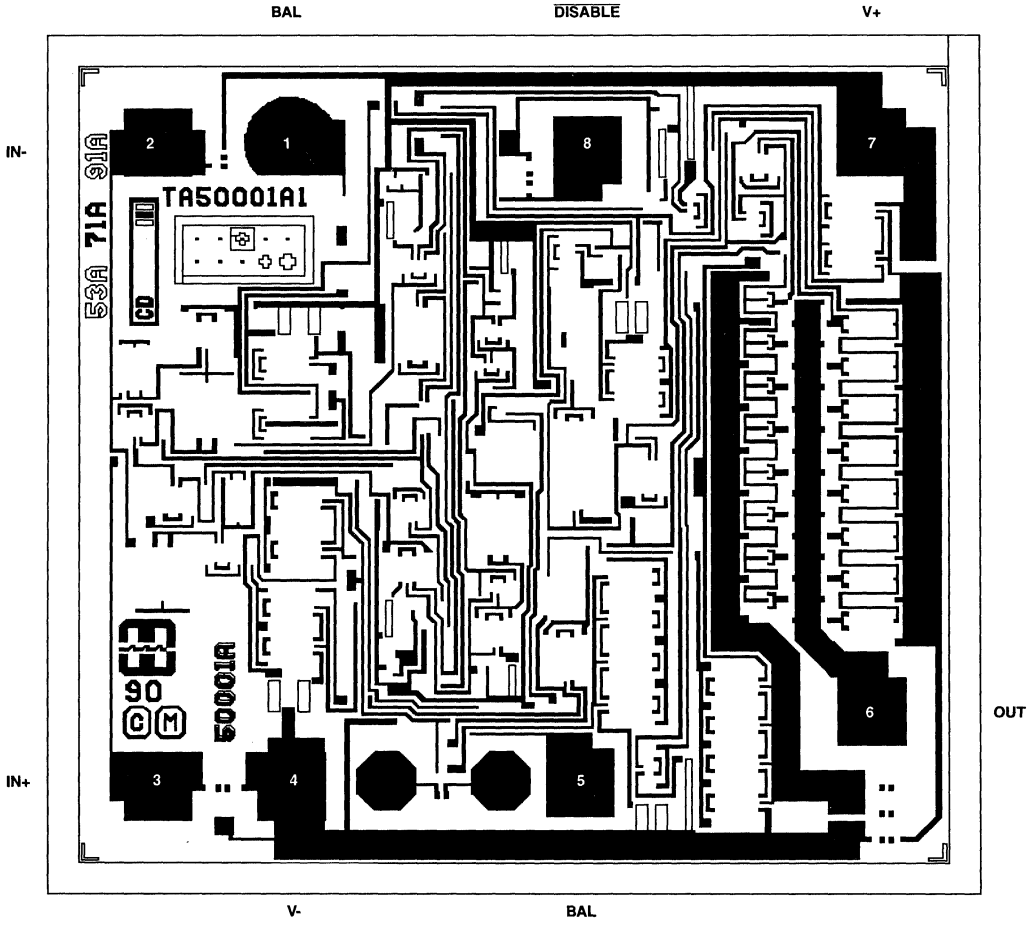
62

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5020



HARRIS SEMICONDUCTOR

HA5022

Dual, 125MHz, Video Current Feedback Amplifier with Disable

November 1996

Features

- Dual Version of HA-5020
- Individual Output Enable/Disable
- Input Offset Voltage 800µV
- Wide Unity Gain Bandwidth 125MHz
- Slew Rate 475V/µs
- Differential Gain 0.03%
- Differential Phase . . . . . 0.03 Degrees
- Supply Current (per Amplifier) 7.5mA
- ESD Protection 4000V
- Guaranteed Specifications at ±5V Supplies

Applications

- Video Multiplexers; Video Switching and Routing
- Video Gain Block
- Video Distribution Amplifier/RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter
- Medical Imaging
- Radar and Imaging Systems

Description

The HA5022 is a dual version of the popular Harris HA-5020. It features wide bandwidth and high slew rate, and is optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The HA5022 also features a disable function that significantly reduces supply current while forcing the output to a true high impedance state. This functionality allows 2:1 video multiplexers to be implemented with a single IC.

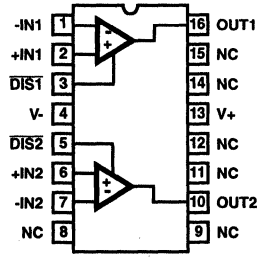
The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA5022IP	-40 to 85	16 Ld PDIP	E16.3
HA5022IB	-40 to 85	16 Ld SOIC	M16.15
HA5022EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HA5022
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1996

File Number **3392.4**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
DC Input Voltage (Note 3) . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage. 10V
Output Current (Note 4) . . . . . Short Circuit Protected
ESD Rating (Note 3)
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 2000V

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage Range (Typical) . . . . . ±4.5V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	90
SOIC Package	115

Maximum Junction Temperature (Note 1) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package, Note 1) . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175^oC for die, and below 150^oC for plastic packages. See Application Information section for safe operating area information.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. The non-inverting input of unused amplifiers must be connected to GND.
4. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.

Electrical Specifications

$V_{SUPPLY} = \pm 5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 11) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (V_{IO})		A	25	-	0.8	3	mV
		A	Full	-	-	5	mV
Delta V_{IO} Between Channels		A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift		B	Full	-	5	-	µV/^oC
V_{IO} Common Mode Rejection Ratio	Note 5	A	25	53	-	-	dB
		A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	60	-	-	dB
		A	Full	55	-	-	dB
Input Common Mode Range	Note 5	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current		A	25	-	3	8	µA
		A	Full	-	-	20	µA
+IN Common Mode Rejection ($+I_{BCMR} = \frac{1}{+R_{IN}}$)	Note 5	A	25	-	-	0.15	µA/V
		A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	-	-	0.1	µA/V
		A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current		A	25, 85	-	4	12	µA
		A	-40	-	10	30	µA
Delta -IN BIAS Current Between Channels		A	25, 85	-	6	15	µA
		A	-40	-	10	30	µA
-IN Common Mode Rejection	Note 5	A	25	-	-	0.4	µA/V
		A	Full	-	-	1.0	µA/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 11) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
-IN Power Supply Rejection	$\pm3.5V \leq V_S \leq \pm6.5V$	A	25	-	-	0.2	µA/V
		A	Full	-	-	0.5	µA/V
Input Noise Voltage	f = 1kHz	B	25	-	4.5	-	nV/√Hz
+Input Noise Current	f = 1kHz	B	25	-	2.5	-	pA/√Hz
-Input Noise Current	f = 1kHz	B	25	-	25.0	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Transimpedance	Note 16	A	25	1.0	-	-	MΩ
		A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain	$R_L = 400\Omega$, $V_{OUT} = \pm2.5V$	A	25	70	-	-	dB
		A	Full	65	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm2.5V$	A	25	50	-	-	dB
		A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing	$R_L = 150\Omega$	A	25	±2.5	±3.0	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	$R_L = 150\Omega$	B	Full	±16.6	±20.0	-	mA
Output Current, Short Circuit	$V_{IN} = \pm2.5V$, $V_{OUT} = 0V$	A	Full	±40	±60	-	mA
Output Current, Disabled	$V_{OUT} = \pm2.5V$, $V_{IN} = 0V$, $\overline{DISABLE} = 0V$	A	Full	-	-	2	µA
Output Disable Time	Note 12	B	25	-	40	-	µs
Output Enable Time	Note 13	B	25	-	40	-	ns
Output Capacitance, Disabled	Note 14	B	25	-	15	-	pF
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		A	25	5	-	15	V
Quiescent Supply Current		A	Full	-	7.5	10	mA/Op Amp
Supply Current, Disabled	$\overline{DISABLE} = 0V$	A	Full	-	5	7.5	mA/Op Amp
$\overline{Disable}$ Pin Input Current	$\overline{DISABLE} = 0V$	A	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable	Note 6	A	Full	350	-	-	µA
Maximum Pin 8 Current to Enable	Note 7	A	Full	-	-	20	µA
AC CHARACTERISTICS ($A_V = +1$)							
Slew Rate	Note 8	B	25	275	400	-	V/µs
Full Power Bandwidth	Note 9	B	25	22	28	-	MHz
Rise Time	Note 10	B	25	-	6	-	ns
Fall Time	Note 10	B	25	-	6	-	ns
Propagation Delay	Note 10	B	25	-	6	-	ns
Overshoot		B	25	-	4.5	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	75	-	ns

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 11) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)							
Slew Rate	Note 8	B	25	-	475	-	V/µs
Full Power Bandwidth	Note 9	B	25	-	26	-	MHz
Rise Time	Note 10	B	25	-	6	-	ns
Fall Time	Note 10	B	25	-	6	-	ns
Propagation Delay	Note 10	B	25	-	6	-	ns
Overshoot		B	25	-	12	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	100	-	ns
Gain Flatness	5MHz	B	25	-	0.02	-	dB
	20MHz	B	25	-	0.07	-	dB
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)							
Slew Rate	Note 8	B	25	350	475	-	V/µs
Full Power Bandwidth	Note 9	B	25	28	38	-	MHz
Rise Time	Note 10	B	25	-	8	-	ns
Fall Time	Note 10	B	25	-	9	-	ns
Propagation Delay	Note 10	B	25	-	9	-	ns
Overshoot		B	25	-	1.8	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	75	-	ns
Settling Time to 0.1%	2V Output Step	B	25	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (Note 15)	$R_L = 150\Omega$	B	25	-	0.03	-	%
Differential Phase (Note 15)	$R_L = 150\Omega$	B	25	-	0.03	-	Degrees

NOTES:

5. $V_{CM} = \pm2.5V$. At -40°C Product is tested at $V_{CM} = \pm2.25V$ because short test duration does not allow self heating.
6. $R_L = 100\Omega$, $V_{IN} = 2.5V$. This is the minimum current which must be pulled out of the $\overline{\text{Disable}}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
7. $V_{IN} = 0V$. This is the maximum current that can be pulled out of the $\overline{\text{Disable}}$ pin with the HA5022 remaining enabled. The HA5022 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
9. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 2V$.
10. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. A. Production Tested; B. Typical or Guaranteed Limit based on characterization; C. Design Typical for information only.
12. $V_{IN} = +2V$, $\overline{\text{DISABLE}} = +5V$ to 0V. Measured from the 50% point of $\overline{\text{DISABLE}}$ to $V_{OUT} = 0V$.
13. $V_{IN} = +2V$, $\overline{\text{DISABLE}} = 0V$ to +5V. Measured from the 50% point of $\overline{\text{DISABLE}}$ to $V_{OUT} = 2V$.
14. $V_{IN} = 0V$, Force V_{OUT} from 0V to $\pm2.5V$, $t_R = t_F = 50ns$, $\overline{\text{DISABLE}} = 0V$.
15. Measured with a VM700A video tester using an NTC-7 composite VITS.
16. $V_{OUT} = \pm2.5V$. At -40°C Product is tested at $V_{OUT} = \pm2.25V$ because short test duration does not allow self heating.

Test Circuits and Waveforms

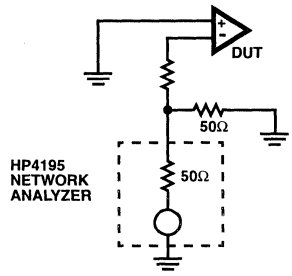


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

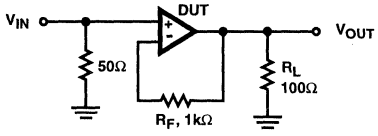


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

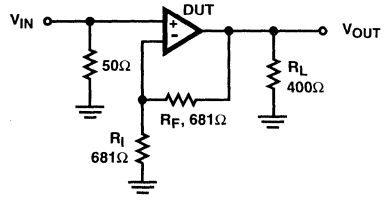
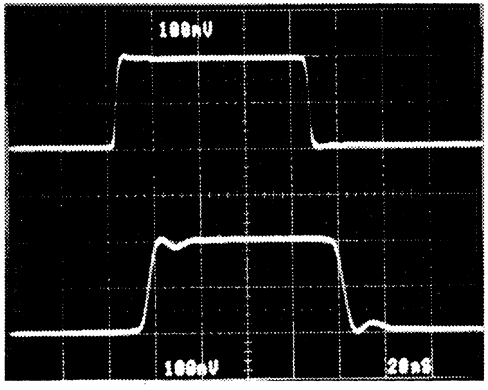
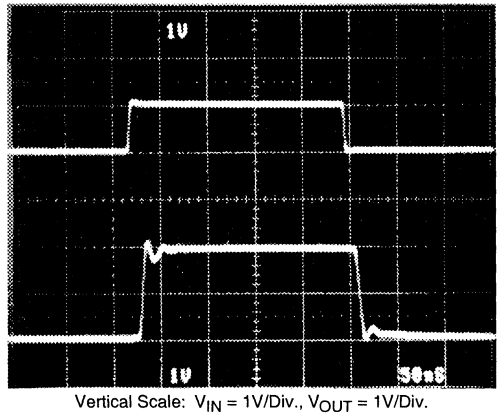


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

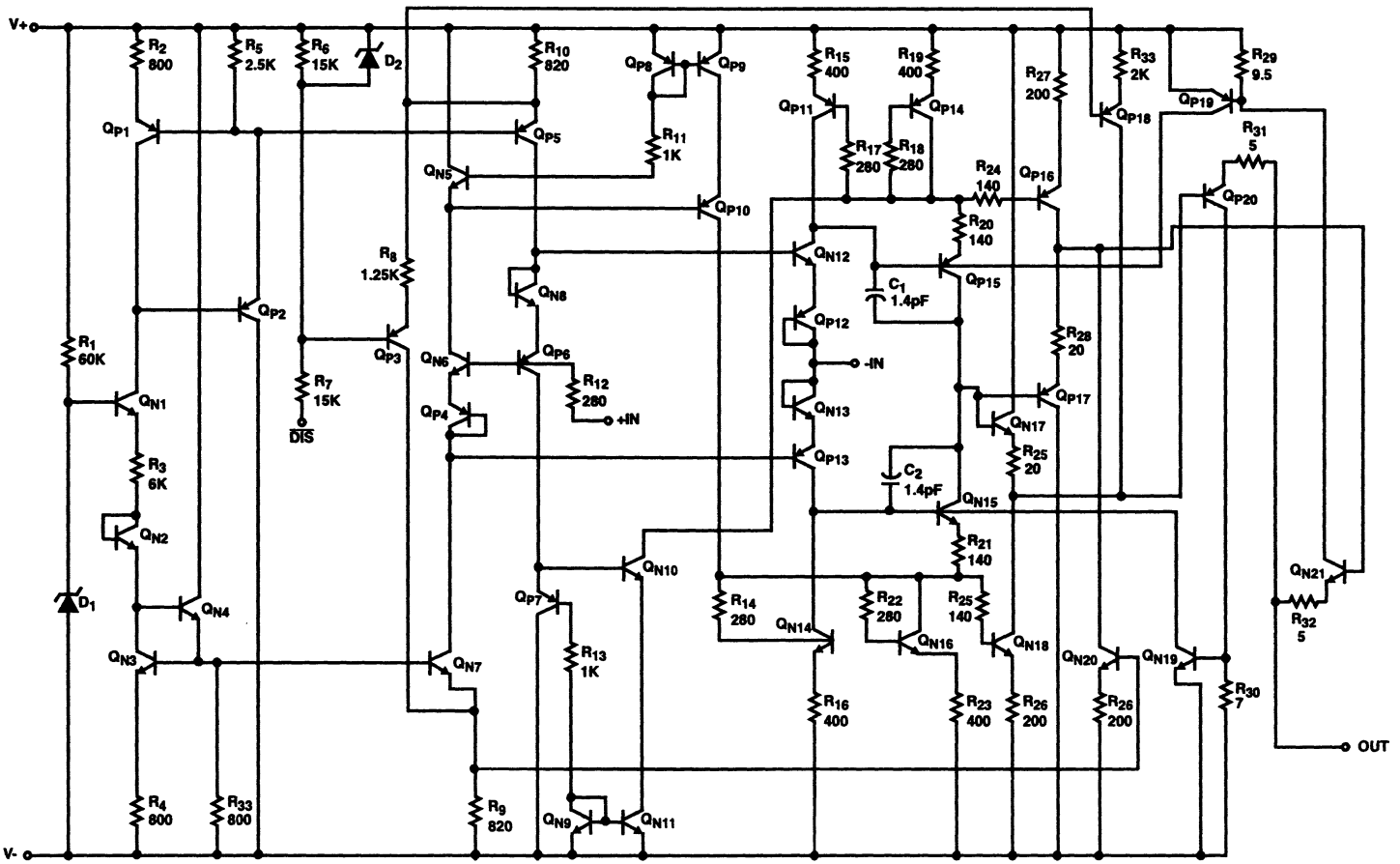
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic Diagram (One Amplifier of Two)



Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 11 and Figure 12 in the Typical Performance Curves section, illustrate the performance of the HA5022 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5022 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10μF) tantalum or electrolytic capacitor in parallel with a small value (0.1μF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

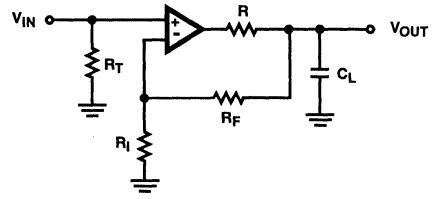


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (PDIP, SOIC). At V_S = ±5V quiescent operation both package styles may be operated over the full industrial range of -40°C to 85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

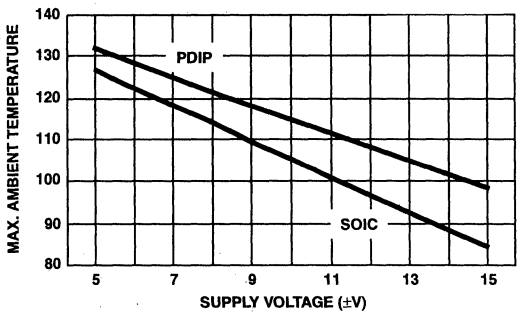


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Enable/Disable Function

When enabled the amplifier functions as a normal current feedback amplifier with all of the data in the electrical specifications table being valid and applicable. When disabled the amplifier output assumes a true high impedance state and the supply current is reduced significantly.

The circuit shown in Figure 8 is a simplified schematic of the enable/disable function. The large value resistors in series with the DISABLE pin makes it appear as a current source to the driver. When the driver pulls this pin low current flows out of the pin and into the driver. This current, which may be as large as 350µA when external circuit and process variables are at their extremes, is required to insure that point "A" achieves the proper potential to disable the output. The driver must have the compliance and capability of sinking all of this current.

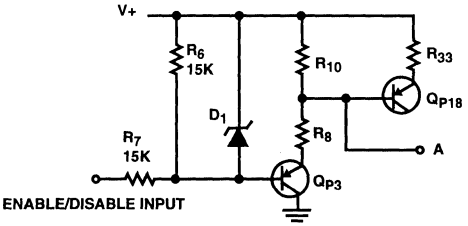


FIGURE 8. SIMPLIFIED SCHEMATIC OF ENABLE/DISABLE FUNCTION

When V_{CC} is +5V the DISABLE pin may be driven with a dedicated TTL gate. The maximum low level output voltage of the TTL gate, 0.4V, has enough compliance to insure that the amplifier will always be disabled even though D_1 will not turn on, and the TTL gate will sink enough current to keep point "A" at its proper voltage. When V_{CC} is greater than +5V the DISABLE pin should be driven with an open collector device that has a breakdown rating greater than V_{CC}.

Referring to Figure 8, it can be seen that R_6 will act as a pull-up resistor to $+V_{CC}$ if the DISABLE pin is left open. In those cases where the enable/disable function is not required on all circuits some circuits can be permanently enabled by letting the DISABLE pin float. If a driver is used to set the enable/disable level, be sure that the driver does not sink more than 20µA when the DISABLE pin is at a high level. TTL gates, especially CMOS versions, do not violate this criteria so it is permissible to control the enable/disable function with TTL.

Typical Applications

Two Channel Video Multiplexer

Referring to the amplifier U_{1A} in Figure 9, R_1 terminates the cable in its characteristic impedance of 75Ω, and R_4 back terminates the cable in its characteristic impedance. The amplifier is set up in a gain configuration of +2 to yield an overall network gain of +1 when driving a double terminated cable. The value of R_3 can be changed if a different network gain is desired. R_5 holds the disable pin at ground thus inhibiting the amplifier until the switch, S_1, is thrown to position 1. At position 1 the switch pulls the disable pin up to the plus supply rail thereby enabling the amplifier. Since all of the actual signal switching takes place within the amplifier, it's differential gain and phase parameters, which are 0.03% and 0.03 degrees respectively, determine the circuit's performance. The other circuit, U_{1B}, operates in a similar manner.

When the plus supply rail is 5V the disable pin can be driven by a dedicated TTL gate as discussed earlier. If a multiplexer IC or its equivalent is used to select channels its logic must be break before make. When these conditions are satisfied the HA5022 is often used as a remote video multiplexer, and the multiplexer may be extended by adding more amplifier ICs.

Low Impedance Multiplexer

Two common problems surface when you try to multiplex multiple high speed signals into a low impedance source such as an A/D converter. The first problem is the low source impedance which tends to make amplifiers oscillate and causes gain errors. The second problem is the multiplexer which supplies no gain, introduces all kinds of distortion and limits the frequency response. Using op amps which have an enable/disable function, such as the HA5022, eliminates the multiplexer problems because the external mux chip is not needed, and the HA5022 can drive low impedance (large capacitance) loads if a series isolation resistor is used.

Referring to Figure 10, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications. Since the drivers usually are terminated in their characteristic impedance the input gain is 0.5, thus the amplifiers, U_2, are configured in a gain of +2 to set the circuit gain equal to one. Resistors R_2 and R_3 determine the amplifier gain, and if a different gain is desired R_2 should be changed according to the equation $G = (1 + R_3/R_2)$. R_3 sets the frequency response of the amplifier so you should refer to the manufacturers data sheet before changing its value. R_5, C_1 and D_1 are an asymmetrical charge/discharge time circuit which configures U_1 as a break before make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels the drive logic must be designed to be break before make. R_4 is enclosed in the feedback loop of the amplifier so that the large open loop amplifier gain of U_2 will present the load with a small closed loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown in Figure 10 was tested for the full range of capacitor values with no oscillations being observed; thus, problem one has been solved.The frequency and gain characteristics of the circuit are now those of the amplifier independent of any multiplexing action; thus, problem two has been solved. The multiplexer transition time is approximately 15µs with the component values shown.

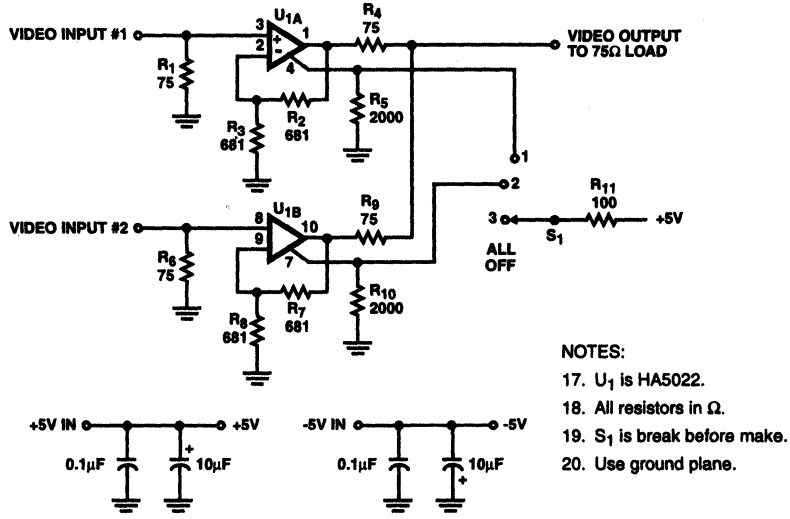


FIGURE 9. TWO CHANNEL HIGH IMPEDANCE MULTIPLEXER

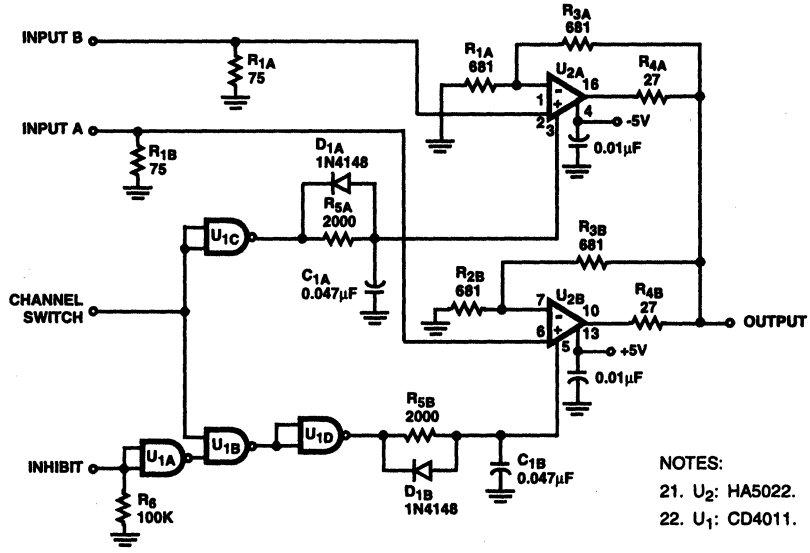


FIGURE 10. LOW IMPEDANCE MULTIPLEXER

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

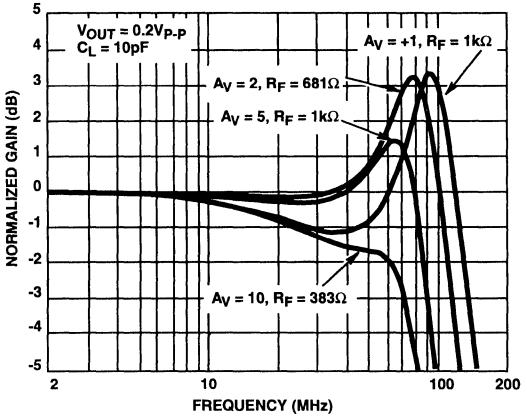


FIGURE 11. NON-INVERTING FREQUENCY RESPONSE

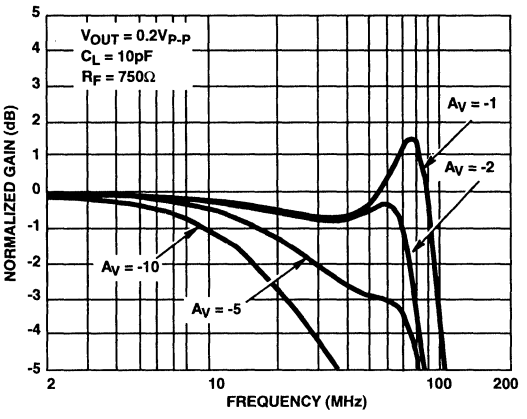


FIGURE 12. INVERTING FREQUENCY RESPONSE

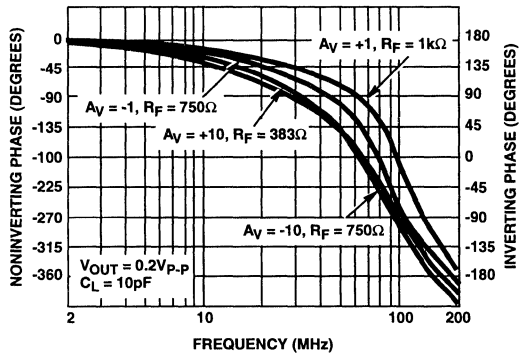


FIGURE 13. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

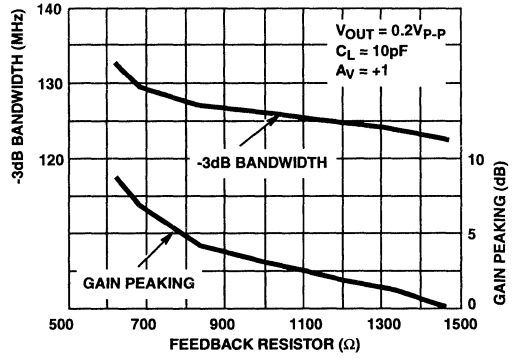


FIGURE 14. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

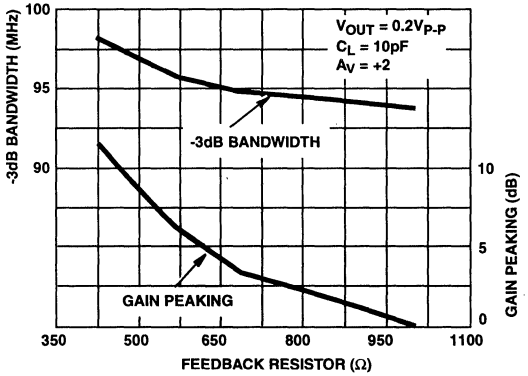


FIGURE 15. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

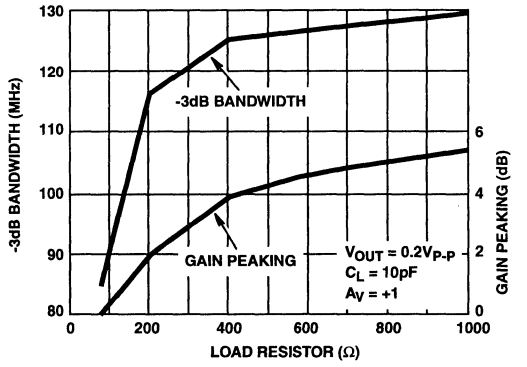


FIGURE 16. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

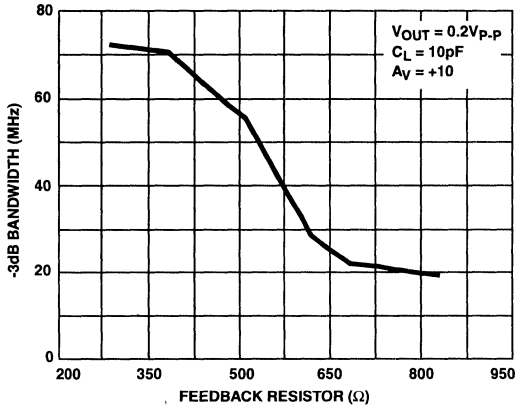


FIGURE 17. BANDWIDTH vs FEEDBACK RESISTANCE

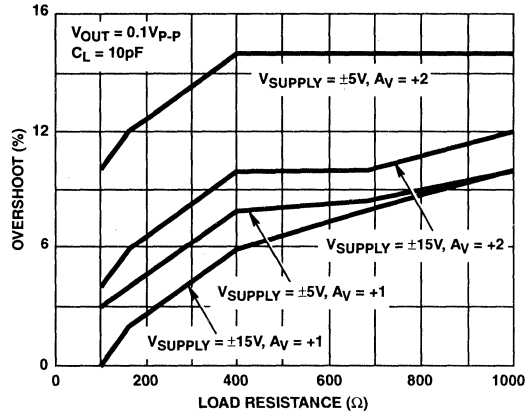


FIGURE 18. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

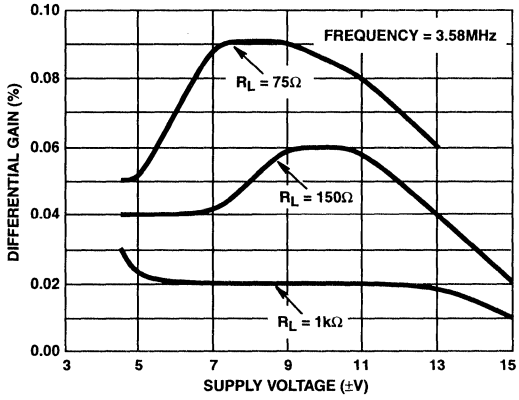


FIGURE 19. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

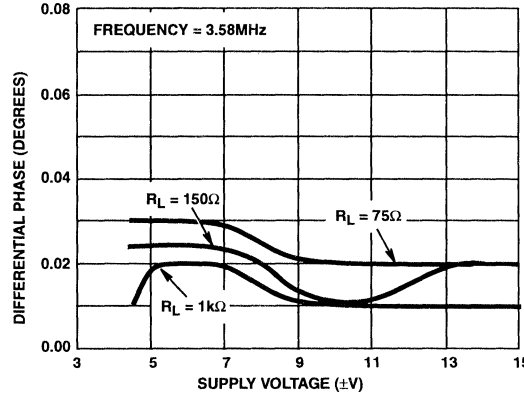


FIGURE 20. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

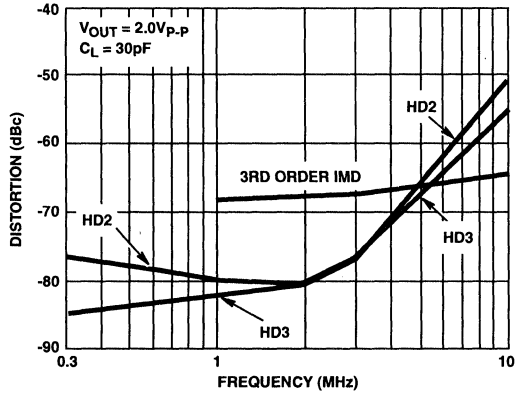


FIGURE 21. DISTORTION vs FREQUENCY

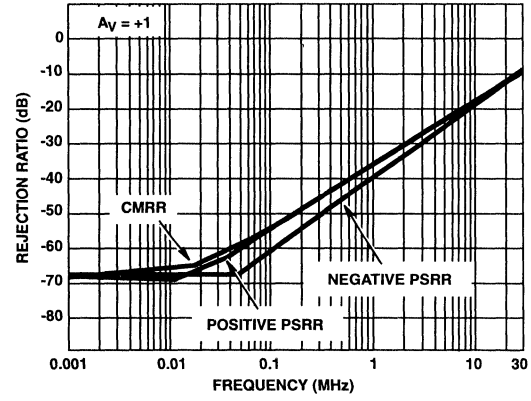


FIGURE 22. REJECTION RATIOS vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

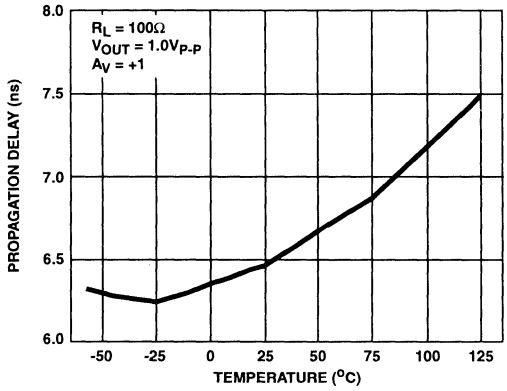


FIGURE 23. PROPAGATION DELAY vs TEMPERATURE

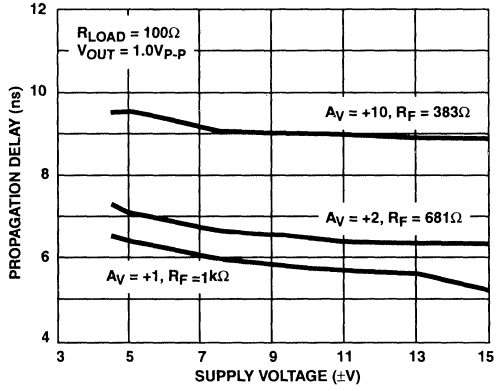


FIGURE 24. PROPAGATION DELAY vs SUPPLY VOLTAGE

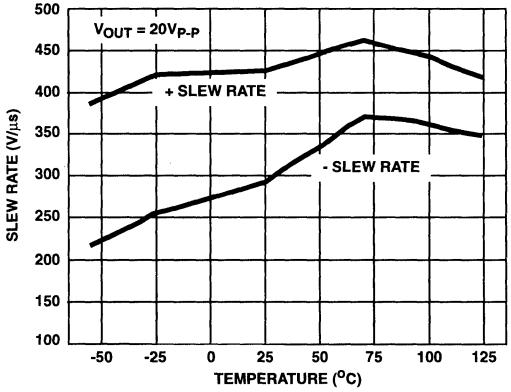


FIGURE 25. SLEW RATE vs TEMPERATURE

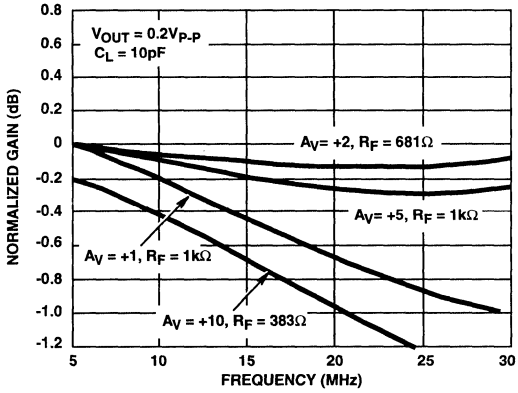


FIGURE 26. NON-INVERTING GAIN FLATNESS vs FREQUENCY

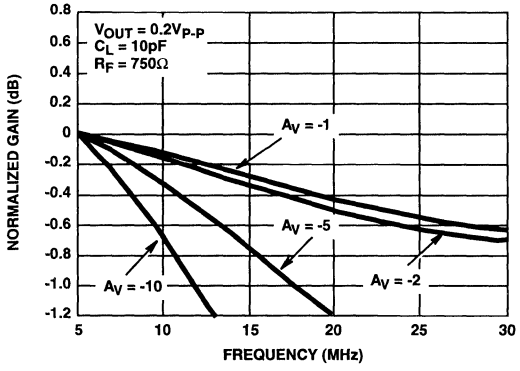


FIGURE 27. INVERTING GAIN FLATNESS vs FREQUENCY

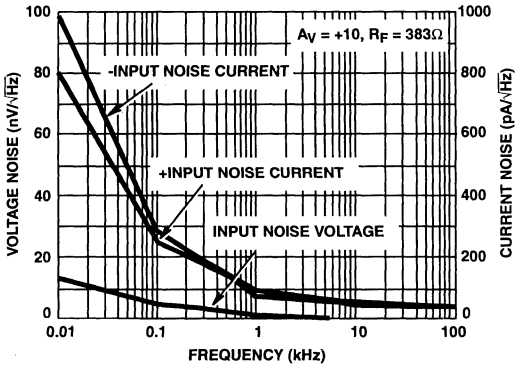


FIGURE 28. INPUT NOISE CHARACTERISTICS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

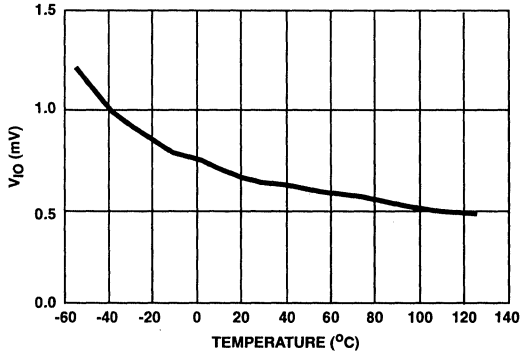


FIGURE 29. INPUT OFFSET VOLTAGE vs TEMPERATURE

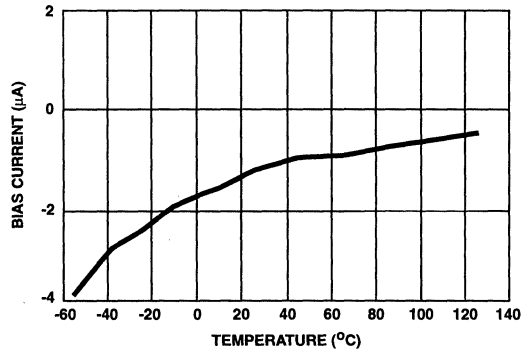


FIGURE 30. +INPUT BIAS CURRENT vs TEMPERATURE

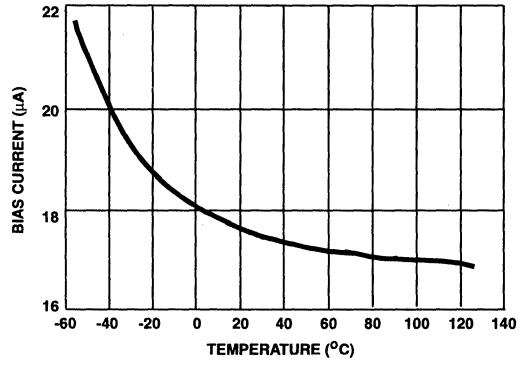


FIGURE 31. -INPUT BIAS CURRENT vs TEMPERATURE

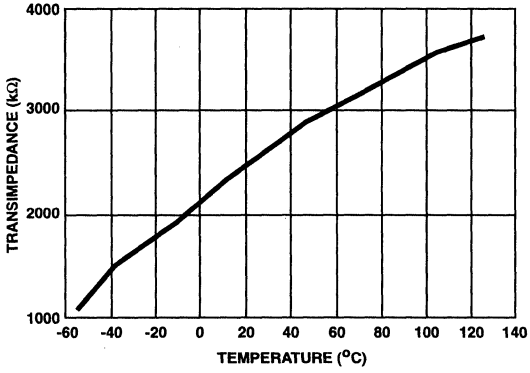


FIGURE 32. TRANSIMPEDANCE vs TEMPERATURE

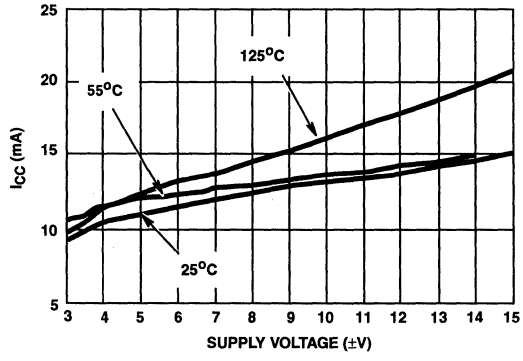


FIGURE 33. SUPPLY CURRENT vs SUPPLY VOLTAGE

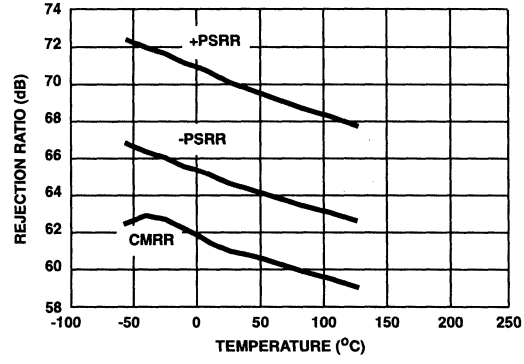


FIGURE 34. REJECTION RATIO vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

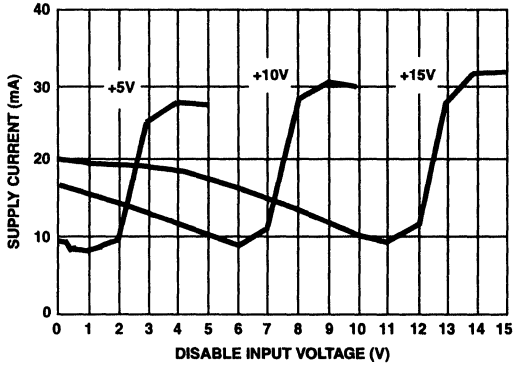


FIGURE 35. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

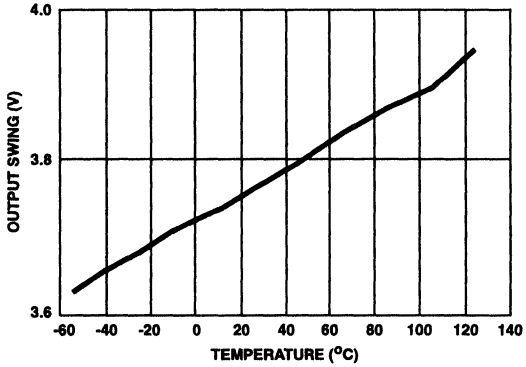


FIGURE 36. OUTPUT SWING vs TEMPERATURE

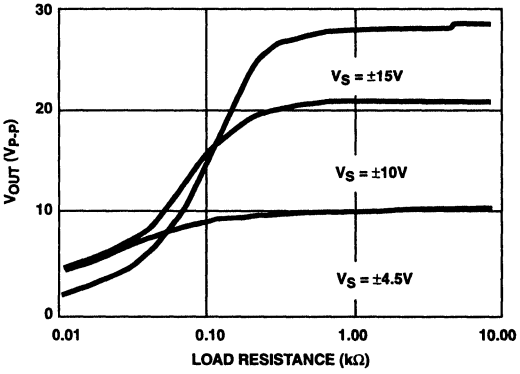


FIGURE 37. OUTPUT SWING vs LOAD RESISTANCE

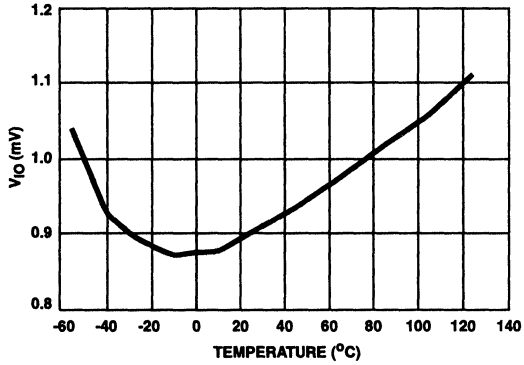


FIGURE 38. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

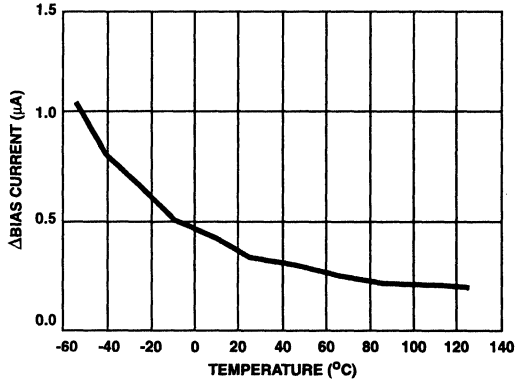


FIGURE 39. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

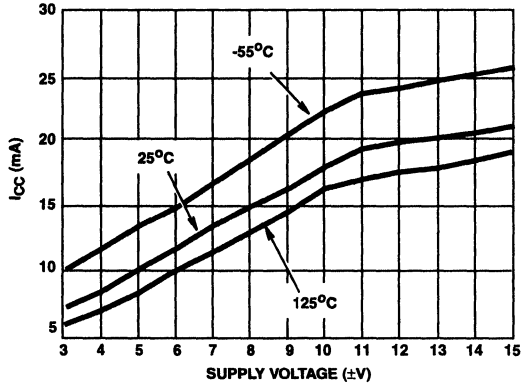


FIGURE 40. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

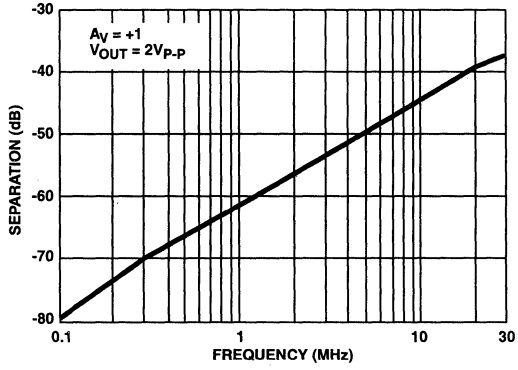


FIGURE 41. CHANNEL SEPARATION vs FREQUENCY

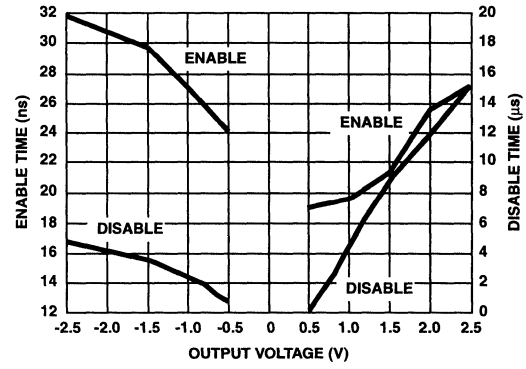


FIGURE 42. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

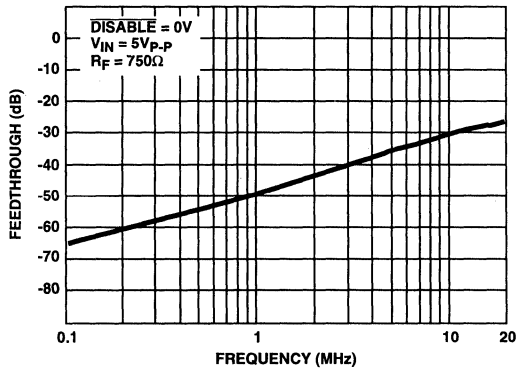


FIGURE 43. DISABLE FEEDTHROUGH vs FREQUENCY

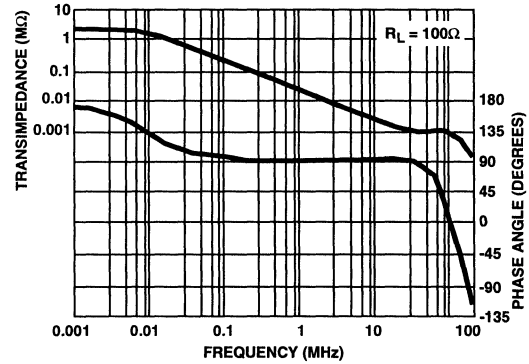


FIGURE 44. TRANSIMPEDANCE vs FREQUENCY

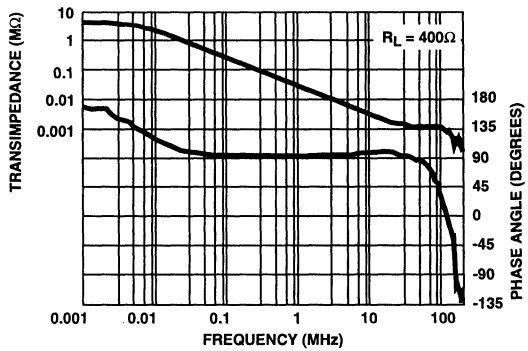


FIGURE 45. TRANSIMPEDENCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

1650µm x 2540µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.4kÅ

TRANSISTOR COUNT:

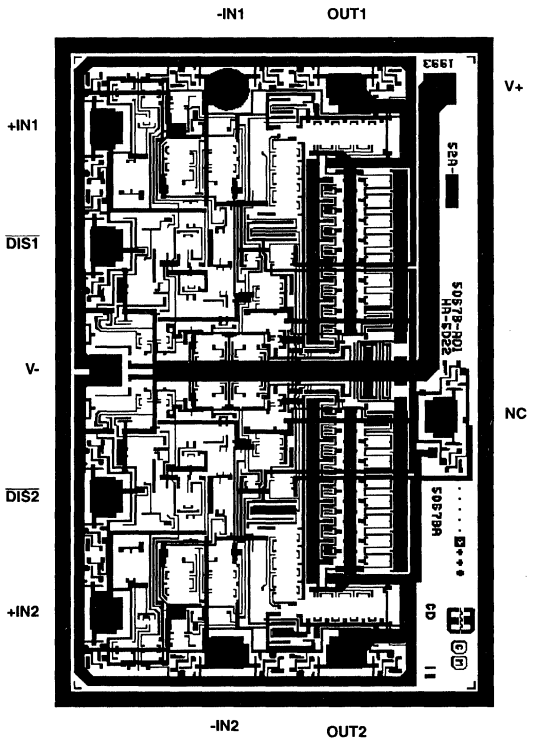
124

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA5022



HARRIS SEMICONDUCTOR

HA5023

Dual 125MHz Video Current Feedback Amplifier

November 1996

Features

- Wide Unity Gain Bandwidth 125MHz
- Slew Rate 475V/μs
- Input Offset Voltage 800μV
- Differential Gain 0.03%
- Differential Phase ..... 0.03 Degrees
- Supply Current (per Amplifier) 7.5mA
- ESD Protection 4000V
- Guaranteed Specifications at ±5V Supplies

Applications

- Video Gain Block
- Video Distribution Amplifier/RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter
- Medical Imaging
- Radar and Imaging Systems
- Video Switching and Routing

Description

The HA5023 is a wide bandwidth high slew rate dual amplifier optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

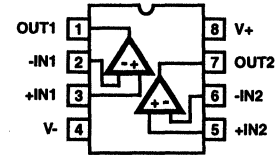
The performance of the HA5023 is very similar to the popular Harris HA-5020.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA5023IP	-40 to 85	8 Ld PDIP	E8.3
HA5023IB (H5023I)	-40 to 85	8 Ld SOIC	M8.15
HA5023EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HA5023
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 3393.5

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
DC Input Voltage (Note 3) . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage. 10V
Output Current (Note 4) . . . . . Short Circuit Protected
ESD Rating (Note 3)
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 2000V

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage Range (Typical) . . . . . ±4.5V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	130
SOIC Package	160

Maximum Junction Temperature (Note 1) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package, Note 1) . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175^oC for die, and below 150^oC for plastic packages. See Application Information section for safe operating area information.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. The non-inverting input of unused amplifiers must be connected to GND.
4. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (V_{IO})		A	25	-	0.8	3	mV
		A	Full	-	-	5	mV
Delta V_{IO} Between Channels		A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift		B	Full	-	5	-	$\mu V/^oC$
V_{IO} Common Mode Rejection Ratio	Note 5	A	25	53	-	-	dB
		A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio	$\pm3.5V \leq V_S \leq \pm6.5V$	A	25	60	-	-	dB
		A	Full	55	-	-	dB
Input Common Mode Range	Note 5	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current		A	25	-	3	8	µA
		A	Full	-	-	20	µA
+IN Common Mode Rejection ($+I_{BCMR} = \frac{1}{+R_{IN}}$)	Note 5	A	25	-	-	0.15	µA/V
		A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection	$\pm3.5V \leq V_S \leq \pm6.5V$	A	25	-	-	0.1	µA/V
		A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current		A	25, 85	-	4	12	µA
		A	-40	-	10	30	µA
Delta -IN BIAS Current Between Channels		A	25, 85	-	6	15	µA
		A	-40	-	10	30	µA

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
-IN Common Mode Rejection	Note 5	A	25	-	-	0.4	µA/V
		A	Full	-	-	1.0	µA/V
-IN Power Supply Rejection	$\pm3.5V \leq V_S \leq \pm6.5V$	A	25	-	-	0.2	µA/V
		A	Full	-	-	0.5	µA/V
Input Noise Voltage	f = 1kHz	B	25	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current	f = 1kHz	B	25	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current	f = 1kHz	B	25	-	25.0	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Transimpedence	Note 11	A	25	1.0	-	-	MΩ
		A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain	$R_L = 400\Omega$, $V_{OUT} = \pm2.5V$	A	25	70	-	-	dB
		A	Full	65	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm2.5V$	A	25	50	-	-	dB
		A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing	$R_L = 150\Omega$	A	25	±2.5	±3.0	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	$R_L = 150\Omega$	B	Full	±16.6	±20.0	-	mA
Output Current, Short Circuit	$V_{IN} = \pm2.5V$, $V_{OUT} = 0V$	A	Full	±40	±60	-	mA
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		A	25	5	-	15	V
Quiescent Supply Current		A	Full	-	7.5	10	mA/Op Amp
AC CHARACTERISTICS ($A_V = +1$)							
Slew Rate	Note 6	B	25	275	350	-	V/µs
Full Power Bandwidth	Note 7	B	25	22	28	-	MHz
Rise Time	Note 8	B	25	-	6	-	ns
Fall Time	Note 8	B	25	-	6	-	ns
Propagation Delay	Note 8	B	25	-	6	-	ns
Overshoot		B	25	-	4.5	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	75	-	ns

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)							
Slew Rate	Note 6	B	25	-	475	-	V/µs
Full Power Bandwidth	Note 7	B	25	-	26	-	MHz
Rise Time	Note 8	B	25	-	6	-	ns
Fall Time	Note 8	B	25	-	6	-	ns
Propagation Delay	Note 8	B	25	-	6	-	ns
Overshoot		B	25	-	12	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	100	-	ns
Gain Flatness	5MHz	B	25	-	0.02	-	dB
	20MHz	B	25	-	0.07	-	dB
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)							
Slew Rate	Note 6	B	25	350	475	-	V/µs
Full Power Bandwidth	Note 7	B	25	28	38	-	MHz
Rise Time	Note 8	B	25	-	8	-	ns
Fall Time	Note 8	B	25	-	9	-	ns
Propagation Delay	Note 8	B	25	-	9	-	ns
Overshoot		B	25	-	1.8	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	75	-	ns
Settling Time to 0.1%	2V Output Step	B	25	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (Note 10)	$R_L = 150\Omega$	B	25	-	0.03	-	%
Differential Phase (Note 10)	$R_L = 150\Omega$	B	25	-	0.03	-	Degrees

NOTES:

5. $V_{CM} = \pm2.5V$. At -40°C Product is tested at $V_{CM} = \pm2.25V$ because Short Test Duration does not allow self heating.
6. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
7. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 2V$.
8. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
9. A. Production Tested; B. Typical or Guaranteed Limit based on characterization; C. Design Typical for information only.
10. Measured with a VM700A video tester using an NTC-7 composite VITS.
11. $V_{OUT} = \pm2.5V$. At -40°C Product is tested at $V_{OUT} = \pm2.25V$ because Short Test Duration does not allow self heating.

Test Circuits and Waveforms

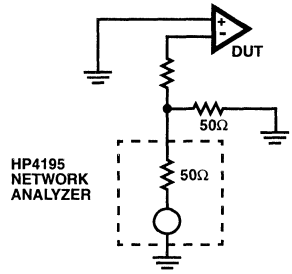


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

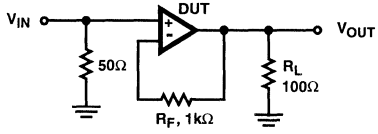


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

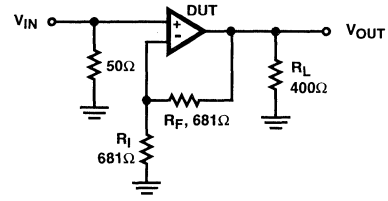
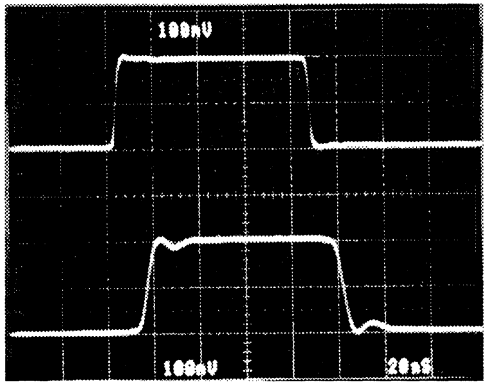
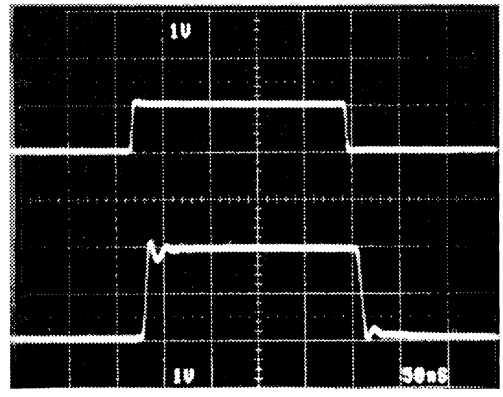


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

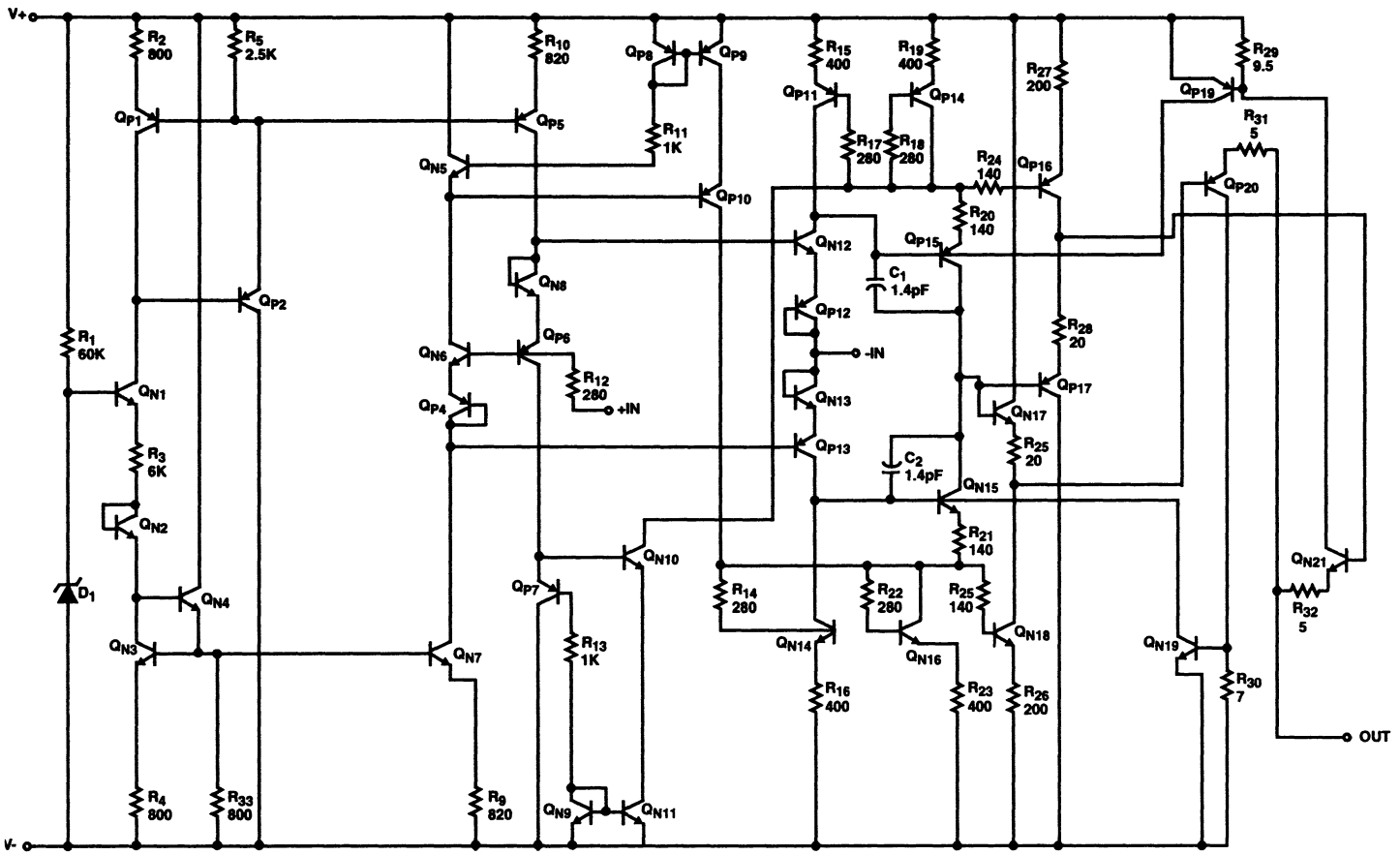
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic Diagram (One Amplifier of Two)



Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 8 and Figure 9 in the typical performance section, illustrate the performance of the HA5023 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5023 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10µF) tantalum or electrolytic capacitor in parallel with a small value (0.1µF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

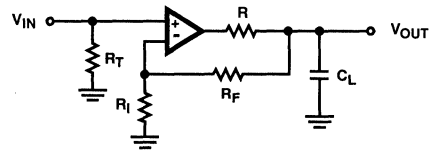


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (Plastic DIP, SOIC). At $\pm 5V_{DC}$ quiescent operation both package styles may be operated over the full industrial range of -40°C to 85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

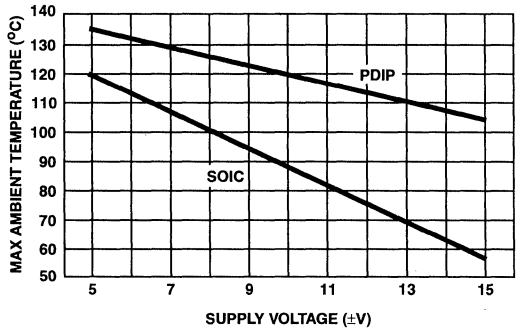


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

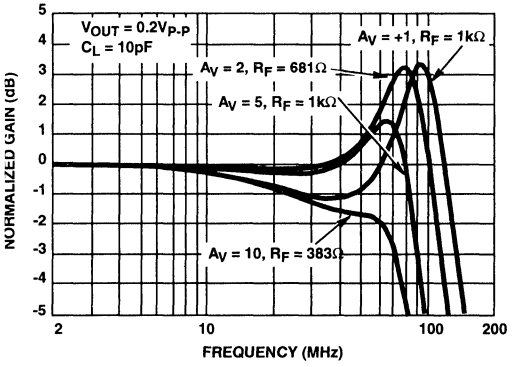


FIGURE 8. NON-INVERTING FREQENCY RESPONSE

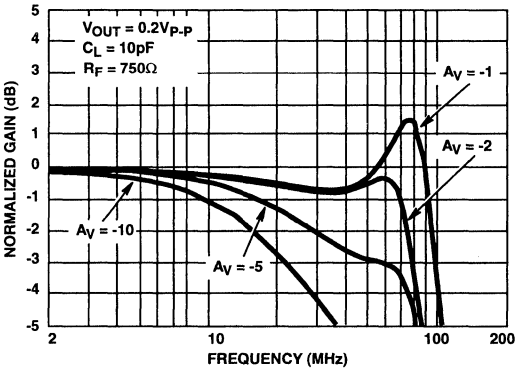


FIGURE 9. INVERTING FREQUENCY RESPONSE

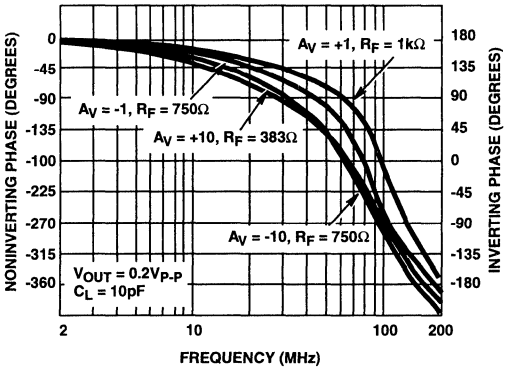


FIGURE 10. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

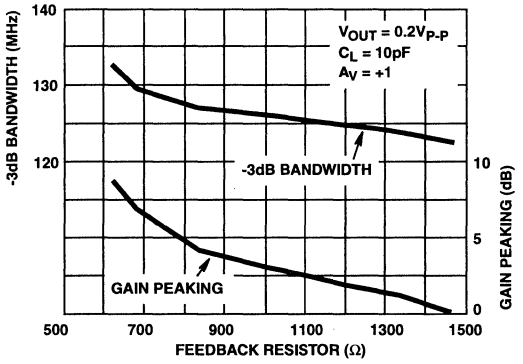


FIGURE 11. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

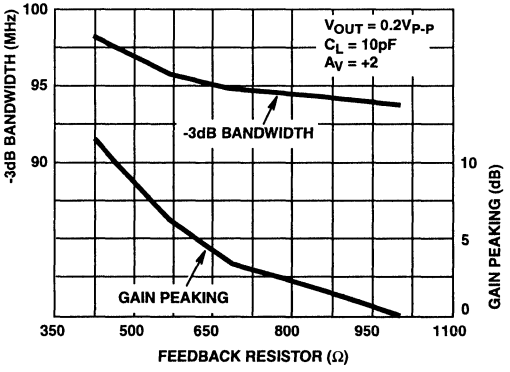


FIGURE 12. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

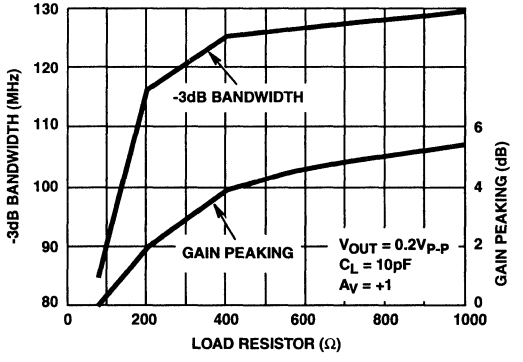


FIGURE 13. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

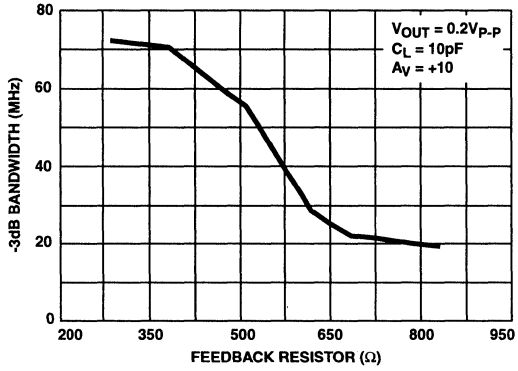


FIGURE 14. BANDWIDTH vs FEEDBACK RESISTANCE

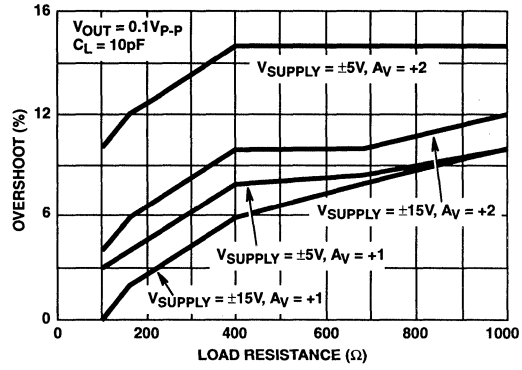


FIGURE 15. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

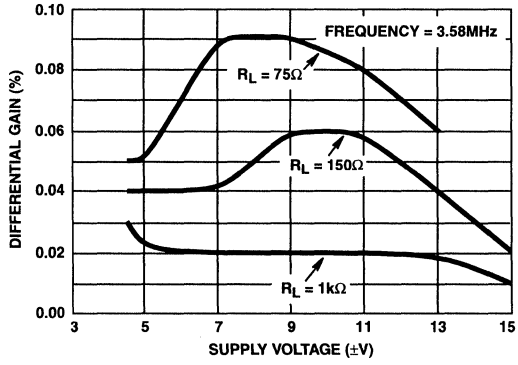


FIGURE 16. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

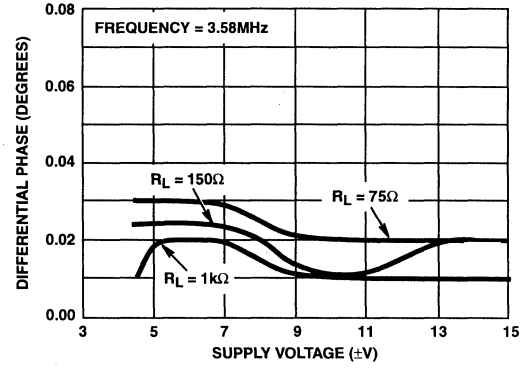


FIGURE 17. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

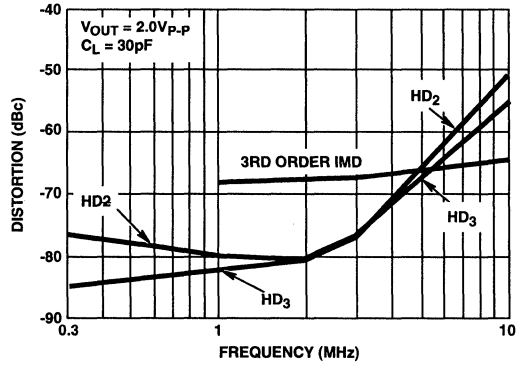


FIGURE 18. DISTORTION vs FREQUENCY

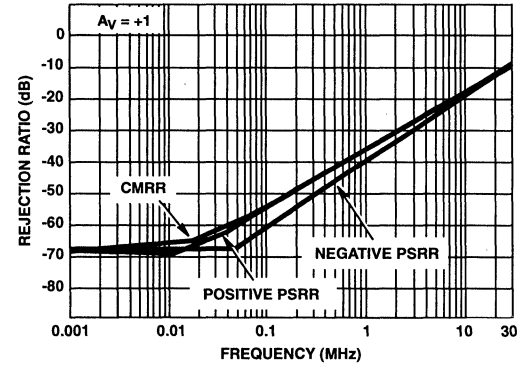


FIGURE 19. REJECTION RATIOS vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

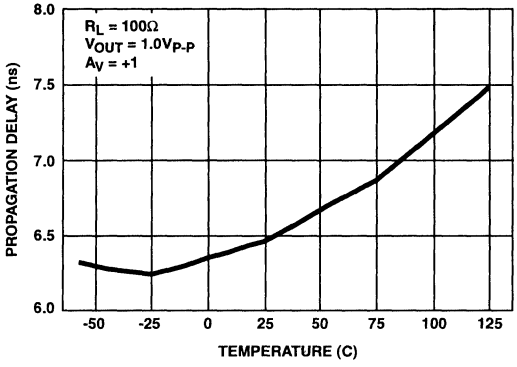


FIGURE 20. PROPAGATION DELAY vs TEMPERATURE

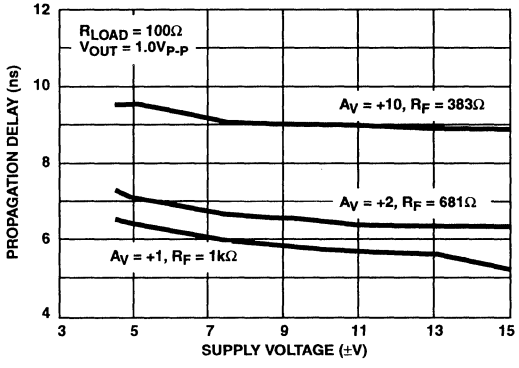


FIGURE 21. PROPAGATION DELAY vs SUPPLY VOLTAGE

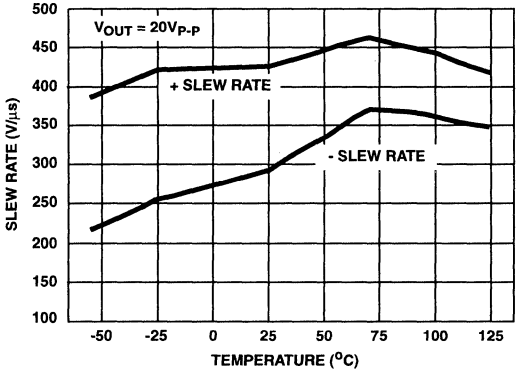


FIGURE 22. FIGURE 22. SLEW RATE vs TEMPERATURE

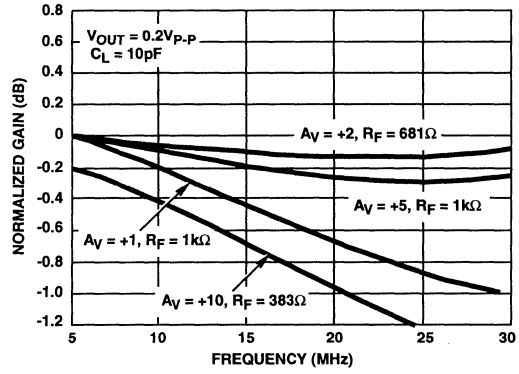


FIGURE 23. NON-INVERTING GAIN FLATNESS vs FREQUENCY

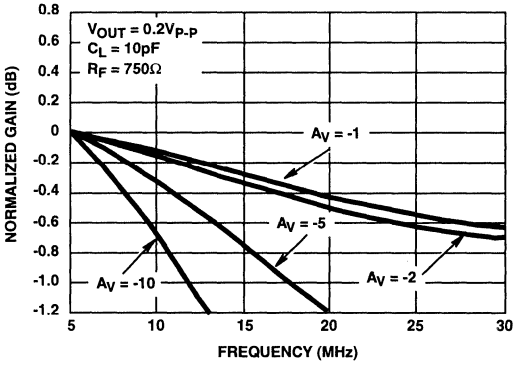


FIGURE 24. INVERTING GAIN FLATNESS vs FREQUENCY

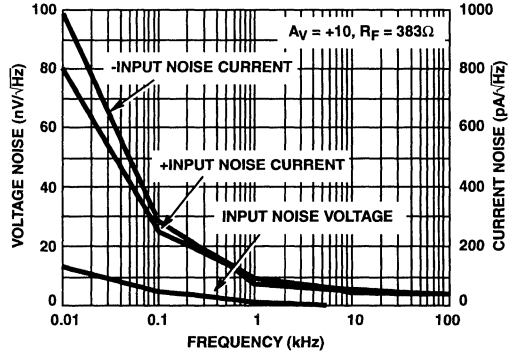


FIGURE 25. INPUT NOISE CHARACTERISTICS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

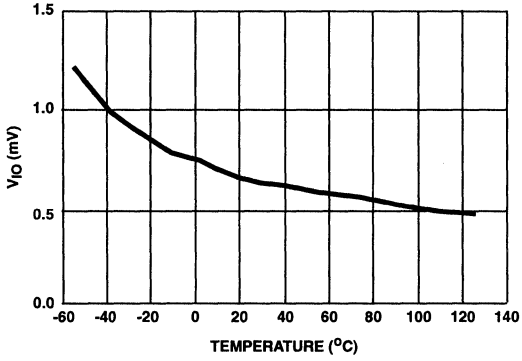


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE

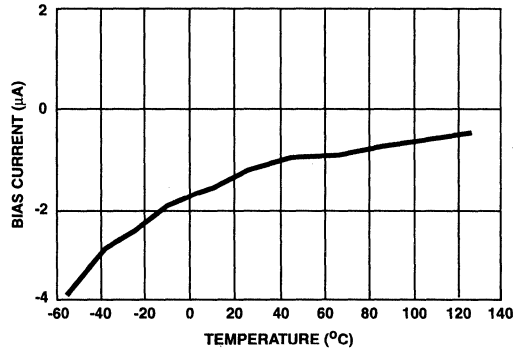


FIGURE 27. +INPUT BIAS CURRENT vs TEMPERATURE

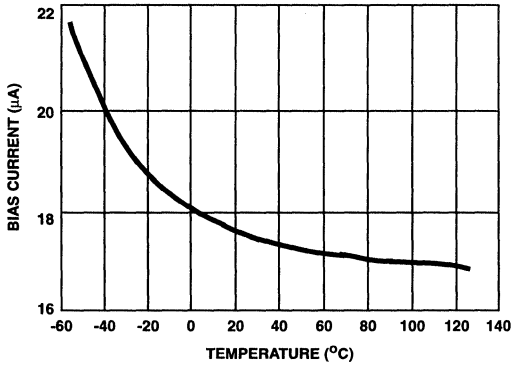


FIGURE 28. -INPUT BIAS CURRENT vs TEMPERATURE

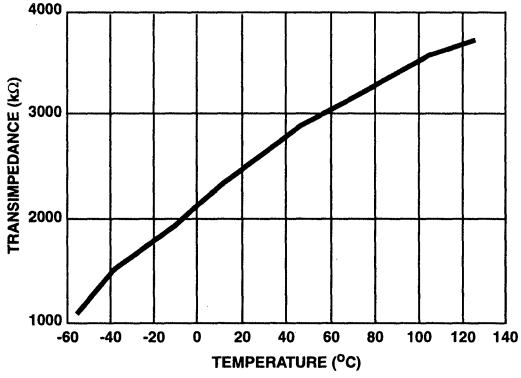


FIGURE 29. TRANSIMPEDANCE vs TEMPERATURE

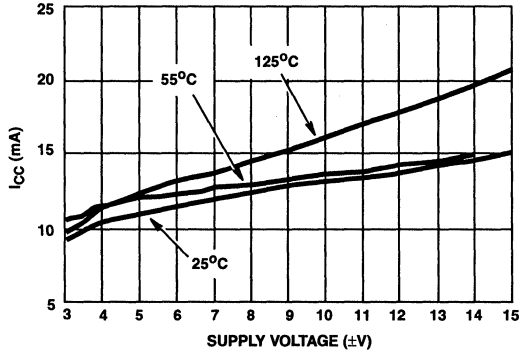


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

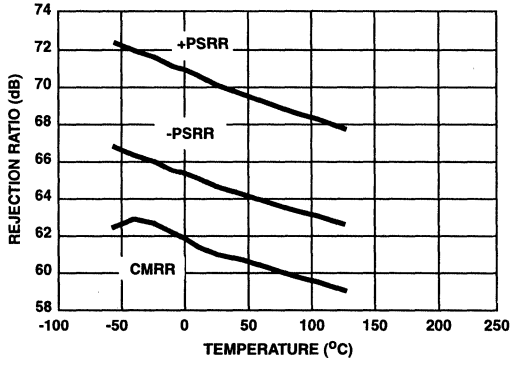


FIGURE 31. REJECTION RATIO vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

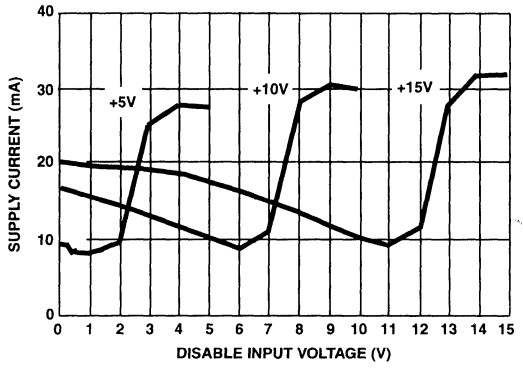


FIGURE 32. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

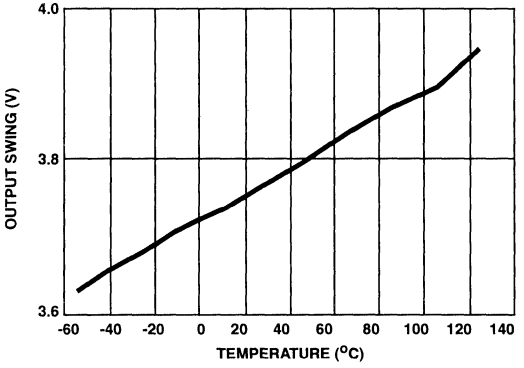


FIGURE 33. OUTPUT SWING vs TEMPERATURE

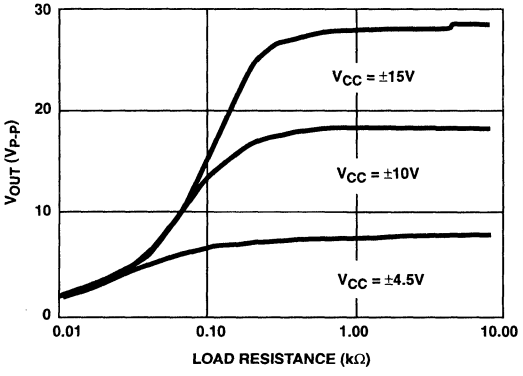


FIGURE 34. OUTPUT SWING vs LOAD RESISTANCE

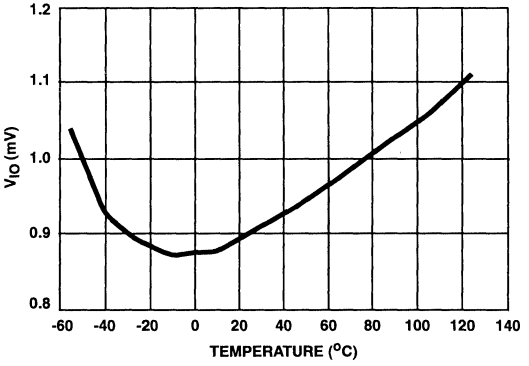


FIGURE 35. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

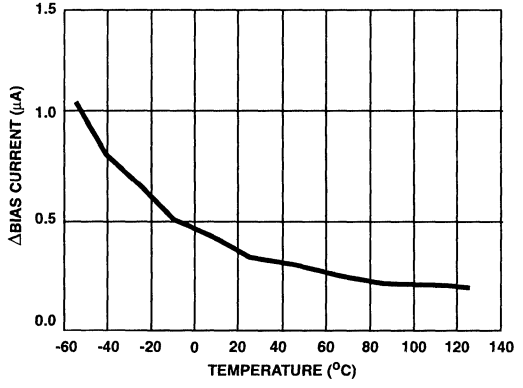


FIGURE 36. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

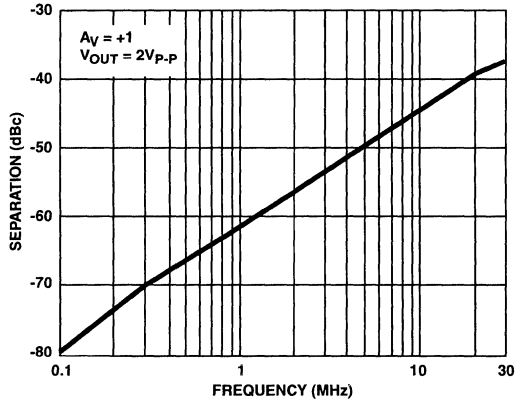


FIGURE 37. CHANNEL SEPARATION vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

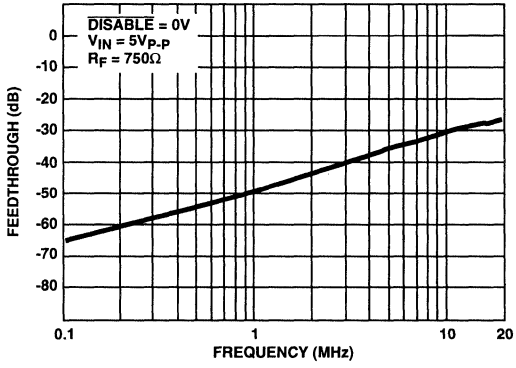


FIGURE 38. DISABLE FEEDTHROUGH vs FREQUENCY

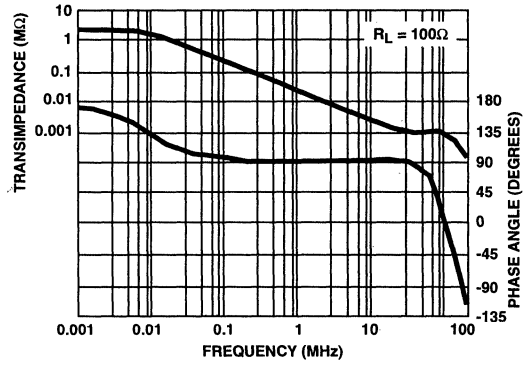


FIGURE 39. TRANSIMPEDANCE vs FREQUENCY

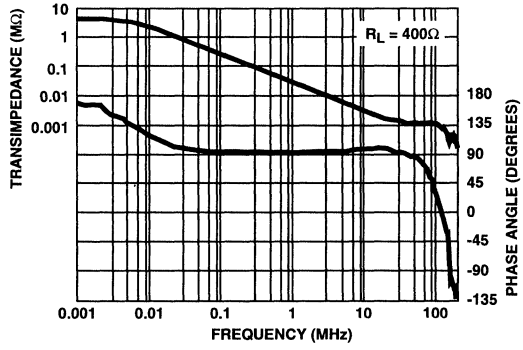


FIGURE 40. TRANSIMPEDENCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

1650µm x 2540µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.4kÅ

TRANSISTOR COUNT:

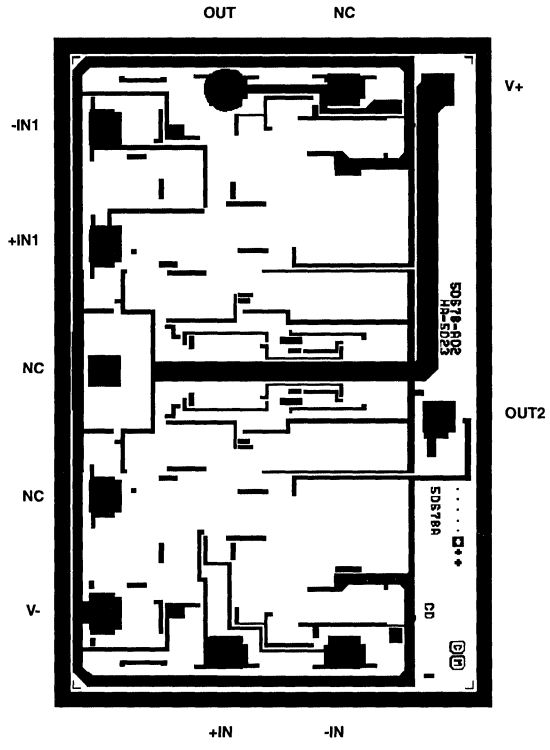
124

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA5023



HARRIS SEMICONDUCTOR

HA5024

Quad 125MHz Video Current Feedback Amplifier with Disable

November 1996

Features

- Quad Version of HA-5020
- Individual Output Enable/Disable
- Input Offset Voltage 800µV
- Wide Unity Gain Bandwidth 125MHz
- Slew Rate 475V/µs
- Differential Gain 0.03%
- Differential Phase ..... 0.03 Degrees
- Supply Current (per Amplifier) 7.5mA
- ESD Protection 4000V
- Guaranteed Specifications at ±5V Supplies

Applications

- Video Multiplexers; Video Switching and Routing
- Video Gain Block
- Video Distribution Amplifier/RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter
- Medical Imaging
- Radar and Imaging Systems

Description

The HA5024 is a quad version of the popular Harris HA5020. It features wide bandwidth and high slew rate, and is optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The HA5024 also features a disable function that significantly reduces supply current while forcing the output to a true high impedance state. This functionality allows 2:1 and 4:1 video multiplexers to be implemented with a single IC.

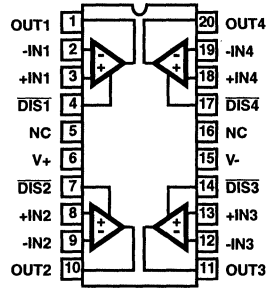
The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA5024IP	-40 to 85	20 Ld PDIP	E20.3
HA5024IB	-40 to 85	20 Ld SOIC	M20.3
HA5024EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HA5024
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3550.3**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
DC Input Voltage (Note 3) . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage. 10V
Output Current (Note 4) . . . . . Short Circuit Protected
ESD Rating (Note 3)
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 2000V

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage Range (Typical) . . . . . $\pm 4.5V$ to $\pm 15V$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	75
SOIC Package	90

Maximum Junction Temperature (Note 1) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package, Note 1) . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175^oC for die, and below 150^oC for plastic packages. See Application Information section for safe operating area information.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. The non-inverting input of unused amplifiers must be connected to GND.
4. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.

Electrical Specifications

$V_{SUPPLY} = \pm 5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 11) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (V_{IO})		A	25	-	0.8	3	mV
		A	Full	-	-	5	mV
Delta V_{IO} Between Channels		A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift		B	Full	-	5	-	$\mu V/^oC$
V_{IO} Common Mode Rejection Ratio	Note 5	A	25	53	-	-	dB
		A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	60	-	-	dB
		A	Full	55	-	-	dB
Input Common Mode Range	Note 5	A	Full	± 2.5	-	-	V
Non-Inverting Input (+IN) Current		A	25	-	3	8	μA
		A	Full	-	-	20	μA
+IN Common Mode Rejection ($+I_{BCMR} = \frac{1}{R_{IN}}$)	Note 5	A	25	-	-	0.15	$\mu A/V$
		A	Full	-	-	0.5	$\mu A/V$
+IN Power Supply Rejection	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	-	-	0.1	$\mu A/V$
		A	Full	-	-	0.3	$\mu A/V$
Inverting Input (-IN) Current		A	25,85	-	4	12	μA
		A	-40	-	10	30	μA
Delta -IN BIAS Current Between Channels		A	25,85	-	6	15	μA
		A	-40	-	10	30	μA
-IN Common Mode Rejection	Note 5	A	25	-	-	0.4	$\mu A/V$
		A	Full	-	-	1.0	$\mu A/V$
-IN Power Supply Rejection	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	-	-	0.2	$\mu A/V$
		A	Full	-	-	0.5	$\mu A/V$

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 11) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Input Noise Voltage	f = 1kHz	B	25	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current	f = 1kHz	B	25	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current	f = 1kHz	B	25	-	25.0	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Transimpedence	Note 16	A	25	1.0	-	-	MΩ
		A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain	$R_L = 400\Omega$, $V_{OUT} = \pm2.5V$	25A	25	70	-	-	dB
		A	Full	65	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm2.5V$	A	25	50	-	-	dB
		A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing	$R_L = 150\Omega$	A	25	±2.5	±3.0	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	$R_L = 150\Omega$	B	Full	±16.6	±20.0	-	mA
Output Current, Short Circuit	$V_{IN} = \pm2.5V$, $V_{OUT} = 0V$	A	Full	±40	±60	-	mA
Output Current, Disabled (Note 5)	$\overline{DISABLE} = 0V$, $V_{OUT} = \pm2.5V$, $V_{IN} = 0V$	A	Full	-	-	2	µA
Output Disable Time	Note 12	B	25	-	40	-	µs
Output Enable Time	Note 13	B	25	-	40	-	ns
Output Capacitance Disabled	Note 14	B	25	-	15	-	pF
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		A	25	5	-	15	V
Quiescent Supply Current		A	Full	-	7.5	10	mA/Op Amp
Supply Current, Disabled	$\overline{DISABLE} = 0V$	A	Full	-	5	7.5	mA/Op Amp
$\overline{Disable}$ Pin Input Current	$\overline{DISABLE} = 0V$	A	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable	Note 6	A	Full	350	-	-	µA
Maximum Pin 8 Current to Enable	Note 7	A	Full	-	-	20	µA
AC CHARACTERISTICS ($A_V = +1$)							
Slew Rate	Note 8	B	25	275	350	-	V/µs
Full Power Bandwidth	Note 9	B	25	22	28	-	MHz
Rise Time	Note 10	B	25	-	6	-	ns
Fall Time	Note 10	B	25	-	6	-	ns
Propagation Delay	Note 10	B	25	-	6	-	ns
Overshoot		B	25	-	4.5	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	75	-	ns
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)							
Slew Rate	Note 8	B	25	-	475	-	V/µs
Full Power Bandwidth	Note 9	B	25	-	26	-	MHz

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 11) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Rise Time	Note 10	B	25	-	6	-	ns
Fall Time	Note 10	B	25	-	6	-	ns
Propagation Delay	Note 10	B	25	-	6	-	ns
Overshoot		B	25	-	12	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	100	-	ns
Gain Flatness	5MHz	B	25	-	0.02	-	dB
	20MHz	B	25	-	0.07	-	dB
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)							
Slew Rate	Note 8	B	25	350	475	-	V/µs
Full Power Bandwidth	Note 9	B	25	28	38	-	MHz
Rise Time	Note 10	B	25	-	8	-	ns
Fall Time	Note 10	B	25	-	9	-	ns
Propagation Delay	Note 10	B	25	-	9	-	ns
Overshoot		B	25	-	1.8	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	75	-	ns
Settling Time to 0.1%	2V Output Step	B	25	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (Note 15)	$R_L = 150\Omega$	B	25	-	0.03	-	%
Differential Phase (Note 15)	$R_L = 150\Omega$	B	25	-	0.03	-	Degrees

NOTES:

5. $V_{CM} = \pm2.5V$. At -40°C Product is tested at $V_{CM} = \pm2.25V$ because short test duration does not allow self heating.
6. $R_L = 100\Omega$, $V_{IN} = 2.5V$. This is the minimum current which must be pulled out of the $\overline{\text{Disable}}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
7. $V_{IN} = 0V$. This is the maximum current that can be pulled out of the $\overline{\text{Disable}}$ pin with the HA5024 remaining enabled. The HA5024 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
9. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 2V$.
10. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. A. Production Tested; B. Typical or Guaranteed Limit based on characterization; C. Design Typical for information only.
12. $V_{IN} = +2V$, $\overline{\text{DISABLE}} = +5V$ to 0V. Measured from the 50% point of $\overline{\text{DISABLE}}$ to $V_{OUT} = 0V$.
13. $V_{IN} = +2V$, $\overline{\text{DISABLE}} = 0V$ to +5V. Measured from the 50% point of $\overline{\text{DISABLE}}$ to $V_{OUT} = 2V$.
14. $V_{IN} = 0V$, Force V_{OUT} from 0V to ±2.5V, $t_R = t_F = 50ns$, $\overline{\text{DISABLE}} = 0V$.
15. Measured with a VM700A video tester using an NTC-7 composite VITS.
16. $V_{OUT} = \pm2.5V$. At -40°C Product is tested at $V_{OUT} = \pm2.25V$ because short test duration does not allow self heating.

Test Circuits and Waveforms

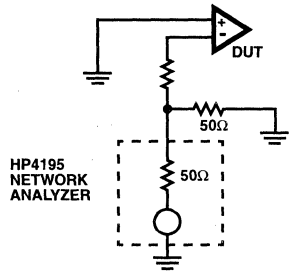


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

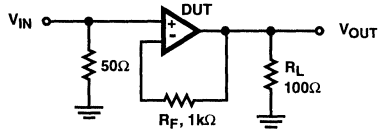


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

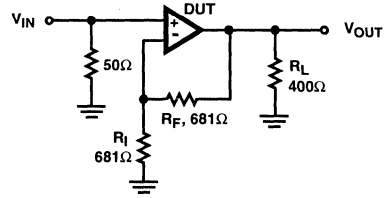
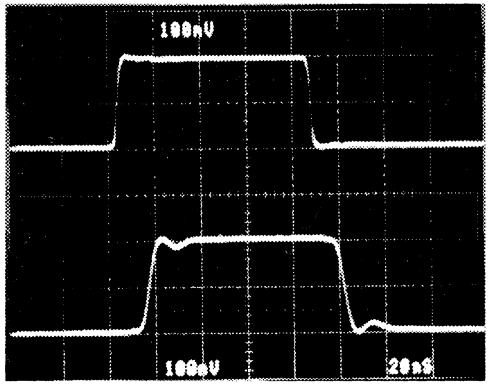
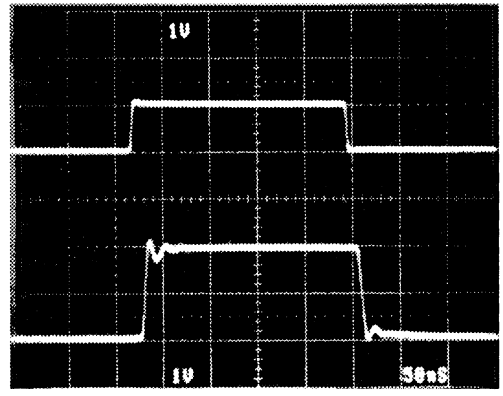


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

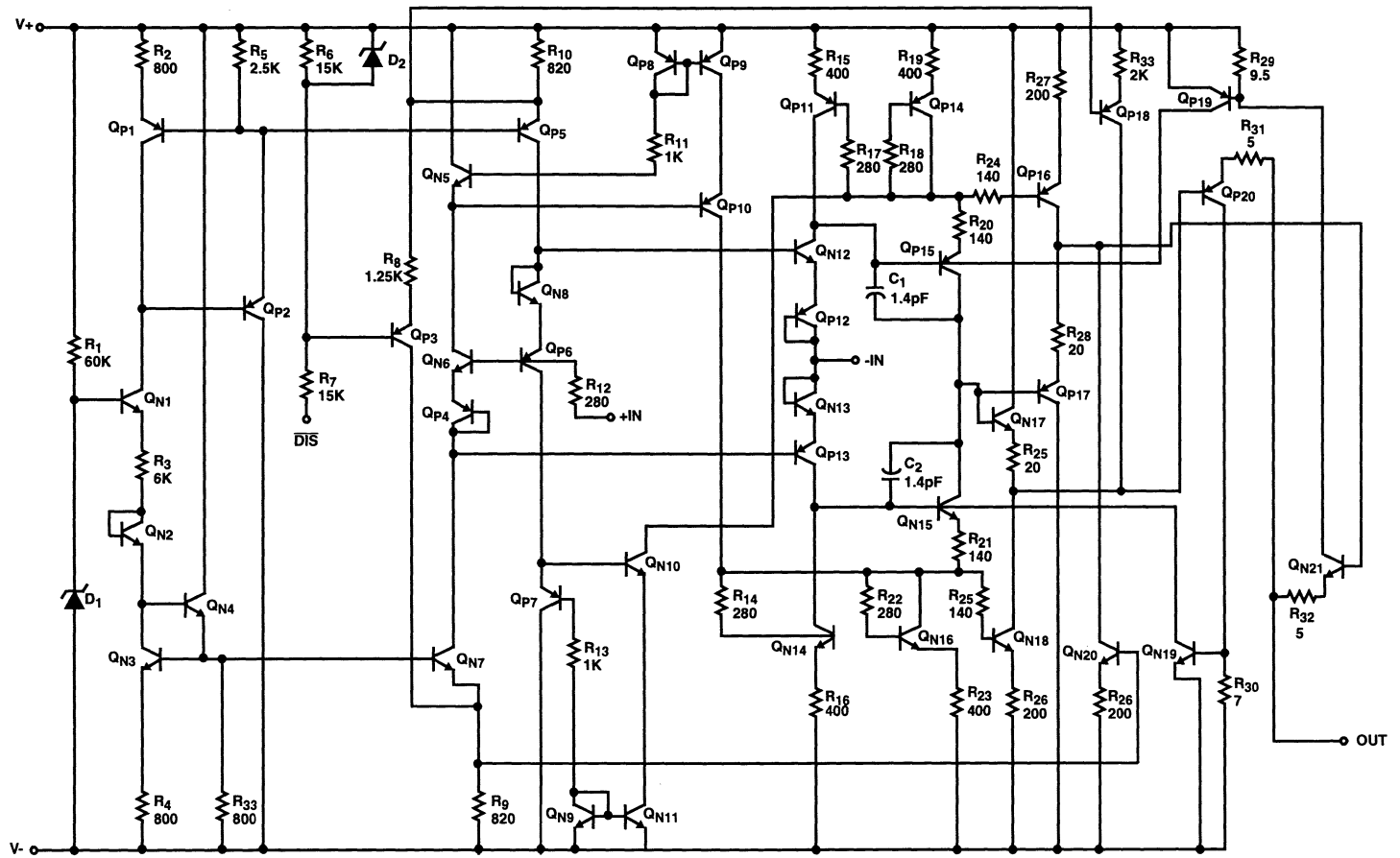
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic (One Amplifier of Four)



Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 11 and Figure 12 in the Typical Performance Curves section, illustrate the performance of the HA5024 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5024 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10μF) tantalum or electrolytic capacitor in parallel with a small value (0.1μF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

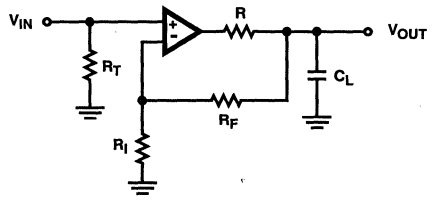


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resister is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (Plastic DIP, SOIC). At $\pm 5V_{DC}$ quiescent operation both package styles may be operated over the full industrial range of -40°C to 85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

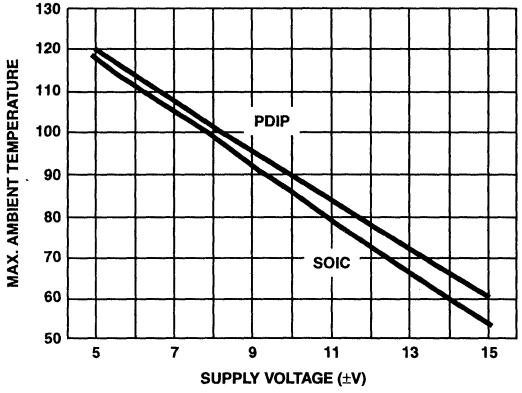


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Enable/Disable Function

When enabled the amplifier functions as a normal current feedback amplifier with all of the data in the electrical specifications table being valid and applicable. When disabled the amplifier output assumes a true high impedance state and the supply current is reduced significantly.

The circuit shown in Figure 8 is a simplified schematic of the enable/disable function. The large value resistors in series with the DISABLE pin makes it appear as a current source to the driver. When the driver pulls this pin low current flows out of the pin and into the driver. This current, which may be as large as 350μA when external circuit and process variables are at their extremes, is required to insure that point "A" achieves the proper potential to disable the output.The driver must have the compliance and capability of sinking all of this current.

When V_{CC} is +5V the DISABLE pin may be driven with a dedicated TTL gate. The maximum low level output voltage of the TTL gate, 0.4V, has enough compliance to insure that the amplifier will always be disabled even though D_1 will not turn on, and the TTL gate will sink enough current to keep point "A" at its proper voltage. When V_{CC} is greater than +5V the DISABLE pin should be driven with an open collector device that has a breakdown rating greater than V_{CC}.

Referring to Figure 8, it can be seen that R_6 will act as a pull-up resistor to $+V_{CC}$ if the DISABLE pin is left open. In those cases where the enable/disable function is not required on all circuits some circuits can be permanently enabled by letting the DISABLE pin float. If a driver is used to set the enable/disable level, be sure that the driver does not sink more than 20μA when the DISABLE pin is at a high level. TTL gates, especially CMOS versions, do not violate this criteria so it is permissible to control the enable/disable function with TTL.

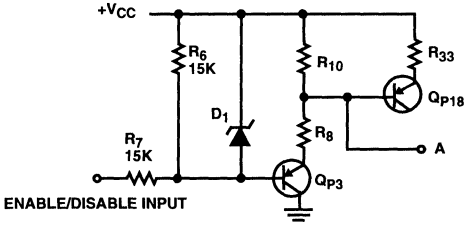


FIGURE 8. SIMPLIFIED SCHEMATIC OF ENABLE/DISABLE FUNCTION

Typical Applications

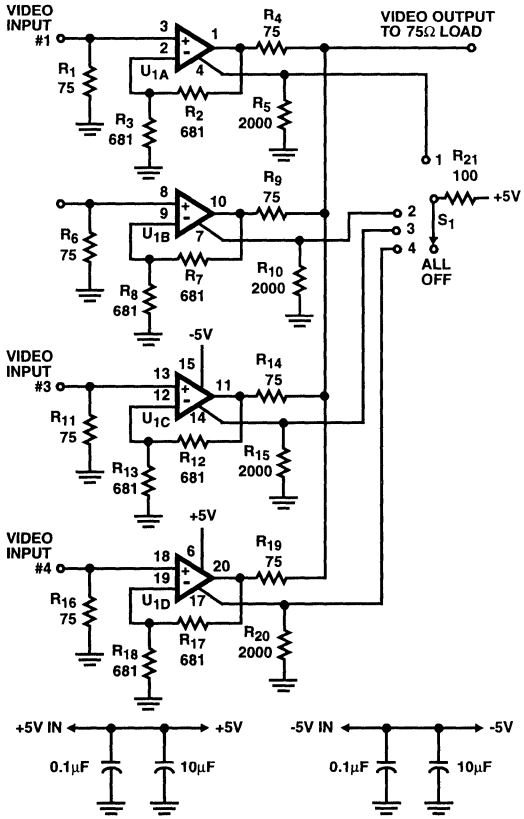
Four Channel Video Multiplexer

Referring to the amplifier U_{1A} in Figure 9, R_1 terminates the cable in its characteristic impedance of 75Ω, and R_4 back terminates the cable in its characteristic impedance. The amplifier is set up in a gain configuration of +2 to yield an overall network gain of +1 when driving a double terminated cable. The value of R_3 can be changed if a different network gain is desired. R_5 holds the disable pin at ground thus inhibiting the amplifier until the switch, S_1, is thrown to position 1. At position 1 the switch pulls the disable pin up to the plus supply rail thereby enabling the amplifier. Since all of the actual signal switching takes place within the amplifier, its differential gain and phase parameters, which are 0.03% and 0.03 degrees respectively, determine the circuit's performance. The other three circuits, U_{1B} through U_{1D}, operate in a similar manner.

When the plus supply rail is 5V the disable pin can be driven by a dedicated TTL gate as discussed earlier. If a multiplexer IC or its equivalent is used to select channels its logic must be break before make. When these conditions are satisfied the HA5024IP is often used as a remote video multiplexer, and the multiplexer may be extended by adding more amplifier ICs.

Low Impedance Multiplexer

Two common problems surface when you try to multiplex multiple high speed signals into a low impedance source such as an A/D converter. The first problem is the low source impedance which tends to make amplifiers oscillate and causes gain errors. The second problem is the multiplexer which supplies no gain, introduces all kinds of distortion and limits the frequency response. Using op amps which have an enable/disable function, such as the HA5024, eliminates the multiplexer problems because the external mux chip is not needed, and the HA5024 can drive low impedance (large capacitance) loads if a series isolation resistor is used.



NOTES:

17. U_1 is HA5024IP.
18. All resistors in Ω.
19. S_1 is break before make.
20. Use ground plane.

FIGURE 9. FOUR CHANNEL VIDEO MULTIPLEXER

Referring to Figure 10, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications. Since the drivers usually are terminated in their characteristic impedance the input gain is 0.5, thus the amplifiers, U_2, are configured in a gain of +2 to set the circuit gain equal to one. Resistors R_2 and R_3 determine the amplifier gain, and if a different gain is desired R_2 should be changed according to the equation $G = (1 + R_3/R_2)$. R_3 sets the frequency response of the amplifier so you should refer to the manufacturers data sheet before changing its value. R_5, C_1 and D_1 are an asymmetrical charge/discharge time circuit which configures U_1 as a break before make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels the drive logic must be designed to be break before make. R_4 is enclosed in the feedback loop of the amplifier so that the large open loop amplifier gain of U_2 will present the load with a small closed loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown in Figure 10 was tested for the full range of capacitor values with no oscillations being observed; thus, problem one has been solved.The frequency and gain characteristics of the circuit are now those of the amplifier independent of any multiplexing action; thus, problem two has been solved. The multiplexer transition time is approximately 15µs with the component values shown.

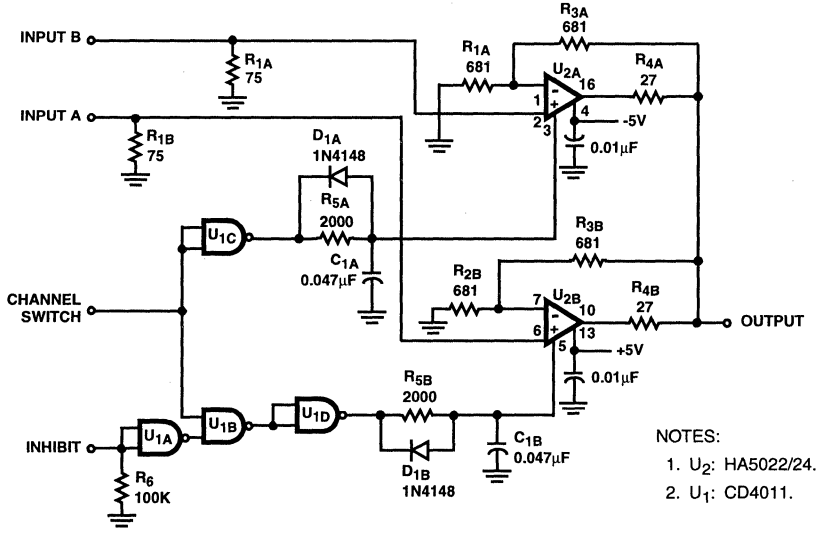


FIGURE 9. LOW IMPEDANCE MULTIPLEXER

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

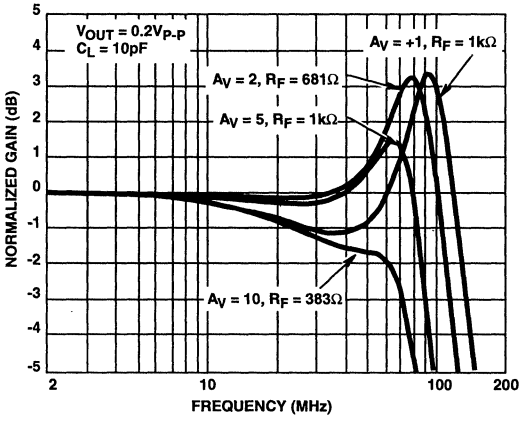


FIGURE 9. NON-INVERTING FREQUENCY RESPONSE

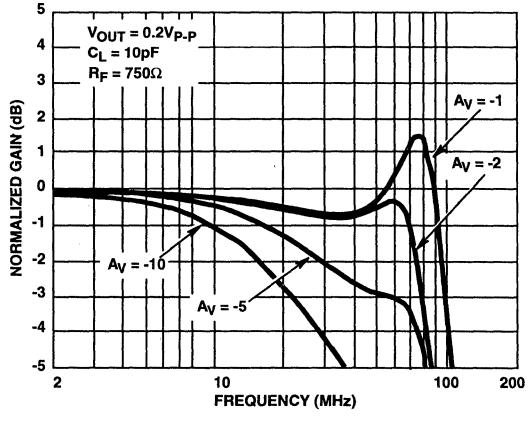


FIGURE 10. INVERTING FREQUENCY RESPONSE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

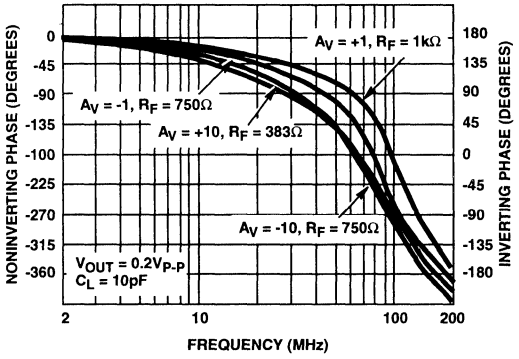


FIGURE 11. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

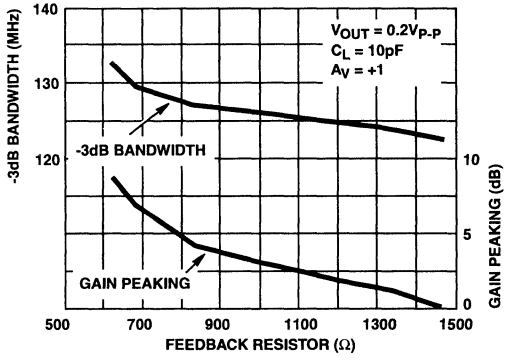


FIGURE 12. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

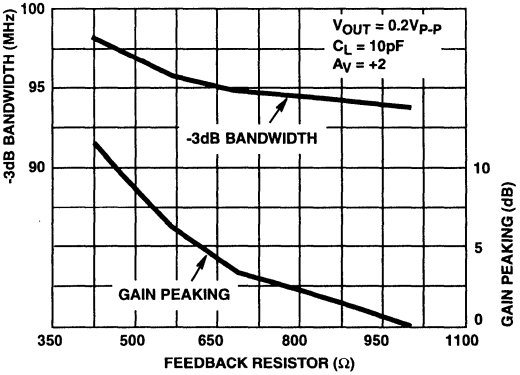


FIGURE 13. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

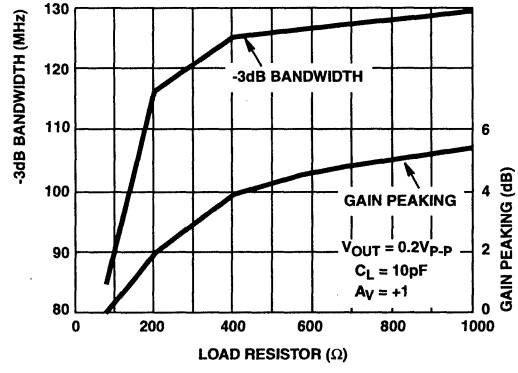


FIGURE 14. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

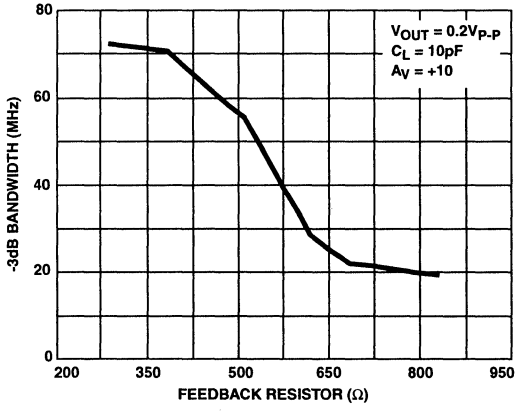


FIGURE 15. BANDWIDTH vs FEEDBACK RESISTANCE

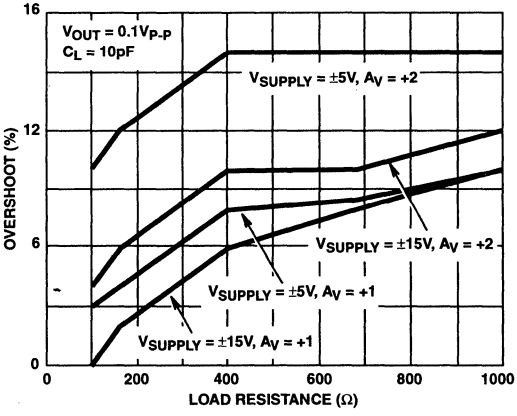


FIGURE 16. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

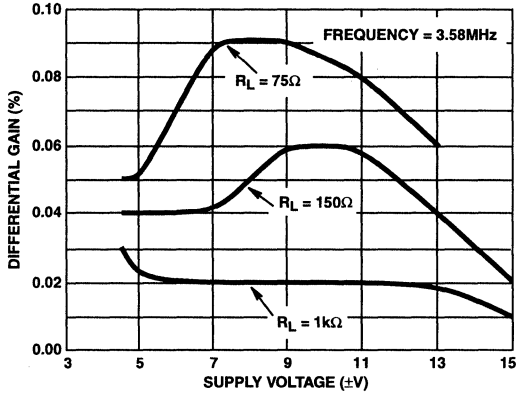


FIGURE 17. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

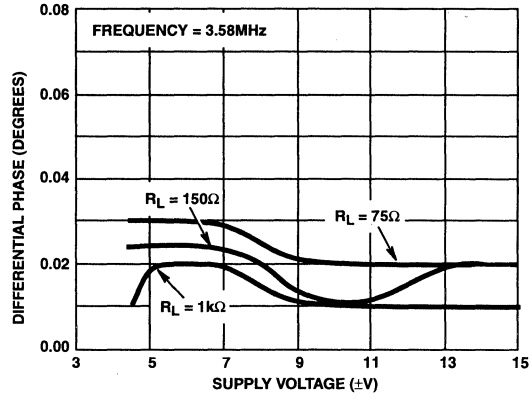


FIGURE 18. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

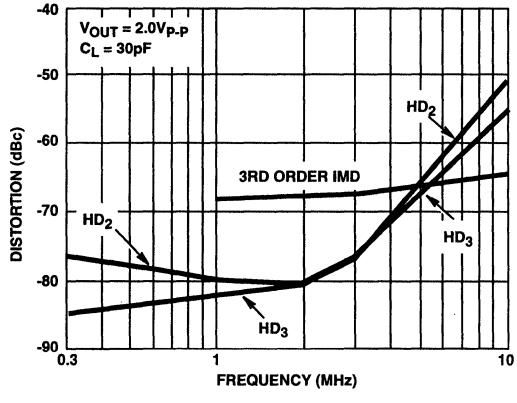


FIGURE 19. DISTORTION vs FREQUENCY

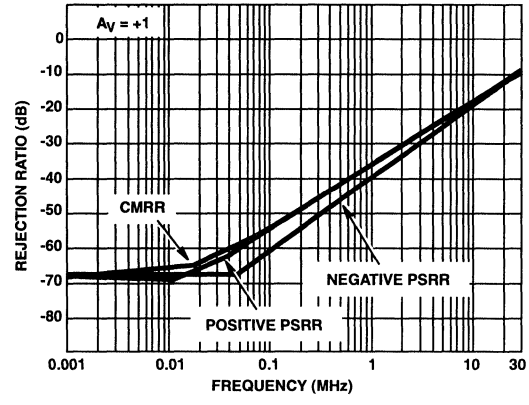


FIGURE 20. REJECTION RATIOS vs FREQUENCY

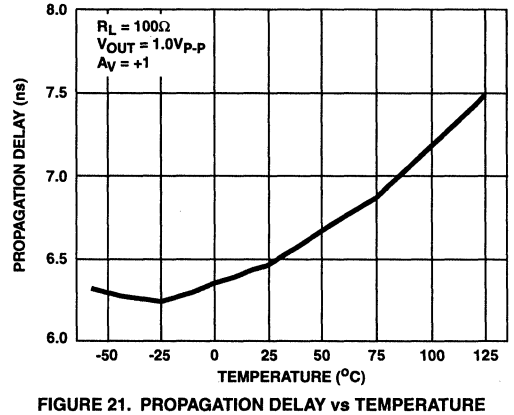


FIGURE 21. PROPAGATION DELAY vs TEMPERATURE

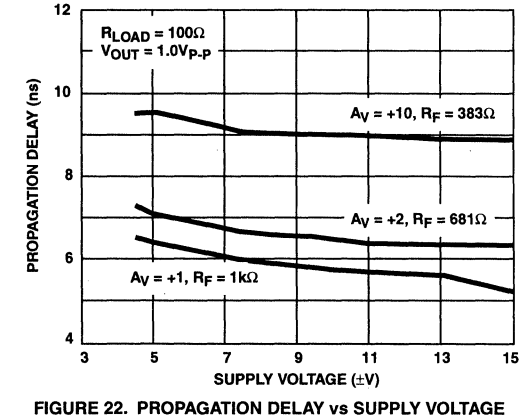


FIGURE 22. PROPAGATION DELAY vs SUPPLY VOLTAGE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

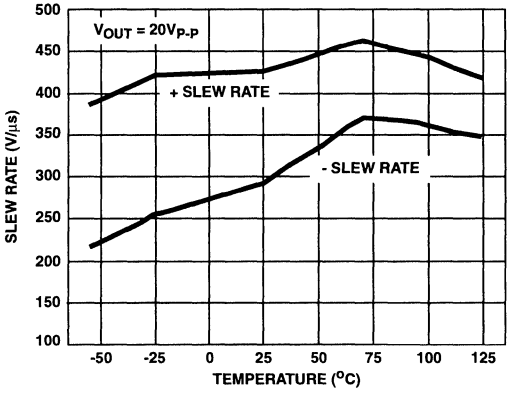


FIGURE 23. SLEW RATE vs TEMPERATURE

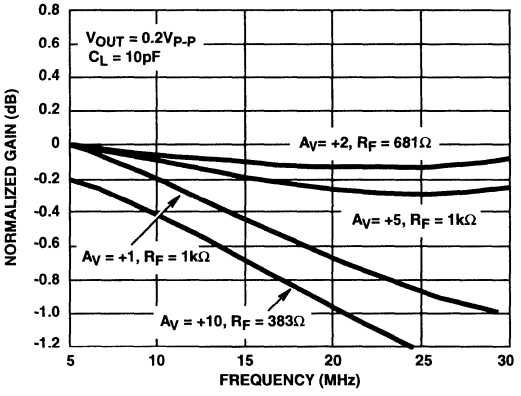


FIGURE 24. NON-INVERTING GAIN FLATNESS vs FREQUENCY

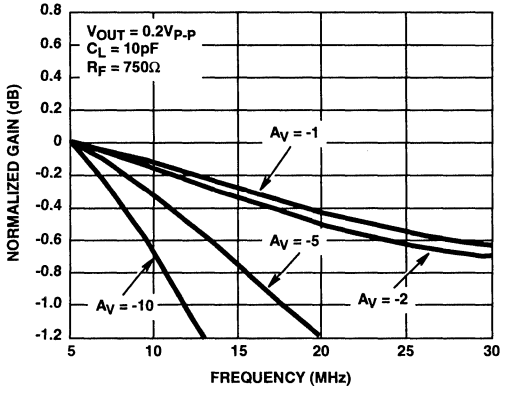


FIGURE 25. INVERTING GAIN FLATNESS vs FREQUENCY

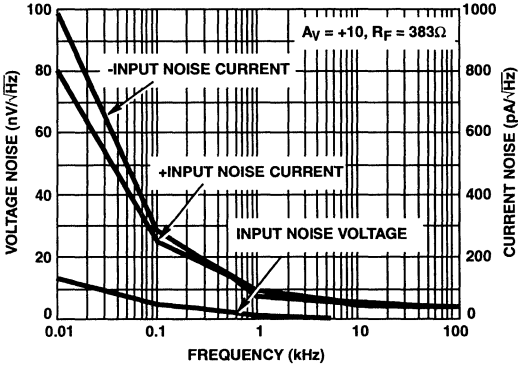


FIGURE 26. INPUT NOISE CHARACTERISTICS

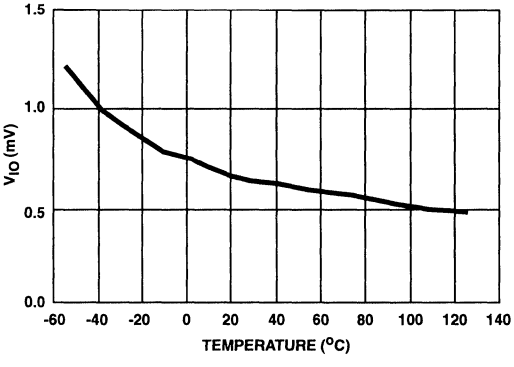


FIGURE 27. INPUT OFFSET VOLTAGE vs TEMPERATURE

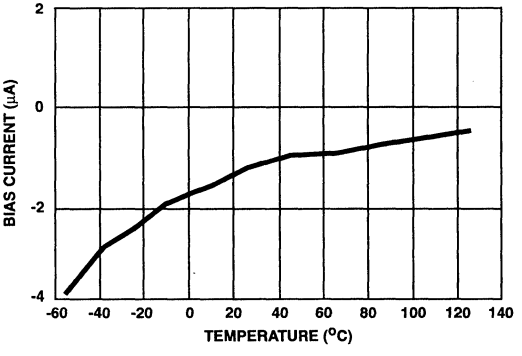


FIGURE 28. +INPUT BIAS CURRENT vs TEMPERATURE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

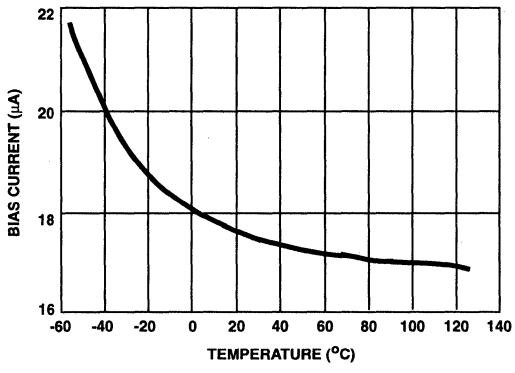


FIGURE 29. -INPUT BIAS CURRENT vs TEMPERATURE

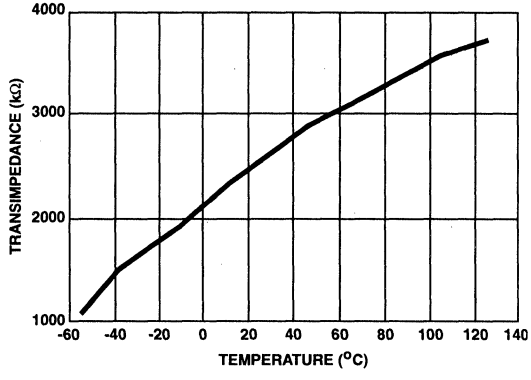


FIGURE 30. TRANSIMPEDANCE vs TEMPERATURE

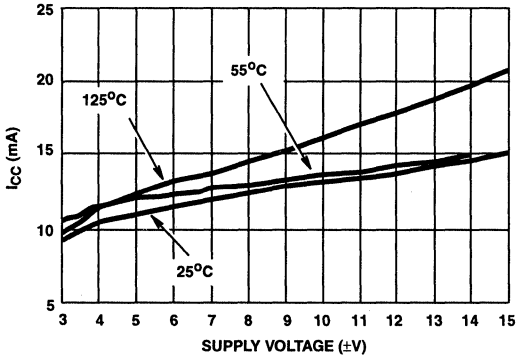


FIGURE 31. SUPPLY CURRENT vs SUPPLY VOLTAGE

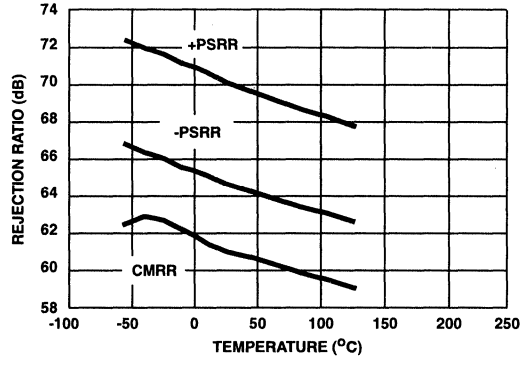


FIGURE 32. REJECTION RATIO vs TEMPERATURE

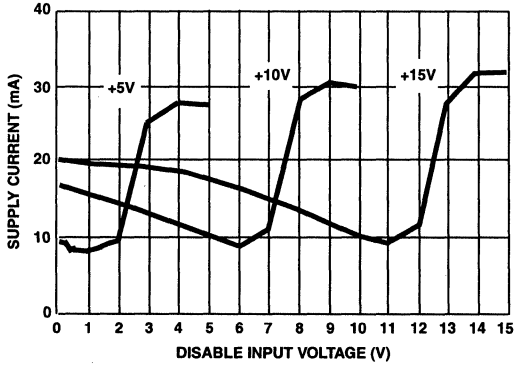


FIGURE 33. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

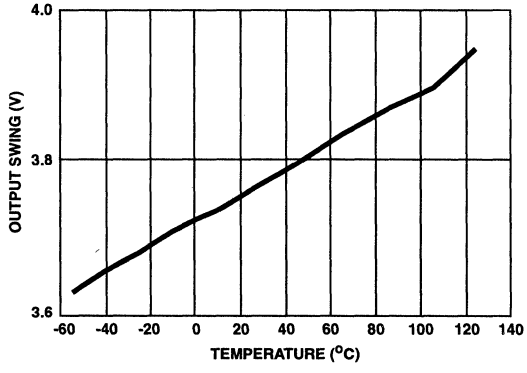


FIGURE 34. OUTPUT SWING vs TEMPERATURE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

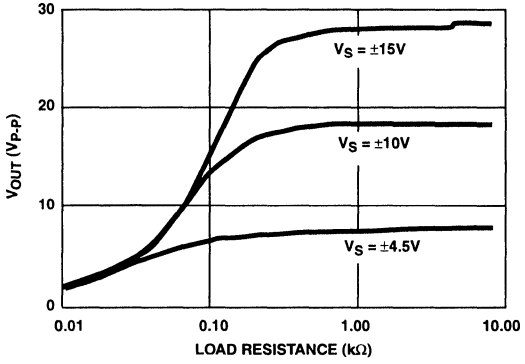


FIGURE 35. OUTPUT SWING vs LOAD RESISTANCE

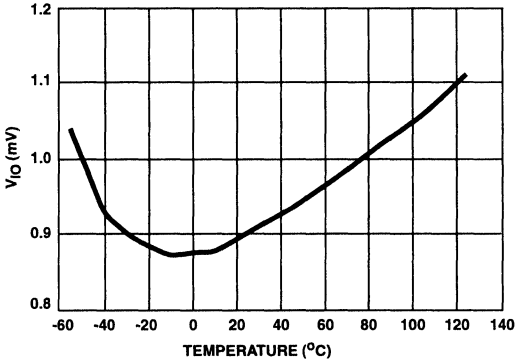


FIGURE 36. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

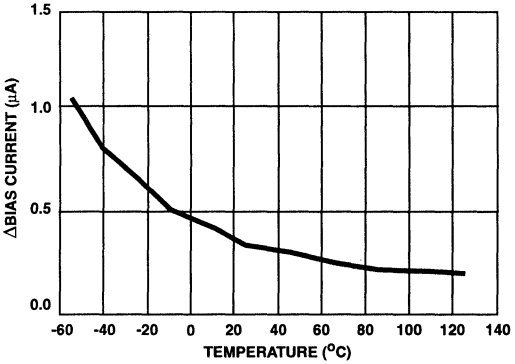


FIGURE 37. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

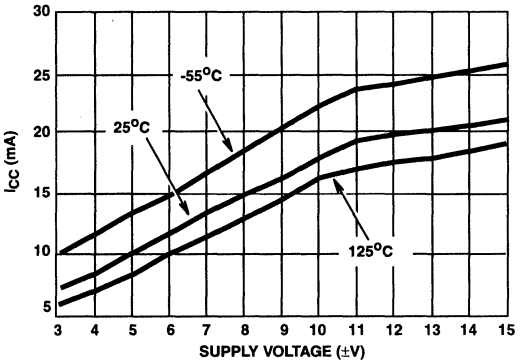


FIGURE 38. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE

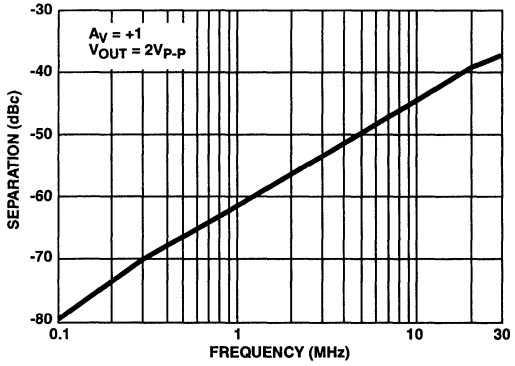


FIGURE 39. CHANNEL SEPARATION vs FREQUENCY

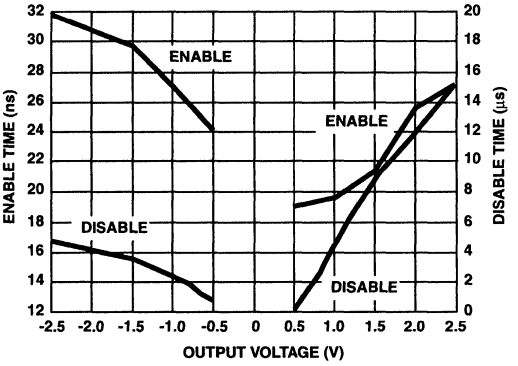


FIGURE 40. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

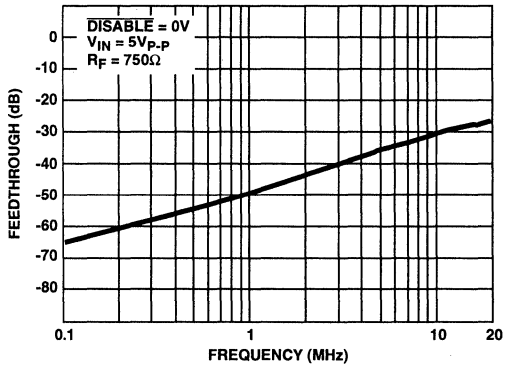


FIGURE 41. DISABLE FEEDTHROUGH vs FREQUENCY

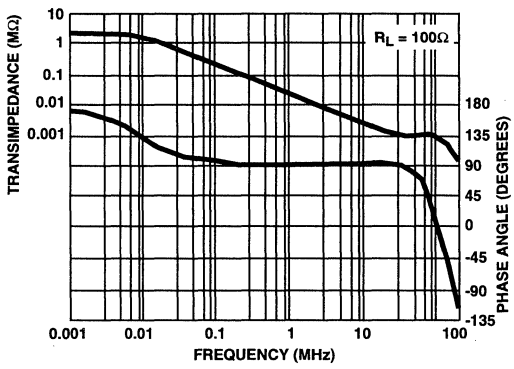


FIGURE 42. TRANSIMPEDANCE vs FREQUENCY

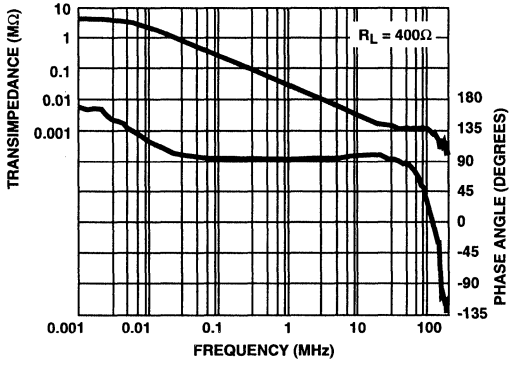


FIGURE 43. TRANSIMPEDENCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

2680µm x 2600µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.4kÅ

TRANSISTOR COUNT:

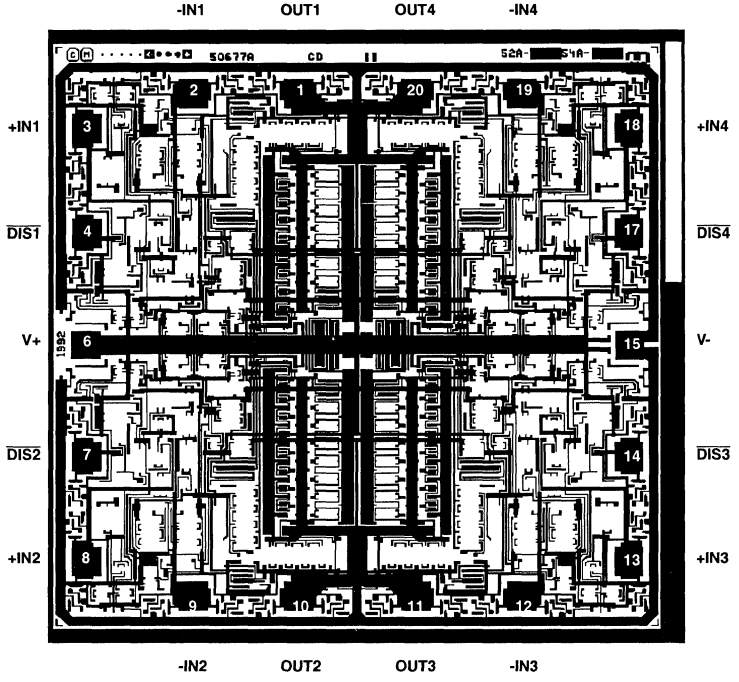
248

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA5024



HARRIS SEMICONDUCTOR

HA5025

Quad, 125MHz Video Current Feedback Amplifier

November 1996

Features

- Wide Unity Gain Bandwidth 125MHz
- Slew Rate 475V/μs
- Input Offset Voltage 800μV
- Differential Gain 0.03%
- Differential Phase ..... 0.03 Degrees
- Supply Current (per Amplifier) 7.5mA
- ESD Protection 4000V
- Guaranteed Specifications at ±5V Supplies

Applications

- Video Gain Block
- Video Distribution Amplifier/RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter
- Medical Imaging
- Radar and Imaging Systems
- Video Switching and Routing

Description

To put art in a text area: insert an anchored frame from the he HA5025 is a wide bandwidth high slew rate quad amplifier optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor.

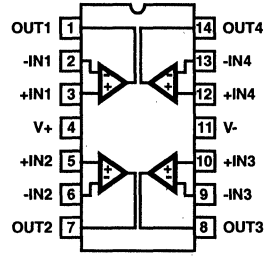
The performance of the HA5025 is very similar to the popular Harris HA-5020.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA5025IP	-40 to 85	14 Ld PDIP	E14.3
HA5025IB	-40 to 85	14 Ld SOIC	M14.15
HA5025EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HA5025
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3591.3**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
DC Input Voltage (Note 3) . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current (Note 4) . . . . . Short Circuit Protected
ESD Rating (Note 3)
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 2000V

Operating Conditions

Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage Range (Typical) . . . . . $\pm 4.5V$ to $\pm 15V$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
PDIP Package	100
SOIC Package	120

Maximum Junction Temperature (Note 1) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package, Note 1) . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below $175^{o}C$ for die, and below $150^{o}C$ for plastic packages. See Application Information section for safe operating area information.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. The non-inverting input of unused amplifiers must be connected to GND.
4. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.

Electrical Specifications

$V_{SUPPLY} = \pm 5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (V_{IO})		A	25	-	0.8	3	mV
		A	Full	-	-	5	mV
Delta V_{IO} Between Channels		A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift		B	Full	-	5	-	$\mu V/^{o}C$
V_{IO} Common Mode Rejection Ratio	Note 5	A	25	53	-	-	dB
		A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	60	-	-	dB
		A	Full	55	-	-	dB
Input Common Mode Range	Note 5	A	Full	± 2.5	-	-	V
Non-Inverting Input (+IN) Current		A	25	-	3	8	μA
		A	Full	-	-	20	μA
+IN Common Mode Rejection ($+I_{BCMR} = \frac{1}{+R_{IN}}$)	Note 5	A	25	-	-	0.15	$\mu A/V$
		A	Full	-	-	0.5	$\mu A/V$
+IN Power Supply Rejection	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	-	-	0.1	$\mu A/V$
		A	Full	-	-	0.3	$\mu A/V$
Inverting Input (-IN) Current		A	25, 85	-	4	12	μA
		A	-40	-	10	30	μA
Delta - IN BIAS Current Between Channels		A	25, 85	-	6	15	μA
		A	-40	-	10	30	μA
-IN Common Mode Rejection	Note 5	A	25	-	-	0.4	$\mu A/V$
		A	Full	-	-	1.0	$\mu A/V$
-IN Power Supply Rejection	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	-	-	0.2	$\mu A/V$
		A	Full	-	-	0.5	$\mu A/V$
Input Noise Voltage	f = 1kHz	B	25	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current	f = 1kHz	B	25	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current	f = 1kHz	B	25	-	25.0	-	$pA/\sqrt{Hz}$

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS							
Transimpedance	Note 11	A	25	1.0	-	-	MΩ
		A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain	$R_L = 400\Omega$, $V_{OUT} = \pm2.5V$	A	25	70	-	-	dB
		A	Full	65	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm2.5V$	A	25	50	-	-	dB
		A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing	$R_L = 150\Omega$	A	25	±2.5	±3.0	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	$R_L = 150\Omega$	B	Full	±16.6	±20.0	-	mA
Output Current, Short Circuit	$V_{IN} = \pm2.5V$, $V_{OUT} = 0V$	A	Full	±40	±60	-	mA
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		A	25	5	-	15	V
Quiescent Supply Current		A	Full	-	7.5	10	mA/Op Amp
AC CHARACTERISTICS ($A_V = +1$)							
Slew Rate	Note 6	B	25	275	350	-	V/µs
Full Power Bandwidth	Note 7	B	25	22	28	-	MHz
Rise Time	Note 8	B	25	-	6	-	ns
Fall Time	Note 8	B	25	-	6	-	ns
Propagation Delay	Note 8	B	25	-	6	-	ns
Overshoot		B	25	-	4.5	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	75	-	ns
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)							
Slew Rate	Note 6	B	25	-	475	-	V/µs
Full Power Bandwidth	Note 7	B	25	-	26	-	MHz
Rise Time	Note 8	B	25	-	6	-	ns
Fall Time	Note 8	B	25	-	6	-	ns
Propagation Delay	Note 8	B	25	-	6	-	ns
Overshoot		B	25	-	12	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	100	-	ns
Gain Flatness	5MHz	B	25	-	0.02	-	dB
	20MHz	B	25	-	0.07	-	dB
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)							
Slew Rate	Note 6	B	25	350	475	-	V/µs
Full Power Bandwidth	Note 7	B	25	28	38	-	MHz
Rise Time	Note 8	B	25	-	8	-	ns
Fall Time	Note 8	B	25	-	9	-	ns
Propagation Delay	Note 8	B	25	-	9	-	ns
Overshoot		B	25	-	1.8	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	75	-	ns

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Settling Time to 0.1%	2V Output Step	B	25	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (Note 10)	$R_L = 150\Omega$	B	25	-	0.03	-	%
Differential Phase (Note 10)	$R_L = 150\Omega$	B	25	-	0.03	-	Degrees

NOTES:

5. $V_{CM} = \pm2.5V$. At -40°C Product is tested at $V_{CM} = \pm2.25V$ because Short Test Duration does not allow self heating.
6. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
7. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 2V$.
8. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
9. A. Production Tested; B. Typical or Guaranteed Limit based on characterization; C. Design Typical for information only.
10. Measured with a VM700A video tester using an NTC-7 composite VITS.
11. $V_{OUT} = \pm2.5V$. At -40°C Product is tested at $V_{OUT} = \pm2.25V$ because Short Test Duration does not allow self heating.

Test Circuits and Waveforms

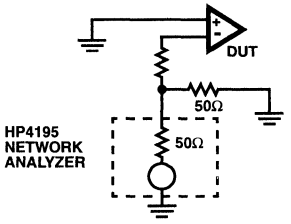


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

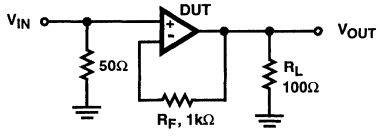


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

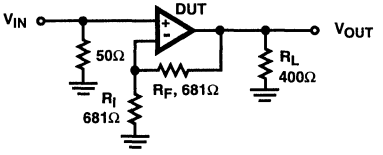
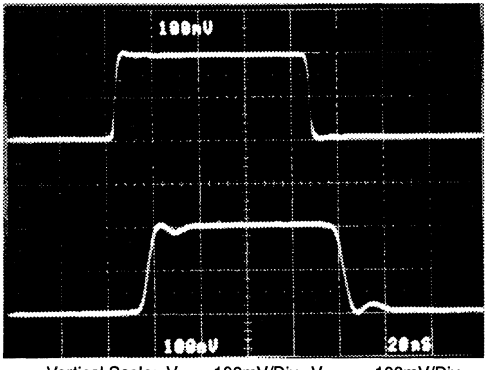
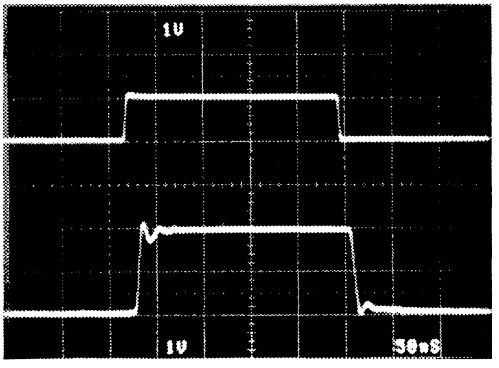


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

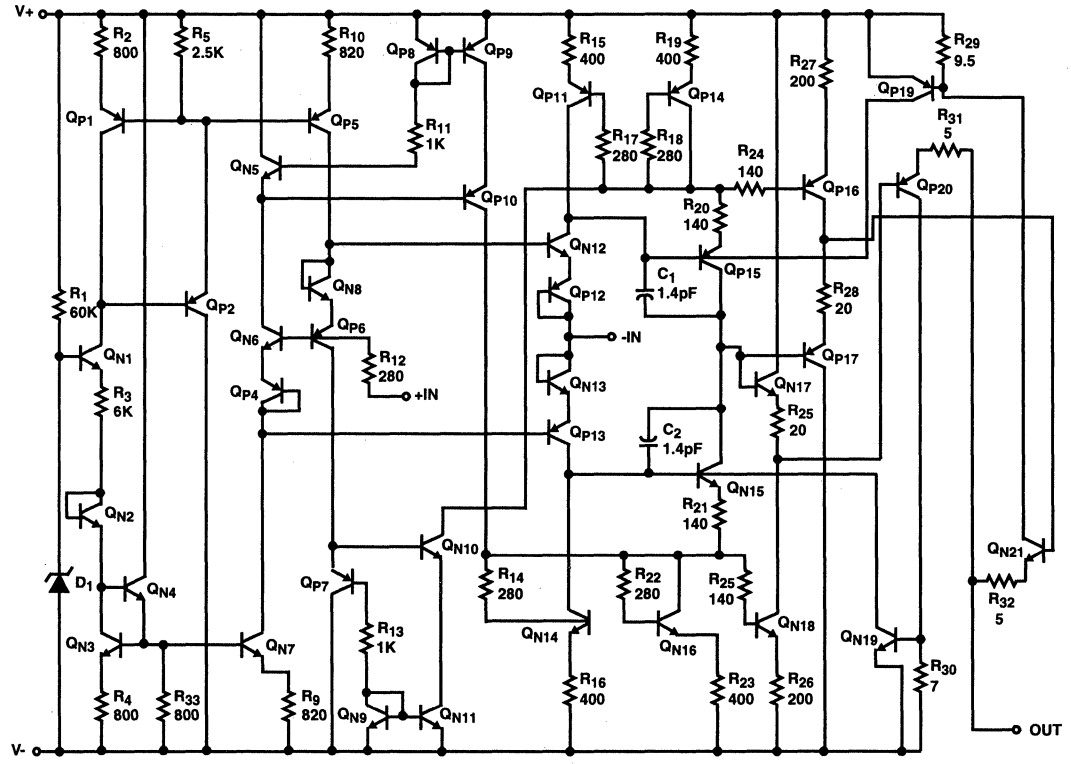
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic Diagram (One Amplifier of Four)



Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 8 and Figure 9 in the typical performance section, illustrate the performance of the HA5025 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5025 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The following table lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10μF) tantalum or electrolytic capacitor in

parallel with a small value (0.1μF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

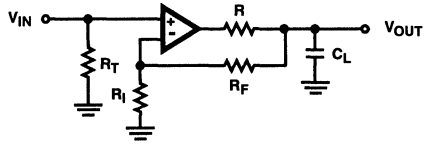


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (PDIP, SOIC). At $V_S = \pm 5V$ quiescent operation both package styles may be operated over the full industrial range of -40°C to 85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

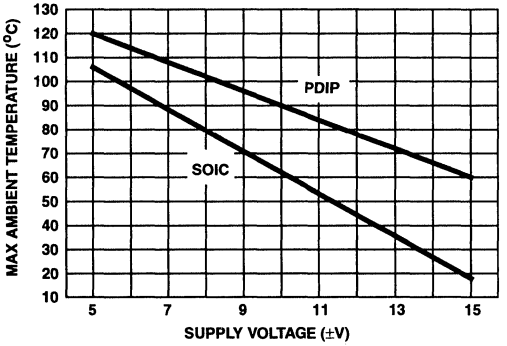


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified

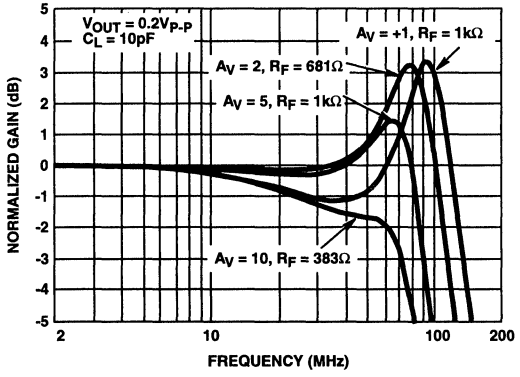


FIGURE 8. NON-INVERTING FREQUENCY RESPONSE

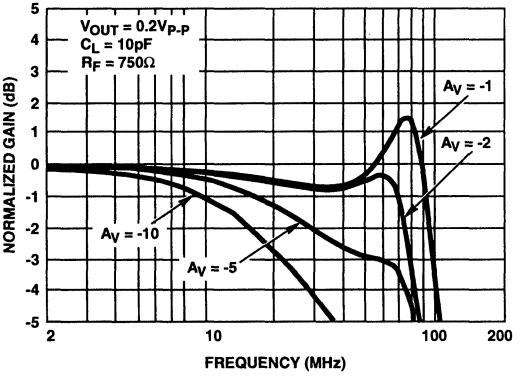


FIGURE 9. INVERTING FREQUENCY RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

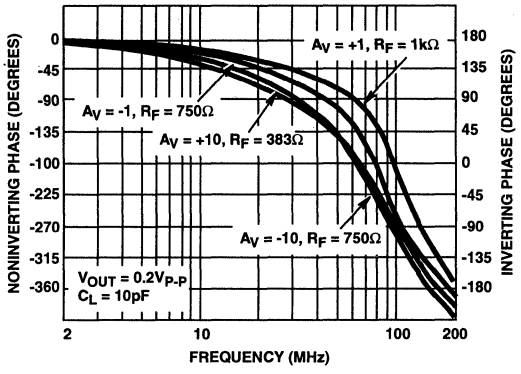


FIGURE 10. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

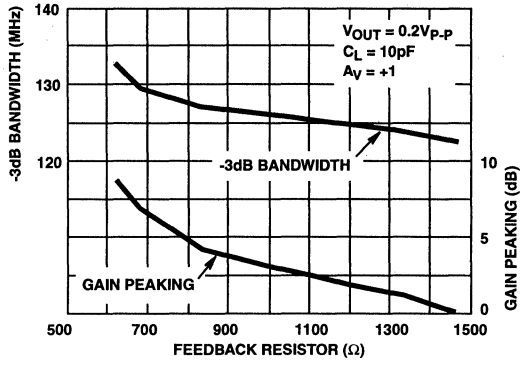


FIGURE 11. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

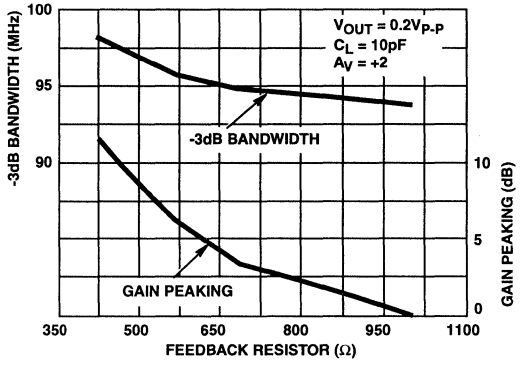


FIGURE 12. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

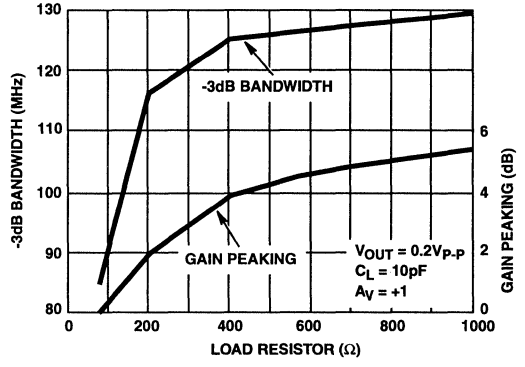


FIGURE 13. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

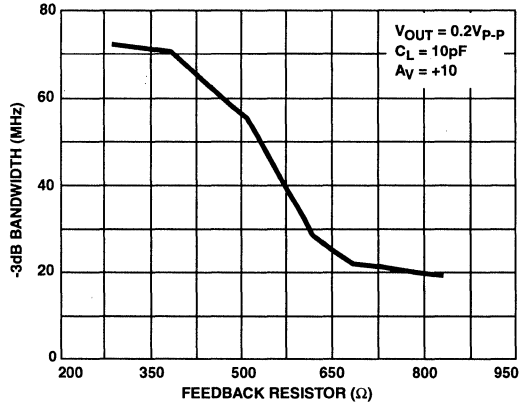


FIGURE 14. BANDWIDTH vs FEEDBACK RESISTANCE

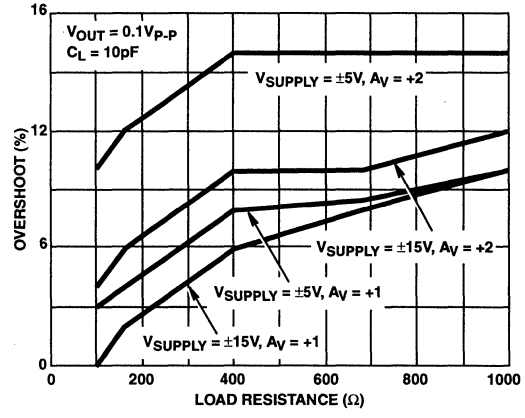


FIGURE 15. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

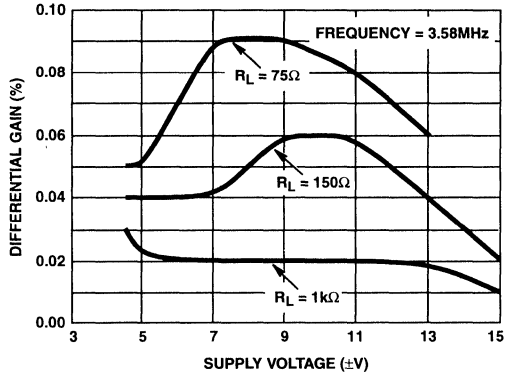


FIGURE 16. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

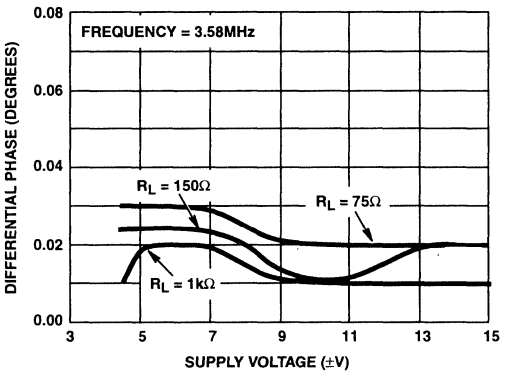


FIGURE 17. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

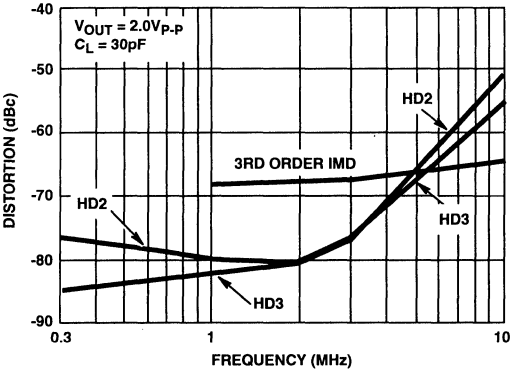


FIGURE 18. DISTORTION vs FREQUENCY

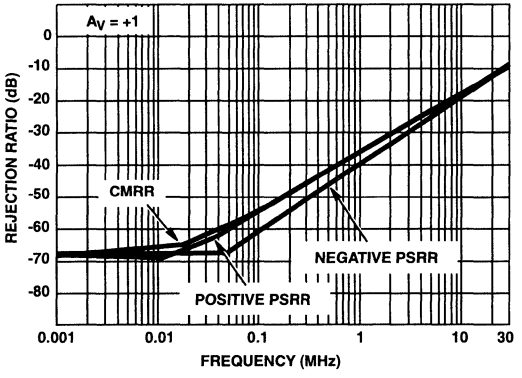


FIGURE 19. REJECTION RATIOS vs FREQUENCY

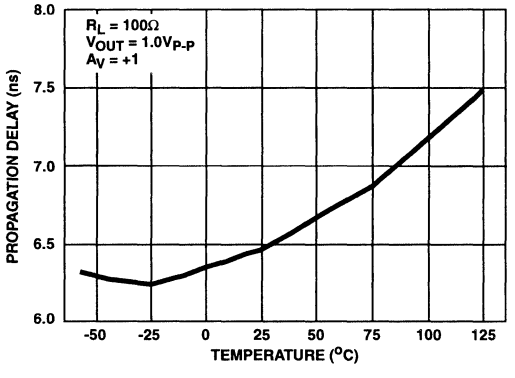


FIGURE 20. PROPAGATION DELAY vs TEMPERATURE

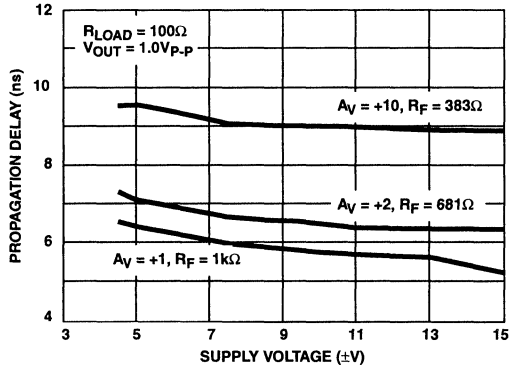


FIGURE 21. PROPAGATION DELAY vs SUPPLY VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

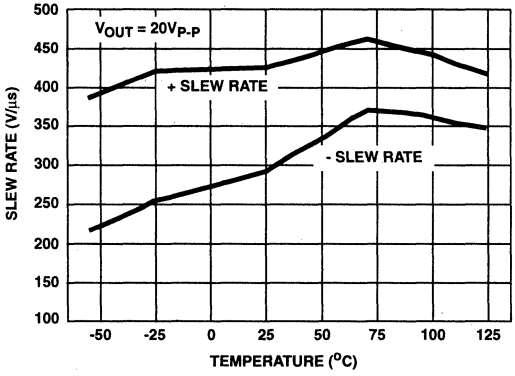


FIGURE 22. SLEW RATE vs TEMPERATURE

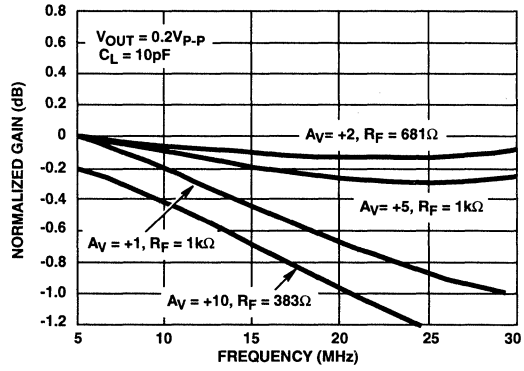


FIGURE 23. NON-INVERTING GAIN FLATNESS vs FREQUENCY

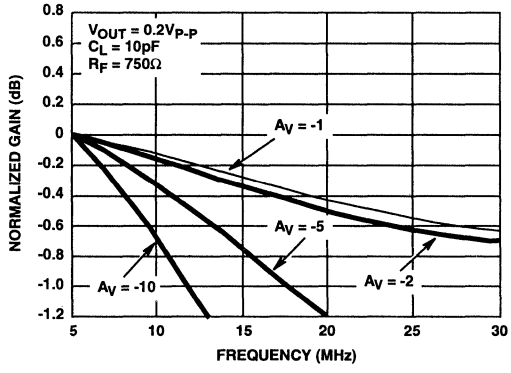


FIGURE 24. INVERTING GAIN FLATNESS vs FREQUENCY

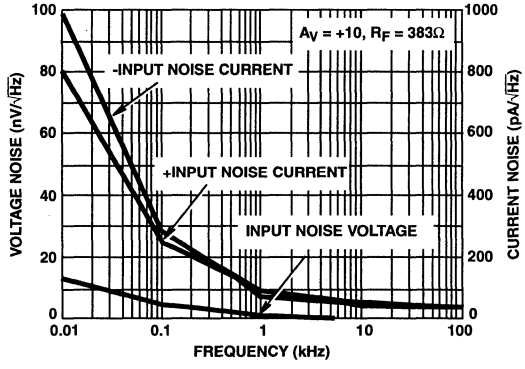


FIGURE 25. INPUT NOISE CHARACTERISTICS

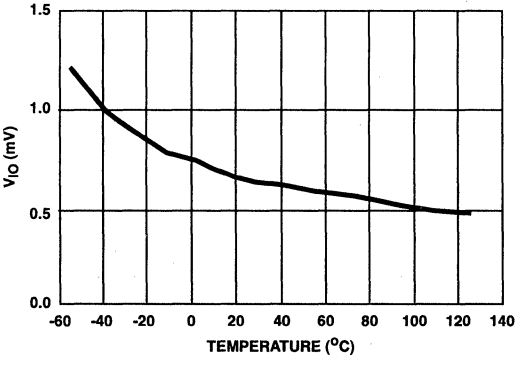


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE

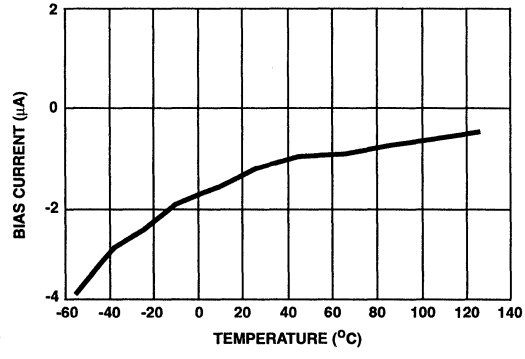


FIGURE 27. +INPUT BIAS CURRENT vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

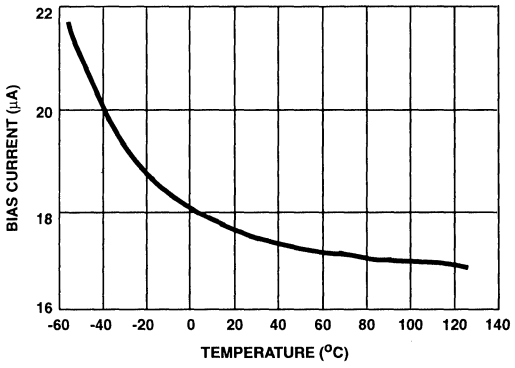


FIGURE 28. -INPUT BIAS CURRENT vs TEMPERATURE

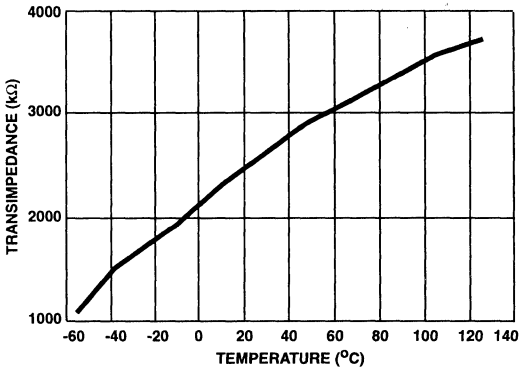


FIGURE 29. TRANSIMPEDANCE vs TEMPERATURE

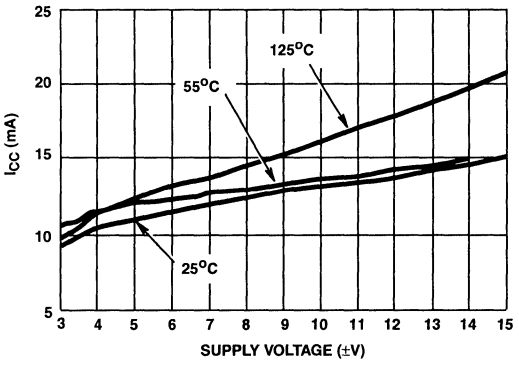


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

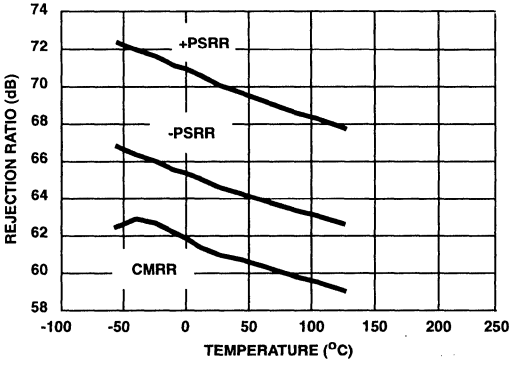


FIGURE 31. REJECTION RATIO vs TEMPERATURE

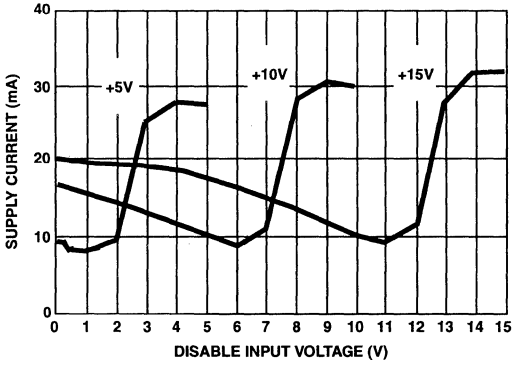


FIGURE 32. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

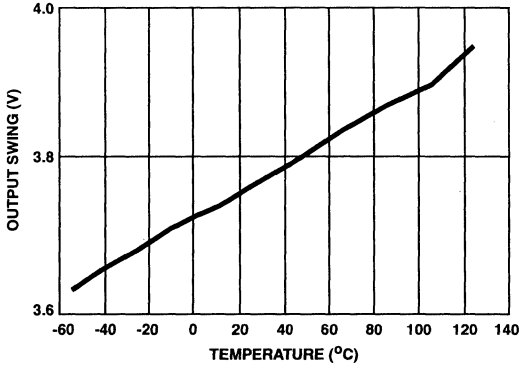


FIGURE 33. OUTPUT SWING vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

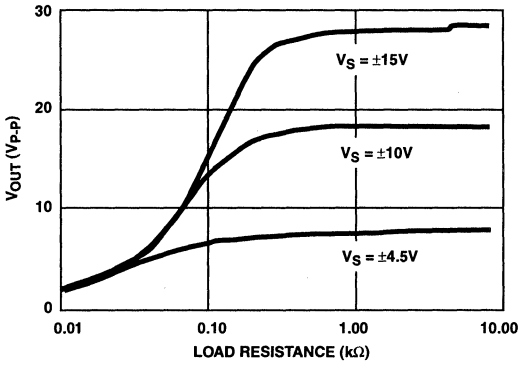


FIGURE 34. OUTPUT SWING vs LOAD RESISTANCE

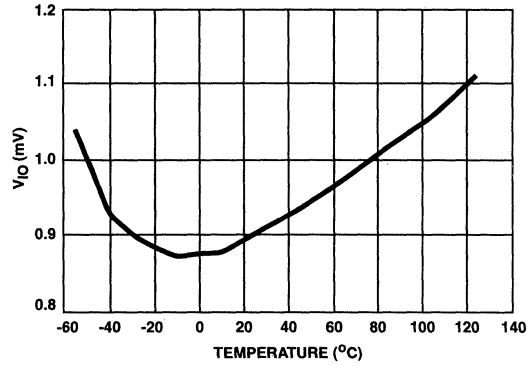


FIGURE 35. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

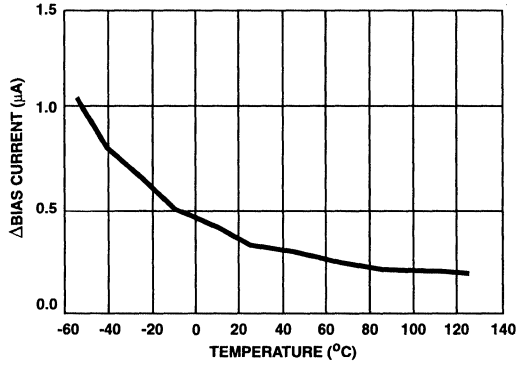


FIGURE 36. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

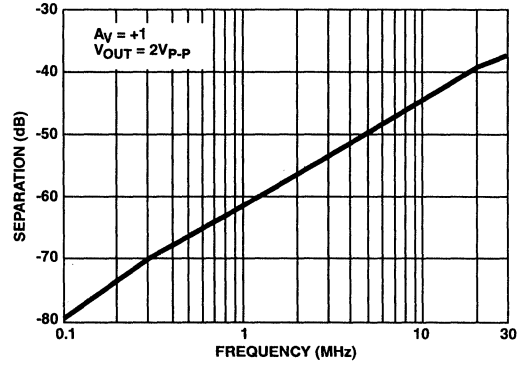


FIGURE 37. CHANNEL SEPARATION vs FREQUENCY

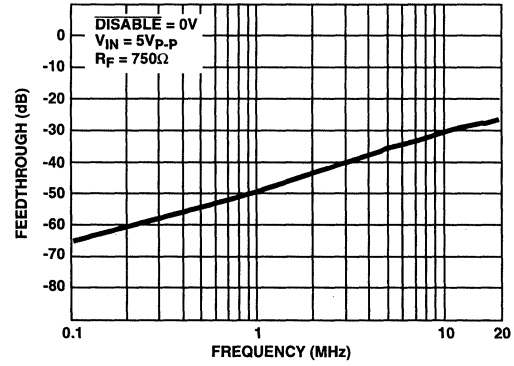


FIGURE 38. DISABLE FEEDTHROUGH vs FREQUENCY

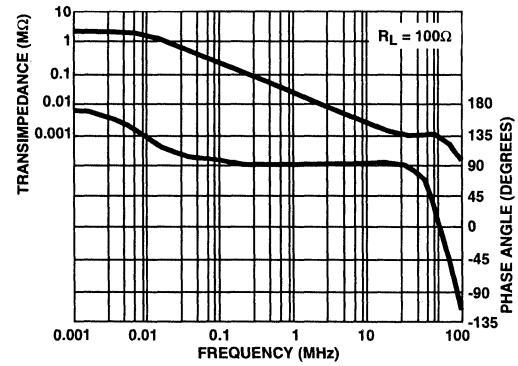


FIGURE 39. TRANSIMPEDANCE vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

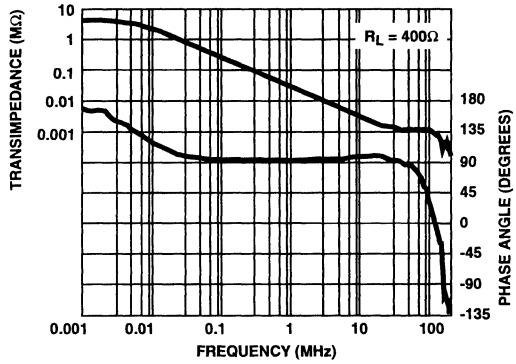


FIGURE 40. TRANSIMPEDANCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

2010µm x 3130µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)
Thickness: Metal 1: 8kÅ ±0.4kÅ

Metal 2: AlCu (1%)
Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.4kÅ

TRANSISTOR COUNT:

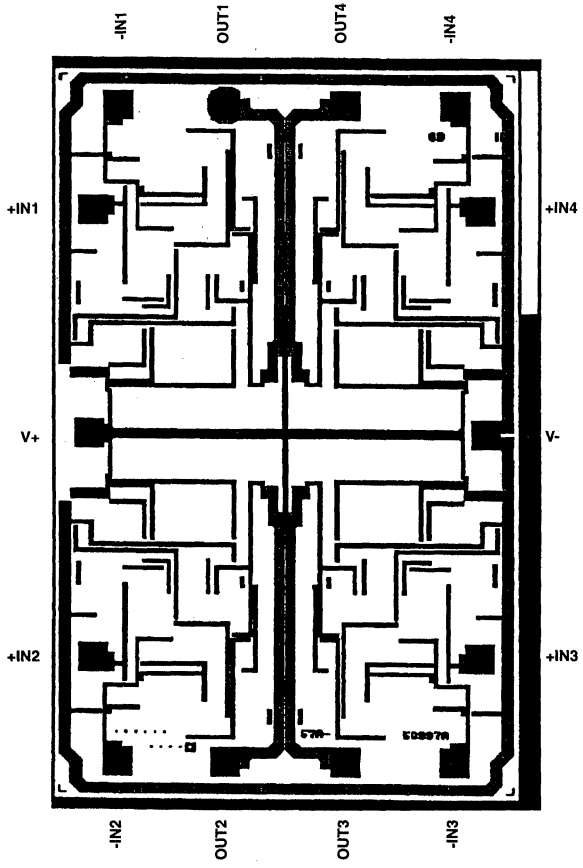
248

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA5025



HARRIS SEMICONDUCTOR

HA-5033

November 1996

250MHz Video Buffer

Features

- Differential Phase Error ..... 0.02 Degrees
- Differential Gain Error 0.03%
- High Slew Rate 1100V/μs
- Wide Bandwidth (Small Signal) 250MHz
- Wide Power Bandwidth ..... DC to 17.5MHz
- Fast Rise Time 3ns
- High Output Drive ..... ±10V With 100Ω Load
- Wide Power Supply Range ..... ±5V to ±16V
- Replace Costly Hybrids

Applications

- Video Buffer
- High Frequency Buffer
- Isolation Buffer
- High Speed Line Driver
- Impedance Matching
- Current Boosters
- High Speed A/D Input Buffers
- Related Literature
  - AN548, Designer's Guide for HA-5033

Description

The HA-5033 is a unity gain monolithic IC designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outstanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/μs and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

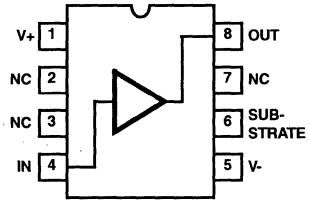
The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce a lower AC performance.

Ordering Information

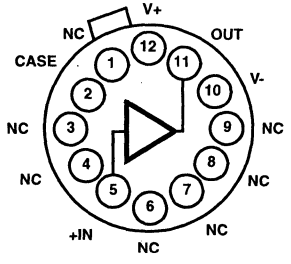
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-5033-2	-55 to 125	12 Pin Metal Can	T12.C
HA2-5033-5	0 to 75	12 Pin Metal Can	T12.C
HA3-5033-5	0 to 75	8 Ld PDIP	E8.3
HA9P5033-5 (H50335)	0 to 60 (Note 3)	8 Ld PSOP	M8.15A

Pinouts

HA-5033
(PDIP, PSOP)
TOP VIEW



HA-5033
(METAL CAN)
TOP VIEW



3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number 2924.2

Absolute Maximum Ratings

Voltage Between V+ and V- Pins 40V
DC Input Voltage . . . . . V+ to V-
Output Current (Peak) (50ms On/1 Second Off) . . . . . ±200mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 2000V

Operating Conditions

Temperature Ranges
HA-5033-2. . . . . -55°C to 125°C
HA-5033-5 (Note 3). . . . . 0°C to 75°C
HA9P5033-5 (Notes 1, 3) . . . . . -40°C to 60°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	65	34
PDIP Package	96	N/A
PSOP Package (Note 4)	129	N/A

Maximum Internal Power Dissipation (Note 1)
Maximum Junction Temperature (Note 1) . . . . . 175°C
Maximum Junction Temperature (Plastic Packages) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below 175°C for the metal can package, and below 150°C for the plastic packages. (See Figure 5.)
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. Maximum operating temperature in the PSOP package is limited to 60°C, for $V_{SUPPLY} = \pm 12V$ to prevent the junction temperature from exceeding 150°C. The maximum operating temperature may have to be derated further, depending on the output load condition. The operating temperature may be increased if the HA9P5033 is operated at lower V_{SUPPLY}. For example, the quiescent operating temperature may be increased to 75°C by operating at $V_{SUPPLY} \leq \pm 9.7V$. See Figure 5 for more information.
4. Direct attach of the PSOP copper slug to copper area on the PCB can reduce the θ_{JA} value to <100°C/W. Consult the Harris Application Group for more information.

Electrical Specifications

$V_{SUPPLY} = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $C_L = 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5033-2			HA-5033-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	5	15	-	5	15	mV
		Full	-	6	25	-	6	25	mV
Average Offset Voltage Drift		Full	-	33	-	-	33	-	µV/°C
Bias Current		25	-	20	35	-	20	35	µA
		Full	-	30	50	-	30	50	µA
Input Resistance		25	-	3	-	-	3	-	MΩ
Input Capacitance		25	-	1.6	-	-	1.6	-	pF
Input Noise Voltage	10Hz to 100MHz	25	-	20	-	-	20	-	μV_{P-P}
TRANSFER CHARACTERISTICS									
Voltage Gain	$R_L = 100\Omega$	25	0.93	-	-	0.93	-	-	V/V
	$R_L = 1k\Omega$	25	0.93	0.99	-	0.93	0.99	-	V/V
	$R_L = 100\Omega$	Full	0.92	-	-	0.92	-	-	V/V
-3dB Bandwidth		25	-	250	-	-	250	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 100\Omega$	Full	±8	±10	-	±8	±10	-	V
	$R_L = 1k\Omega$, $V_S = \pm 15V$	Full	±11	±12	-	±11	±12	-	V
Output Current		25	±80	±100	-	±80	±100	-	mA
Output Resistance		25	-	8	-	-	8	-	Ω
Full Power Bandwidth	$V_{OUT} = 1V_{RMS}$, $R_L = 1k\Omega$	25	-	146	-	-	146	-	MHz
Full Power Bandwidth (Note 5)		25	15.9	17.5	-	15.9	17.5	-	MHz
TRANSIENT RESPONSE									
Rise Time	$V_{OUT} = 500mV$	25	-	4.6	-	-	4.6	-	ns
Propagation Delay		25	-	1	-	-	1	-	ns
Overshoot		25	-	3	-	-	3	-	%
Slew Rate (Note 5)		25	1	1.1	-	1	1.1	-	V/ns
Settling Time to 0.1%		25	-	50	-	-	50	-	ns

Electrical Specifications $V_{SUPPLY} = \pm12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $C_L = 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5033-2			HA-5033-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Phase Error (Note 6)		25	-	0.02	-	-	0.02	-	Degree
Differential Gain Error (Note 6)		25	-	0.03	-	-	0.03	-	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	21	25	-	21	25	mA
		Full	-	21	30	-	21	30	mA
Power Supply Rejection Ratio		Full	54	-	-	54	-	-	dB
Harmonic Distortion	$V_{IN} = 1V_{RMS}$ at 100kHz	25	-	<0.1	-	-	<0.1	-	%

NOTES:

5. $V_{SUPPLY} = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 1k\Omega$.
6. Differential gain and phase error are nonlinear signal distortions found in video systems and are defined as follows: Differential gain error is defined as the change in amplitude at the color subcarrier frequency as the picture signal is varied from blanking to white level. Differential phase error is defined as the change in the phase of the color subcarrier as the picture signal is varied from blanking to white level. $R_L = 300\Omega$.

Test Circuits and Waveforms

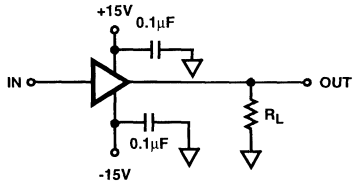


FIGURE 1. SLEW RATE AND SETTLING TIME

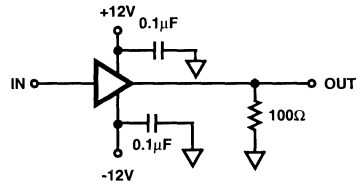


FIGURE 2. TRANSIENT RESPONSE

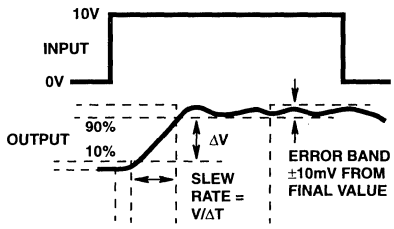
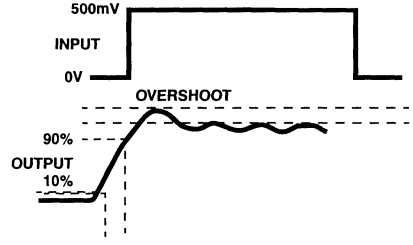
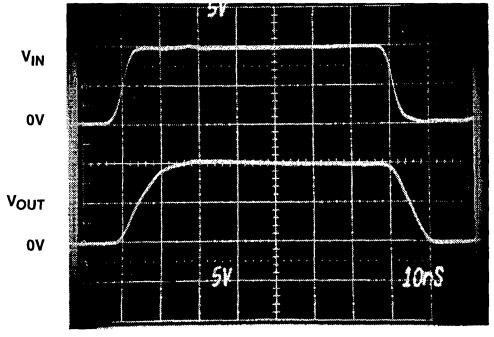


FIGURE 3. SETTLING TIME



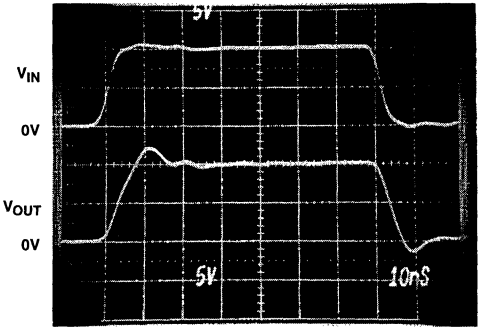
NOTE: Measured on both positive and negative transitions.

FIGURE 4. RISE TIME



$T_A = 25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$

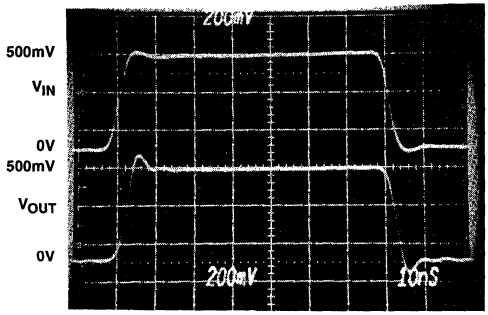
+10V RESPONSE



$T_A = 25^oC$, $R_S = 50\Omega$, $R_L = 1k\Omega$

+10V RESPONSE

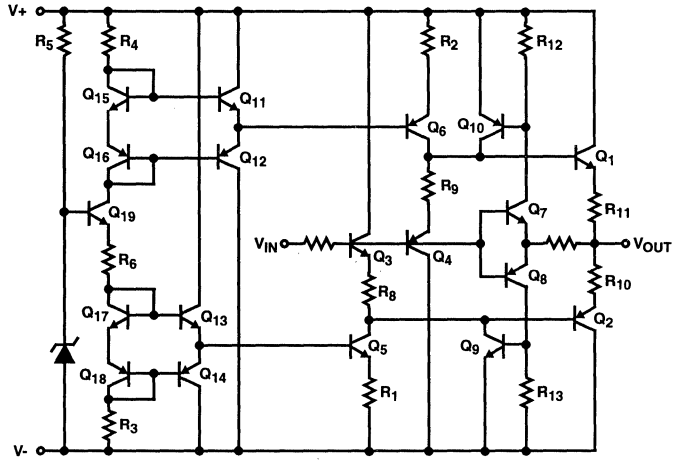
Test Circuits and Waveforms (Continued)



$T_A = 25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$

PULSE RESPONSE

Schematic Diagram



Application Information

Layout Considerations

The wide bandwidth of the HA-5033 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance. This ground plane shielding can also incorporate the metal case of the HA-5033 since pin #2 is internally tied to the package. This feature allows the user to make metal to metal contact between the ground plane and the package, which extends shielding, provides additional heat sinking and eliminates the use of a socket, IC sockets contribute inter-lead capacitance which limits device bandwidth and should be avoided.

For the PDIP, pin 6 can be tied to either supply, grounded, or simply not used. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimum device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01µF to 0.1µF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1µF or larger will optimize low frequency performance.

It is also recommended that the bypass capacitors be connected close to the HA-5033 (preferably directly to the supply pins).

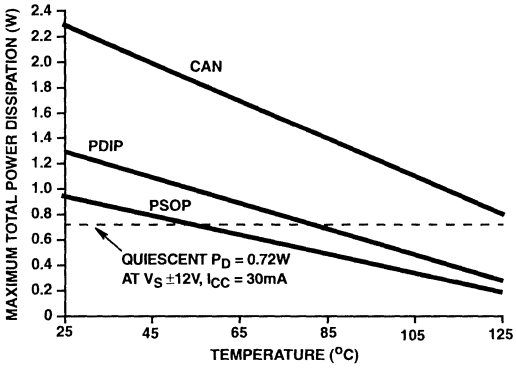


FIGURE 5. FREE AIR POWER DISSIPATION

Graph is based on:

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$$

Where: T_{JMAX} = Maximum Junction Temperature of the Device

T_A = Ambient Temperature

θ_{JA} = Junction to Ambient Thermal Resistance

Typical Applications (Also see Application Note AN548)

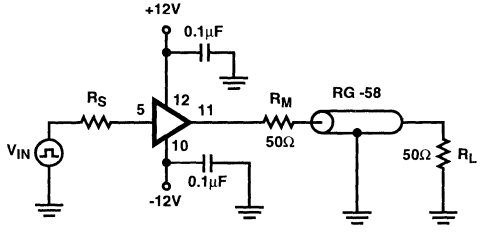


FIGURE 6. VIDEO COAXIAL LINE DRIVER 50Ω SYSTEM

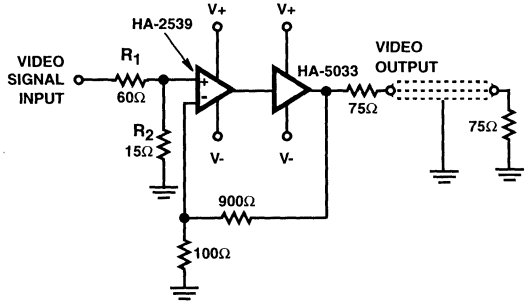
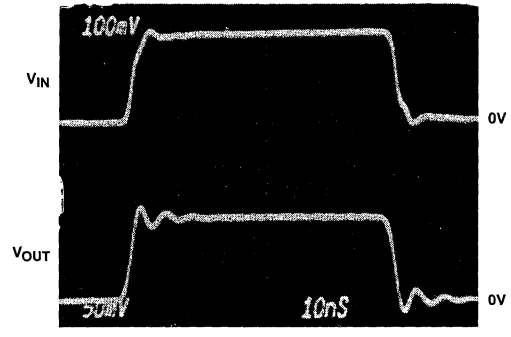


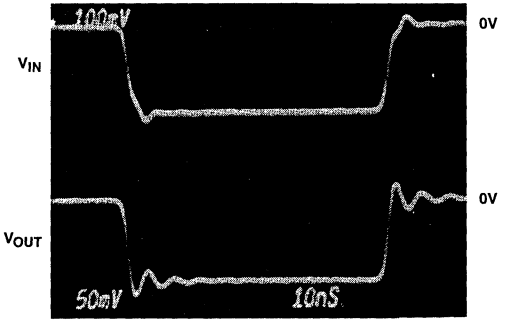
FIGURE 7. VIDEO GAIN BLOCK



$T_A = 25^oC$, $R_S = 50\Omega$, $R_M = R_L = 50\Omega$

$$V_O = V_{IN}\left[\frac{R_L}{R_L + R_M}\right] = \left[\frac{1}{2}\right]V_{IN}$$

POSITIVE PULSE RESPONSE



$T_A = 25^oC$, $R_S = 50\Omega$, $R_M = R_L = 50\Omega$

$$V_O = V_{IN}\left[\frac{R_L}{R_L + R_M}\right] = \left[\frac{1}{2}\right]V_{IN}$$

NEGATIVE PULSE RESPONSE

Typical Performance Curves

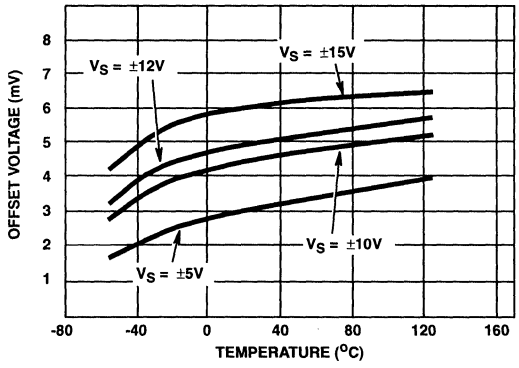


FIGURE 8. INPUT OFFSET VOLTAGE vs TEMPERATURE

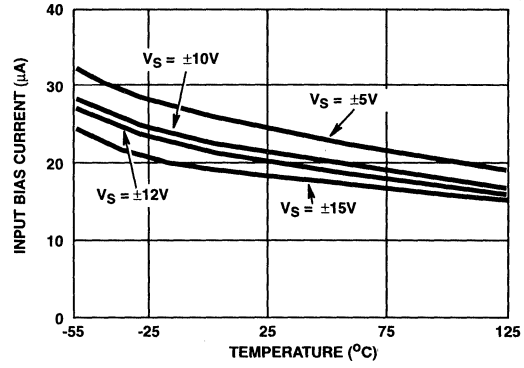


FIGURE 9. INPUT BIAS CURRENT vs TEMPERATURE

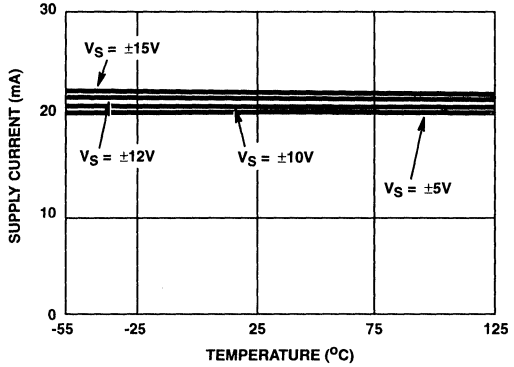


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

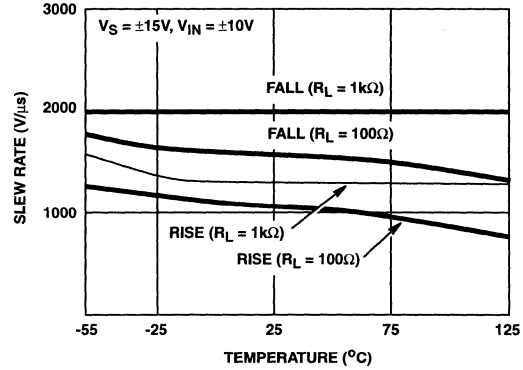


FIGURE 11. SLEW RATE vs TEMPERATURE

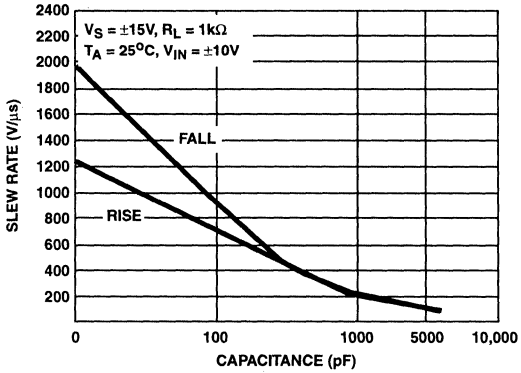


FIGURE 12. SLEW RATE vs LOAD CAPACITANCE

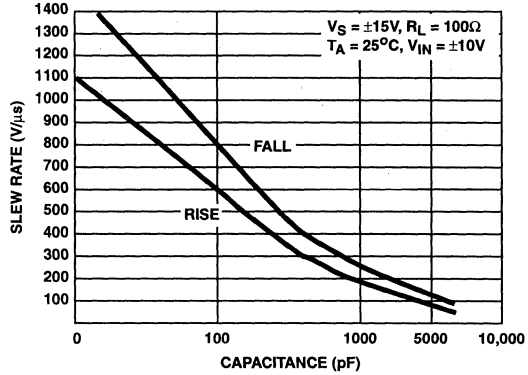


FIGURE 13. SLEW RATE vs LOAD CAPACITANCE

Typical Performance Curves (Continued)

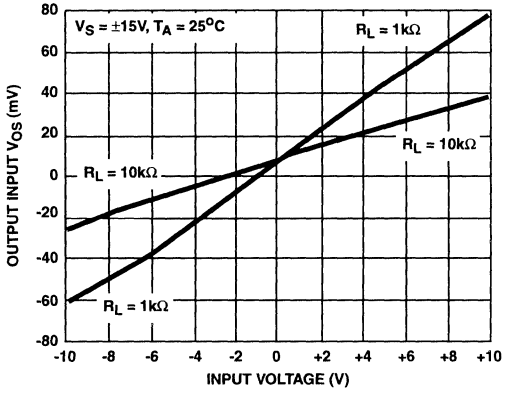


FIGURE 14. GAIN ERROR vs INPUT VOLTAGE

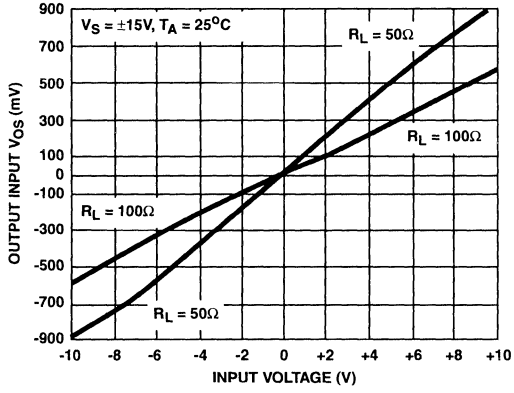


FIGURE 15. GAIN ERROR vs INPUT VOLTAGE

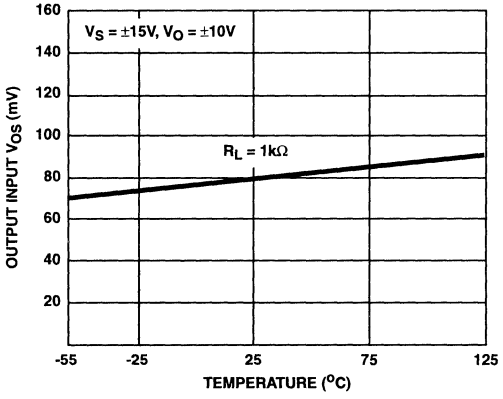


FIGURE 16. GAIN ERROR vs TEMPERATURE

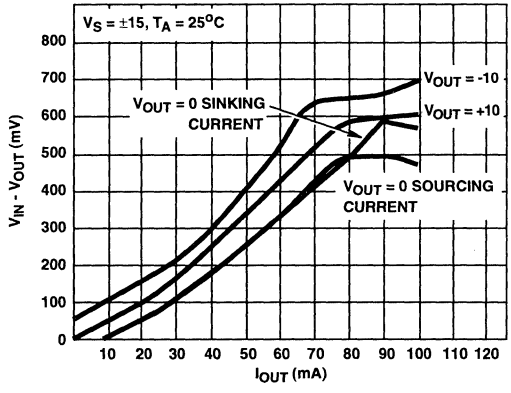


FIGURE 17. $V_{IN} - V_{OUT}$ vs I_{OUT}

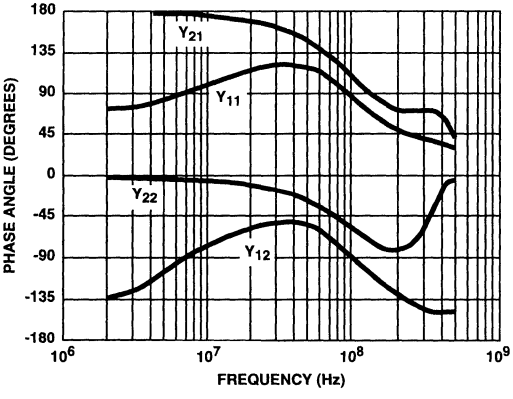


FIGURE 18. Y - PARAMETERS PHASE vs FREQUENCY

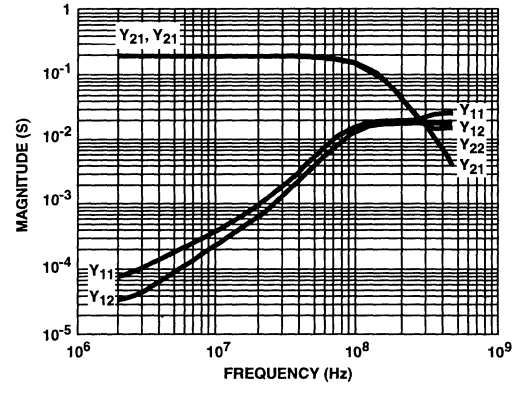


FIGURE 19. Y - PARAMETER MAGNITUDE vs FREQUENCY

Typical Performance Curves (Continued)

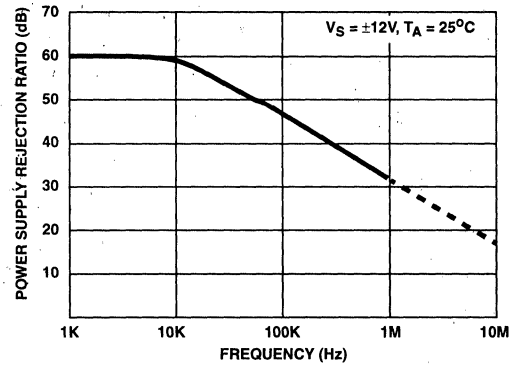


FIGURE 20. POWER SUPPLY REJECTION RATIO vs FREQUENCY

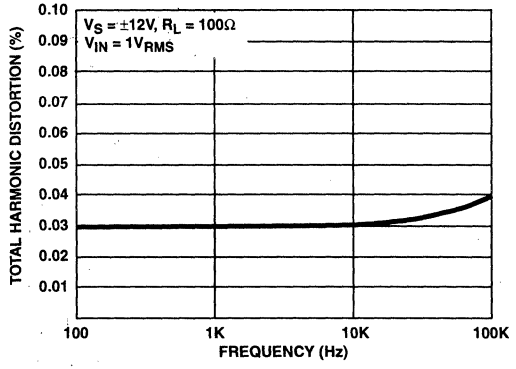


FIGURE 21. TOTAL HARMONIC DISTORTION vs FREQUENCY

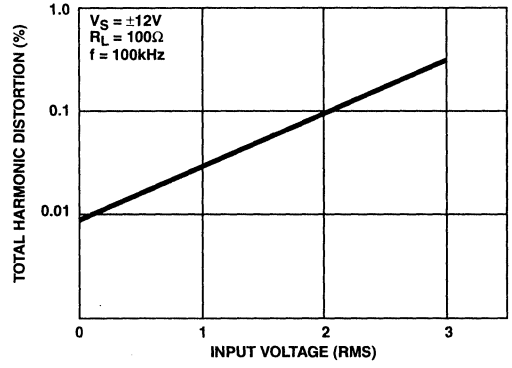


FIGURE 22. TOTAL HARMONIC DISTORTION vs INPUT VOLTAGE

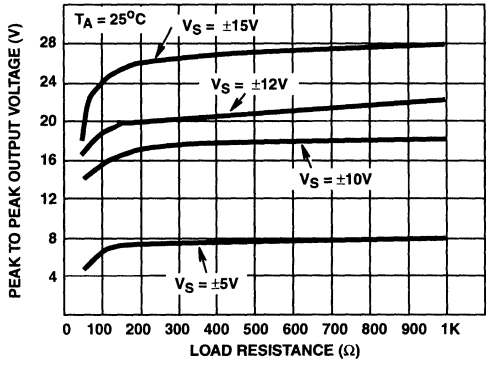


FIGURE 23. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

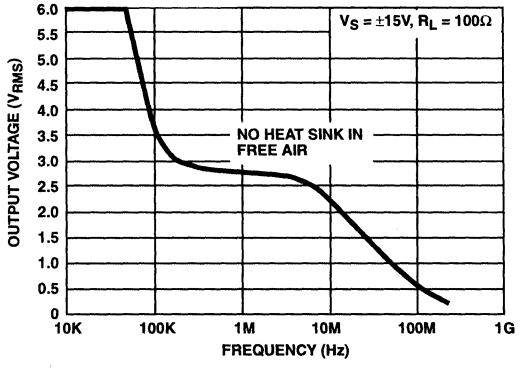


FIGURE 24. OUTPUT SWING vs FREQUENCY (NOTE)

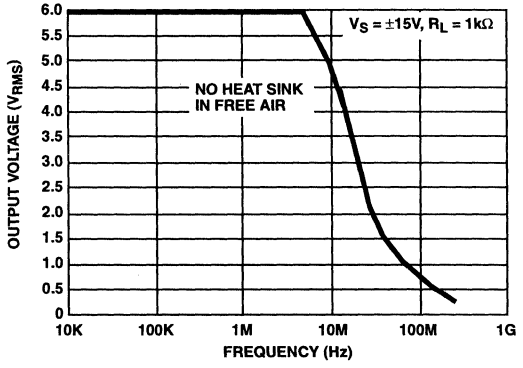


FIGURE 25. OUTPUT SWING vs FREQUENCY (NOTE)

NOTE:
This curve was obtained by noting the output voltage necessary to produce an observable distortion for a given frequency. If higher distortion is acceptable, then a higher output voltage for a given frequency can be obtained. However, operating the HA-5033 with increased distortion (to the right of curve shown), will also be accompanied by an increase in supply current. The resulting increase in chip temperature must be considered and heat sinking will be necessary to prevent thermal runaway. This characteristic is the result of the output transistor operation. If the signal amplitude or signal frequency or both are increased beyond the curve shown, the NPN, PNP output transistors will approach a condition of being simultaneously on. Under this condition, thermal runaway can occur.

Die Characteristics

DIE DIMENSIONS:

51 mils x 67 mils x 19 mils
1300µm x 1700µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

TRANSISTOR COUNT:

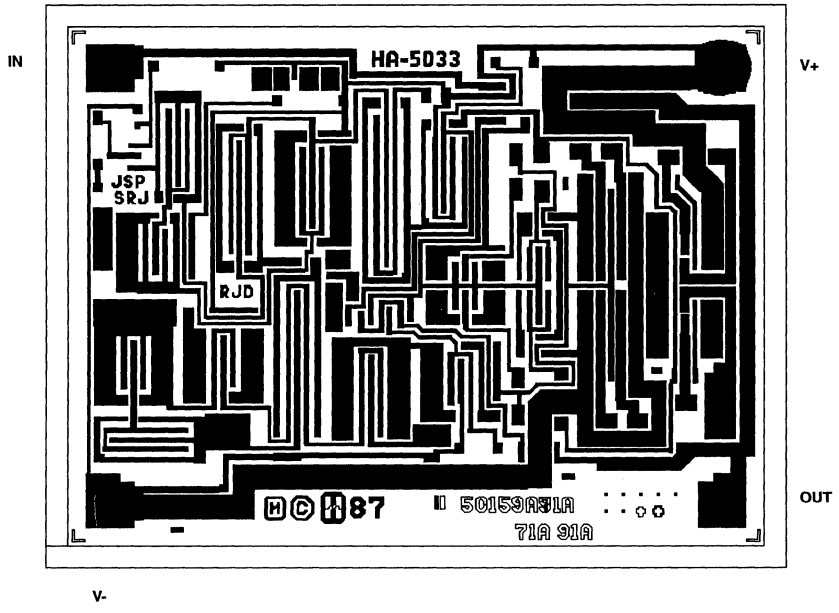
20

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5033



HA-5101, HA-5111

10MHz and 100MHz, Low Noise, Operational Amplifiers

November 1996

Features

- Low Noise ..... 3.0nV/√Hz at 1kHz
- Bandwidth ..... 10MHz (Compensated)
  100MHz (Uncompensated)
- Slew Rate ..... 10V/µs (Compensated)
  50V/µs (Uncompensated)
- Low Offset Voltage Drift ..... 3µV/°C
- High Gain ..... 1 x 10^6V/V
- High CMRR/PSRR 100dB
- High Output Drive Capability 30mA

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators
- For Further Design Ideas, See Application Note AN554, Harris AnswerFAX (407-724-7800) Document #9554

Description

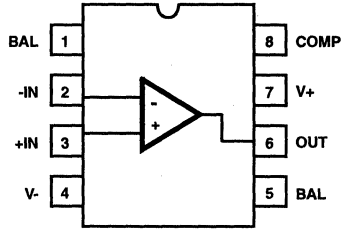
The HA-5101/5111 are dielectrically isolated operational amplifiers featuring low noise. Both amplifiers have an excellent noise voltage density of 3.0nV/√Hz at 1kHz. The uncompensated HA-5111 is stable at a minimum gain of 10 and has the same DC specifications as the unity gain stable HA-5101. The difference in compensation yields a 100MHz gain-bandwidth product and a 50V/µs slew rate for the HA-5111 versus a 10MHz unity gain bandwidth and a 10V/µs slew rate for the HA-5101.

DC characteristics of the HA-5101/5111 assure accurate performance. The 0.5mV offset voltage is externally adjustable and offset voltage drift is just 3µV/°C. An offset current of only 30nA reduces input current errors and an open loop voltage gain of 1 x 10^6V/V increases loop gain for low distortion amplification.

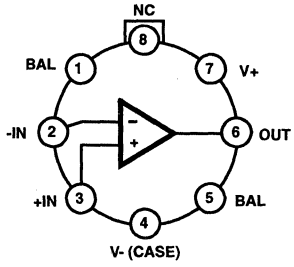
The HA-5101/5111 are ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head and phono cartridge preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators and high Q filters.

Pinouts

HA-5101, HA-5111 (PDIP, CERDIP, SOIC)
TOP VIEW



HA-5101 (CAN)
TOP VIEW



Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-5101-2	-55 to 125	8 Pin Can	T8.C
HA3-5101-5	0 to 75	8 Ld PDIP	E8.3
HA7-5101-2	-55 to 125	8 Ld CERDIP	F8.3A
HA9P5101-5 (H51015)	0 to 75	8 Ld SOIC	M8.15
HA9P5101-9 (H51019)	-40 to 85	8 Ld SOIC	M8.15
HA3-5111-5	0 to 75	8 Ld PDIP	E8.3
HA7-5111-2	-55 to 125	8 Ld CERDIP	F8.3A
HA9P5111-5 (H51115)	0 to 75	8 Ld SOIC	M8.15
HA9P5111-9 (H51119)	-40 to 85	8 Ld SOIC	M8.15

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2905.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage. 7V
Input Voltage . . . . . $\pm V_{SUPPLY}$
Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-5101/5111-2 . . . . . -55^oC to 125^oC
HA-5101/5111-5 . . . . . 0^oC to 75^oC
HA-5101/5111-9 . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
Can Package	165	80
PDIP Package	94	N/A
CERDIP Package	135	50
SOIC Package	157	N/A

Maximum Junction Temperature (Note 1) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below 175^oC for hermetic packages, and below 150^oC for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm 15V$, $R_S = 100\Omega$, $R_L = 2k\Omega$, $C_L = 50pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HA-5101-2, -5; HA-5111-2, -5			HA-5101-9, HA-5111-9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	0.5	3	-	0.5	3	mV
		Full	-	-	4	-	-	4	mV
Offset Voltage Drift		Full	-	3	-	-	3	-	$\mu V/^oC$
Bias Current		25	-	100	200	-	100	200	nA
		Full	-	-	325	-	-	325	nA
Offset Current		25	-	30	75	-	30	75	nA
		Full	-	-	125	-	-	125	nA
Input Resistance		25	-	500	-	-	500	-	kΩ
Common Mode Range		Full	±12	-	-	±12	-	-	V
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$	25	-	1000	-	-	1000	-	kV/V
		Full	100	250	-	100	250	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	Full	80	100	-	80	100	-	dB
Small Signal Bandwidth	HA-5101, $A_V = 1$	25	-	10	-	-	10	-	MHz
Gain Bandwidth Product	HA-5111, $A_V = 10$	25	-	100	-	-	100	-	MHz
Minimum Stable Gain	HA-5101	Full	1	-	-	1	-	-	V/V
	HA-5111	Full	10	-	-	10	-	-	V/V
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 10k\Omega$	Full	±12	±13	-	±12	±13	-	V
	$R_L = 2k\Omega$	Full	±12	±13	-	±12	±13	-	V
	$V_S = \pm 18V$, $R_L = 600\Omega$	25	±15	-	-	±15	-	-	V
Output Current (Note 3)		25	25	30	-	25	30	-	mA

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_S = 100\Omega$, $R_L = 2k\Omega$, $C_L = 50pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5101-2, -5; HA-5111-2, -5			HA-5101-9, HA-5111-9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Full Power Bandwidth (Note 4)	HA-5101	25	95	160	-	95	160	-	kHz
	HA-5111	25	630	790	-	630	790	-	kHz
Output Resistance		25	-	110	-	-	110	-	Ω
Maximum Load Capacitance		25	-	800	-	-	800	-	pF
TRANSIENT RESPONSE (Note 5)									
Rise Time	HA-5101	25	-	50	100	-	50	100	ns
	HA-5111	25	-	30	60	-	30	60	ns
Overshoot	HA-5101	25	-	20	35	-	20	35	%
	HA-5111	25	-	20	40	-	20	40	%
Slew Rate	HA-5101	25	6	10	-	6	10	-	V/μs
	HA-5111	25	40	50	-	40	50	-	V/μs
Settling Time (Note 6)	HA-5101 0.01%	-	-	2.6	-	-	2.6	-	μs
	HA-5111 0.01%	-	-	0.5	-	-	0.5	-	μs
NOISE CHARACTERISTICS (Note 7)									
Input Noise Voltage	f = 10Hz	25	-	5	7	-	5	7	$nV/\sqrt{Hz}$
	f = 1kHz	25	-	3.0	4.0	-	3.0	4.0	$nV/\sqrt{Hz}$
Input Noise Current	f = 10Hz	25	-	4.0	9	-	4.0	9	$pA/\sqrt{Hz}$
	f = 1kHz		-	0.6	2.5	-	0.6	2.5	$pA/\sqrt{Hz}$
Broadband Noise Voltage	f = DC To 30kHz	25	-	0.870	-	-	0.870	-	μV_{RMS}
POWER SUPPLY CHARACTERISTICS									
Supply Current HA-5101/5111		Full	-	4	6	-	4	7	mA
Power Supply Rejection Ratio	$\Delta V_S = \pm5V$	Full	80	100	-	80	100	-	dB

NOTES:

3. Output current is measured with $V_{OUT} = \pm15V$ with $V_{SUPPLY} = \pm18V$.
4. Full power bandwidth is guaranteed by equation: Full power bandwidth $= \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, $V_{PEAK} = 10V$.
5. Refer to Test Circuits section of the data sheet.
6. Settling time is measured to 0.01% of final value for a 10V output step, and $A_V = -10$ for HA-5111 and 0.01% of final value for a 10V output step, $A_V = -1$ for HA-5101.
7. The limits for these parameters are guaranteed based on lab characterization, and reflect lot-to-lot variation.

Test Circuits and Waveforms

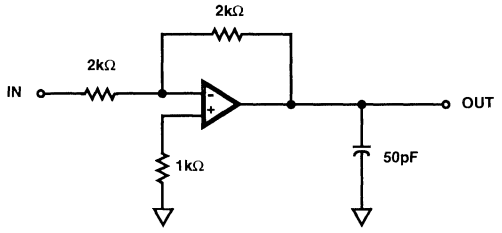


FIGURE 1. HA-5101 LARGE SIGNAL RESPONSE CIRCUIT

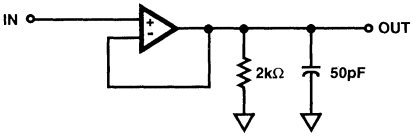
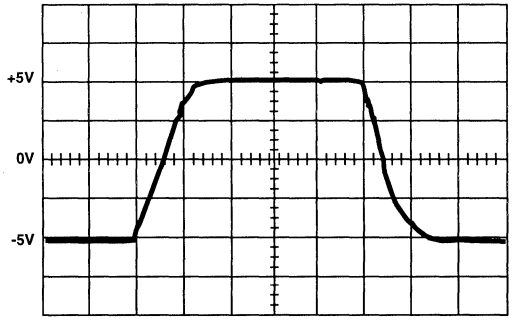
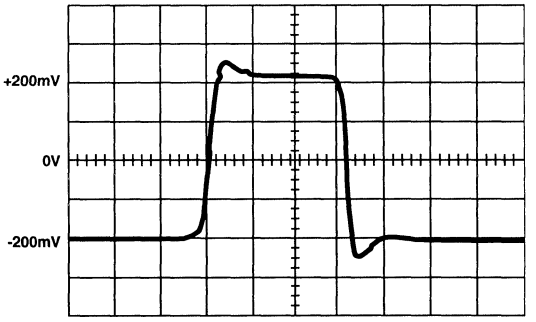


FIGURE 2. HA-5101 SMALL SIGNAL RESPONSE CIRCUIT



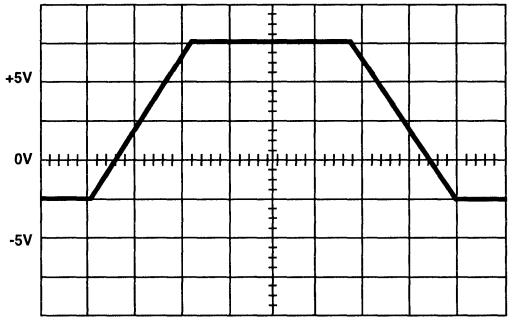
Ch. 1 = 2.5V/Div.
Timebase = 200ns/Div.

FIGURE 3. HA-5111 LARGE SIGNAL TRANSIENT RESPONSE



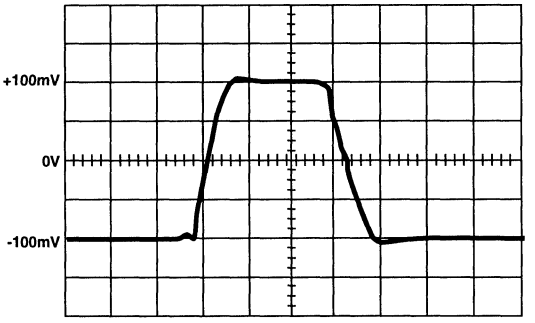
Ch. 1 = 100mV/Div.
Timebase = 100ns/Div.

FIGURE 4. HA-5111 SMALL SIGNAL TRANSIENT RESPONSE



Ch. 1 = 2.5V/Div.
Timebase = 1.00µs/Div.

FIGURE 5. HA-5101 LARGE SIGNAL TRANSIENT RESPONSE



Ch. 1 = 50mV/Div.
Timebase = 100ns/Div.

FIGURE 6. HA-5101 SMALL SIGNAL TRANSIENT RESPONSE

Test Circuits and Waveforms (Continued)

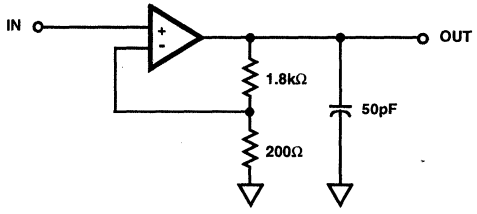
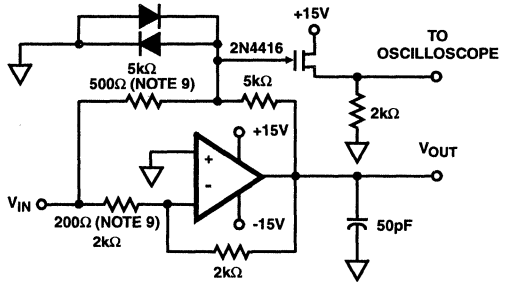


FIGURE 7. HA-5111 LARGE AND SMALL SIGNAL RESPONSE CIRCUIT

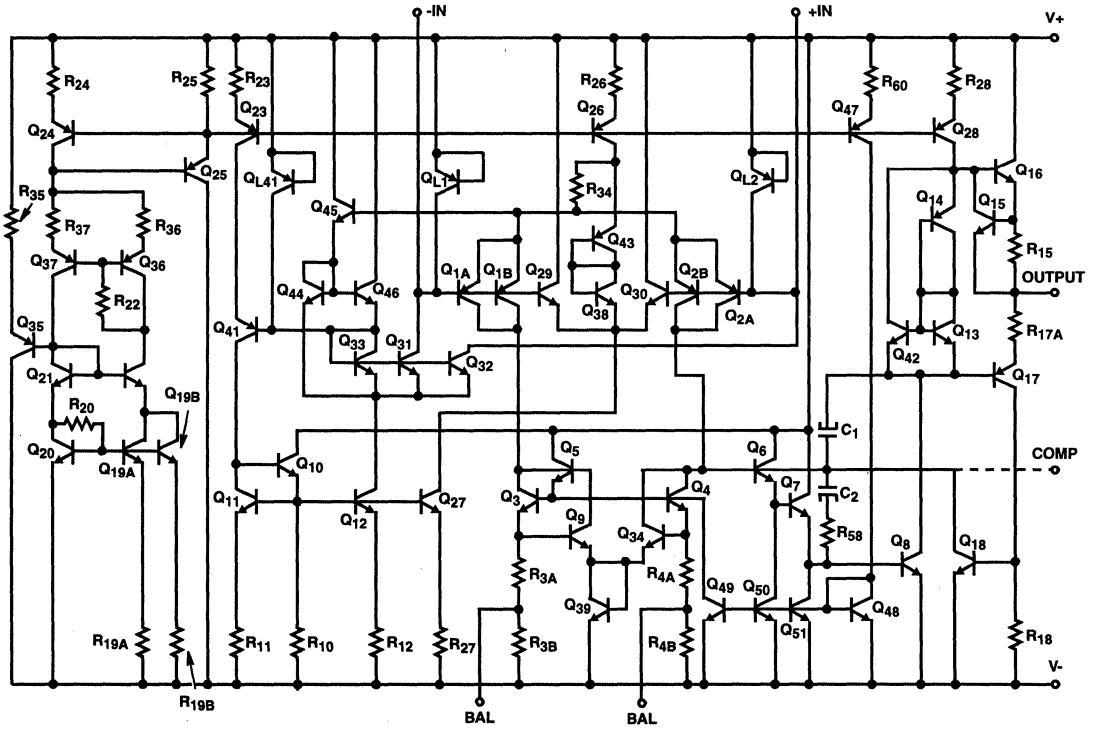


NOTES:

8. A_V = -1 (HA-5101), A_V = -10 (HA-5111).
9. Feedback and summing resistors should be 0.1% matched.
10. Clipping diodes are optional, HP5082-2810 recommended.

FIGURE 8. SETTLING TIME CIRCUIT

Schematic



Application Information

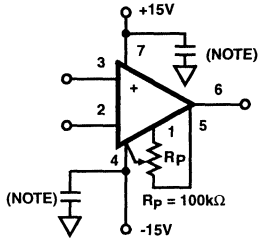
Operation At ±5V Supply

The HA-5101/11 performs well at $V_S = \pm 5V$ exhibiting typical characteristics as listed below:

I_{CC}	3.7mA
V_{IO}	0.5mV
I_{BIAS}	56nA
A_{VOL} ($V_O = \pm 3V$)	106kV/V
V_{OUT}	3.7V
I_{OUT}	13mA
CMRR ($\Delta V_{CM} = \pm 2.5V$)	90dB
PSRR ($\Delta V_S = 0.5V$)	90dB
Unity Gain Bandwidth (5101)	10MHz
GBWP (5111)	100MHz
Slew Rate (5101)	7V/µs
Slew Rate (5111)	40V/µs

Offset Adjustment

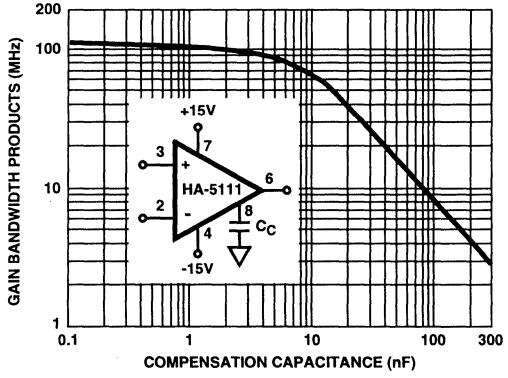
The following is the recommended V_{IO} adjust configuration:



NOTE: Proper decoupling is always recommended, 0.1µF high quality capacitor should be at or very near the device's supply pins.

Compensation

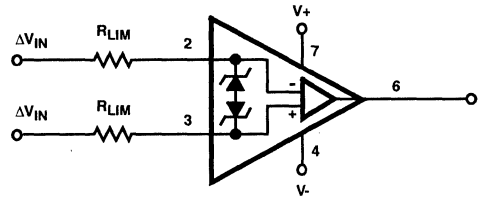
An external compensation capacitor can be used with the HA-5111 connected between pin 8 and ground (or V-, V+ not Recommended). A plot of gain bandwidth product vs compensation capacitor has been included as a design aid. The capacitor should be a high frequency type mounted near the device leads to minimize parasitics.



Input Protection

The HA-5101/11 has built-in back-to-back protection diodes which will limit the differential input voltage to approximately 7V. If the 5101/11 will be used in conditions where that voltage may be exceeded, then current limiting resistors must be used. No more than 25mA should be allowed to flow in the HA-5101/11's input.

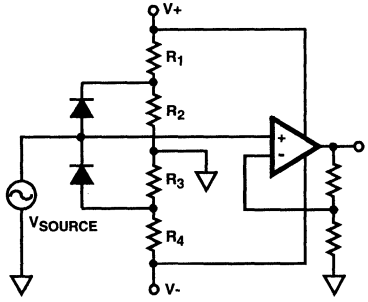
Comparator Circuit



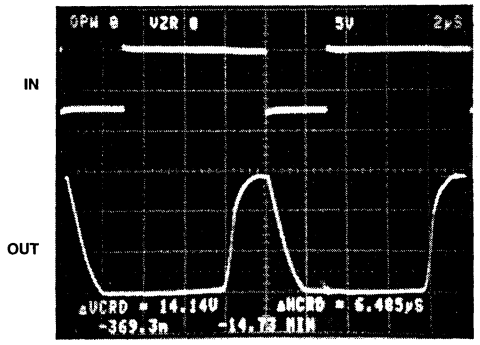
Choose R_{LIM} Such That: $\frac{(\Delta V_{INMAX} - 7V)}{25mA} \leq 2R_{LIM}$

Output Saturation

When an op amp is overdriven, output devices can saturate and sometimes take a long time to recover. Saturation can be avoided (sometimes) by using circuits such as:



If saturation cannot be avoided the HA-5101/11 recovers from a 25% overdrive in about 6.5µs (see photos).



Top: Input
Bottom: Output, 5V/Div., 2µs/Div.
Output is overdriven negative and recovers in 6µs.

Typical Performance Curves

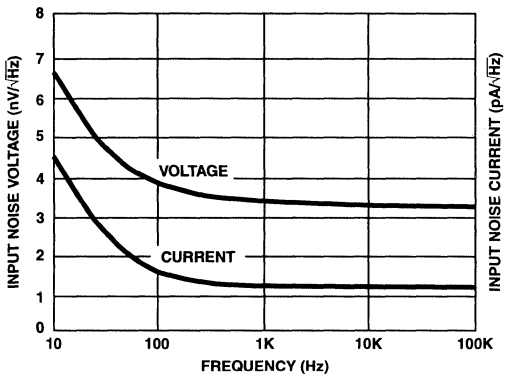


FIGURE 9. HA-5101/11 NOISE SPECTRUM

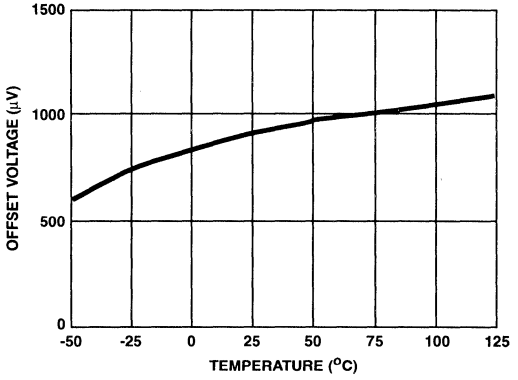
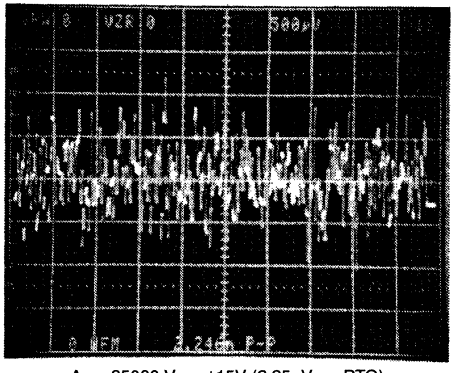
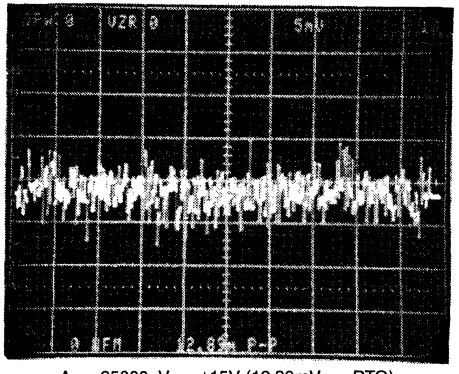


FIGURE 10. OFFSET VOLTAGE vs TEMPERATURE



A_V = 25000 V_S = ±15V (2.25µV_{P-P} RTO)

PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz



A_V = 25000, V_S = ±15V (12.89mV_{P-P} RTO)

PEAK-TO-PEAK TOTAL NOISE 0.1Hz TO 1MHz

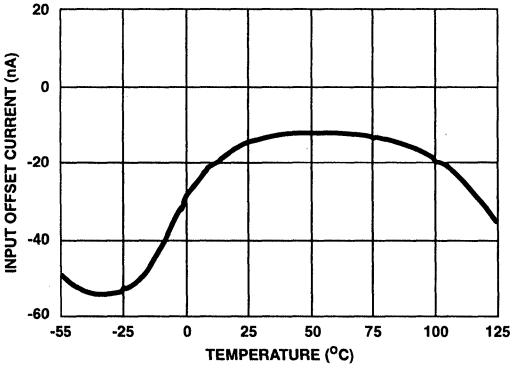


FIGURE 11. INPUT OFFSET CURRENT vs TEMPERATURE

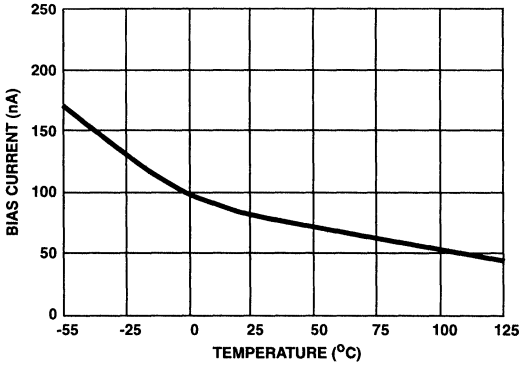


FIGURE 12. INPUT BIAS CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

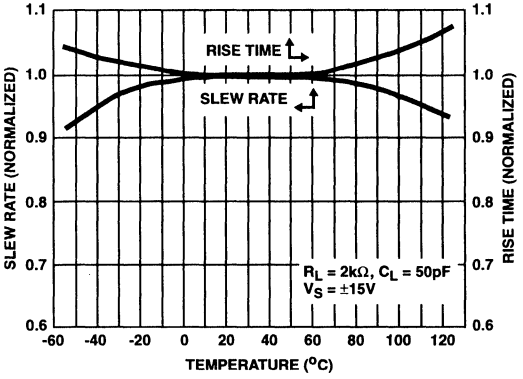


FIGURE 13. SLEW RATE/RISE TIME vs TEMPERATURE

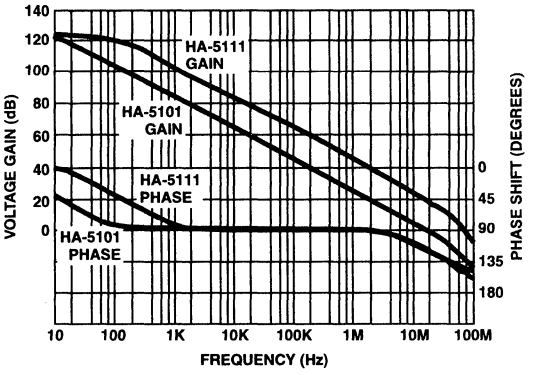


FIGURE 14. OPEN-LOOP GAIN/PHASE vs FREQUENCY

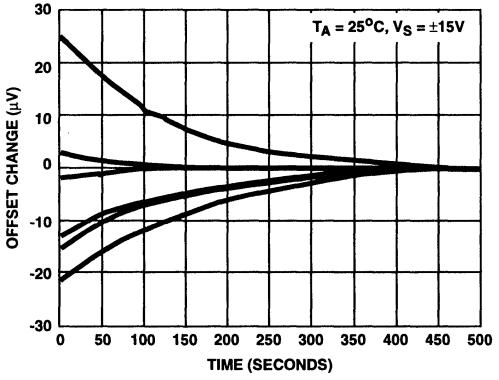


FIGURE 15. INPUT OFFSET WARMUP DRIFT vs TIME (NORMALIZED TO ZERO FINAL VALUE) (SIX REPRESENTATIVE UNITS)

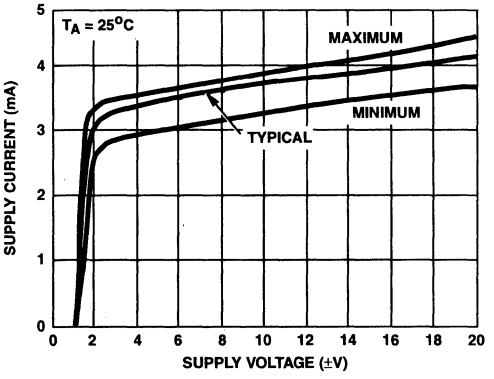


FIGURE 16. SUPPLY CURRENT vs SUPPLY VOLTAGE

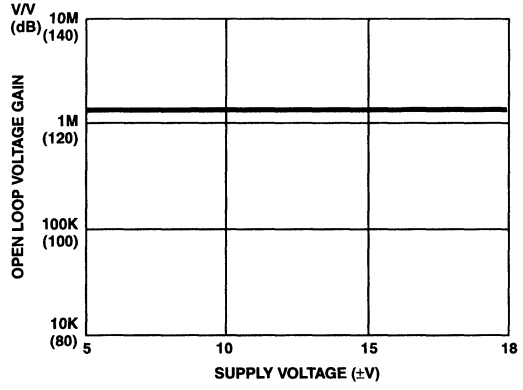
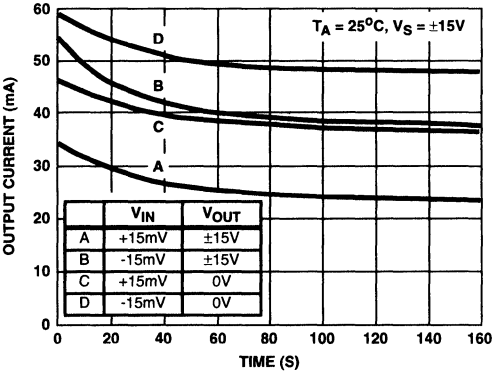


FIGURE 17. DC OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



	V_{IN}	V_{OUT}
A	+15mV	±15V
B	-15mV	±15V
C	+15mV	0V
D	-15mV	0V

FIGURE 18. SHORT CIRCUIT CURRENT vs TIME

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued)

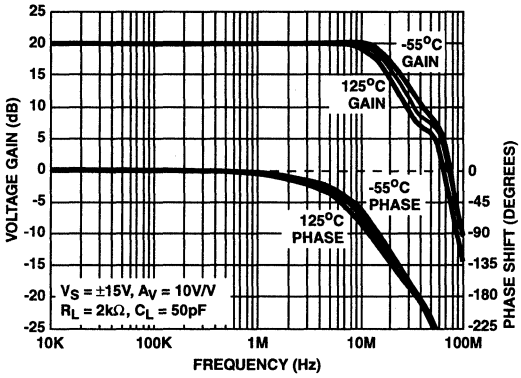


FIGURE 19. HA-5111 FREQUENCY RESPONSE

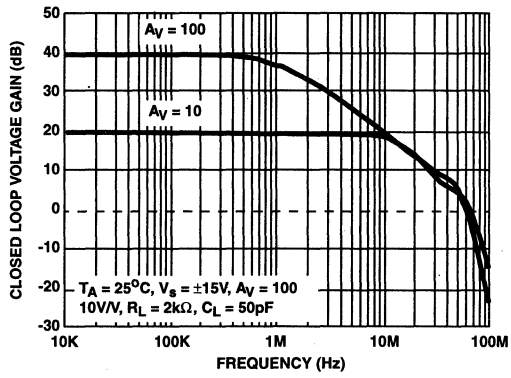


FIGURE 20. HA-5111 CLOSED-LOOP GAIN vs FREQUENCY

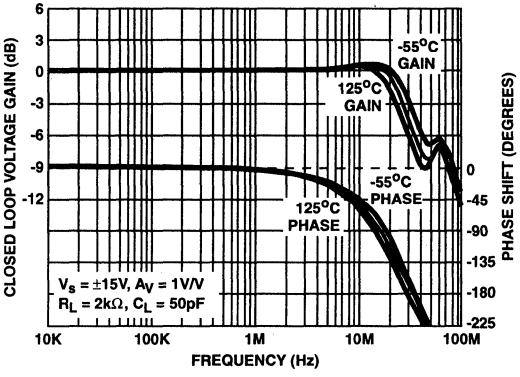


FIGURE 21. HA-5101 FREQUENCY RESPONSE

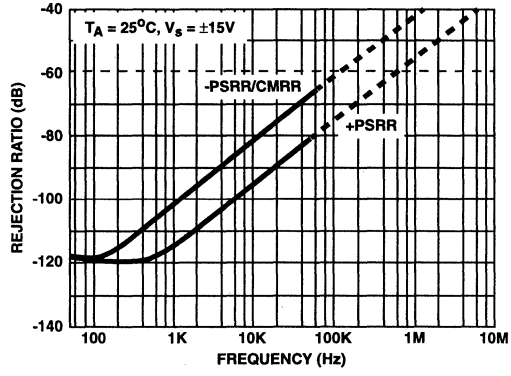


FIGURE 22. HA-5111 REJECTION RATIOS vs FREQUENCY

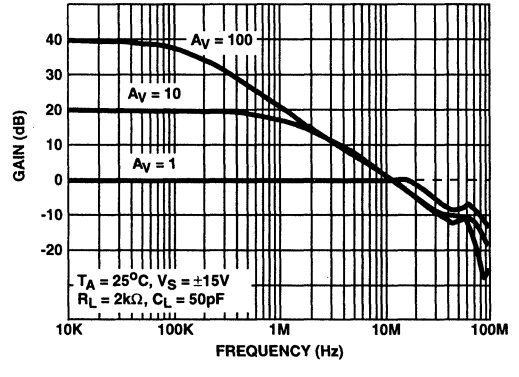


FIGURE 23. HA-5101 CLOSED-LOOP GAIN vs FREQUENCY

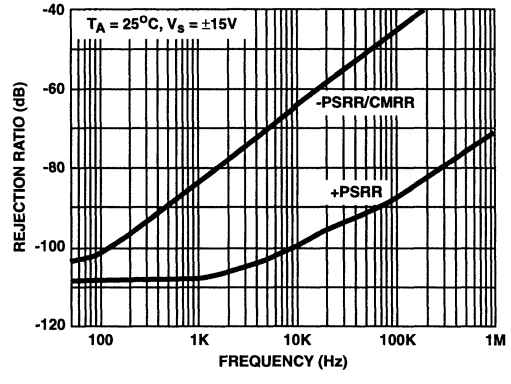


FIGURE 24. HA-5101 REJECTION RATIOS vs FREQUENCY

Typical Performance Curves (Continued)

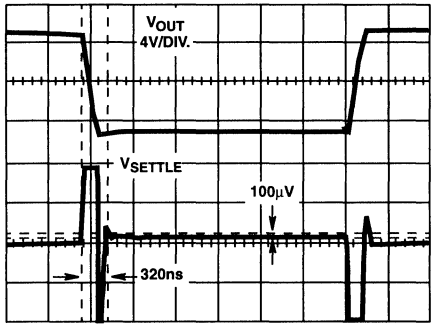


FIGURE 25. HA-5111 SETTLING WAVEFORM 500ns/DIV.

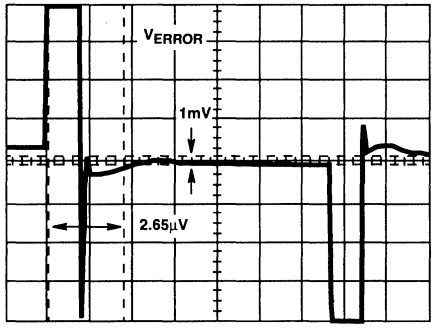


FIGURE 26. HA-5101 SETTLING WAVEFORM 1.5µs/DIV.

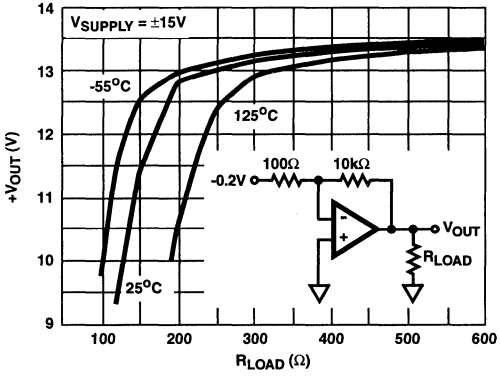


FIGURE 27. HA-5101 $+V_{OUT}$ vs R_L

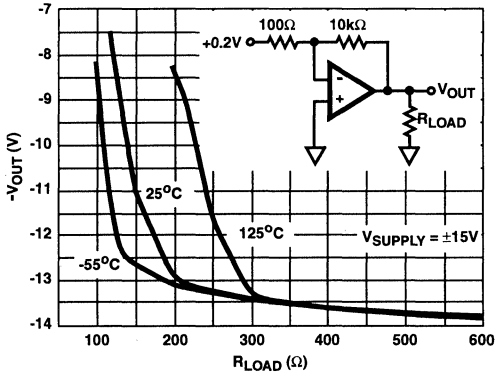


FIGURE 28. HA-5101 $-V_{OUT}$ vs R_L

Die Characteristics

DIE DIMENSIONS:
70 mils x 70 mils x 19 mils
1790µm x 1780µm x 483µm

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:
Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

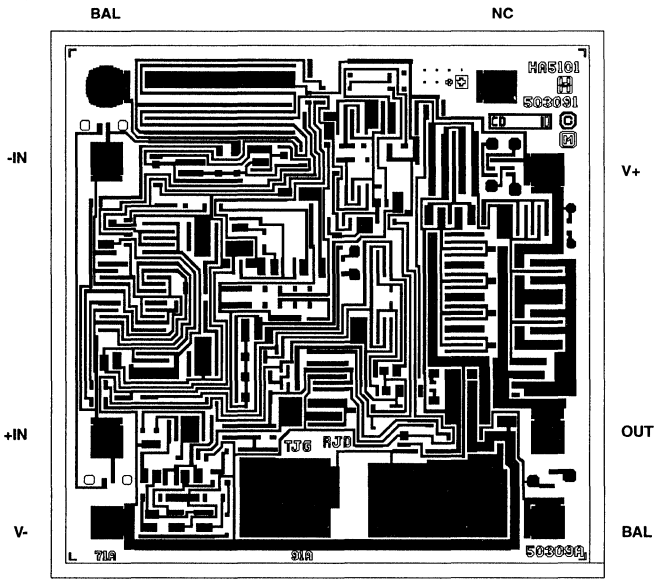
SUBSTRATE POTENTIAL (Powered Up): V-

TRANSISTOR COUNT: 54

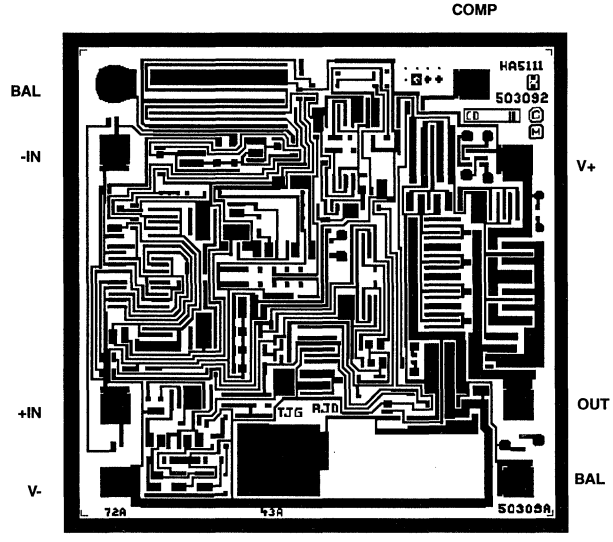
PROCESS: Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5101



HA-5111



HARRIS SEMICONDUCTOR

HA-5102, HA-5104, HA-5112, HA-5114

Dual and Quad, 8MHz and 60MHz, Low Noise Operational Amplifiers

November 1996

Features

- Low Noise . . . . . 4.3nV/√Hz
- Bandwidth . . . . . 8MHz (Compensated)
  60MHz (Uncompensated)
- Slew Rate . . . . . 3V/µs (Compensated)
  20V/µs (Uncompensated)
- Low Offset Voltage 0.5mV
- Available in Duals or Quads

Applications

- Applications
- High Q, Active Filters
- Audio Amplifiers
- Instrumentation Amplifiers
- Integrators
- Signal Generators
- For Further Design Ideas, See Application Note AN554

Description

Low noise and high performance are key words describing HA-5102 and HA-5104, HA-5112, HA-5114. These general purpose amplifiers offer an array of dynamic specifications ranging from a 3V/µs slew rate and 8MHz bandwidth (5102/04) to 20V/µs slew rate and 60MHz gain-bandwidth-product (HA-5112/14). Complementing these outstanding parameters is a very low noise specification of 4.3nV/√Hz at 1kHz.

Fabricated using the Harris high frequency DI process, these operational amplifiers also offer excellent input specifications such as a 0.5mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 60dB channel separation. Consuming a very modest amount of power (90mW/ package for duals and 150mW/package for quads), HA-5102/04/12/14 also provide 15mA of output current.

This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

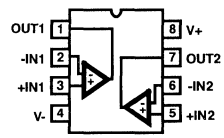
These operational amplifiers are available in dual or quad form with industry standard pinouts allowing form immediate interchangeability with most other dual and quad operational amplifiers

HA-5102	Dual, Comp.	HA-5104	Quad, Comp.
HA-5112	Dual, Uncomp.	HA-5114	Quad, Uncomp.

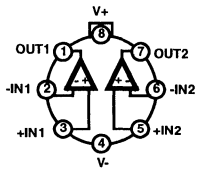
Refer to the /883 data sheet for military product.

Pinouts (See Ordering Information on next page)

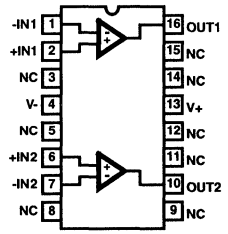
HA-5102/5112 (PDIP, CERDIP)
TOP VIEW



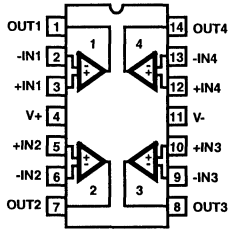
HA-5102 (METAL CAN)
TOP VIEW



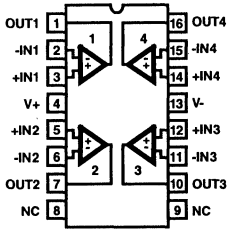
HA-5102/5112 (SOIC)
TOP VIEW



HA-5104/5114 (PDIP, CERDIP)
TOP VIEW



HA5104/5114 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2925.2**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO
HA2-5102-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-5102-5	0 to 75	8 Pin Metal Can	T8.C
HA3-5102-5	0 to 75	8 Ld PDIP	E8.3
HA7-5102-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5102-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P5102-5	0 to 75	16 Ld SOIC	M16.3
HA9P5102-9	-40 to 85	16 Ld SOIC	M16.3
HA1-5104-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-5104-5	0 to 75	14 Ld CERDIP	F14.3
HA3-5104-5	0 to 75	14 Ld PDIP	E14.3
HA9P5104-5	0 to 75	16 Ld SOIC	M16.3
HA9P5104-9	-40 to 85	16 Ld SOIC	M16.3
HA3-5112-5	0 to 75	8 Ld PDIP	E8.3
HA7-5112-2	-55 to 125	8 Ld CERDIP	F8.3A
HA9P5112-5	0 to 75	16 Ld SOIC	M16.3
HA9P5112-9	-40 to 85	16 Ld SOIC	M16.3
HA1-5114-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-5114-5	0 to 75	14 Ld CERDIP	F14.3
HA3-5114-5	0 to 75	14 Ld PDIP	E14.3
HA9P5114-5	0 to 75	16 Ld SOIC	M16.3
HA9P5114-9	-40 to 85	16 Ld SOIC	M16.3

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 40V
Differential Input Voltage. 7V
Input Voltage. . . . . $\pm V_{SUPPLY}$
Output Short Circuit Duration (Note 3) . . . . . Indefinite

Operating Conditions

Temperature Range
HA-5102/5104/5112/5114-2 . . . . . -55°C to 125°C
HA-5102/5104/5112/5114-5 . . . . . 0°C to 75°C
HA-5102/5104/5112/5114-9 . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	165	80
8 Lead PDIP Package	92	N/A
8 Lead CERDIP Package	135	50
SOIC Package (HA-5102, HA-5112)	112	N/A
14 Lead CERDIP Package	80	30
14 Lead PDIP Package	86	N/A
SOIC Package (HA-5104, HA-5114)	96	N/A

Maximum Junction Temperature (Note 1, Ceramic Package) . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below 175°C for hermetic packages, and below 150°C for plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. Any one amplifier may be shorted to ground indefinitely.

Electrical Specifications $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER	TEMP. (°C)	HA-5102-2, -5 HA-5112-2, -5			HA-5104-2, -5 HA-5114-2, -5			HA-5102-9 HA-5112-9			HA-5104-9 HA-5114-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS														
Offset Voltage	25	-	0.5	2.0	-	0.5	2.5	-	0.5	2.0	-	0.5	2.5	mV
	Full	-	-	2.5	-	-	3.0	-	-	2.5	-	-	3.0	mV
Offset Voltage Average Drift	Full	-	3	-	-	3	-	-	3	-	-	3	-	µV/°C
Bias Current	25	-	130	200	-	130	200	-	130	200	-	130	200	nA
	Full	-	-	325	-	-	325	-	-	500	-	-	500	nA
Offset Current	25	-	30	75	-	30	75	-	30	75	-	30	75	nA
	Full	-	-	125	-	-	125	-	-	125	-	-	125	nA
Input Resistance	25	-	500	-	-	500	-	-	500	-	-	500	-	kΩ
Common Mode Range	Full	±12	-	-	±12	-	-	±12	-	-	±12	-	-	V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain ($V_{OUT} = \pm 5V$, $R_L = 2k\Omega$)	25	100	250	-	100	250	-	80	250	-	80	250	-	kV/V
	Full	100	-	-	100	-	-	80	-	-	80	-	-	kV/V
Common Mode Rejection Ratio ($V_{CM} = \pm 5.0V$)	Full	86	95	-	86	95	-	80	95	-	80	95	-	dB
Small Signal Bandwidth HA-5102/5104 ($A_V = 1$)	25	-	8	-	-	8	-	-	8	-	-	8	-	MHz
Gain Bandwidth Product HA-5112/5114 ($A_V = 10$)	25	-	60	-	-	60	-	-	60	-	-	60	-	MHz
Channel Separation (Note 4)	25	-	60	-	-	60	-	-	60	-	-	60	-	dB

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP. (°C)	HA-5102-2, -5 HA-5112-2, -5			HA-5104-2, -5 HA-5114-2, -5			HA-5102-9 HA-5112-9			HA-5104-9 HA-5114-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS														
Output Voltage Swing														
(R_L = 10kΩ)	Full	±12	±13	-	±12	±13	-	±12	±13	-	±12	±13	-	V
(R_L = 2kΩ)	Full	±10	±12	-	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (V_{OUT} = ±5V)	Full	±10	±15	-	±10	±15	-	±7	±15	-	±7	±15	-	mA
Full Power Bandwidth (Note 5)														
HA-5102/5104	25	16	47	-	16	47	-	16	47	-	16	47	-	kHz
HA-5112/5114	25	191	318	-	191	318	-	191	318	-	191	318	-	kHz
Output Resistance	25	-	110	-	-	110	-	-	110	-	-	110	-	Ω
STABILITY														
Minimum Stable Closed Loop Gain														
HA-5102/5104	Full	1	-	-	1	-	-	1	-	-	1	-	-	V/V
HA-5112/5114	Full	10	-	-	10	-	-	10	-	-	10	-	-	V/V
TRANSIENT RESPONSE (Note 6)														
Rise Time														
HA-5102/5104	25	-	108	200	-	108	200	-	108	200	-	108	200	ns
HA-5112/5114	25	-	48	100	-	48	100	-	48	100	-	48	100	ns
Overshoot														
HA-5102/5104	25	-	20	35	-	20	35	-	20	35	-	20	35	%
HA-5112/5114	25	-	30	40	-	30	40	-	30	40	-	30	40	%
Slew Rate														
HA-5102/5104	25	1	3	-	1	3	-	1	3	-	1	3	-	V/µs
HA-5112/5114	25	12	20	-	12	20	-	12	20	-	12	20	-	V/µs
Settling Time (Note 7)														
HA-5102/5104	25	-	4.5	-	-	4.5	-	-	4.5	-	-	4.5	-	µs
HA-5112/5114	25	-	0.6	-	-	0.6	-	-	0.6	-	-	0.6	-	µs
NOISE CHARACTERISTICS (Note 8)														
Input Noise Voltage														
f = 10Hz	25	-	9	25	-	9	25	-	9	25	-	9	25	nV/√Hz
f = 1kHz	25	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	nV/√Hz
Input Noise Current														
f = 10Hz	25	-	5.1	15	-	5.1	15	-	5.1	15	-	5.1	15	pA/√Hz
f = 1kHz	25	-	0.57	3	-	0.57	3	-	0.57	3	-	0.57	3	pA/√Hz
Broadband Noise Voltage														
f = DC to 30kHz	25	-	870	-	-	870	-	-	870	-	-	870	-	nV_{RMS}

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

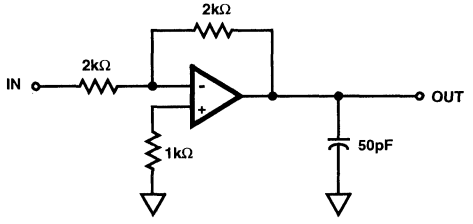
PARAMETER	TEMP. (°C)	HA-5102-2, -5 HA-5112-2, -5			HA-5104-2, -5 HA-5114-2, -5			HA-5102-9 HA-5112-9			HA-5104-9 HA-5114-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS														
Supply Current (All Amps)	25	-	3.0	5.0	-	5.0	6.5	-	3.0	5.0	-	5.0	6.5	mA
Power Supply Rejection Ratio (ΔV_S = ±5V)	Full	86	100	-	86	100	-	80	100	-	80	100	-	dB

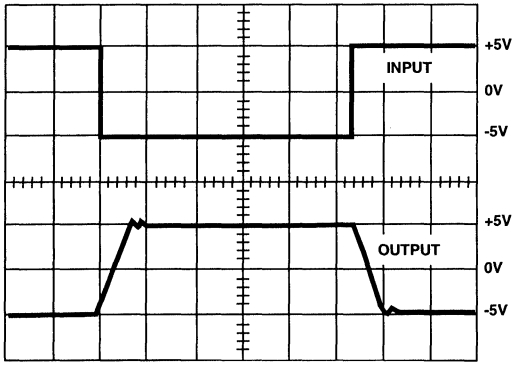
NOTES:

4. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 100mV_{PEAK}; R_S = 1kΩ.
5. Full power bandwidth is guaranteed by equation: Full power bandwidth = $\frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
6. Refer to Test Circuits section of the data sheet.
7. Settling time is measured to 0.1% of final value for a 1V input step, and A_V = -10 for HA-5112/5114, and a 10V input step, A_V = -1 for HA-5102/5104.
8. The limits for these parameters are guaranteed based on lab characterization, and reflect lot-to-lot variation.

Test Circuits and Waveforms

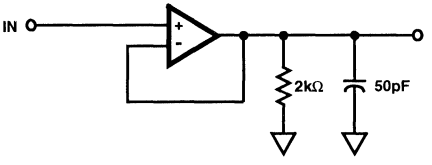
HA-5102, HA-5104

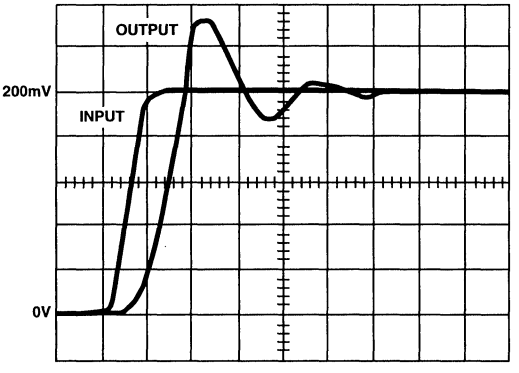




Vertical = 5V/Div., Horizontal = 5µs/Div. (A_V = -1)

FIGURE 1. LARGE SIGNAL RESPONSE CIRCUIT



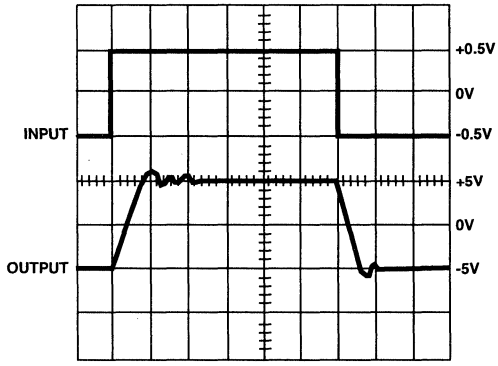


Vertical = 40mV/Div., Horizontal = 50ns/Div. (A_V = +1)

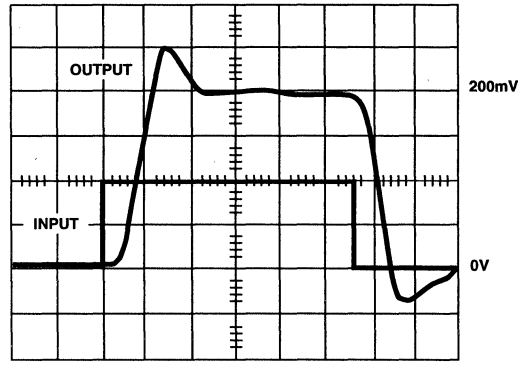
FIGURE 2. SMALL SIGNAL RESPONSE CIRCUIT

Test Circuits and Waveforms (Continued)

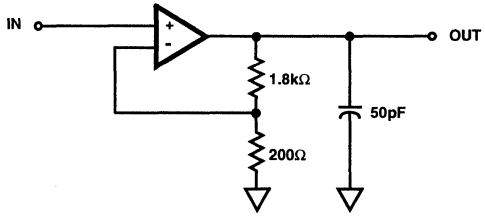
HA-5112, HA-5114



Input = 0.5V/Div., Output = 5V/Div., Time = 50ns/Div.

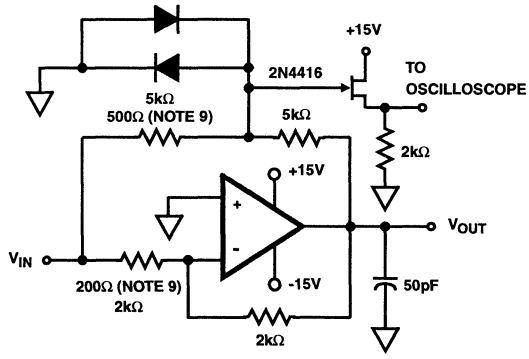


Input = 10mV/Div., Output = 50mV/Div., Time = 50ns/Div.



NOTE: A_V = +10.

FIGURE 3. LARGE AND SMALL SIGNAL RESPONSE CIRCUIT (A_V = +10)

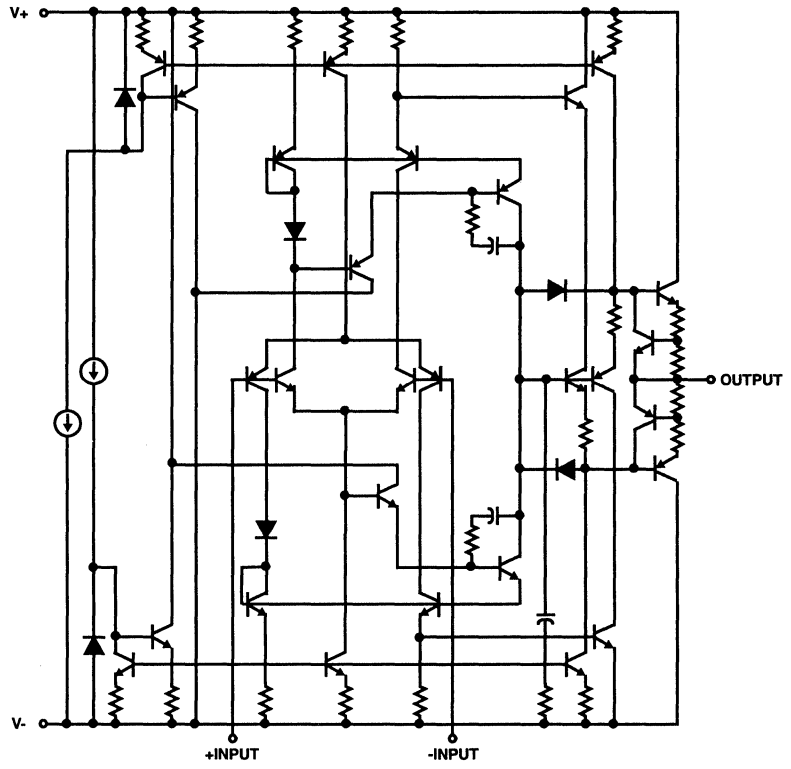


NOTES:

9. A_V = -1 (HA-5102/5104), A_V = -10 (HA-5112/5114).
10. Feedback and summing resistors should be 0.1% matched.
11. Clipping diodes are optional, HP5082-2810 recommended.

FIGURE 4. SETTLING TIME CIRCUIT

Simplified Schematic



Typical Performance Curves

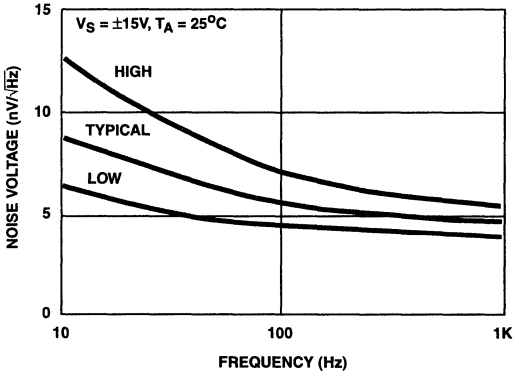


FIGURE 5. INPUT NOISE VOLTAGE DENSITY

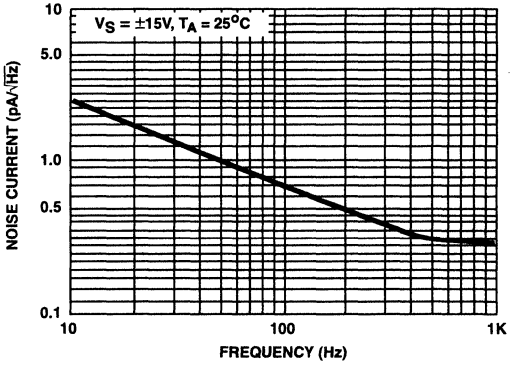
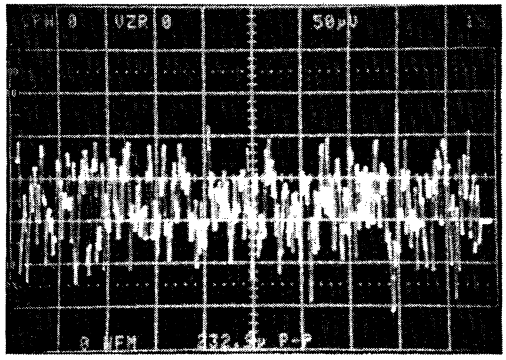


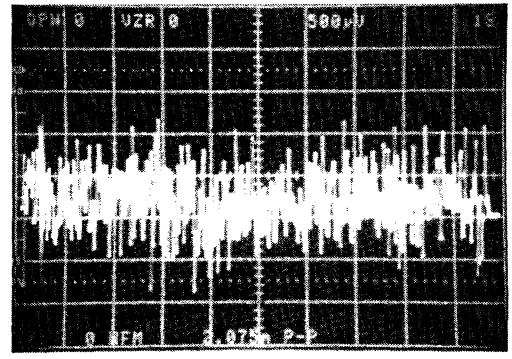
FIGURE 6. INPUT NOISE CURRENT DENSITY

Typical Performance Curves (Continued)



$V_S = \pm15V$, $T_A = 25^oC$, 50µV/Div., 1s/Div., $A_V = 1000V/V$
Input Noise = $0.232\mu V_{P-P}$

FIGURE 7. 0.1Hz TO 10Hz NOISE



$V_S = \pm15V$, $T_A = 25^oC$, 500µV/Div., 1s/Div., $A_V = 1000V/V$
Total Output Noise = $2.075\mu V_{P-P}$

FIGURE 8. 0.1Hz TO 1MHz NOISE

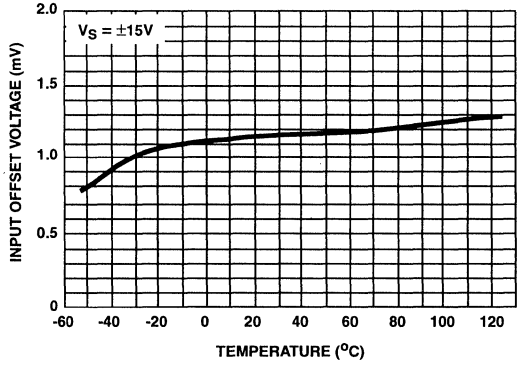


FIGURE 9. V_{IO} vs TEMPERATURE

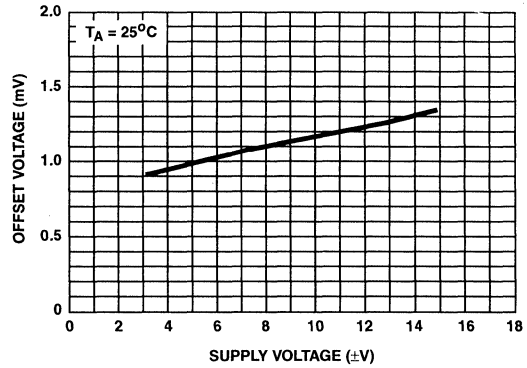


FIGURE 10. V_{IO} vs V_S

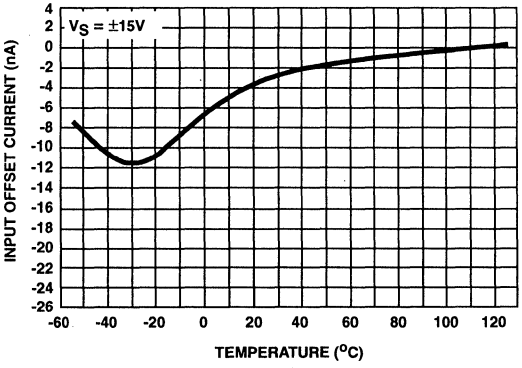


FIGURE 11. I_{IO} vs TEMPERATURE

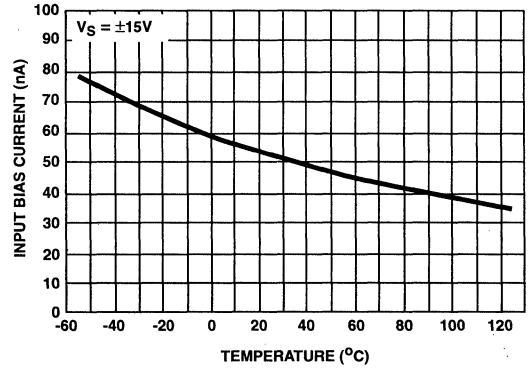


FIGURE 12. I_{BIAS} vs TEMPERATURE

Typical Performance Curves (Continued)

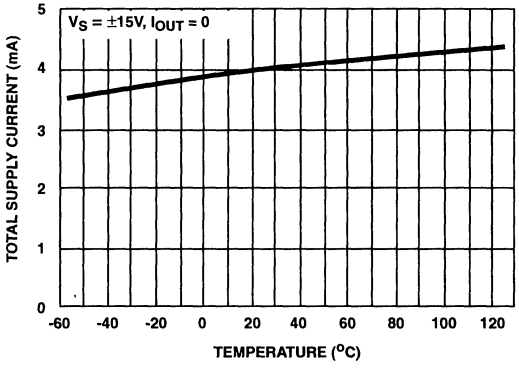


FIGURE 13. I_{CC} vs TEMPERATURE (HA-5104/14)

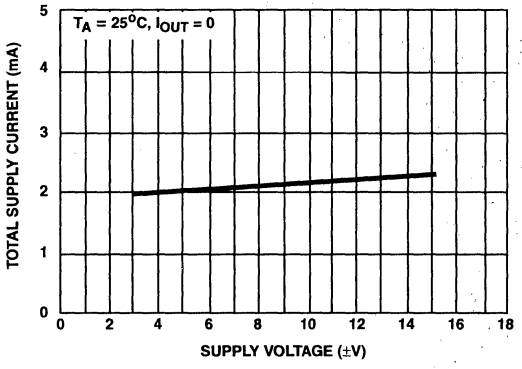


FIGURE 14. I_{CC} vs V_S (HA-5102/12)

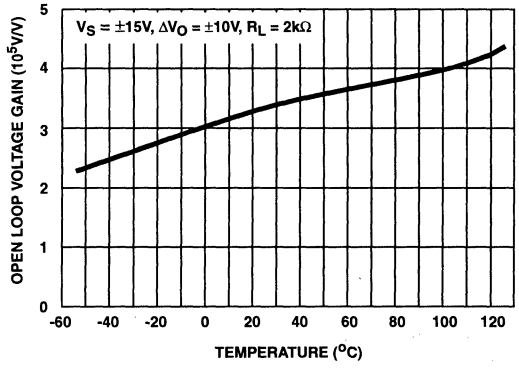


FIGURE 15. A_{VOL} vs TEMPERATURE

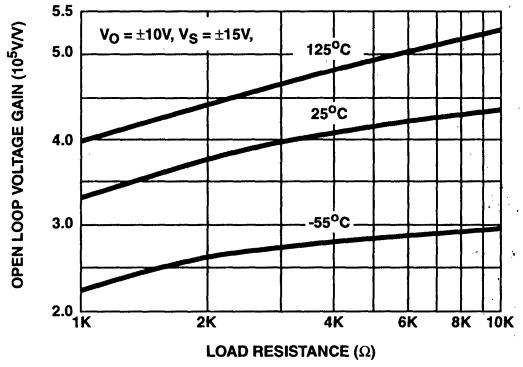


FIGURE 16. A_{VOL} vs LOAD RESISTANCE

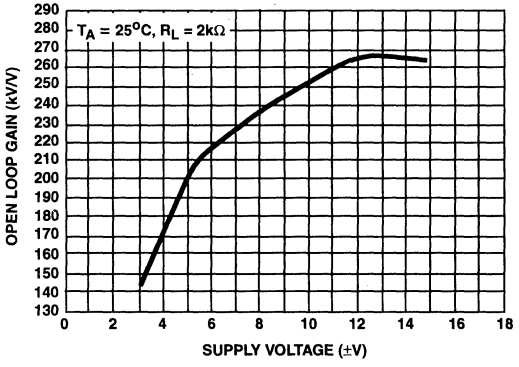


FIGURE 17. A_{VOL} vs V_S

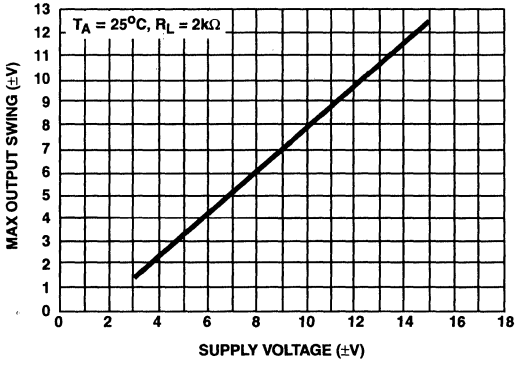


FIGURE 18. V_{OUT} vs V_S

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued)

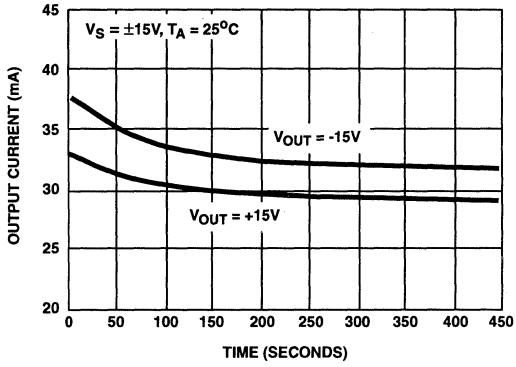


FIGURE 19. OUTPUT SHORT CIRCUIT CURRENT vs TIME

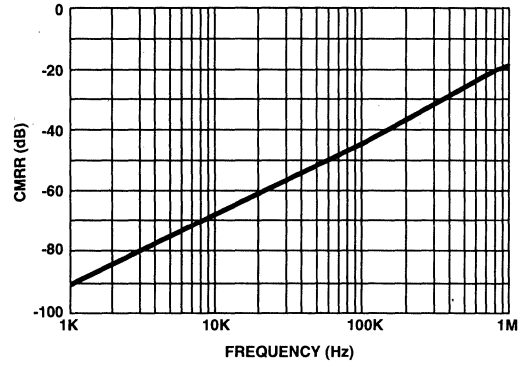


FIGURE 20. CMRR vs FREQUENCY

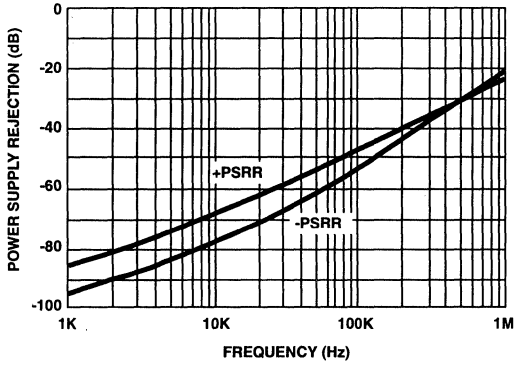


FIGURE 21. PSRR vs FREQUENCY

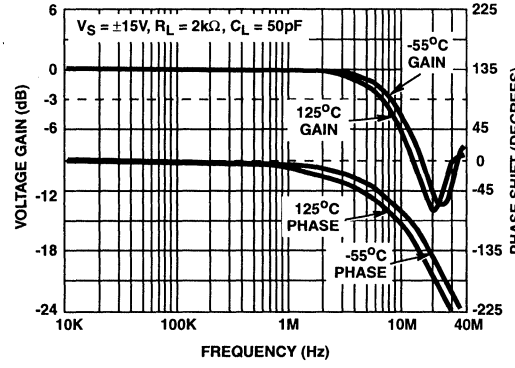


FIGURE 22. HA-5104/02 UNITY GAIN FREQUENCY RESPONSE

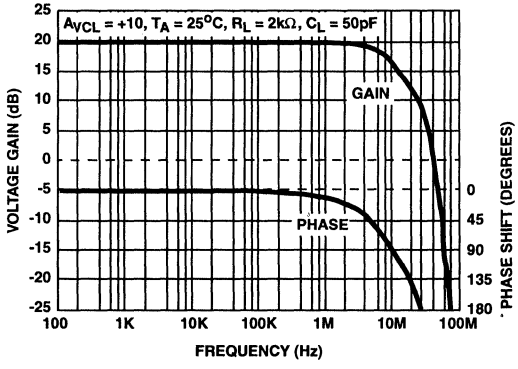


FIGURE 23. HA-5112/14 FREQUENCY RESPONSE

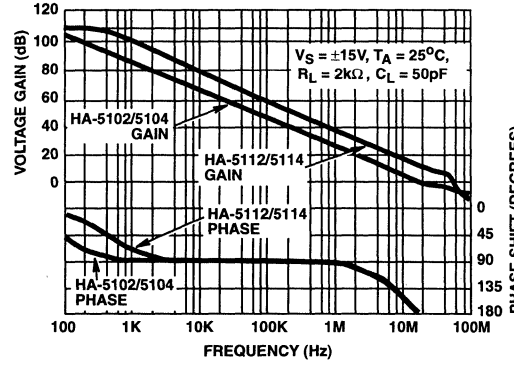


FIGURE 24. OPEN LOOP GAIN vs FREQUENCY

Typical Performance Curves (Continued)

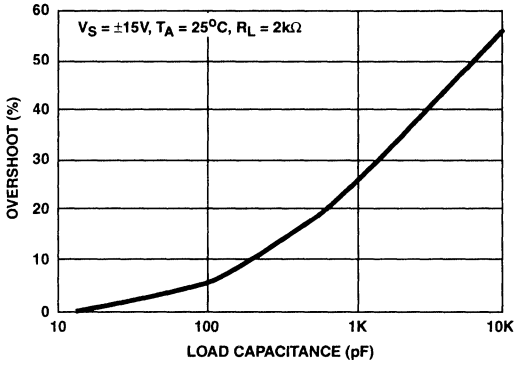


FIGURE 25. SMALL SIGNAL OVERSHOOT vs C_{LOAD}

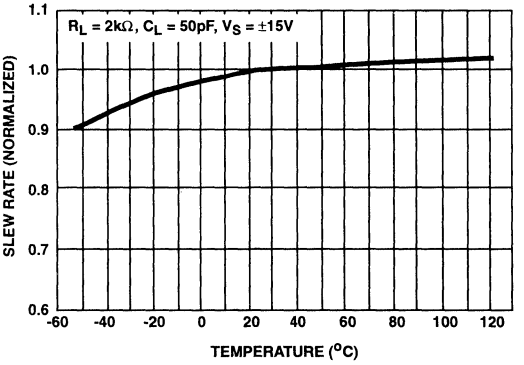


FIGURE 26. SLEW RATE vs TEMPERATURE

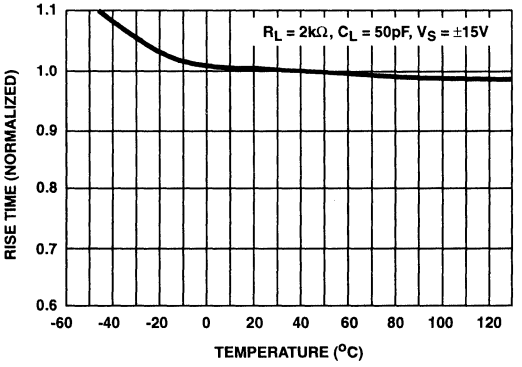


FIGURE 27. RISE TIME vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

98.4 mils x 67.3 mils x 19 mils
2500µm x 1710µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

TRANSISTOR COUNT:

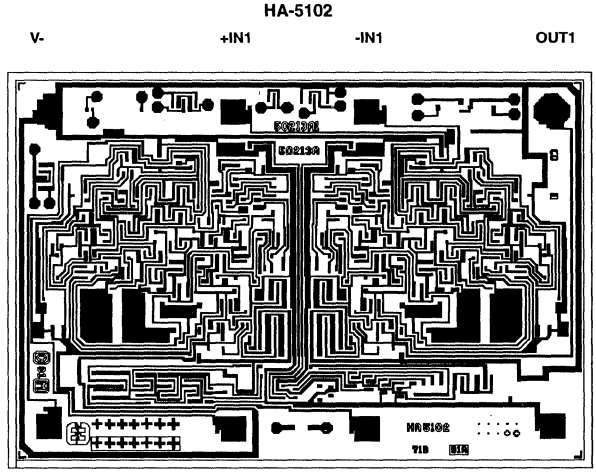
93

PROCESS:

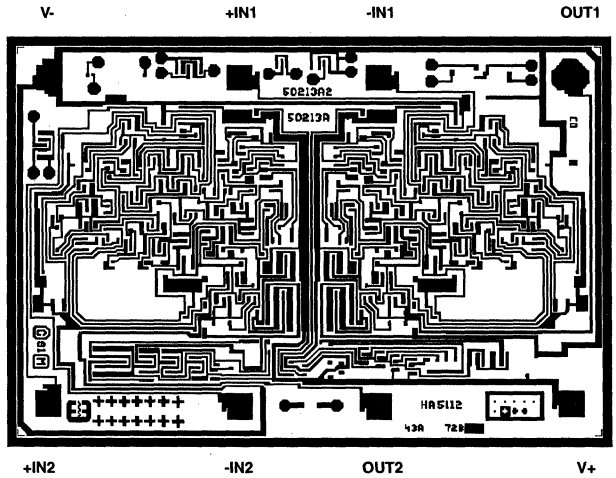
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5102



HA-5112



Die Characteristics

DIE DIMENSIONS:

95 mils x 99 mils x 19 mils
2420µm x 2530µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

TRANSISTOR COUNT:

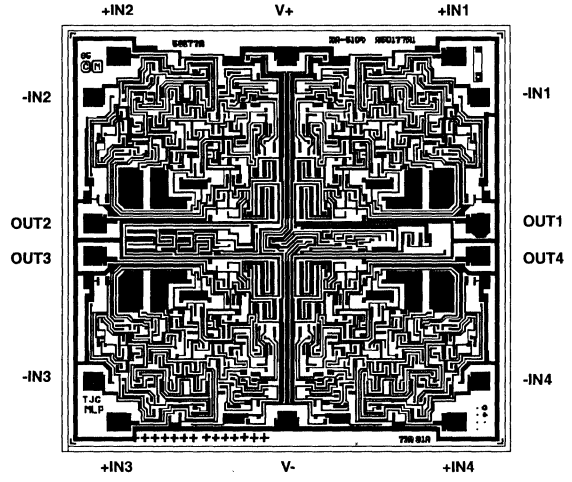
175

PROCESS:

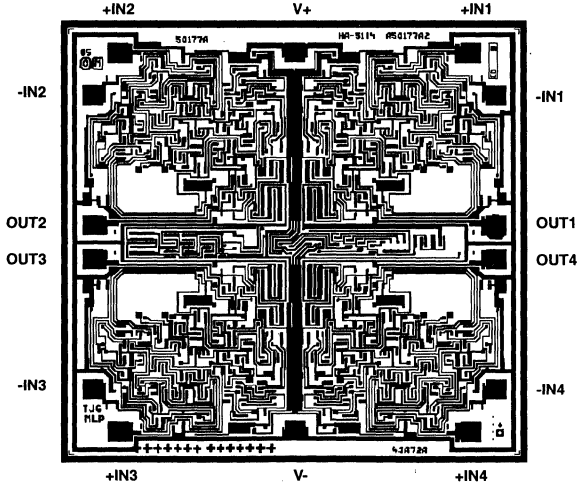
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5104



HA-5114



HARRIS SEMICONDUCTOR

HA-5127, HA-5127A

8.5MHz, Ultra-Low Noise Precision Operational Amplifier

November 1996

Features

- Slew Rate 10V/μs
- Unity Gain Bandwidth 8.5MHz
- Low Noise ..... 3nV/√Hz at 1kHz
- Low V_{OS} 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3-5127-5	0 to 75	8 Ld PDIP	E8.3
HA3-5127A-5	0 to 75	8 Ld PDIP	E8.3
HA7-5127-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5127-5	0 to 75	8 Ld CERDIP	F8.3A
HA7-5127A-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5127A-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P5127-5 (H51275)	0 to 75	8 Ld SOIC	M8.15

Description

The HA-5127 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/√Hz) precision instrumentation performance with high speed (10V/μs) wideband capability.

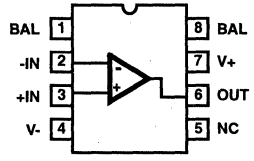
This amplifier's impressive list of features include low V_{OS} (10μV), wide unity gain-bandwidth (8.5MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

Using the HA-5127 allows designers to minimize errors while maximizing speed and bandwidth.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5127's qualities include instrumentation amplifiers, pulse amplifiers, audio preamplifiers, and signal conditioning circuits. This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37. For the military grade product, refer to the HA-5127/883 data sheet.

Pinout

HA-5127
(PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1996

File Number **2906.2**

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 3) 0.7V
Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-5127/27A-2 . . . . . $-55^{o}C$ to $125^{o}C$
HA5127/27A-5 . . . . . $0^{o}C$ to $75^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
CERDIP Package	135	50
PDIP Package	92	N/A
SOIC Package	157	N/A

Maximum Junction Temperature (Ceramic Package, Note 1) . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load must be designed to maintain the maximum junction temperature below $175^{o}C$ for Hermetic packages, and below $150^{o}C$ for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L < 50pF$, $R_S < 100\Omega$

PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	HA-5127A			HA-5127			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	10	25	-	30	100	µV
		Full	-	30	60	-	70	300	µV
Average Offset Voltage Drift		Full	-	0.2	0.6	-	0.4	1.8	µV/^{o}C
Bias Current		25	-	±10	±40	-	±15	±80	nA
		Full	-	±20	±60	-	±35	±150	nA
Offset Current		25	-	7	35	-	12	75	nA
		Full	-	15	50	-	30	135	nA
Common Mode Range		Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 4)		25	1.5	6	-	0.8	4	-	MΩ
Input Noise Voltage (Note 5)	0.1Hz to 10Hz	25	-	0.08	0.18	-	0.09	0.25	μV_{P-P}
Input Noise Voltage Density (Note 6)	f = 10Hz	25	-	3.5	8.0	-	3.8	8.0	nV/$\sqrt{Hz}$
	f = 100Hz		-	3.1	4.5	-	3.3	4.5	nV/$\sqrt{Hz}$
	f = 1000Hz		-	3.0	3.8	-	3.2	3.8	nV/$\sqrt{Hz}$
Input Noise Current Density (Note 6)	f = 10Hz	25	-	1.7	4.0	-	1.7	-	pA/$\sqrt{Hz}$
	f = 100Hz		-	1.0	2.3	-	1.0	-	pA/$\sqrt{Hz}$
	f = 1000Hz		-	0.4	0.6	-	0.4	0.6	pA/$\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 2k\Omega$	25	1000	1800	-	700	1500	-	V/mV
		Full	600	1200	-	300	800	-	V/mV
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	Full	114	126	-	100	120	-	dB
Minimum Stable Gain		25	1	-	-	1	-	-	V/V
Unity-Gain-Bandwidth		25	5	8.5	-	5	8.5	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 600\Omega$	25	±10.0	±11.5	-	±10.0	±11.5	-	V
	$R_L = 2k\Omega$	Full	±11.7	±13.8	-	±11.5	±13.5	-	V
Full Power Bandwidth (Note 7)		25	111	160	-	111	160	-	kHz
Output Resistance	Open Loop	25	-	70	-	-	70	-	Ω
Output Current		25	16.5	25	-	16.5	25	-	mA
TRANSIENT RESPONSE (Note 8)									
Rise Time		25	-	-	150	-	-	150	ns
Slew Rate	$V_{OUT} = 10V$	25	7	10	-	7	10	-	V/µs

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L < 50pF$, $R_S < 100\Omega$ **(Continued)**

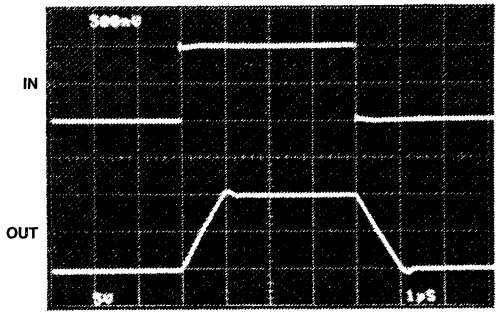
PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5127A			HA-5127			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time (Note 9)		25	-	1.5	-	-	1.5	-	µs
Overshoot		25	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	3.5	-	-	3.5	-	mA
		Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	Full	-	2	4	-	16	51	µV/V

NOTES:

4. This parameter value is based upon design calculations.
5. Refer to Typical Performance Curves.
6. The limits for this parameter are guaranteed based on lab characterization, and reflect lot-to-lot variation.
7. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of the data sheet.
9. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -1$.

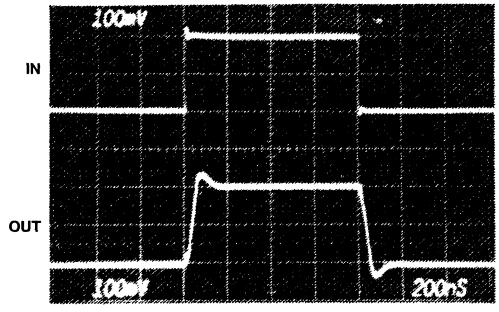
Test Circuits and Waveforms

FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUITS



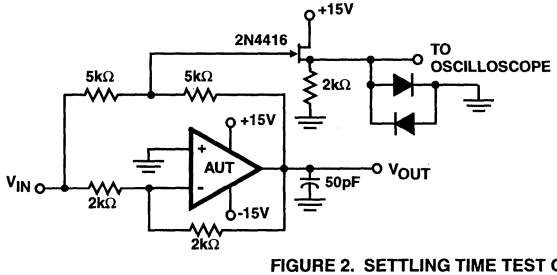
Vertical Scale: Input = 0.5V/Div., Output = 5V/Div.
Horizontal Scale: 1µs/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: 100mV/Div.
Horizontal Scale: 200ns/Div.

SMALL SIGNAL RESPONSE

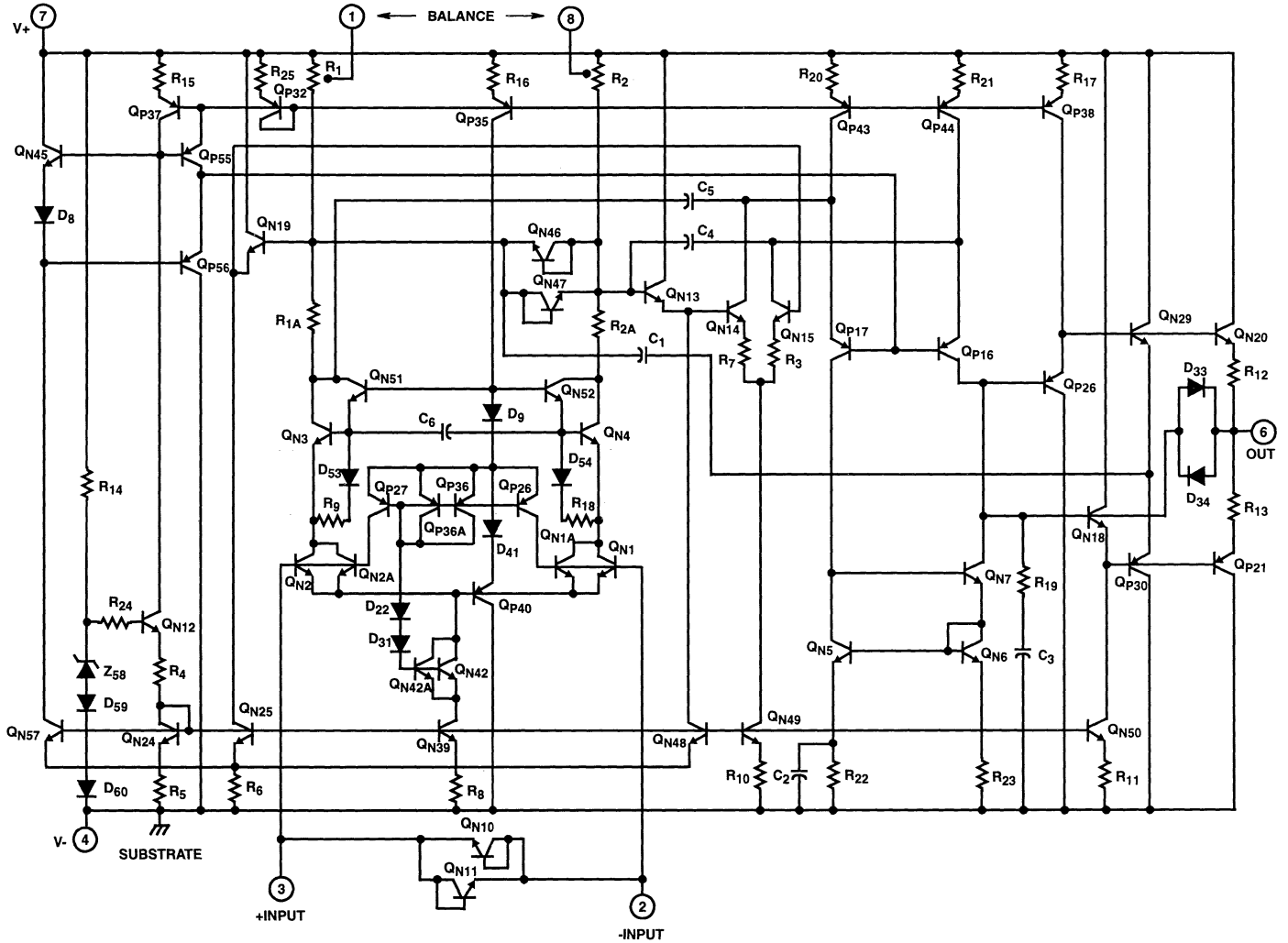


NOTES:

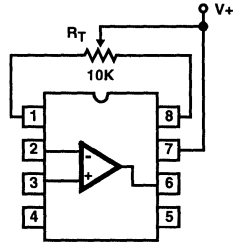
10. $A_V = -1$.
11. Feedback and summing resistors should be 0.1% matched.
12. Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram



Application Information



NOTE: Tested Offset Adjustment Range is $|V_{OS}$ + 1mV| minimum referred to output. Typical range is ±4mV with R_T = 10kΩ.

FIGURE 3. SUGGESTED OFFSET VOLTAGE ADJUSTMENT

Low resistances are preferred for low noise applications as a 1kΩ resistor has 4nV/√Hz of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 4. SUGGESTED STABILITY CIRCUITS

Typical Performance Curves Unless Otherwise Specified: T_A = 25°C, V_{SUPPLY} = ±15V

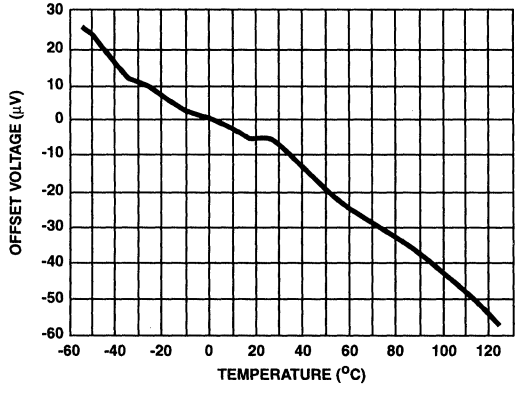


FIGURE 5. TYPICAL OFFSET VOLTAGE DRIFT vs TEMPERATURE

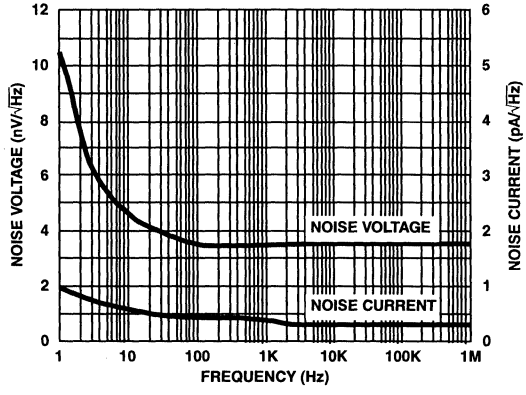


FIGURE 6. NOISE CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$ (Continued)

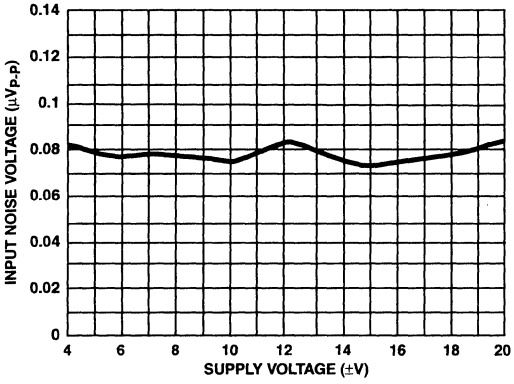


FIGURE 7. NOISE vs SUPPLY VOLTAGE

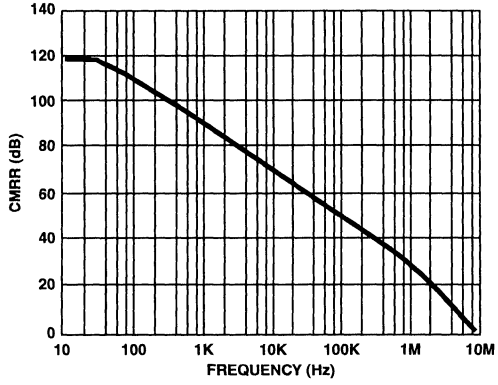


FIGURE 8. CMRR vs FREQUENCY

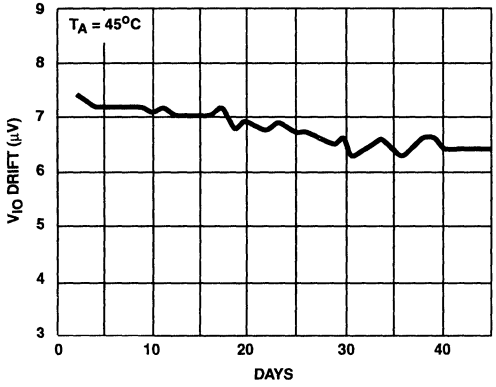


FIGURE 9. OFFSET VOLTAGE DRIFT vs TIME

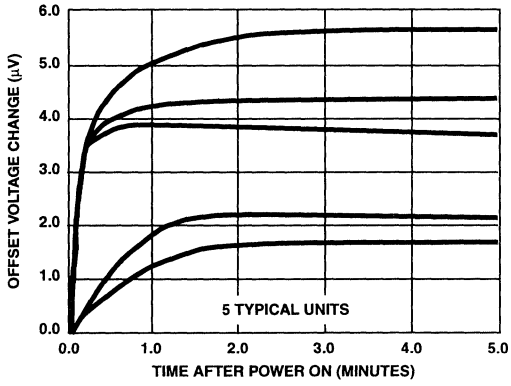


FIGURE 10. OFFSET VOLTAGE WARM UP DRIFT

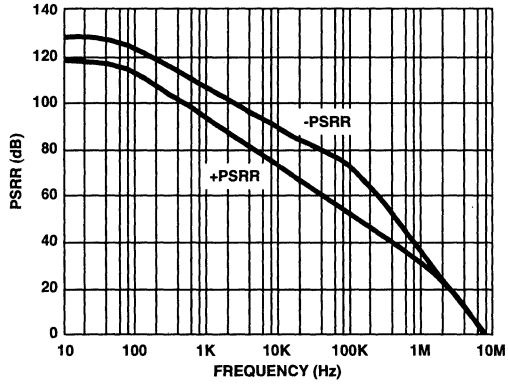


FIGURE 11. PSRR vs FREQUENCY

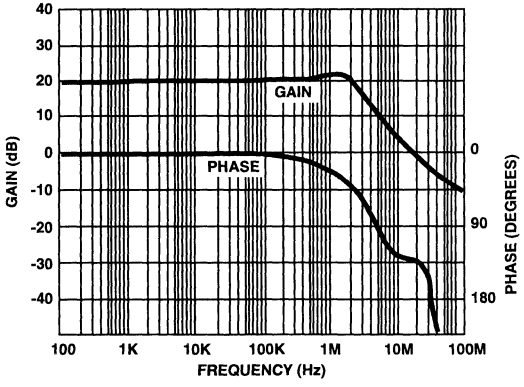


FIGURE 12. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$ (Continued)

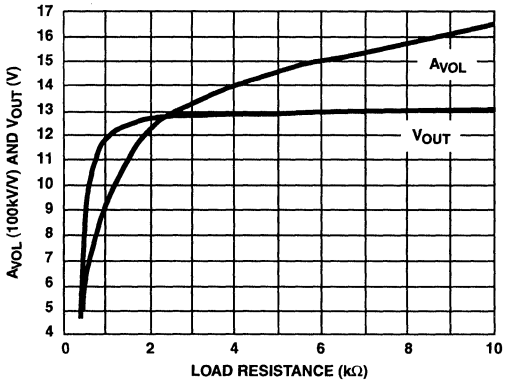


FIGURE 13. A_{VOL} AND V_{OUT} vs LOAD RESISTANCE

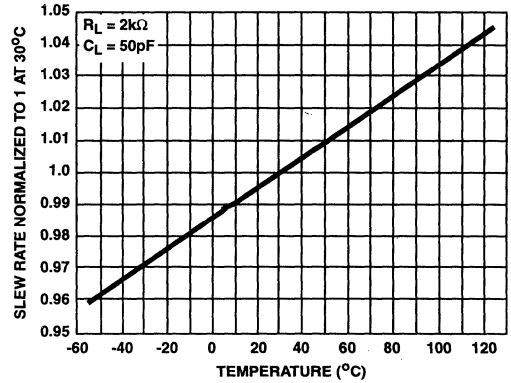


FIGURE 14. NORMALIZED SLEW RATE vs TEMPERATURE

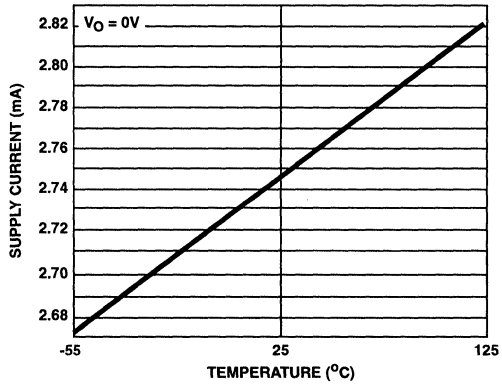


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

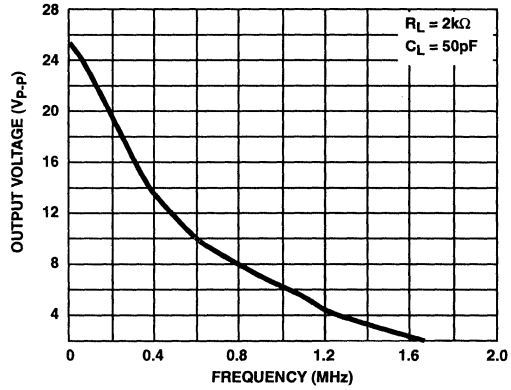


FIGURE 16. MAX UNDISTORTED SINEWAVE OUTPUT vs FREQUENCY

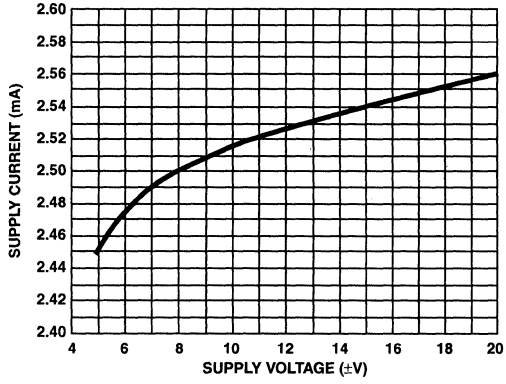


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

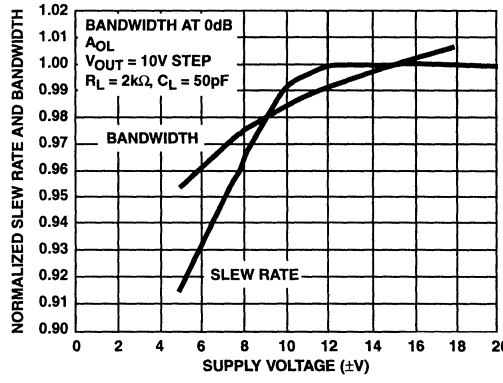


FIGURE 18. BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$ (Continued)

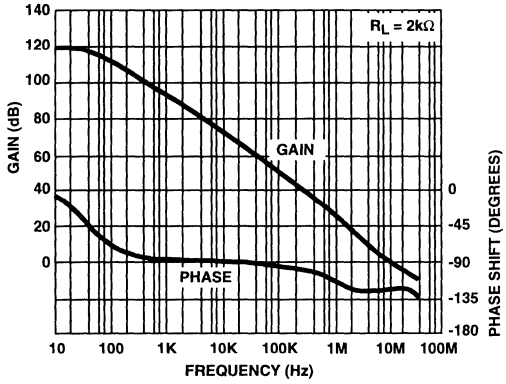


FIGURE 19. OPEN LOOP GAIN AND PHASE

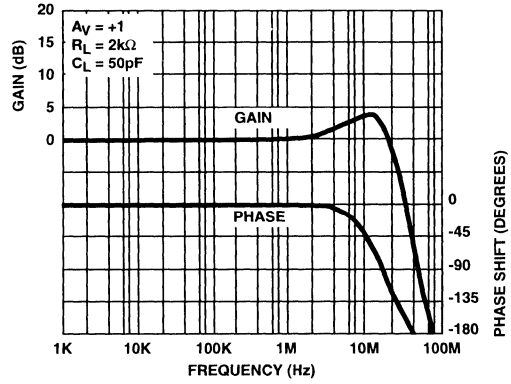
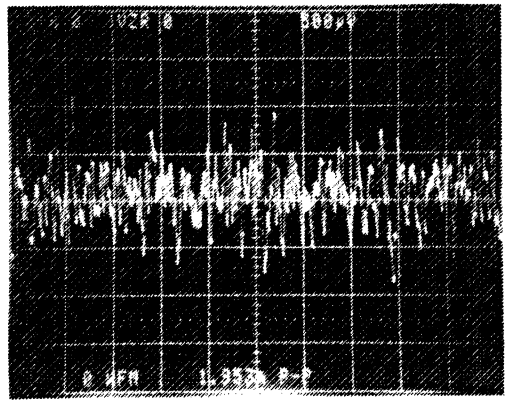


FIGURE 20. CLOSED LOOP GAIN AND PHASE



Horizontal Scale = 1s/Div.
Vertical Scale = 0.002μV/Div.
A_{CL} = 25,000V/V, E_N = 0.08μV_{P-P} RTI

FIGURE 21. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)

Die Characteristics

DIE DIMENSIONS:

104 mils x 65 mils x 19 mils
2650µm x 1650µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

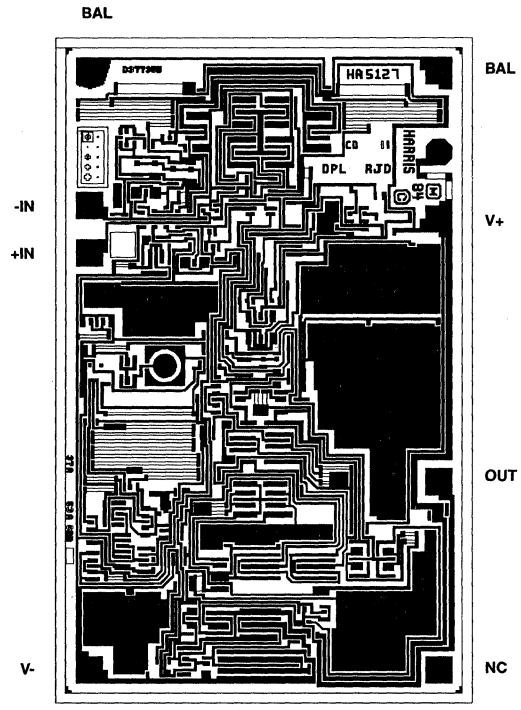
63

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5127



HA-5130, HA-5135

November 1996

2.5MHz, Precision Operational Amplifiers

Features

- Low Offset Voltage..... 25μV (Max)
- Low Offset Voltage Drift ..... 0.4μV/°C
- Low Noise..... 9nV/√Hz
- Open Loop Gain..... 140dB
- Unity Gain Bandwidth 2.5MHz
- All Bipolar Construction

Applications

- High Gain Instrumentation
- Precision Data Acquisition
- Precision Integrators
- Biomedical Amplifiers
- Precision Threshold Detectors

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-5130-5	0 to 75	8 Pin Metal Can	T8.C
HA2-5135-5	0 to 75	8 Pin Metal Can	T8.C
HA7-5130-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5130-5	0 to 75	8 Ld CERDIP	F8.3A
HA7-5135-2	-55 to 125	8 Ld CERDIP	E8.3A
HA7-5135-5	0 to 75	8 Ld CERDIP	E8.3A

Description

The Harris HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

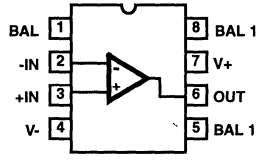
A Super Beta input stage is combined with laser trimming, dielectric isolation and matching techniques to produce 25μV (Maximum) input offset voltage and 0.4μV/°C input offset voltage average drift. Other features enhanced by this process include 9nV/√Hz (Typ.) Input Noise Voltage, 1nA Input Bias Current and 140dB Open Loop Gain.

These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, make this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

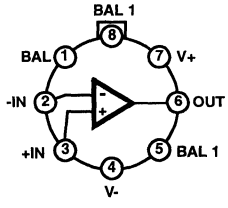
HA-5130/5135 offers added features over the industry standard OP-07 in regards to bandwidth and slew rate specifications. For the military grade product, refer to the HA-5135/883 data sheet.

Pinouts

HA-5130/5135 (CERDIP)
TOP VIEW



HA-5130/5135 (METAL CAN)
TOP VIEW



NOTE: Both BAL 1 pins are connected together internally.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage. 7V
Output Short Circuit Duration . . . . . Indefinite

Operating Conditions

Temperature Ranges
HA-5130/5135-2 . . . . . -55°C to 125°C
HA-5130/5135-5 . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	135	50
Metal Can Package	165	80

Maximum Junction Temperature (Note 1) . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below 175°C.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 15V$

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5130-2/-5			HA-5135-2/-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	10	25	-	10	75	µV
		Full	-	50	60	-	50	130	µV
Average Offset Voltage Drift		Full	-	0.4	0.6	-	0.4	1.3	µV/°C
Bias Current		25	-	±1	±2	-	±1	±4	nA
		Full	-	-	±4	-	-	±6	nA
Bias Current Average Drift		Full	-	0.02	0.04	-	0.02	0.04	nA/°C
Offset Current		25	-	-	2	-	-	4	nA
		Full	-	-	4	-	-	5.5	nA
Offset Current Average Drift		Full	-	0.02	0.04	-	0.02	0.04	nA/°C
Common Mode Range		Full	±12	-	-	±12	-	-	V
Differential Input Resistance		25	20	30	-	20	30	-	MΩ
Input Noise Voltage (Note 3)	0.1Hz to 10Hz	25	-	-	0.6	-	-	0.6	μV_{P-P}
Input Noise Voltage Density (Note 3)	f = 10Hz	25	-	13.0	18.0	-	13.0	18.0	$nV/\sqrt{Hz}$
	f = 100Hz		-	10.0	13.0	-	10.0	13.0	$nV/\sqrt{Hz}$
	f = 1000Hz		-	9.0	11.0	-	9.0	11.0	$nV/\sqrt{Hz}$
Input Noise Current (Note 3)	0.1Hz to 10Hz	25	-	15	30	-	15	30	pA_{P-P}
Input Noise Current Density (Note 3)	f = 10Hz	25	-	0.4	0.8	-	0.4	0.8	$pA/\sqrt{Hz}$
	f = 100Hz		-	0.17	0.23	-	0.17	0.23	$pA/\sqrt{Hz}$
	f = 1000Hz		-	0.14	0.17	-	0.14	0.17	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2k\Omega$	25	120	140	-	120	140	-	dB
		Full	120	-	-	120	-	-	dB
Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	Full	110	120	-	106	120	-	dB
Closed Loop Bandwidth	$A_{VCL} = +1$	25	0.6	2.5	-	0.6	2.5	-	MHz

Electrical Specifications $V_{SUPPLY} = \pm15V$ (Continued)

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5130-2/-5			HA-5135-2/-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 600\Omega$	25	±10	±12	-	±10	±12	-	V
		Full	±10	-	-	±10	-	-	V
Full Power Bandwidth (Note 4)	$R_L = 2k\Omega$	25	8	10	-	8	10	-	kHz
Output Current	$V_{OUT} = 10V$	25	±15	±20	-	±15	±20	-	mA
Output Resistance	Note 5	25	-	45	-	-	45	-	Ω
TRANSIENT RESPONSE (Note 6)									
Rise Time		25	-	340	-	-	340	-	ns
Slew Rate		25	0.5	0.8	-	0.5	0.8	-	V/µs
Settling Time (Note 7)		25	-	11	-	-	11	-	µs
POWER SUPPLY CHARACTERISTICS									
Supply Current		Full	-	1.0	1.7	-	1.0	1.7	mA
Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm20V$	Full	100	130	-	94	130	-	dB

NOTES:

3. Not tested. 90% of units meet or exceed these specifications.
4. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
5. Output resistance measured under open loop conditions (f = 100Hz).
6. Refer to test circuits section of the data sheet.
7. Settling time is measured to 0.1% of final value for a 10V output step and $A_V = -1$.

Test Circuits and Waveforms

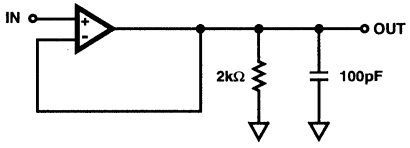
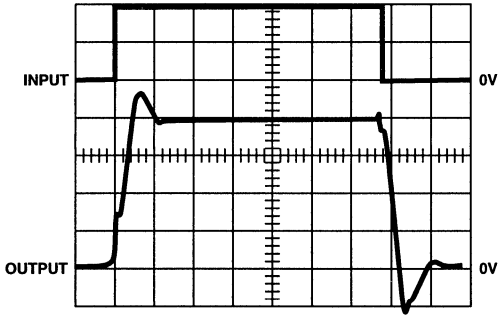
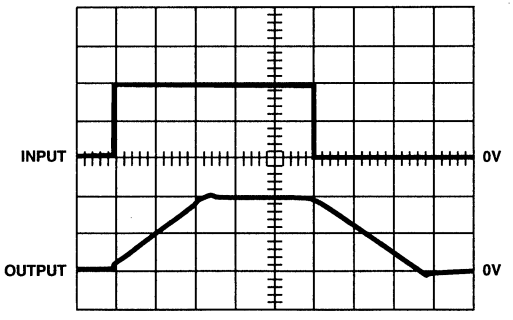


FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



Vertical Scale: Input = 50mV/Div. Output = 100mV/Div.
Horizontal Scale: 1µs/Div.

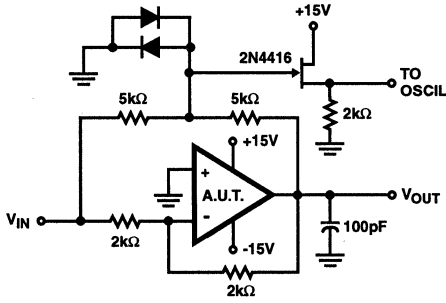
SMALL SIGNAL RESPONSE



Vertical Scale: 5V/Div.
Horizontal Scale: 5µs/Div.

LARGE SIGNAL RESPONSE

Test Circuits and Waveforms (Continued)

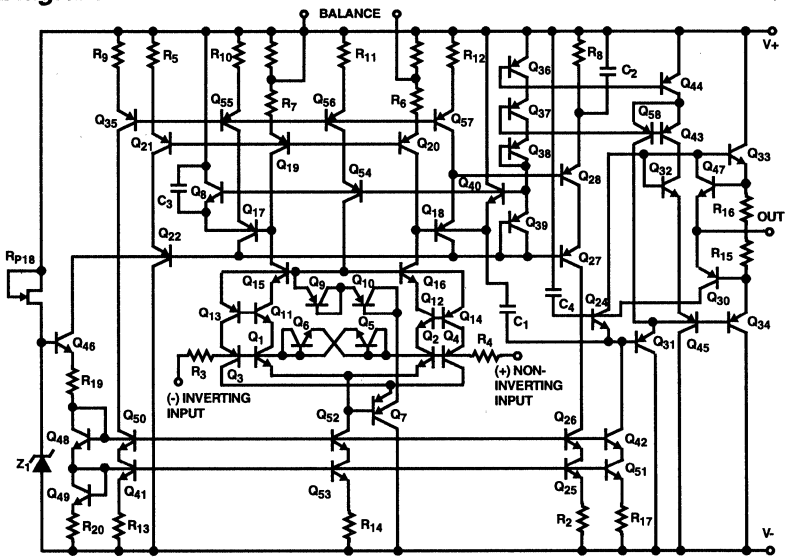


NOTES:

8. $A_V = -1$.
9. Feedback and summing resistors should be 0.1% matched.
10. Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME CIRCUIT

Schematic Diagram



Application Information

Power Supply Decoupling

Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

Considerations For Prototyping:

The following list of recommendations are suggested for prototyping.

1. Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
2. Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuity from heat generating components is recommended.
3. Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.

Large Capacitive Loads

When driving large capacitive loads (>500pF), a small value resistor (≈50Ω) should be connected in series with the output and inside the feedback loop.

Offset Voltage Adjustment (See Figure 3)

A 20kΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10kΩ, 50kΩ and 100kΩ may be used. The minimum adjustment range for given values is ±2mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}. Tested Offset Adjustment is $|V_{OS}| + 1mV|$ minimum referred to output.

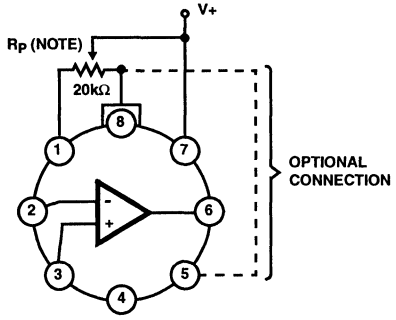


FIGURE 3. OFFSET NULLING CONNECTIONS

Saturation Recovery

Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.

Differential Input Voltages

Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of 1V are applied between the inputs, the use of limiting resistors at the inputs is recommended.

Typical Applications

The excellent input and gain characteristics of HA-5130 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-5130, virtually nullifies the need for more expensive chopper-type amplifiers.

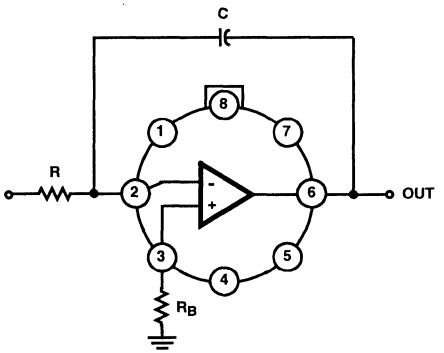
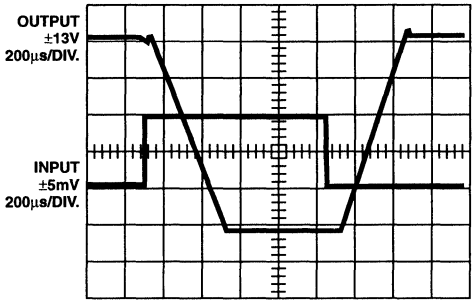


FIGURE 4. PRECISION INTEGRATOR

Low V_{OS} coupled with high open loop Gain, high CMRR and high PSRR make HA-5130 ideally suited for precision detector applications, such as the zero crossing detector shown in Figure 5.



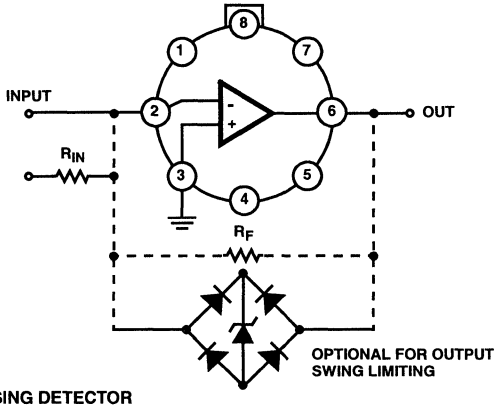


FIGURE 5. ZERO CROSSING DETECTOR

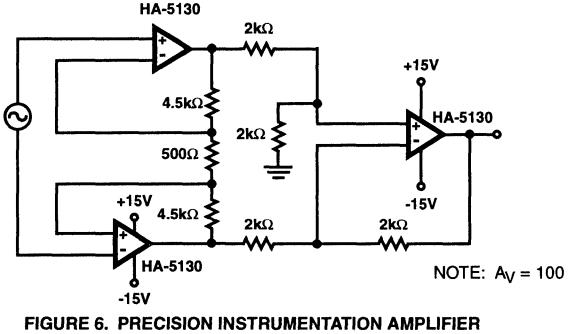


FIGURE 6. PRECISION INSTRUMENTATION AMPLIFIER

Typical Performance Curves

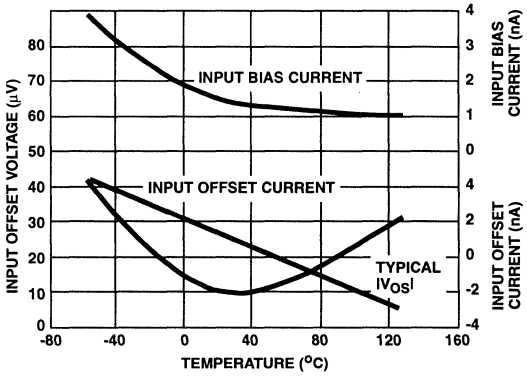


FIGURE 7. INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

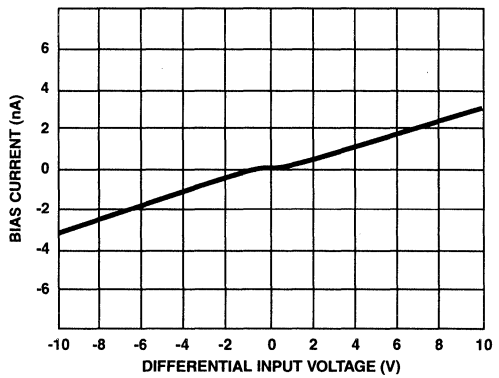


FIGURE 8. INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

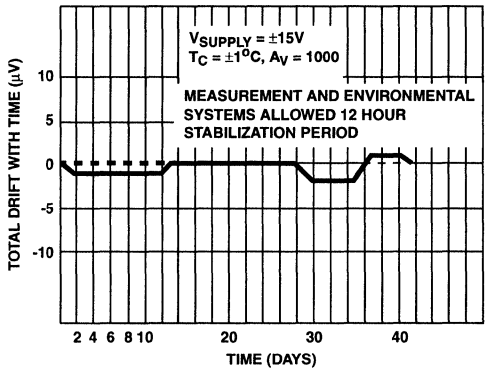


FIGURE 9. HA-5130 OFFSET VOLTAGE STABILITY vs TIME

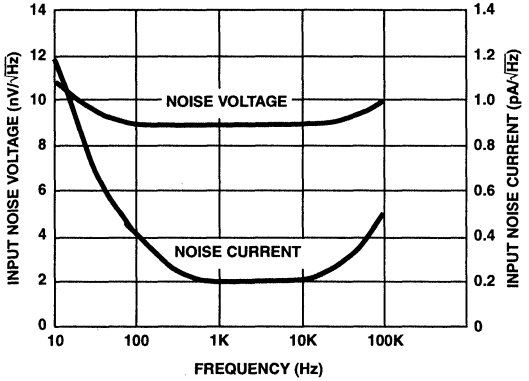


FIGURE 10. INPUT NOISE vs FREQUENCY

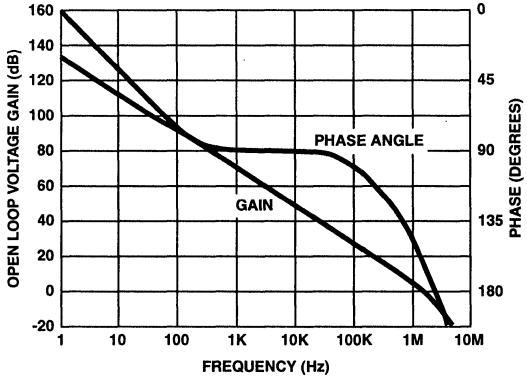


FIGURE 11. OPEN LOOP FREQUENCY RESPONSE

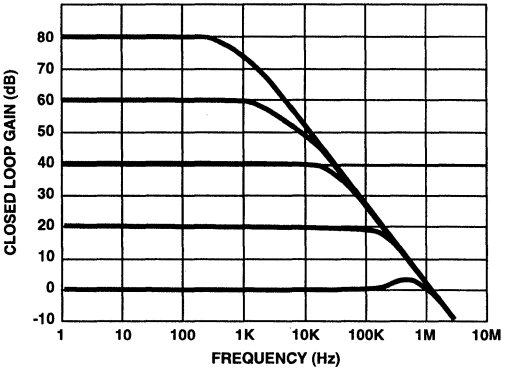


FIGURE 12. CLOSED LOOP FREQUENCY RESPONSE

Typical Performance Curves (Continued)

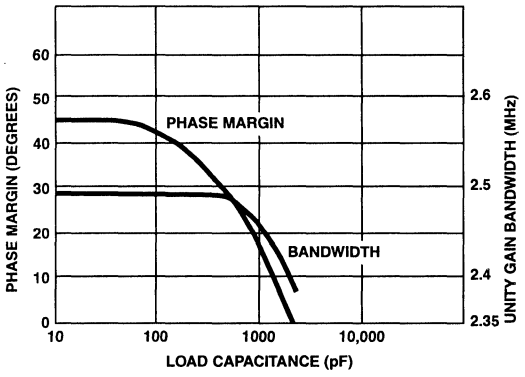


FIGURE 13. SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

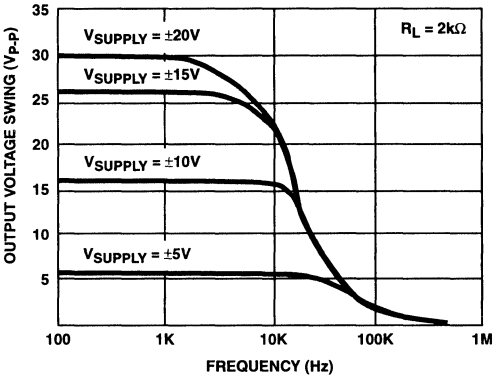


FIGURE 14. OUTPUT VOLTAGE SWING vs FREQUENCY

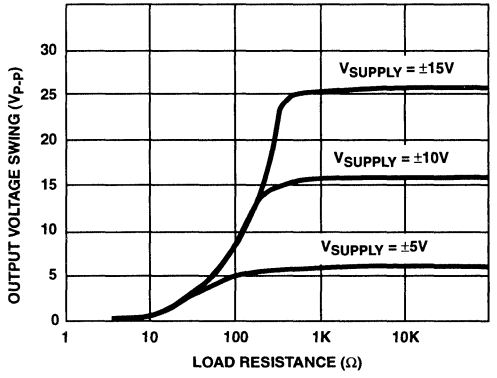


FIGURE 15. MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

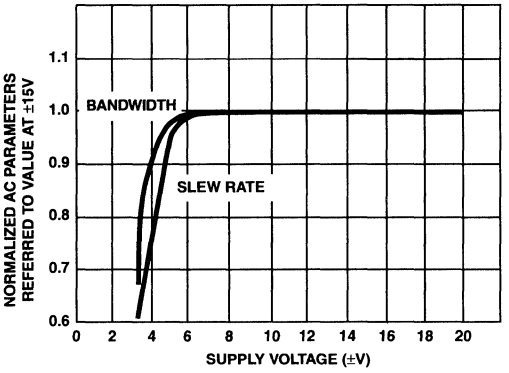


FIGURE 16. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

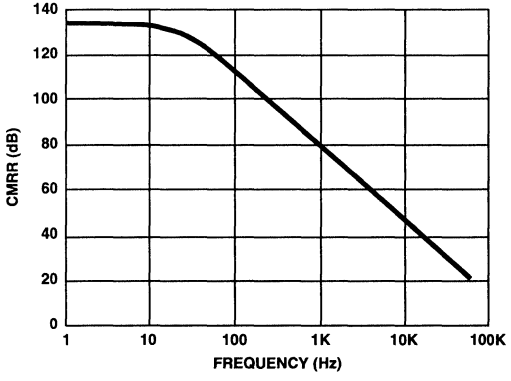


FIGURE 17. CMRR vs FREQUENCY

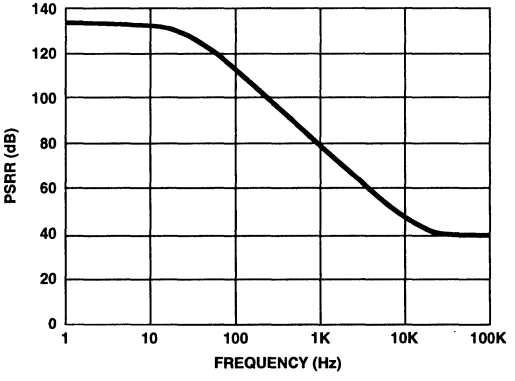


FIGURE 18. PSRR vs FREQUENCY

Typical Performance Curves (Continued)

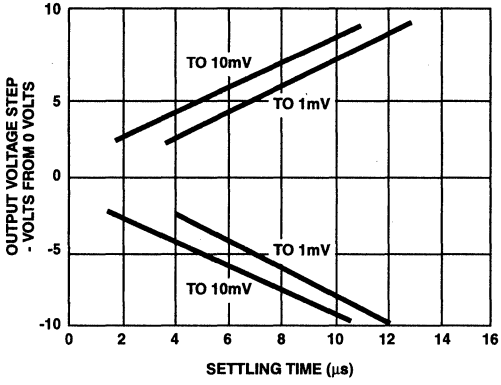


FIGURE 19. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

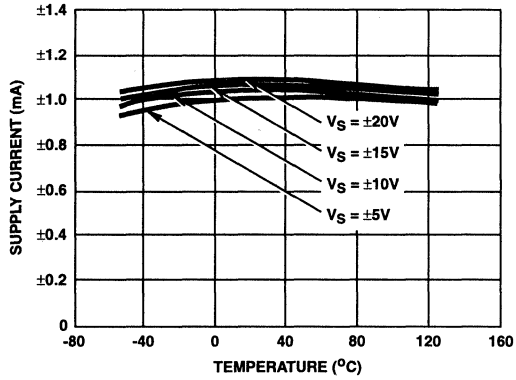


FIGURE 20. POWER SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

72 mils x 103 mils x 19 mils
(1840µm x 2620µm x 483µm)

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (S_iO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

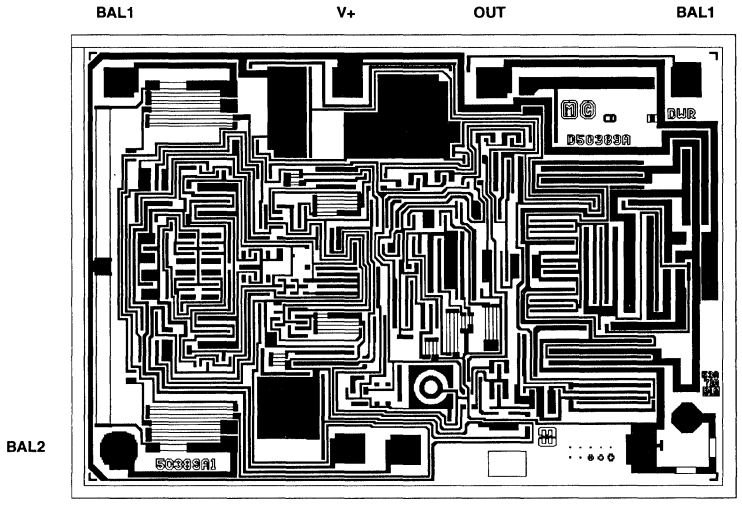
71

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5130, HA-5135



HARRIS SEMICONDUCTOR

HA-5134

November 1996

4MHz, Precision, Quad Operational Amplifier

Features

- Low Offset Voltage. . . . . .200µV (Max)
- Low Offset Voltage Drift . . . . . 2µV/°C (Max)
- High Channel Separation 120dB
- Low Noise. . . . . 7nV/√Hz
- Unity Gain Bandwidth 4MHz
- High CMRR/PSRR . . . . . 120dB (Typ)

Applications

- Instrumentation Amplifiers
- State-Variable Filters
- Precision Integrators
- Threshold Detectors
- Precision Data Acquisition Systems
- Low-Level Transducer Amplifiers

Description

The HA-5134 is a precision quad operational amplifier that is pin compatible with the OP-400, LT1014, OP11, RM4156, and LM148 as well as the HA-4741. Each amplifier features guaranteed maximum values for offset voltage of 200µV, offset voltage drift of 2µV/°C, and offset current of 75nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and A_{VOL} is guaranteed above 500kV/V from -55°C to 125°C.

Precision performance of the HA-5134 is enhanced by a noise voltage density of 7nV/√Hz at 1kHz, noise current density of 1pA/√Hz at 1kHz and channel separation of 120dB. Each unity-gain stable quad amplifier is fabricated using the dielectric isolation process to assure performance in the most demanding applications.

The HA-5134 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low-level transducer amplifiers. Other applications include precision data acquisition, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

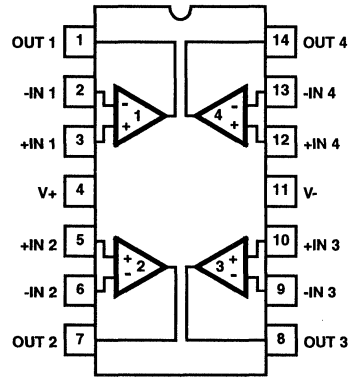
For military grade product, refer to the HA-5134/883 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-5134-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-5134-5	0 to 75	14 Ld CERDIP	F14.3

Pinout

HA-5134
(CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2926.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage (Note 2). 6V
Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-5134-2. . . . . -55°C to 125°C
HA-5134-5. . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	80	30

Maximum Junction Temperature (Note 3) . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. For differential input voltages greater than 6V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below 175°C.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 2k\Omega$, $C_L = 50pF$, $R_S \leq 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5134-2/-5 MIN	HA-5134-2/-5 TYP	HA-5134-2/-5 MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage		25	-	50	200	µV
		Full	-	75	350	µV
Average Offset Voltage Drift		Full	-	0.3	2	µV/°C
Bias Current		25	-	±10	±50	nA
		Full	-	±20	±75	nA
Offset Current		25	-	10	50	nA
		Full	-	15	75	nA
Average Offset Current Drift		Full	-	0.05	-	nA/°C
Common Mode Range		Full	±10	-	-	V
Differential Input Resistance		25	-	30	-	MΩ
Input Noise Voltage	0.1Hz to 10Hz	25	-	0.2	-	μV_{P-P}
Input Noise Voltage Density	f = 10Hz	25	-	10	-	$nV/\sqrt{Hz}$
	f = 100Hz		-	7.5	-	$nV/\sqrt{Hz}$
	f = 1kHz		-	7	-	$nV/\sqrt{Hz}$
Input Noise Current Density	f = 10Hz	25	-	3	-	$pA/\sqrt{Hz}$
	f = 100Hz		-	1.5	-	$pA/\sqrt{Hz}$
	f = 1kHz		-	1	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	$V_{OUT} = \pm10V$	25	800	1200	-	kV/V
		Full	500	750	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	25	100	120	-	dB
		Full	94	115	-	dB
Minimum Stable Gain		25	1	-	-	V/V
Unity-Gain Bandwidth		25	-	4	-	MHz
OUTPUT CHARACTERISTICS						
Output Voltage Swing		Full	12	13.5	-	V

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 2k\Omega$, $C_L = 50pF$, $R_S \leq 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5134-2/-5			UNITS
			MIN	TYP	MAX	
Output Current		25	-	20	-	mA
Full Power Bandwidth (Note 4)		25	12	16	-	kHz
Channel Separation	$V_{OUT} = \pm10V$	25	120	136	-	dB
TRANSIENT RESPONSE (Note 5)						
Rise Time	$A_V = +1$, $V_{OUT} = 200mV$	25	-	200	400	ns
Slew Rate	$A_V = +1$	25	0.75	1.0	-	V/µs
Overshoot	$A_V = +1$	25	-	20	40	%
Settling Time (Note 6)		25	-	13	-	µs
POWER SUPPLY CHARACTERISTICS						
Supply Current	All Amps	Full	-	6.5	8	mA
Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm18V$	25	100	120	-	dB
		Full	94	115	-	dB

NOTES:

4. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 10V$.
5. Refer to Test Circuits section of the data sheet.
6. Specified to 0.01% of a 10V step, $A_V = -1$.

Test Circuits and Waveforms

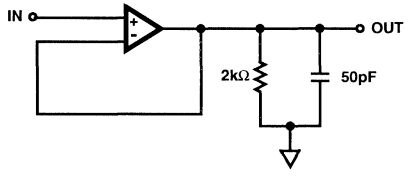
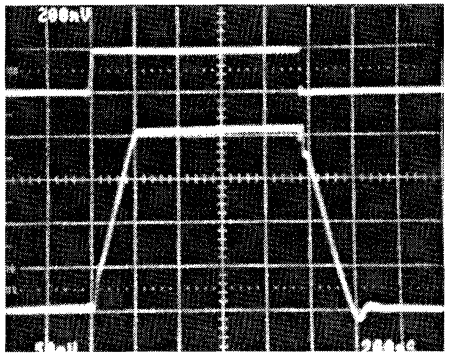
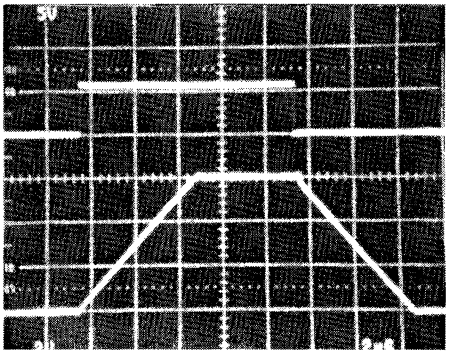


FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



Vertical: 50mV/Div., Horizontal: 200ns/Div.
$T_A = 25°C$, $V_S = \pm15V$, $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$

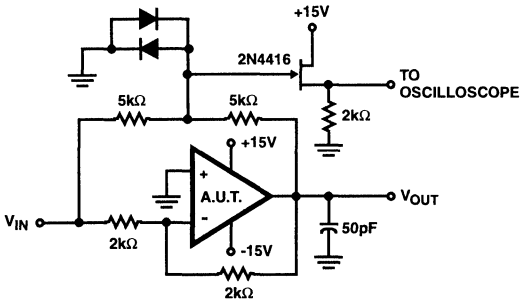
SMALL SIGNAL RESPONSE



Vertical: 2V/Div., Horizontal: 2µs/Div.
$T_A = 25°C$, $V_S = \pm15V$, $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$

LARGE SIGNAL RESPONSE

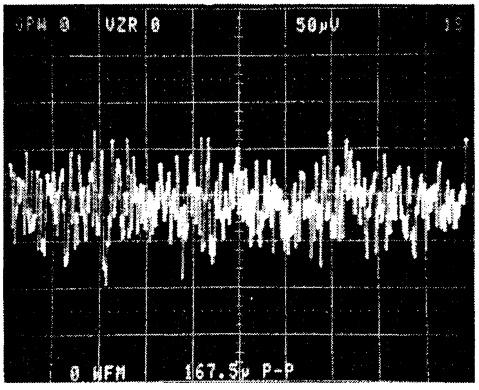
Test Circuits and Waveforms (Continued)



NOTES:

7. $A_V = -1$.
8. Feedback and summing resistors should be 0.1% matched.
9. Clipping diodes are optional. HP5082-2810 recommended.

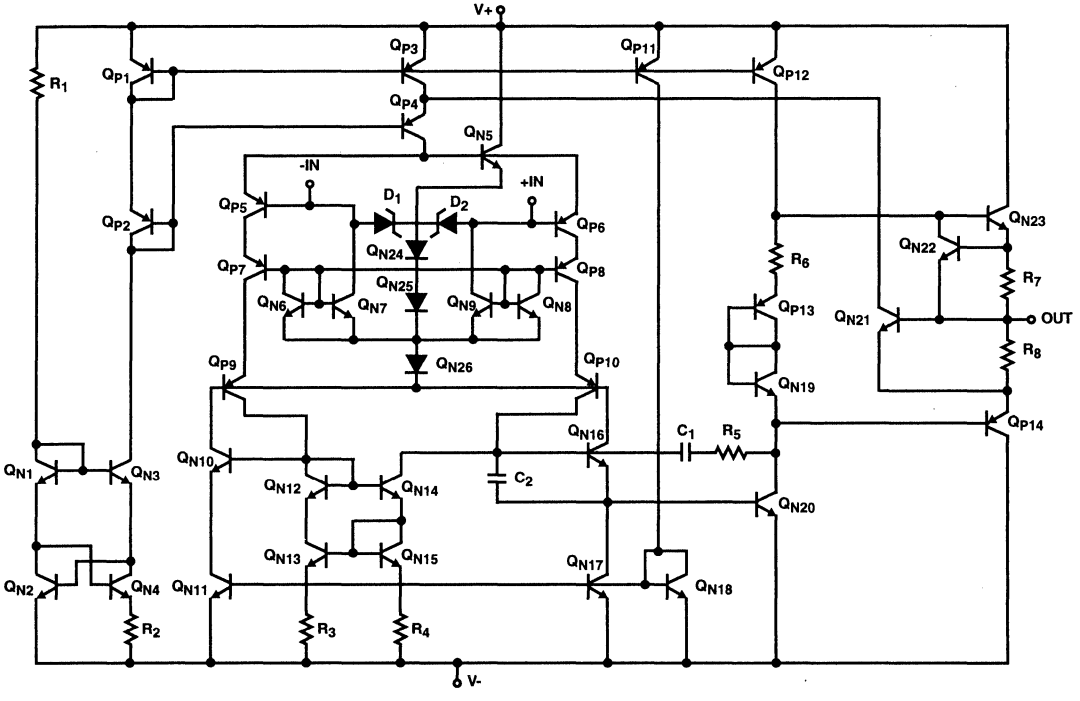
FIGURE 2. SETTLING TIME CIRCUIT



$T_A = 25^oC$, $V_S = \pm15V$, $A_V = 1000$
$e_n = 0.167\mu V_{P-P}$
0.05µV/Div., 1s/Div.

PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz

Schematic Diagram (Each Amplifier)



Application Information

Power Supply Decoupling

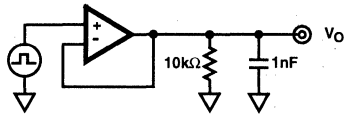
Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

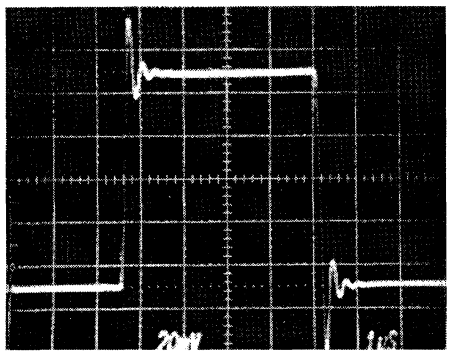
Considerations For Prototyping

The following list of recommendations are suggested for prototyping.

1. Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
2. Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
3. Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.

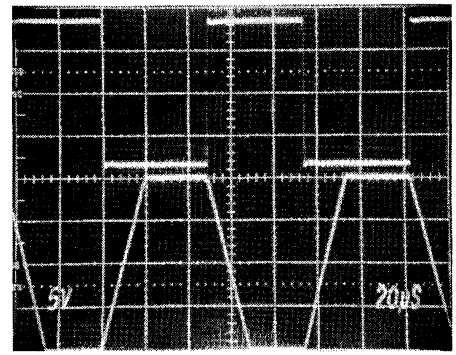
Typical Applications





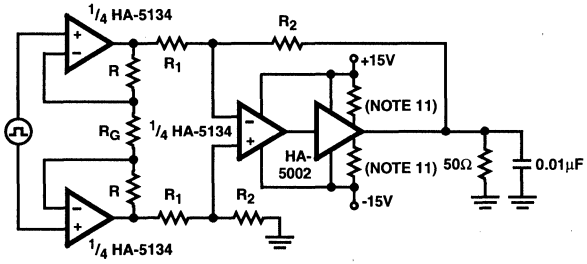
$T_A = 25^oC$, $V_S = \pm15V$, $A_V = 1$, $R_L = 10k\Omega$
20mV/Div., 1µs/Div.

FIGURE 3. SMALL SIGNAL TRANSIENT RESPONSE (C_{LOAD} = 1nF)



$V_{OUT} = \pm10V$, $R_{LOAD} = 50\Omega$ $C_{LOAD} = 0.01\mu F$, $A_V = 3$, $V_S = \pm15V$
Top: Input, 2V/Div., 20µs/Div. Bottom: Output, 5V/Div, 20µs/Div.

TRANSIENT RESPONSE OF APPLICATION CIRCUIT #1

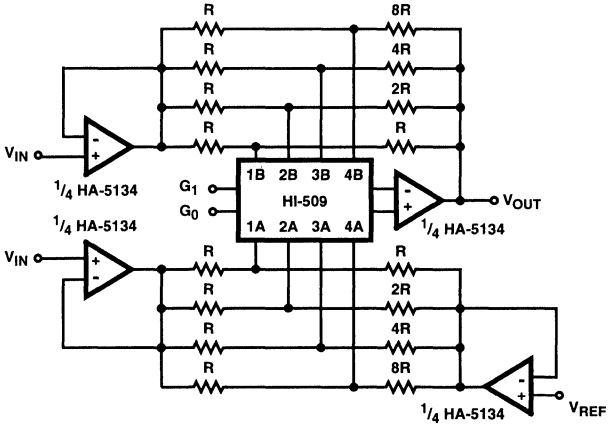


NOTES:

10. $-A_V = \left(1 + \frac{2R}{R_G}\right)\left(\frac{R_2}{R_1}\right)$.
11. 10Ω - 100Ω recommended for short circuit limiting.
12. When driving heavy loads the HA-5002 may contribute to thermal errors. Proper thermal shielding is recommended.

FIGURE 4. APPLICATION CIRCUIT #1: INSTRUMENTATION AMPLIFIER WITH POWER OUTPUT

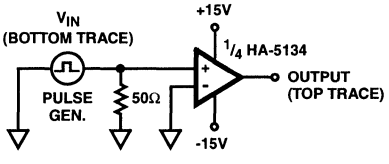
Typical Applications (Continued)

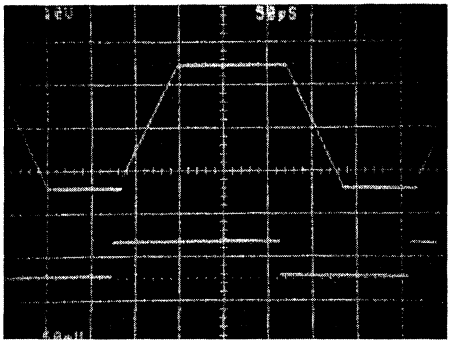


G_1	G_0	A_V
0	0	-1
0	1	-2
1	0	-4
1	1	-8

High A_{VOL} of HA-5134 reduces gain error.
Gain Error ≅ 0.004% at A_V = 8.

FIGURE 5. APPLICATION CIRCUIT #2: PROGRAMMABLE GAIN AMPLIFIER





NOTE: If differential input voltages greater than 6V are present, input current must be limited to less than 25mA.

Horizontal: 50µs/Div.
V_{IN} = ±25mV, V_{OUT} = ±14V

FIGURE 6. APPLICATION CIRCUIT #3: PRECISION COMPARATOR

Typical Performance Curves

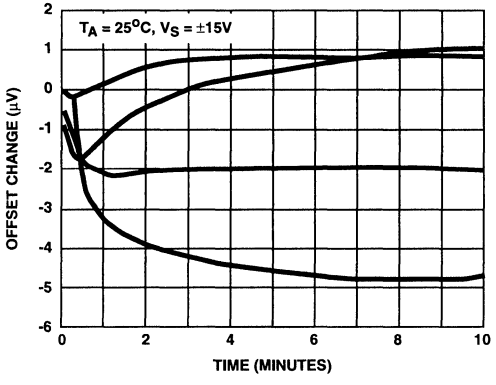


FIGURE 7. V_{IO} WARM-UP DRIFT

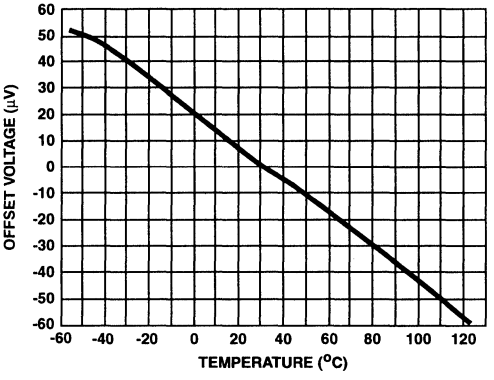


FIGURE 8. INPUT OFFSET VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

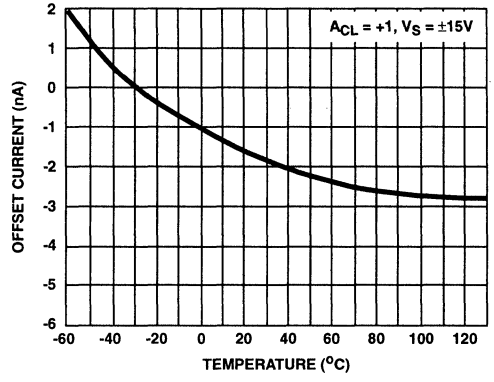


FIGURE 9. OFFSET CURRENT vs TEMPERATURE

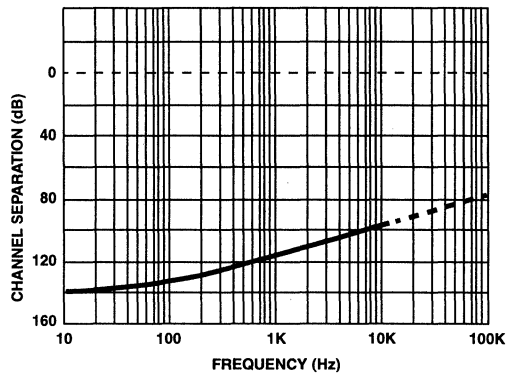


FIGURE 10. CHANNEL SEPARATION vs FREQUENCY

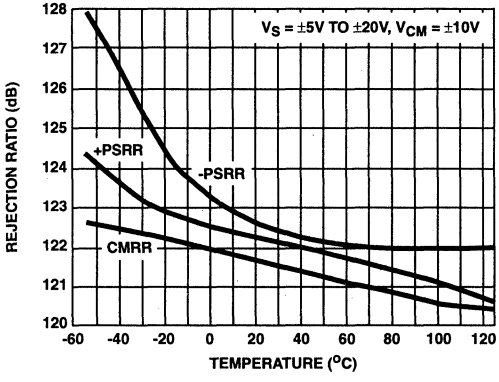


FIGURE 11. REJECTION RATIOS vs TEMPERATURE

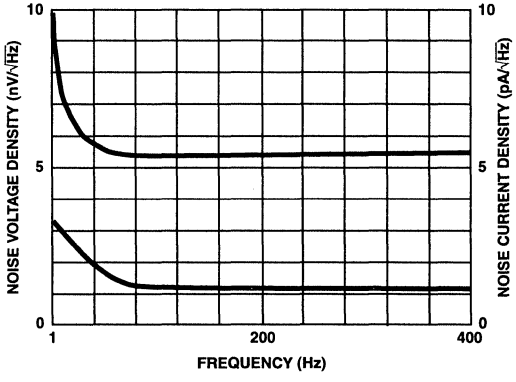


FIGURE 12. NOISE DENSITY vs FREQUENCY

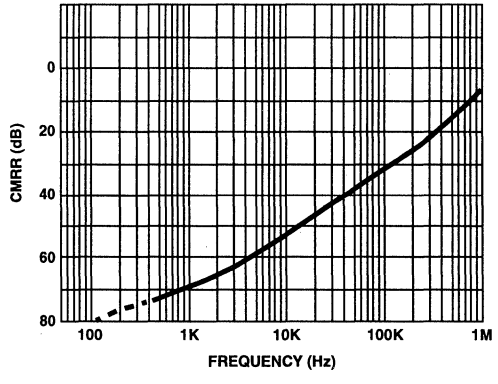


FIGURE 13. CMRR vs FREQUENCY

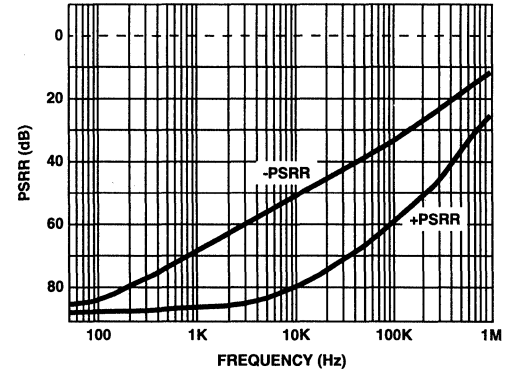


FIGURE 14. PSRR vs FREQUENCY

Typical Performance Curves (Continued)

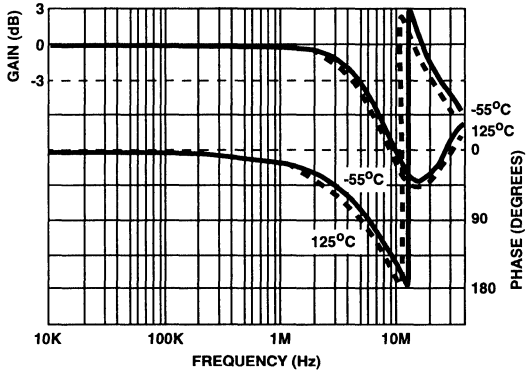


FIGURE 15. CLOSED LOOP FREQUENCY RESPONSE

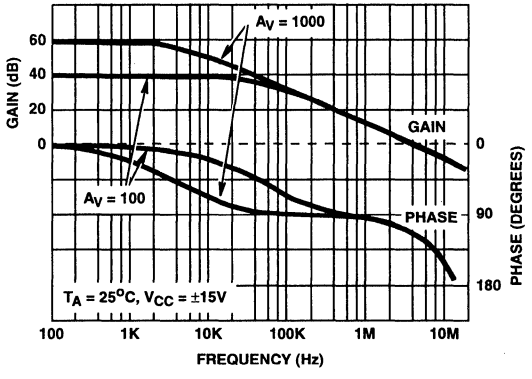


FIGURE 16. CLOSED LOOP GAIN/PHASE vs FREQUENCY

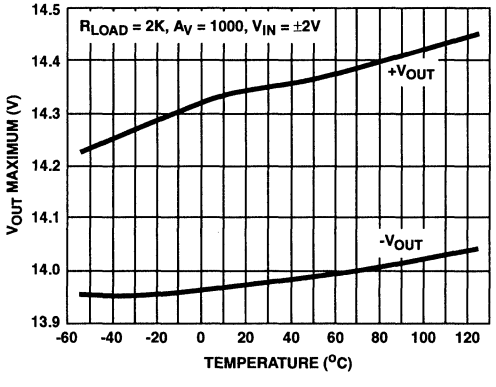


FIGURE 17. MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

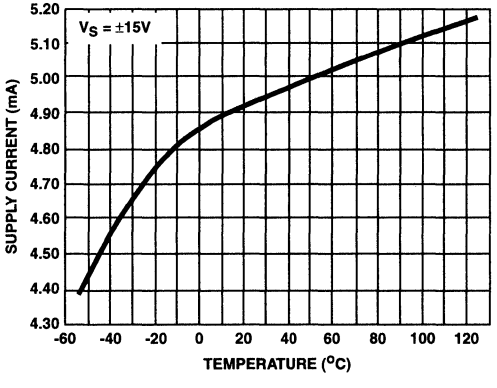


FIGURE 18. SUPPLY CURRENT vs TEMPERATURE

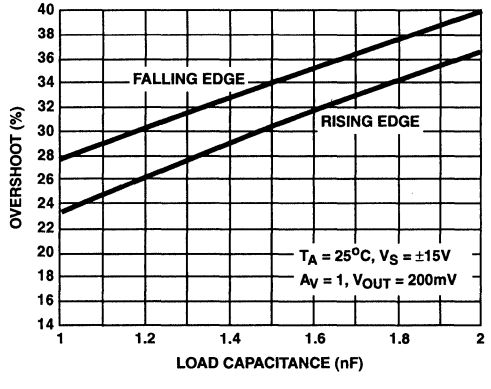


FIGURE 19. OVERSHOOT vs C_{LOAD}

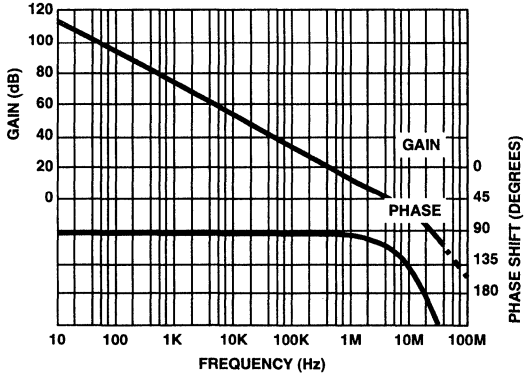


FIGURE 20. OPEN LOOP GAIN AND PHASE vs FREQUENCY

HA-5137, HA-5137A

63MHz, Ultra-Low Noise Precision Operational Amplifier

November 1996

Features

- Slew Rate 20V/μs
- Wide Gain Bandwidth ($A_V \geq 5$) 63MHz
- Low Noise ..... 3nV/$\sqrt{Hz}$ at 1kHz
- Low V_{OS} 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers
- For Further Design Ideas See Application Note 553

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3-5137A-5	0 to 75	8 Ld PDIP	E8.3
HA7-5137-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5137-5	0 to 75	8 Ld CERDIP	F8.3A
HA7-5137A-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5137A-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P5137-5 (H51375)	0 to 75	8 Ld SOIC	M8.15

Description

The HA-5137 operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris Dielectric Isolation technology and advanced processing techniques, this unique design unites low noise (3nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (20V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10μV), wide gain bandwidth (63MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

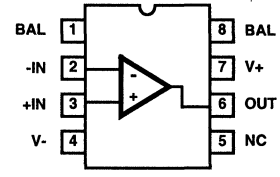
Using the HA-5137 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than five.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5137's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than five. For the military grade product, refer to the HA-5137/883 data sheet.

Pinout

HA-5137, HA-5137A
(PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2908.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 1). 0.7V
Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-5137/37A-2 . . . . . $-55^{o}C$ to $125^{o}C$
HA-5137/37A-5 . . . . . $0^{o}C$ to $75^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
CERDIP Package	135	50
PDIP Package	120	N/A
SOIC Package	160	N/A

Maximum Junction Temperature (Hermetic Package) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Packages) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

Die Characteristics

Back Side Potential . . . . . V-
Number of Transistors 63

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L \leq 50pF$, $R_S \leq 100\Omega$

PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	HA-5137			HA-5137A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	30	100	-	10	25	µV
		Full	-	70	300	-	30	60	µV
Average Offset Voltage Drift		Full	-	0.4	1.8	-	0.2	0.6	µV/°C
Bias Current		25	-	15	80	-	10	40	nA
		Full	-	35	150	-	20	60	nA
Offset Current		25	-	12	75	-	7	35	nA
		Full	-	30	135	-	15	50	nA
Common Mode Range		Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 3)		25	0.8	4	-	1.5	6	-	MΩ
Input Noise Voltage (Note 4)	0.1Hz to 10Hz	25	-	0.09	0.25	-	0.08	0.18	μV_{P-P}
Input Noise Voltage Density (Note 5)	f = 10Hz	25	-	3.8	8.0	-	3.5	8.0	$nV/\sqrt{Hz}$
	f = 100Hz	25	-	3.3	4.5	-	3.1	4.5	$nV/\sqrt{Hz}$
	f = 1000Hz	25	-	3.2	3.8	-	3.0	3.8	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 5)	f = 10Hz	25	-	1.7	-	-	1.7	4.0	$pA/\sqrt{Hz}$
	f = 100Hz	25	-	1.0	-	-	1.0	2.3	$pA/\sqrt{Hz}$
	f = 1000Hz	25	-	0.4	0.6	-	0.4	0.6	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_{OUT} = \pm10V$	25	700	1500	-	1000	1800	-	V/mV
		Full	300	800	-	600	1200	-	V/mV
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	Full	100	120	-	114	126	-	dB
Minimum Stable Gain		25	5	-	-	5	-	-	V/V

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L \leq 50pF$, $R_S \leq 100\Omega$ **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5137			HA-5137A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Gain-Bandwidth-Product	f = 10kHz	25	60	80	-	60	80	-	MHz
	f = 1MHz	25	-	63	-	-	63	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 600\Omega$	25	±10.0	±11.5	-	±10.0	±11.5	-	V
	$R_L = 2k\Omega$	Full	±11.4	±13.5	-	±11.7	±13.8	-	V
Full Power Bandwidth (Note 6)		25	220	320	-	220	320	-	kHz
Output Resistance	Open Loop	25	-	70	-	-	70	-	Ω
Output Current		25	16.5	25	-	16.5	25	-	mA
TRANSIENT RESPONSE (Note 7)									
Rise Time		25	-	-	100	-	-	100	ns
Slew Rate	$V_{OUT} = \pm3V$	25	14	20	-	14	20	-	V/µs
Settling Time	Note 8	25	-	1.0	-	-	1.0	-	µs
Overshoot		25	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	3.5	-	-	3.5	-	mA
		Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	Full	-	16	51	-	2	4	µV/V

NOTES:

3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. The limits for this parameter are based on lab characterization, and reflect lot-to-lot variation.
6. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
7. Refer to Test Circuits section of the data sheet.
8. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -5$.

Test Circuits and Waveforms

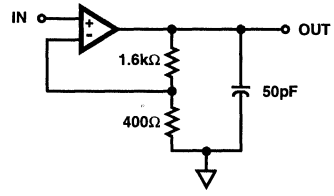
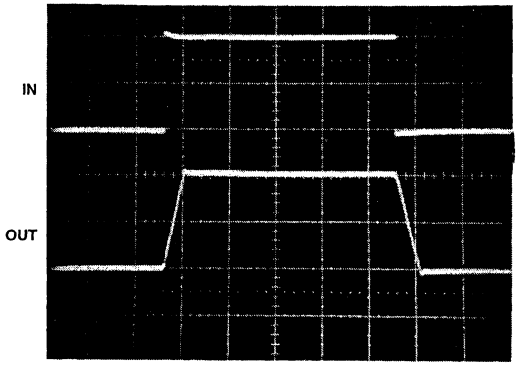


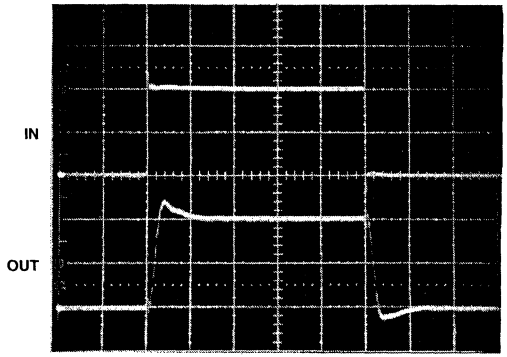
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

Test Circuits and Waveforms (Continued)



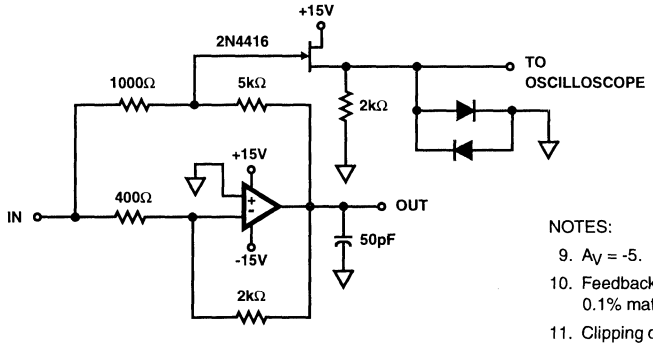
Vertical Scale: Input = 1V/Div.
Output = 5V/Div.
Horizontal Scale: 1µs/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: Input = 20mV/Div.
Output = 100mV/Div.
Horizontal Scale: 100ns/Div.

SMALL SIGNAL RESPONSE

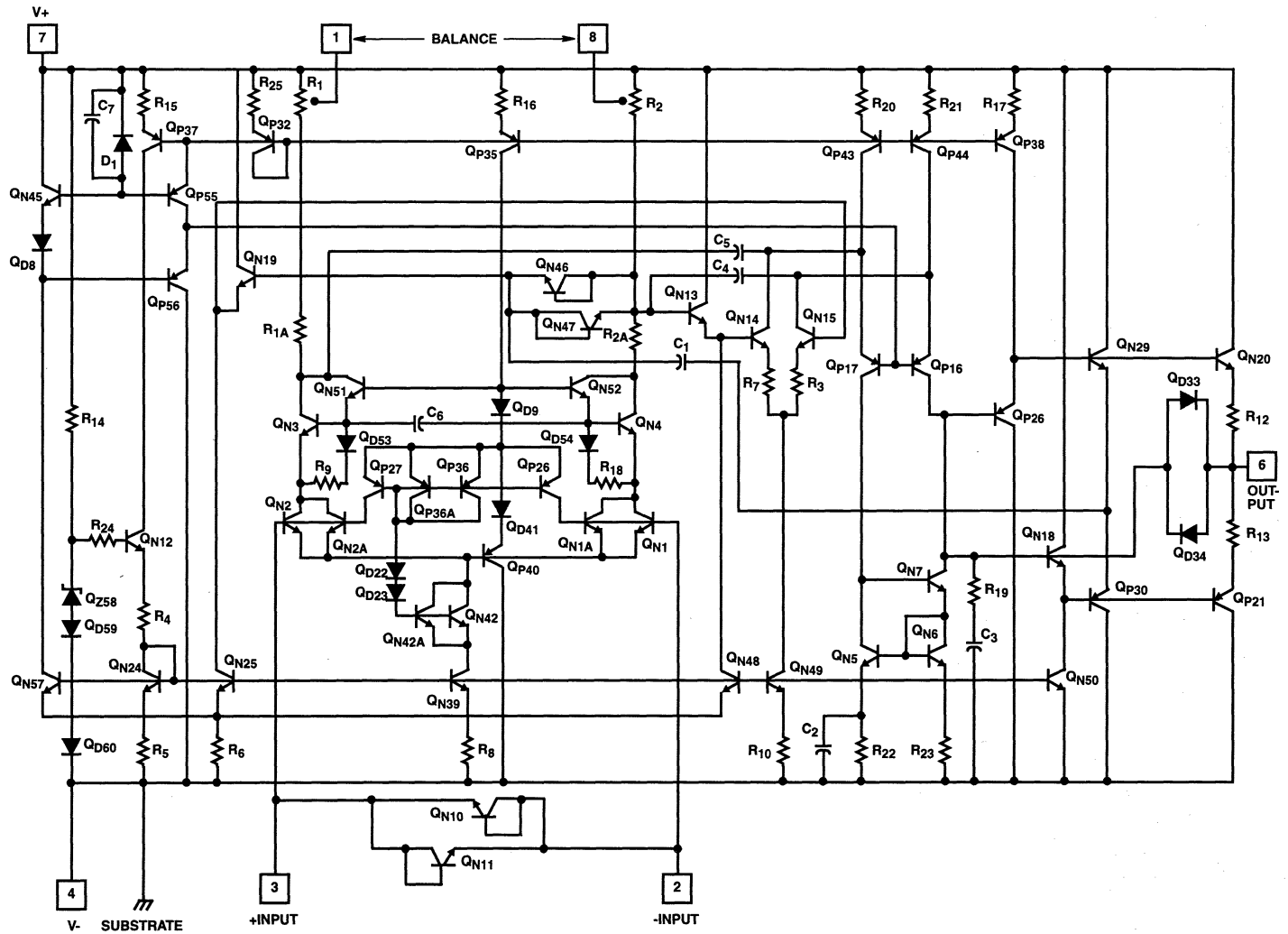


NOTES:

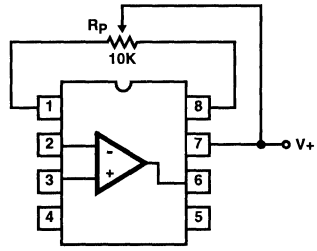
9. A_V = -5.
10. Feedback and summing resistors should be 0.1% matched.
11. Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram

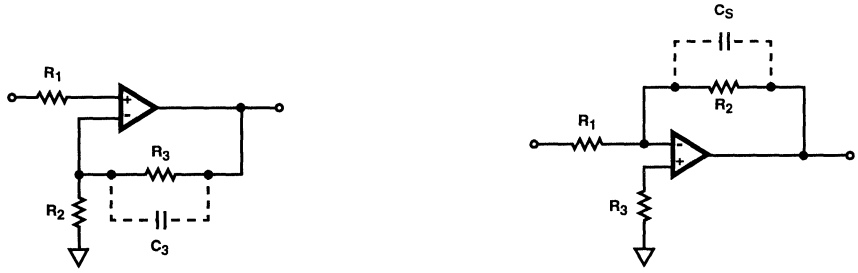


Application Information



NOTE: Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±4mV with R_P = 10kΩ.

FIGURE 3. SUGGESTED OFFSET VOLTAGE ADJUSTMENT



NOTE: Low resistances are preferred for low noise applications as a 1kΩ resistor has 4nV/√Hz of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 4. SUGGESTED STABILITY CIRCUITS

Typical Performance Curves Unless Otherwise Specified: T_A = 25°C, V_{SUPPLY} = ±15V

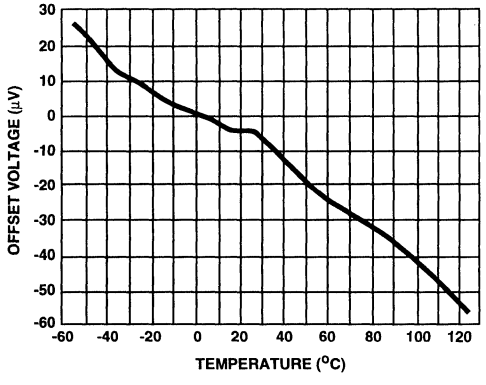


FIGURE 5. TYPICAL OFFSET VOLTAGE DRIFT vs TEMPERATURE

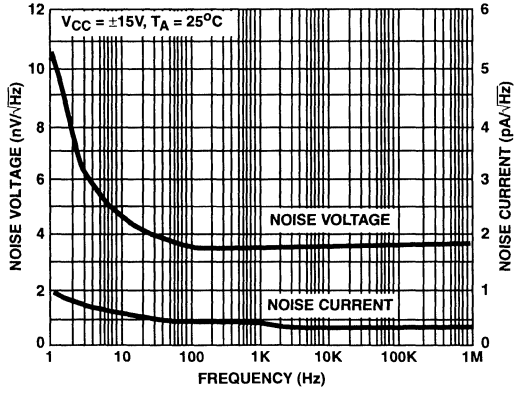


FIGURE 6. NOISE CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$ (Continued)

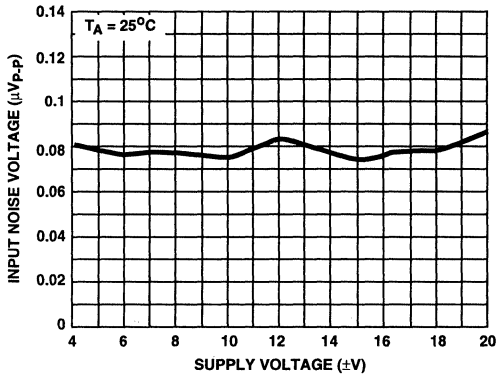


FIGURE 7. NOISE vs SUPPLY VOLTAGE

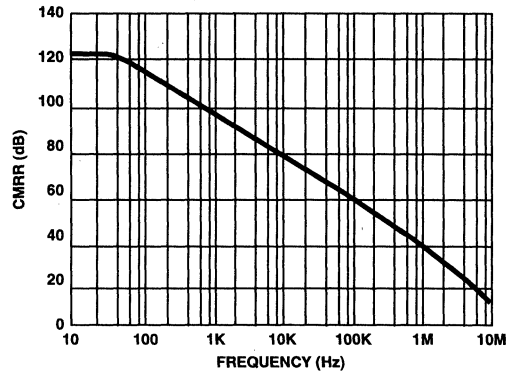


FIGURE 8. CMRR vs FREQUENCY

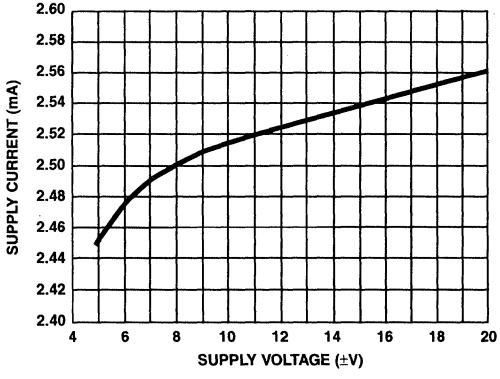


FIGURE 9. SUPPLY CURRENT vs SUPPLY VOLTAGE

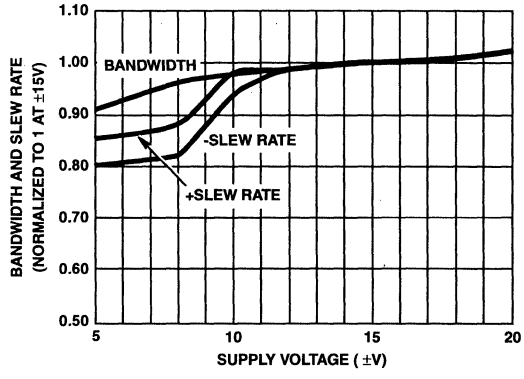


FIGURE 10. BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE

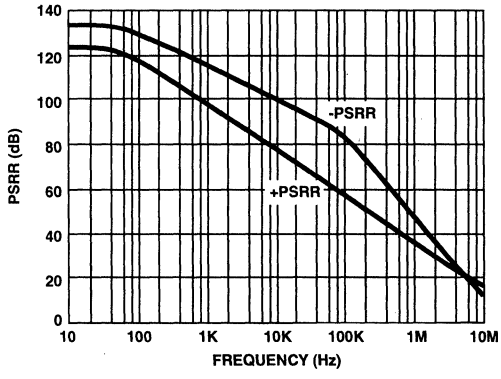


FIGURE 11. PSRR vs FREQUENCY

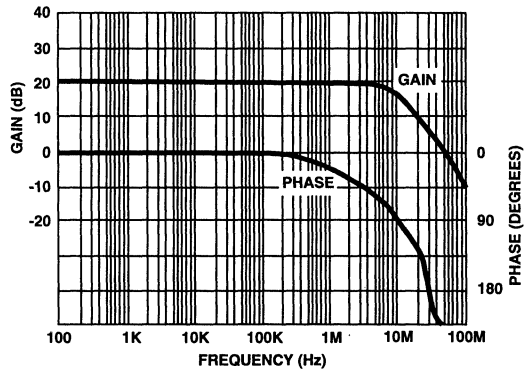


FIGURE 12. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$ (Continued)

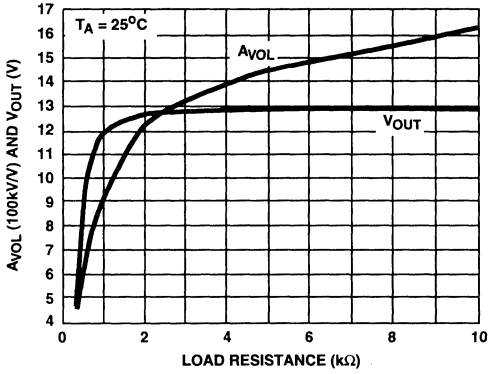


FIGURE 13. A_{VOL} AND V_{OUT} vs LOAD RESISTANCE

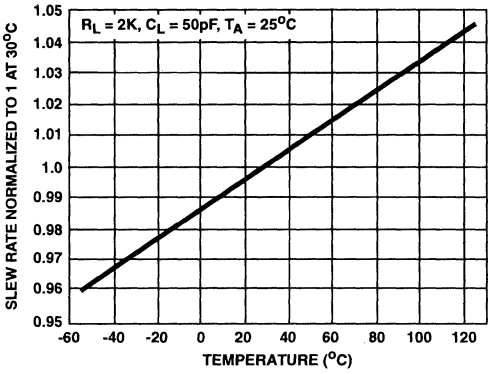


FIGURE 14. NORMALIZED SLEW RATE vs TEMPERATURE

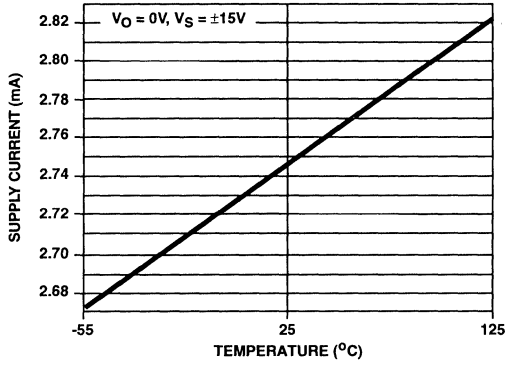


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

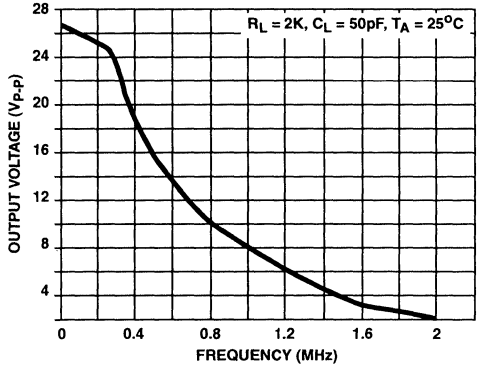


FIGURE 16. V_{OUT} MAX (UNDISTORTED SINEWAVE OUTPUT) vs FREQUENCY

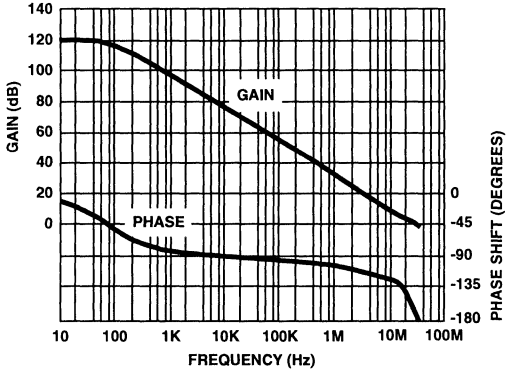
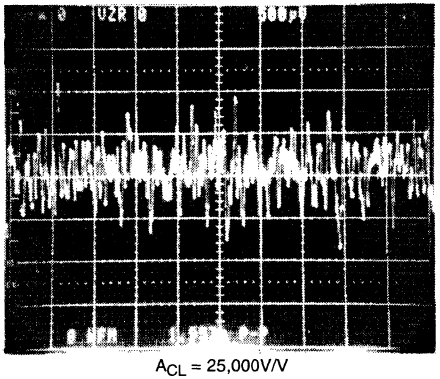


FIGURE 17. OPEN LOOP GAIN AND PHASE vs FREQUENCY



A_{CL} = 25,000V/V
Horizontal Scale = 1s/Div.
Vertical Scale = 0.002μV/Div., E_N = 0.08μV_{P-P} RTI

FIGURE 18. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)

3 OPERATIONAL AMPLIFIERS

HA-5142, HA-5144

Dual/Quad, 400kHz, Ultra-Low Power Operational Amplifiers

November 1996

Features

- Low Supply Current 45μA/Amp
- Wide Supply Voltage Range Single . . . . . 3V to 30V
  or Dual . . . . . ±1.5V to ±15V
- High Slew Rate 1.5V/μs
- High Gain 100kV/V
- Unity Gain Stable
- Available in Duals and Quads

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation
- For Further Design Ideas See Application Note 544

Description

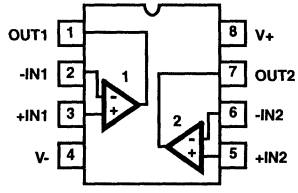
The HA-5142/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. In applications which require low power dissipation and good AC electrical characteristics, this family offers the industry's best speed/power ratio.

The HA-5142/44 provides accurate signal processing by virtue of their low input offset voltage (2mV), low input bias current (45nA), high open loop gain (100kV/V) and low noise (20nV/$\sqrt{Hz}$), for low power operational amplifiers. These characteristics coupled with a 1.5V/μs slew rate and a 400kHz bandwidth make the HA-5142/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment. These parts are also tested and guaranteed at both ±15V and single ended +5V supplies.

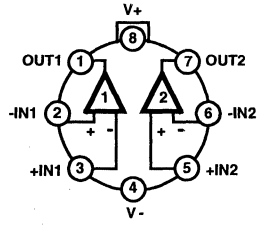
These amplifiers are available with industry standard pinouts which allow the HA-5142/5144s to be interchangeable with most other operational amplifiers. For military grade product refer to the 5142, 5144/883 data sheet.

Pinouts (See Ordering Information on Next Page)

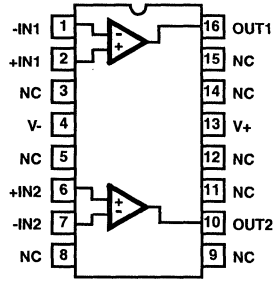
HA-5142 (PDIP, CERDIP)
TOP VIEW



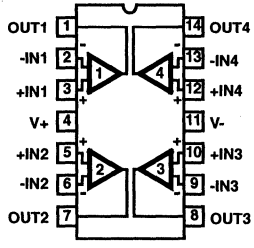
HA-5142 (METAL CAN)
TOP VIEW



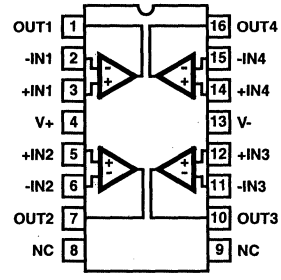
HA-5142 (SOIC)
TOP VIEW



HA-5144 (PDIP, CERDIP)
TOP VIEW



HA-5144 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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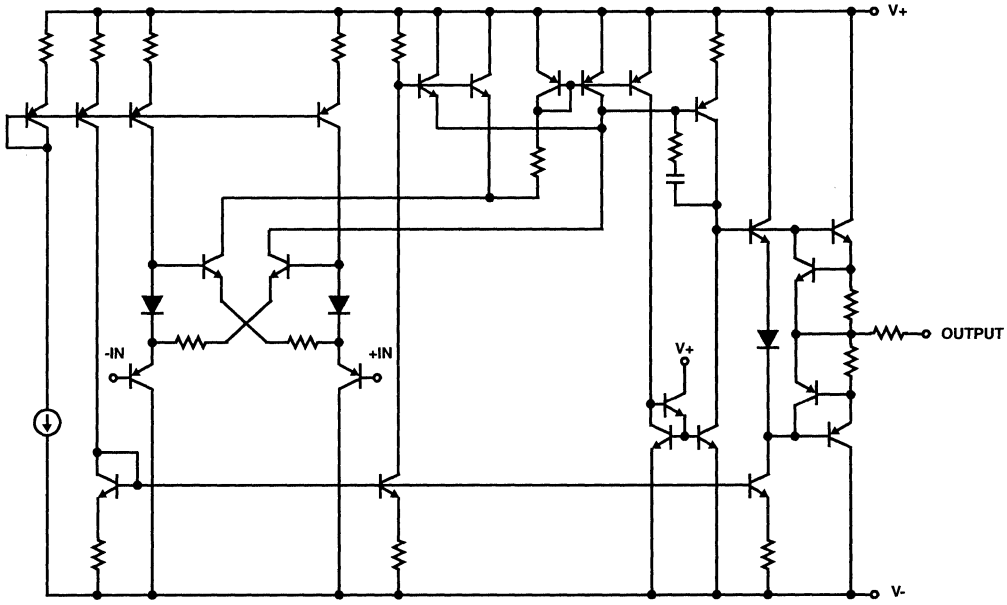
File Number **2909.2**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-5142-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-5142-5	0 to 75	8 Pin Metal Can	T8.C
HA3-5142-5	0 to 75	8 Ld PDIP	E8.3
HA7-5142-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5142-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P5142-9	-40 to 85	16 Ld SOIC	M16.3
HA1-5144-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-5144-5	0 to 75	14 Ld CERDIP	F14.3
HA3-5144-5	0 to 75	14 Ld PDIP	E14.3
HA9P5144-5	0 to 75	16 Ld SOIC	M16.3
HA9P5144-9	-40 to 85	16 Ld SOIC	M16.3

Schematic Diagram



Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 35V
Differential Input Voltage. 7V
Output Current . . . . . Short Circuit Protected

Operating Conditions

Temperature Range
HA-5142/44-5 . . . . . 0°C to 75°C
HA-5142/44-2 . . . . . -55°C to 125°C
HA-5142/44-9 . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Lead CERDIP Package	75	20
8 Pin Metal Can Package	155	67
14 Lead PDIP Package	100	N/A
8 Lead PDIP Package	120	N/A
8 Lead CERDIP Package	135	50
16 Lead SOIC Package (HA-5142)	110	N/A
16 Lead SOIC Package (HA-5144)	100	N/A

Maximum Junction Temperature (Hermetic Packages) . . . . . 175°C
Maximum Junction Temperature (Plastic Packages) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$R_S = 100\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	-2, -5, -9 V+ = +5V, V- = 0V			-2, -5, -9 V+ = +15V, V- = -15V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage	Note 11	25	-	2	6	-	2	6	mV
		Full	-	-	8	-	-	8	mV
Average Offset Voltage Drift		Full	-	3	-	-	3	-	µV/°C
Bias Current	Note 11	25	-	45	100	-	45	100	nA
		Full	-	-	125	-	-	125	nA
Offset Current	Note 11	25	-	0.3	10	-	0.3	10	nA
		Full	-	-	20	-	-	20	nA
Common Mode Range		Full	0 to 3	-	-	±10	-	-	V
Differential Input Resistance		25	-	0.6	-	-	0.6	-	MΩ
Input Noise Voltage	f = 1kHz	25	-	20	-	-	20	-	nV/√Hz
Input Noise Current	f = 1kHz	25	-	0.25	-	-	0.25	-	pA/√Hz
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	Notes 2, 4	25	20	100	-	20	100	-	kV/V
		Full -2, -5	15	-	-	15	-	-	kV/V
		Full -9	12	-	-	12	-	-	kV/V
Common Mode Rejection Ratio	Note 7	Full -2, -5	77	105	-	77	105	-	dB
		Full -9	70	105	-	70	105	-	dB

Electrical Specifications $R_S = 100\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	-2, -5, -9 V+ = +5V, V- = 0V			-2, -5, -9 V+ = +15V, V- = -15V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Bandwidth	Notes 2, 3	25	-	0.4	-	-	0.4	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	Notes 2, 10	25	1.0 to 3.8	0.7 to 4.2	-	±10	±13	-	V
		Full	1.2 to 3.5	0.9 to 4.0	-	±10	±13	-	V
Full Power Bandwidth	Notes 2, 4, 8	25	-	240	-	-	24	-	kHz
TRANSIENT RESPONSE (Notes 2, 3)									
Rise Time		25	-	600	-	-	600	-	ns
Slew Rate	Note 6	25	0.8	1.5	-	0.8	1.5	-	V/µs
Settling Time	Note 5	25	-	10	-	-	10	-	µs
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	45	80	-	100	150	µA/Amp
		Full	-	-	100	-	-	200	µA/Amp
Power Supply Rejection Ratio	Note 9	Full -2, -5	77	105	-	77	105	-	dB
		Full -9	70	105	-	70	105	-	dB

NOTES:

2. $R_L = 50k\Omega$.
3. $C_L = 50pF$.
4. $V_O = 1.4$ to 2.5V for $V_{SUPPLY} = +5, 0V$; $V_O = \pm 10V$ for $V_{SUPPLY} = \pm 15V$.
5. Settling Time is specified to 0.1% of final value for a 3V output step and $A_V = -1$ for $V_{SUPPLY} = +5V, 0V$. Output step = 10V for $V_{SUPPLY} = \pm 15V$.
6. Maximum input slew rate = 10V/µs.
7. $V_{CM} = 0$ to 3V for $V_{SUPPLY} = +5, 0V$; $V_{CM} = \pm 10V$ for $V_{SUPPLY} = \pm 15V$.
8. Full Power Bandwidth is guaranteed by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
9. $\Delta V_S = +10V$ for $V_{SUPPLY} = +5, 0V$; $\Delta V_S = \pm 5V$ for $V_{SUPPLY} = \pm 15V$.
10. For $V_{SUPPLY} = +5, 0V$ terminate R_L at +2.5V. Typical output current is ±3mA.
11. $V_O = 1.4V$ for $V_{SUPPLY} = +5V, 0V$.

Test Circuits and Waveforms

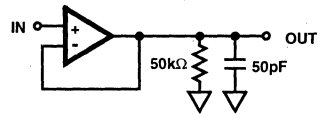
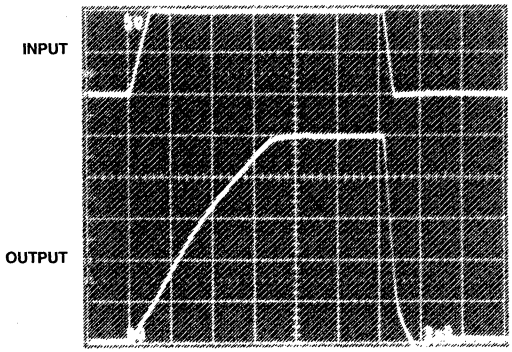
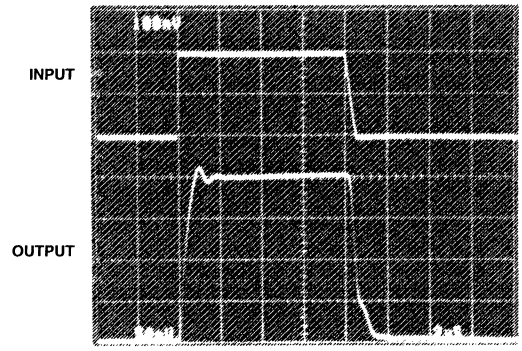


FIGURE 1. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



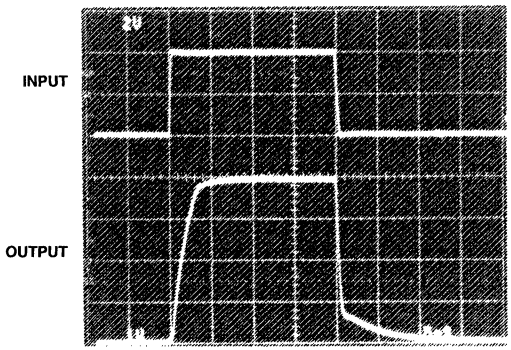
Vertical Scale: Input = 5V/Div.; Output = 2V/Div.
Horizontal Scale: 2µs/Div.

LARGE SIGNAL RESPONSE



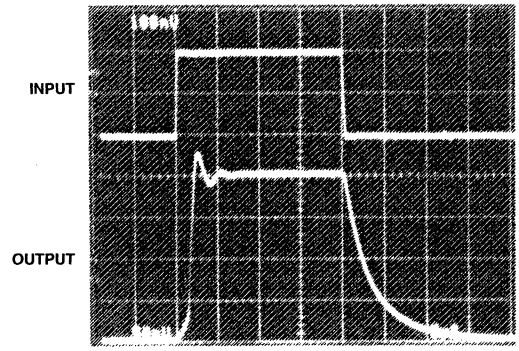
Vertical Scale: Input = 100mV/Div.; Output = 50mV/Div.
Horizontal Scale: 2µs/Div.

SMALL SIGNAL RESPONSE



Vertical Scale: Input = 2V/Div.; Output = 1V/Div.
Horizontal Scale: 5µs/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: Input = 100mV/Div.; Output = 50mV/Div.
Horizontal Scale: 5µs/Div.

SMALL SIGNAL RESPONSE

Typical Performance Curves $V_S = \pm 2.5V$, $T_A = 25^oC$, Unless Otherwise Specified

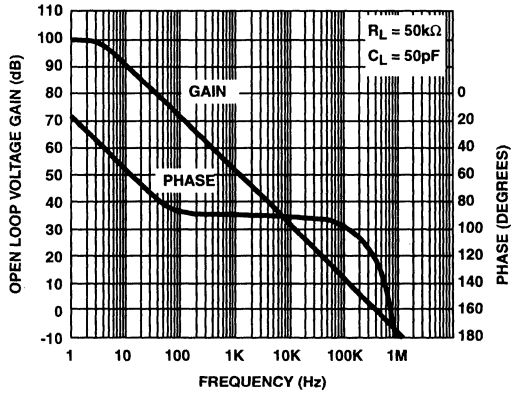


FIGURE 2. OPEN LOOP FREQUENCY RESPONSE

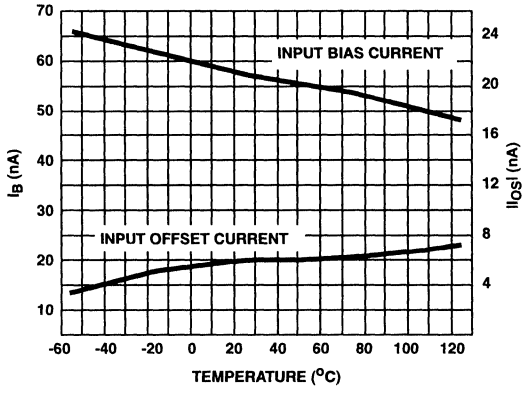


FIGURE 3. INPUT OFFSET CURRENT AND BIAS CURRENT vs TEMPERATURE

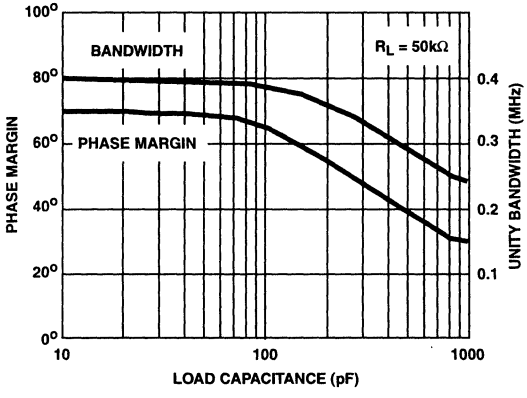


FIGURE 4. BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

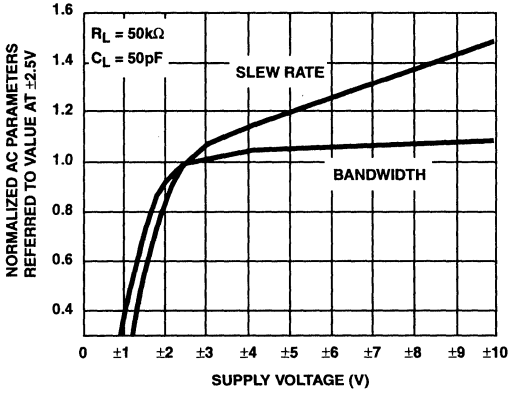


FIGURE 5. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

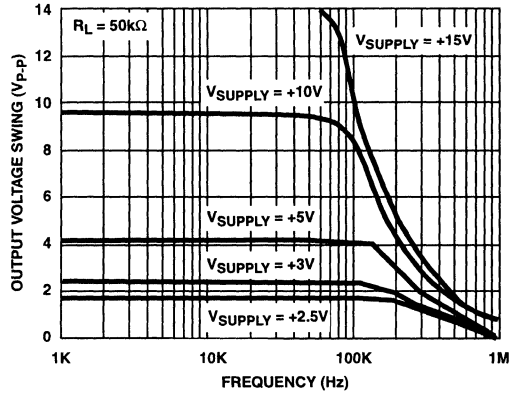


FIGURE 6. OUTPUT VOLTAGE SWING vs FREQUENCY AND SINGLE SUPPLY VOLTAGE

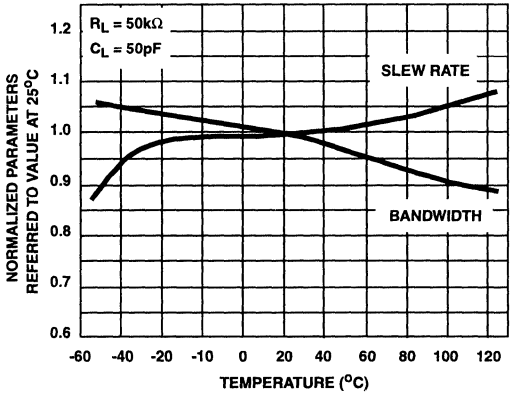


FIGURE 7. NORMALIZED AC PARAMETERS vs TEMPERATURE

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_S = \pm 2.5V$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

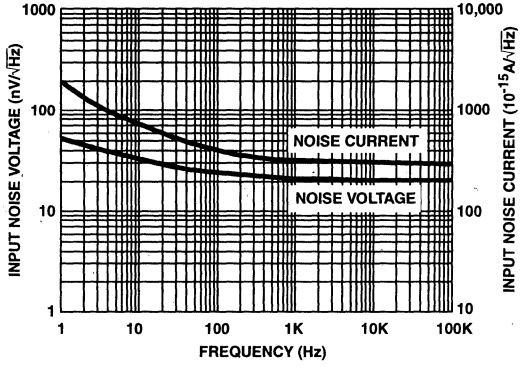


FIGURE 8. INPUT NOISE vs FREQUENCY

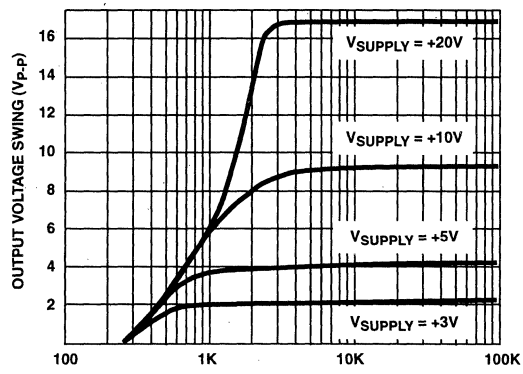


FIGURE 9. MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE

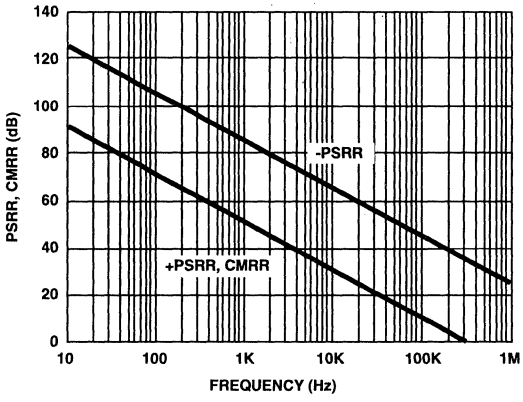


FIGURE 10. PSRR AND CMRR vs FREQUENCY

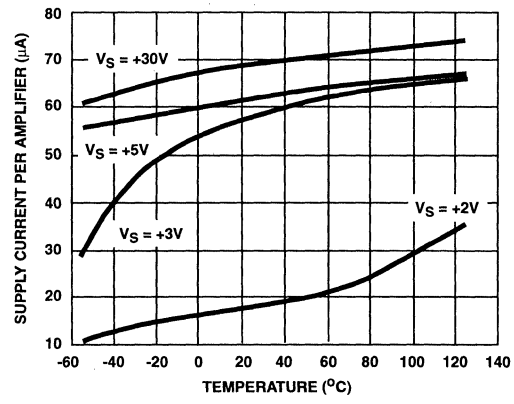


FIGURE 11. POWER SUPPLY CURRENT vs TEMPERATURE AND SINGLE SUPPLY VOLTAGE

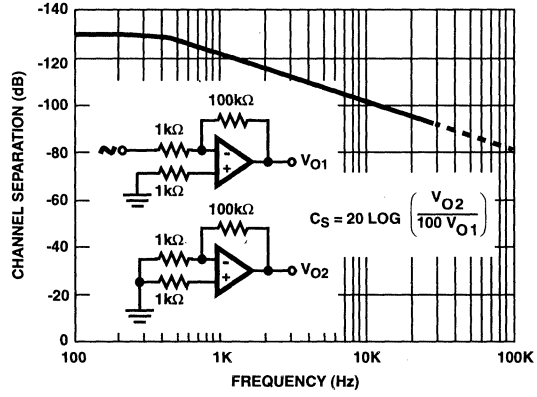


FIGURE 12. CHANNEL SEPARATION vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

104 mils x 55 mils x 19 mils
2650µm x 1400µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

72

SUBSTRATE POTENTIAL (Powered Up):

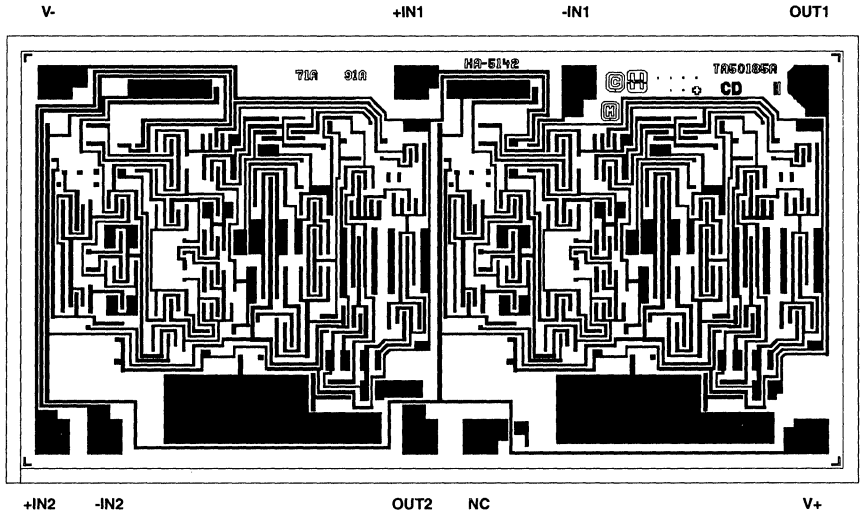
V-

PROCESS:

Bipolar/JFET Dielectric Isolation

Metallization Mask Layout

HA-5142



HARRIS SEMICONDUCTOR

HA-5147, HA-5147A

120MHz, Ultra-Low Noise Precision Operational Amplifiers

November 1996

Features

- Slew Rate 35V/μs
- Wide Gain Bandwidth ($A_V \geq 10$) 120MHz
- Low Noise ..... 3nV/$\sqrt{Hz}$ at 1kHz
- Low V_{OS} 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-5147-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-5147-5	0 to 75	8 Pin Metal Can	T8.C
HA2-5147A-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-5147A-5	0 to 75	8 Pin Metal Can	T8.C
HA3-5147-5	0 to 75	8 Ld PDIP	E8.3
HA7-5147-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5147-5	0 to 75	8 Ld CERDIP	F8.3A
HA7-5147A-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5147A-5	0 to 75	8 Ld CERDIP	F8.3A

Description

The HA-5147 operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (35V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10μV), wide gain bandwidth (120MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

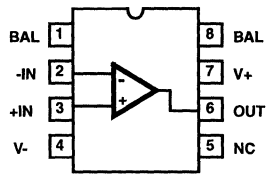
Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits. Further application ideas are given in Application Note 553, Harris AnswerFAX (407-724-7800) document #9553.

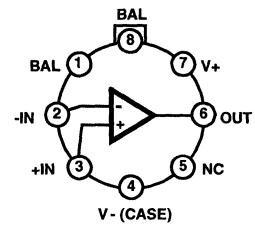
This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than ten. For military grade product, refer to the HA-5147/883 data sheet.

Pinouts

HA-5147, HA-5147A
(PDIP, CERDIP)
TOP VIEW



HA-5147, HA-5147A
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2910.2**

Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- Terminals . . . . . ±44V
Differential Input Voltage (Note 1) 0.7V
Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-5147/47A-2 . . . . . -55°C to 125°C
HA-5147/47A-5 . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	135	50
Can Package	155	67
PDIP Package	120	N/A

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Die Characteristics

Back Side Potential . . . . . V-
Number of Transistors 63

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L \leq 50pF$, $R_S \leq 100\Omega$

PARAMETERS	TEST CONDITIONS	TEMP. (°C)	HA-5147			HA-5147A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	30	100	-	10	25	µV
		Full	-	70	300	-	30	60	µV
Average Offset Voltage Drift		Full	-	0.4	1.8	-	0.2	0.6	µV/°C
Bias Current		25	-	15	80	-	10	40	nA
		Full	-	35	150	-	20	60	nA
Offset Current		25	-	12	75	-	7	35	nA
		Full	-	30	135	-	15	50	nA
Common Mode Range		Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 3)		25	0.8	4	-	1.5	6	-	MΩ
Input Noise Voltage (Note 4)	0.1Hz to 10Hz	25	-	0.09	0.25	-	0.08	0.18	μV_{P-P}
Input Noise Voltage Density (Note 5)	f = 10Hz	25	-	3.8	8.0	-	3.5	8.0	$nV/\sqrt{Hz}$
	f = 100Hz		-	3.3	4.5	-	3.1	4.5	$nV/\sqrt{Hz}$
	f = 1000Hz		-	3.2	3.8	-	3.0	3.8	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 5)	f = 10Hz	25	-	1.7	-	-	1.7	4.0	$pA/\sqrt{Hz}$
	f = 100Hz		-	1.0	-	-	1.0	2.3	$pA/\sqrt{Hz}$
	f = 1000Hz		-	0.4	0.6	-	0.4	0.6	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Minimum Stable Gain		25	10	-	-	10	-	-	V/V
Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 2k\Omega$	25	700	1500	-	1000	1800	-	V/mV
		Full	300	800	-	600	1200	-	V/mV
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	Full	100	120	-	114	126	-	dB

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L \leq 50pF$, $R_S \leq 100\Omega$ **(Continued)**

PARAMETERS	TEST CONDITIONS	TEMP. (°C)	HA-5147			HA-5147A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Gain-Bandwidth-Product	f = 10kHz	25	120	140	-	120	140	-	MHz
	f = 1MHz		-	120	-	-	120	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 600\Omega$	25	±10.0	±11.5	-	±10.0	±11.5	-	V
	$R_L = 2k\Omega$	Full	±11.4	±13.5	-	±11.7	±13.8	-	V
Full Power Bandwidth (Note 6)		25	445	500	-	445	500	-	kHz
Output Resistance	Open Loop	25	-	70	-	-	70	-	Ω
Output Current		25	16.5	25	-	16.5	25	-	mA
TRANSIENT RESPONSE (Note 7)									
Rise Time		25	-	22	50	-	22	50	ns
Slew Rate	$V_{OUT} = \pm3V$	25	28	35	-	28	35	-	V/µs
Settling Time	Note 8	25	-	400	-	-	400	-	ns
Overshoot		25	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	3.5	-	-	3.5	-	mA
		Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio	$V_S = \pm4V$ to ±18V	Full	-	16	51	-	2	4	µV/V

NOTES:

3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. The limits for this parameter are guaranteed based on lab characterization, and reflect lot-to-lot variation.
6. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
7. Refer to Test Circuits section of the data sheet.
8. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -10$.

Test Circuits and Waveforms

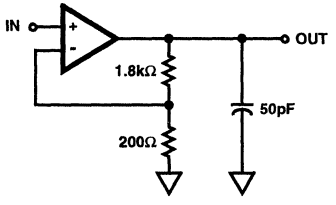
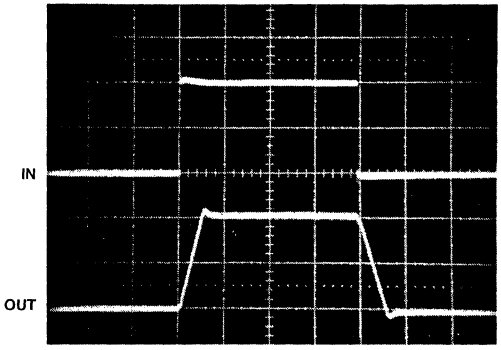


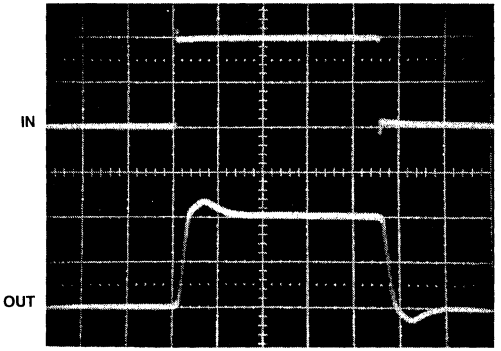
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

Test Circuits and Waveforms (Continued)



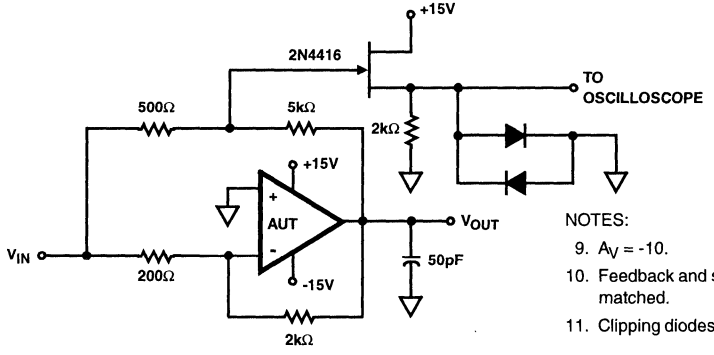
Vertical Scale: Input = 0.5V/Div.
Output = 5V/Div.
Horizontal Scale: 500ns/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: Input = 10mV/Div.
Output = 100mV/Div.
Horizontal Scale: 100ns/Div.

SMALL SIGNAL RESPONSE

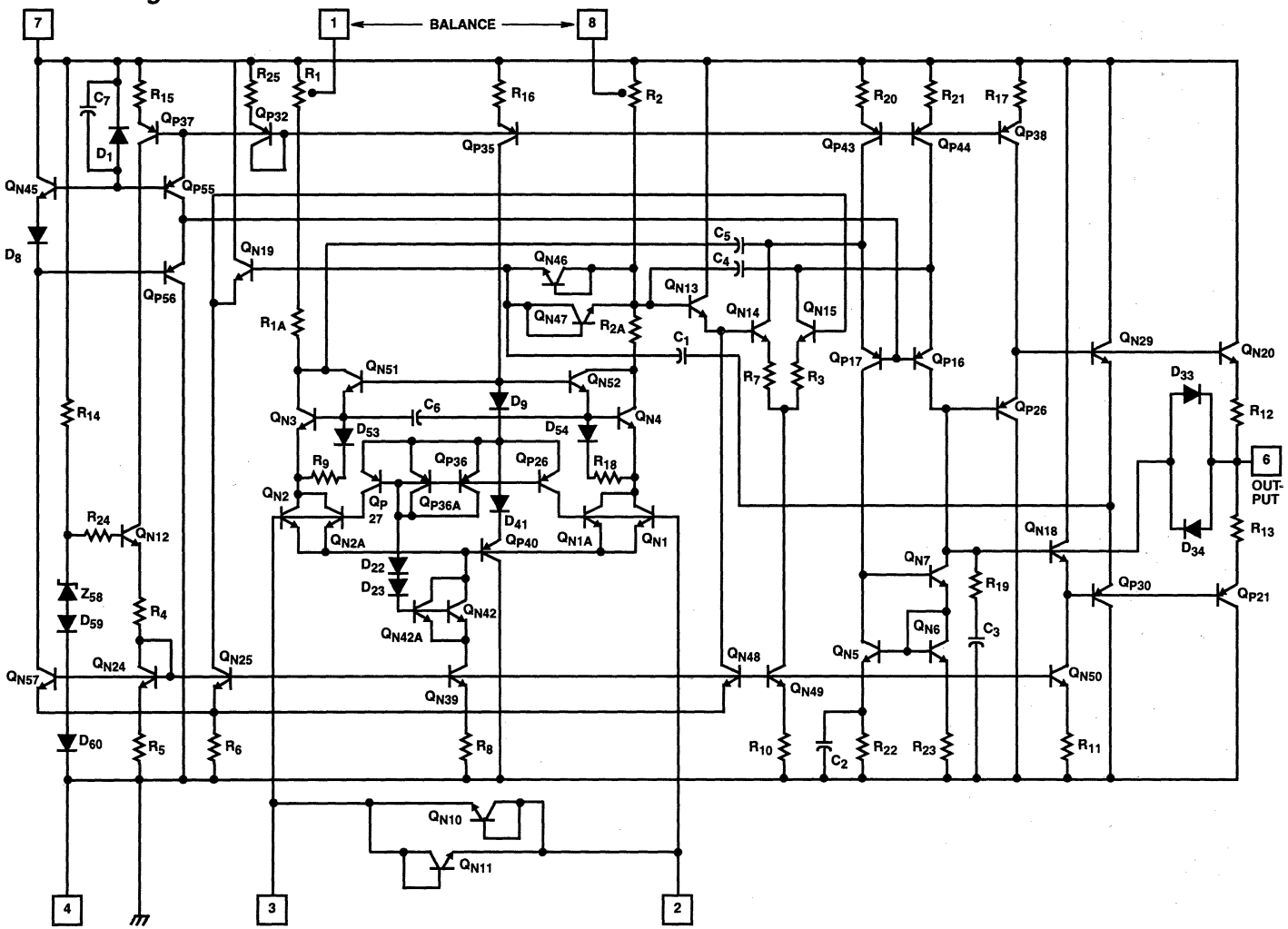


NOTES:

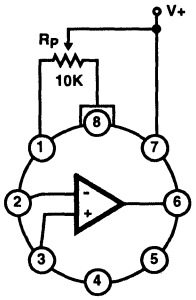
9. $A_V = -10$.
10. Feedback and summing resistors should be 0.1% matched.
11. Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram

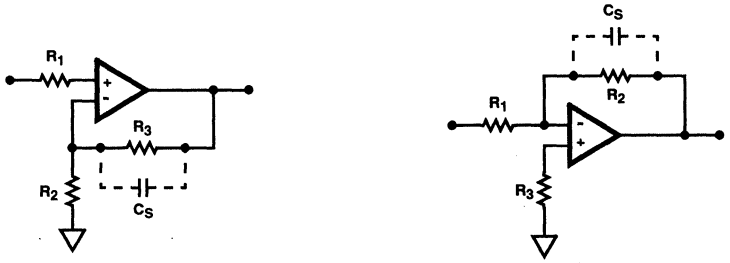


Application Information



NOTE: Tested Offset Adjustment Range is $|V_{OS}$ +1mV| minimum referred to output. Typical range is ±4mV with R_P = 10kΩ.

FIGURE 3. SUGGESTED OFFSET VOLTAGE ADJUSTMENT



NOTE: Low resistances are preferred for low noise applications as a 1kΩ resistor has 4nV/√Hz of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 4. SUGGESTED STABILITY CIRCUITS

Typical Performance Curves T_A = 25°C, V_{SUPPLY} = ±15V, Unless Otherwise Specified

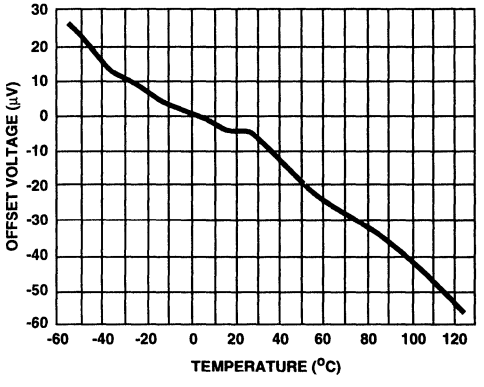


FIGURE 5. TYPICAL OFFSET VOLTAGE vs TEMPERATURE

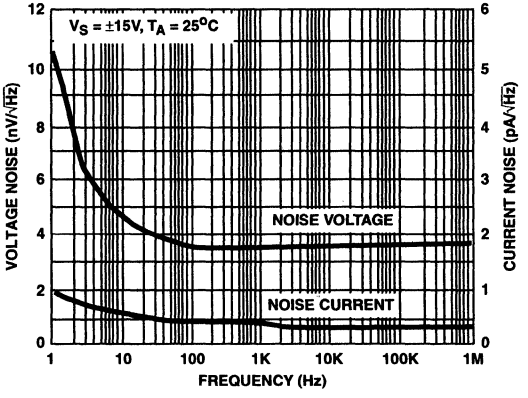


FIGURE 6. NOISE CHARACTERISTICS

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified (Continued)

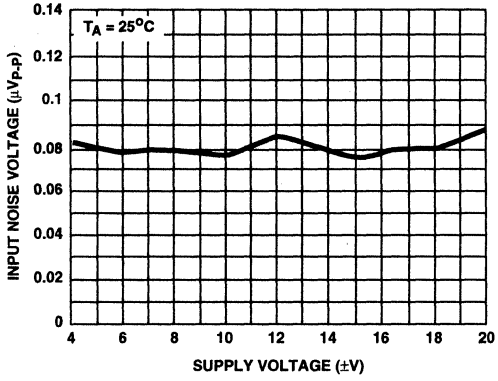


FIGURE 7. NOISE vs SUPPLY VOLTAGE

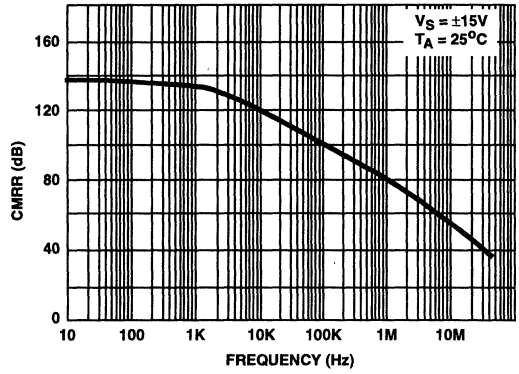


FIGURE 8. CMRR vs FREQUENCY

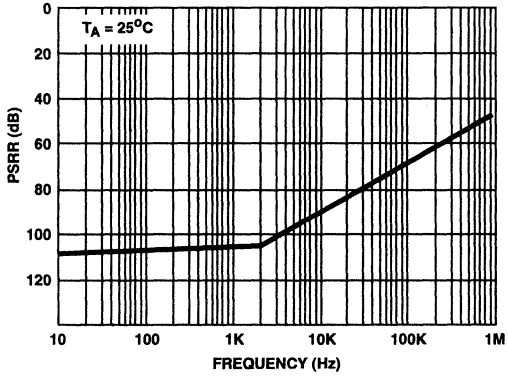


FIGURE 9. PSRR vs FREQUENCY

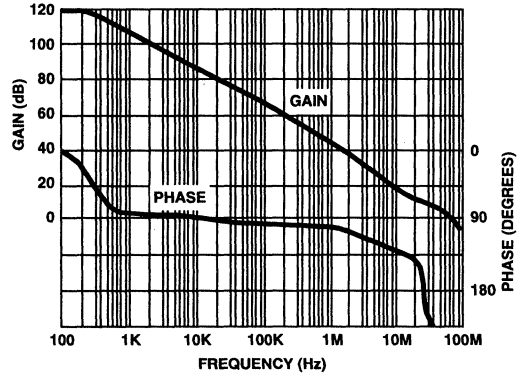


FIGURE 10. OPEN LOOP GAIN AND PHASE vs FREQUENCY

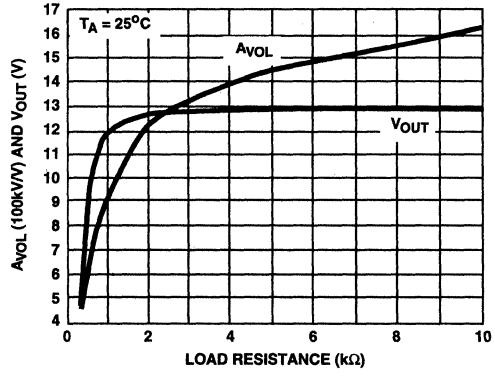


FIGURE 11. A_{VOL} AND V_{OUT} vs LOAD RESISTANCE

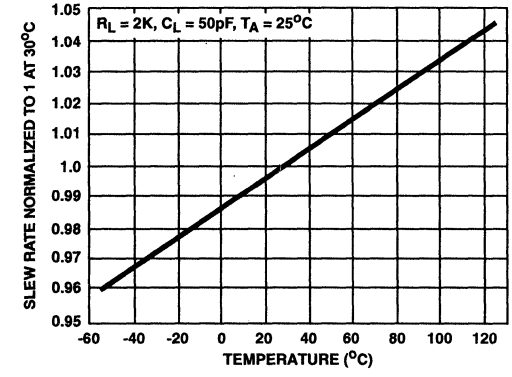


FIGURE 12. NORMALIZED SLEW RATE vs TEMPERATURE

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified (Continued)

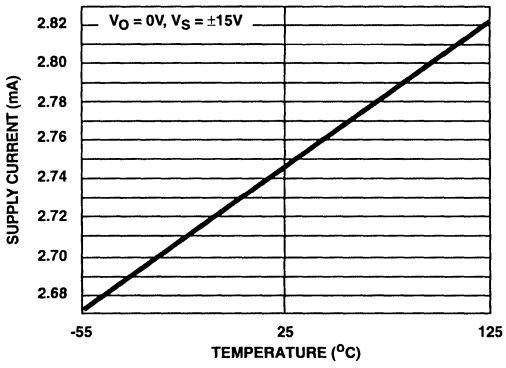


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

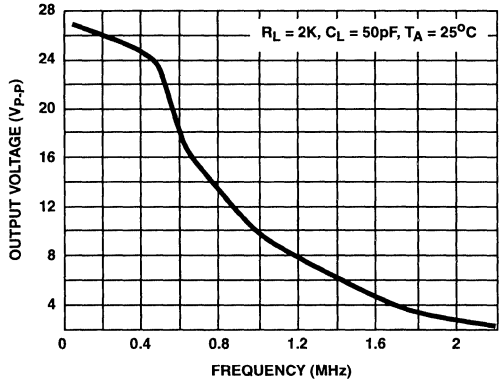


FIGURE 14. V_{OUT} MAX (UNDISTORTED SINEWAVE OUTPUT) vs FREQUENCY

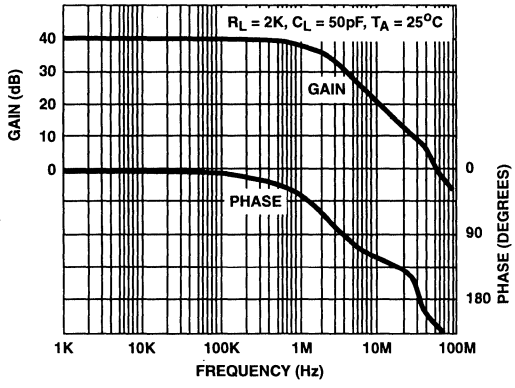
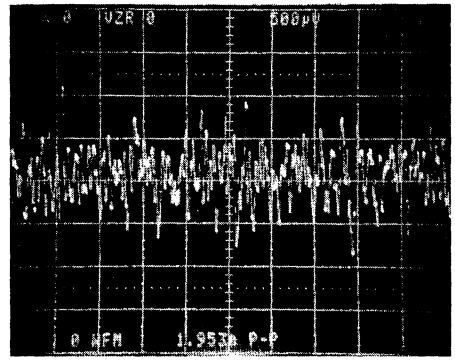


FIGURE 15. CLOSED LOOP GAIN AND PHASE vs FREQUENCY



A_{CL} = 25,000V/V; E_N = 0.08μV_{P-P} RTI
Horizontal Scale = 1s/Div.; Vertical Scale = 0.002μV/Div.

FIGURE 16. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)

HARRIS SEMICONDUCTOR

HA-5160, HA-5162

100MHz, JFET Input, High Slew Rate, Uncompensated, Operational Amplifiers

November 1996

Features

- Wide Gain Bandwidth ($A_V \geq 10$) 100MHz
- High Slew Rate..... 120V/μs
- Settling Time 280ns
- Power Bandwidth..... 1.9MHz
- Offset Voltage..... 1.0mV
- Bias Current..... 20pA

Applications

- Video and RF Amplifiers
- Data Acquisition
- Pulse Amplifiers
- Precision Signal Generation

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA2-5160-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-5160-5	0 to 75	8 Pin Metal Can	T8.C
HA2-5162-5	0 to 75	8 Pin Metal Can	T8.C

Description

The HA-5160 is a wideband, uncompensated, operational amplifier with FET/Bipolar technologies and Dielectric Isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

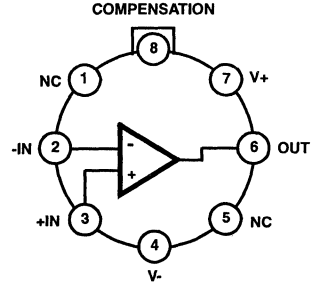
The HA-5160/5162 offers a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the Harris devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that Harris specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and a very high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications. The HA-5160 provides excellent performance for applications which require both precision and high speed performance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

Military version (/883) data sheets are available upon request.

Pinout

HA-5160/5162
(METAL CAN)
TOP VIEW



NOTE: Case connected to V-.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2911.2**

Absolute Maximum Ratings

Voltage Between V+ and V- 40V
Differential Input Voltage. 40V
Peak Output Current. . . . . Full Short Circuit Protection

Operating conditions

Temperature Ranges
HA-5160-2. . . . . -55°C to 125°C
HA-5160-5, HA-5162-5 . . . . . 0°C to 75°C
Supply Voltage Range (Typical) . . . . . ±7V to ±18V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	155	67

Maximum Junction Temperature . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Die Characteristics

Number of Transistors 82
Substrate Potential (Powered Up) . . . . . Floating

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5160-2 -55°C to 125°C			HA-5160-5 0°C to 75°C			HA-5162-5 0°C to 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS												
Offset Voltage		25	-	1	3	-	1	3	-	3	15	mV
		Full	-	3	5	-	3	5	-	5	20	mV
Offset Voltage Average Drift		Full	-	10	-	-	20	-	-	20	35	µV/°C
Bias Current		25	-	20	50	-	20	50	-	20	65	pA
		Full	-	5	10	-	5	10	-	5	10	nA
Offset Current		25	-	2	10	-	2	10	-	2	10	pA
		Full	-	2	5	-	2	5	-	2	5	nA
Input Capacitance		25	-	5	-	-	5	-	-	5	-	pF
Input Resistance		25	-	10^{12}	-	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Range		Full	±10	±11	-	±10	±11	-	±10	±11	-	V
TRANSFER CHARACTERISTICS												
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2kΩ	25	75	150	-	75	150	-	25	100	-	kV/V
		Full	60	100	-	60	100	-	25	75	-	kV/V
Common Mode Rejection Ratio	V_{CM} = ±10V	Full	74	80	-	74	80	-	70	80	-	dB
Minimum Stable Gain		25	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth Product	$A_V \geq 10$	Full	-	100	-	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS												
Output Voltage Swing	R_L = 2kΩ	25	±10	±11	-	±10	±11	-	±10	±11	-	V
		Full	±10	±11	-	±10	±11	-	±10	±11	-	V
Output Current	V_{OUT} = ±10V	25	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Short Circuit Current		25	-	±35	-	-	±35	-	-	±35	-	mA
Full Power Bandwidth (Note 2)	V_{OUT} = ±10V, R_L = 2kΩ	25	1.6	1.9	-	1.6	1.9	-	0.8	1.1	-	MHz
Output Resistance	Open Loop	25	-	50	-	-	50	-	-	50	-	Ω
TRANSIENT RESPONSE (Note 3)												
Rise Time	A_V = +10	25	-	20	-	-	20	-	-	20	-	ns
Slew Rate	A_V = +10	25	100	120	-	100	120	-	50	70	-	V/µs
Settling Time (Note 4)	A_V = -10	25	-	280	-	-	280	-	-	400	-	ns

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5160-2 -55°C to 125°C			HA-5160-5 0°C to 75°C			HA-5162-5 0°C to 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS												
Supply Current		Full	-	8	10	-	8	10	-	8	12	mA
Power Supply Rejection Ratio	V_S = ±10V to ±20V	25	74	86	-	74	86	-	70	86	-	dB

NOTES:

2. Full Power Bandwidth guaranteed, based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
3. Refer to Test circuits section of the data sheet.
4. Settling Time is measured to 0.2% of final value for a 10V output step.

Test Circuits and Waveforms

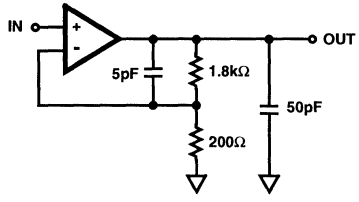
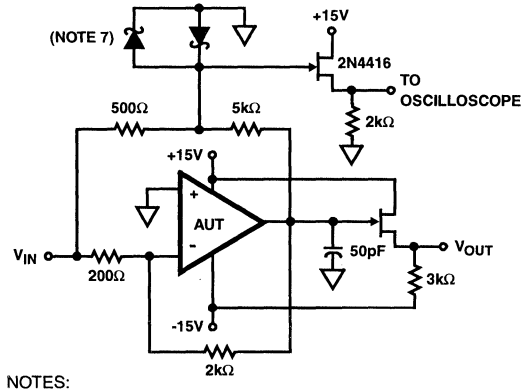


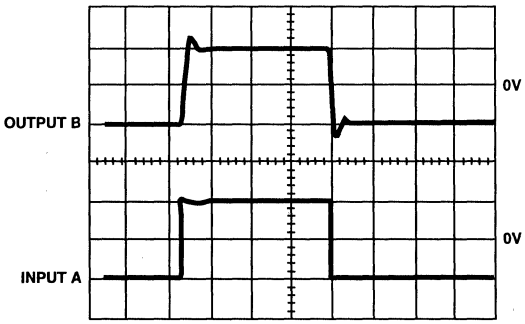
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



NOTES:

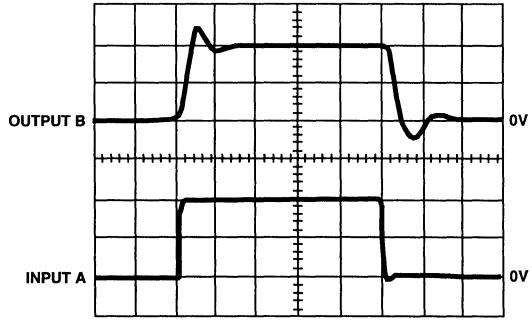
5. A_V = -10.
6. Feedback and summing resistors should be 0.1% matched.
7. Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT



Vertical Scale: A = 0.5V/Div., B = 5V/Div.
Horizontal Scale: 500ns/Div.

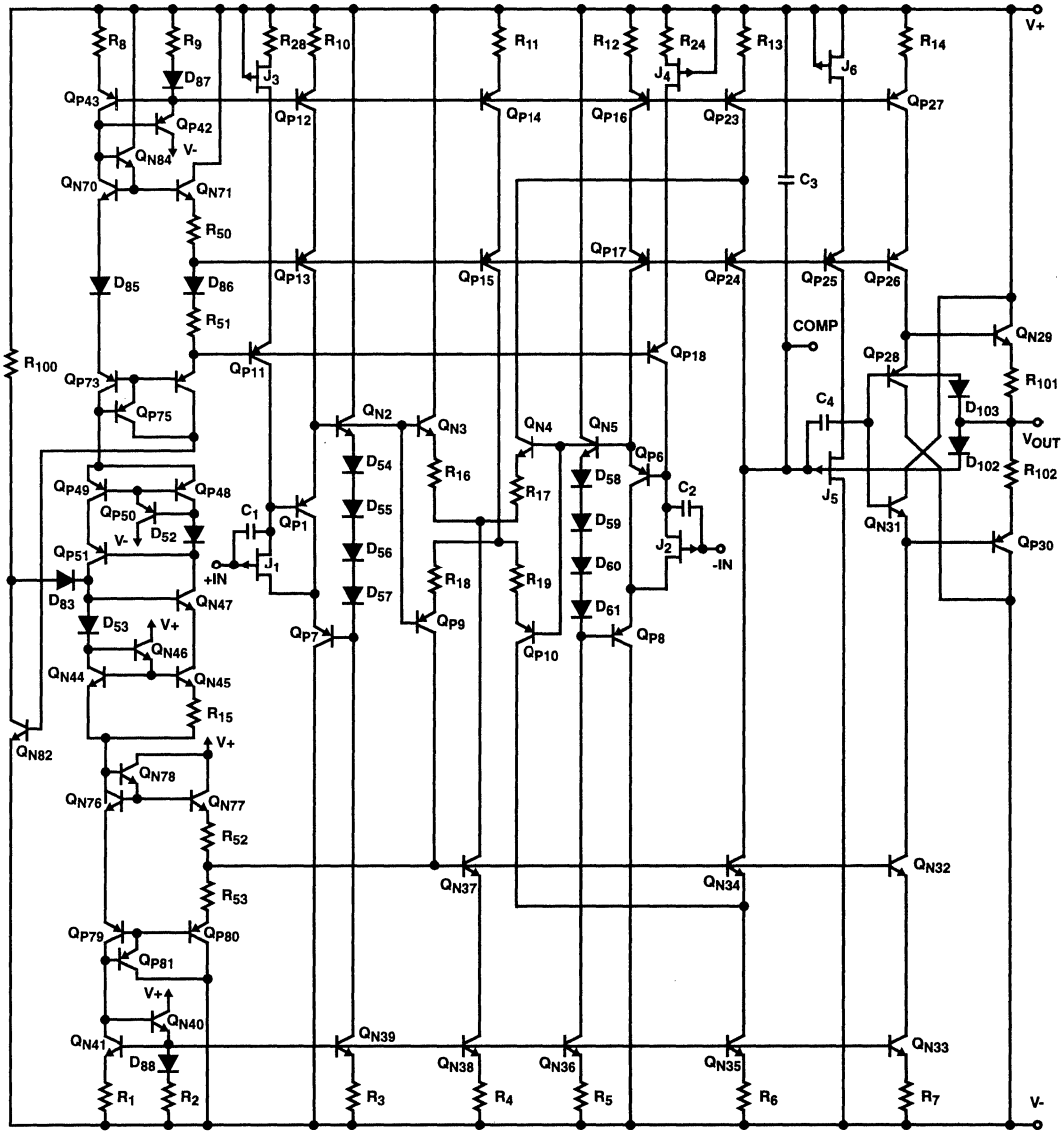
LARGE SIGNAL RESPONSE



Vertical Scale: A = 10mV/Div., B = 100mV/Div.
Horizontal Scale: 100ns/Div.

SMALL SIGNAL RESPONSE

Schematic Diagram



Application Information

Power Supply Decoupling

Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

Stability

The phase margin of the HA-5160/5162 will be improved by connecting a small capacitor (>10pF) between the output and the inverting input of the device This small capacitor compensates for the input capacitance of the FET.

Capacitive Loads

When driving large capacitive loads (>100pF), it is suggested that a small resistor (≈100Ω) be connected in series with the output of the device and inside the feedback loop.

Power Supply Minimum

The absolute supply minimum is ±6V and the safe level is ±7V.

Typical Applications

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY (NOTE)

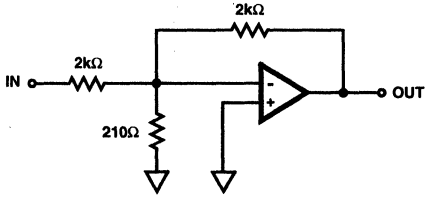
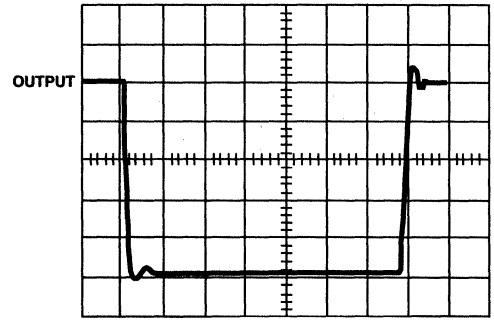


FIGURE 3A. INVERTING UNITY GAIN CIRCUIT



Vertical Scale: 2V/Div.
Horizontal Scale: 500ns/Div.

FIGURE 3B. INVERTING UNITY GAIN PULSE RESPONSE

FIGURE 3. GAIN OF -1

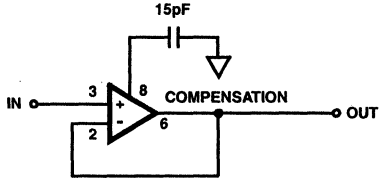
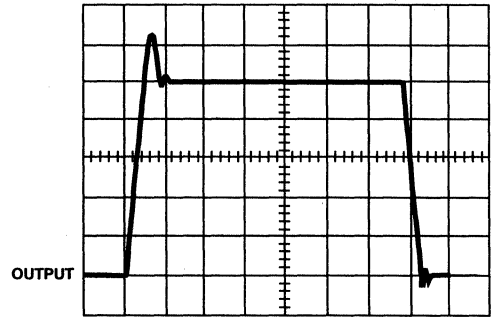


FIGURE 4A. NONINVERTING UNITY GAIN CIRCUIT



Vertical Scale: 2V/Div.
Horizontal Scale: 500ns/Div.

FIGURE 4B. NONINVERTING UNITY GAIN PULSE RESPONSE

FIGURE 4. GAIN OF +1

NOTE: Values were determined experimentally for optimum speed and settling time.

Typical Performance Curves

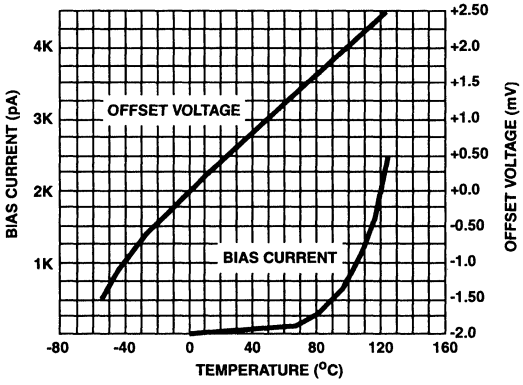


FIGURE 5. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

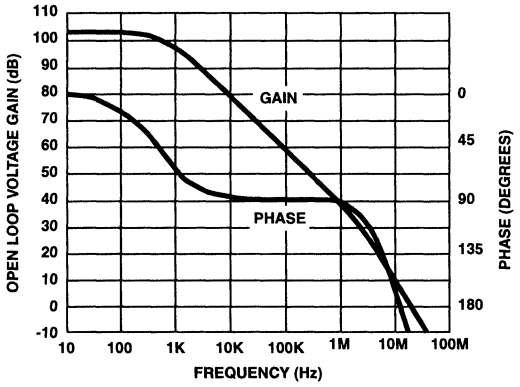


FIGURE 6. OPEN LOOP FREQUENCY RESPONSE

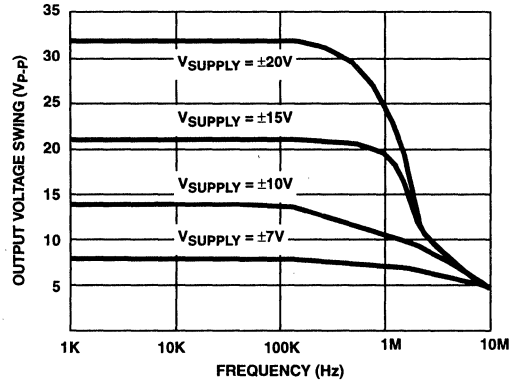


FIGURE 7. OUTPUT VOLTAGE SWING vs FREQUENCY

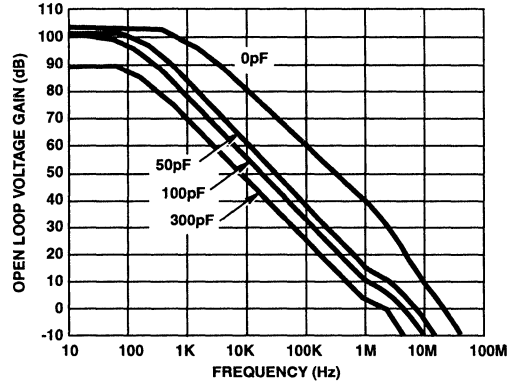


FIGURE 8. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS COMPENSATION CAPACITANCES

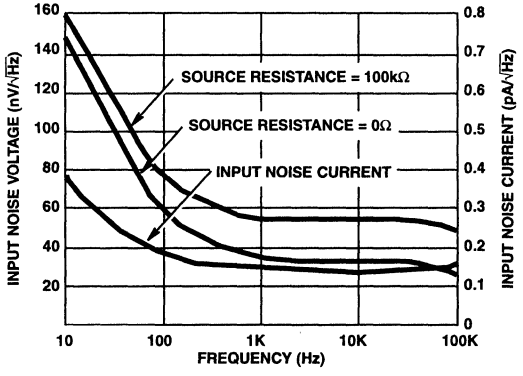


FIGURE 9. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

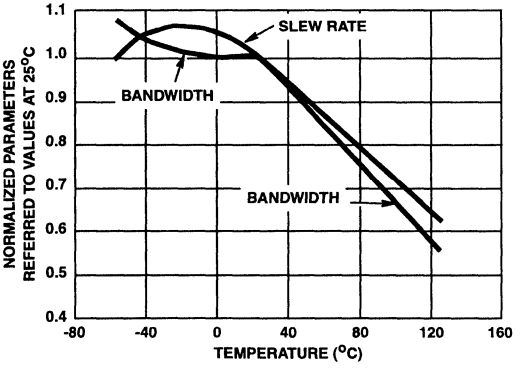


FIGURE 10. NORMALIZED AC PARAMETERS vs TEMPERATURE

Typical Performance Curves (Continued)

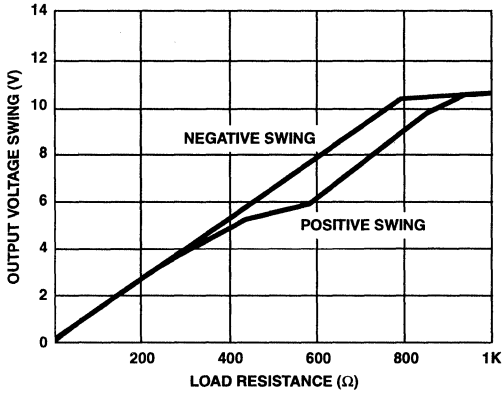


FIGURE 11. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

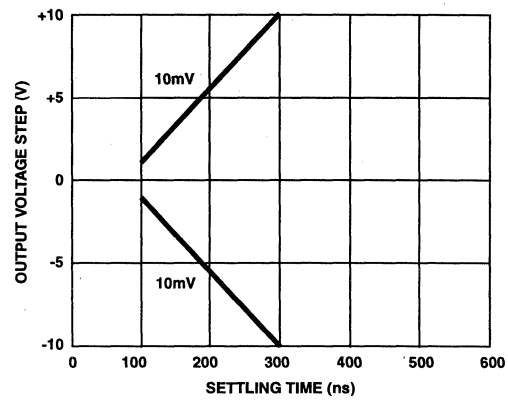


FIGURE 12. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

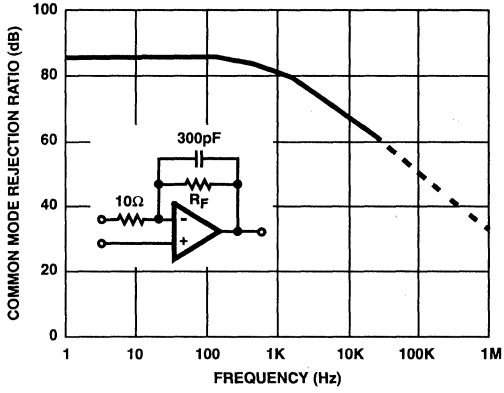


FIGURE 13. COMMON MODE REJECTION RATIO vs FREQUENCY

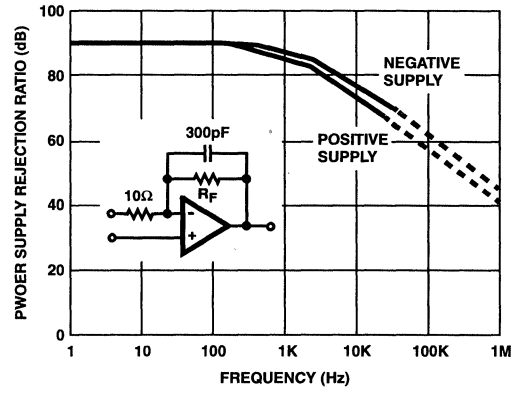


FIGURE 14. POWER SUPPLY REJECTION RATIO vs FREQUENCY

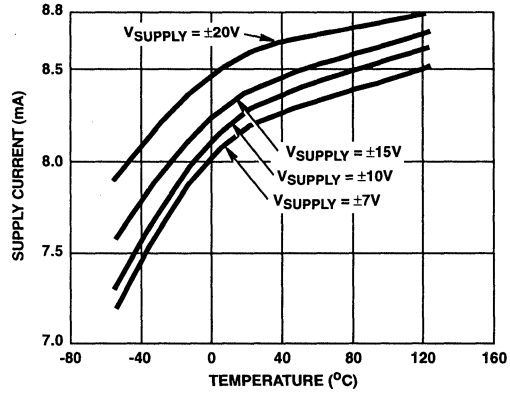


FIGURE 15. POWER SUPPLY CURRENT vs TEMPERATURE

HARRIS SEMICONDUCTOR

HA-5170

8MHz, Precision, JFET Input Operational Amplifier

November 1996

Features

- Low Offset Voltage 100μV
- Low Offset Voltage Drift . . . . . 2μV/°C
- Low Noise . . . . . 10nV/$\sqrt{Hz}$
- High Open Loop Gain 600kV/V
- Wide Bandwidth 8MHz
- Unity Gain Stable

Applications

- High Gain Instrumentation Amplifiers
- Precision Data Acquisition
- Precision Integrators
- Precision Threshold Detectors
- For Further Design Ideas, Refer to Application Note 540

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-5170-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-5170-5	0 to 75	8 Pin Metal Can	T8.C
HA7-5170-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5170-5	0 to 75	8 Ld CERDIP	F8.3A

Description

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

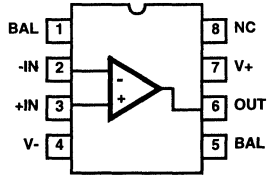
Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate and 8MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems. For application assistance, please refer to Application Note AN540 addressing specifically this device.

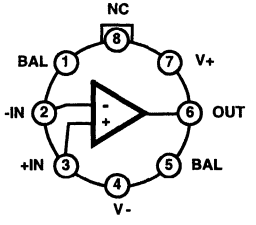
Military version (-8) product and data sheets available upon request.

Pinouts

HA-5170
(CERDIP)
TOP VIEW



HA-5170
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number **2912.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage. 30V
Output Short Circuit Duration . . . . . Indefinite

Operating Conditions

Temperature Range
HA-5170-2. . . . . -55°C to 125°C
HA-5170-5. . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	135	50
Metal Can Package	155	67

Maximum Junction Temperature . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5170-2 -55°C to 125°C			HA-5170-5 0°C to 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	0.1	0.3	-	0.1	0.3	mV
		Full	-	-	0.5	-	-	0.5	mV
Average Offset Voltage Drift (Note 3)		Full	-	2	5	-	2	5	µV/°C
Bias Current		25	-	20	100	-	20	100	pA
		Full	-	3	30	-	0.1	2	nA
Bias Current Average Drift		Full	-	3	-	-	3	-	pA/°C
Offset Current		25	-	3	30	-	3	60	pA
		Full	-	-	5	-	-	0.1	nA
Offset Current Average Drift (Note 3)		Full	-	0.3	1	-	0.3	1	pA/°C
Common Mode Range		Full	±10	+15.1	-	±10	+15.1	-	V
		Full		-12	-	-	-12	-	V
Differential Input Capacitance		25	-	80	100	-	80	100	pF
Differential Input Resistance (Note 3)		25	1×10^{10}	6×10^{10}	-	1×10^{10}	6×10^{10}	-	Ω
Input Capacitance (Single Ended)		25	-	12	-	-	12	-	pF
Input Noise Voltage (Note 3)	0.1Hz to10Hz	25	-	0.5	5	-	0.5	5	μV_{P-P}
Input Noise Voltage Density (Note 3)	f = 10Hz	25	-	20	150	-	20	150	$nV/\sqrt{Hz}$
	f = 100Hz	25	-	12	50	-	12	50	$nV/\sqrt{Hz}$
	f = 1000Hz	25	-	10	25	-	10	25	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 3)	f = 10Hz	25	-	0.05	-	-	0.05	-	$pA/\sqrt{Hz}$
	f = 100Hz	25	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
	f = 1000Hz	25	-	0.01	0.1	-	0.01	0.1	$pA/\sqrt{Hz}$

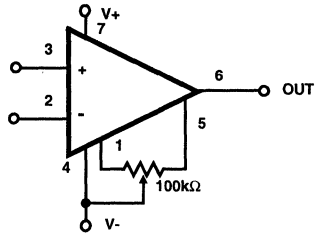
Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5170-2 -55°C to 125°C			HA-5170-5 0°C to 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2kΩ	25	300	600	-	300	600	-	kV/V
		Full	200	-	-	250	-	-	kV/V
Common Mode Rejection Ratio	ΔV_{CM} = ±10V	Full	85	100	-	90	100	-	dB
Minimum Stable Gain		25	1	-	-	1	-	-	V/V
Closed Loop Bandwidth	A_{VCL} = +1	25	4	8	-	4	8	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 2kΩ	25	±10	±12	-	±10	±12	-	V
Full Power Bandwidth (Note 4)	R_L = 2kΩ	25	80	120	-	80	120	-	kHz
Output Current (Note 5)	V_{OUT} = ±10V	25	±10	±15	-	±10	±15	-	mA
Output Resistance (Note 3)	Open Loop, 100Hz	25	-	45	100	-	45	100	Ω
TRANSIENT RESPONSE									
Rise Time	Note 2	25	-	45	100	-	45	100	ns
Slew Rate	Note 2	25	5	8	-	5	8	-	V/µs
Settling Time (Notes 3, 7)		25	-	1	5	-	1	5	µs
POWER SUPPLY CHARACTERISTICS									
Supply Current		Full	-	1.9	2.5	-	1.9	2.5	mA
Power Supply Rejection Ratio (Note 8)		Full	85	105	-	90	105	-	dB

NOTES:

2. See "Test Circuits and Waveforms" section.
3. Parameter is not 100% tested. 90% of all units meet or exceed these specifications.
4. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
5. I_{SC} turns on at ≅ 23mA.
6. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
7. V+ = +15V, V- = -10V to -20V and V- = -15V, V+ = +10V to +20V.

Test Circuits and Waveforms



Tested Offset Adjustment Range is $|V_{OS}$ + 1mV| minimum referred to output. Typical range is ±5mV with R_T = 1kΩ and ±15mV with R_T = 100kΩ.

FIGURE 1. V_{OS} ADJUSTMENT

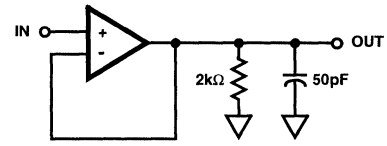
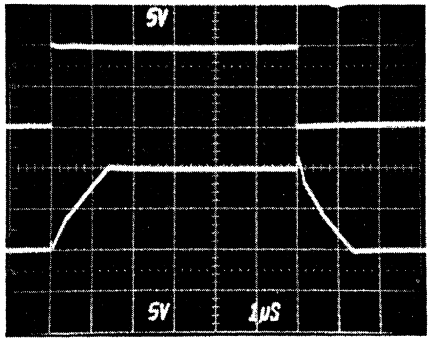
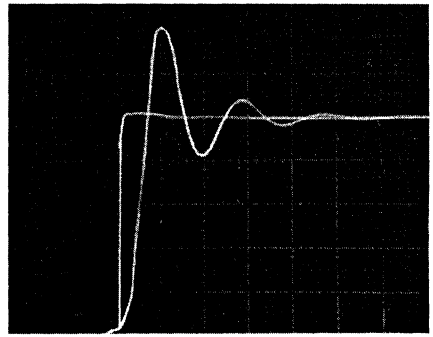


FIGURE 2. LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



Vertical Scale: 5V/Div.
Horizontal Scale: 1μs/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: 10mV/Div.
Horizontal Scale: 100ns/Div.

SMALL SIGNAL RESPONSE

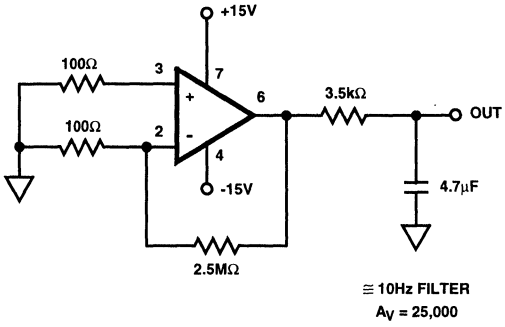
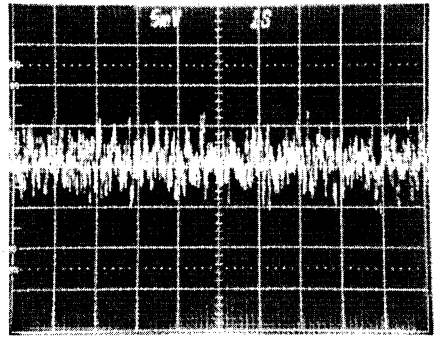


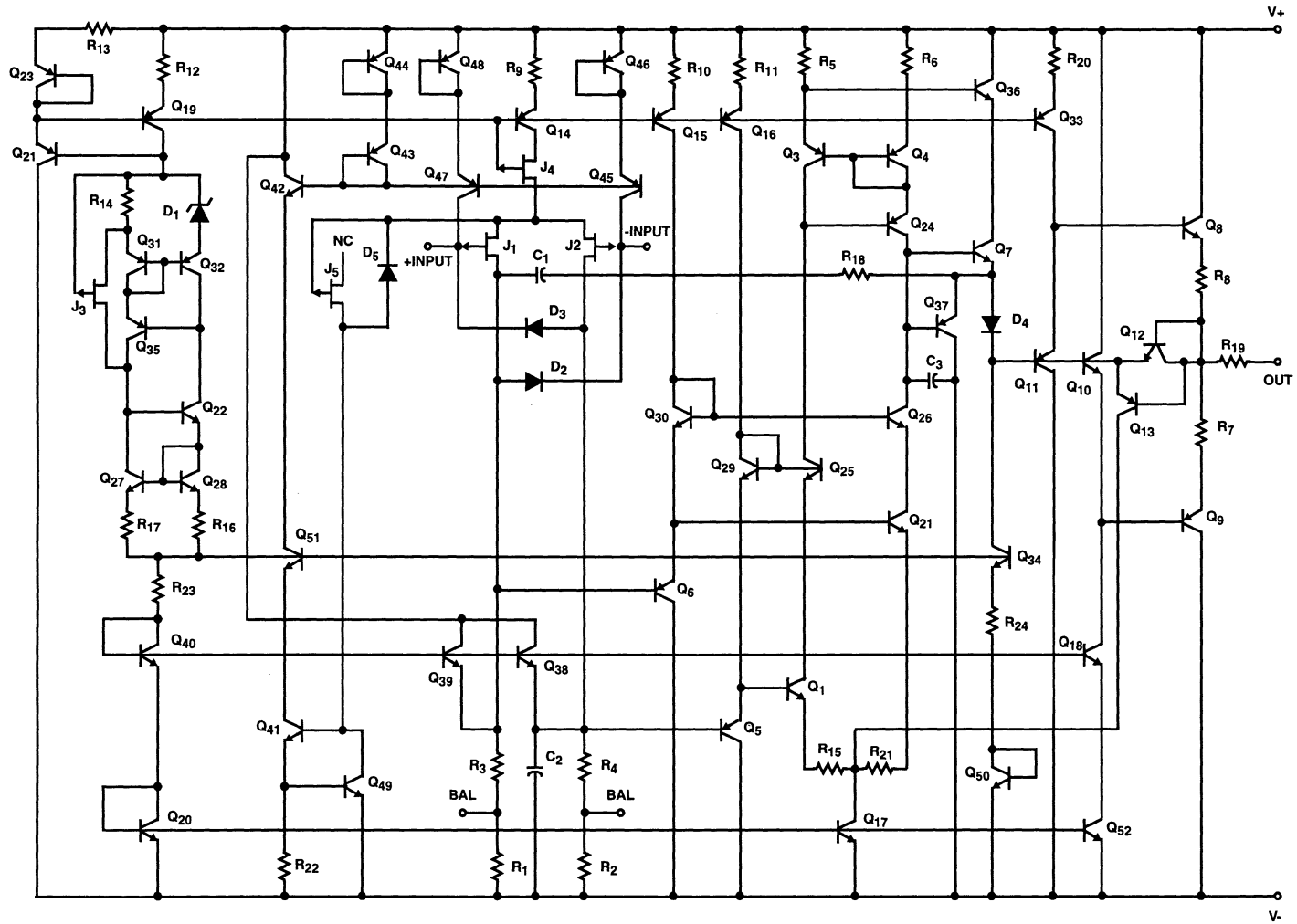
FIGURE 3. LOW FREQUENCY NOISE TEST CIRCUIT



Vertical Scale: 200nV/Div. (Noise Referred to Input)
5mV/Div. at Output, A_{VCL} = 25,000
Horizontal Scale: 1s/Div.

HA-5170 LOW FREQUENCY NOISE (0.1Hz TO 10Hz)

Schematic Diagram



Typical Performance Curves

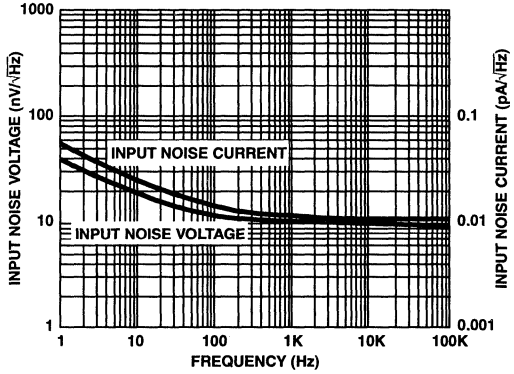


FIGURE 4. INPUT NOISE vs FREQUENCY

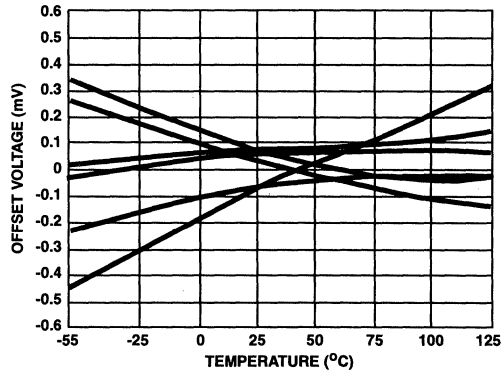


FIGURE 5. OFFSET VOLTAGE DRIFT vs TEMPERATURE OF REPRESENTATIVE UNITS

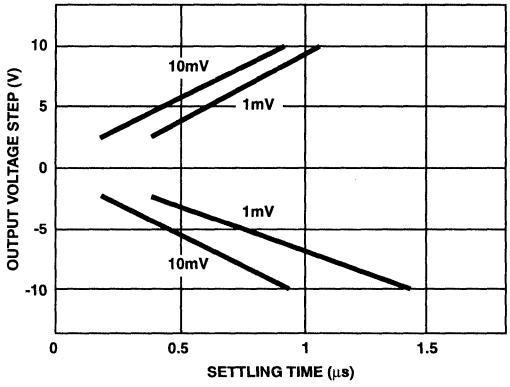


FIGURE 6. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

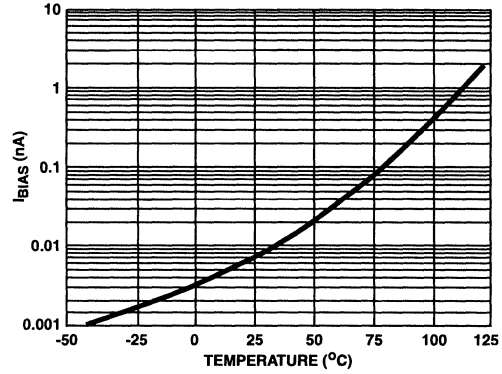


FIGURE 7. BIAS CURRENT vs TEMPERATURE

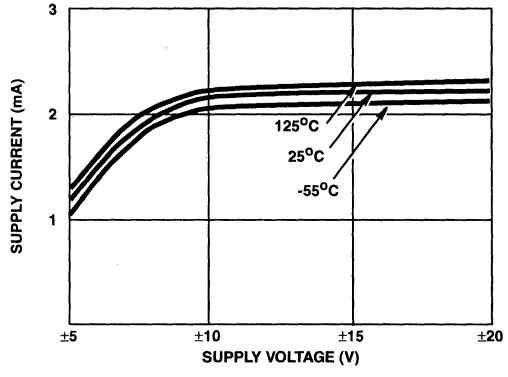


FIGURE 8. POWER SUPPLY CURRENT vs SUPPLY VOLTAGE

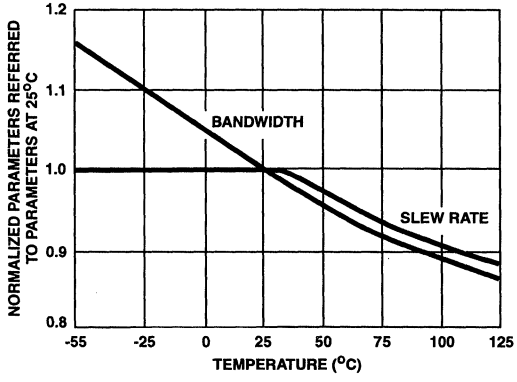


FIGURE 9. NORMALIZED AC PARAMETERS vs TEMPERATURE

Typical Performance Curves (Continued)

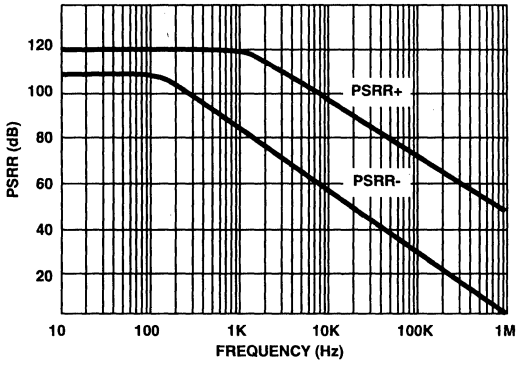


FIGURE 10. POWER SUPPLY REJECTION RATIO vs FREQUENCY

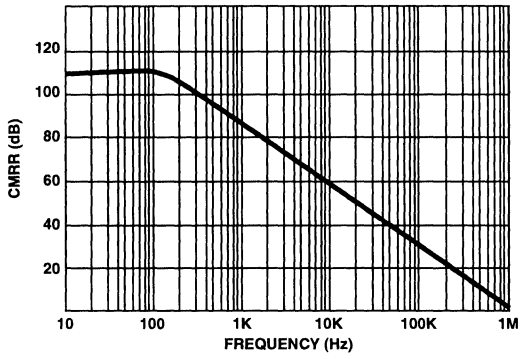


FIGURE 11. COMMON MODE REJECTION RATIO vs FREQUENCY

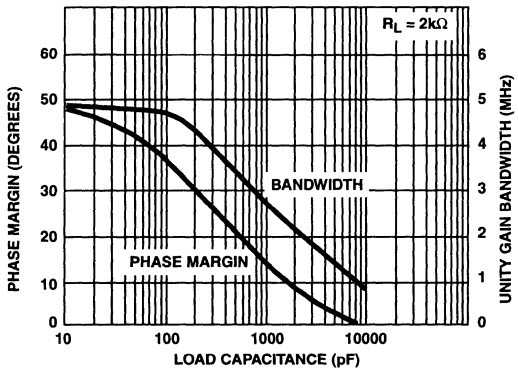


FIGURE 12. SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

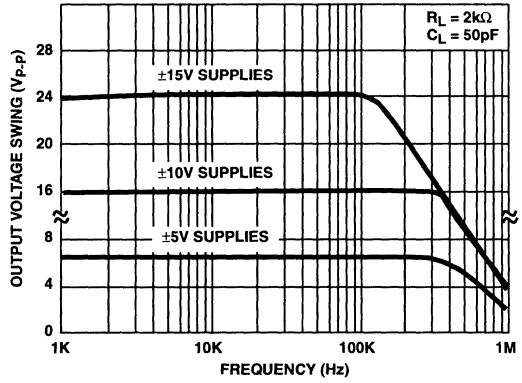


FIGURE 13. OUTPUT VOLTAGE SWING vs FREQUENCY AND SUPPLY VOLTAGE

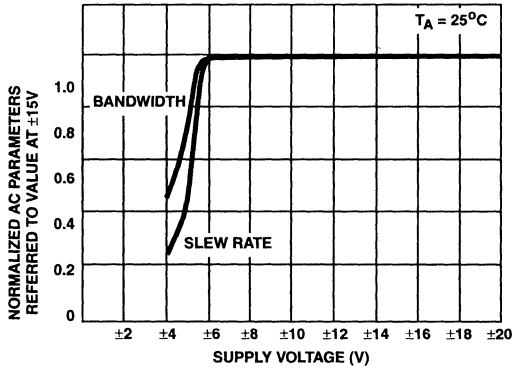


FIGURE 14. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

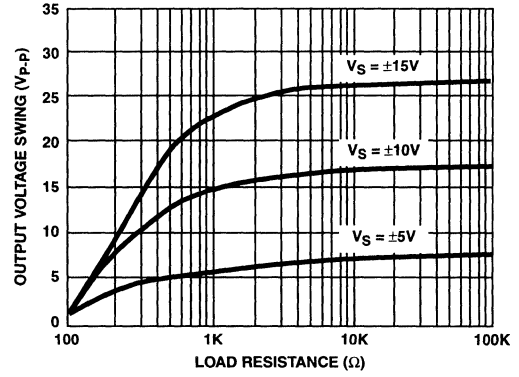


FIGURE 15. MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

Typical Performance Curves (Continued)

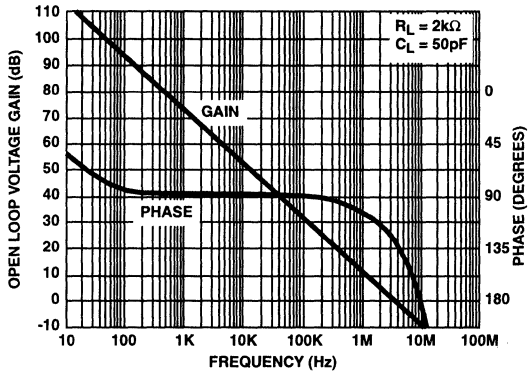


FIGURE 16. OPEN LOOP FREQUENCY RESPONSE

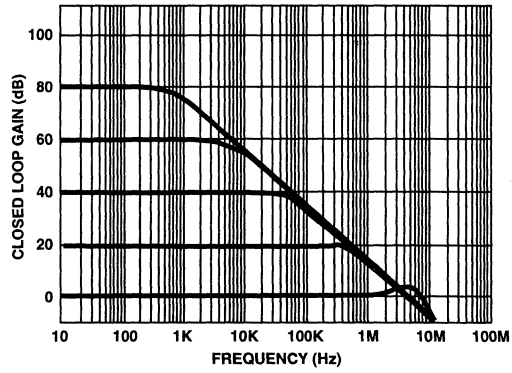


FIGURE 17. CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS

NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

HA-5177

2MHz, Ultra-Low Offset Voltage Operational Amplifier

November 1996

Features

- Low Offset Voltage 20μV
- Low Offset Voltage Drift . . . . . 0.2μV/°C
- High Voltage Gain 150dB
- High CMRR 140dB
- High PSRR 135dB
- Low Noise . . . . . 9.0nV/√Hz
- Low Power Consumption . . . . . 51mW (Max)

Applications

- High Gain Instrumentation Amplifiers
- Precision Control Systems
- Precision Integrators
- High Resolution Data Converters
- Precision Threshold Detectors
- Low Level Transducer Amplifiers

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3-5177-5	0 to 75	8 Ld PDIP	E8.3
HA7-5177-5	0 to 75	8 Ld CERDIP	F8.3A

Description

The HA-5177 is an all bipolar, precision operational amplifier, utilizing Harris dielectric isolation and advance processing techniques. This design features a combination of precision input characteristics, wide bandwidth (2MHz) and high speed (0.8V/μs).

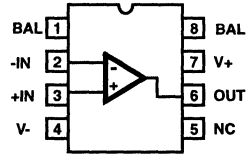
The HA-5177 uses advanced matching techniques and laser trimming to produce low offset voltage (20μV) and low offset voltage drift (0.2μV/°C). This design also features low voltage noise (9.0nV/√Hz), low current noise (1.2pA/√Hz), nanoamp input currents, and 120dB minimum gain.

These outstanding features along with high CMRR (140dB) and high PSRR (135dB) make this unity gain stable amplifier ideal for high resolution data acquisition systems, precision integrators, and low level transducer amplifiers.

The HA-5177 can be used as a direct replacement for the OP05, OP07, and OP77 while offering higher bandwidth and slew rate. See the HA-5177/883 data sheet for military grade parts and LCC package. Harris AnswerFAX (407-724-7800) Document #3733.

Pinout

HA-5177
(PDIP, CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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HA-5190, HA-5195

150MHz, Fast Settling Operational Amplifiers

November 1996

Features

- **Fast Settling Time (0.1%) 70ns**
- **Very High Slew Rate 200V/μs**
- **Wide Gain-Bandwidth ($A_V \geq 5$) 150MHz**
- **Full Power Bandwidth 6.5MHz**
- **Low Offset Voltage..... 3mV**
- **Input Noise Voltage ..... 6nV/$\sqrt{Hz}$**
- **Bipolar D.I. Construction**

Applications

- **Fast, Precise D/A Converters**
- **High Speed Sample-Hold Circuits**
- **Pulse and Video Amplifiers**
- **Wideband Amplifiers**

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA1-5190-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-5195-5	0 to 75	14 Ld CERDIP	F14.3
HA2-5190-2	-55 to 125	12 Pin Metal Can	T12.C
HA2-5195-5	0 to 75	12 Pin Metal Can	T12.C
HA9P5195-5	0 to 75	14 Ld SOIC	M14.15

Description

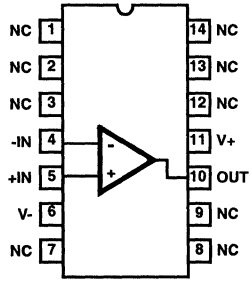
HA-5190/5195 are operational amplifiers featuring a combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with Dielectric Isolation, these devices are capable of delivering 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain bandwidth product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 3mV offset voltage and 6.0nV/$\sqrt{Hz}$ input voltage noise at 1kHz.

With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. The 5190/5195 are also ideally suited for a variety of pulse and wideband video amplifiers. Please refer to Application Notes AN525 and AN526 for some of these application designs.

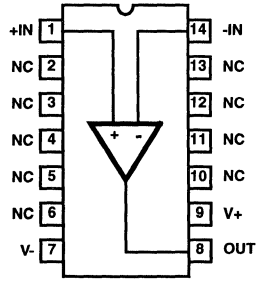
At temperatures above 75^{o}C a heat sink is required for the HA-5190 (see Note 2 and Application Note AN556). For military versions, please request the HA-5190/883 data sheet.

Pinout

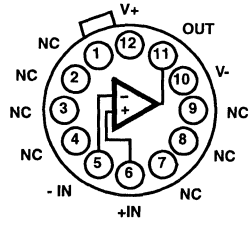
HA-5190/5195 (CERDIP)
TOP VIEW



HA-5195 (SOIC)
TOP VIEW



HA-5190/5195 (METAL CAN)
TOP VIEW



NOTE: Case Tied To V-.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2914.2**

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V+ to V-) 35V
Differential Input Voltage. 6V
Output Current . . . . . 50mA (Peak)

Operating Conditions

Temperature Range
HA-5190-2. . . . . -55°C to 125°C
HA-5195-5. . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
Metal Can Package	65	34
SOIC Package	119	N/A

Maximum Junction Temperature (Hermetic Package, Note 1) . . 175°C
Maximum Junction Temperature (Plastic Package, Note 1) . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Heat sinking may be required, especially at $T_A \geq 75^oC$.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5190-2			HA-5195-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	3	5	-	3	6	mV
		Full	-	-	10	-	-	10	mV
Average Offset Voltage Drift		Full	-	20	-	-	20	-	µV/°C
Bias Current		25	-	5	15	-	5	15	µA
		Full	-	-	20	-	-	20	µA
Offset Current		25	-	1	4	-	1	4	µA
		Full	-	-	6	-	-	6	µA
Input Resistance		25	-	10	-	-	10	-	kΩ
Input Capacitance		25	-	1	-	-	1	-	pF
Common Mode Range		Full	±5	-	-	±5	-	-	V
Input Noise Current	f = 1kHz, $R_G = 0\Omega$	25	-	5	-	-	5	-	$pA/\sqrt{Hz}$
Input Noise Voltage	f = 1kHz, $R_G = 0\Omega$	25	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Note 3)		25	15	30	-	10	30	-	kV/V
		Full	5	-	-	5	-	-	kV/V
Common Mode Rejection Ratio	$\Delta V_{CM} = \pm5V$	Full	74	95	-	74	95	-	dB
Minimum Stable Gain		25	5	-	-	5	-	-	V/V
Gain-Bandwidth-Product	$V_{OUT} = 90mV$, $A_V = 10$	25	-	150	-	150	-	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing (Note 3)		Full	±5	±8	-	±5	±8	-	V
Output Current (Note 3)		25	±25	±30	-	±25	±30	-	mA
Output Resistance	Open Loop	25	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3, 4)		25	5	6.5	-	5	6.5	-	MHz
TRANSIENT RESPONSE (Note 5)									
Rise Time		25	-	13	18	-	13	18	ns
Overshoot		25	-	8	-	-	8	-	%
Slew Rate		25	160	200	-	160	200	-	V/µs
Settling Time (Note 5)	5V Step to 0.1%	25	70	-	-	70	-	ns	25
	5V Step to 0.01%	25	-	100	-	-	100	-	ns
	2.5V Step to 0.1%	25	-	50	-	-	50	-	ns
	2.5V Step to 0.01%	25	-	80	-	-	80	-	ns

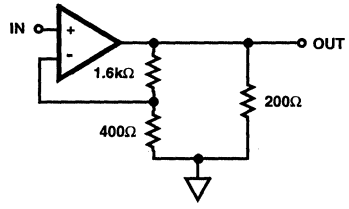
Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5190-2			HA-5195-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Supply Current		Full	-	19	28	-	19	28	mA
Power Supply Rejection Ratio	ΔV_S = ±10V to ±20V	Full	70	90	-	70	90	-	dB

NOTES:

3. R_L = 200Ω, C_L < 10pF, V_{OUT} = ±5V.
4. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
5. Refer to Test Circuits section of the data sheet.

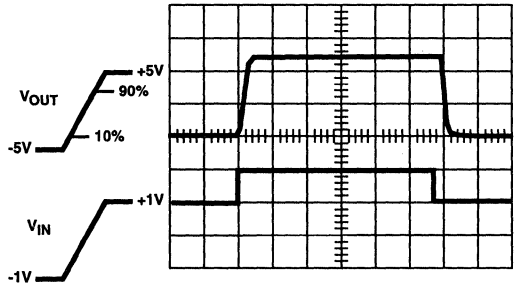
Test Circuits and Waveforms



NOTES:

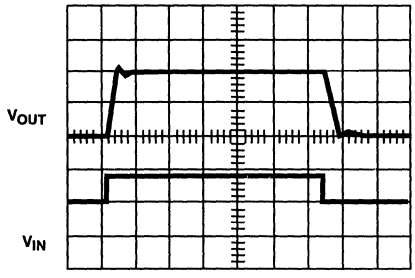
6. A_V = 5.
7. C_L < 10pF.

FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



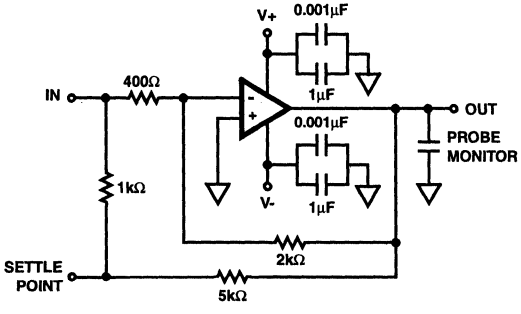
Vertical Scale: V_{IN} = 2.0V/Div., V_{OUT} = 4.0/Div.
Horizontal Scale: 100ns/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: V_{IN} = 50mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 100ns/Div

SMALL SIGNAL RESPONSE

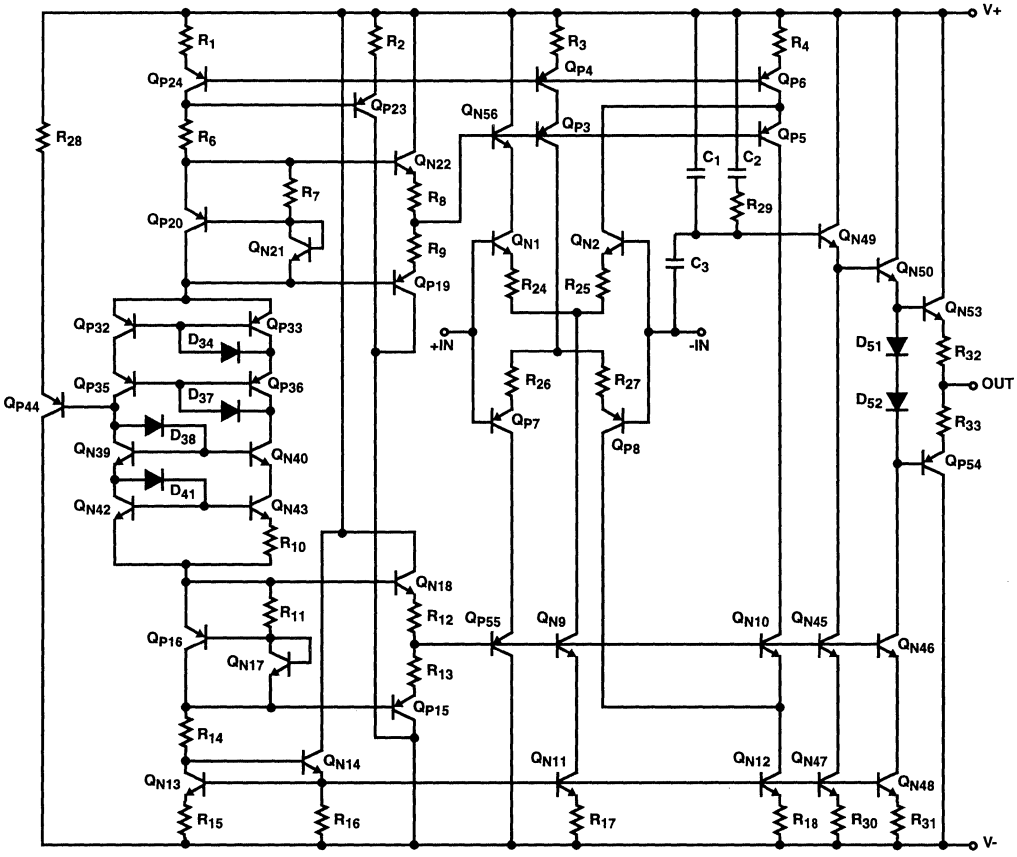


NOTES:

8. A_V = -5.
9. Load Capacitance should be less than 10pF.
10. It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
11. Settle Point (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram



Application Information

Power Supply Decoupling

Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

Stability Considerations

HA-5190/5195 is stable at gains > 5. Gains < 5 are covered below. Feedback resistors should be of carbon composition located as near to the input terminals as possible.

Wiring Considerations

Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.

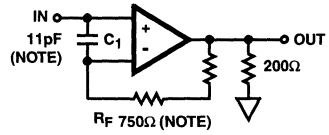
Output Short Circuit

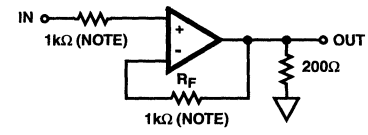
HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.

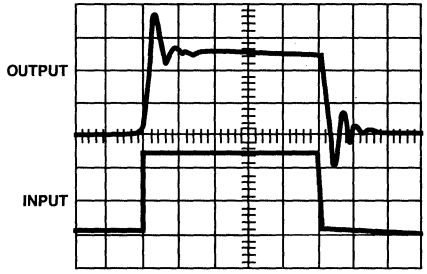
Heavy Capacitive Loads

When driving heavy capacitive loads (>100pF) a small resistor (100Ω) should be connected in series with the output and inside the feedback loop.

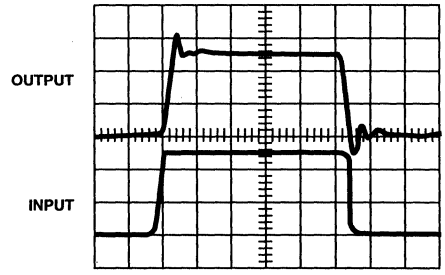
Typical Applications (Also see Application Notes AN525 and AN526)







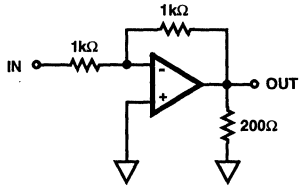
Vertical Scale: 2V/Div.
Horizontal Scale: 100ns/Div.

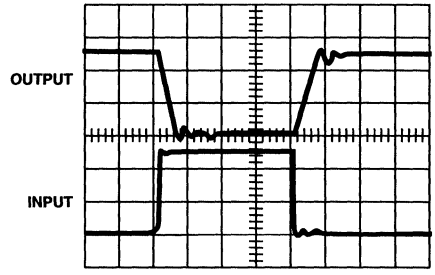


Vertical Scale: 2V/Div.
Horizontal Scale: 100ns/Div

NOTE: Values were determined experimentally for optimum speed and settling time. R_F and C_1 should be optimized for each particular application to ensure best overall frequency response.

FIGURE 3. SUGGESTED COMPENSATION FOR NONINVERTING UNITY GAIN AMPLIFIER





Vertical Scale: 2V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 4. SUGGESTED COMPENSATION FOR INVERTING UNITY GAIN AMPLIFIER

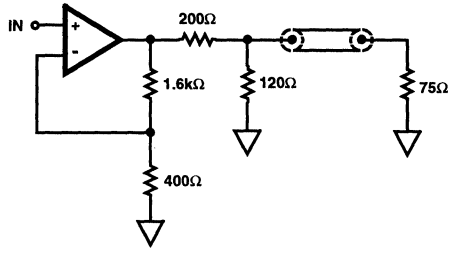


FIGURE 5. VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER

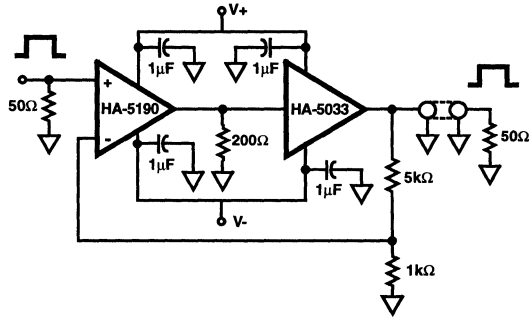


FIGURE 6. VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$, Unless Otherwise Specified

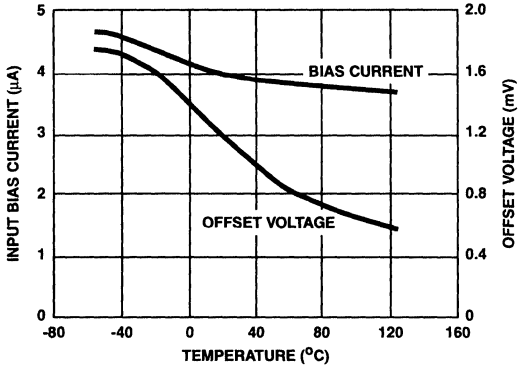


FIGURE 7. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

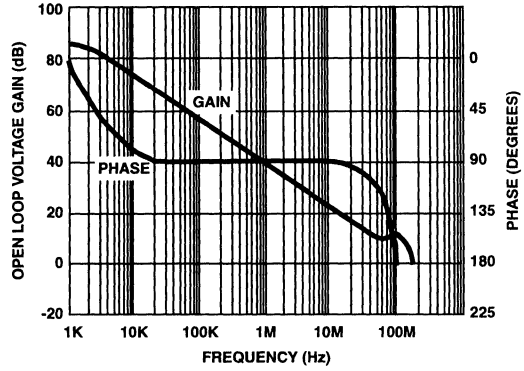


FIGURE 8. OPEN LOOP FREQUENCY RESPONSE

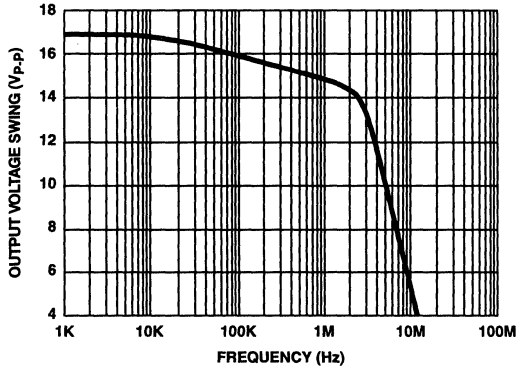


FIGURE 9. OUTPUT VOLTAGE SWING vs FREQUENCY

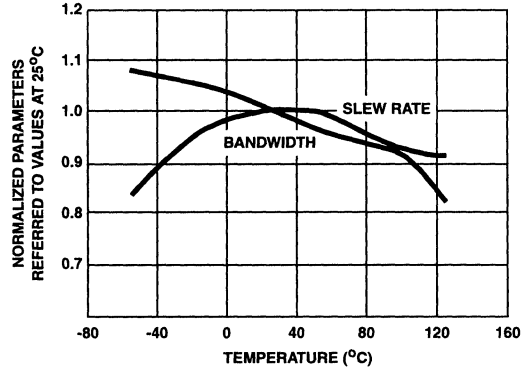


FIGURE 10. NORMALIZED AC PARAMETERS vs TEMPERATURE

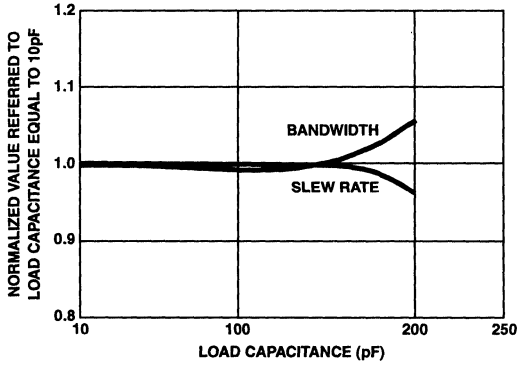


FIGURE 11. NORMALIZED AC PARAMETERS vs LOAD CAPACITANCE

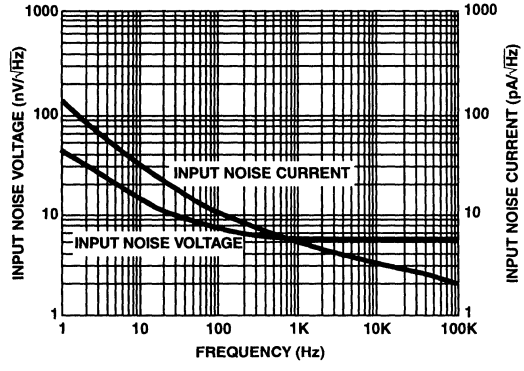


FIGURE 12. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified (Continued)

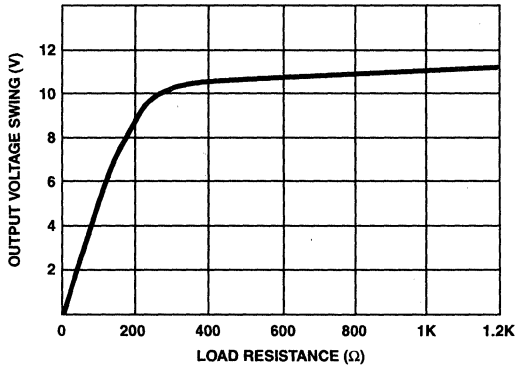


FIGURE 13. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

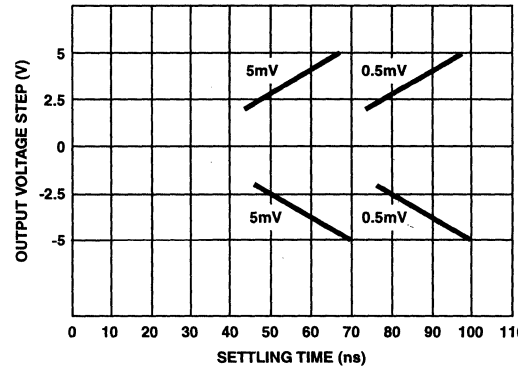


FIGURE 14. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

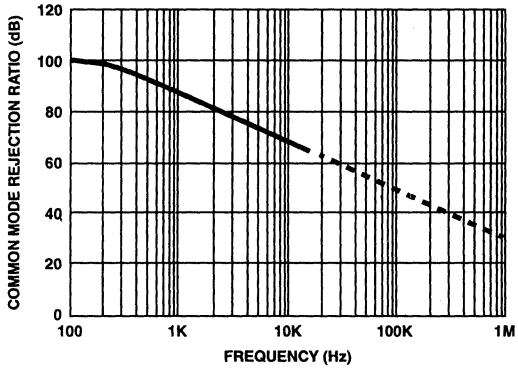


FIGURE 15. COMMON MODE REJECTION RATIO vs FREQUENCY

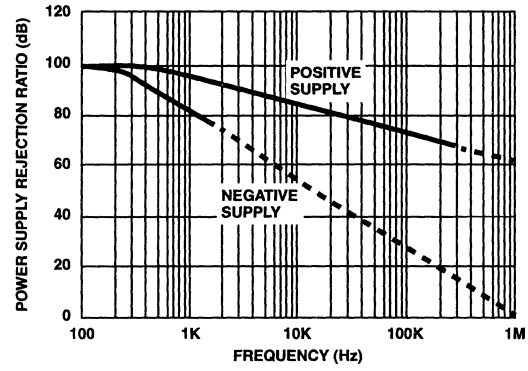


FIGURE 16. POWER SUPPLY REJECTION RATIO vs FREQUENCY

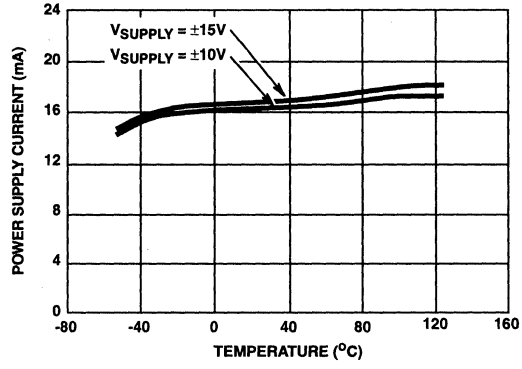


FIGURE 17. POWER SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

54 mils x 88 mils x 19 mils
1360µm x 2240µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

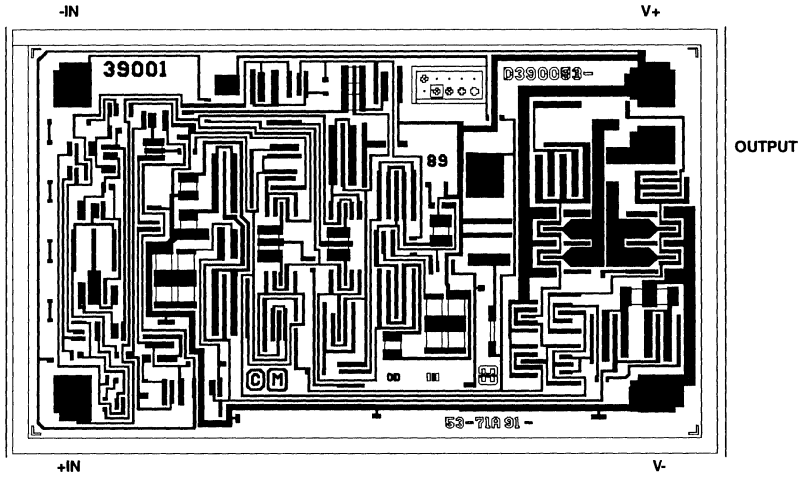
49

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5190



HARRIS SEMICONDUCTOR

HA-5221, HA-5222

100MHz, Single and Dual Low Noise, Precision Operational Amplifiers

November 1996

Features

- Gain Bandwidth Product 100MHz
- Unity Gain Bandwidth 25MHz
- Slew Rate 25V/μs
- Low Offset Voltage 0.3mV
- High Open Loop Gain 128dB
- Channel Separation at 10kHz 110dB
- Low Noise Voltage at 1kHz . . . . . 3.4nV/$\sqrt{Hz}$
- High Output Current 56mA
- Low Supply Current per Amplifier 8mA

Applications

- Precision Test Systems
- Active Filtering
- Small Signal Video
- Accurate Signal Processing
- RF Signal Conditioning

Description

The HA-5221/5222 are single and dual high performance dielectrically isolated, op amps, featuring precision DC characteristics while providing excellent AC characteristics. Designed for audio, video, and other demanding applications, noise (3.4nV/$\sqrt{Hz}$ at 1kHz), total harmonic distortion (<0.005%), and DC errors are kept to a minimum.

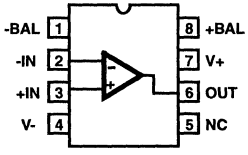
The precision performance is shown by low offset voltage (0.3mV), low bias currents (40nA), low offset currents (15nA), and high open loop gain (128dB). The combination of these excellent DC characteristics with the fast settling time (0.4μs) make the HA-5221/5222 ideally suited for precision signal conditioning.

The unique design of the HA-5221/5222 gives them outstanding AC characteristics not normally associated with precision op amps, high unity gain bandwidth (35MHz) and high slew rate (25V/μs). Other key specifications include high CMRR (95dB) and high PSRR (100dB). The combination of these specifications will allow the HA-5221/5222 to be used in RF signal conditioning as well as video amplifiers.

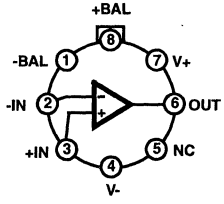
For MIL-STD-883C compliant product and Ceramic LCC packaging, consult the HA-5221/5222/883C data sheet. Harris AnswerFAX (407-724-7800) Document #3716.

Pinouts

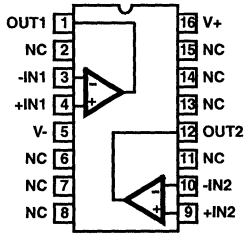
HA-5221 (PDIP, CERDIP, SOIC)
TOP VIEW



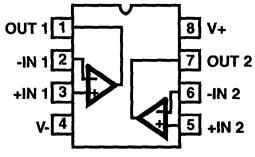
HA-5221 (METAL CAN)
TOP VIEW



HA-5222 (PDIP, SOIC)
TOP VIEW



HA-5222 (CERDIP)
TOP VIEW



Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-5221-5	0 to 75	8 Pin Metal Can	T8.C
HA3-5221-5	0 to 75	8 Ld PDIP	E8.3
HA7-5221-5	0 to 75	8 Ld CERDIP	F8.3A
HA7-5221-9	-40 to 85	8 Ld CERDIP	F8.3A
HA9P5221-5 (H52215)	0 to 75	8 Ld SOIC	M8.15
HA3-5222-5	0 to 75	16 Ld PDIP	E16.3
HA7-5222-5	0 to 75	8 Ld CERDIP	F8.3A
HA7-5222-9	-40 to 85	8 Ld CERDIP	F8.3A
HA9P5222-5	0 to 75	16 Ld SOIC	M16.3
HA9P5222-9	-40 to 85	16 Ld SOIC	M16.3

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2915.2**

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 35V
Differential Input Voltage (Note 1). 5V
Output Current Short Circuit Duration . . . . . Indefinite

Operating Conditions

Temperature Range
HA-5221/5222-9 . . . . . $-40^{o}C$ to $85^{o}C$
HA-5221/5222-5 . . . . . $0^{o}C$ to $75^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
Metal Can Package	165	80
CERDIP Package (HA7-5221)	135	50
CERDIP Package (HA7-5222)	115	30
8 Ld PDIP Package	92	N/A
8 Ld SOIC Package	157	N/A
16 Ld PDIP Package	85	N/A
16 Ld SOIC Package	95	N/A

Maximum Junction Temperature (Hermetic Package) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Input is protected by back-to-back zener diodes. See applications section.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	HA-5221-9, HA-5222-9			HA-5221-5, HA-5222-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Input Offset Voltage		25	-	0.30	0.75	-	0.30	0.75	mV
		Full	-	0.35	1.5	-	0.35	1.5	mV
Average Offset Voltage Drift		Full	-	0.5	-	-	0.5	-	$\mu V/^{o}C$
Input Bias Current		25	-	40	80	-	40	100	nA
		Full	-	70	200	-	70	200	nA
Input Offset Current		25	-	15	50	-	15	100	nA
		Full	-	30	150	-	30	150	nA
Input Offset Voltage Match		25	-	400	750	-	400	750	μV
		Full	-	-	1500	-	-	1500	μV
Common Mode Range		25	±12	-	-	±12	-	-	V
Differential Input Resistance		25	-	70	-	-	70	-	kΩ
Input Noise Voltage	f = 0.1Hz to 10Hz	25	-	0.25	-	-	0.25	-	μV_{P-P}
Input Noise Voltage	f = 10Hz	25	-	6.2	10	-	6.2	10	$nV/\sqrt{Hz}$
Density (Notes 3, 12)	f = 100Hz	25	-	3.6	6	-	3.6	6	$nV/\sqrt{Hz}$
	f = 1000Hz	25	-	3.4	4.0	-	3.4	4.0	$nV/\sqrt{Hz}$
Input Noise Current	f = 10Hz	25	-	4.7	8.0	-	4.7	8.0	$pA/\sqrt{Hz}$
Density (Notes 3, 12	f = 100Hz	25	-	1.8	2.8	-	1.8	2.8	$pA/\sqrt{Hz}$
	f = 1000Hz	25	-	0.97	1.8	-	0.97	1.8	$pA/\sqrt{Hz}$
THD+N	Note 4	25	-	<0.005	-	-	<0.005	-	%

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5221-9, HA-5222-9			HA-5221-5, HA-5222-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	Note 5	25	106	128	-	106	128	-	dB
		Full	100	120	-	100	120	-	dB
CMRR	V_{CM} = ±10V	Full	86	95	-	86	95	-	dB
Unity Gain Bandwidth	-3dB	25	-	35	-	-	35	-	MHz
Gain Bandwidth Product	1kHz to 400kHz	25	-	100	-	-	100	-	MHz
Minimum Stable Gain		Full	1	-	-	1	-	-	V/V
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 333Ω	Full	±10	-	-	±10	-	-	V
	R_L = 1kΩ	25	±12	±12.5	-	±12	±12.5	-	V
	R_L = 1kΩ	Full	±11.5	±12.1	-	±11.5	±12.1	-	V
Output Current	V_{OUT} = ±10V	Full	±30	±56	-	±30	±56	-	mA
Output Resistance		25	-	10	-	-	10	-	Ω
Full Power Bandwidth	Note 6	25	239	398	-	239	398	-	kHz
Channel Separation	Note 7	25	-	110	-	-	110	-	dB
TRANSIENT RESPONSE (Note 11)									
Slew Rate	Notes 8, 12	Full	15	25	-	15	25	-	V/µs
Rise Time	Notes 9, 12	Full	-	13	20	-	13	20	ns
Overshoot	Notes 9, 12	Full	-	28	50	-	28	50	%
Settling Time (Note 10)	0.1%	25	-	0.4	-	-	0.4	-	µs
	0.01%	25	-	1.5	-	-	1.5	-	µs
POWER SUPPLY									
PSRR	V_S = ±10V to ±20V	Full	86	100	-	86	100	-	dB
Supply Current		Full	-	8	11	-	8	11	mA/Op Amp

NOTES:

3. Refer to typical performance curve in data sheet.
4. A_{VCL} = 10, f_O = 1kHz, V_O = $5V_{RMS}$, R_L = 600Ω, 10Hz to 100kHz, Minimum resolution of test equipment is 0.005%.
5. V_{OUT} = 0 to ±10V, R_L = 1kΩ, C_L = 50pF.
6. Full Power Bandwidth is calculated by: FPBW = $\frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, V_{PEAK} = 10V.
7. HA-5222 only, f = 10kHz, R_L = 1kΩ, C_L = 50pF.
8. V_{OUT} = ±2.5V, R_L = 1kΩ, C_L = 50pF.
9. V_{OUT} = ±100mV, R_L = 1kΩ, C_L = 50pF.
10. Settling time is specified for a 10V step and A_V = -1.
11. See Test Circuits.
12. Guaranteed by characterization.

Test Circuits and Waveforms

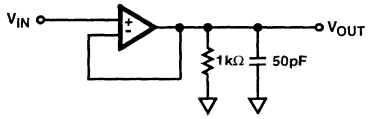
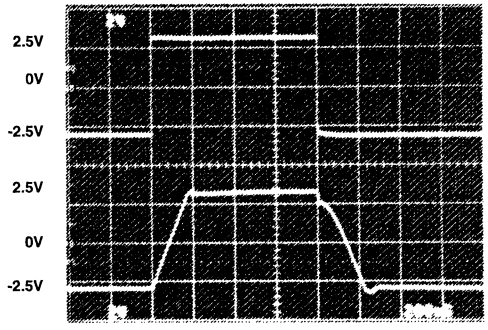
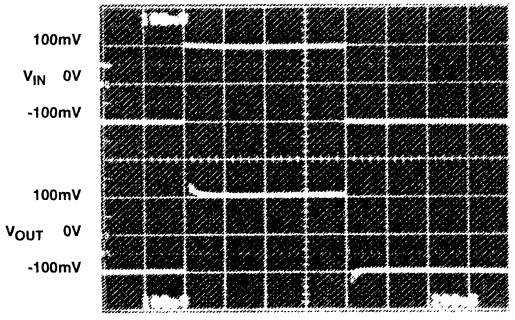


FIGURE 1. TRANSIENT RESPONSE TEST CIRCUIT



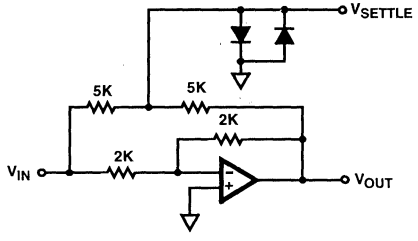
V_{OUT} = 2.5V
Vertical Scale = 2V/Div.,
Horizontal Scale = 200ns/Div.

FIGURE 2. LARGE SIGNAL RESPONSE



V_{OUT} = ±100mV
Vertical Scale = 100mV/Div.,
Horizontal Scale = 200ns/Div.

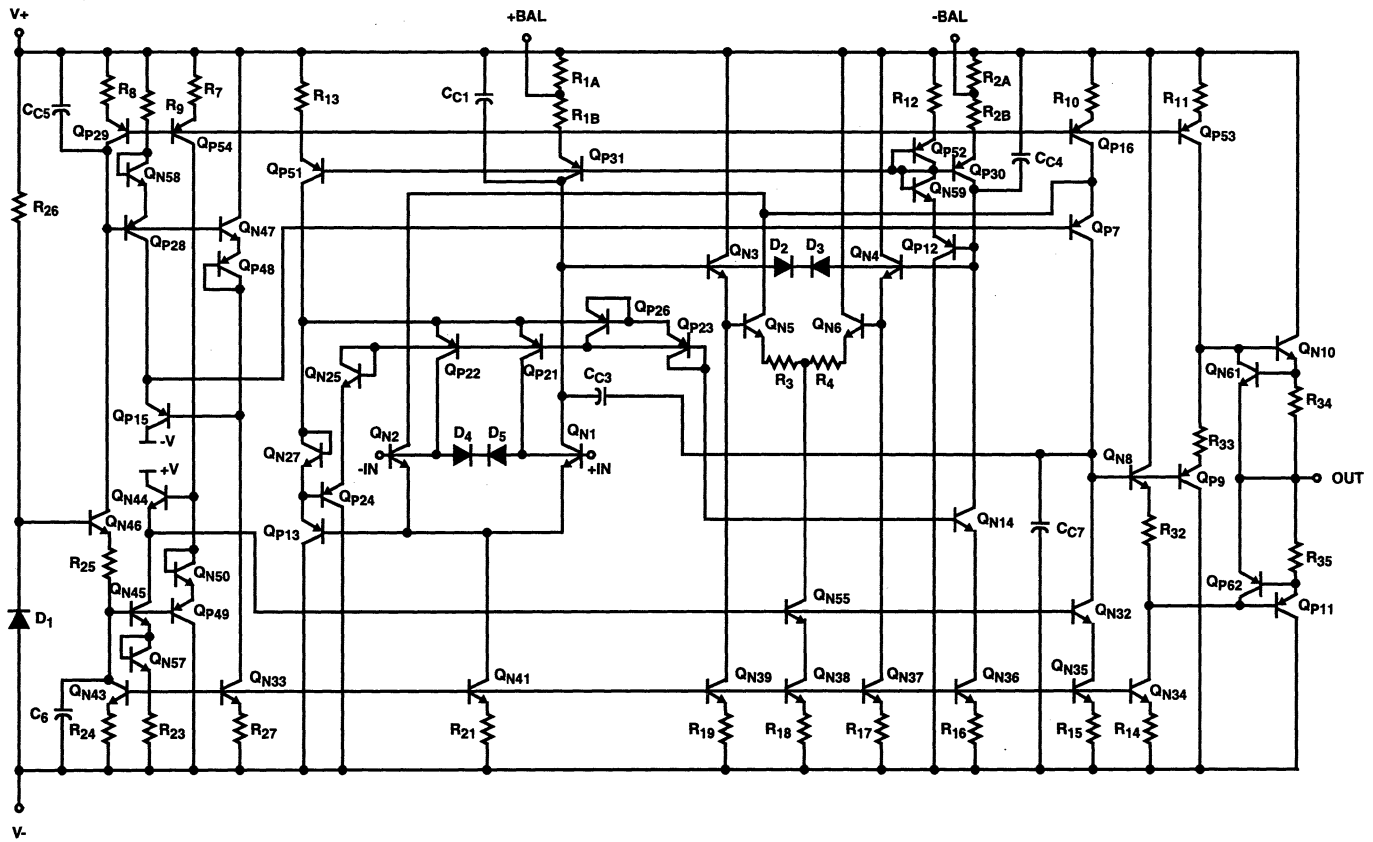
FIGURE 3. SMALL SIGNAL RESPONSE



13. AV = -1.
14. Feedback and summing resistors must be matched (0.1%).
15. HP5082-2810 clipping diodes recommended.
16. Tektronix P6201 FET probe used at settling point.

FIGURE 4. SETTLING TIME TEST CIRCUIT

Schematic Diagram



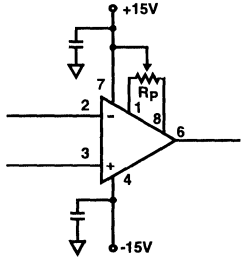
Application Information

Operation at Various Supply Voltages

The HA-5221/5222 operates over a wide range of supply voltages with little variation in performance. The supplies may be varied from ±5V to ±15V. See typical performance curves for variations in supply current, slew rate and output voltage swing.

Offset Adjustment

The following diagram shows the offset voltage adjustment configuration for the HA-5221. By moving the potentiometer wiper towards pin 8 (+BAL), the op amps output voltage will increase; towards pin 1 (-BAL) decreases the output voltage. A 20kΩ trim pot will allow an offset voltage adjustment of about 10mV.



Capacitive Loading Considerations

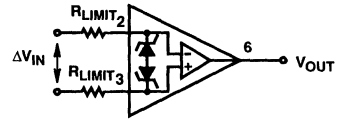
When driving capacitive loads >80pF, a small resistor, 50Ω to 100Ω, should be connected in series with the output and inside the feedback loop.

Saturation Recovery

When an op amp is over driven, output devices can saturate and sometimes take a long time to recover. By clamping the input, output saturation can be avoided. If output saturation can not be avoided, the maximum recovery time when over-driven into the positive rail is 10.6µs. When driven into the negative rail the maximum recovery time is 3.8µs.

Input Protection

The HA-5221/5222 has built in back-to-back protection diodes which limit the maximum allowable differential input voltage to approximately 5V. If the HA-5221/5222 will be used in circuits where the maximum differential voltage may be exceeded, then current limiting resistors must be used. The input current should be limited to a maximum of 10mA.



PC Board Layout Guidelines

When designing with the HA-5221 or the HA-5222, good high frequency (RF) techniques should be used when building a PC board. Use of ground plane is recommended. Power supply decoupling is very important. A 0.01µF to 0.1µF high quality ceramic capacitor at each power supply pin with a 2.2µF to 10µF tantalum close by will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and basically no lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance.

Typical Performance Curves $V_S = \pm15V, T_A = 25^oC$

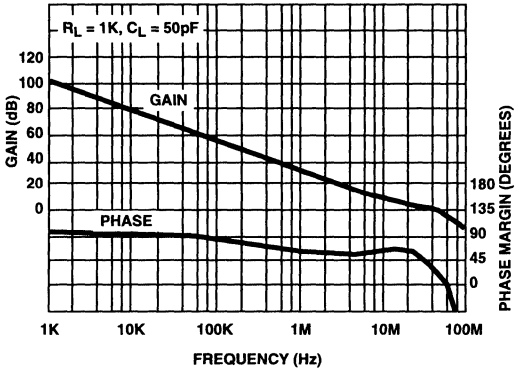


FIGURE 5. OPEN LOOP GAIN AND PHASE vs FREQUENCY

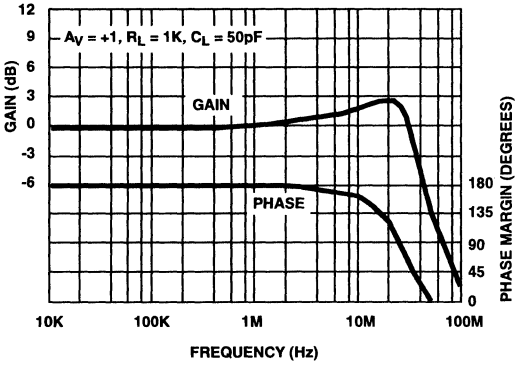


FIGURE 6. CLOSED LOOP GAIN vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$ (Continued)

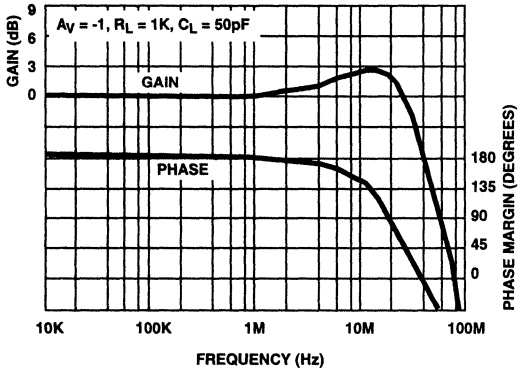


FIGURE 7. CLOSED LOOP GAIN vs FREQUENCY

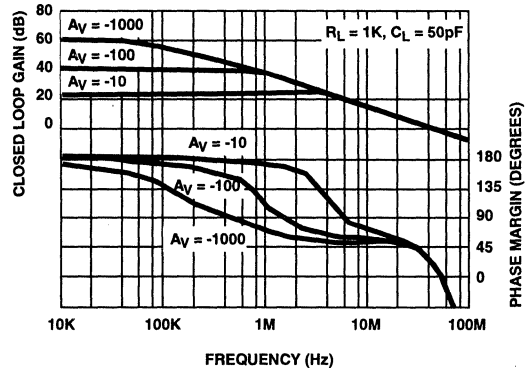


FIGURE 8. VARIOUS CLOSED LOOP GAINS vs FREQUENCY

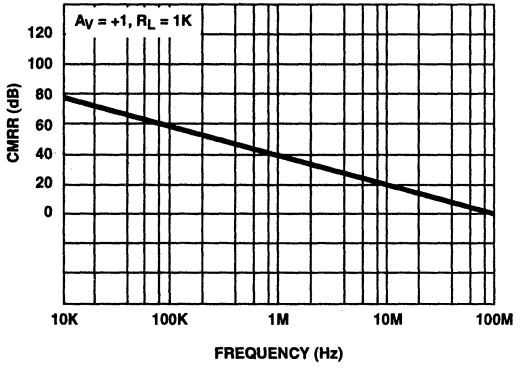


FIGURE 9. CMRR vs FREQUENCY

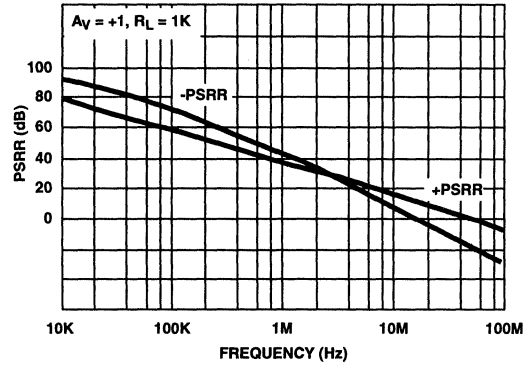


FIGURE 10. PSRR vs FREQUENCY

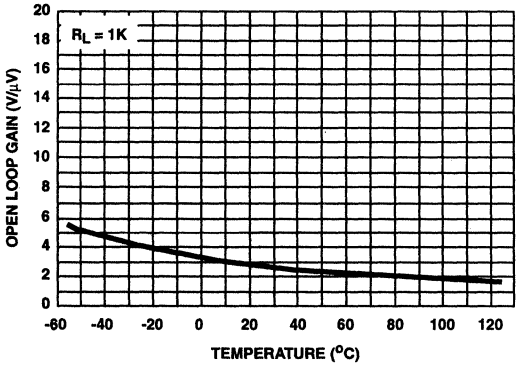


FIGURE 11. OPEN LOOP GAIN vs TEMPERATURE

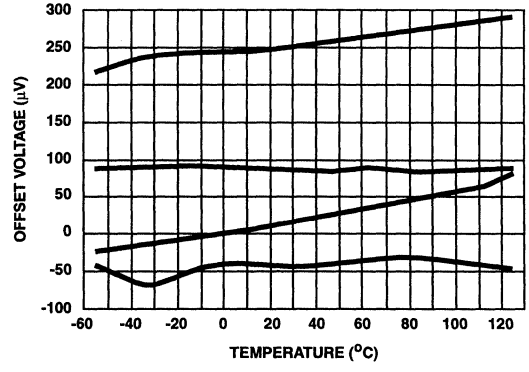


FIGURE 12. OFFSET VOLTAGE vs TEMPERATURE (4 REPRESENTATIVE UNITS)

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$ (Continued)

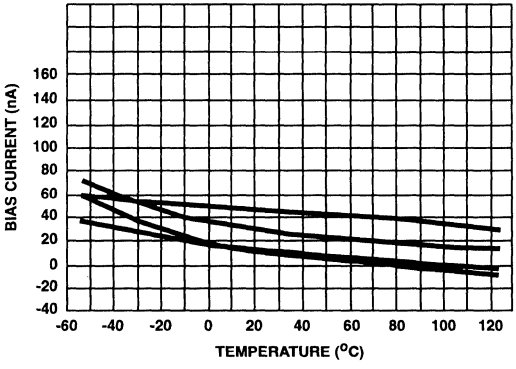


FIGURE 13. BIAS CURRENT vs TEMPERATURE (4 REPRESENTATIVE UNITS)

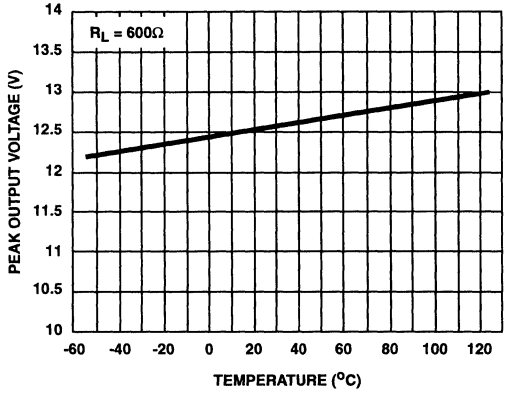


FIGURE 14. OUTPUT VOLTAGE SWING vs TEMPERATURE

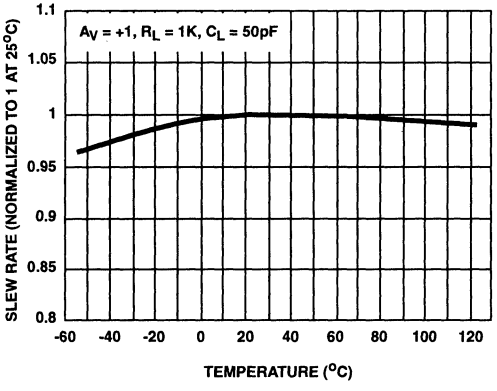


FIGURE 15. SLEW RATE vs TEMPERATURE

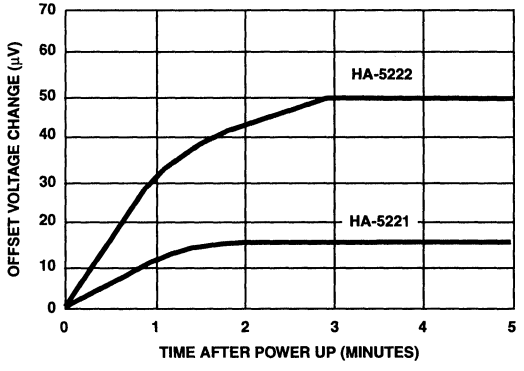


FIGURE 16. OFFSET VOLTAGE WARM-UP DRIFT (CERDIP PACKAGES)

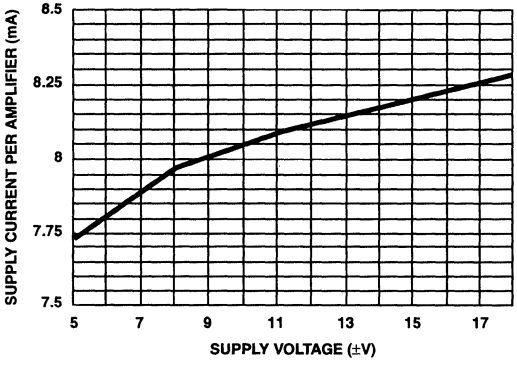


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

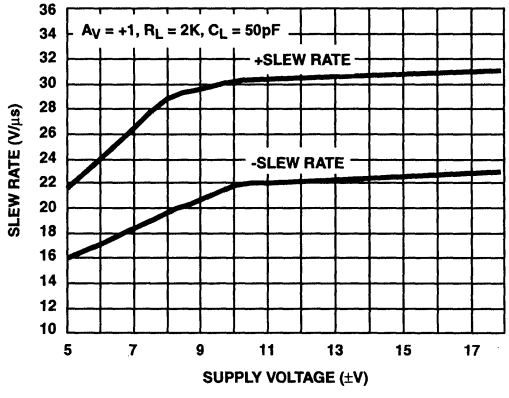


FIGURE 18. SLEW RATE vs SUPPLY VOLTAGE

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$ (Continued)

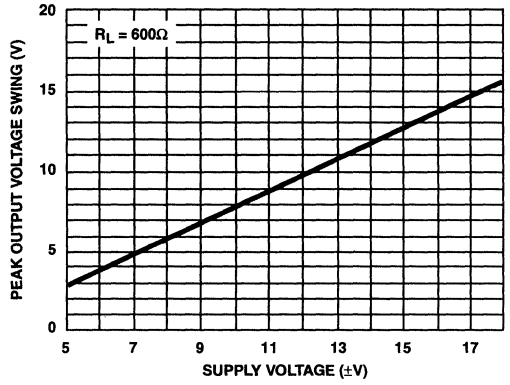


FIGURE 19. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

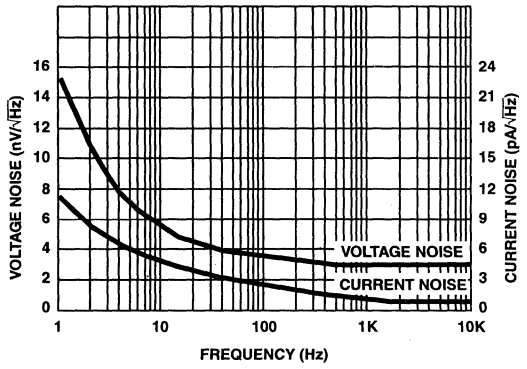


FIGURE 20. NOISE CHARACTERISTICS

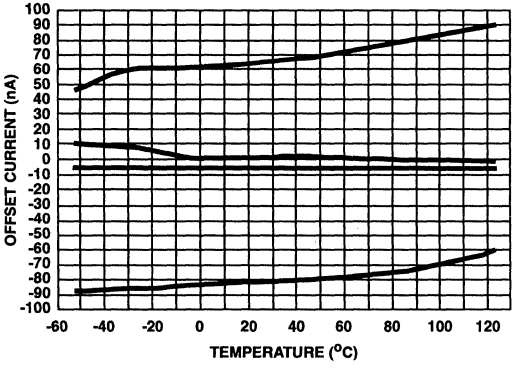


FIGURE 21. OFFSET CURRENT vs TEMPERATURE (4 REPRESENTATIVE UNITS)

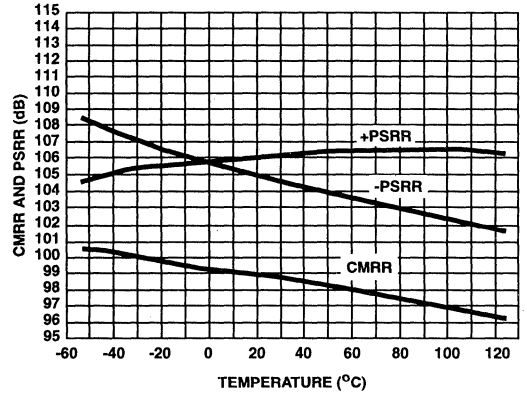


FIGURE 22. CMRR AND PSRR vs TEMPERATURE

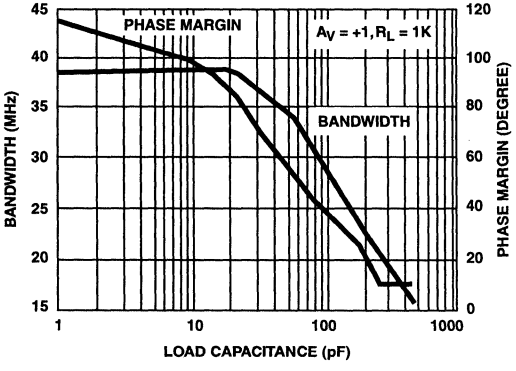


FIGURE 23. BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

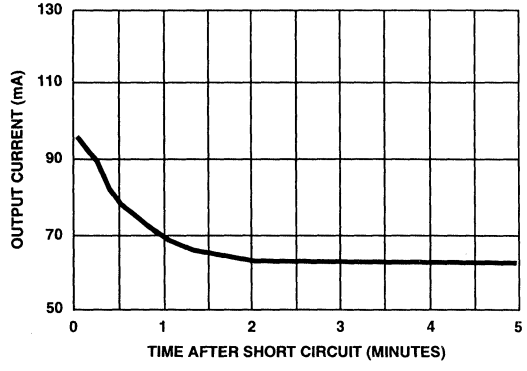
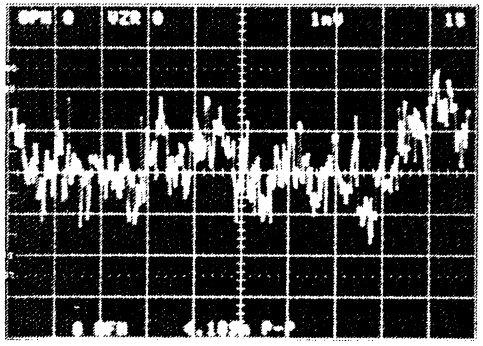


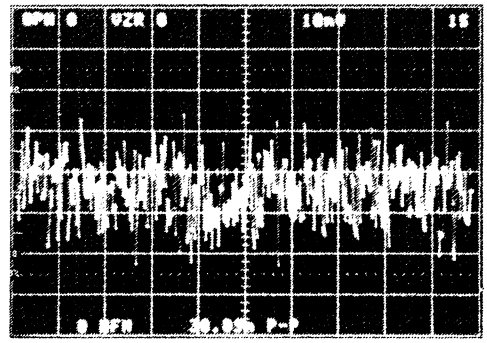
FIGURE 24. SHORT CIRCUIT OUTPUT CURRENT vs TIME

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$ (Continued)



Vertical Scale = 1mV/Div.; Horizontal Scale = 1s/Div.
A_V = +25,000; E_N = 0.168μV_{P-P} RTI

FIGURE 25. 0.1Hz TO 10Hz NOISE



Vertical Scale = 10mV/Div.; Horizontal Scale = 1s/Div.
A_V = +25,000; E_N = 1.5μV_{P-P} RTI

FIGURE 26. 0.1Hz TO 1MHz

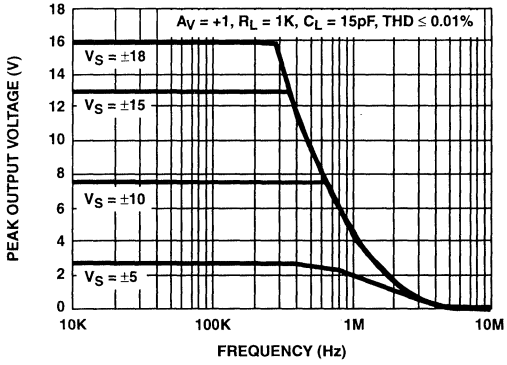


FIGURE 27. OUTPUT VOLTAGE SWING vs FREQUENCY

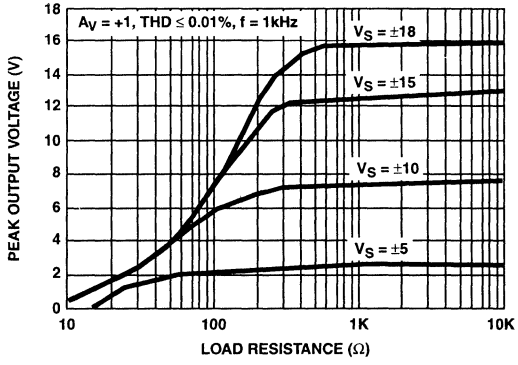


FIGURE 28. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

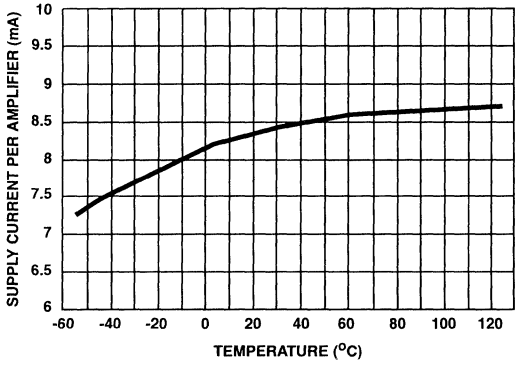


FIGURE 29. SUPPLY CURRENT/AMPLIFIER vs TEMPERATURE

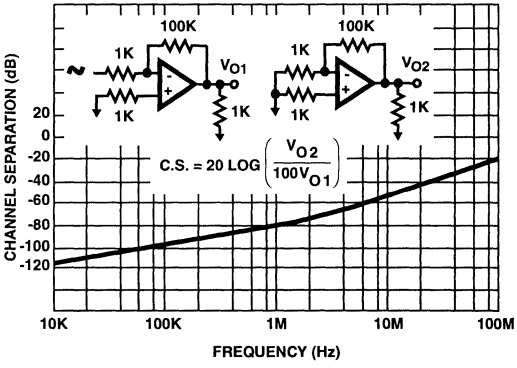


FIGURE 30. CHANNEL SEPARATION vs FREQUENCY (HA-5222 ONLY)

Die Characteristics

DIE DIMENSIONS:

72 mils x 94 mils x 19 mils
1840µm x 2400µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

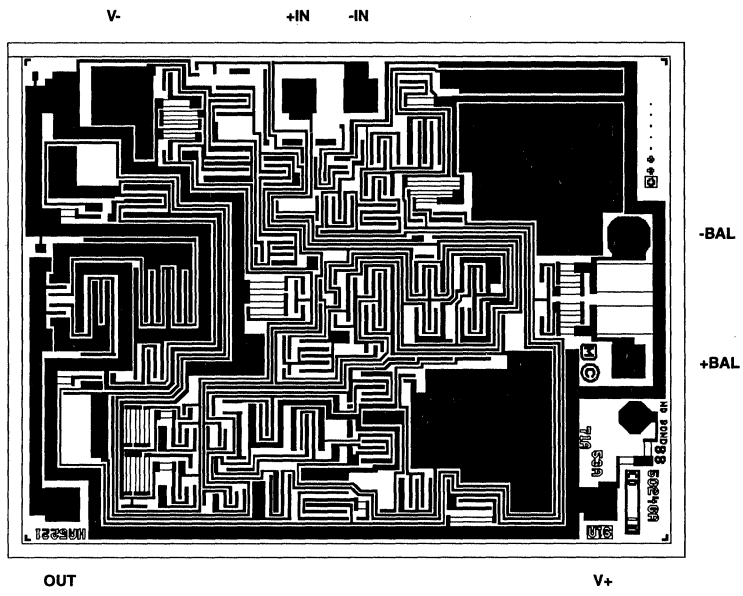
62

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5221



Die Characteristics

DIE DIMENSIONS:

78 mils x 185 mils x 19 mils
1980µm x 4690µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

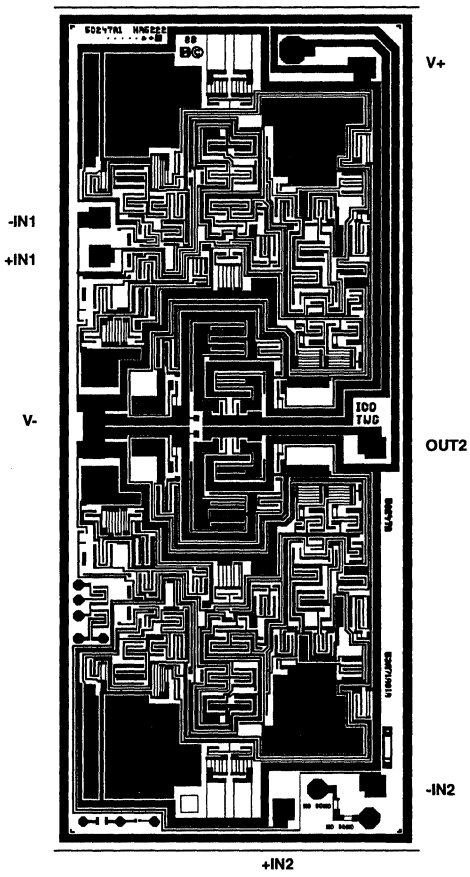
128

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5222



HFA1100, HFA1120

850MHz, Low Distortion Current Feedback Operational Amplifiers

November 1996

Features

- Low Distortion (30MHz, HD2) ..... -56dBc
- -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2300V/µs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) ..... ±0.14dB
  - (50MHz) ..... ±0.04dB
  - (30MHz) ..... ±0.01dB
- High Output Current 60mA
- Overdrive Recovery ..... <10ns

Applications

- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems
- Related Literature
  - AN9420, Current Feedback Theory
  - AN9202, HFA11XX Evaluation Fixture

Description

The HFA1100, 1120 are a family of high-speed, wideband, fast settling current feedback amplifiers. Built with Harris' proprietary complementary bipolar UHF-1 process, these devices are the fastest monolithic amplifiers available from any semiconductor manufacturer.

The HFA1100 is a basic op amp with uncommitted pins 1, 5, and 8. The HFA1120 includes inverting input bias current adjust pins (pins 1 and 5) for adjusting the output offset voltage.

These devices offer a significant performance improvement over the AD811, AD9617/18, the CLC400-409, and the EL2070, EL2073, EL2030.

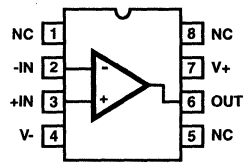
For Military grade product refer to the HFA1100/883, HFA1120/883 data sheet.

Ordering Information

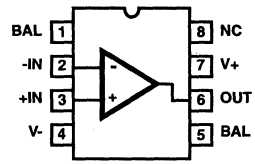
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1100MJ/883, HFA1120MJ/883	-55 to 125	8 Ld CERDIP	F8.3A
HFA1100IJ, HFA1120IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1100IP, HFA1120IP	-40 to 85	8 Ld PDIP	E8.3
HFA1100IB, HFA1120IB (H1100I, H1120I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High-Speed Op Amps		

Pinouts

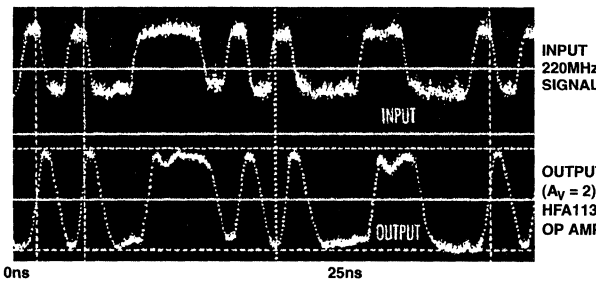
HFA1100
(PDIP, CERDIP, SOIC)
TOP VIEW



HFA1120
(PDIP, CERDIP, SOIC)
TOP VIEW



The Op Amps With Fastest Edges



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2945.5**

Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- 12V
Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	115	35
PDIP Package	130	N/A
SOIC Package	170	N/A

Maximum Junction Temperature (Die or CERDIP) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (Note 3)		A	25	-	2	6	mV
		A	Full	-	-	10	mV
Input Offset Voltage Drift		C	Full	-	10	-	$\mu V/^oC$
V_{IO} CMRR	$\Delta V_{CM} = \pm2V$	A	25	40	46	-	dB
		A	Full	38	-	-	dB
V_{IO} PSRR	$\Delta V_S = \pm1.25V$	A	25	45	50	-	dB
		A	Full	42	-	-	dB
Non-Inverting Input Bias Current (Note 3)	+IN = 0V	A	25	-	25	40	μA
		A	Full	-	-	65	μA
$+I_{BIAS}$ Drift		C	Full	-	40	-	$nA/^oC$
$+I_{BIAS}$ CMS	$\Delta V_{CM} = \pm2V$	A	25	-	20	40	$\mu A/V$
		A	Full	-	-	50	$\mu A/V$
Inverting Input Bias Current (Note 3)	-IN = 0V	A	25	-	12	50	μA
		A	Full	-	-	60	μA
$-I_{BIAS}$ Drift		C	Full	-	40	-	$nA/^oC$
$-I_{BIAS}$ CMS	$\Delta V_{CM} = \pm2V$	A	25	-	1	7	$\mu A/V$
		A	Full	-	-	10	$\mu A/V$
$-I_{BIAS}$ PSS	$\Delta V_S = \pm1.25V$	A	25	-	6	15	$\mu A/V$
		A	Full	-	-	27	$\mu A/V$
$-I_{BIAS}$ Adj. Range (HFA1120)		A	25	±100	±200	-	μA
Non-Inverting Input Resistance		A	25	25	50	-	$k\Omega$
Inverting Input Resistance		C	25	-	20	30	Ω
Input Capacitance (Either Input)		B	25	-	2	-	pF
Input Common Mode Range		C	Full	±2.5	±3.0	-	V
Input Noise Voltage (Note 3)	100kHz	B	25	-	4	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 3)	100kHz	B	25	-	18	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 3)	100kHz	B	25	-	21	-	$pA/\sqrt{Hz}$

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified							
Open Loop Transimpedance (Note 3)		B	25	-	300	-	kΩ
-3dB Bandwidth (Note 3)	$V_{OUT} = 0.2V_{P-P}$, $A_V = +1$	B	25	530	850	-	MHz
-3dB Bandwidth	$V_{OUT} = 0.2V_{P-P}$, $A_V = +2$, $R_F = 360\Omega$	B	25	-	670	-	MHz
Full Power Bandwidth	$V_{OUT} = 4V_{P-P}$, $A_V = -1$	B	25	-	300	-	MHz
Gain Flatness (Note 3)	To 100MHz	B	25	-	±0.14	-	dB
Gain Flatness	To 50MHz	B	25	-	±0.04	-	dB
Gain Flatness	To 30MHz	B	25	-	±0.01	-	dB
Linear Phase Deviation (Note 3)	DC to 100MHz	B	25	-	0.6	-	Degrees
Differential Gain	NTSC, $R_L = 75\Omega$	B	25	-	0.03	-	%
Differential Phase	NTSC, $R_L = 75\Omega$	B	25	-	0.05	-	Degrees
Minimum Stable Gain		A	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified							
Output Voltage (Note 3)	$A_V = -1$	A	25	±3.0	±3.3	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	$R_L = 50\Omega$, $A_V = -1$	A	25, 85	50	60	-	mA
		A	-40	35	50	-	mA
DC Closed Loop Output Impedance (Note 3)		B	25	-	0.07	-	Ω
2nd Harmonic Distortion (Note 3)	30MHz, $V_{OUT} = 2V_{P-P}$	B	25	-	-56	-	dBc
3rd Harmonic Distortion (Note 3)	30MHz, $V_{OUT} = 2V_{P-P}$	B	25	-	-80	-	dBc
3rd Order Intercept (Note 3)	100MHz	B	25	20	30	-	dBm
1dB Compression	100MHz	B	25	15	20	-	dBm
TRANSIENT RESPONSE $A_V = +2$, Unless Otherwise Specified							
Rise Time	$V_{OUT} = 2.0V$ Step	B	25	-	900	-	ps
Overshoot (Note 3)	$V_{OUT} = 2.0V$ Step	B	25	-	10	-	%
Slew Rate	$A_V = +1$, $V_{OUT} = 5V_{P-P}$	B	25	-	1400	-	V/µs
Slew Rate	$A_V = +2$, $V_{OUT} = 5V_{P-P}$	B	25	1850	2300	-	V/µs
0.1% Settling (Note 3)	$V_{OUT} = 2V$ to 0V	B	25	-	11	-	ns
0.2% Settling (Note 3)	$V_{OUT} = 2V$ to 0V	B	25	-	7	-	ns
Overdrive Recovery Time	2X Overdrive	B	25	-	7.5	10	ns
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		B	Full	±4.5	-	±5.5	V
Supply Current (Note 3)		A	25	-	21	26	mA
		A	Full	-	-	33	mA

NOTES:

2. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
3. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor (R_F)

The enclosed plots of inverting and non-inverting frequency response detail the performance of the HFA1100/1120 in various gains. Although the bandwidth dependency on A_{CL} isn't as severe as that of a voltage feedback amplifier, there is an appreciable decrease in bandwidth at higher gains. This decrease can be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and the R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1100, 1120 designs are optimized for a 510Ω R_F, at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth. The table below lists recommended R_F values for various gains, and the expected bandwidth.

A_{CL}	R_F (Ω)	BW (MHz)
+1	510	850
-1	430	580
+2	360	670
+5	150	520
+10	180	240
+19	270	125

Offset Adjustment

The HFA1120 allows for adjustment of the inverting input bias current to null the output offset voltage. $-I_{BIAS}$ flows through R_F, so any change in bias current forces a corresponding change in output voltage. The amount of adjustment is a function of R_F. With R_F = 510Ω, the typical adjust range is ±100mV. For offset adjustment connect a 10kΩ potentiometer between pins 1 and 5 with the wiper connected to V-.

Use of Die in Hybrid Applications

These amplifiers are designed with compensation to negate the package parasitics that typically lead to instabilities. As a result, the use of die in hybrid applications results in overcompensated performance due to lower parasitic capacitances. Reducing R_F below the recommended values for packaged units will solve the problem. For A_V = +2 the recommended starting point is 300Ω, while unity gain applications should try 400Ω.

PC Board Layout

The frequency performance of these amplifiers depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

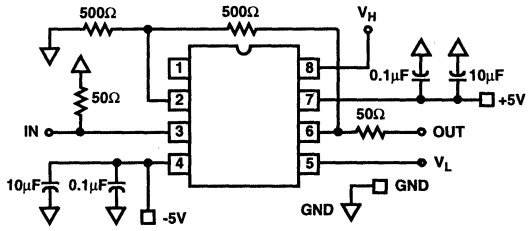
Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown below.

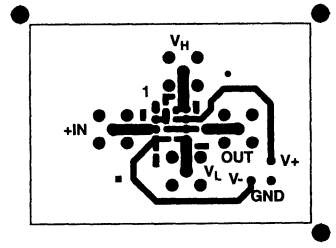
Evaluation Board

An evaluation board is available for the HFA1100 (Part Number HFA11XXEVAL). Please contact your local sales office for information.

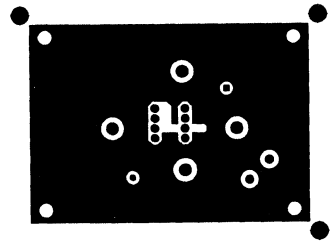
The layout and schematic of the board are shown below:



TOP LAYOUT



BOTTOM LAYOUT



Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

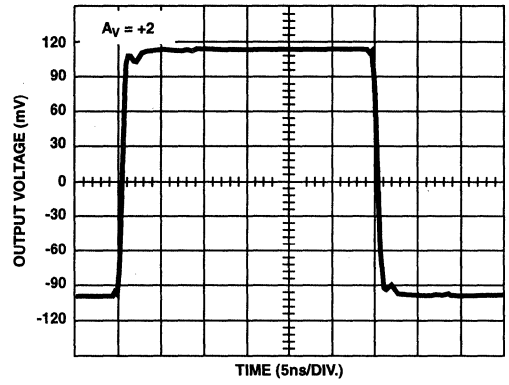


FIGURE 1. SMALL SIGNAL PULSE

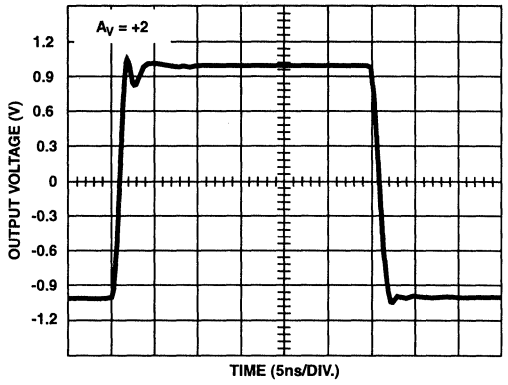


FIGURE 2. LARGE SIGNAL PULSE

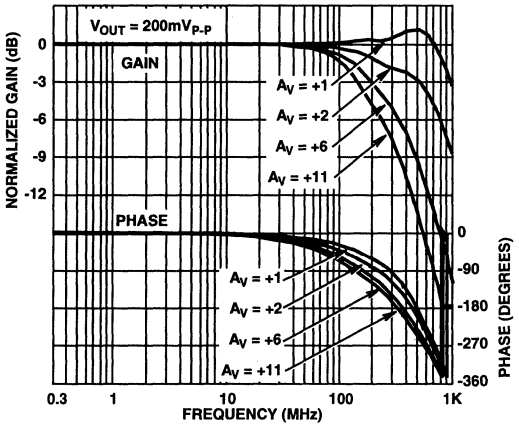


FIGURE 3. NON-INVERTING FREQUENCY RESPONSE

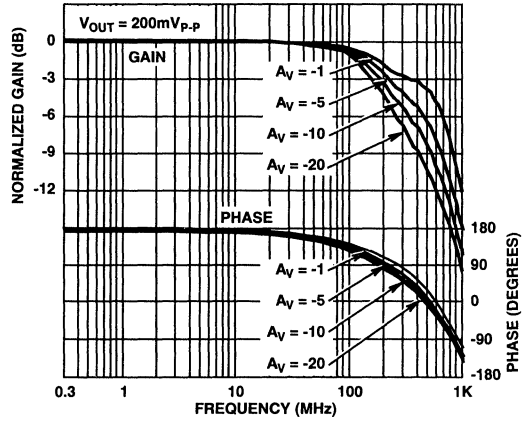


FIGURE 4. INVERTING FREQUENCY RESPONSE

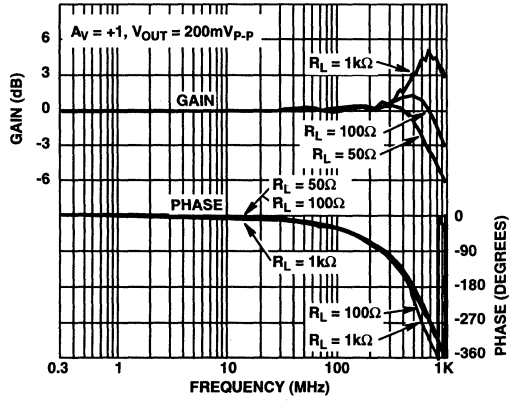


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

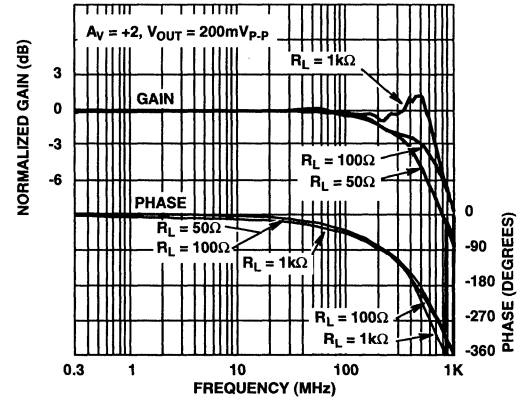


FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

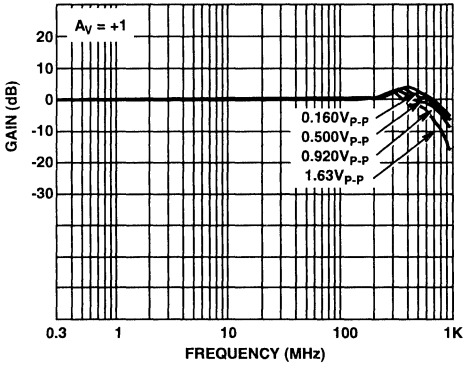


FIGURE 7. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

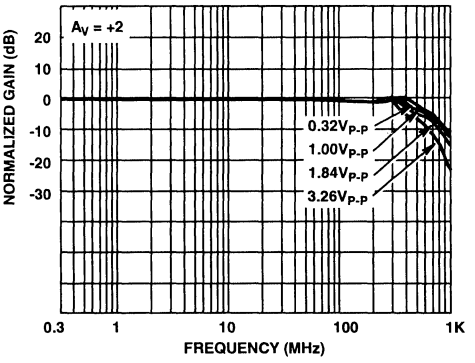


FIGURE 8. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

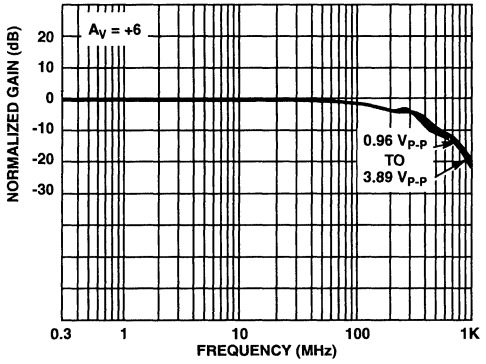


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

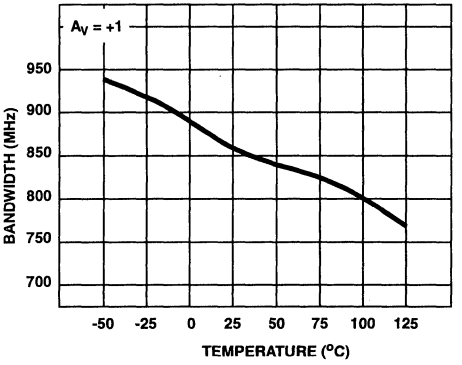


FIGURE 10. -3dB BANDWIDTH vs TEMPERATURE

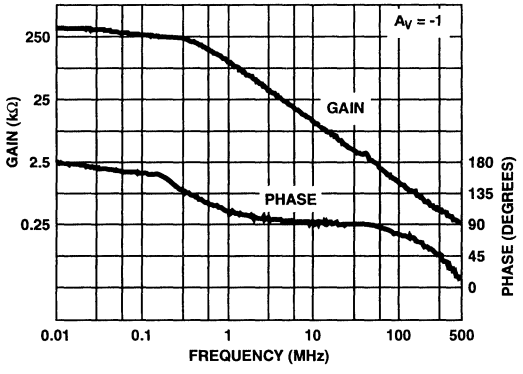


FIGURE 11. OPEN LOOP TRANSIMPEDANCE

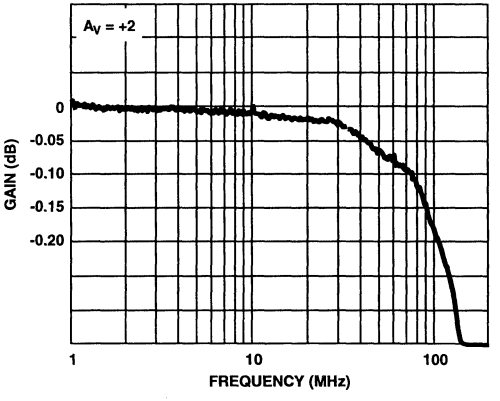


FIGURE 12. GAIN FLATNESS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

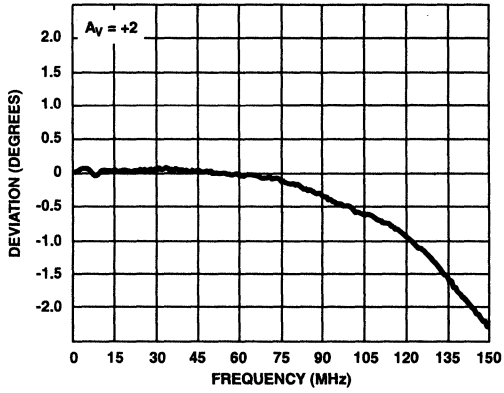


FIGURE 13. DEVIATION FROM LINEAR PHASE

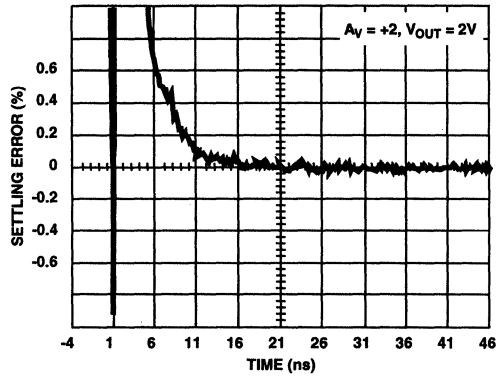


FIGURE 14. SETTLING RESPONSE

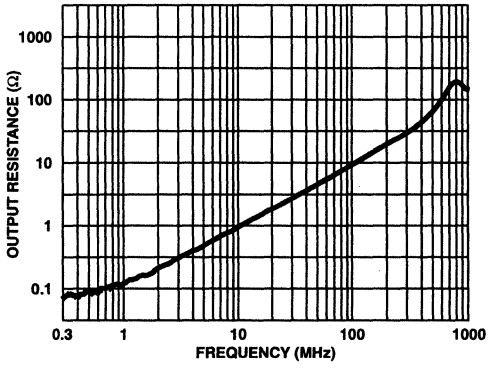


FIGURE 15. CLOSED LOOP OUTPUT RESISTANCE

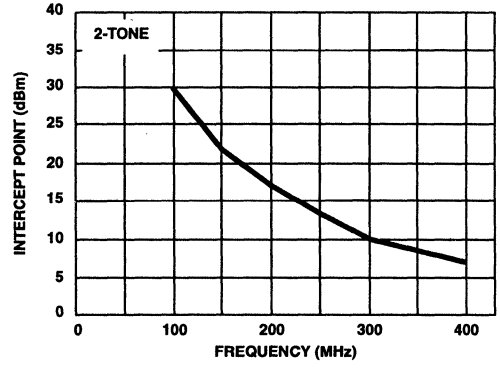


FIGURE 16. 3rd ORDER INTERMODULATION INTERCEPT

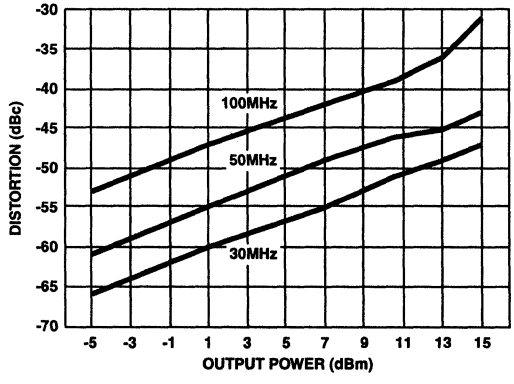


FIGURE 17. 2nd HARMONIC DISTORTION vs P_{OUT}

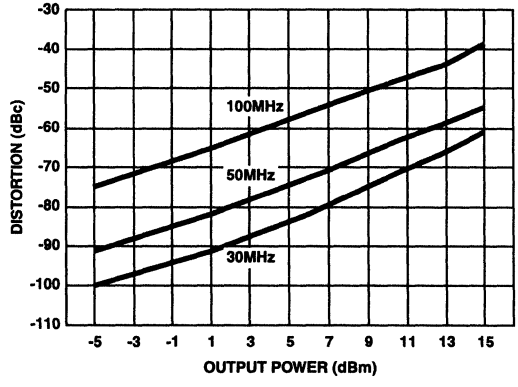


FIGURE 18. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

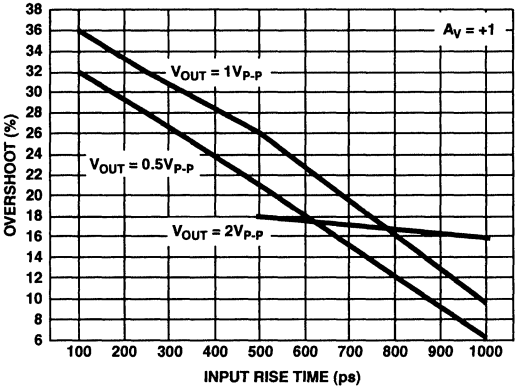


FIGURE 19. OVERSHOOT vs INPUT RISE TIME

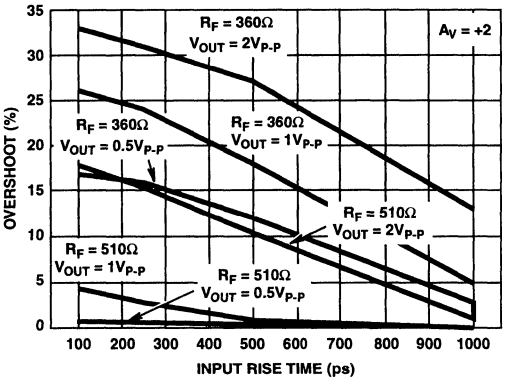


FIGURE 20. OVERSHOOT vs INPUT RISE TIME

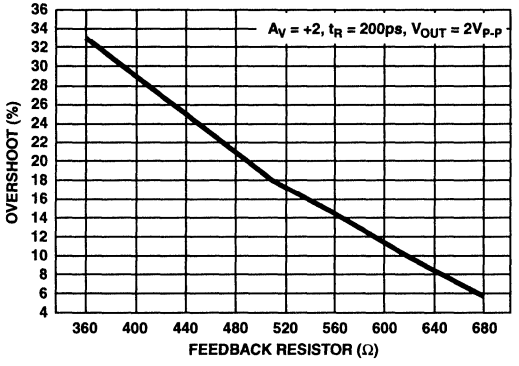


FIGURE 21. OVERSHOOT vs FEEDBACK RESISTOR

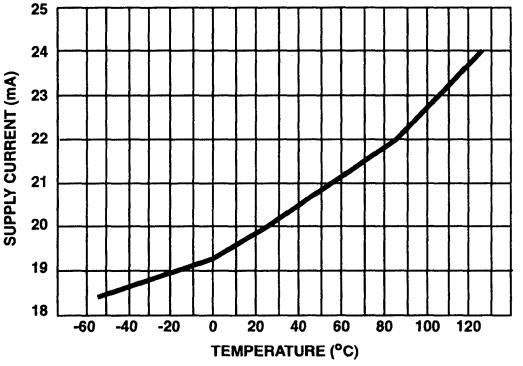


FIGURE 22. SUPPLY CURRENT vs TEMPERATURE

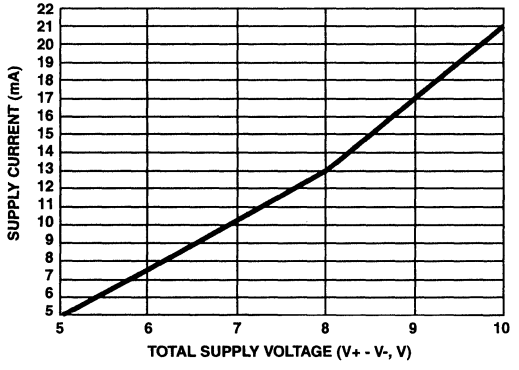


FIGURE 23. SUPPLY CURRENT vs SUPPLY VOLTAGE

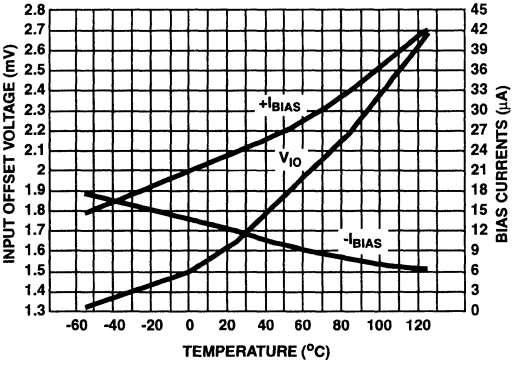


FIGURE 24. V_{IO} AND BIAS CURRENTS vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

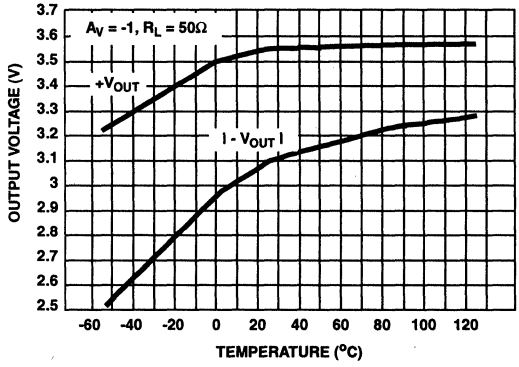


FIGURE 25. OUTPUT VOLTAGE vs TEMPERATURE

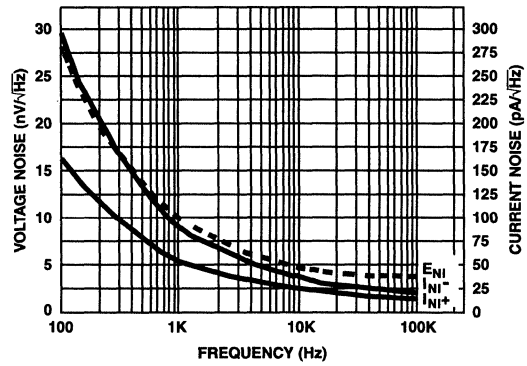


FIGURE 26. INPUT NOISE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

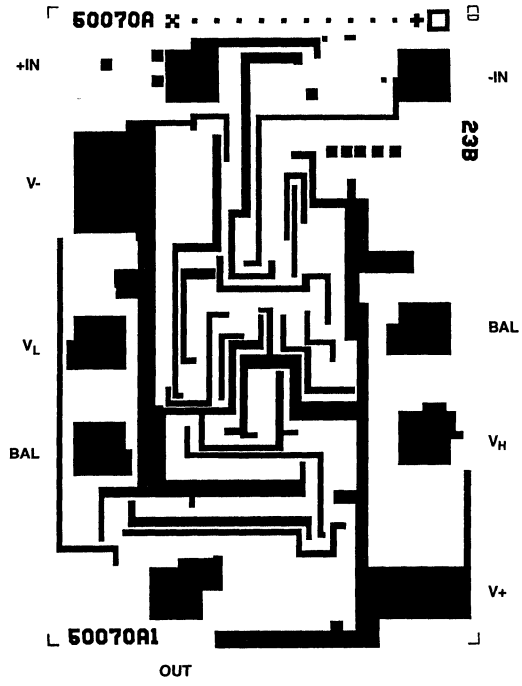
52

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1100, HFA1120



HARRIS SEMICONDUCTOR

HFA1102

600MHz Current Feedback Amplifier with Compensation Pin

November 1996

Features

- Compensation Pin for Bandwidth Limiting
- Low Distortion (HD2 at 30MHz) ..... -56dBc
- -3dB Bandwidth 600MHz
- Very Fast Slew Rate 2000V/µs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) ..... ±0.05dB
  - (50MHz) ..... ±0.02dB
  - (30MHz) ..... ±0.01dB
- High Output Current 60mA
- Overdrive Recovery ..... <10ns

Applications

- Low Noise Amplifiers
- Video Switching and Routing
- Pulse and Video Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems

Description

The HFA1102 is a high speed wideband current feedback amplifier featuring a compensation pin for bandwidth limiting. Built with Harris' proprietary complementary bipolar UHF-1 process, it has excellent AC performance and low distortion.

Because the HFA1102 is already unity gain stable, the primary purpose for limiting the bandwidth is to reduce the total noise (broadband) of the circuit. The bandwidth of the HFA1102 may be limited by connecting a capacitor and series damping resistor from pin 8 to ground. Typical bandwidths for various values of compensation capacitors are shown in the Electrical Specifications section of this datasheet.

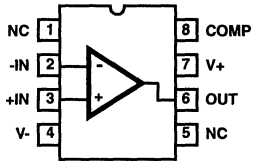
A variety of packages and temperature grades are available. See the ordering information below for details.

Ordering Information

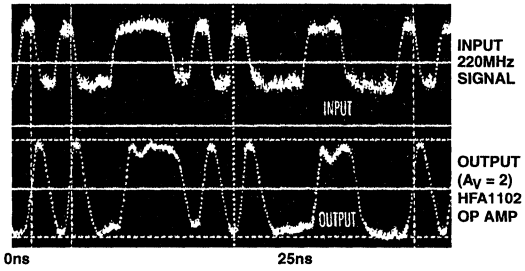
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1102IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1102IP	-40 to 85	8 Ld PDIP	E8.3
HFA1102IB (HI102I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1102
(PDIP, CERDIP, SOIC)
TOP VIEW



The Op Amps with Fastest Edges



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3597.2**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA

Operating Conditions

Temperature Range ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	120	35
PDIP Package	130	N/A
SOIC Package	170	N/A

Maximum Junction Temperature (Ceramic Package and Die) ..175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, C_{COMP} = 0pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage		25	-	2	6	mV
		Full	-	-	10	mV
Input Offset Voltage Drift		Full	-	10	-	µV/°C
V_{IO} CMRR	ΔV_{CM} = ±2V	25	40	46	-	dB
		Full	38	-	-	dB
V_{IO} PSRR	ΔV_S = ±1.25V	25	45	50	-	dB
		Full	42	-	-	dB
Non-Inv. Input Bias Current	+IN = 0V	25	-	25	40	µA
		Full	-	-	65	µA
$+I_{BIAS}$ Drift		Full	-	40	-	nA/°C
$+I_{BIAS}$ CMS	ΔV_{CM} = ±2V	25	-	20	40	µA/V
		Full	-	-	50	µA/V
Inv. Input Bias Current	-IN = 0V	25	-	12	50	µA
		Full	-	-	60	µA
$-I_{BIAS}$ Drift		Full	-	40	-	nA/°C
$-I_{BIAS}$ CMS	ΔV_{CM} = ±2V	25	-	1	7	µA/V
		Full	-	-	10	µA/V
$-I_{BIAS}$ PSS	ΔV_S = ±1.25V	25	-	6	15	µA/V
		Full	-	-	27	µA/V
Non-Inv. Input Resistance		25	25	50	-	kΩ
Inv. Input Resistance		25	-	16	30	Ω
Input Capacitance	Either Input	25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±3.0	-	V
Input Noise Voltage	100kHz	25	-	4	-	$nV/\sqrt{Hz}$
+Input Noise Current	100kHz	25	-	18	-	$pA/\sqrt{Hz}$
-Input Noise Current	100kHz	25	-	21	-	$pA/\sqrt{Hz}$

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, $C_{COMP} = 0pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS $A_V = +1$, $R_F = 150\Omega$, $R_{DAMP} = 120\Omega$, Unless Otherwise Specified						
Open Loop Transimpedance		25	-	500	-	kΩ
Linear Phase Deviation	DC to 100MHz	25	-	0.6	-	Degrees
Differential Gain	NTSC, $R_L = 75\Omega$	25	-	0.03	-	%
Differential Phase	NTSC, $R_L = 75\Omega$	25	-	0.03	-	Degrees
Minimum Stable Gain		Full	1	-	-	V/V
Bandwidth Limiting Characteristics -3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, $A_V = +1$)	$C_{COMP} = 0pF$	25	-	600	-	MHz
	$C_{COMP} = 1pF$	25	-	350	-	MHz
	$C_{COMP} = 3pF$	25	-	190	-	MHz
	$C_{COMP} = 7pF$	25	-	55	-	MHz
Gain Flatness (To 30MHz)	$C_{COMP} = 0pF$	25	-	±0.01	-	dB
	$C_{COMP} = 1pF$	25	-	±0.05	-	dB
	$C_{COMP} = 3pF$	25	-	±0.10	-	dB
Gain Flatness	To 100MHz	25	-	±0.05	-	dB
Gain Flatness	To 50MHz	25	-	±0.02	-	dB
OUTPUT CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified						
Output Voltage	$A_V = -1$	25	±3.0	±3.3	-	V
		Full	±2.5	±3.0	-	V
Output Current	$R_L = 50\Omega$, $A_V = -1$	25	50	65	-	mA
		Full	40	60	-	mA
Closed Loop Output Impedance	DC	25	-	0.1	-	Ω
2nd Harmonic Distortion	30MHz, $V_{OUT} = 2V_{P-P}$	25	-	-56	-	dBc
3rd Harmonic Distortion	30MHz, $V_{OUT} = 2V_{P-P}$	25	-	-80	-	dBc
3rd Order Intercept	100MHz	25	-	30	-	dBm
1dB Compression	100MHz	25	-	20	-	dBm
TRANSIENT RESPONSE $A_V = +1$, $R_F = 150\Omega$, $R_{DAMP} = 120\Omega$, Unless Otherwise Specified						
Rise Time	$V_{OUT} = 2.0V$ Step	25	-	600	-	ps
Overshoot	$V_{OUT} = 2.0V$ Step	25	-	10	-	%
Slew Rate	$A_V = +1$, $V_{OUT} = 5V_{P-P}$	25	-	1200	-	V/µs
	$A_V = +2$, $V_{OUT} = 5V_{P-P}$	25	-	2000	-	V/µs
0.1% Settling Time	$V_{OUT} = 2V$ to 0V	25	-	11	-	ns
0.2% Settling Time	$V_{OUT} = 2V$ to 0V	25	-	7	-	ns
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current		25	-	21	26	mA
		Full	-	-	33	mA

Application Information

Optimum Feedback Resistor (R_F)

All current feedback amplifiers require a feedback resistor, even for unity gain applications. The R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1102 design is optimized for a 150Ω R_F, at a gain of +1. Decreasing R_F in a unity gain application decreases stability, leading to excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

Bandwidth Limiting

The bandwidth of the HFA1102 may be limited by connecting a resistor (R_{DAMP}) and capacitor in series from pin 8 to GND. The series resister is required to damp the interaction between the package parasitics and C_{COMP}. Typical bandwidths for various values of compensation capacitor are shown in the specification tables. Because the HFA1102 is already unity gain stable, the main reason for limiting the bandwidth is to reduce the total noise (broadband) of the circuit. Additionally, compensating the HFA1102 allows the use of a lower value R_F for a given gain. The decreased bandwidth due to C_{COMP} offsets the bandwidth increase from the lower R_F, keeping the amplifier stable. Reducing R_F provides the double benefits of reduced DC errors ($-I_B \times R_F$) and reduced total noise ($I_{NI} \times R_F$ and $4KTR_F$).

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

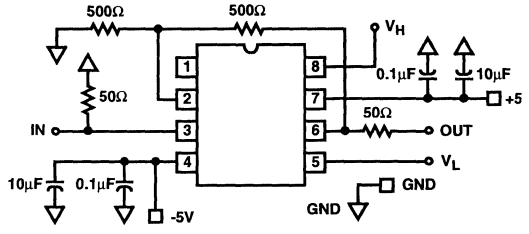
Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

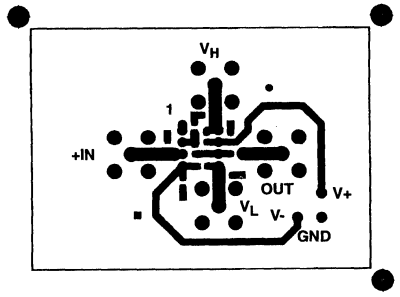
An example of a good high frequency layout is the Evaluation Board shown.

Evaluation Board

The HFA1102 may be evaluated using the HFA11XX Evaluation Board which is available from your local sales office (part number HFA11XXEVAL). R_{DAMP} and C_{COMP} should be connected in series from the socket pin to the GND plane. The trace from pin 8 to the V_H connector should be cut near the socket to remove this parallel capacitance.The layout and schematic of the board are shown below:



TOP LAYOUT



BOTTOM LAYOUT

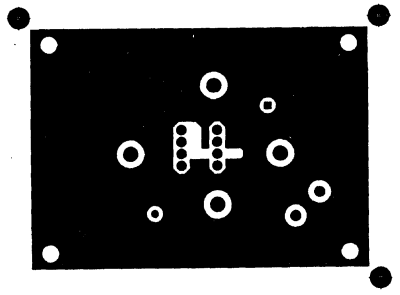


FIGURE 1. EVALUATION BOARD SCHEMATIC AND LAYOUT

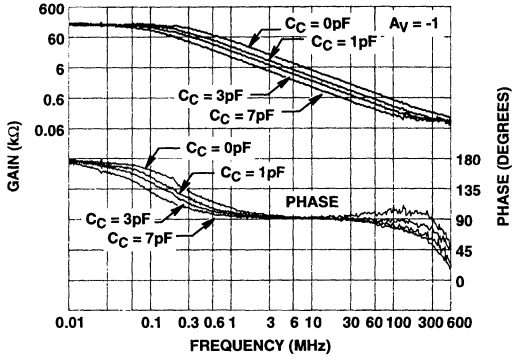


FIGURE 2. OPEN LOOP TRANSIMPEDANCE FOR VARIOUS COMPENSATION CAPACITORS

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

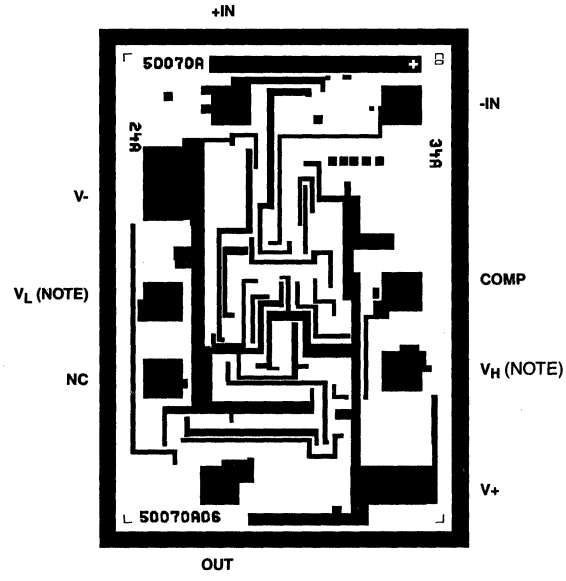
52

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1102



NOTE: Output Limiting Function (V_H, V_L) is available to users of the HFA1102 in die form. Please refer to the HFA1130 data sheet for information regarding the operation and use of this function.

HARRIS SEMICONDUCTOR

HFA1103

200MHz, Video Op Amp with High Speed Sync Stripper

November 1996

Features

- Removes Sync Signal From Component Video
- Low Residual Sync ..... 8mV (Typ)
- -3dB Bandwidth 200MHz
- Very Fast Slew Rate 600V/µs
- Fast Settling Time (0.1%) 9ns
- Excellent Gain Flatness, 32MHz ..... ±0.1dB
- Overdrive Recovery ..... <12ns

Applications

- RGB Video Sync Stripping
- RGB Video Distribution Amplifier for Workstations and PC Networks
- Video Conferencing Systems
- RGB Video Monitor Preamp
- Fiberoptic Receivers

Description

The HFA1103 is a high-speed, wideband, fast settling current feedback op amp with a sync stripping function. The HFA1103 is a basic op amp with a modified output stage that enables it to strip the sync from a component video signal. The output stage has an open emitter NPN transistor that prevents the output from going low during the sync pulse. Removing the sync signal benefits digitizing systems because only the active video information is applied to the A/D converter. This enables the full dynamic range of the A/D converter to be used to process the video signal. The HFA1103 includes inverting input bias current adjust pins (pins 1 and 5) for adjusting the output offset voltage.

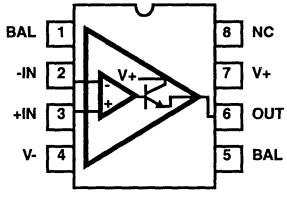
Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1103IP	-40 to 85	8 Ld PDIP	E8.3
HFA1103IB (H1103I)	-40 to 85	8 Ld SOIC	M8.15

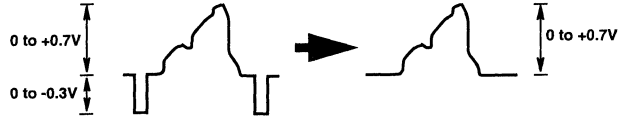
3 OPERATIONAL AMPLIFIERS

Pinout

HFA1103
(PDIP, SOIC)
TOP VIEW



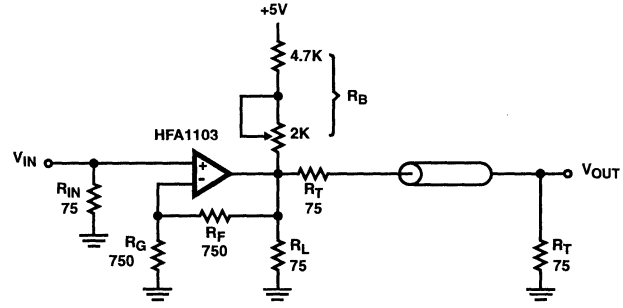
Sync Stripper Waveforms



COMPONENT (RGB) VIDEO INPUT

HFA1103 OUTPUT

Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 3957.2

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA

Operating Conditions

Temperature Range ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +2$, $R_F = 750\Omega$, $R_L = 50\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Residual Sync (Note 2)	$V_{IN} = -300mV$, $A_V = +1$	25	-	8	10	mV
		Full	-	-	12	mV
Output Offset Voltage (Notes 3, 5)		25	-	10	30	mV
		Full	-	-	40	mV
Output Offset Voltage Drift (Note 3)		Full	-	10	-	µV/°C
V_{OS} PSRR	$\Delta V_S = \pm1.25V$	25	39	45	-	dB
		Full	35	-	-	dB
Non-Inverting Input Bias Current	+IN = 0V	25	-	5	40	µA
		Full	-	-	65	µA
Inverting Input Bias Current	-IN = 0V	25	-	5	50	µA
		Full	-	-	60	µA
$-I_{BIAS}$ Adjust Range (Notes 4, 6)		25	100	200	-	µA
Non-Inverting Input Resistance		25	25	50	-	kΩ
Inverting Input Resistance		25	-	16	30	Ω
Input Capacitance		25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±3.0	-	V
Input Noise Voltage	100kHz	25	-	4	-	$nV/\sqrt{Hz}$
+Input Noise Current	100kHz	25	-	18	-	$pA/\sqrt{Hz}$
-Input Noise Current	100kHz	25	-	21	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified						
Open Loop Transimpedance		25	-	500	-	kΩ
-3dB Bandwidth	$V_{OUT} = 1.0V_{P-P}$, $A_V = +2$	25	-	200	-	MHz
Gain Flatness	To ±0.1dB	25	-	32	-	MHz
Minimum Stable Gain		Full	1	-	-	V/V
OUTPUT CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified						
Output Voltage (Note 3)		25, 85	2.5	3.0	-	V
		-40°C	1.75	2.5	-	V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +2, R_F = 750Ω, R_L = 50Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
Output Current		25, 85	50	60	-	mA
		-40°C	35	50	-	mA
Linearity Near Zero		25	-	0.01	-	%
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified						
Rise Time	V_{OUT} = 2.0V Step	25	-	2	-	ns
Overshoot	V_{OUT} = 2.0V Step	25	-	10	-	%
Slew Rate	A_V = +2, V_{OUT} = 0 to 2V, +2V to 0V	25	-	600	-	V/µs
0.1% Settling	V_{OUT} = 2V to 0V	25	-	9	-	ns
Overdrive Recovery Time	2X Overdrive	25	-	12	-	ns
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current (No Load)		25	-	11	16	mA
		Full	-	-	23	mA

NOTES:

2. The residual sync is specified at the output of a doubly terminated circuit (see page 1 of this data sheet).
3. Since the HFA1103 has an open emitter NPN output stage, this measurement is only valid for positive values.
4. The $-I_{BIAS}$ current can be used to adjust the offset voltage to zero, but $-I_{BIAS}$ does not flow bidirectionally because the HFA1103 output stage is an open emitter NPN transistor.
5. V_{OS} includes the error contribution of I_{BSN} at R_F = 750Ω.
6. This is the minimum change in inverting input bias current when a BAL pin is connected to V- through a 50Ω resistor.

Test Circuit

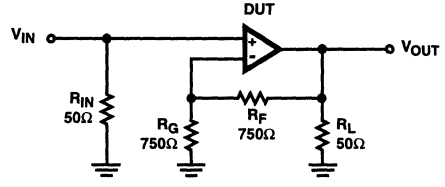


FIGURE 1. TEST CIRCUIT

Application Information

Offset Adjustment

The HFA1103 allows for adjustment of the inverting input bias current to null the output offset voltage. $-I_{BIAS}$ flows through R_F, so any change in bias current forces a corresponding change in output voltage. The amount of adjustment is a function of R_F. With R_F = 750Ω, the typical adjust range is 150mV. For offset adjustment connect a 10kΩ potentiometer between pins 1 and 5 with the wiper connected to V-.

PC Board Layout

The frequency performance of these amplifiers depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Evaluation Board

The HFA1100 series evaluation board may be used for the HFA1103 with minor modifications. The evaluation board may be ordered using part number HFA11XXEVAL. Please note that an HFA1103 sample is not included with the evaluation board and must be ordered separately.

The layout and schematic of the board are shown below:

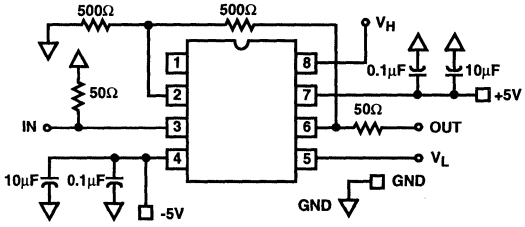
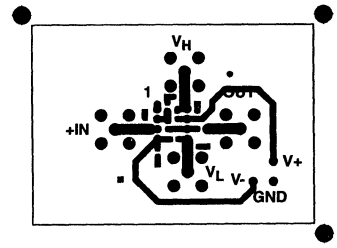


FIGURE 2. EVALUATION BOARD SCHEMATIC

TOP LAYOUT



BOTTOM LAYOUT

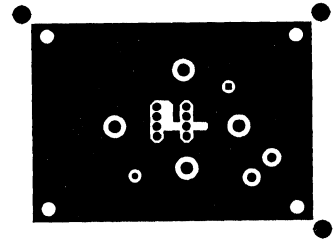


FIGURE 3. EVALUATION BOARD ARTWORK

Typical Application

A circuit which performs the sync stripper and DC restore functions is shown in Figure 4. Please reference Harris Application Note AN9514, titled "Video Amplifier with Sync Stripper and DC Restore", for details on this circuit.

The standard output of a VM700 video measurement set is shown in Figure 5. The output, after passing through the Applications Schematic shown on the first page of this data sheet, is shown in Figure 6.

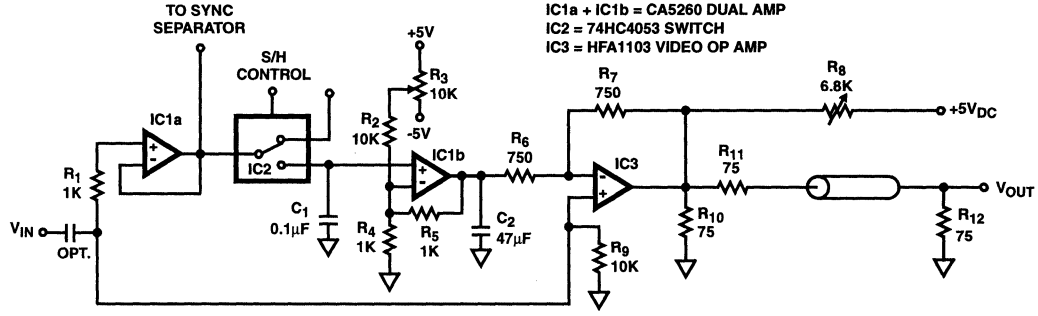


FIGURE 4. VIDEO AMPLIFIER WITH SYNC STRIPPER AND DC RESTORE

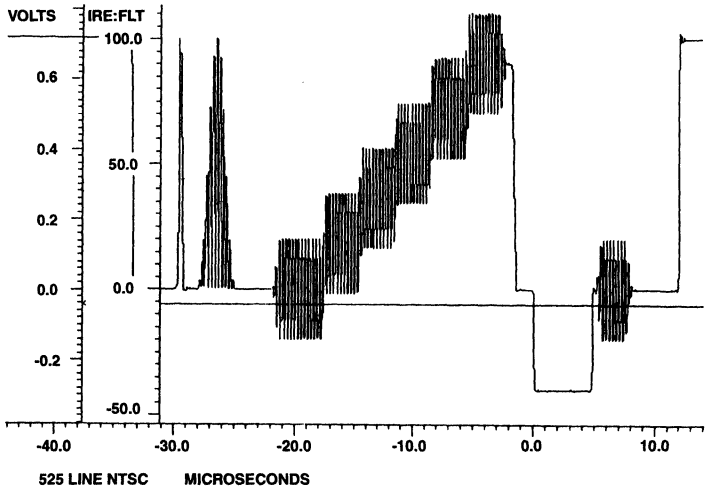


FIGURE 5. OUTPUT OF VM700 VIDEO MEASUREMENT SET

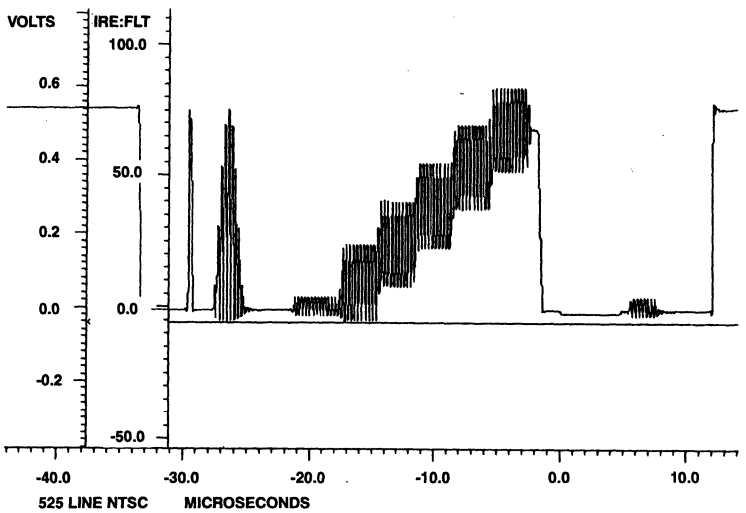


FIGURE 6. OUTPUT OF HFA1103 SYNC STRIPPER CONFIGURED AS ON THE FIRST PAGE OF THIS DATA SHEET

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (2%)
Thickness: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

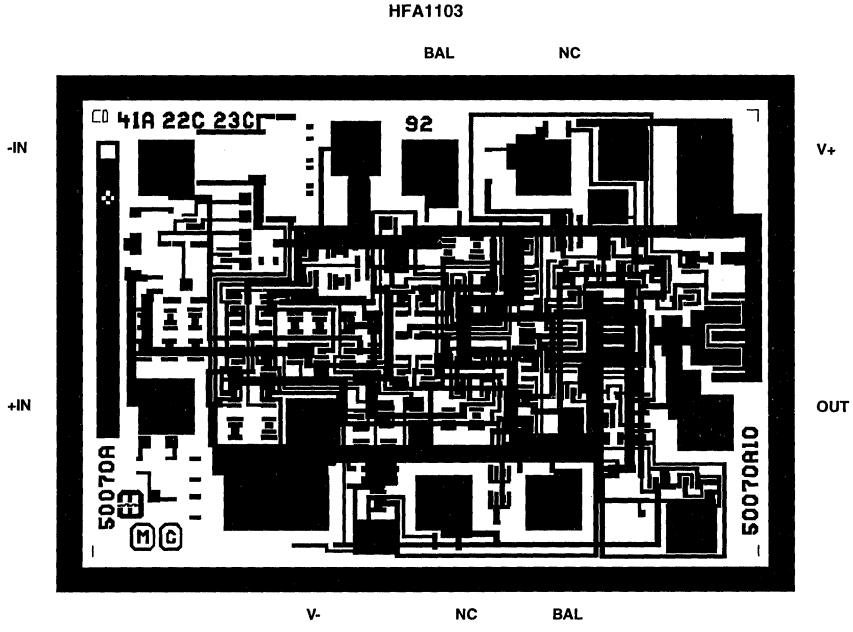
PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

50

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HFA1105

330MHz, Low Power, Current Feedback Video Operational Amplifier

November 1996

Features

- Low Supply Current 5.8mA
- High Input Impedance 1MΩ
- Wide -3dB Bandwidth 330MHz
- Very Fast Slew Rate 1000V/μs
- Gain Flatness (to 75MHz) 0.1dB
- Differential Gain 0.02%
- Differential Phase . . . . . 0.03 Degrees
- Pin Compatible Upgrade for CLC406

Applications

- Flash A/D Drivers
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications

Description

The HFA1105 is a high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

This amplifier features an excellent combination of low power dissipation (58mW) and high performance. The slew rate, bandwidth, and low output impedance (0.08Ω) make this amplifier a good choice for driving Flash ADCs. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications. The HFA1105 is ideal for interfacing to Harris' line of video crosspoint switches (HA4201, HA4600, HA4314, HA4404, HA4344), to create high performance, low power switchers and routers.

The HFA1105 is a low power, high performance upgrade for the CLC406. For a comparable amplifier with output disable or output limiting functions, please see the data sheets for the HFA1145 and HFA1135 respectively.

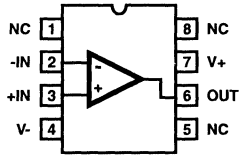
For Military grade product, please refer to the HFA1145/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1105IP	-40 to 85	8 Ld PDIP	E8.3
HFA1105IB (H1105I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1105
(PDIP, SOIC)
TOP VIEW



3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 3395.5

Absolute Maximum Ratings

Supply Voltage (V+ to V-) 11V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 1) ..... Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating ..... >600V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Die) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range ..... -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	47	50	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	45	48	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	50	54	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	47	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	47	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	0.8	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	25	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	2	5	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	60	-	Ω
Input Capacitance		C	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS Tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 6)	f = 100kHz	B	25	-	3.5	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	2.5	-	$pA/\sqrt{Hz}$
Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	20	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain	$A_V = -1$	C	25	-	500	-	kΩ
AC CHARACTERISTICS $R_F = 510\Omega$, Unless Otherwise Specified							
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, Note 6)	$A_V = +1$, $+R_S = 510\Omega$	B	25	-	270	-	MHz
		B	Full	-	240	-	MHz
	$A_V = -1$, $R_F = 425\Omega$	B	25	-	300	-	MHz
	$A_V = +2$	B	25	-	330	-	MHz
		B	Full	-	260	-	MHz
	$A_V = +10$, $R_F = 180\Omega$	B	25	-	130	-	MHz
		B	Full	-	90	-	MHz
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$ at $A_V = +2/-1$, $4V_{P-P}$ at $A_V = +1$, Note 6)	$A_V = +1$, $+R_S = 510\Omega$	B	25	-	135	-	MHz
	$A_V = -1$	B	25	-	140	-	MHz
	$A_V = +2$	B	25	-	115	-	MHz
Gain Flatness ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$, Note 6)	To 25MHz	B	25	-	±0.03	-	dB
		B	Full	-	±0.04	-	dB
	To 75MHz	B	25	-	±0.11	-	dB
		B	Full	-	±0.22	-	dB
Gain Flatness ($A_V = +1$, $+R_S = 510\Omega$, $V_{OUT} = 0.2V_{P-P}$, Note 6)	To 25MHz	B	25	-	±0.03	-	dB
	To 75MHz	B	25	-	±0.09	-	dB
Minimum Stable gain		A	Full	-	1	-	V/V
OUTPUT CHARACTERISTICS $A_V = +2$, $R_F = 510\Omega$, Unless Otherwise Specified							
Output Voltage Swing (Note 6)	$A_V = -1$, $R_L = 100\Omega$	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Output Current (Note 6)	$A_V = -1$, $R_L = 50\Omega$	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
Closed Loop Output Impedance (Note 6)	DC	B	25	-	0.08	-	Ω
Second Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 6)	10MHz	B	25	-	-48	-	dBc
	20MHz	B	25	-	-44	-	dBc
Third Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 6)	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Reverse Isolation (S_{12}, Note 6)	30MHz	B	25	-	-55	-	dB
TRANSIENT CHARACTERISTICS $A_V = +2$, $R_F = 510\Omega$, Unless Otherwise Specified							
Rise and Fall Times	$V_{OUT} = 0.5V_{P-P}$	B	25	-	1.1	-	ns
		B	Full	-	1.4	-	ns
Overshoot (Note 4) ($V_{OUT} = 0$ to 0.5V, V_{IN} $t_{RISE} = 1ns$)	+OS	B	25	-	3	-	%
	-OS	B	25	-	5	-	%
Overshoot (Note 4) ($V_{OUT} = 0.5V_{P-P}$, V_{IN} $t_{RISE} = 1ns$)	+OS	B	25	-	3	-	%
	-OS	B	25	-	11	-	%
Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $+R_S = 510\Omega$)	+SR	B	25	-	1000	-	V/µs
		B	Full	-	975	-	V/µs
	-SR (Note 5)	B	25	-	650	-	V/µs
		B	Full	-	580	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$)	+SR	B	25	-	1400	-	V/µs
		B	Full	-	1200	-	V/µs
	-SR (Note 5)	B	25	-	800	-	V/µs
		B	Full	-	700	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = -1$)	+SR	B	25	-	2100	-	V/µs
		B	Full	-	1900	-	V/µs
	-SR (Note 5)	B	25	-	1000	-	V/µs
		B	Full	-	900	-	V/µs
Settling Time ($V_{OUT} = +2V$ to 0V step, Note 6)	To 0.1%	B	25	-	15	-	ns
	To 0.05%	B	25	-	23	-	ns
	To 0.02%	B	25	-	30	-	ns
Overdrive Recovery Time	$V_{IN} = \pm2V$	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS $A_V = +2$, $R_F = 510\Omega$, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	$R_L = 150\Omega$	B	25	-	0.02	-	%
	$R_L = 75\Omega$	B	25	-	0.03	-	%

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current		A	25	-	5.8	6.1	mA
		A	Full	-	5.9	6.3	mA

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. Undershoot dominates for output signal swings below GND (e.g., $0.5V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0 to 0.5V condition. See the "Application Information" section for details.
5. Slew rates are asymmetrical if the output swings below GND (e.g. a bipolar signal). Positive unipolar output signals have symmetric positive and negative slew rates comparable to the +SR specification. See the "Application Information" section, and the pulse response graphs for details.
6. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1105 design is optimized for R_F = 510Ω at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains, however, the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For a gain of +1, a resistor (+R_S) in series with +IN is required to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	425	300
+1	510 (+R_S = 510Ω)	270
+2	510	330
+5	200	300
+10	180	130

Non-Inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Pulse Undershoot and Asymmetrical Slew Rates

The HFA1105 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (See Figures 5, 8, and 11). This undershoot isn't present for small bipolar signals, or large positive signals. Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (See Figures 5, 8, and 11), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (See Figures 4, 7, and 10).

PC Board Layout

The amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the device's input and output connections. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 270MHz (for A_V = +1). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, the bandwidth decreases as the load capacitance increases. For example, at A_V = +1, R_S = 62Ω, C_L = 40pF, the overall bandwidth is limited to 180MHz, and bandwidth drops to 75MHz at A_V = +1, R_S = 8Ω, C_L = 400pF.

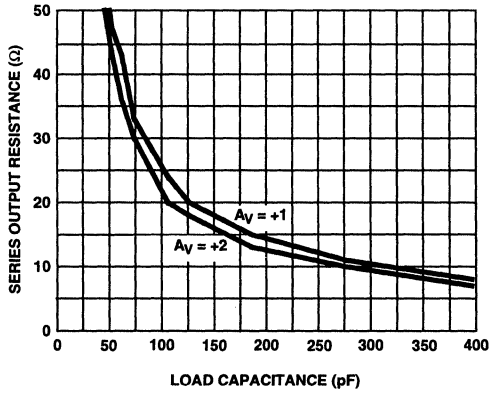


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1105 may be evaluated using the HFA11XX Evaluation Board.

The layout and schematic of the board are shown in Figure 2. To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

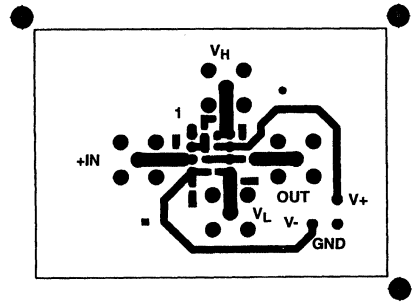


FIGURE 2A. TOP LAYOUT

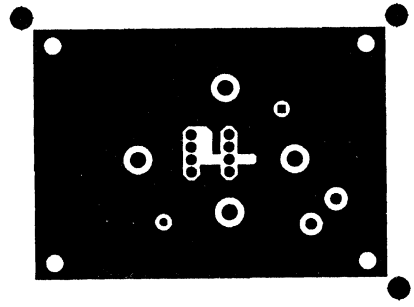


FIGURE 2B. BOTTOM LAYOUT

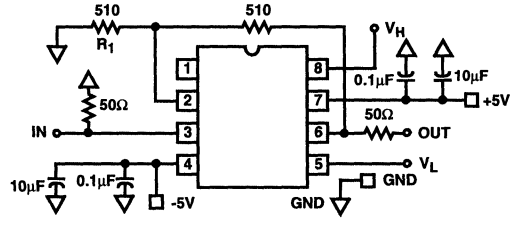


FIGURE 2C. SCHEMATIC

FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

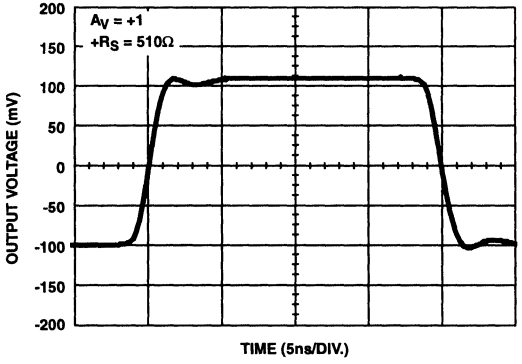


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

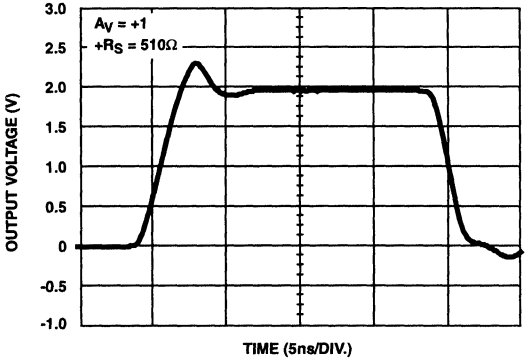


FIGURE 4. LARGE SIGNAL POSITIVE PULSE RESPONSE

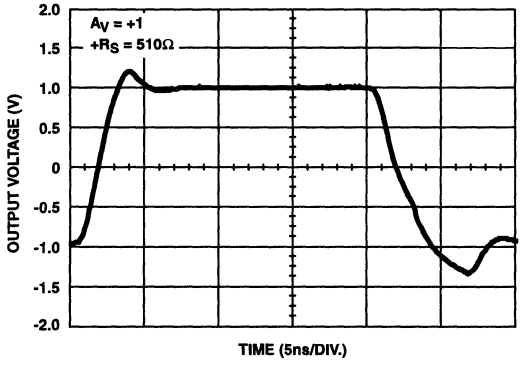


FIGURE 5. LARGE SIGNAL BIPOLAR PULSE RESPONSE

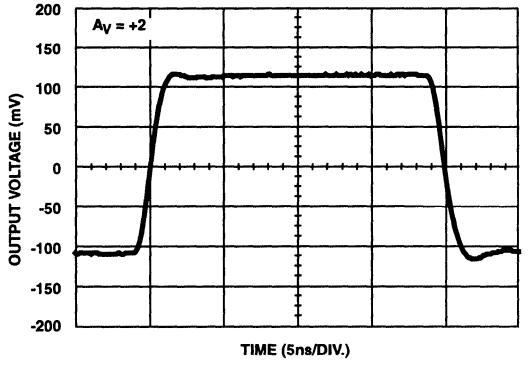


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

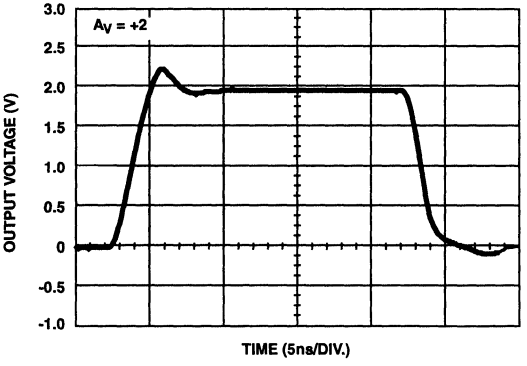


FIGURE 7. LARGE SIGNAL POSITIVE PULSE RESPONSE

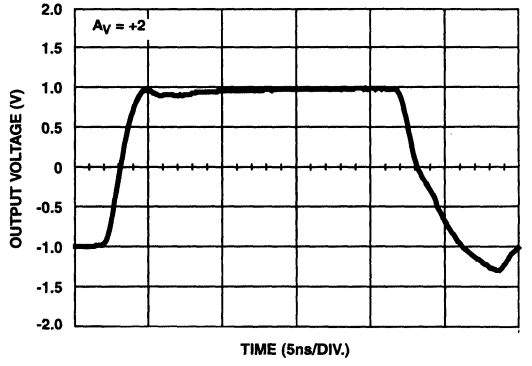


FIGURE 8. LARGE SIGNAL BIPOLAR PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

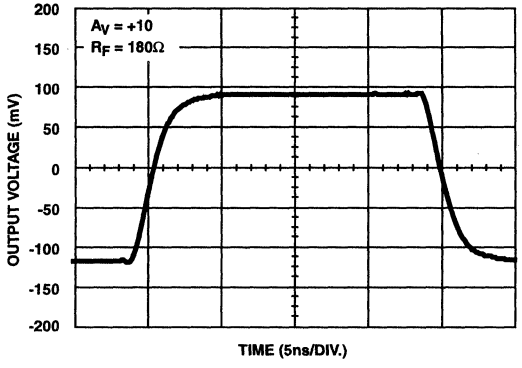


FIGURE 9. SMALL SIGNAL PULSE RESPONSE

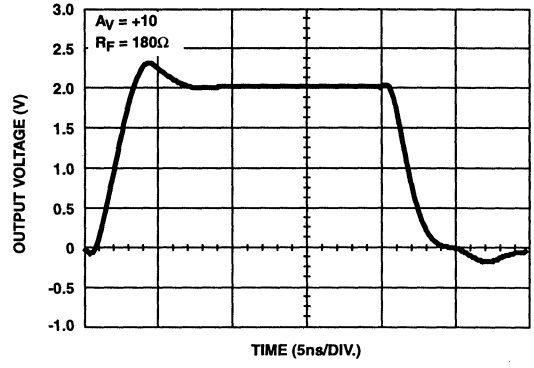


FIGURE 10. LARGE SIGNAL POSITIVE PULSE RESPONSE

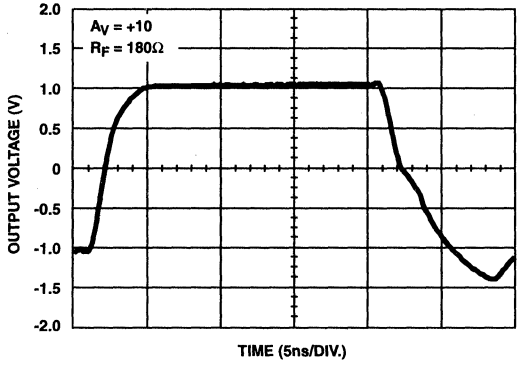


FIGURE 11. LARGE SIGNAL BIPOLAR PULSE RESPONSE

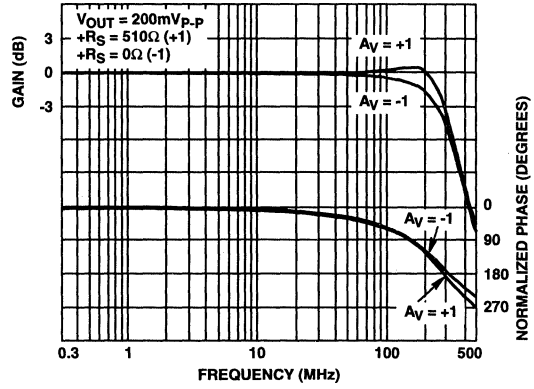


FIGURE 12. FREQUENCY RESPONSE

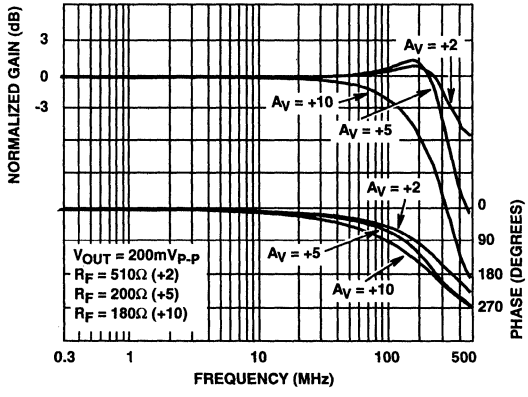


FIGURE 13. FREQUENCY RESPONSE

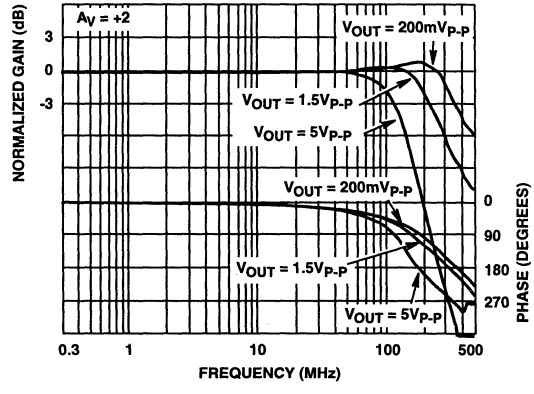


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

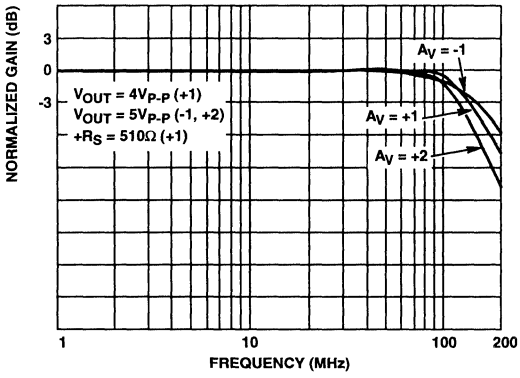


FIGURE 15. FULL POWER BANDWIDTH

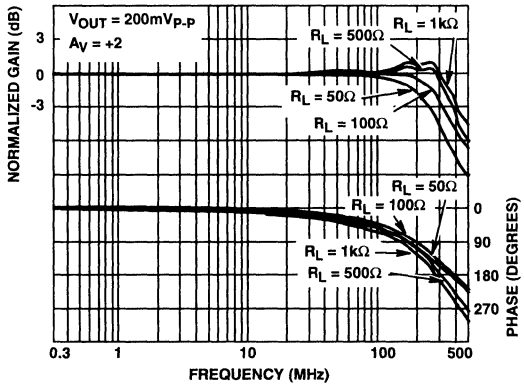


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

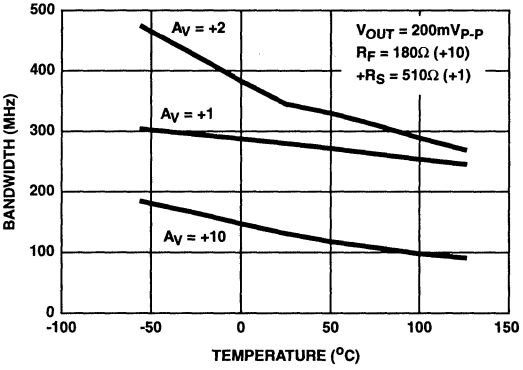


FIGURE 17. -3dB BANDWIDTH vs TEMPERATURE

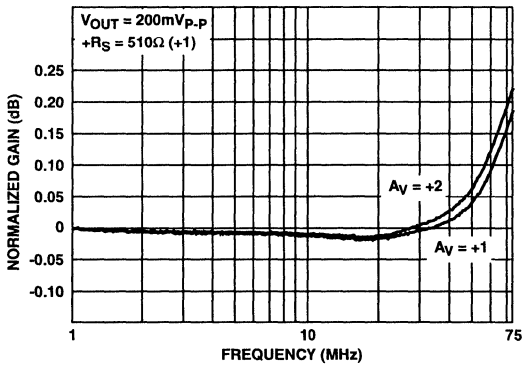


FIGURE 18. GAIN FLATNESS

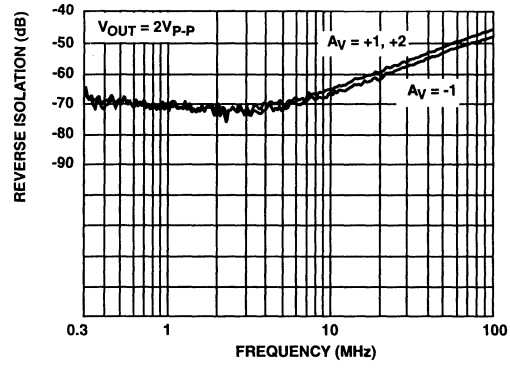


FIGURE 19. REVERSE ISOLATION

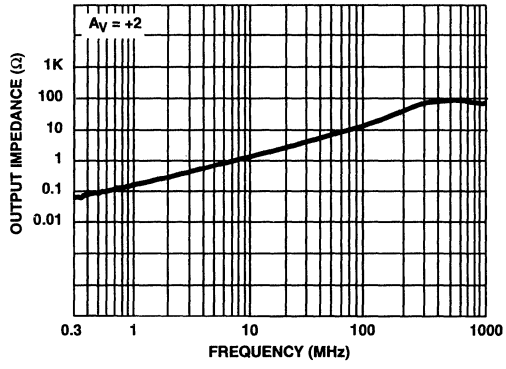


FIGURE 20. OUTPUT IMPEDANCE

3

OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

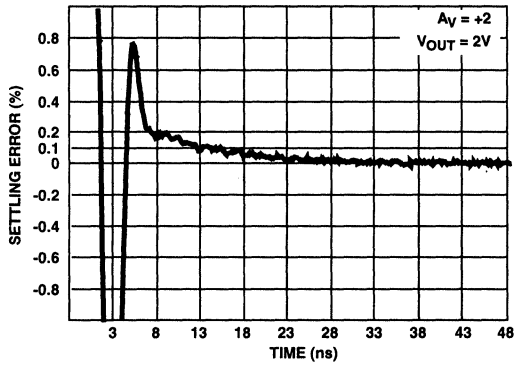


FIGURE 21. SETTLING RESPONSE

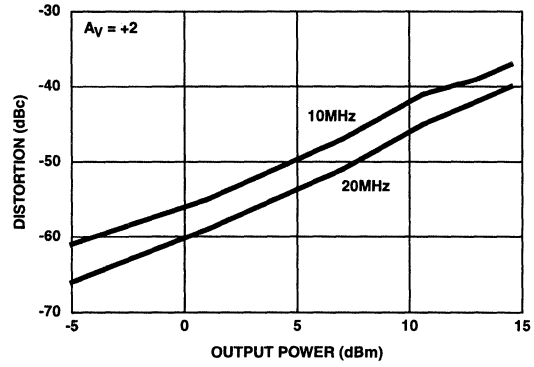


FIGURE 22. SECOND HARMONIC DISTORTION vs P_{OUT}

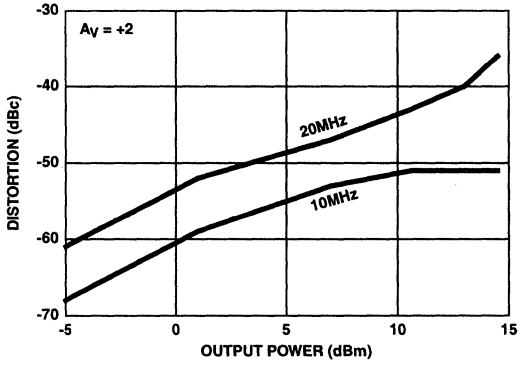


FIGURE 23. THIRD HARMONIC DISTORTION vs P_{OUT}

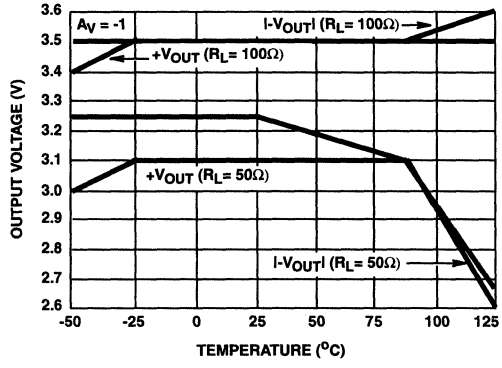


FIGURE 24. OUTPUT VOLTAGE vs TEMPERATURE

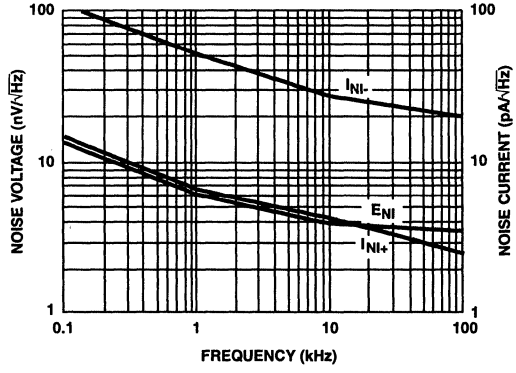


FIGURE 25. INPUT NOISE CHARACTERISTICS

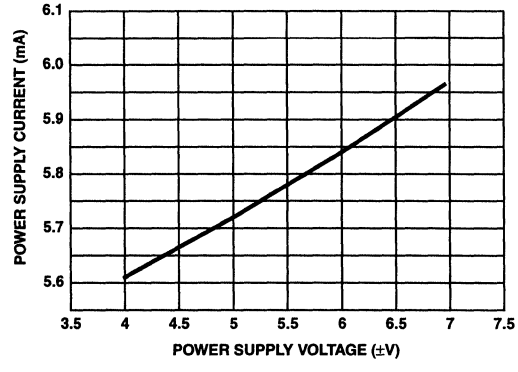


FIGURE 26. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

59 mils x 59 mils x 19 mils
1500µm x 1500µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

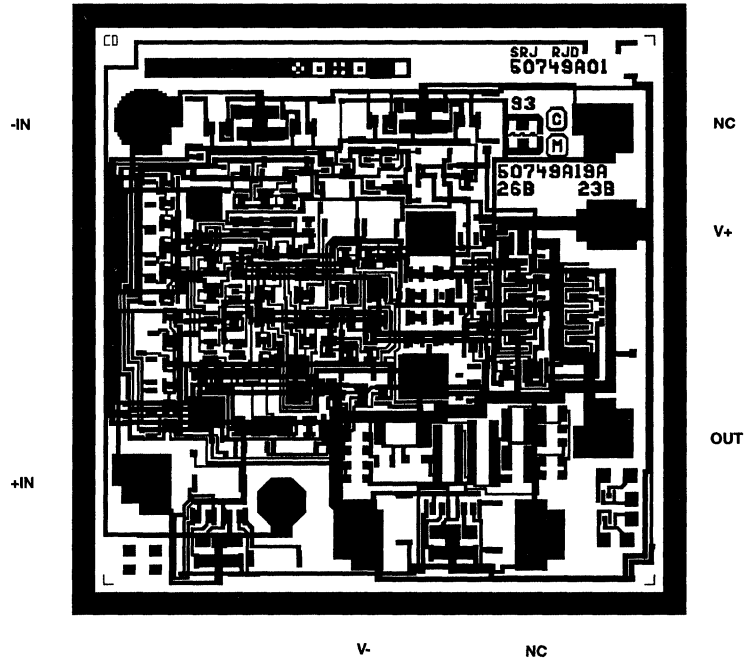
75

SUBSTRATE POTENTIAL (Powered Up):

Floating
(Recommend Connection to V-)

Metallization Mask Layout

HFA1105



HARRIS SEMICONDUCTOR

HFA1106

315MHz, Low Power, Video Operational Amplifier with Compensation Pin

November 1996

Features

- Compensation Pin for Bandwidth Limiting
- Lower Lot-to-Lot Variability With External Compensation
- High Input Impedance 1MΩ
- Differential Gain 0.02%
- Differential Phase ..... 0.05 Degrees
- Wide -3dB Bandwidth 315MHz
- Very Fast Slew Rate 700V/μs
- Low Supply Current 5.8mA
- Gain Flatness (to 100MHz) ..... ±0.1dB

Applications

- Noise Critical Applications
- Professional Video Processing
- Medical Imaging
- Video Digitizing Boards/Systems
- Radar/IF Processing
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- Flash A/D Drivers
- Oscilloscopes and Analyzers

Description

The HFA1106 is a high speed, low power current feedback operational amplifier built with Harris' proprietary complementary bipolar UHF-1 process. This amplifier features a compensation pin connected to the internal high impedance node, which allows for implementation of external clamping or bandwidth limiting.

Bandwidth limiting is accomplished by connecting a capacitor (C_{COMP}) and series damping resistor (R_{COMP}) from pin 8 to ground. Amplifier performance for various values of C_{COMP} is documented in the Electrical Specifications.

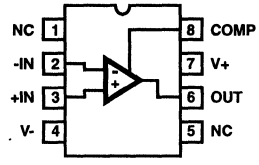
The HFA1106 is ideal for noise critical wideband applications. Not only can the bandwidth be limited to minimize broadband noise, the HFA1106 is optimized for lower feedback resistors (R_F = 100Ω for A_V = +2) than most current feedback amplifiers. The low feedback resistor reduces the inverting input noise current contribution to total output noise, while reducing DC errors as well. Please see the "Application Information" section for details.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1106IP	-40 to 85	8 Ld PDIP	E8.3
HFA1106IB (H1106I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1106
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3922.1**

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 1) ..... Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating ..... >600V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Die Only) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range ..... -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability; however, continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $C_{COMP} = 0pF$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	47	50	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	45	48	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	50	54	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	47	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	47	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	0.8	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	25	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	2	5	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	4	8	µA/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $C_{COMP} = 0pF$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Resistance		C	25	-	60	-	Ω
Input Capacitance		C	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS Tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	3.5	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	2.5	-	$pA/\sqrt{Hz}$
Inverting Input Noise Current Density	f = 100kHz	B	25	-	20	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain	$A_V = -1$	C	25	-	500	-	kΩ
AC CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
-3dB Bandwidth ($A_V = +1$, $R_F = 150\Omega$, $V_{OUT} = 0.2V_{P-P}$)	$C_C = 0pF$	B	25	250	315	-	MHz
	$C_C = 2pF$	B	25	140	170	-	MHz
	$C_C = 5pF$	B	25	65	80	-	MHz
-3dB Bandwidth ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$)	$C_C = 0pF$	B	25	185	245	-	MHz
	$C_C = 2pF$	B	25	110	140	-	MHz
	$C_C = 5pF$	B	25	55	70	-	MHz
±0.1dB Flat Bandwidth ($A_V = +1$, $R_F = 150\Omega$, $V_{OUT} = 0.2V_{P-P}$)	$C_C = 0pF$	B	25	45	65	-	MHz
	$C_C = 2pF$	B	25	25	40	-	MHz
	$C_C = 5pF$	B	25	13	17	-	MHz
±0.1dB Flat Bandwidth ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$)	$C_C = 0pF$	B	25	60	100	-	MHz
	$C_C = 2pF$	B	25	15	30	-	MHz
	$C_C = 5pF$	B	25	11	14	-	MHz
Minimum Stable Gain		A	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
Output Voltage Swing	$A_V = -1$, $R_F = 510\Omega$	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current	$A_V = -1$, $R_L = 50\Omega$, $R_F = 510\Omega$	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Closed Loop Output Impedance	DC	B	25	-	0.07	-	Ω
Output Short Circuit Current	$A_V = -1$	B	25	-	90	-	mA
Second Harmonic Distortion (10MHz, $V_{OUT} = 2V_{P-P}$)	$C_C = 0pF$	B	25	-45	-53	-	dBc
	$C_C = 2pF$	B	25	-42	-48	-	dBc
	$C_C = 5pF$	B	25	-38	-44	-	dBc
Third Harmonic Distortion (10MHz, $V_{OUT} = 2V_{P-P}$)	$C_C = 0pF$	B	25	-50	-57	-	dBc
	$C_C = 2pF$	B	25	-48	-56	-	dBc
	$C_C = 5pF$	B	25	-48	-56	-	dBc
Second Harmonic Distortion (20MHz, $V_{OUT} = 2V_{P-P}$)	$C_C = 0pF$	B	25	-42	-46	-	dBc
	$C_C = 2pF$	B	25	-38	-42	-	dBc
	$C_C = 5pF$	B	25	-34	-38	-	dBc
Third Harmonic Distortion (20MHz, $V_{OUT} = 2V_{P-P}$)	$C_C = 0pF$	B	25	-46	-57	-	dBc
	$C_C = 2pF$	B	25	-52	-57	-	dBc
	$C_C = 5pF$	B	25	-50	-57	-	dBc

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $C_{COMP} = 0pF$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
TRANSIENT CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$, $A_V = +1$, $R_F = 150\Omega$)	$C_C = 0pF$	B	25	-	2.6	2.9	ns
	$C_C = 2pF$	B	25	-	3.7	4.2	ns
	$C_C = 5pF$	B	25	-	5.2	6.2	ns
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$, $A_V = +2$)	$C_C = 0pF$	B	25	-	2.7	3.2	ns
	$C_C = 2pF$	B	25	-	3.9	4.4	ns
	$C_C = 5pF$	B	25	-	5.9	6.9	ns
Overshoot (Note 4) ($A_V = +1$, $R_F = 150\Omega$, V_{IN} $t_{RISE} = 2.5ns$)	$V_{OUT} = 250mV_{P-P}$	B	25	-	1.5	4	%
	$V_{OUT} = 2V_{P-P}$	B	25	-	6	10	%
	$V_{OUT} = 0V$ to $2V$	B	25	-	4	7.5	%
Overshoot (Note 4) ($A_V = +2$, V_{IN} $t_{RISE} = 2.5ns$)	$V_{OUT} = 250mV_{P-P}$	B	25	-	2	5	%
	$V_{OUT} = 2V_{P-P}$	B	25	-	6.5	12	%
	$V_{OUT} = 0V$ to $2V$	B	25	-	2.5	7.5	%
Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $R_F = 150\Omega$)	+SR, $C_C = 0pF$	B	25	580	680	-	V/µs
	-SR, $C_C = 0pF$	B	25	400	545	-	V/µs
	+SR, $C_C = 2pF$	B	25	470	530	-	V/µs
	-SR, $C_C = 2pF$	B	25	300	410	-	V/µs
	+SR, $C_C = 5pF$	B	25	320	365	-	V/µs
	-SR, $C_C = 5pF$	B	25	200	300	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$)	+SR, $C_C = 0pF$	B	25	750	910	-	V/µs
	-SR, $C_C = 0pF$	B	25	500	720	-	V/µs
	+SR, $C_C = 2pF$	B	25	550	730	-	V/µs
	-SR, $C_C = 2pF$	B	25	350	520	-	V/µs
	+SR, $C_C = 5pF$	B	25	380	485	-	V/µs
	-SR, $C_C = 5pF$	B	25	250	375	-	V/µs
Settling Time ($V_{OUT} = +2V$ to $0V$ Step, $C_C = 0pF$ to $5pF$)	To 0.1%	B	25	-	26	35	ns
	To 0.05%	B	25	-	33	43	ns
	To 0.02%	B	25	-	49	75	ns
Overdrive Recovery Time	$V_{IN} = \pm2V$	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
Differential Gain ($f = 3.58MHz$, $R_L = 150\Omega$)	$C_C = 0pF$	B	25	-	0.02	-	%
	$C_C = 5pF$	B	25	-	0.02	-	%
Differential Phase ($f = 3.58MHz$, $R_L = 150\Omega$)	$C_C = 0pF$	B	25	-	0.05	-	Degrees
	$C_C = 5pF$	B	25	-	0.07	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current		A	25	-	5.8	6.1	mA
		A	Full	-	5.9	6.3	mA

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. Undershoot dominates for output signal swings below GND (e.g. $2V_{P-P}$) yielding a higher overshoot limit compared to the $V_{OUT} = 0V$ to $2V$ condition.

Application Information

Optimum Feedback Resistor

All current feedback amplifiers (CFAs) require a feedback resistor (R_F) even for unity gain applications, and R_F in conjunction with the internal compensation capacitor sets the dominant pole of the frequency response. Thus the amplifier's bandwidth is inversely proportional to R_F. The HFA1106 design is optimized for $R_F = 150\Omega$ at a gain of +1. Decreasing R_F decreases stability resulting in excessive peaking and overshoot - Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies. At higher gains, however, the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth (e.g., $R_F = 100\Omega$ for $A_V = +2$).

Why Use Externally Compensated Amplifiers?

Externally compensated op amps were originally developed to allow operation at gains below the amplifier's minimum stable gain. This enabled development of non-unity gain stable op amps with very high bandwidth and slew rates. Users needing lower closed loop gains could stabilize the amplifier with external compensation if the associated performance decrease was tolerable.

With the advent of CFAs, unity gain stability and high performance are no longer mutually exclusive, so why offer unity gain stable op amps with compensation pins?

The main reason for external compensation is to allow users to tailor the amplifier's performance to their specific system needs. Bandwidth can be limited to the exact value required, thereby eliminating excess bandwidth and its associated noise. A compensated op amp is also more predictable; lower lot-to-lot variation requires less system overdesign to cover process variability. Finally, access to the internal high impedance node allows users to implement external output limiting or allows for stabilizing the amplifier when driving large capacitive loads.

Noise Advantages - Uncompensated

The HFA1106 delivers lower broadband noise even without an external compensation capacitor. Package capacitance present at the Comp pin stabilizes the op amp, so lower value feedback resistors can be used. A smaller value R_F minimizes the noise voltage contribution of the amplifier's inverting input noise current - $I_{NI} \times R_F$, usually a large contributor on CFAs - and minimizes the resistor's thermal noise contribution ($4KTR_F$). Figure 1 details the HFA1105 broadband noise performance in its recommended configuration of $A_V = +2$, and $R_F = 510\Omega$. Adding a Comp pin to the HFA1105 (thereby creating the HFA1106) yields the 23% noise reduction shown in Figure 2. In both cases, the scope bandwidth, 100MHz, limits the measurement range to prevent amplifier bandwidth differences from affecting the results.

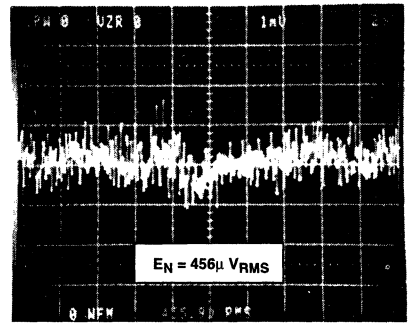


FIGURE 1. HFA1105 NOISE PERFORMANCE, $A_V = +2$, $R_F = 510\Omega$

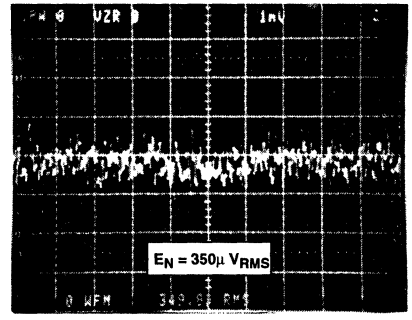


FIGURE 2. HFA1106 NOISE PERFORMANCE, UNCOMPENSATED, $A_V = +2$, $R_F = 100\Omega$

Offset Advantage

An added advantage of the lower value R_F is a smaller DC output offset. The op amp's inverting input bias current (I_{BI}) flows through the feedback resistor and generates an offset voltage error defined by:

$$V_E = I_{BI} \times R_F; \text{ and } V_{OS} = A_V (\pm V_{IO}) \pm V_E$$

Reducing R_F reduces these errors.

Bandwidth Limiting

The HFA1106 bandwidth may be limited by connecting a resistor, R_{COMP} (required to damp the interaction between the compensation capacitor and the package parasitics), and capacitor, C_{COMP}, in series from pin 8 to GND. Typical performance characteristics for various C_{COMP} values are listed in the specification table. The HFA1106 is already unity gain stable, so the main reason for limiting the bandwidth is to reduce the broadband noise.

Noise Advantages - Compensated

System noise reduction is maximized by limiting the op amp to the bandwidth required for the application. Noise increases as the square root of the bandwidth increase (4x bandwidth increase yields 2x noise increase), so eliminating excess

bandwidth significantly reduces system noise. Figure 3 illustrates the noise performance of the HFA1106 with its bandwidth limited to 40MHz by a 10pF C_{COMP}. As expected the noise decreases by approximately 37% (100% x (1-$\sqrt{40MHz/100MHz}$)) compared with Figure 2. The decrease is an even more dramatic 48% versus the HFA1105 noise level in Figure 1.

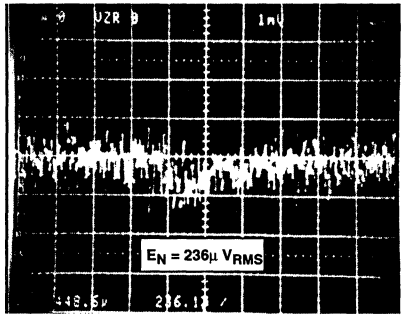


FIGURE 3. HFA1106 NOISE PERFORMANCE, COMPENSATED, A_V = +2, R_F = 100Ω, C_C = 10pF

Additionally, compensating the HFA1106 allows the use of a lower value R_F for a given gain. The decreased bandwidth due to C_{COMP} keeps the amplifier stable by offsetting the increased bandwidth from the lower R_F. As noted previously, a lower value R_F provides the double benefit of reduced DC errors and lower total noise.

Less Lot-to-Lot Variability

External compensation provides another advantage by allowing designers to set the op amp's performance with a precision external component. On-chip compensation capacitors can vary by 10-20% over the process extremes. A precise external capacitor dominates the on-chip compensation for consistent lot-to-lot performance and more robust designs. Compensating high frequency amplifiers to lower bandwidths can simplify design tasks and ensure long term manufacturability.

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the device's input and output connections. Capacitance, parasitic or planned, connected to the output must be minimized, compensated for by increasing C_{COMP}, or isolated by a series output resistor.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

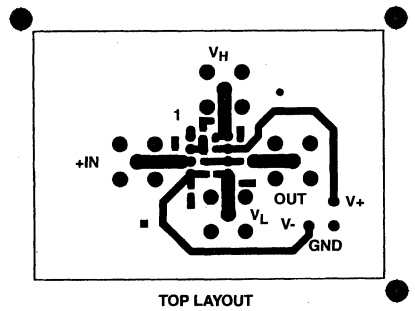
An example of a good high frequency layout is the Evaluation Board shown in Figure 4.

Evaluation Board

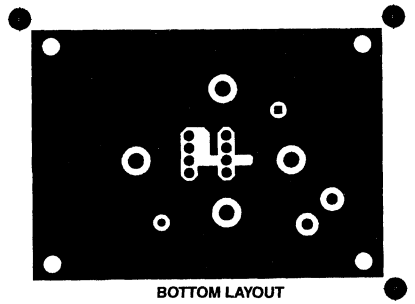
The performance of the HFA1106 may be evaluated using the HFA11XX Evaluation Board.

Figure 4 details the evaluation board layout and schematic. Connecting R_{COMP} and C_{COMP} in series from socket pin 8 to the GND plane compensates the op amp. Cutting the trace from pin 8 to the V_H connector removes the stray parallel capacitance, which would otherwise affect the evaluation. Additionally, the 500Ω feedback and gain setting resistors should be changed to the proper value for the gain being evaluated.

To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.



TOP LAYOUT



BOTTOM LAYOUT

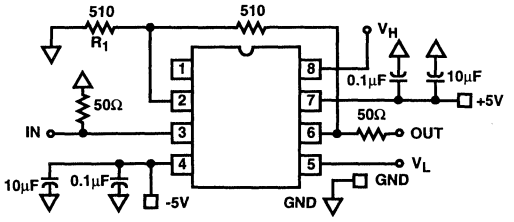


FIGURE 4. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

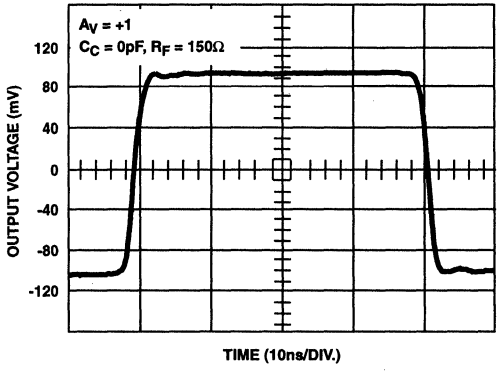


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

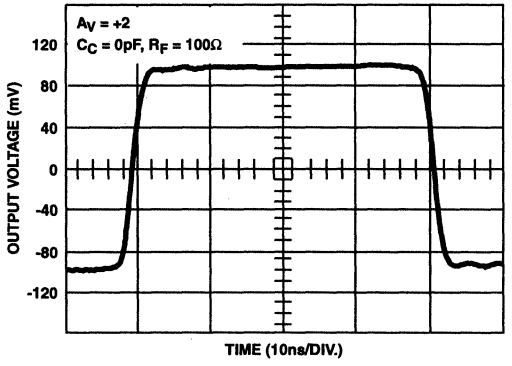


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

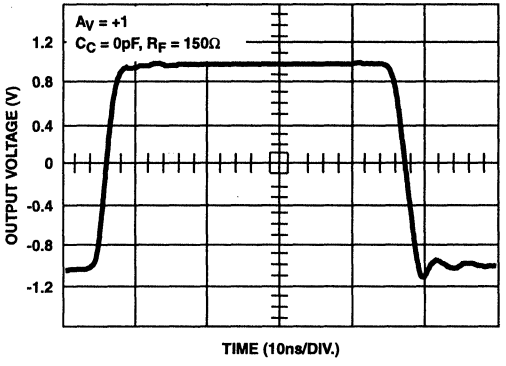


FIGURE 7. LARGE SIGNAL PULSE RESPONSE

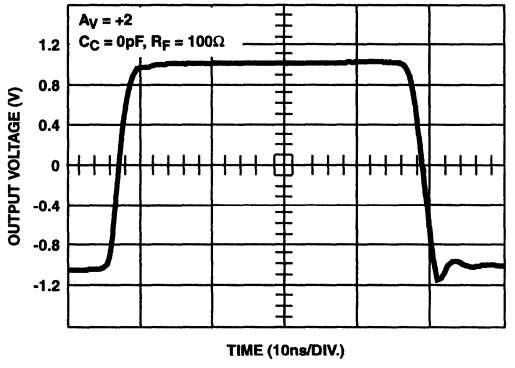


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

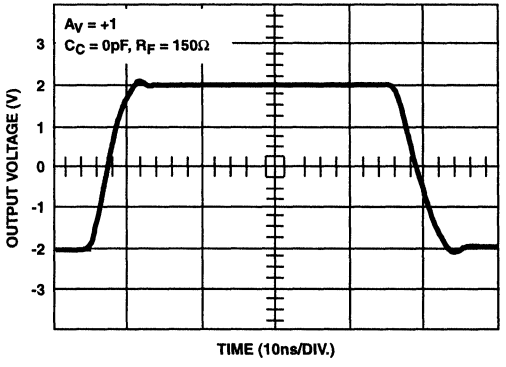


FIGURE 9. LARGE SIGNAL PULSE RESPONSE

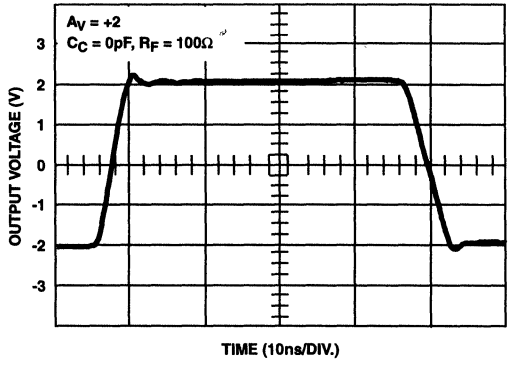


FIGURE 10. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

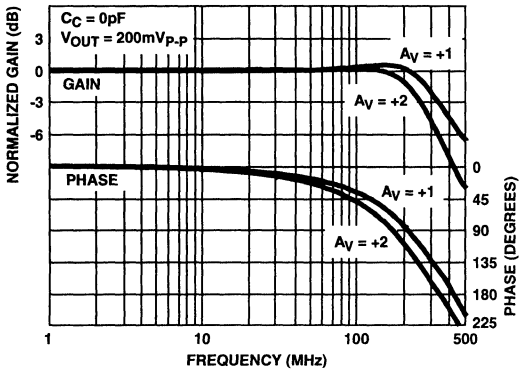


FIGURE 11. FREQUENCY RESPONSE

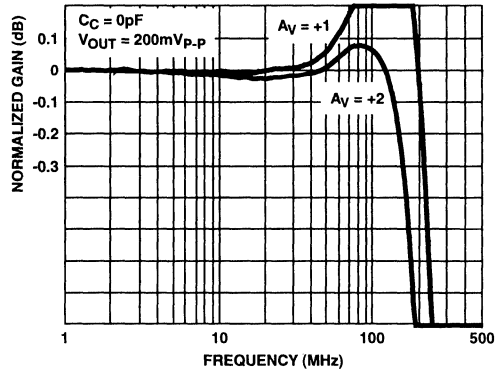


FIGURE 12. GAIN FLATNESS

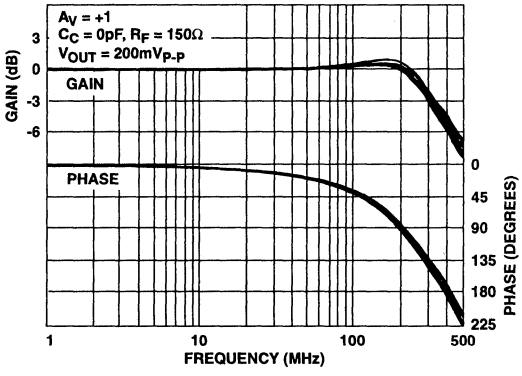


FIGURE 13. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

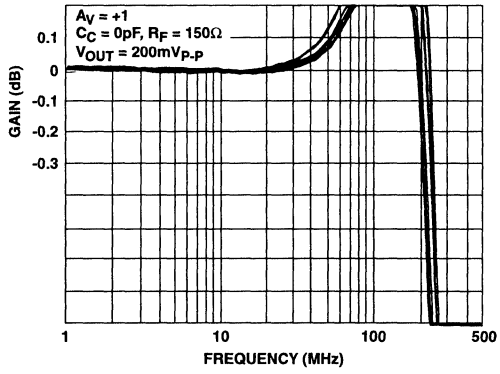


FIGURE 14. GAIN FLATNESS (12 UNITS, 4 RUNS)

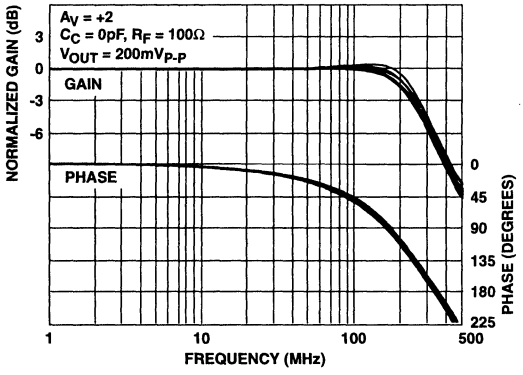


FIGURE 15. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

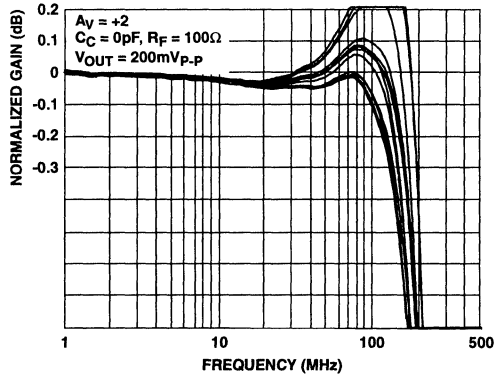


FIGURE 16. GAIN FLATNESS (12 UNITS, 4 RUNS)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

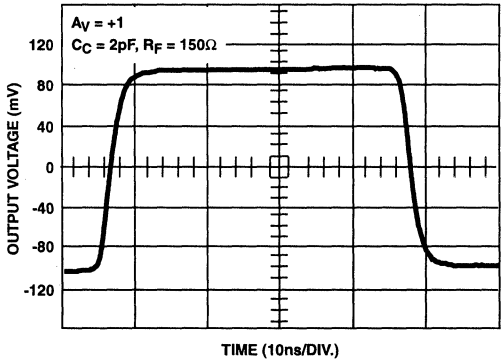


FIGURE 17. SMALL SIGNAL PULSE RESPONSE

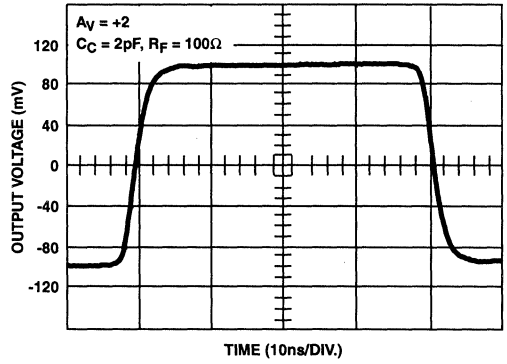


FIGURE 18. SMALL SIGNAL PULSE RESPONSE

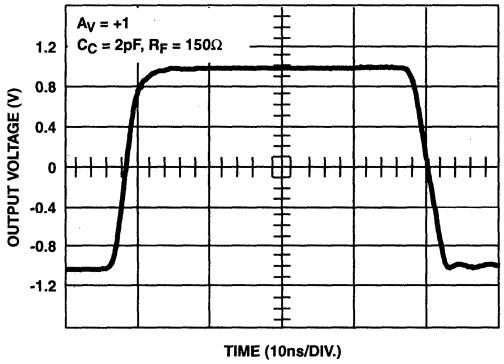


FIGURE 19. LARGE SIGNAL PULSE RESPONSE

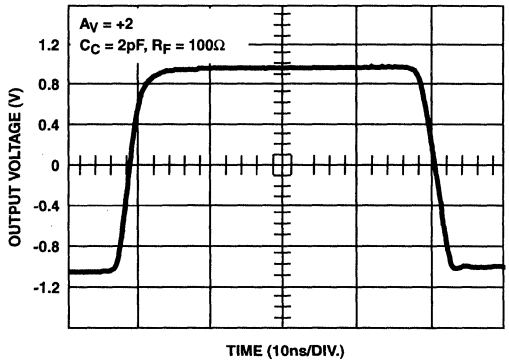


FIGURE 20. LARGE SIGNAL OUTPUT VOLTAGE

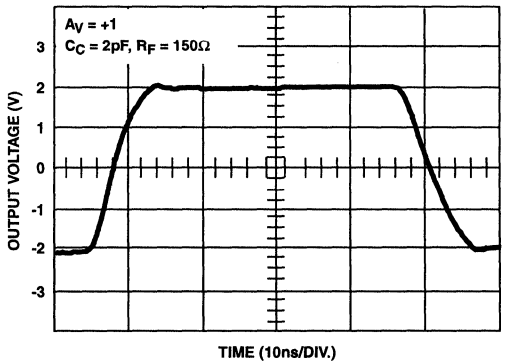


FIGURE 21. LARGE SIGNAL PULSE RESPONSE

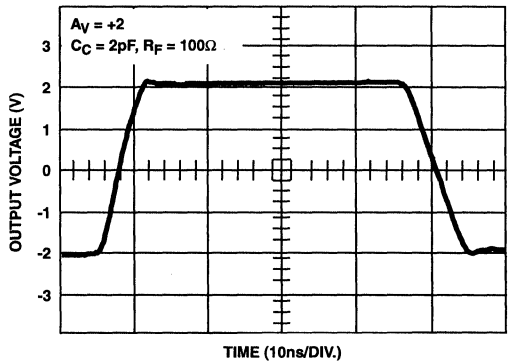


FIGURE 22. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

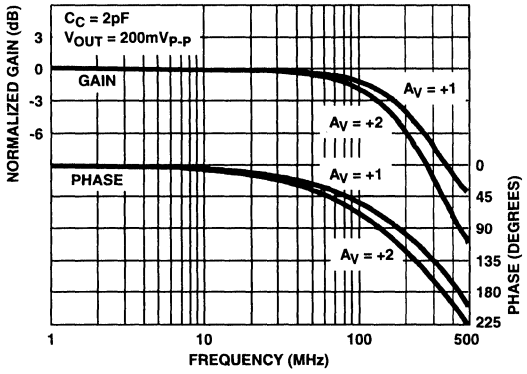


FIGURE 23. FREQUENCY RESPONSE

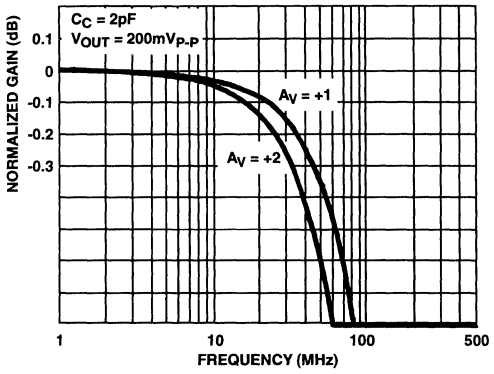


FIGURE 24. GAIN FLATNESS

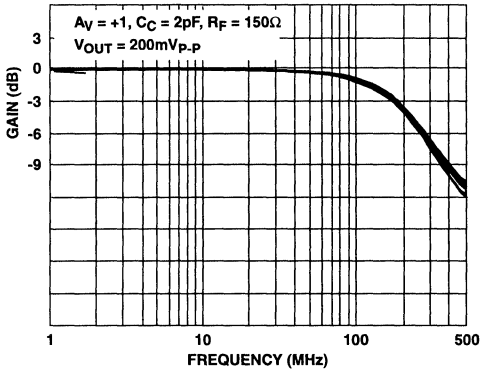


FIGURE 25. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

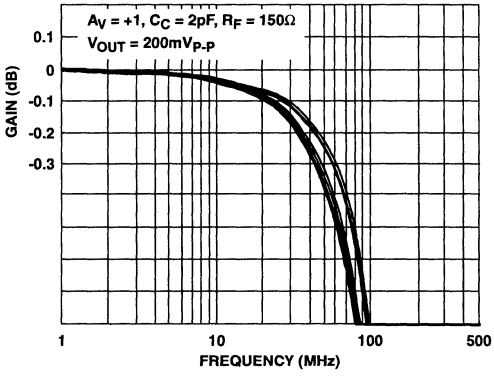


FIGURE 26. GAIN FLATNESS (12 UNITS, 4 RUNS)

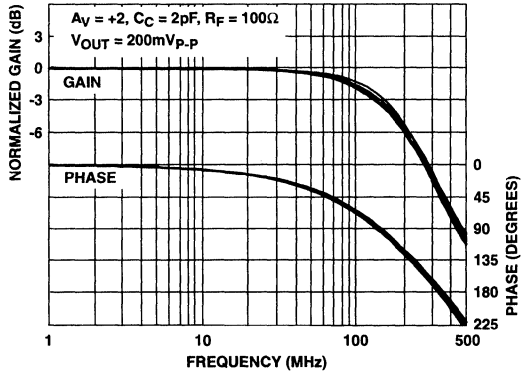


FIGURE 27. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

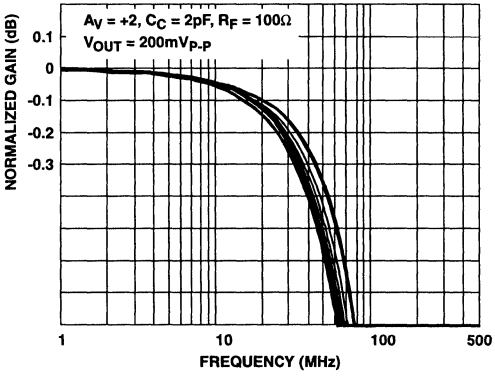


FIGURE 28. GAIN FLATNESS (12 UNITS, 4 RUNS)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

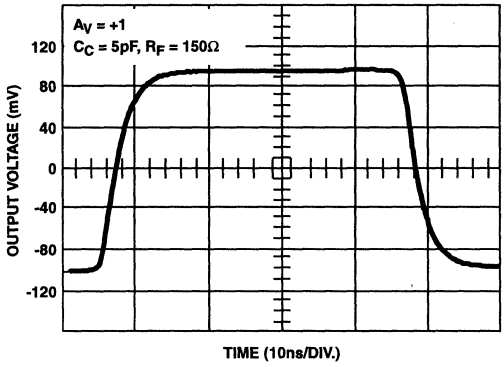


FIGURE 29. SMALL SIGNAL PULSE RESPONSE

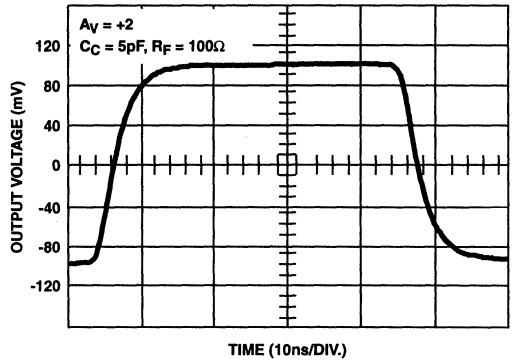


FIGURE 30. SMALL SIGNAL PULSE RESPONSE

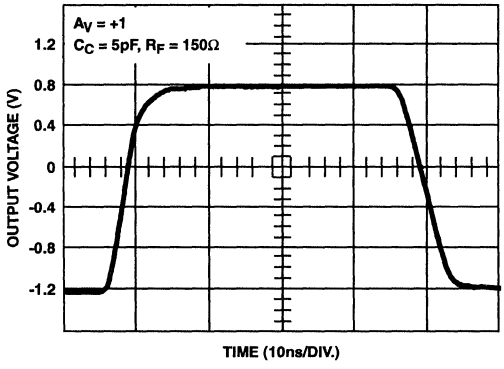


FIGURE 31. LARGE SIGNAL PULSE RESPONSE

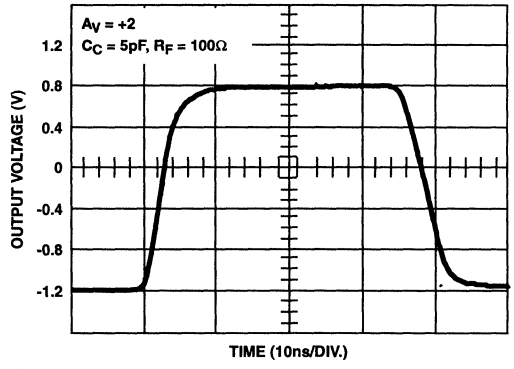


FIGURE 32. LARGE SIGNAL PULSE RESPONSE

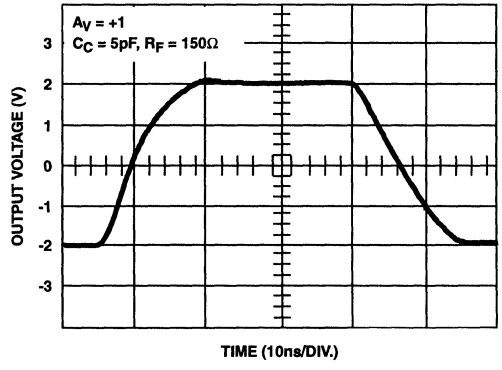


FIGURE 33. LARGE SIGNAL PULSE RESPONSE

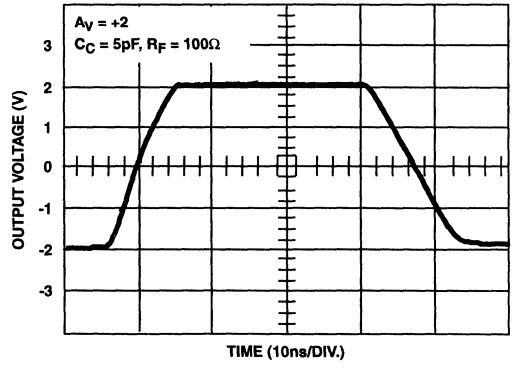


FIGURE 34. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

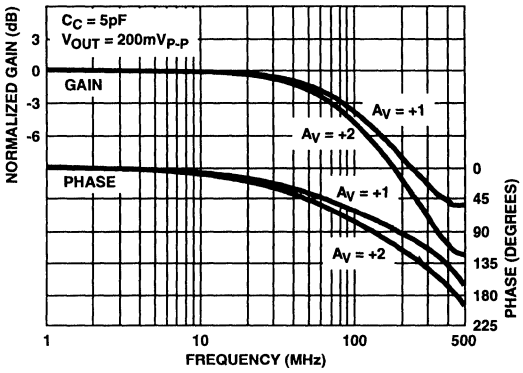


FIGURE 35. FREQUENCY RESPONSE

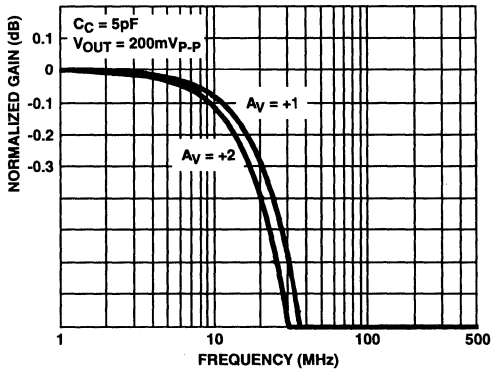


FIGURE 36. GAIN FLATNESS

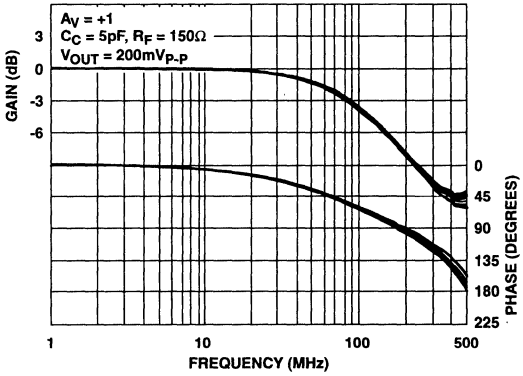


FIGURE 37. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

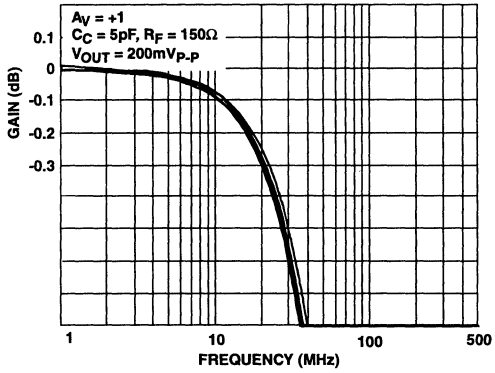


FIGURE 38. GAIN FLATNESS (12 UNITS, 4 RUNS)

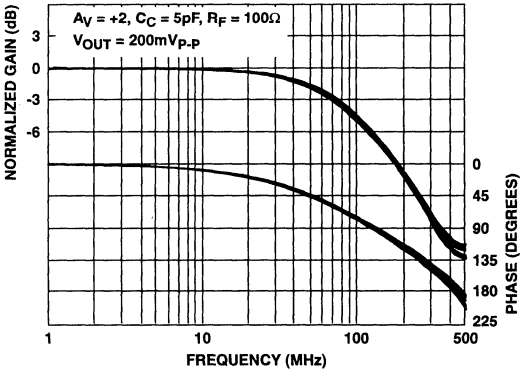


FIGURE 39. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

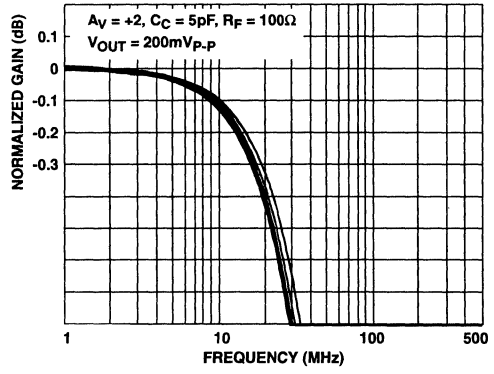


FIGURE 40. GAIN FLATNESS (12 UNITS, 4 RUNS)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

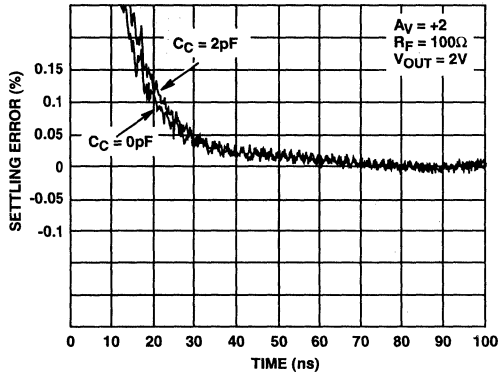


FIGURE 41. SETTLING RESPONSE

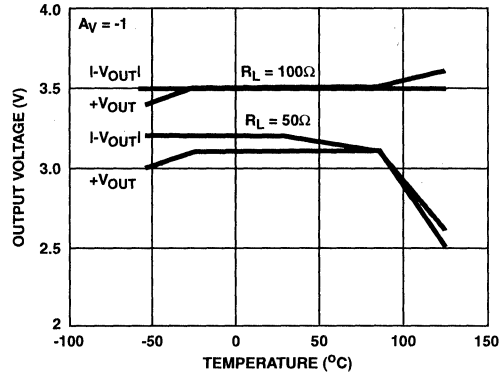


FIGURE 42. OUTPUT VOLTAGE vs TEMPERATURE

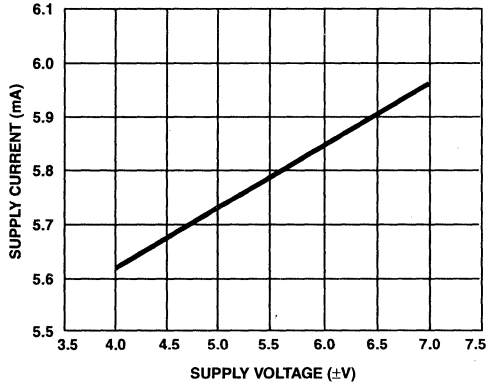


FIGURE 43. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

59 mils x 58.2 mils x 19 mils
1500µm x 1480µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

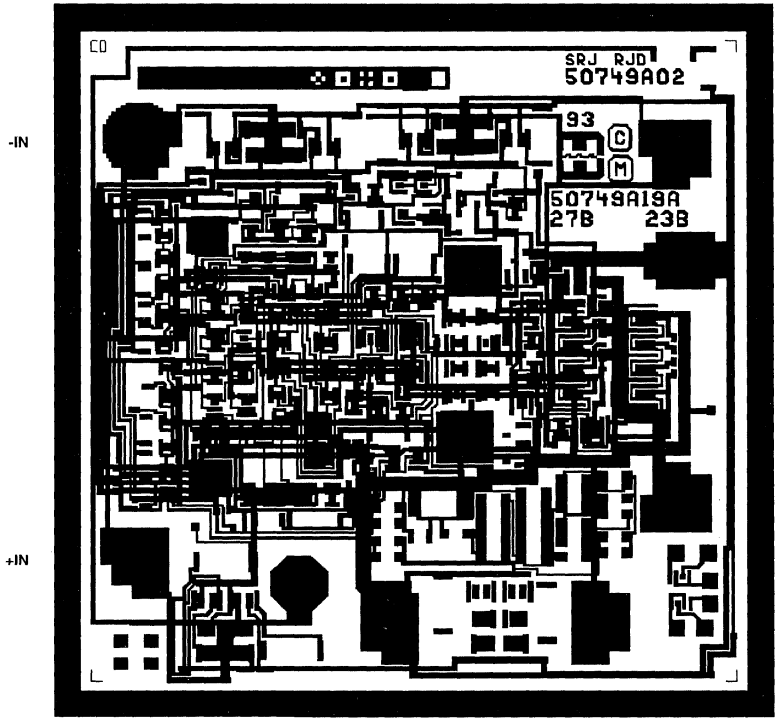
75

SUBSTRATE POTENTIAL (Powered Up):

Floating
(Recommend Connection to V-)

Metallization Mask Layout

HFA1106



Complete data sheet available via web, Harris home page http://www.semi.harris.com/ or via Harris AnswerFAX, see Section 12

HFA1109, HFA1149

PRELIMINARY

November 1996

550MHz, Low Power, Current Feedback Operational Amplifiers

Features

- Wide - 3dB Bandwidth (A_V = +2) 550MHz
- Gain Flatness (To 250MHz) 0.5dB
- Very Fast Slew Rate (A_V = +2) 1200V/µs
- High Input Impedance 1.7MΩ
- Differential Gain/Phase . . . . . 0.02%/0.02 Degrees
- Low Supply Current 10mA
- Fast Output Enable/Disable (HFA1149)

Applications

- Professional Video Processing
- Video Switchers and Routers
- Medical Imaging
- PC Multimedia Systems
- Video Pixel Switching (HFA1149)
- Video Distribution Amplifiers
- Flash Converter Drivers
- Radar/IF Processing

Description

The HFA1109, and HFA1149 are high speed, low power, current feedback amplifiers built with Harris' proprietary complementary bipolar UHF-1 process. These amplifiers feature a unique combination of power and performance specifically tailored for video applications.

The HFA1109 is a standard pinout op amp. It is a higher performance, drop-in replacement (no feedback resistor change required) for the CLC409.

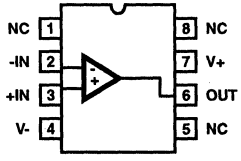
The HFA1149 incorporates an output disable pin which is TTL/CMOS compatible, and user programmable for polarity (active high or low). This feature eliminates the inverter required between amplifiers in multiplexer configurations. The ultra-fast (10ns) enable and disable times make the HFA1149 the obvious choice for pixel switching and other high speed multiplexing applications. The HFA1149 is a high performance, pin compatible upgrade for the popular HA-5020 and HFA1145, as well as the CLC410.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1109IP, HFA1149IP	-40 to 85	8 Ld PDIP	E8.3
HFA1109IB, HFA1149IB (H1109I, H1149I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

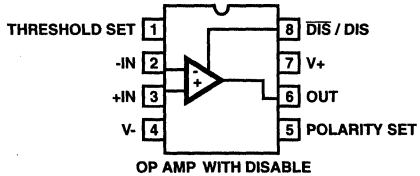
Pinouts

HFA1109 (PDIP, SOIC)
TOP VIEW



OP AMP

HFA1149 (PDIP, SOIC)
TOP VIEW



OP AMP WITH DISABLE

HFA1149 PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
Threshold Set	Optional Logic Thresold Set. Maintains Disable Pin TTL Compatibility with Asymmetrical Supplies (e.g., +10V, 0V).
Polarity Set	Defines Polarity of Disable Input. High or Floating Selects Active Low Disable (i.e., $\overline{DIS}$).
$\overline{DIS}$/DIS	TTL Compatible Disable Input. Output is Driven to a True Hi-Z State When Active. Polarity depends on state of Polarity Set Pin.

HFA1149 DISABLE FUNCTIONALITY

POLARITY SET (PIN 5)	DISABLE (PIN 8)	OUTPUT (PIN 6)
High or Float	High or Float	Enabled
High or Float	Low	Disabled
Low	High or Float	Disabled
Low	Low	Enabled

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **4019.1**

HARRIS SEMICONDUCTOR

HFA1110

750MHz, Low Distortion Unity Gain, Closed Loop Buffer

November 1996

Features

- Wide -3dB Bandwidth 750MHz
- Very Fast Slew Rate..... 1300V/µs
- Fast Settling Time (0.2%) 7ns
- High Output Current 60mA
- Fixed Gain of +1
- Gain Flatness (100MHz)..... 0.03dB
- Differential Phase..... 0.025 Degrees
- Differential Gain..... 0.04%
- 3rd Harmonic Distortion (50MHz)..... -80dBc
- 3rd Order Intercept (100MHz) 30dBm

Applications

- Video Switching and Routing
- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Radar Systems

Description

The HFA1110 is a unity gain closed loop buffer that achieves -3dB bandwidth of 750MHz, while offering excellent video performance and low distortion. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1110 also offers very fast slew rate, and high output current. It is one more example of Harris' intent to enhance its leadership position in products for high speed signal processing applications.

The HFA1110's settling time of 11ns to 0.1%, low distortion and ability to drive capacitive loads make it an ideal flash A/D driver.

The HFA1110 is an enhanced, pin compatible upgrade for the AD9620, AD9630, CLC110, EL2072, BUF600 and BUF601.

For buffer applications requiring a standard op amp pinout, or selectable gain (-1, +1, +2), see the HFA1112 data sheet. For output limiting see the HFA1113 datasheet.

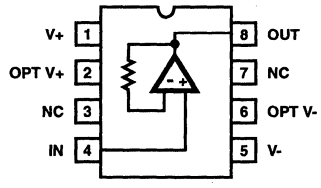
For military grade product please refer to the HFA1110/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1110IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1110IP	-40 to 85	8 Ld PDIP	E8.3
HFA1110IB (H1110I)	-40 to 85	8 Ld SOIC	M8.15
HFA1110EVAL	High Speed Buffer DIP Evaluation Board		

Pinout

HFA1110
(PDIP, CERDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
V+	1	Positive Supply
Opt V+	2	Optional Positive Supply
NC	3	No Connection
IN	4	Input
V-	5	Negative Supply
Opt V-	6	Optional Negative Supply
NC	7	No Connection
OUT	8	Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2944.5**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage . . . . . V_{SUPPLY}
Output Current 60mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	120	35
PDIP Package	98	N/A
SOIC Package	158	N/A

Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±5V, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Output Offset Voltage (Note 2)		25	-	8	25	mV
		Full	-	-	35	mV
Output Offset Voltage Drift		Full	-	10	-	µV/°C
PSRR		25	39	45	-	dB
		Full	35	-	-	dB
Input Noise Voltage (Note 2)	100kHz	25	-	14	-	nV/√Hz
Input Noise Current (Note 2)	100kHz	25	-	51	-	pA/√Hz
Input Bias Current (Note 2)		25	-	10	40	µA
		Full	-	-	65	µA
Input Resistance		25	25	50	-	kΩ
Input Capacitance		25	-	2	-	pF
TRANSFER CHARACTERISTICS						
Gain	V_{OUT} = $2V_{P-P}$	25	0.980	0.990	1.02	V/V
		Full	0.975	-	1.025	V/V
DC Non-Linearity (Note 2)	±2V Full Scale	25	-	0.003	-	%
OUTPUT CHARACTERISTICS						
Output Voltage (Note 2)		25	3.0	3.3	-	±V
		Full	2.5	3.0	-	±V
Output Current (Note 2)	R_L = 50Ω	25, 85	50	60	-	mA
		-40	35	50	-	mA
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	4.5	-	5.5	±V
Supply Current (Note 2)		25	-	21	26	mA
		Full	-	-	33	mA
AC CHARACTERISTICS						
-3dB Bandwidth (Note 2)	V_{OUT} = $0.2V_{P-P}$	25	-	750	-	MHz
Slew Rate	V_{OUT} = $5V_{P-P}$	25	-	1300	-	V/µs
Full Power Bandwidth (Note 2)	V_{OUT} = $4V_{P-P}$	25	-	150	-	MHz
Gain Flatness (Note 2)	To 100MHz	25	-	±0.03	-	dB
	To 30MHz	25	-	±0.01	-	dB
Linear Phase Deviation (Note 2)	DC to 100MHz	25	-	±0.3	-	Degrees
2nd Harmonic Distortion (Note 2)	50MHz, V_{OUT} = $2V_{P-P}$	25	-	-60	-	dBc

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
3rd Harmonic Distortion (Note 2)	50MHz, $V_{OUT} = 2V_{P-P}$	25	-	-80	-	dBc
3rd Order Intercept (Note 2)	100MHz	25	-	30	-	dBm
-1dB Gain Compression	100MHz	25	-	14	-	dBm
Reverse Gain (S_{12}, Note 2)	100MHz, $V_{OUT} = 1V_{P-P}$	25	-	-60	-	dB
TRANSIENT RESPONSE						
Rise Time	$V_{OUT} = 0.5V$ Step	25	-	0.5	-	ns
Overshoot (Note 2)	$V_{OUT} = 1.0V$ Step, Input Signal Rise/Fall = 1ns	25	-	2.5	-	%
0.2% Settling Time (Note 2)	$V_{OUT} = 1V$ to 0V	25	-	7	-	ns
0.1% Settling Time (Note 2)	$V_{OUT} = 1V$ to 0V	25	-	11	-	ns
Overdrive Recovery Time		25	-	15	-	ns
Differential Gain	3.58MHz, $R_L = 75\Omega$	25	-	0.04	-	%
Differential Phase	3.58MHz, $R_L = 75\Omega$	25	-	0.025	-	Degrees

NOTE:

2. See Typical Performance Curves for more information.

Application Information

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

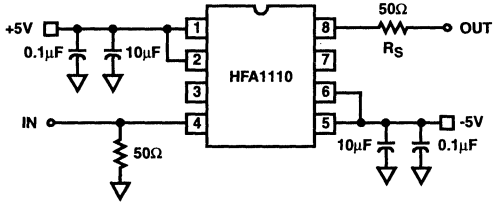
Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output. See the "Recommended RS vs Load Capacitance" graph for specific recommendations.

An example of a good high frequency layout is the Evaluation Board shown below.

Evaluation Board

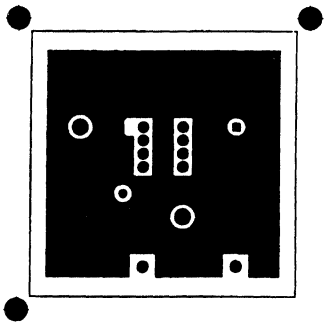
An evaluation board is available for the HFA1110 (part number HFA1110EVAL). Please contact your local sales office for information.

The layout and schematic of the board are shown here:

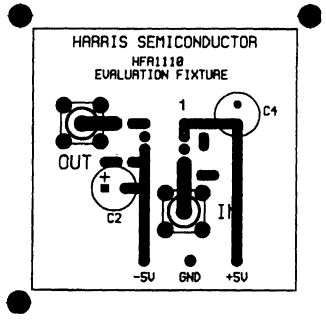


SCHEMATIC DIAGRAM

BOTTOM LAYOUT



TOP LAYOUT



Typical Performance Curves

$V_{SUPPLY} = \pm 5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

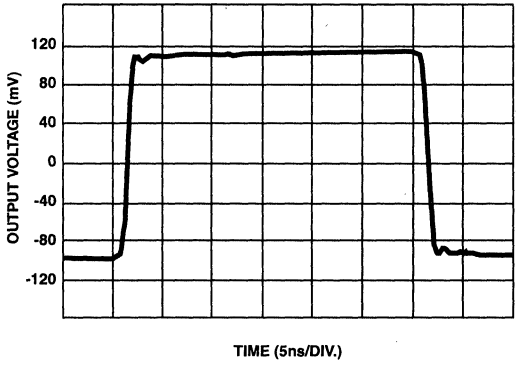


FIGURE 1. SMALL SIGNAL PULSE RESPONSE

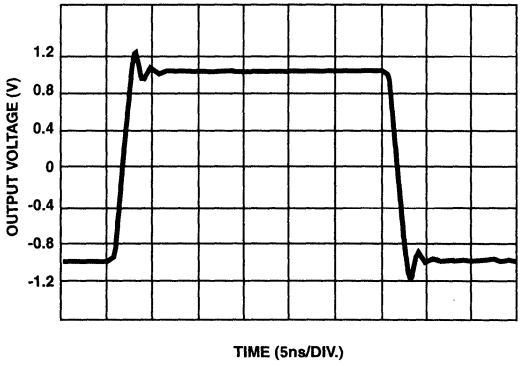


FIGURE 2. LARGE SIGNAL PULSE RESPONSE

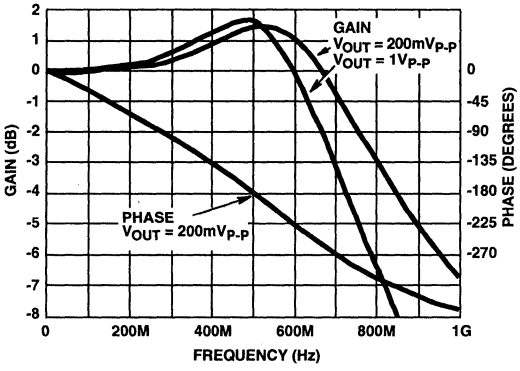


FIGURE 3. FREQUENCY RESPONSE

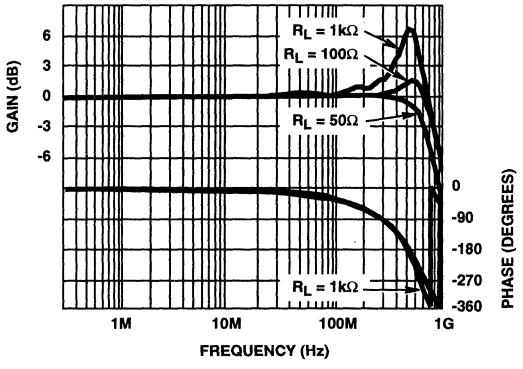


FIGURE 4. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

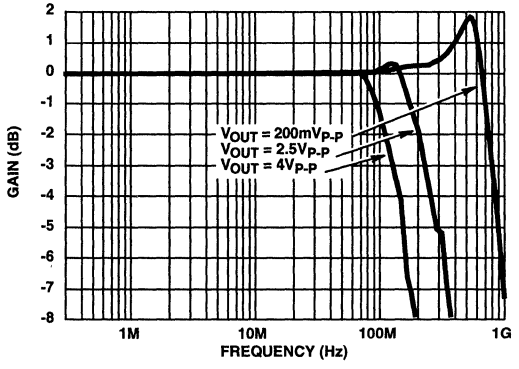


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

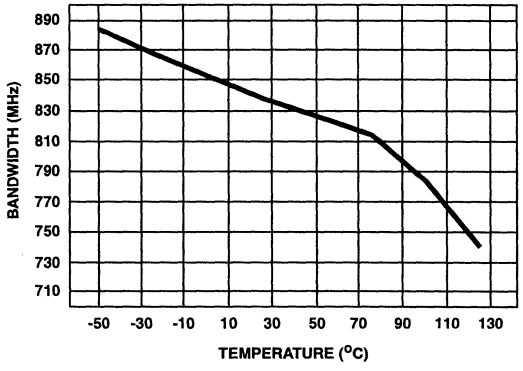


FIGURE 6. -3dB BANDWIDTH vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

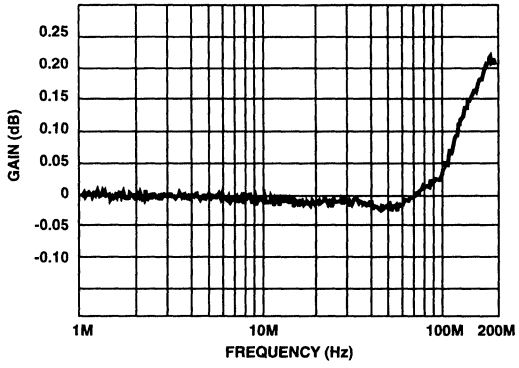


FIGURE 7. GAIN FLATNESS

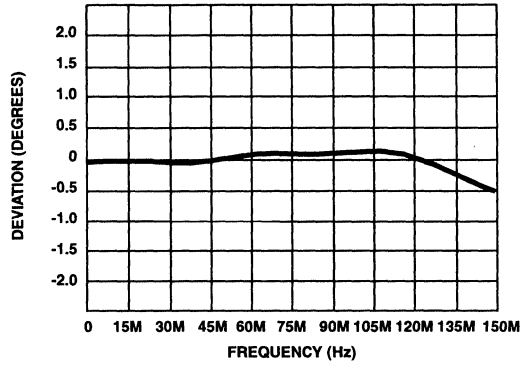


FIGURE 8. DEVIATION FROM LINEAR PHASE

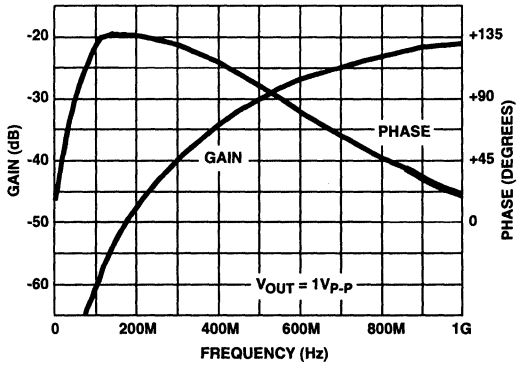


FIGURE 9. REVERSE GAIN AND PHASE (S_{12})

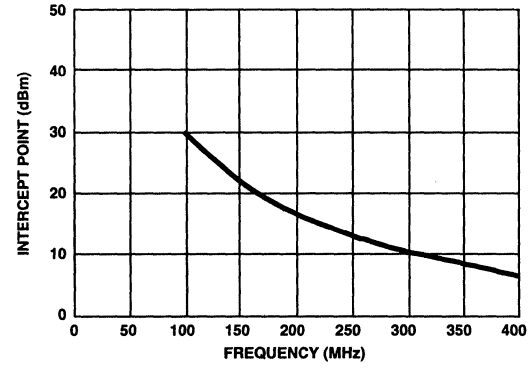


FIGURE 10. TWO-TONE, THIRD ORDER INTERMODULATION INTERCEPT

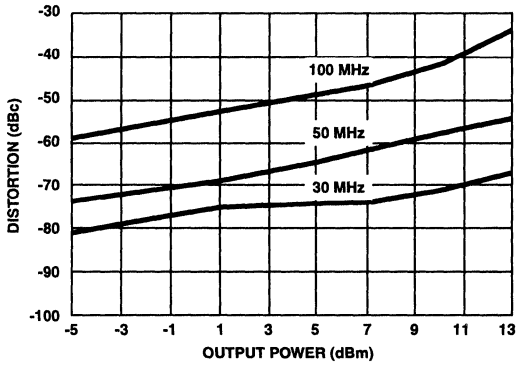


FIGURE 11. SECOND HARMONIC DISTORTION vs P_{OUT}

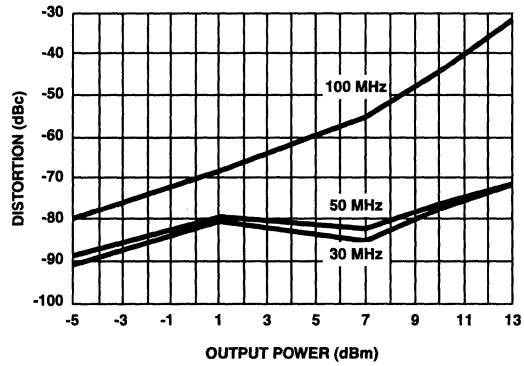


FIGURE 12. THIRD HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

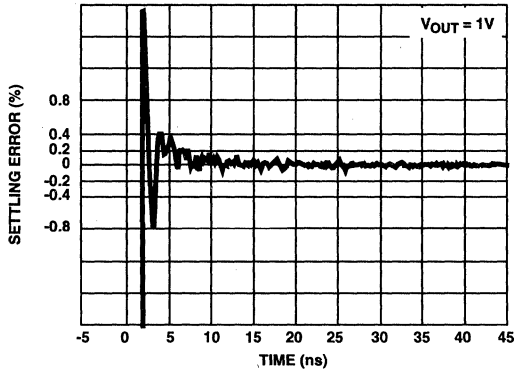


FIGURE 13. SETTLING RESPONSE

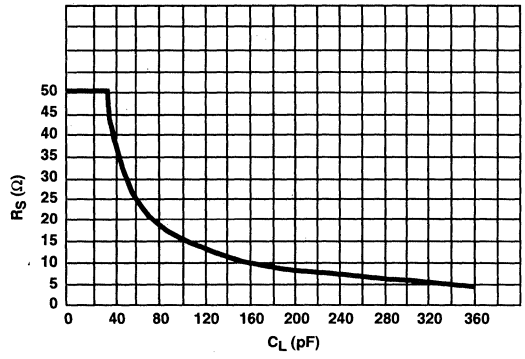


FIGURE 14. RECOMMENDED SERIES OUTPUT RESISTOR vs C_{LOAD}

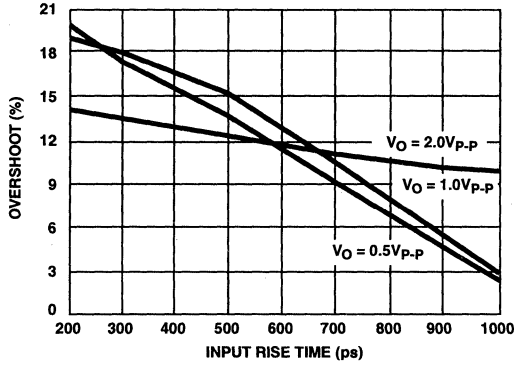


FIGURE 15. OVERSHOOT vs INPUT RISETIME

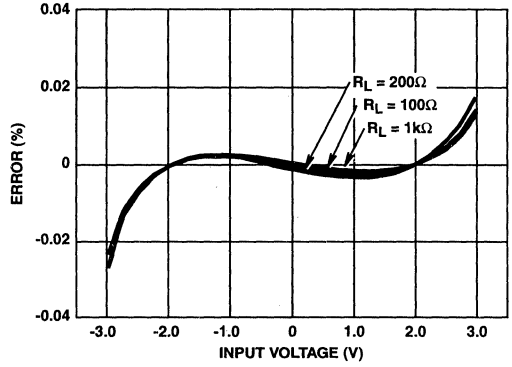


FIGURE 16. INTEGRAL LINEARITY ERROR

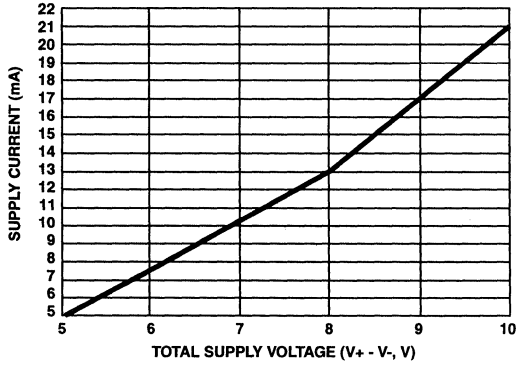


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

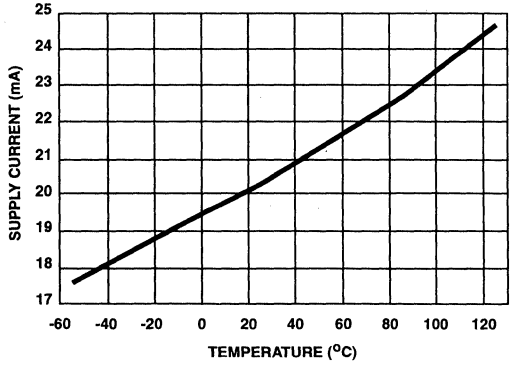


FIGURE 18. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

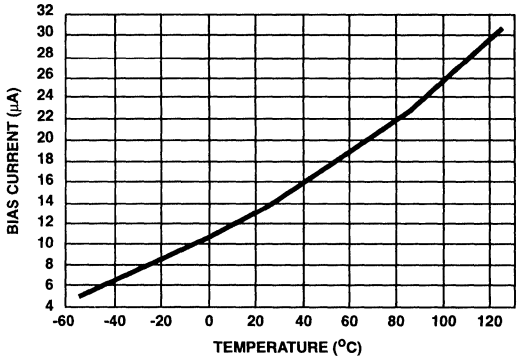


FIGURE 19. BIAS CURRENT vs TEMPERATURE

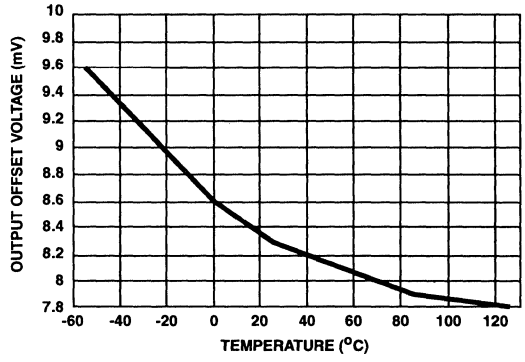


FIGURE 20. OFFSET VOLTAGE vs TEMPERATURE

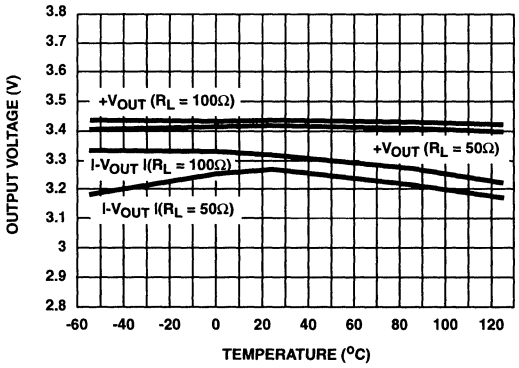


FIGURE 21. OUTPUT VOLTAGE vs TEMPERATURE

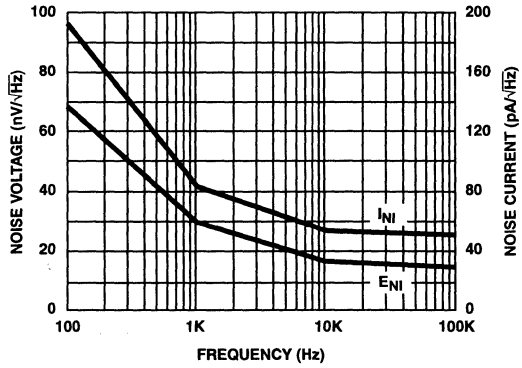


FIGURE 22. INPUT NOISE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

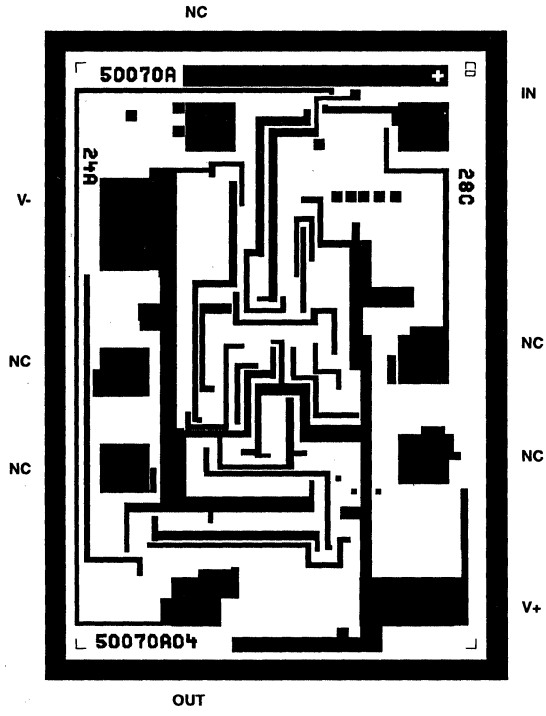
52

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1110



HARRIS SEMICONDUCTOR

HFA1112

850MHz, Low Distortion Programmable Gain Buffer Amplifier

November 1996

Features

- User Programmable for Closed-Loop Gains of +1, -1 or +2 without Use of External Resistors
- Wide -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2400V/µs
- Fast Settling Time (0.1%) 11ns
- High Output Current 60mA
- Excellent Gain Accuracy 0.99V/V
- Overdrive Recovery ..... <10ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems
- Related Literature
  - AN9507, Video Cable Drivers Save Board Space

Description

The HFA1112 is a closed loop Buffer featuring user programmable gain and ultra high speed performance. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1112 offers a wide -3dB bandwidth of 850MHz, very fast slew rate, excellent gain flatness, low distortion and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

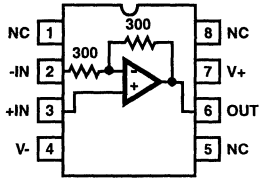
This amplifier is available with programmable output limiting as the HFA1113. For applications requiring a standard buffer pinout, please refer to the HFA1110 datasheet. For Military product, refer to the HFA1112/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1112IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1112IP	-40 to 85	8 Ld PDIP	E8.3
HFA1112IB (H1112I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HFA1112
(PDIP, CERDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1, 5, 8	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
OUT	6	Output
V+	7	Positive Supply

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage. . . . . V_{SUPPLY}
Output Current 60mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	120	35
PDIP Package	98	N/A
SOIC Package	170	N/A

Maximum Junction Temperature (Ceramic Package and Die) . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Output Offset Voltage		25	-	8	25	mV
		Full	-	-	35	mV
Output Offset Voltage Drift		Full	-	10	-	µV/°C
PSRR		25	39	45	-	dB
		Full	35	-	-	dB
Input Noise Voltage (Note 3)	100kHz	25	-	9	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current (Note 3)	100kHz	25	-	37	-	$pA/\sqrt{Hz}$
Non-Inverting Input Bias Current		25	-	25	40	µA
		Full	-	-	65	µA
Non-Inverting Input Resistance		25	25	50	-	kΩ
Inverting Input Resistance (Note 2)		25	240	300	360	Ω
Input Capacitance		25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±2.8	-	V
TRANSFER CHARACTERISTICS						
Gain	$A_V = +1$, $V_{IN} = +2V$	25	0.980	0.990	1.02	V/V
		Full	0.975	-	1.025	V/V
Gain	$A_V = +2$, $V_{IN} = +1V$	25	1.96	1.98	2.04	V/V
		Full	1.95	-	2.05	V/V
DC Non-Linearity (Note 3)	$A_V = +2$, ±2V Full Scale	25	-	0.02	-	%
OUTPUT CHARACTERISTICS						
Output Voltage (Note 3)	$A_V = -1$	25	±3.0	±3.3	-	V
		Full	±2.5	±3.0	-	V
Output Current (Note 3)	$R_L = 50\Omega$	25, 85	50	60	-	mA
		-40	35	50	-	mA
Closed Loop Output Impedance	DC, $A_V = +2$	25	-	0.3	-	Ω
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current (Note 3)		25	-	21	26	mA
		Full	-	-	33	mA

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS						
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Notes 2, 3)	A_V = -1	25	450	800	-	MHz
	A_V = +1	25	500	850	-	MHz
	A_V = +2	25	350	550	-	MHz
Slew Rate (V_{OUT} = 5V_{P-P}, Note 2)	A_V = -1	25	1500	2400	-	V/µs
	A_V = +1	25	800	1500	-	V/µs
	A_V = +2	25	1100	1900	-	V/µs
Full Power Bandwidth (V_{OUT} = 5V_{P-P}, Note 3)	A_V = -1	25	-	300	-	MHz
	A_V = +1	25	-	150	-	MHz
	A_V = +2	25	-	220	-	MHz
Gain Flatness (to 30MHz, Notes 2, 3)	A_V = -1	25	-	±0.02	-	dB
	A_V = +1	25	-	±0.1	-	dB
	A_V = +2	25	-	±0.015	±0.04	dB
Gain Flatness (to 50MHz, Notes 2, 3)	A_V = -1	25	-	±0.05	-	dB
	A_V = +1	25	-	±0.2	-	dB
	A_V = +2	25	-	±0.036	±0.08	dB
Gain Flatness (to 100MHz, Notes 2, 3)	A_V = -1	25	-	±0.10	-	dB
	A_V = +2	25	-	±0.07	±0.22	dB
Linear Phase Deviation (to 100MHz, Note 3)	A_V = -1	25	-	±0.13	-	Degrees
	A_V = +1	25	-	±0.83	-	Degrees
	A_V = +2	25	-	±0.05	-	Degrees
2nd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-52	-	dBc
	A_V = +1	25	-	-57	-	dBc
	A_V = +2	25	-	-52	-45	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-71	-	dBc
	A_V = +1	25	-	-73	-	dBc
	A_V = +2	25	-	-72	-65	dBc
2nd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-47	-	dBc
	A_V = +1	25	-	-53	-	dBc
	A_V = +2	25	-	-47	-40	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-63	-	dBc
	A_V = +1	25	-	-68	-	dBc
	A_V = +2	25	-	-65	-55	dBc
2nd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-41	-	dBc
	A_V = +1	25	-	-50	-	dBc
	A_V = +2	25	-	-42	-35	dBc
3rd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-55	-	dBc
	A_V = +1	25	-	-49	-	dBc
	A_V = +2	25	-	-62	-45	dBc
3rd Order Intercept (A_V = +2, Note 3)	100MHz	25	-	28	-	dBm
	300MHz	25	-	13	-	dBm
1dB Compression (A_V = +2, Note 3)	100MHz	25	-	19	-	dBm
	300MHz	25	-	12	-	dBm

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
Reverse Isolation (S_{12}, Note 3)	40MHz	25	-	-70	-	dB
	100MHz	25	-	-60	-	dB
	600MHz	25	-	-32	-	dB
TRANSIENT CHARACTERISTICS						
Rise Time (V_{OUT} = 0.5V Step, Note 2)	$A_V = -1$	25	-	500	800	ps
	$A_V = +1$	25	-	480	750	ps
	$A_V = +2$	25	-	700	1000	ps
Rise Time (V_{OUT} = 2V Step)	$A_V = -1$	25	-	0.82	-	ns
	$A_V = +1$	25	-	1.06	-	ns
	$A_V = +2$	25	-	1.00	-	ns
Overshoot (V_{OUT} = 0.5V Step, Input t_R/t_F = 200ps, Notes 2, 3, 4)	$A_V = -1$	25	-	12	30	%
	$A_V = +1$	25	-	45	65	%
	$A_V = +2$	25	-	6	20	%
0.1% Settling Time (Note 3)	V_{OUT} = 2V to 0V	25	-	11	-	ns
0.05% Settling Time	V_{OUT} = 2V to 0V	25	-	15	-	ns
Overdrive Recovery Time	$V_{IN} = 5V_{P-P}$	25	-	8.5	-	ns
Differential Gain	$A_V = +1$, 3.58MHz, $R_L = 150\Omega$	25	-	0.03	-	%
	$A_V = +2$, 3.58MHz, $R_L = 150\Omega$	25	-	0.02	-	%
Differential Phase	$A_V = +1$, 3.58MHz, $R_L = 150\Omega$	25	-	0.05	-	Degrees
	$A_V = +2$, 3.58MHz, $R_L = 150\Omega$	25	-	0.04	-	Degrees

NOTES:

2. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
3. See Typical Performance Curves for more information.
4. Overshoot decreases as input transition times increase, especially for $A_V = +1$. Please refer to Typical Performance Curves.

Application Information

Closed Loop Gain Selection

The HFA1112 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 50Ω, C_L = 30pF, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at A_V = +1, R_S = 5Ω, C_L = 340pF.

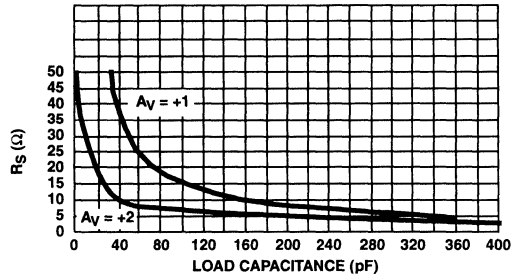


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1112 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R_2), and leave the connection open.
2. a. For A_V = +1 evaluation, remove the 500Ω gain setting resistor (R_1), and leave pin 2 floating.
   b. For A_V = +2, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

The layout and modified schematic of the board are shown in Figure 2.

To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

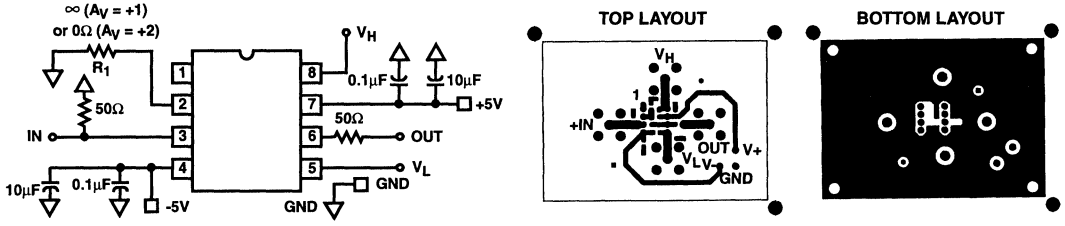


FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

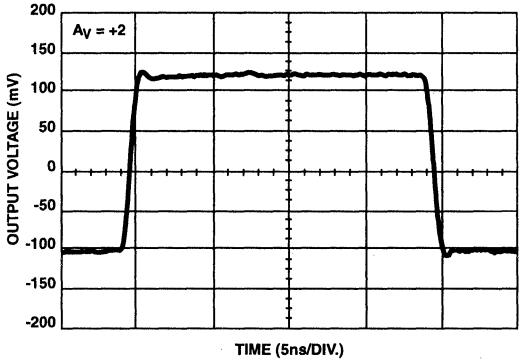


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

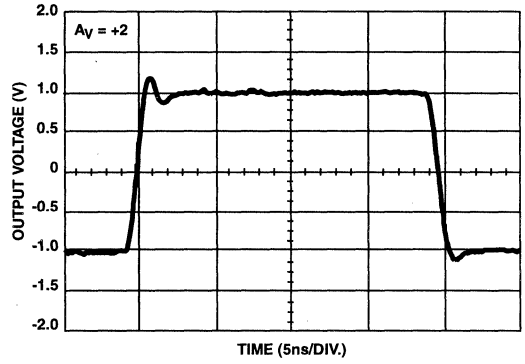


FIGURE 4. LARGE SIGNAL PULSE RESPONSE

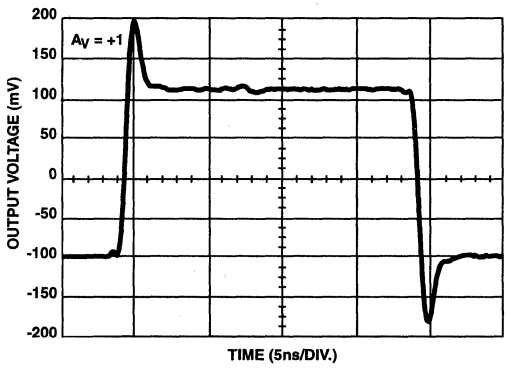


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

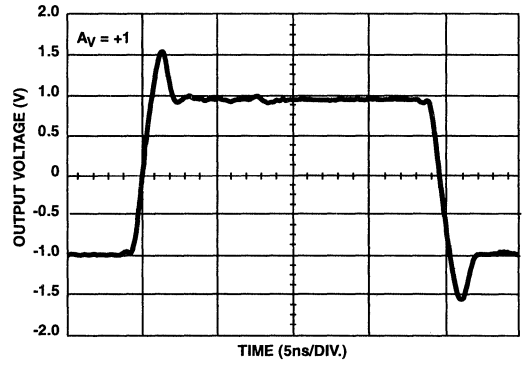


FIGURE 6. LARGE SIGNAL PULSE RESPONSE

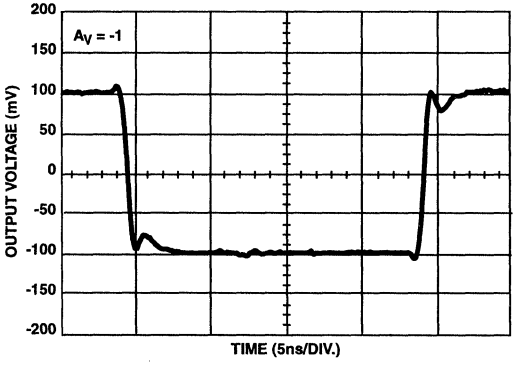


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

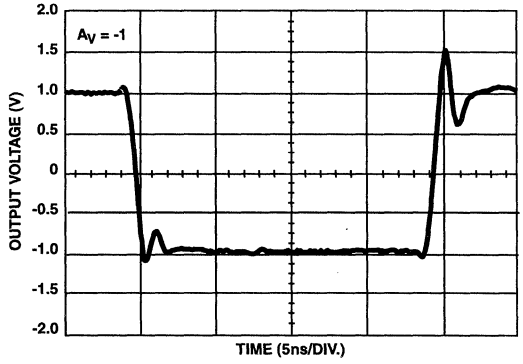


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

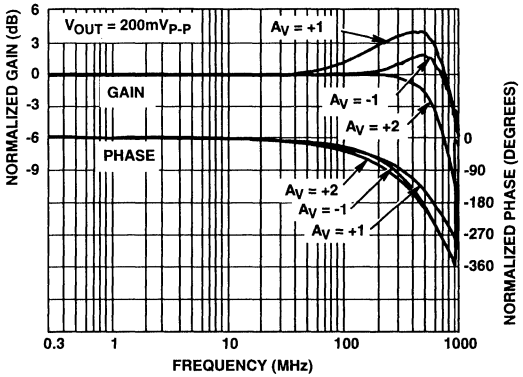


FIGURE 9. FREQUENCY RESPONSE

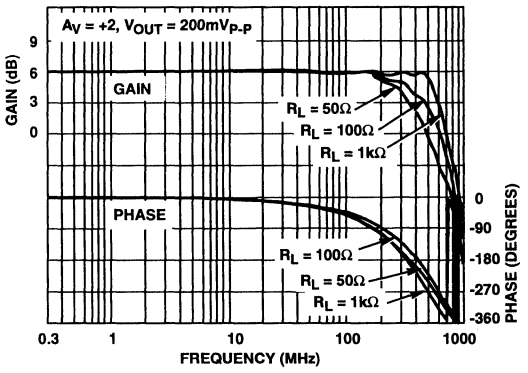


FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

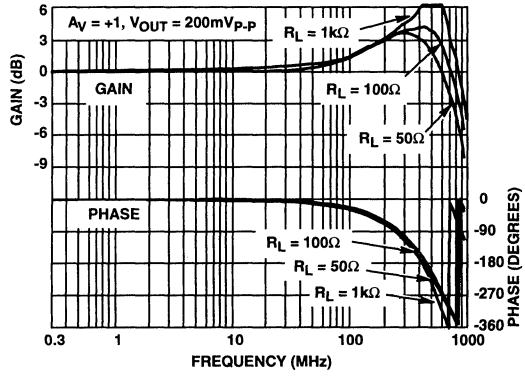


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

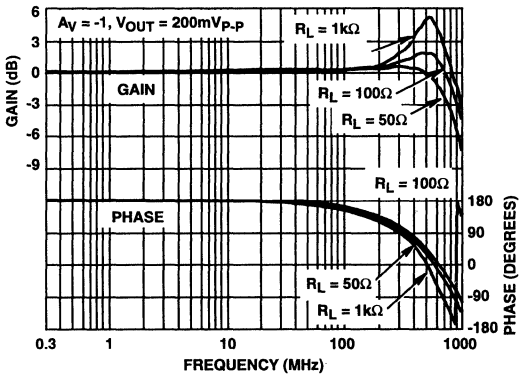


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

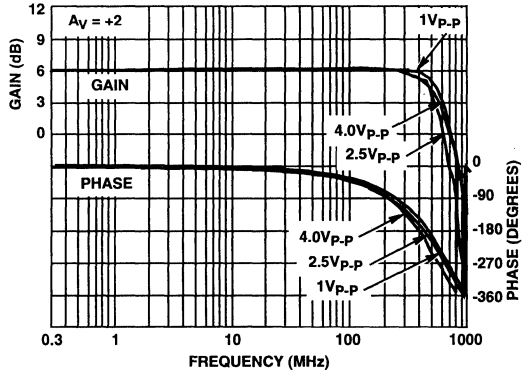


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

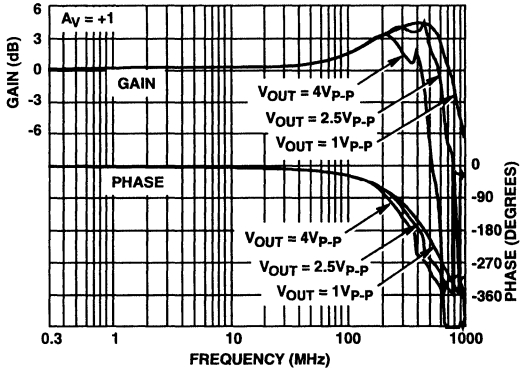


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

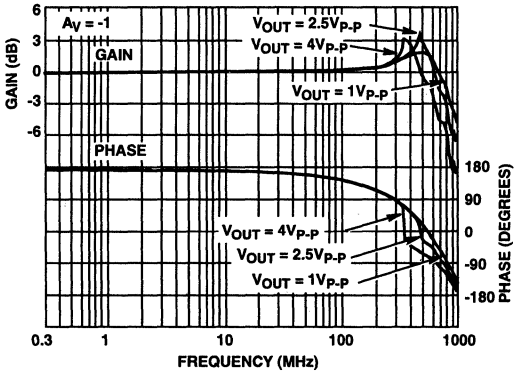


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

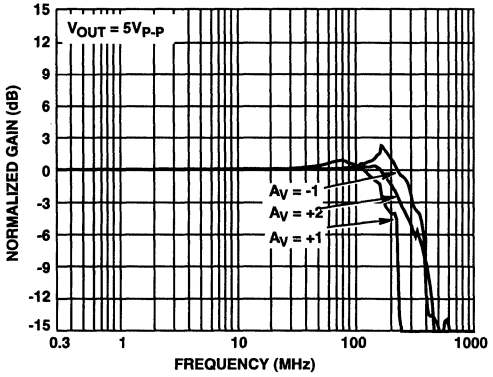


FIGURE 16. FULL POWER BANDWIDTH

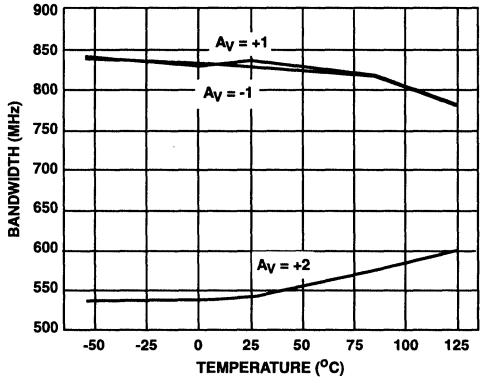


FIGURE 17. -3dB BANDWIDTH vs TEMPERATURE

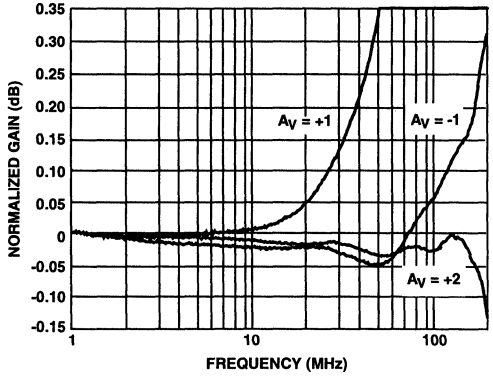


FIGURE 18. GAIN FLATNESS

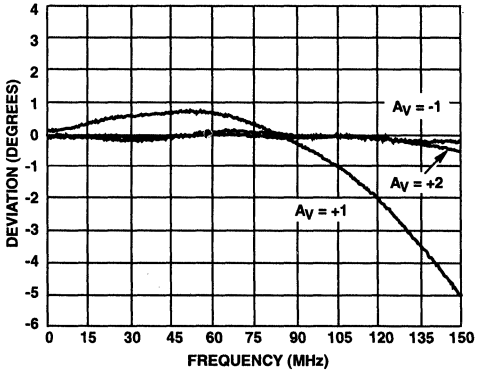


FIGURE 19. DEVIATION FROM LINEAR PHASE

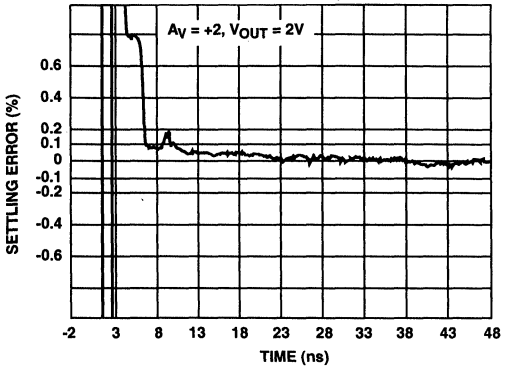


FIGURE 20. SETTLING RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

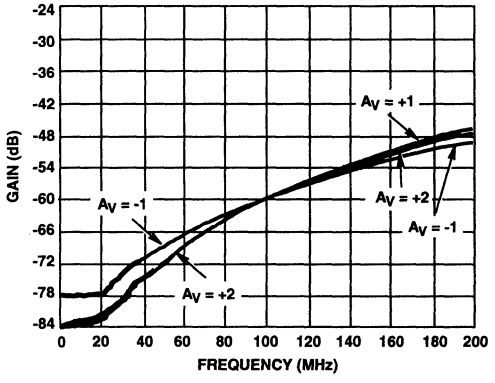


FIGURE 21. LOW FREQUENCY REVERSE ISOLATION (S_{12})

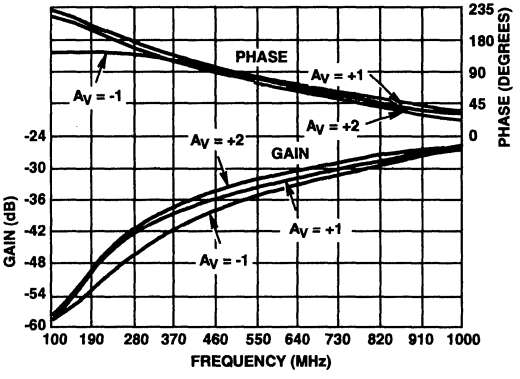


FIGURE 22. HIGH FREQUENCY REVERSE ISOLATION (S_{12})

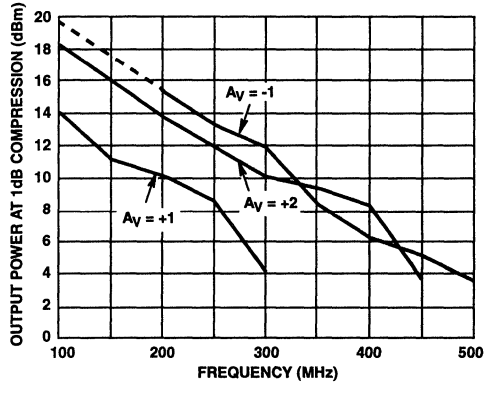


FIGURE 23. 1dB GAIN COMPRESSION vs FREQUENCY

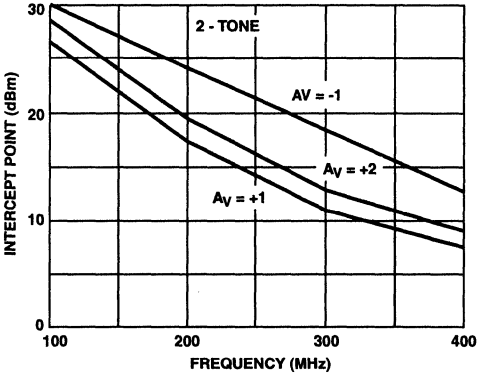


FIGURE 24. 3rd ORDER INTERMODULATION INTERCEPT vs FREQUENCY

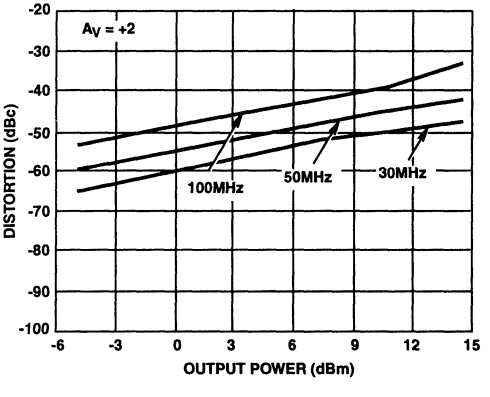


FIGURE 25. 2nd HARMONIC DISTORTION vs P_{OUT}

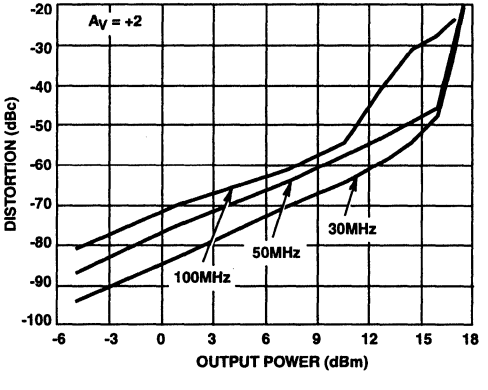


FIGURE 26. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

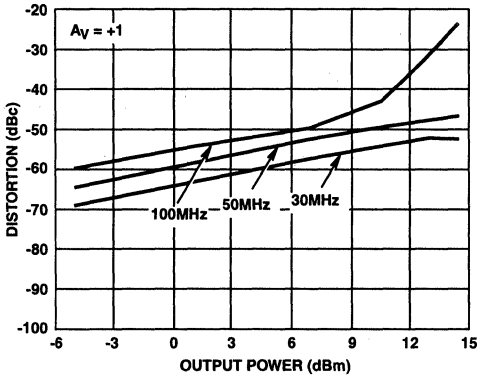


FIGURE 27. 2nd HARMONIC DISTORTION vs P_{OUT}

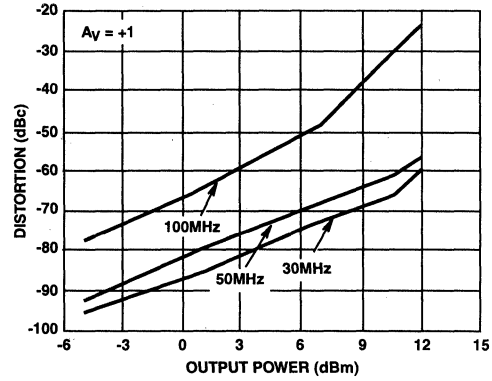


FIGURE 28. 3rd HARMONIC DISTORTION vs P_{OUT}

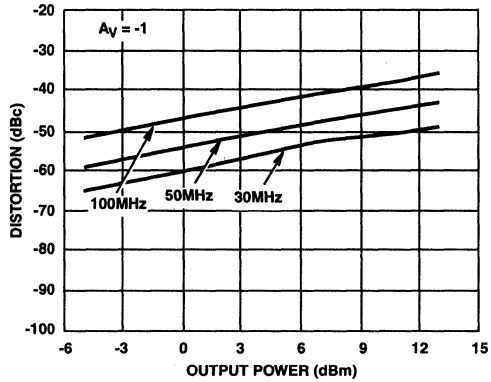


FIGURE 29. 2nd HARMONIC DISTORTION vs P_{OUT}

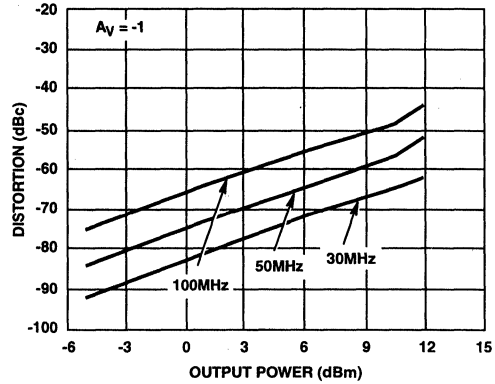


FIGURE 30. 3rd HARMONIC DISTORTION vs P_{OUT}

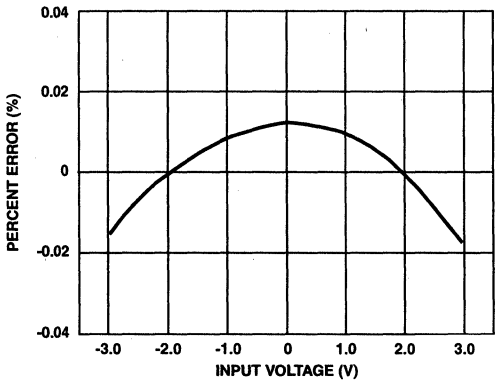


FIGURE 31. INTEGRAL LINEARITY ERROR

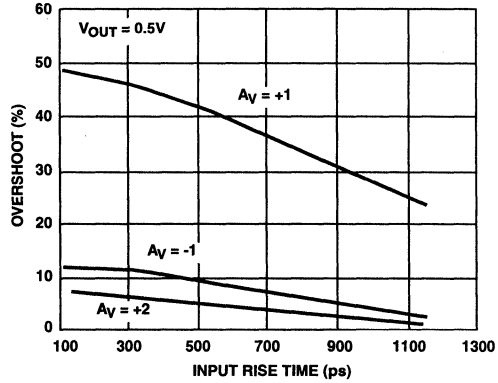


FIGURE 32. OVERSHOOT vs INPUT RISE TIME

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

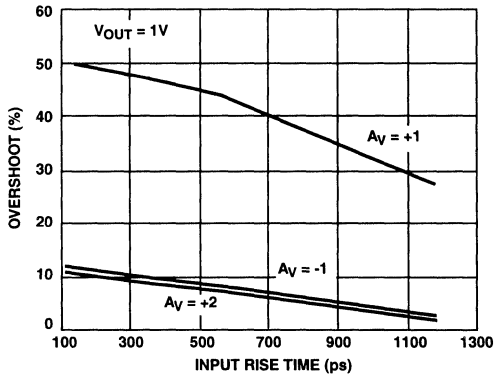


FIGURE 33. OVERSHOOT vs INPUT RISE TIME

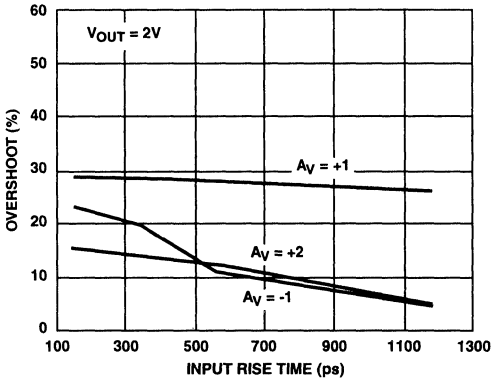


FIGURE 34. OVERSHOOT vs INPUT RISE TIME

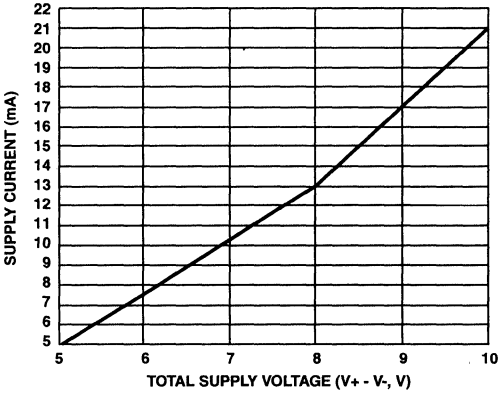


FIGURE 35. SUPPLY CURRENT vs SUPPLY VOLTAGE

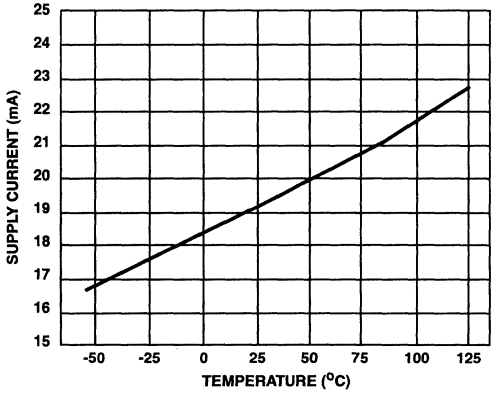


FIGURE 36. SUPPLY CURRENT vs TEMPERATURE

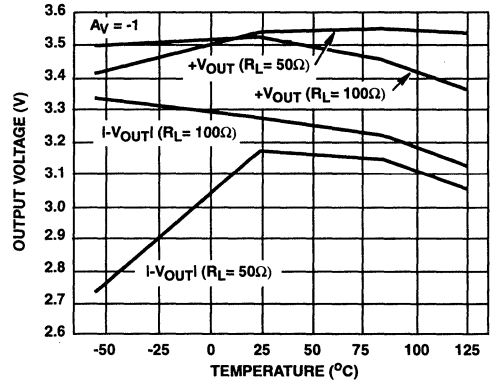


FIGURE 37. OUTPUT VOLTAGE vs TEMPERATURE

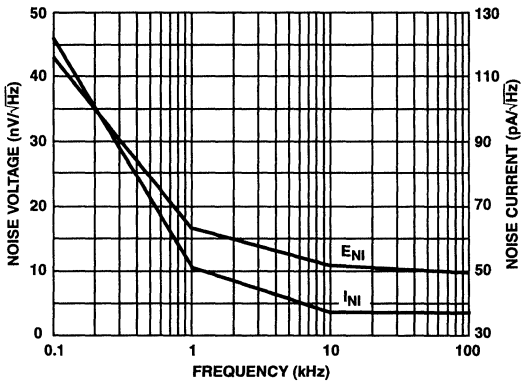


FIGURE 38. INPUT NOISE CHARACTERISTICS

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm 483µm

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

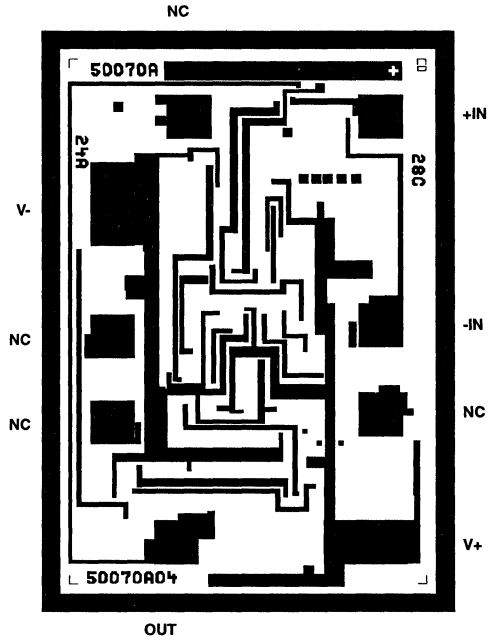
52

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1112



HARRIS SEMICONDUCTOR

HFA1113

850MHz, Low Distortion, Output Limiting, Programmable Gain, Buffer Amplifier

November 1996

Features

- User Programmable Output Voltage Limiting
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Wide -3dB Bandwidth 850MHz
- Excellent Gain Flatness (to 100MHz) ..... ±0.07dB
- Low Differential Gain and Phase.... 0.02%/0.04 Degrees
- Low Distortion (HD3, 30MHz) ..... -73dBc
- Very Fast Slew Rate 2400V/µs
- Fast Settling Time (0.1%) 13ns
- High Output Current 60mA
- Excellent Gain Accuracy..... 0.99V/V
- Overdrive Recovery..... <1ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems

Description

The HFA1113 is a high speed Buffer featuring user programmable gain and output limiting coupled with ultra high speed performance. This buffer is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. The output limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation following an overdrive condition.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components, as described in the "Application Information" section. Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

Component and composite video systems will also benefit from this buffer's performance, as indicated by the excellent gain flatness, and 0.02%/0.04 Degree Differential Gain/Phase specifications (R_L = 150Ω).

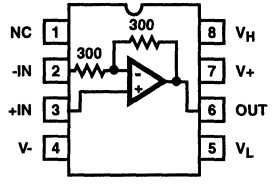
For Military product, refer to the HFA1113/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1113MJ/883	-55 to 125	8 Ld CERDIP	F8.3A
HFA1113IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1113IP	-40 to 85	8 Ld PDIP	E8.3
HFA1113IB (H1113I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board For High Speed Op Amps		

Pinout

HFA1113
(PDIP, CERDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
V_L	5	Lower Output Limit
OUT	6	Output
V+	7	Positive Supply
V_H	8	Upper Output Limit

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1342.3**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage . . . . . V_{SUPPLY}
Voltage at V_H or V_L Terminal . . . . . (V+) + 2V to (V-) - 2V
Output Current (50% Duty Cycle) 60mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	120	35
PDIP Package	98	N/A
SOIC Package	158	N/A

Maximum Junction Temperature (Ceramic Package and Die) . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Output Offset Voltage		25	-	8	25	mV
		Full	-	-	35	mV
Output Offset Voltage Drift		Full	-	10	-	µV/°C
PSRR		25	39	45	-	dB
		Full	35	-	-	dB
Input Noise Voltage (Note 3)	100kHz	25	-	9	-	nV/√Hz
+Input Noise Current (Note 3)	100kHz	25	-	37	-	pA/√Hz
Non-Inverting Input Bias Current		25	-	25	40	µA
		Full	-	-	65	µA
Non-Inverting Input Resistance		25	25	50	-	kΩ
Inverting Input Resistance (Note 2)		25	240	300	360	Ω
Input Capacitance		25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±2.8	-	V
TRANSFER CHARACTERISTICS						
Gain	A_V = +1, V_{IN} = +2V	25	0.980	0.990	1.020	V/V
		Full	0.975	-	1.025	V/V
	A_V = +2, V_{IN} = +1V	25	1.96	1.98	2.04	V/V
		Full	1.95	-	2.05	V/V
DC Non-Linearity (Note 3)	A_V = +2, ±2V Full Scale	25	-	0.02	-	%
OUTPUT CHARACTERISTICS						
Output Voltage (Note 3)	A_V = -1	25	±3.0	±3.3	-	V
		Full	±2.5	±3.0	-	V
Output Current (Note 3)	R_L = 50Ω	25, 85	50	60	-	mA
		-40	35	50	-	mA
Closed Loop Output Impedance	DC, A_V = +2	25	-	0.3	-	Ω
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current (Note 3)		25	-	21	26	mA
		Full	-	-	33	mA
AC CHARACTERISTICS						
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Notes 2, 3)	A_V = -1	25	450	800	-	MHz
	A_V = +1	25	500	850	-	MHz
	A_V = +2	25	350	550	-	MHz

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Slew Rate (V_{OUT} = 5V_{P-P}, Note 2)	A_V = -1	25	1500	2400	-	V/µs
	A_V = +1	25	800	1500	-	V/µs
	A_V = +2	25	1100	1900	-	V/µs
Full Power Bandwidth (V_{OUT} = 5V_{P-P}, Note 3)	A_V = -1	25	-	300	-	MHz
	A_V = +1	25	-	150	-	MHz
	A_V = +2	25	-	220	-	MHz
Gain Flatness (to 30MHz, Notes 2, 3)	A_V = -1	25	-	±0.02	-	dB
	A_V = +1	25	-	±0.1	-	dB
	A_V = +2	25	-	±0.015	±0.04	dB
Gain Flatness (to 50MHz, Notes 2, 3)	A_V = -1	25	-	±0.05	-	dB
	A_V = +1	25	-	±0.2	-	dB
	A_V = +2	25	-	±0.036	±0.08	dB
Gain Flatness (to 100MHz, Notes 2, 3)	A_V = -1	25	-	±0.10	-	dB
	A_V = +2	25	-	±0.07	±0.22	dB
Linear Phase Deviation (to 100MHz, Note 3)	A_V = -1	25	-	±0.13	-	Degrees
	A_V = +1	25	-	±0.83	-	Degrees
	A_V = +2	25	-	±0.05	-	Degrees
2nd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-52	-	dBc
	A_V = +1	25	-	-57	-	dBc
	A_V = +2	25	-	-52	-45	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-71	-	dBc
	A_V = +1	25	-	-73	-	dBc
	A_V = +2	25	-	-72	-65	dBc
2nd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-47	-	dBc
	A_V = +1	25	-	-53	-	dBc
	A_V = +2	25	-	-47	-40	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-63	-	dBc
	A_V = +1	25	-	-68	-	dBc
	A_V = +2	25	-	-65	-55	dBc
2nd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-41	-	dBc
	A_V = +1	25	-	-50	-	dBc
	A_V = +2	25	-	-42	-35	dBc
3rd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-55	-	dBc
	A_V = +1	25	-	-49	-	dBc
	A_V = +2	25	-	-62	-45	dBc
3rd Order Intercept (A_V = +2, Note 3)	100MHz	25	-	28	-	dBm
	300MHz	25	-	13	-	dBm
1dB Compression (A_V = +2, Note 3)	100MHz	25	-	19	-	dBm
	300MHz	25	-	12	-	dBm
Reverse Isolation (S_{12}, Note 3)	40MHz	25	-	-70	-	dB
	100MHz	25	-	-60	-	dB
	600MHz	25	-	-32	-	dB
TRANSIENT CHARACTERISTICS						
Rise Time (V_{OUT} = 0.5V Step, Note 2)	A_V = -1	25	-	500	800	ps
	A_V = +1	25	-	480	750	ps
	A_V = +2	25	-	700	1000	ps

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Rise Time (V_{OUT} = 2V Step)	A_V = -1	25	-	0.82	-	ns
	A_V = +1	25	-	1.06	-	ns
	A_V = +2	25	-	1.00	-	ns
Overshoot (V_{OUT} = 0.5V Step, Input t_R/t_F = 200ps, Notes 2, 3, 4)	A_V = -1	25	-	12	30	%
	A_V = +1	25	-	45	65	%
	A_V = +2	25	-	6	20	%
0.1% Settling Time (Note 3)	V_{OUT} = 2V to 0V	25	-	13	20	ns
0.05% Settling Time	V_{OUT} = 2V to 0V	25	-	20	33	ns
Differential Gain	A_V = +1, 3.58MHz, R_L = 150Ω	25	-	0.03	-	%
	A_V = +2, 3.58MHz, R_L = 150Ω	25	-	0.02	-	%
Differential Phase	A_V = +1, 3.58MHz, R_L = 150Ω	25	-	0.05	-	Degrees
	A_V = +2, 3.58MHz, R_L = 150Ω	25	-	0.04	-	Degrees
OUTPUT LIMITING CHARACTERISTICS	A_V = +2, V_H = +1V, V_L = -1V, Unless Otherwise Specified					
Clamp Accuracy (Note 3)	V_{IN} = ±1.6V, A_V = -1	25	-	±100	±150	mV
		Full	-	-	±200	mV
Clamp Overshoot	V_{IN} = ±1V, Input t_R/t_F = 500ps	25	-	7	-	%
Overdrive Recovery Time (Note 3)	V_{IN} = ±1V	25	-	0.75	1.5	ns
Negative Clamp Range		25	-	-5.0 to +2.0	-	V
Positive Clamp Range		25	-	-2.0 to +5.0	-	V
Clamp Input Bias Current (Note 3)		25	-	50	200	µA
		Full	-	-	300	µA
Clamp Input Bandwidth (Note 3)	V_H or V_L = 100mV_{P-P}	25	-	500	-	MHz

NOTES:

2. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
3. See Typical Performance Curves for more information.
4. Overshoot decreases as input transition times increase, especially for A_V = +1. Please refer to Typical Performance Curves.

Application Information

Closed Loop Gain Selection

The HFA1113 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±Inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

	CONNECTIONS	
GAIN (A_{CL})	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at $A_V = +1$, $R_S = 50\Omega$, $C_L = 30pF$, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at $A_V = +1$, $R_S = 5\Omega$, $C_L = 340pF$.

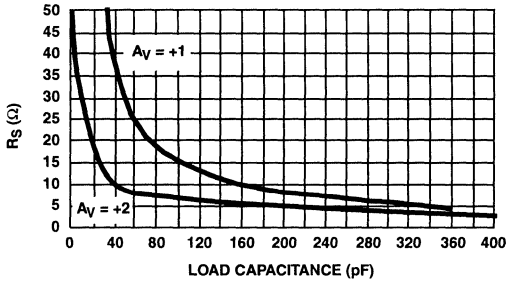


FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1113 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R_2), and leave the connection open.
2. a. For $A_V = +1$ evaluation, remove the 500Ω gain setting resistor (R_1), and leave pin 2 floating.
   b. For $A_V = +2$, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

The modified schematic and layout of the board are shown in Figures 2 and 3.

To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

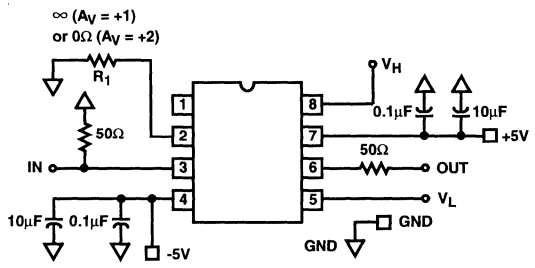


FIGURE 2. MODIFIED EVALUATION BOARD SCHEMATIC

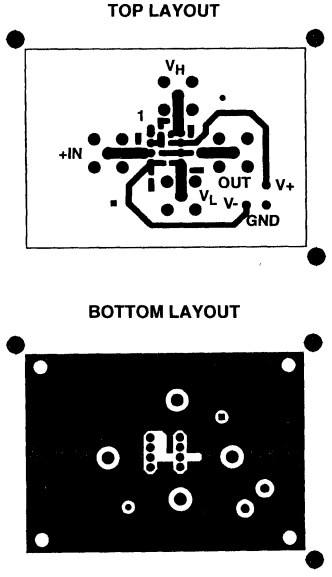


FIGURE 3. EVALUATION BOARD LAYOUT

Limiting Operation

General

The HFA1113 features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Clamp Circuitry

Figure 4 shows a simplified schematic of the HFA1113 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (Q_{X1} - Q_{X2})

between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of:

$(V_{-IN} - V_{OUT})/R_F + V_{-IN}/R_G$

This current is mirrored onto the high impedance node (Z) by Q_{X3}-Q_{X4}, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by Q_{P4} and Q_{N4}. Note that when the output reaches its quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (Q_{N6} and Q_{P6}) to set up the base voltage on Q_{P5}.

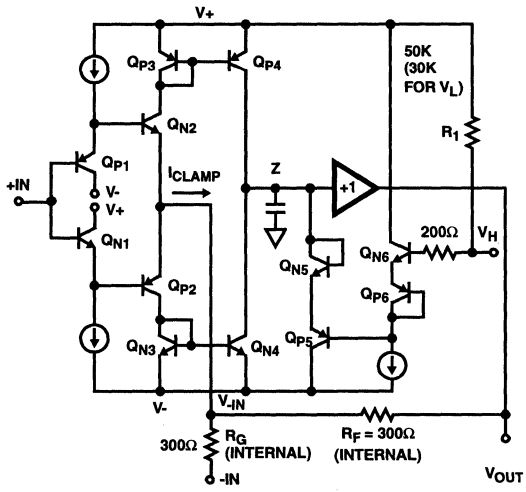


FIGURE 4. HFA1113 SIMPLIFIED V_H CLAMP CIRCUITRY

Q_{P5} begins to conduct whenever the high impedance node reaches a voltage equal to Q_{P5}'s base voltage + $2V_{BE}$ (Q_{P5} and Q_{N5}). Thus, Q_{P5} clamps node Z whenever Z reaches V_H. R_1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. Q_{P5} must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node. The clamping current is calculated as:

$I_{CLAMP} = (V_{-IN} - V_{OUT\ CLAMPED})/300\Omega + V_{-IN}/R_G$.

As an example, a unity gain circuit with V_{IN} = 2V, and V_H = 1V, would have I_{CLAMP} = (2V - 1V)/300Ω + 2V/∞ = 3.33mA ($R_G = \infty$ because -IN is floated for unity gain applications). Note that I_{CC} will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 4, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the Q_{X6} transistors, and the Q_{X5} transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The Q_{X6} transistors are biased at a constant current, but as described earlier, the current through Q_{X5} is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level (A_{VCL} x V_{IN} - $V_{OUT\ CLAMPED}$), so clamp accuracy degrades as the overdrive increases. As an example, the specified accuracy of ±100mV (A_V = -1, V_H = 1V) for a 1.6X overdrive degrades to ±240mV for a 3X (200%) overdrive, as shown in Figure 43.

Consideration must also be given to the fact that the clamp voltages have an affect on amplifier linearity. The "Nonlinearity Near Clamp Voltage" curve, Figure 48, illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1113 could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won't be in a DC output voltage from an AC input signal. A 150mV - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP}/A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of "Unclamped Performance" and "Clamped Performance" (Figures 41 and 42) highlight the HFA1113's subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 8.0ns for the unclamped pulse, and 8.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HFA1113 propagation delay is 500ps.

Overdrive recovery time is also a function of the overdrive level. Figure 47 details the overdrive recovery time for various clamp and overdrive levels.

Typical Performance Curves

$V_{SUPPLY} = \pm 5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

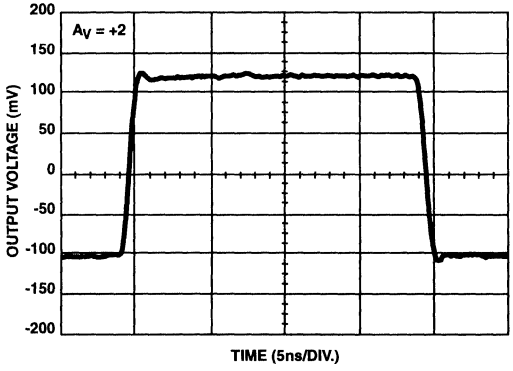


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

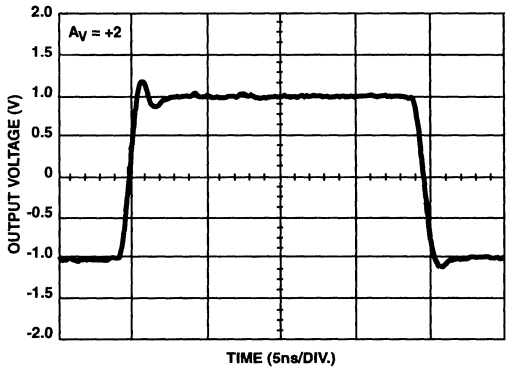


FIGURE 6. LARGE SIGNAL PULSE RESPONSE

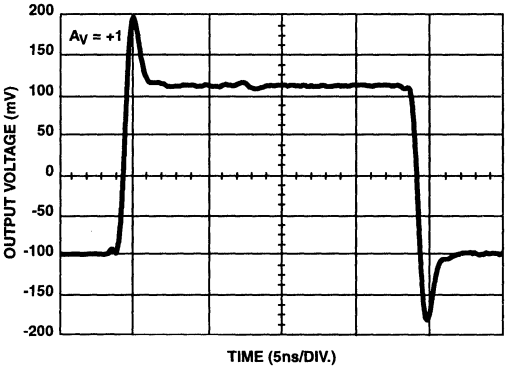


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

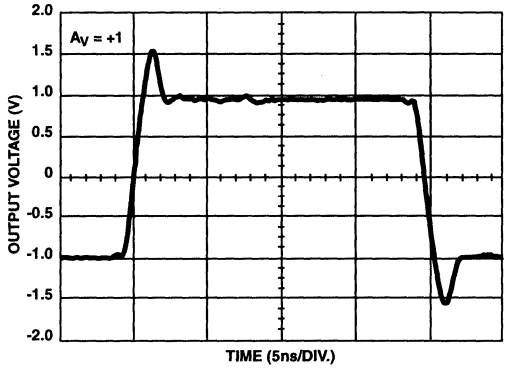


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

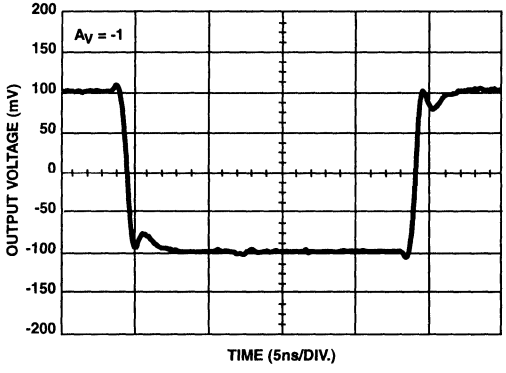


FIGURE 9. SMALL SIGNAL PULSE RESPONSE

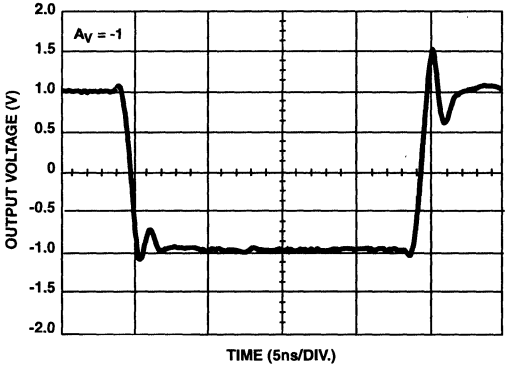


FIGURE 10. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

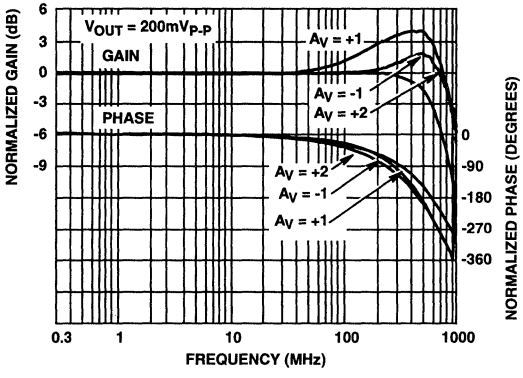


FIGURE 11. FREQUENCY RESPONSE

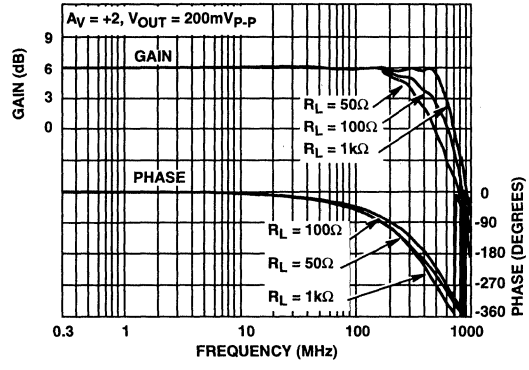


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

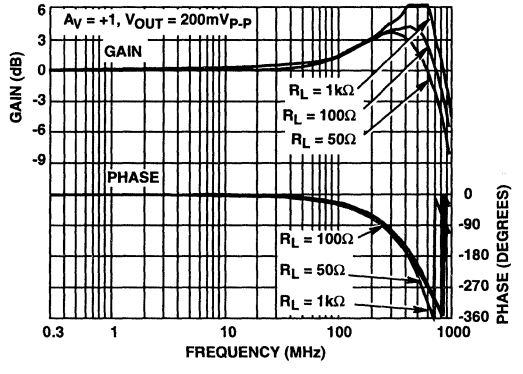


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

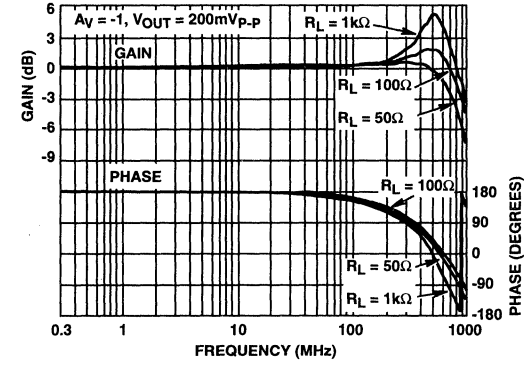


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

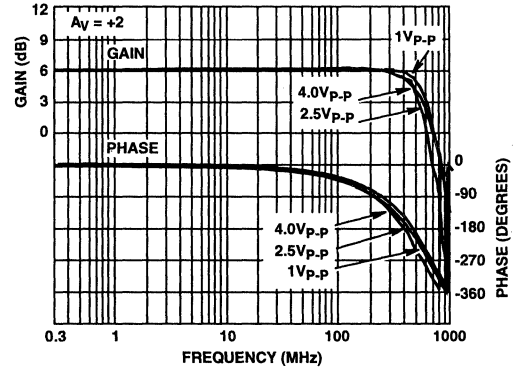


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

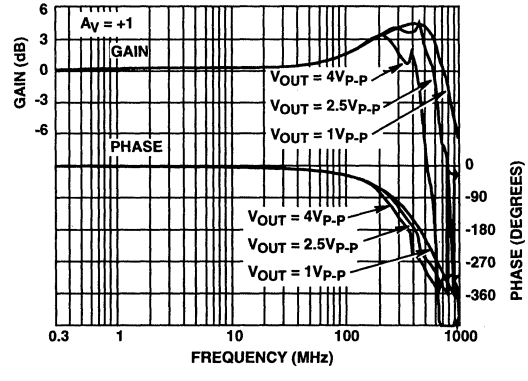


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

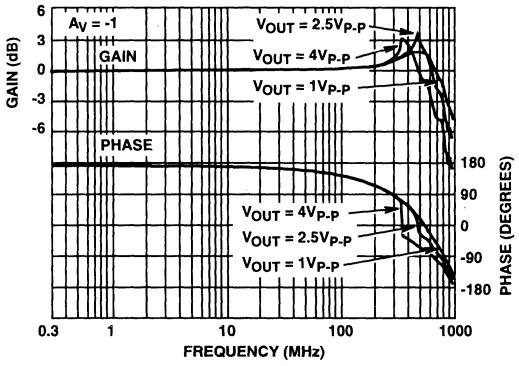


FIGURE 17. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

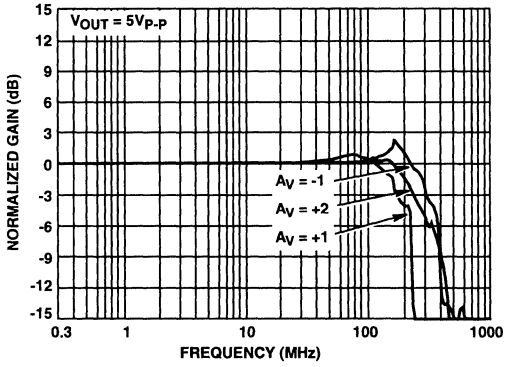


FIGURE 18. FULL POWER BANDWIDTH

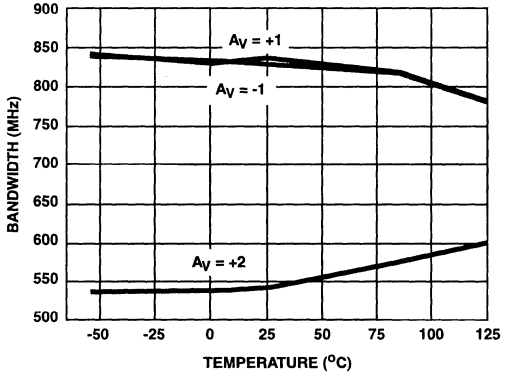


FIGURE 19. -3dB BANDWIDTH vs TEMPERATURE

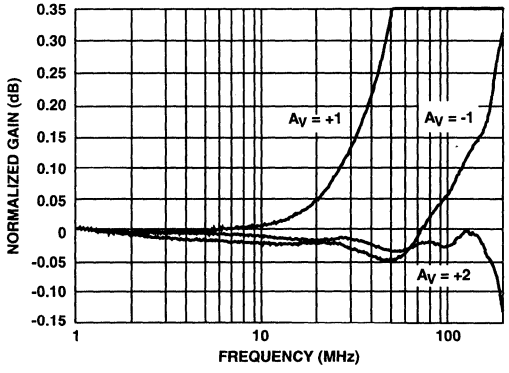


FIGURE 20. GAIN FLATNESS

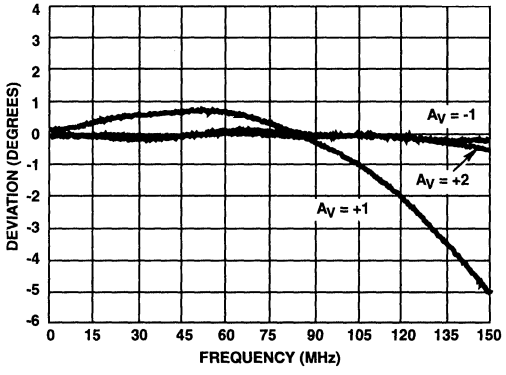


FIGURE 21. DEVIATION FROM LINEAR PHASE

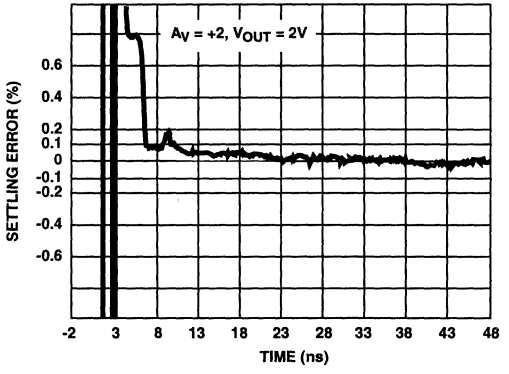


FIGURE 22. SETTLING RESPONSE

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

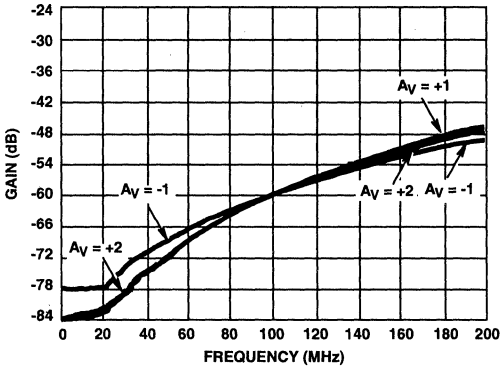


FIGURE 23. LOW FREQUENCY REVERSE ISOLATION (S_{12})

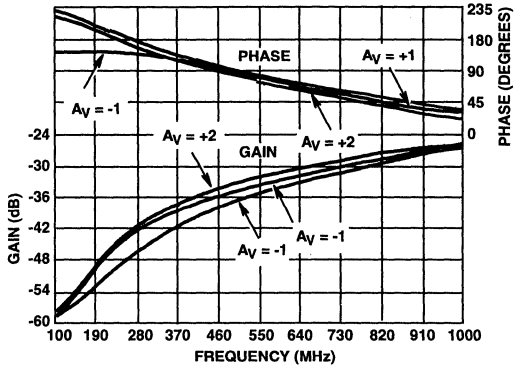


FIGURE 24. HIGH FREQUENCY REVERSE ISOLATION (S_{12})

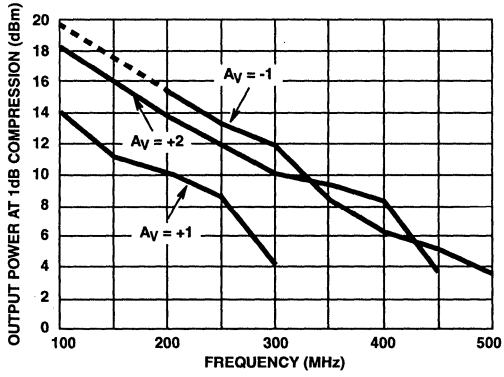


FIGURE 25. 1dB GAIN COMPRESSION vs FREQUENCY

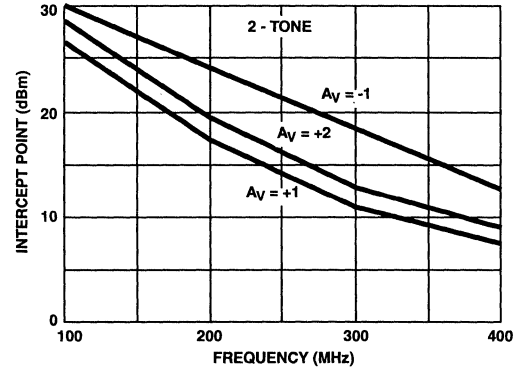


FIGURE 26. THIRD ORDER INTERMODULATION INTERCEPT vs FREQUENCY

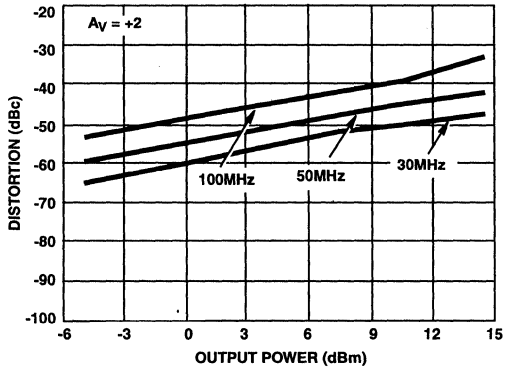


FIGURE 27. SECOND HARMONIC DISTORTION vs P_{OUT}

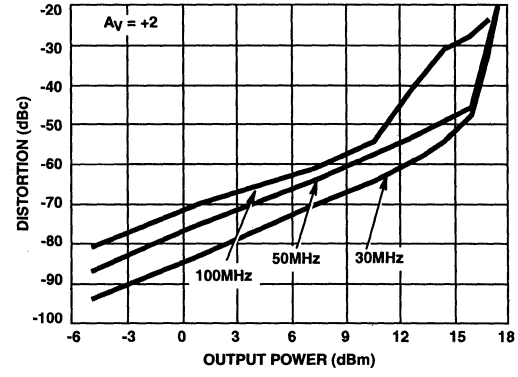


FIGURE 28. THIRD HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

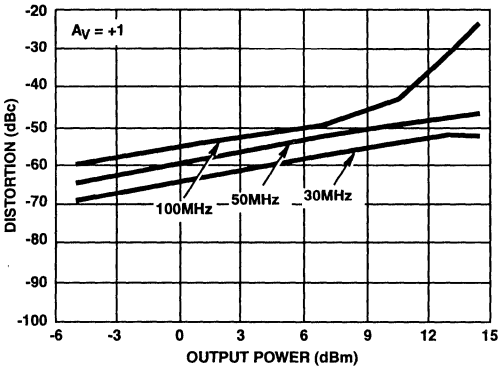


FIGURE 29. SECOND HARMONIC DISTORTION vs P_{OUT}

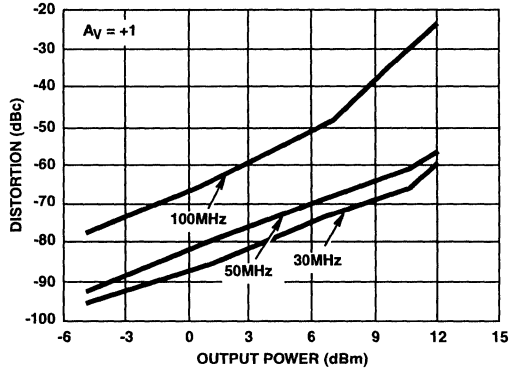


FIGURE 30. THIRD HARMONIC DISTORTION vs P_{OUT}

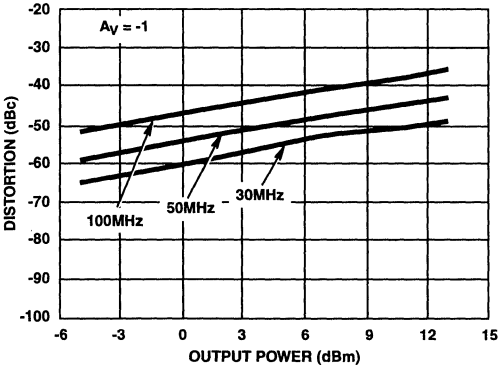


FIGURE 31. SECOND HARMONIC DISTORTION vs P_{OUT}

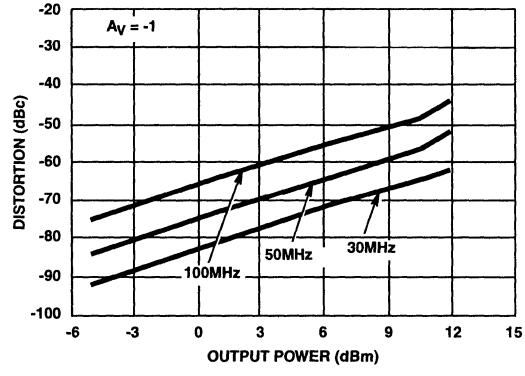


FIGURE 32. THIRD HARMONIC DISTORTION vs P_{OUT}

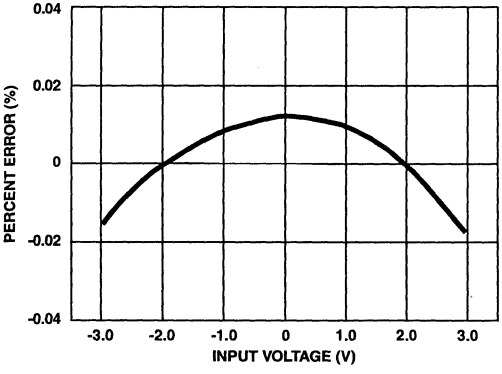


FIGURE 33. INTEGRAL LINEARITY ERROR

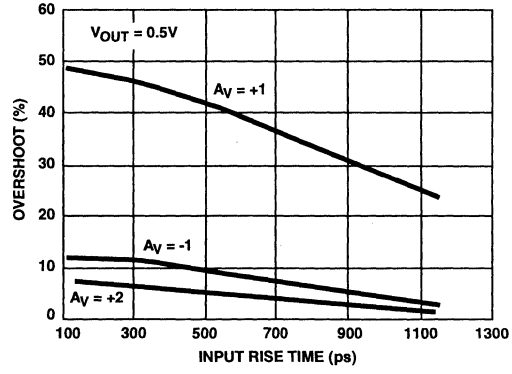


FIGURE 34. OVERSHOOT vs INPUT RISE TIME

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

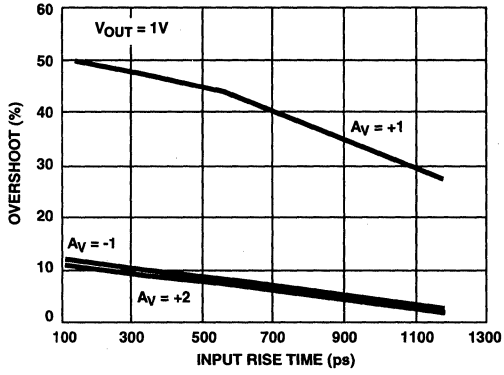


FIGURE 35. OVERSHOOT vs INPUT RISE TIME

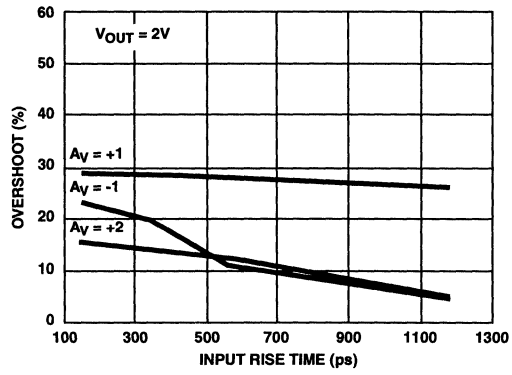


FIGURE 36. OVERSHOOT vs INPUT RISE TIME

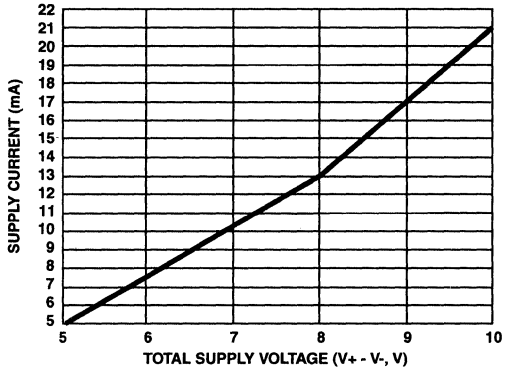


FIGURE 37. SUPPLY CURRENT vs SUPPLY VOLTAGE

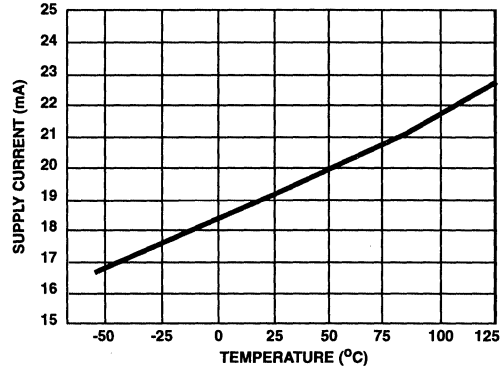


FIGURE 38. SUPPLY CURRENT vs TEMPERATURE

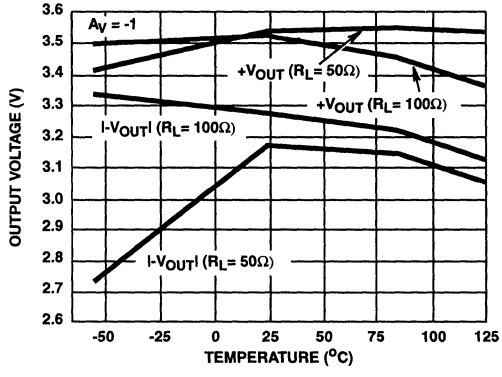


FIGURE 39. OUTPUT VOLTAGE vs TEMPERATURE

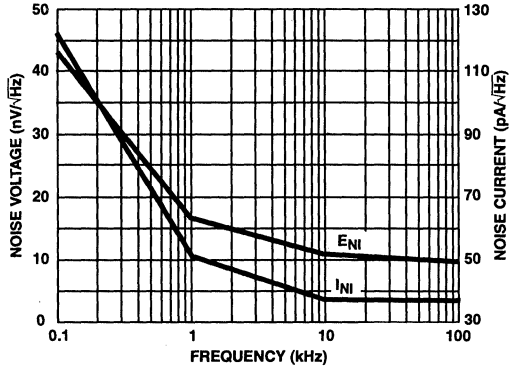


FIGURE 40. INPUT NOISE CHARACTERISTICS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

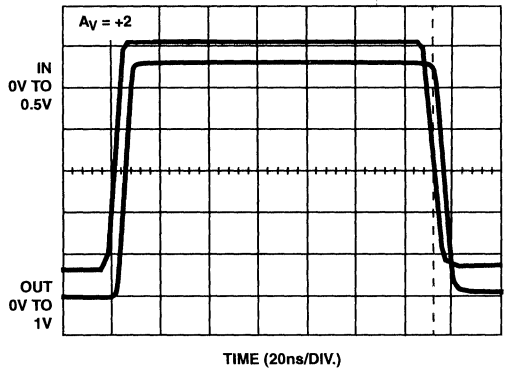


FIGURE 41. UNCLAMPED PERFORMANCE

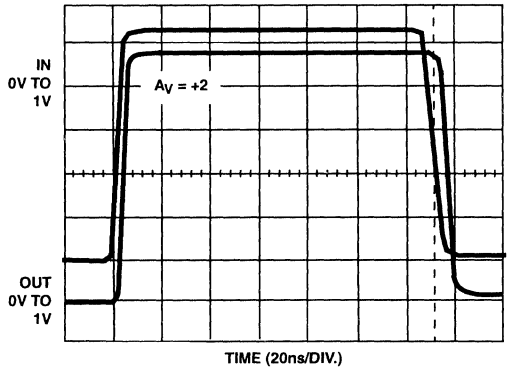


FIGURE 42. CLAMPED PERFORMANCE

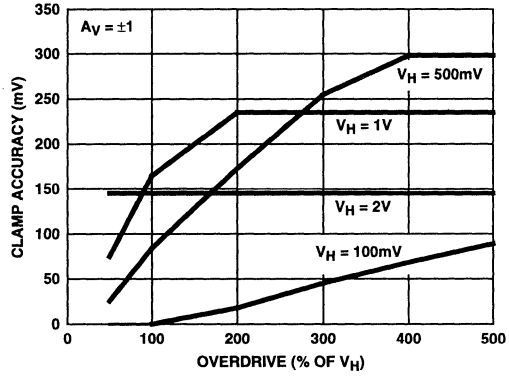


FIGURE 43. V_H CLAMP ACCURACY vs OVERDRIVE

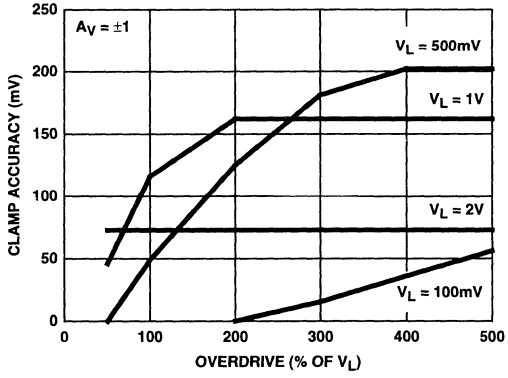


FIGURE 44. V_L CLAMP ACCURACY vs OVERDRIVE

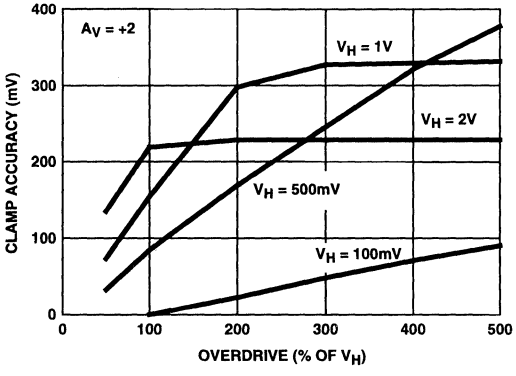


FIGURE 45. V_H CLAMP ACCURACY vs OVERDRIVE

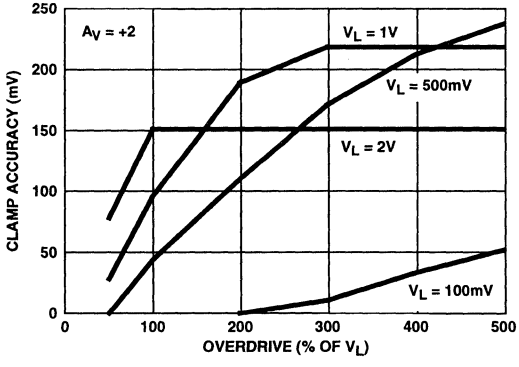


FIGURE 46. V_L CLAMP ACCURACY vs OVERDRIVE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

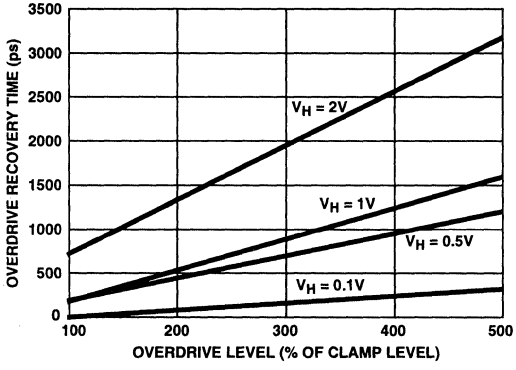


FIGURE 47. OVERDRIVE RECOVERY vs OVERDRIVE

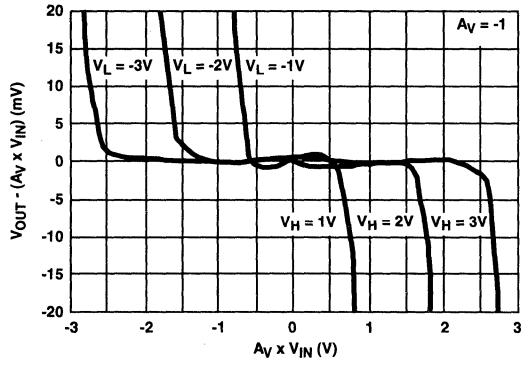


FIGURE 48. NON-LINEARITY NEAR CLAMP VOLTAGE

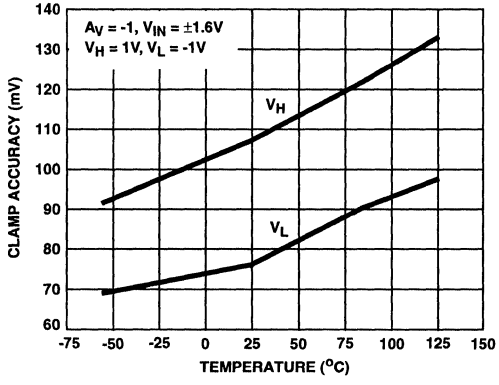


FIGURE 49. CLAMP ACCURACY vs TEMPERATURE

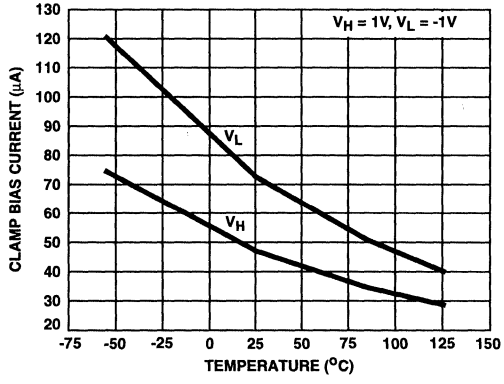


FIGURE 50. CLAMP BIAS CURRENT vs TEMPERATURE

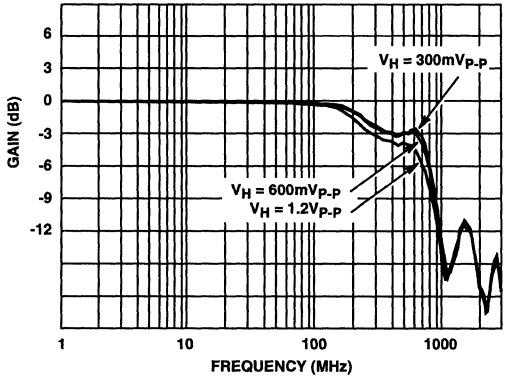


FIGURE 51. V_H CLAMP INPUT BANDWIDTH

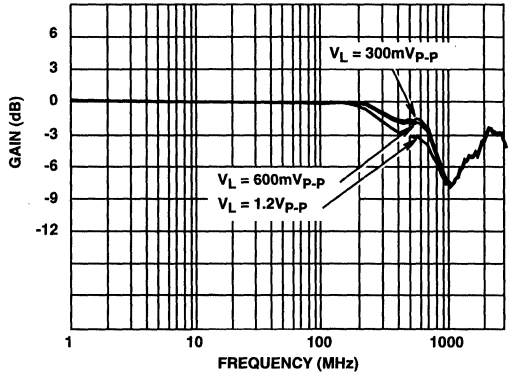


FIGURE 52. V_L CLAMP INPUT BANDWIDTH

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

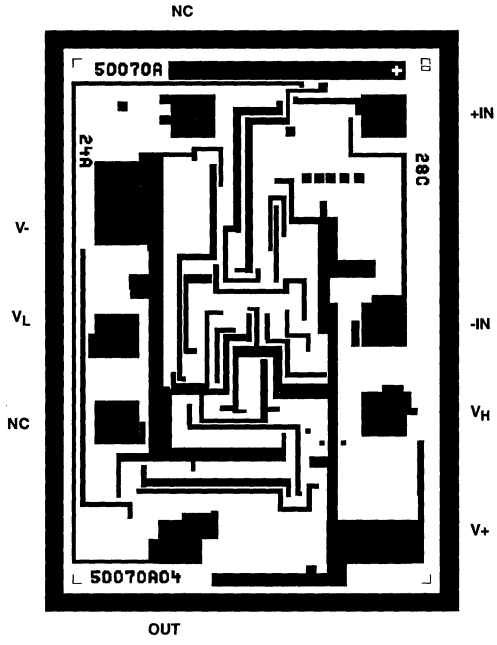
52

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1113



HARRIS SEMICONDUCTOR

HFA1114

November 1996

850MHz Video Cable Driving Buffer

Features

- Access to Summing Node Allows Circuit Customization
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Wide -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2400V/µs
- Fast Settling Time (0.1%) 11ns
- High Output Current 60mA
- Excellent Gain Accuracy 0.99V/V
- Overdrive Recovery ..... <10ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems

Description

The HFA1114 is a closed loop Buffer featuring user programmable gain and ultra high speed performance. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1114 offers a wide -3dB bandwidth of 850MHz, very fast slew rate, excellent gain flatness, low distortion and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

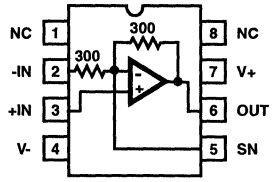
For applications requiring a standard buffer pinout, please refer to the HFA1110 datasheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1114IP	-40 to 85	8 Ld PDIP	E8.3
HFA1114IB (H1114I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1114
(PDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1, 8	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
SN	5	Summing Node
OUT	6	Output
V+	7	Positive Supply

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 3151.3

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current 60mA

Operating Conditions

Temperature Range ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Die) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Output Offset Voltage		25	-	8	25	mV
		Full	-	-	35	mV
Output Offset Voltage Drift		Full	-	10	-	µV/°C
PSRR		25	39	45	-	dB
		Full	35	-	-	dB
Input Noise Voltage	100kHz	25	-	9	-	nV/√Hz
Non-Inverting Input Noise Current	100kHz	25	-	37	-	pA/√Hz
Non-Inverting Input Bias Current		25	-	25	40	µA
		Full	-	-	65	µA
Non-Inverting Input Resistance		25	25	50	-	kΩ
Inverting Input Resistance		25	240	300	360	Ω
Input Capacitance	Either Input	25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±2.8	-	V
TRANSFER CHARACTERISTICS						
Gain	$A_V = +1$, $V_{IN} = +2V$	25	0.980	0.990	1.02	V/V
		Full	0.975	-	1.025	V/V
	$A_V = +2$, $V_{IN} = +1V$	25	1.96	1.98	2.04	V/V
		Full	1.95	-	2.05	V/V
DC Non-Linearity	$A_V = +2$, ±2V Full Scale	25	-	0.02	-	%
OUTPUT CHARACTERISTICS						
Output Voltage	$A_V = -1$	25	±3.0	±3.3	-	V
		Full	±2.5	±3.0	-	V
Output Current	$A_V = -1$, $R_L = 50\Omega$	25, 85	50	60	-	mA
		-40°C	35	50	-	mA
Closed Loop Output Impedance	$A_V = +2$, DC	25	-	0.3	-	Ω

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current		25	-	21	26	mA
		Full	-	-	33	mA
AC CHARACTERISTICS						
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$)	$A_V = -1$	25	-	800	-	MHz
	$A_V = +1$	25	-	850	-	MHz
	$A_V = +2$	25	-	550	-	MHz
Slew Rate ($V_{OUT} = 5V_{P-P}$)	$A_V = -1$	25	-	2400	-	V/µs
	$A_V = +1$	25	-	1500	-	V/µs
	$A_V = +2$	25	-	1900	-	V/µs
Full Power BW	$5V_{P-P}$, $A_V = +2$	25	-	220	-	MHz
Gain Flatness	To 30MHz, $A_V = +2$	25	-	±0.015	-	dB
Gain Flatness	To 100MHz, $A_V = +2$	25	-	±0.07	-	dB
2nd Harmonic Distortion	50MHz, $V_{OUT} = 2V_{P-P}$	25	-	-53	-	dBc
3rd Harmonic Distortion	50MHz, $V_{OUT} = 2V_{P-P}$	25	-	-68	-	dBc
3rd Order Intercept	100MHz, $A_V = +2$	25	-	28	-	dBm
1dB Compression	100MHz, $A_V = +2$	25	-	19	-	dBm
Rise Time ($V_{OUT} = 0.5V$ Step)	$A_V = +2$	25	-	700	-	ps
	$A_V = +1$	25	-	480	-	ps
Overshoot	$V_{OUT} = 0.5V$ Step, $A_V = +2$	25	-	6	-	%
0.1% Settling Time	$V_{OUT} = 2V$ to $0V$	25	-	11	-	ns
0.05% Settling Time	$V_{OUT} = 2V$ to $0V$	25	-	15	-	ns
Overdrive Recovery Time		25	-	8.5	-	ns
Differential Gain	$A_V = +1$, 3.58MHz, $R_L = 150\Omega$	25	-	0.03	-	%
	$A_V = +2$, 3.58MHz, $R_L = 150\Omega$	25	-	0.02	-	%
Differential Phase	$A_V = +1$, 3.58MHz, $R_L = 150\Omega$	25	-	0.05	-	Degrees
	$A_V = +2$, 3.58MHz, $R_L = 150\Omega$	25	-	0.04	-	Degrees

Application Information

Closed Loop Gain Selection

The HFA1114 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 50Ω, C_L = 30pF, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at A_V = +1, R_S = 5Ω, C_L = 340pF.

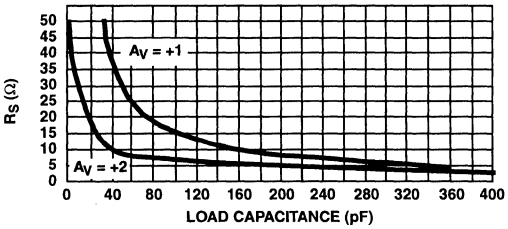


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1114 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

2. Remove the 500Ω feedback resistor (R_2), and leave the connection open.
3. a. For A_V = +1 evaluation, remove the 500Ω gain setting resistor (R_1), and leave pin 2 floating.
   b. For A_V = +2, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.
4. Isolate Pin 5 from the stray board capacitance to minimize peaking and overshoot.

The layout and modified schematic of the board are shown in Figure 2.

To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

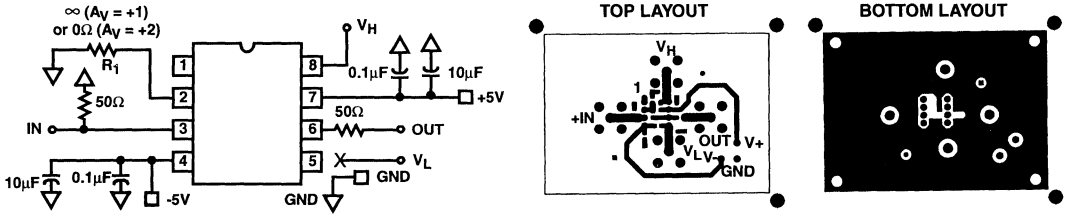


FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

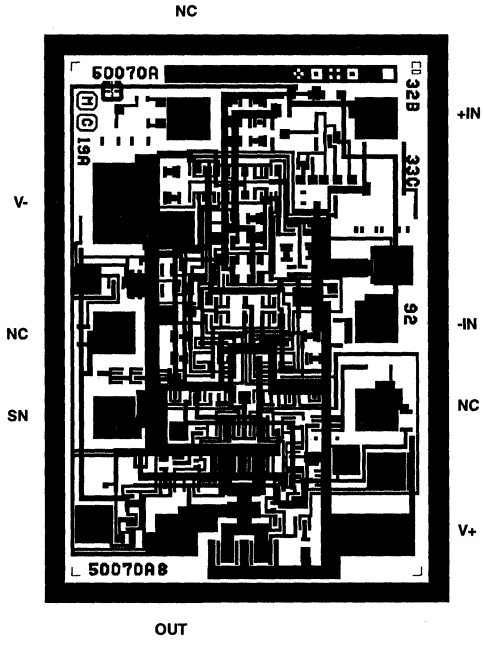
52

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1114



HARRIS SEMICONDUCTOR

HFA1115

225MHz, Low Power, Output Limiting, Closed Loop Buffer Amplifier

November 1996

Features

- User Programmable Output Voltage Limiting
- High Input Impedance 1MΩ
- Differential Gain 0.02%
- Differential Phase ..... 0.03 Degrees
- Wide -3dB Bandwidth (A_V = +2) 225MHz
- Very Fast Slew Rate (A_V = -1) 1135V/µs
- Low Supply Current 7.1mA
- High Output Current 60mA
- Excellent Gain Accuracy 0.99V/V
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Fast Overdrive Recovery ..... <1ns
- Standard Operational Amplifier Pinout

Applications

- Flash A/D Drivers
- Video Cable Drivers
- High Resolution Monitors
- Professional Video Processing
- Medical Imaging
- Video Digitizing Boards/Systems
- Battery Powered Communications

Description

The HFA1115 is a high speed closed loop Buffer featuring both user programmable gain and output limiting. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1115 also offers a wide -3dB bandwidth of 225MHz, very fast slew rate, excellent gain flatness and high output current.

This buffer is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. The limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The HFA1115 also allows for voltage gains of +2, +1, and -1, without the use of external resistors. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" text. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

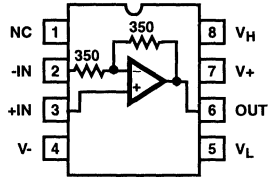
Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path, should a higher closed loop gain be needed at a future date. For Military product, refer to the HFA1115/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1115IP	-40 to 85	8 Ld PDIP	E8.3
HFA1115IB (H1115I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HFA1115
(PDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
V_L	5	Lower Output Limit
OUT	6	Output
V+	7	Positive Supply
V_H	8	Upper Output Limit

3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3606.3**

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Output Current (Note 2) . . . . . Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage Range (Typical) . . . . . 5V to 10V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Die) . . . . . 175^oC
Maximum Junction Temperature (Plastic Packages) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 30mA for maximum reliability.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Output Offset Voltage		A	25	-	2	10	mV
		A	Full	-	3	15	mV
Average Output Offset Voltage Drift		B	Full	-	22	70	$\mu V/^oC$
Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	42	45	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	40	44	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	40	45	-	dB
Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	45	49	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	43	48	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	43	48	-	dB
Non-Inverting Input Bias Current		A	25	-	1	15	μA
		A	Full	-	3	25	μA
Non-Inverting Input Bias Current Drift		B	Full	-	30	80	$nA/^oC$
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.1	-	$M\Omega$
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	1.4	-	$M\Omega$
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	1.3	-	$M\Omega$
Inverting Input Resistance		C	25	280	350	420	Ω
Input Capacitance		C	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR and $+R_{IN}$ Tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	7	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	3.6	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Gain	$A_V = -1$	A	25	-0.98	-0.996	-1.02	V/V
		A	Full	-0.975	-1.000	-1.025	V/V
	$A_V = +1$	A	25	0.98	0.992	1.02	V/V
		A	Full	0.975	0.993	1.025	V/V
	$A_V = +2$	A	25	1.96	1.988	2.04	V/V
		A	Full	1.95	1.990	2.05	V/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS							
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$)	$A_V = -1$	B	25	-	225	-	MHz
	$A_V = +1$, $+R_S = 620\Omega$	B	25	-	170	-	MHz
	$A_V = +2$	B	25	-	225	-	MHz
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$ at $A_V = +2/-1$, $4V_{P-P}$ at $A_V = +1$)	$A_V = -1$	B	25	-	157	-	MHz
	$A_V = +1$, $+R_S = 620\Omega$	B	25	-	140	-	MHz
	$A_V = +2$	B	25	-	125	-	MHz
Gain Flatness (to 25MHz, $V_{OUT} = 0.2V_{P-P}$)	$A_V = +1$, $+R_S = 620\Omega$	B	25	-	±0.1	-	dB
	$A_V = +2$	B	25	-	±0.04	-	dB
Gain Flatness (to 50MHz, $V_{OUT} = 0.2V_{P-P}$)	$A_V = +1$, $+R_S = 620\Omega$	B	25	-	±0.25	-	dB
	$A_V = +2$	B	25	-	±0.1	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing	$A_V = -1$	A	25	±3.0	±3.2	-	V
		A	Full	±2.8	±3.0	-	V
Output Current	$A_V = -1$, $R_L = 50\Omega$	A	25, 85	50	55	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
Closed Loop Output Impedance	DC, $A_V = +2$	B	25	-	0.07	-	Ω
Second Harmonic Distortion ($A_V = +2$, $V_{OUT} = 2V_{P-P}$)	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Third Harmonic Distortion ($A_V = +2$, $V_{OUT} = 2V_{P-P}$)	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
TRANSIENT RESPONSE $A_V = +2$, Unless Otherwise Specified							
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$)	Rise Time	B	25	-	1.7	-	ns
	Fall Time	B	25	-	1.9	-	ns
Overshoot ($V_{OUT} = 0.5V_{P-P}$, V_{IN} $t_{RISE} = 2.5ns$)	+OS	B	25	-	0	-	%
	-OS	B	25	-	0	-	%
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = -1$)	+SR	B	25	-	1660	-	V/µs
	-SR	B	25	-	1135	-	V/µs
Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $+R_S = 620\Omega$)	+SR	B	25	-	1125	-	V/µs
	-SR	B	25	-	800	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$)	+SR	B	25	-	1265	-	V/µs
	-SR	B	25	-	870	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step)	To 0.1%	B	25	-	15	-	ns
	To 0.05%	B	25	-	20	-	ns
	To 0.02%	B	25	-	30	-	ns
VIDEO CHARACTERISTICS							
Differential Gain	f = 3.58MHz, $A_V = +2$, $R_L = 150\Omega$	B	25	-	0.02	-	%
Differential Phase	f = 3.58MHz, $A_V = +2$, $R_L = 150\Omega$	B	25	-	0.03	-	Degrees

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	4.5	-	5.5	±V
Power Supply Current		A	25	6.6	6.9	7.1	mA
		A	Full	-	7.1	7.3	mA
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.25V	A	25	-	0.5	1	µA/V
		A	Full	-	-	3	µA/V
OUTPUT LIMITING CHARACTERISTICS	A_V = +2, V_H = +1V, V_L = -1V, Unless Otherwise Specified						
Clamp Accuracy	V_{IN} = ±1.6V, A_V = -1	A	Full	-125	-70	125	mV
Overdrive Recovery Time	V_{IN} = ±1V	B	25	-	0.8	-	ns
Negative Clamp Range		B	25	-5.0 to +2.0			V
Positive Clamp Range		B	25	-2.0 to +5.0			V
Clamp Input Bias Current		A	Full	-	85	200	µA
Clamp Input Bandwidth		C	25	-	100	-	MHz

NOTE:

3. Test Level: A. Production Tested.; B. Typical or Guaranteed Limit Based on Characterization.; C. Design Typical for Information Only.

Application Information

Closed Loop Gain Selection

The HFA1115 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1 (see next section for layout caveats), while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

Unity Gain Considerations

Unity gain selection is accomplished by floating the -Input of the HFA1115. Anything that tends to short the -Input to GND, such as stray capacitance at high frequencies, will cause the amplifier gain to increase toward a gain of +2. The result is excessive high frequency peaking, and possible instability. Even the minimal amount of capacitance associated with attaching the -Input lead to the PCB results in approximately 3dB of gain peaking. At a minimum this requires due care to ensure the minimum capacitance at the -Input connection.

Table 1 lists five alternate methods for configuring the HFA1115 as a unity gain buffer, and the corresponding performance. The implementations vary in complexity and involve performance trade-offs. The easiest approach to implement is simply shorting the two input pins together, and applying the input signal to this common node. The amplifier bandwidth drops from 400MHz to 200MHz, but excellent gain flatness is the benefit. Another drawback to this approach is that the amplifier input noise voltage and input offset voltage terms see a gain of +2, resulting in higher noise and output offset voltages. Alternately, a 100pF capacitor between the inputs shorts them only at high frequencies, which prevents the increased output offset voltage but delivers less gain flatness.

Another straightforward approach is to add a 620Ω resistor in series with the positive input. This resistor and the HFA1115 input capacitance form a low pass filter which rolls off the signal bandwidth before gain peaking occurs. This configuration was employed to obtain the datasheet AC and transient parameters for a gain of +1.

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 1.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 225MHz. By decreasing R_S as C_L increases the maximum bandwidth is obtained without sacrificing stability.

Evaluation Board

The performance of the HFA1115 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

4. Remove the 500Ω feedback resistor (R_2), and leave the connection open.
5. a. For A_V = +1 evaluation, remove the 500Ω gain setting resistor (R_1), and leave pin 2 floating.
   b. For A_V = +2, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

The layout and modified schematic of the board are shown in Figure 1.

To order evaluation boards (Part Number HFA11XXEVAL), please contact your local sales office.

TABLE 1. UNITY GAIN PERFORMANCE FOR VARIOUS IMPLEMENTATIONS

APPROACH	PEAKING (dB)	BW (MHz)	+SR/-SR (V/μs)	±0.1dB GAIN FLATNESS (MHz)
Remove Pin 2	2.5	400	1200/850	20
$+R_S$ = 620Ω	0.6	170	1125/800	25
$+R_S$ = 620Ω and Remove Pin 2	0	165	1050/775	65
Short Pins 2, 3	0	200	875/550	45
100pF cap. between pins 2, 3	0.2	190	900/550	19

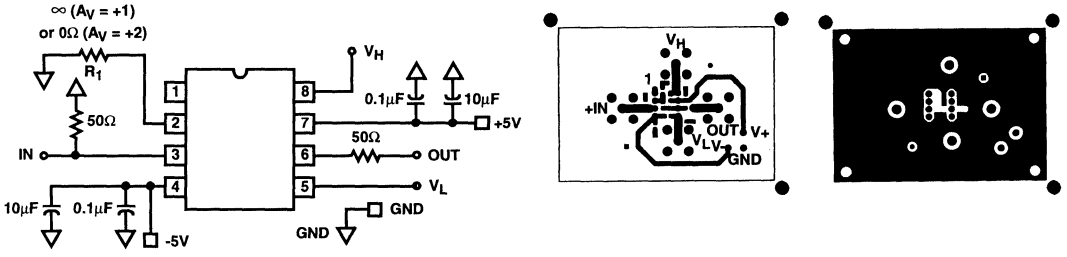


FIGURE 1. EVALUATION BOARD SCHEMATIC AND LAYOUT

Die Characteristics

DIE DIMENSIONS:

59 mils x 58.2 mils x 19 mils
1500µm x 1480µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

PASSIVATION:

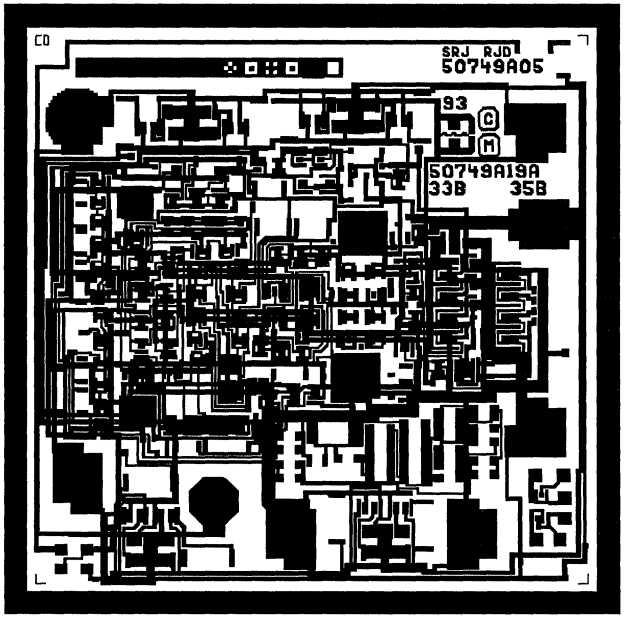
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

89

Metallization Mask Layout

HFA1115



HARRIS SEMICONDUCTOR HFA1118, HFA1119

ADVANCE INFORMATION

November 1996

500MHz Programmable Gain Video Buffers with Output Limiting and Output Disable

Features

- User Programmable For Closed Loop Gains of ±1, or +2 Without Use of External Resistors
- User Programmable Output Limiting (HFA1119)
- Standard Operational Amplifier Pinout
- Excellent Gain Accuracy ..... ±0.5%
- Wide -3dB Bandwidth (A_V = +2) 500MHz
- Gain Flatness (to 250MHz) ..... ±0.5dB
- Very Fast Slew Rate (A_V = +2) 1200V/µs
- Differential Gain/Phase ..... 0.02%/0.02 Degrees
- Fast Output Enable/Disable 10ns

Applications

- Flash A/D Drivers
- Video Cable Drivers
- Professional Video Processing
- Medical Imaging
- PC Multimedia Systems
- Video Pixel Switching
- Oscilloscopes and Analyzers

Description

The HFA1118, and HFA1119 are high speed, low power, closed loop buffers built with Harris' proprietary complementary bipolar UHF-1 process. Both buffers allow for selection of voltage gains of +2 and ±1, without the use of external gain setting resistors.

The HFA1119 is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. For added flexibility, the HFA1119 also features an active low, TTL/CMOS compatible disable input, which when activated forces the output to a high impedance state, and reduces supply current.

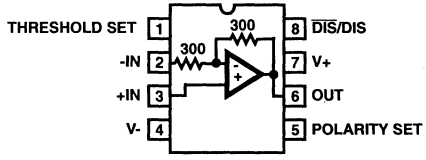
The HFA1118 features a TTL/CMOS compatible output disable pin which is user programmable for polarity (active high or low). This feature eliminates the inverter required between amplifiers in multiplexer configurations. The ultra-fast (10ns) enable and disable times make the HFA1118 and HFA1119 the obvious choices for pixel switching and other high speed multiplexing applications.

Ordering Information

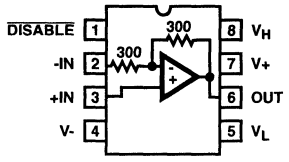
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1118IP, HFA1119IP	-40 to 85	8 Ld PDIP	E8.3
HFA1118IB, HFA1119IB	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinouts

HFA1118
(PDIP, SOIC)
TOP VIEW



HFA1119
(PDIP, SOIC)
TOP VIEW



HFA1118 PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
Threshold Set	Optional Logic Threshold Set. Maintains Disable Pin TTL Compatibility with Asymmetrical Supplies (e.g., +10V, 0V)
Polarity Set	Defines Polarity of Disable Input. High or Floating Selects Active Low Disable (i.e., $\overline{DIS}$).
$\overline{DIS}$/DIS	TTL Compatible Disable Input. Output is Driven to a True Hi-Z State When Active. Polarity depends on state of Polarity Set Pin.

HFA1118 DISABLE FUNCTIONALITY

POLARITY SET (PIN 5)	DISABLE (PIN 8)	OUTPUT (PIN 6)
High or Float	High or Float	Enabled
High or Float	Low	Disabled
Low	High or Float	Disabled
Low	Low	Enabled

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 4020.1

HARRIS SEMICONDUCTOR

HFA1130

850MHz, Output Limiting, Low Distortion Current Feedback Operational Amplifier

November 1996

Features

- User Programmable Output Voltage Limits
- Low Distortion (30MHz, HD2) ..... -56dBc
- -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2300V/μs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) 0.14dB
  - (50MHz) 0.04dB
  - (30MHz) 0.01dB
- High Output Current 60mA
- Overdrive Recovery ..... <1ns

Applications

- Residue Amplifier
- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems
- Related Literature
  - AN9420, Current Feedback Theory
  - AN9202, HFA11XX Evaluation Fixture

Description

The HFA1130 is a high speed wideband current feedback amplifier featuring programmable output limits. Built with Harris' proprietary complementary bipolar UHF-1 process, it is the fastest monolithic amplifier available from any semiconductor manufacturer.

This amplifier is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overdrive recovery times. The output limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation, following an overdrive condition.

The HFA1130 offers significant performance improvements over the CLC500/501/502.

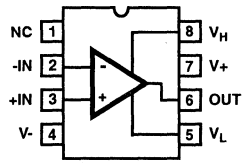
A variety of packages and temperature grades are available. See the ordering information below for details. For /883 product refer to the HFA1130/883 datasheet.

Ordering Information

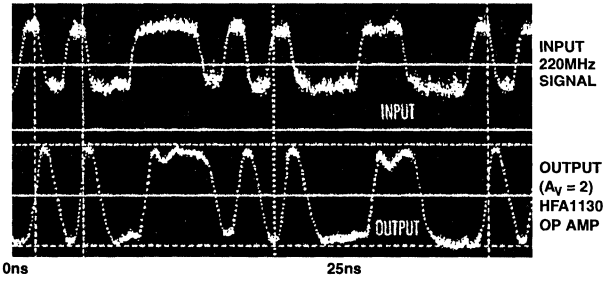
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1130MJ/883	-55 to 125	8 Ld CERDIP	F8.3A
HFA1130IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1130IP	-40 to 85	8 Ld PDIP	E8.3
HFA1130IB (H1130I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High-Speed Op Amps		

Pinout

HFA1130
(PDIP, CERDIP, SOIC)
TOP VIEW



The Op Amps With Fastest Edges



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3369.1**

Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- 12V
Input Voltage..... V_{SUPPLY}
Differential Input Voltage..... 5V
Output Current (50% Duty Cycle)..... 60mA

Operating Conditions

Temperature Range ..... -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	120	35
PDIP Package	130	N/A
SOIC Package	170	N/A

Maximum Junction Temperature (Die or CERDIP) ..... 175^oC
Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to T_A to 150^oC
Maximum Lead Temperature (Soldering 10s)..... 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (Note 3)		A	25	-	2	6	mV
		A	Full	-	-	10	mV
Input Offset Voltage Drift		C	Full	-	10	-	$\mu V/^oC$
V_{IO} CMRR	$\Delta V_{CM} = \pm2V$	A	25	40	46	-	dB
		A	Full	38	-	-	dB
V_{IO} PSRR	$\Delta V_S = \pm1.25V$	A	25	45	50	-	dB
		A	Full	42	-	-	dB
Non-Inverting Input Bias Current (Note 3)	+IN = 0V	A	25	-	25	40	μA
		A	Full	-	-	65	μA
$+I_{BIAS}$ Drift		C	Full	-	40	-	$nA/^oC$
$+I_{BIAS}$ CMS	$\Delta V_{CM} = \pm2V$	A	25	-	20	40	$\mu A/V$
		A	Full	-	-	50	$\mu A/V$
Inverting Input Bias Current (Note 3)	-IN = 0V	A	25	-	12	50	μA
		A	Full	-	-	60	μA
$-I_{BIAS}$ Drift		C	Full	-	40	-	$nA/^oC$
$-I_{BIAS}$ CMS	$\Delta V_{CM} = \pm2V$	A	25	-	1	7	$\mu A/V$
		A	Full	-	-	10	$\mu A/V$
$-I_{BIAS}$ PSS	$\Delta V_S = \pm1.25V$	A	25	-	6	15	$\mu A/V$
		A	Full	-	-	27	$\mu A/V$
Non-Inverting Input Resistance		A	25	25	50	-	$k\Omega$
Inverting Input Resistance		C	25	-	20	30	Ω
Input Capacitance (Either Input)		B	25	-	2	-	pF
Input Common Mode Range		C	Full	±2.5	±3.0	-	V
Input Noise Voltage (Note 3)	100kHz	B	25	-	4	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 3)	100kHz	B	25	-	18	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 3)	100kHz	B	25	-	21	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified							
Open Loop Transimpedance (Note 3)		B	25	-	300	-	$k\Omega$
-3dB Bandwidth (Note 3)	$V_{OUT} = 0.2V_{P-P}$, $A_V = +1$	B	25	530	850	-	MHz

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
-3dB Bandwidth	V_{OUT} = 0.2V_{P-P}, A_V = +2, R_F = 360Ω	B	25	-	670	-	MHz
Full Power Bandwidth	4V_{P-P}, A_V = -1	B	Full	-	300	-	MHz
Gain Flatness (Note 3)	To 100MHz	B	25	-	±0.14	-	dB
Gain Flatness	To 50MHz	B	25	-	±0.04	-	dB
Gain Flatness	To 30MHz	B	25	-	±0.01	-	dB
Linear Phase Deviation (Note 3)	DC to 100MHz	B	25	-	0.6	-	Degrees
Differential Gain	NTSC, R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase	NTSC, R_L = 75Ω	B	25	-	0.05	-	Degrees
Minimum Stable Gain		A	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS A_V = +2, Unless Otherwise Specified							
Output Voltage (Note 3)	A_V = -1	A	25	±3.0	±3.3	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	R_L = 50Ω, A_V = -1	A	25, 85	50	60	-	mA
		A	-40	35	50	-	mA
DC Closed Loop Output Impedance (Note 3)		B	25	-	0.07	-	Ω
2nd Harmonic Distortion (Note 3)	30MHz, V_{OUT} = 2V_{P-P}	B	25	-	-56	-	dBc
3rd Harmonic Distortion (Note 3)	30MHz, V_{OUT} = 2V_{P-P}	B	25	-	-80	-	dBc
3rd Order Intercept (Note 3)	100MHz	B	25	20	30	-	dBm
1dB Compression	100MHz	B	25	15	20	-	dBm
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified							
Rise Time	V_{OUT} = 2.0V Step	B	25	-	900	-	ps
Overshoot (Note 3)	V_{OUT} = 2.0V Step	B	25	-	10	-	%
Slew Rate	A_V = +1, V_{OUT} = 5V_{P-P}	B	25	-	1400	-	V/µs
	A_V = +2, V_{OUT} = 5V_{P-P}	B	25	1850	2300	-	V/µs
0.1% Settling Time (Note 3)	V_{OUT} = 2V to 0V	B	25	-	11	-	ns
0.2% Settling Time (Note 3)	V_{OUT} = 2V to 0V	B	25	-	7	-	ns
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		B	Full	±4.5	-	±5.5	V
Supply Current (Note 3)		A	25	-	21	26	mA
		A	Full	-	-	33	mA
LIMITING CHARACTERISTICS A_V = +2, V_H = +1V, V_L = -1V, Unless Otherwise Specified							
Clamp Accuracy	V_{IN} = ±2V, A_V = -1	A	25	-	60	±125	mV
Clamped Overshoot	V_{IN} = ±1V, Input t_R/t_F = 2ns	B	25	-	4	-	%
Overdrive Recovery Time	V_{IN} = ±1V	B	25	-	0.75	1.5	ns
Negative Clamp Range		B	25	-	-5.0 to +2.0	-	V
Positive Clamp Range		B	25	-	-2.0 to +5.0	-	V
Clamp Input Bias Current		A	25	-	50	200	µA
Clamp Input Bandwidth	V_H or V_L = 100mV_{P-P}	B	25	-	500	-	MHz

NOTES:

2. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
3. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor (R_F)

The enclosed plots of inverting and non-inverting frequency response detail the performance of the HFA1100/1120 in various gains. Although the bandwidth dependency on A_{CL} isn't as severe as that of a voltage feedback amplifier, there is an appreciable decrease in bandwidth at higher gains. This decrease can be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and the R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1100, 1120 designs are optimized for a 510Ω R_F, at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth. The table below lists recommended R_F values for various gains, and the expected bandwidth.

A_{CL}	R_F (Ω)	BW (MHz)
+1	510	850
-1	430	580
+2	360	670
+5	150	520
+10	180	240
+19	270	125

Clamp Operation

General

The HFA1130 features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Clamp Circuitry

Figure 1 shows a simplified schematic of the HFA1130 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (Q_{X1} - Q_{X2}) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of $(V_{-IN} - V_{OUT})/R_F$. This current is mirrored onto the high impedance node (Z) by Q_{X3}-Q_{X4}, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by Q_{P4} and Q_{N4}. Note that when the output reaches it's quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

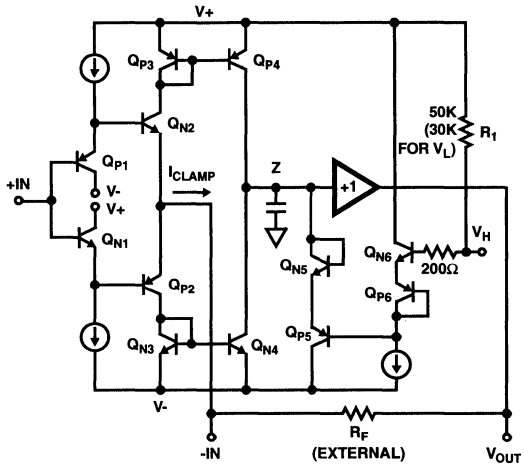


FIGURE 1. HFA1130 SIMPLIFIED V_H CLAMP CIRCUITRY

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (Q_{N6} and Q_{P6}) to set up the base voltage on Q_{P5}. Q_{P5} begins to conduct whenever the high impedance node reaches a voltage equal to Q_{P5}'s base + $2V_{BE}$ (Q_{P5} and Q_{N5}). Thus, Q_{P5} clamps node Z whenever Z reaches V_H. R_1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. Q_{P5} must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node. The clamping current is calculated as $(V_{-IN} - V_{OUT})/R_F$. As an example, a unity gain circuit with V_{IN} = 2V, V_H = 1V, and R_F = 510Ω would have I_{CLAMP} = (2-1)/510Ω = 1.96mA. Note that I_{CC} will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 1, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the Q_{X6} transistors, and the Q_{X5} transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The Q_{X6} transistors are biased at a constant current, but as described earlier, the current through Q_{X5} is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level (V_{-IN} -$V_{OUTCLAMPED}$) and R_F, so clamp accuracy degrades as the overdrive increases, or as R_F decreases. As an example, the specified accuracy of ±60mV for a 2X overdrive with R_F = 510Ω degrades to ±220mV for R_F = 240Ω at the same overdrive, or to ±250mV for a 3X overdrive with R_F = 510Ω.

Consideration must also be given to the fact that the clamp voltages have an effect on amplifier linearity. The "Nonlinearity Near Clamp Voltage" curve in the data sheet illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1130 could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won't be in a DC output voltage from an AC input signal. A 150 - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP}/A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of "Unclamped Performance" and "Clamped Performance" highlight the HFA1130's subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 4.0ns for the unclamped pulse, and 4.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HFA1130 propagation delay is 500ps.

Use of Die in Hybrid Applications

This amplifier is designed with compensation to negate the package parasitics that typically lead to instabilities. As a result, the use of die in hybrid applications results in overcompensated performance due to lower parasitic capacitances. Reducing R_F below the recommended values for packaged units will solve the problem. For A_V = +2 the recommended starting point is 300Ω, while unity gain applications should try 400Ω.

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown below.

Evaluation Board

An evaluation board is available for the HFA1130, (Part Number HFA11XXEVAL). Please contact your local sales office for information.

The layout and schematic of the board are shown here:

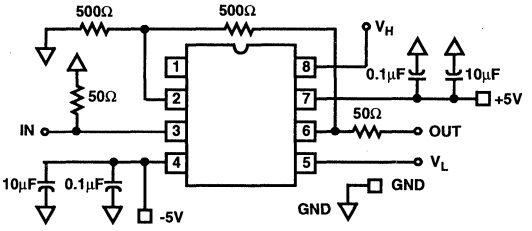
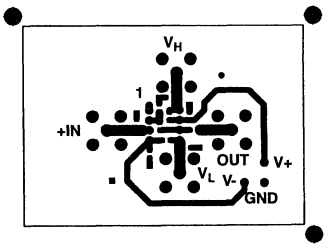
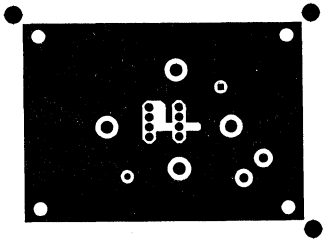


FIGURE 2. BOARD SCHEMATIC

TOP LAYOUT



BOTTOM LAYOUT



Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

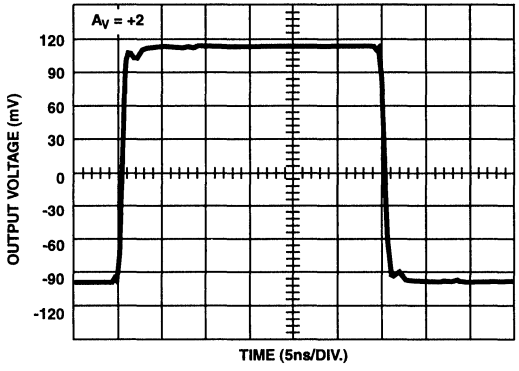


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

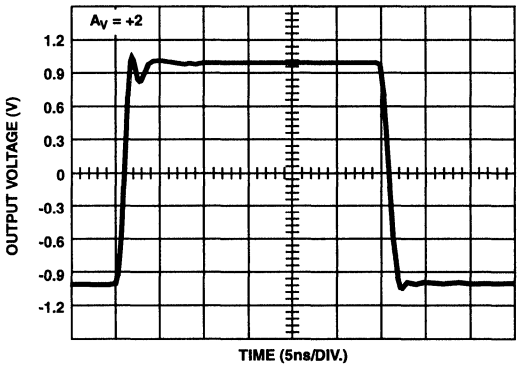


FIGURE 4. LARGE SIGNAL PULSE RESPONSE

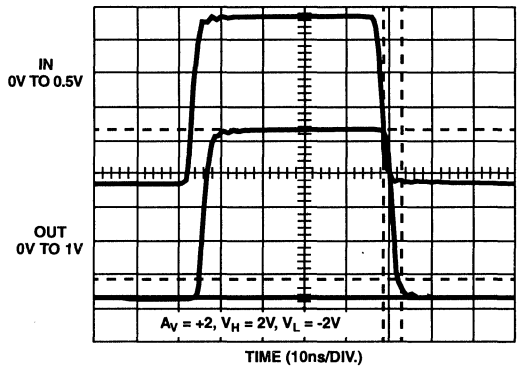


FIGURE 5. UNCLAMPED PERFORMANCE

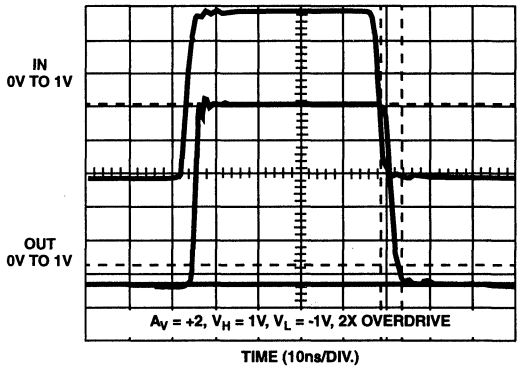


FIGURE 6. CLAMPED PERFORMANCE

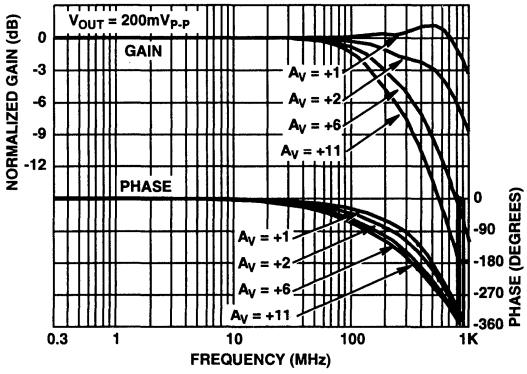


FIGURE 7. NON-INVERTING FREQUENCY RESPONSE

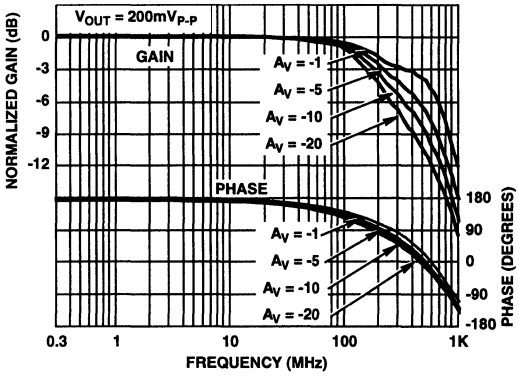


FIGURE 8. INVERTING FREQUENCY RESPONSE

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

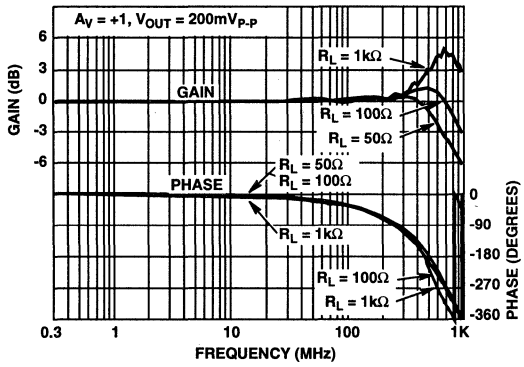


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

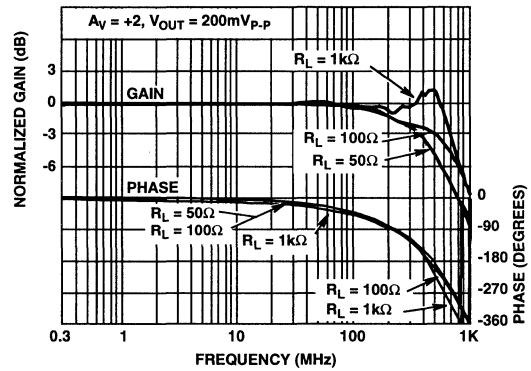


FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

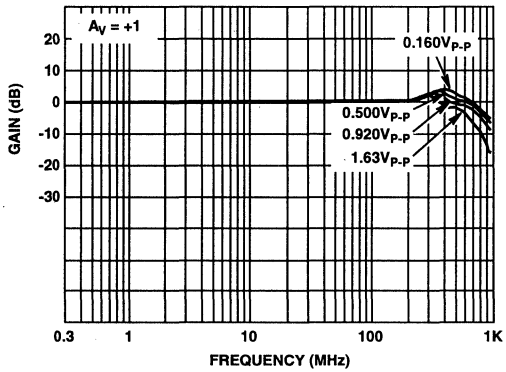


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

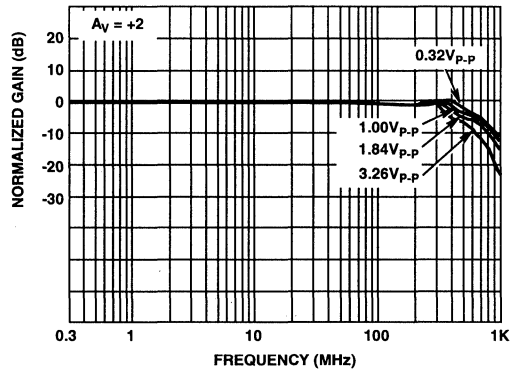


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

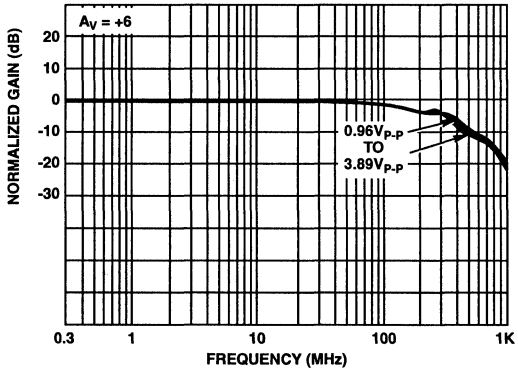


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

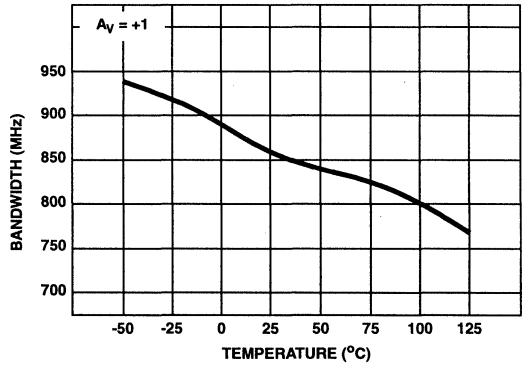


FIGURE 14. -3dB BANDWIDTH vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

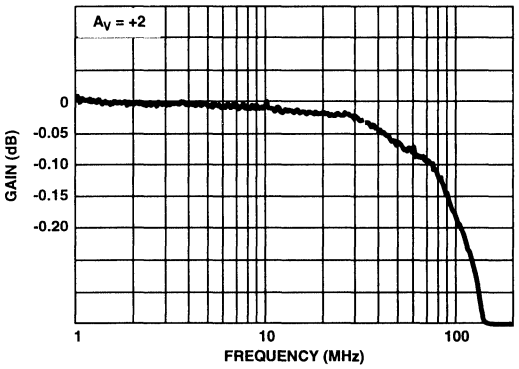


FIGURE 15. GAIN FLATNESS

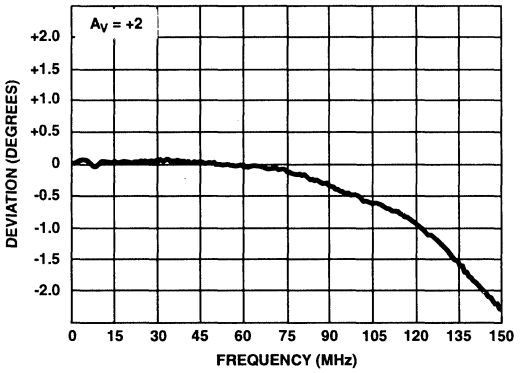


FIGURE 16. DEVIATION FROM LINEAR PHASE

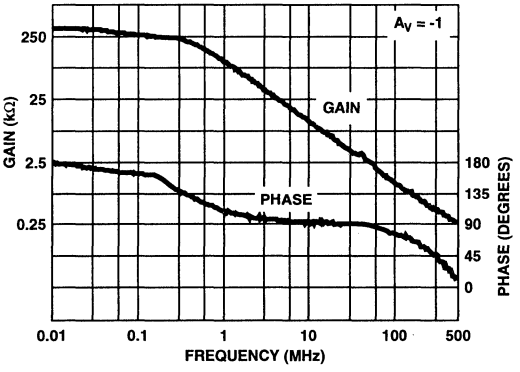


FIGURE 17. OPEN LOOP TRANSIMPEDANCE

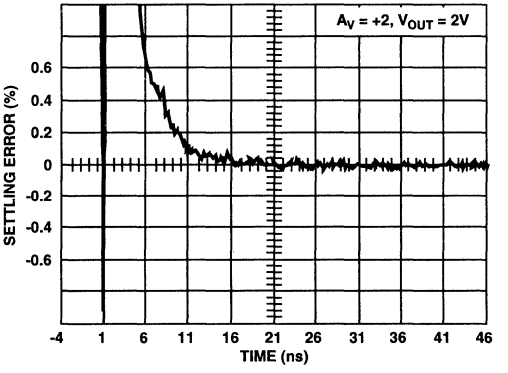


FIGURE 18. SETTLING RESPONSE

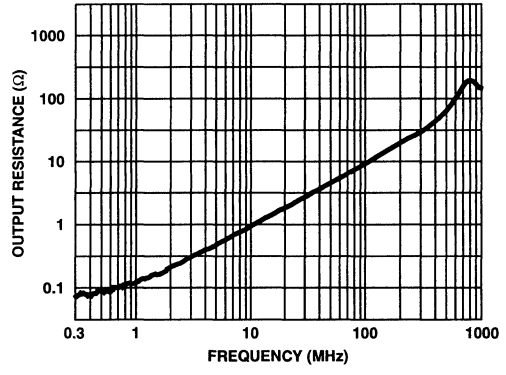


FIGURE 19. CLOSED LOOP OUTPUT RESISTANCE

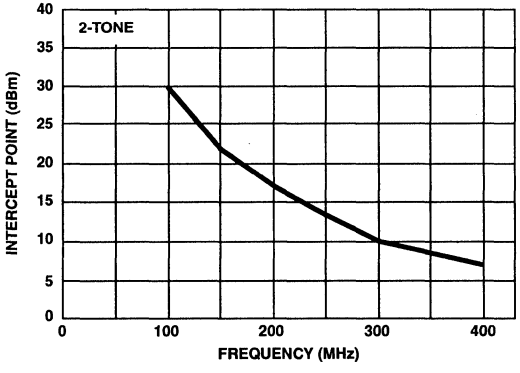


FIGURE 20. 3rd ORDER INTERMODULATION INTERCEPT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

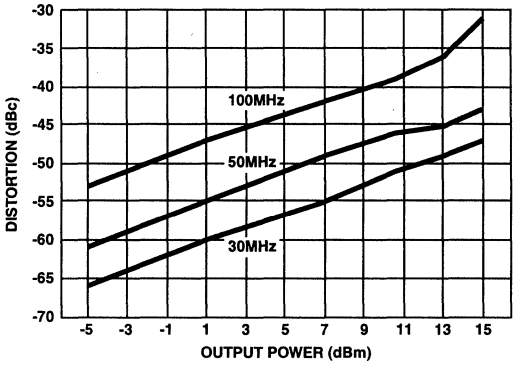


FIGURE 21. 2nd HARMONIC DISTORTION vs P_{OUT}

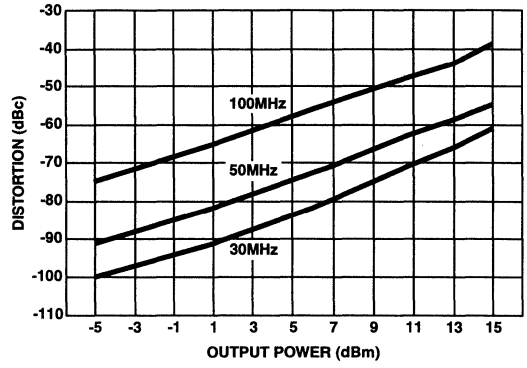


FIGURE 22. 3rd HARMONIC DISTORTION vs P_{OUT}

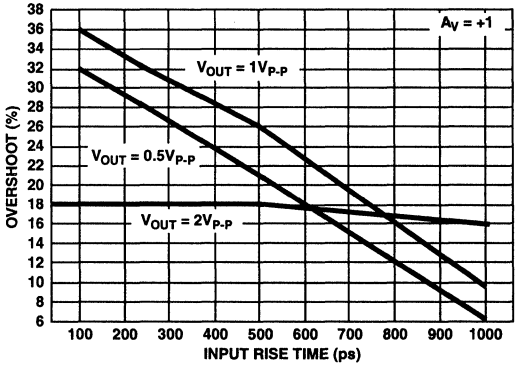


FIGURE 23. OVERSHOOT vs INPUT RISE TIME

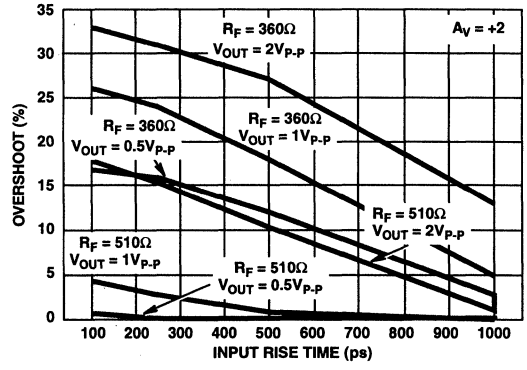


FIGURE 24. OVERSHOOT vs INPUT RISE TIME

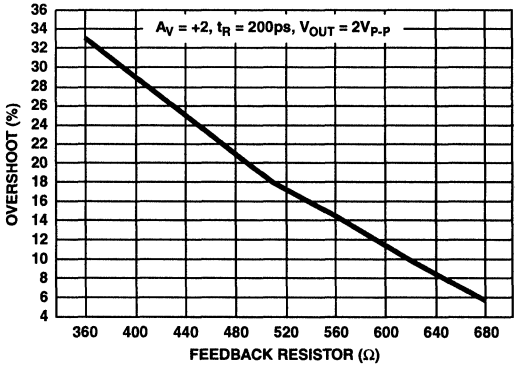


FIGURE 25. OVERSHOOT vs FEEDBACK RESISTOR

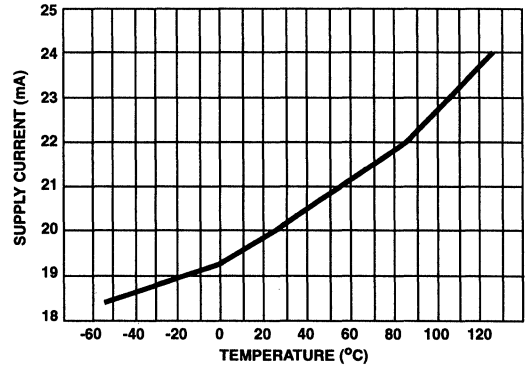


FIGURE 26. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

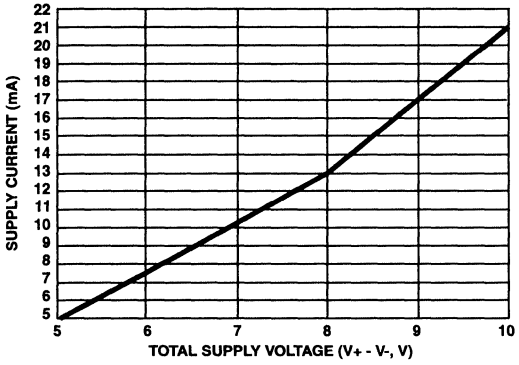


FIGURE 27. SUPPLY CURRENT vs SUPPLY VOLTAGE

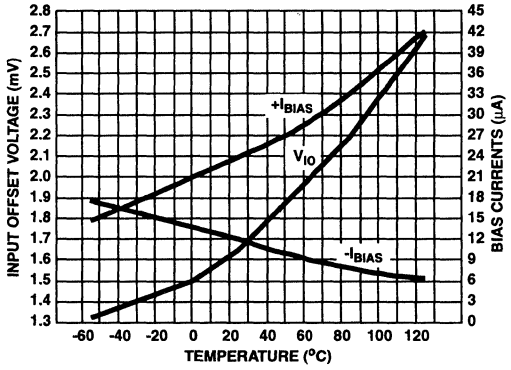


FIGURE 28. V_{IO} AND BIAS CURRENTS vs TEMPERATURE

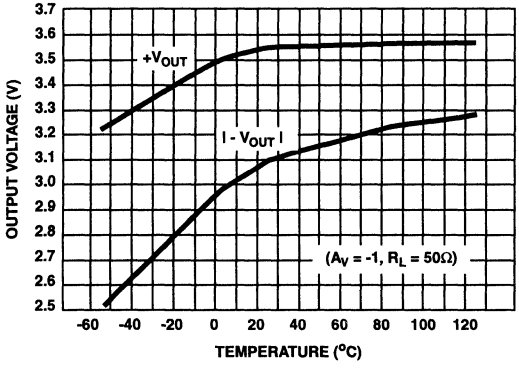


FIGURE 29. OUTPUT VOLTAGE vs TEMPERATURE

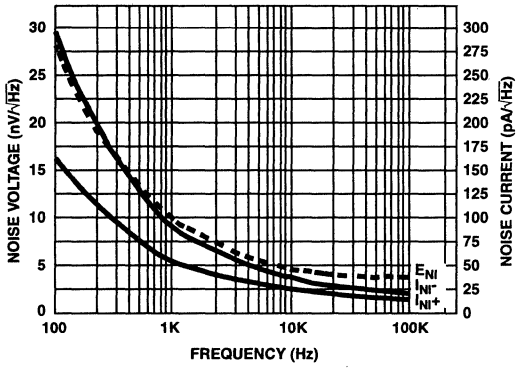


FIGURE 30. INPUT NOISE vs FREQUENCY

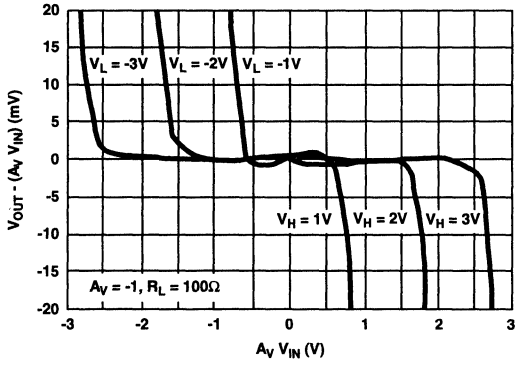


FIGURE 31. NON-LINEARITY NEAR CLAMP VOLTAGE

Die Characteristics

DIE DIMENSIONS:
63 mils x 44 mils x 19 mils
1600µm x 1130µm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: ALCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

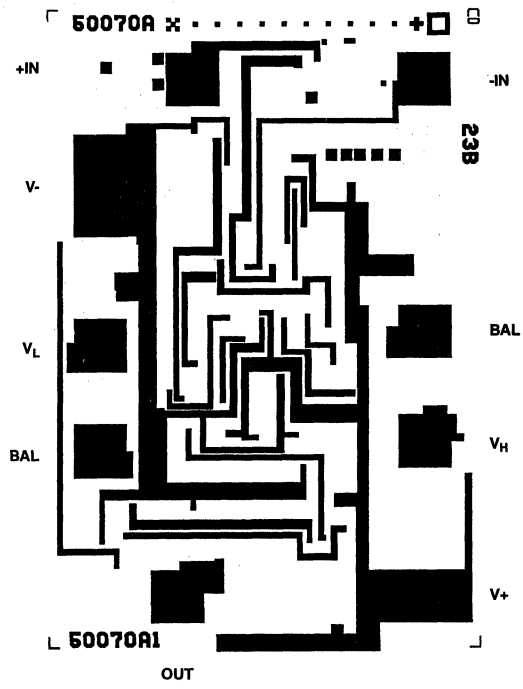
52

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1130



HARRIS SEMICONDUCTOR

HFA1135

360MHz, Low Power, Video Operational Amplifier with Output Limiting

November 1996

Features

- User Programmable Output Voltage Limiting
- Fast Overdrive Recovery..... <1ns
- Low Supply Current..... 6.8mA
- High Input Impedance..... 2MΩ
- Wide -3dB Bandwidth 360MHz
- Very Fast Slew Rate..... 1200V/μs
- Gain Flatness (to 50MHz) ..... ±0.07dB
- Differential Gain..... 0.02%
- Differential Phase..... 0.04 Degrees
- Pin Compatible Upgrade to CLC501 and CLC502

Applications

- Flash A/D Drivers
- High Resolution Monitors
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications

Description

The HFA1135 is a high speed, low power current feedback amplifier build with Harris' proprietary complementary bipolar UHF-1 process. This amplifier features user programmable output limiting, via the V_H and V_L pins.

The HFA1135 is the ideal choice for high speed, low power applications requiring output limiting (e.g. flash A/D drivers), especially those requiring fast overdrive recovery times. The limiting function allows the designer to set the maximum and minimum output levels to protect downstream stages from damage or input saturation. The sub-nanosecond overdrive recovery time ensures a quick return to linear operation following an overdrive condition.

Component and composite video systems also benefit from this operational amplifier's performance, as indicated by the gain flatness, and differential gain and phase specifications.

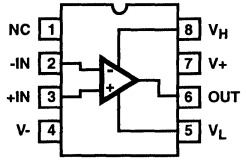
The HFA1135 is a low power, high performance upgrade for the CLC501 and CLC502.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1135IP	-40 to 85	8 Ld PDIP	E8.3
HFA1135IB (H1135I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1135
(PDIP, SOIC)
TOP VIEW



3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 3653.2

Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- 11V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 1) ..... Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating ..... >600V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Die Only) ..... 175^oC
Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range ..... -40^oC to 85^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$ (Note 4), $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	$\mu V/^oC$
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	47	50	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	45	48	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	50	54	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	47	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	47	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	$nA/^oC$
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	1.3	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	$nA/^oC$
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	25	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40	-	4	8	µA/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω (Note 4), R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	40	-	Ω
Input Capacitance (Either Input)		C	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density	f = 100kHz	B	25	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain	A_V = -1	C	25	-	500	-	kΩ
AC CHARACTERISTICS A_V = +2, R_F = 250Ω, Unless Otherwise Specified							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})	A_V = +1, R_F = 1.5kΩ	B	25	-	660	-	MHz
	A_V = +2, R_F = 250Ω	B	25	-	360	-	MHz
	A_V = +2, R_F = 330Ω	B	25	-	315	-	MHz
	A_V = -1, R_F = 330Ω	B	25	-	290	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1)	A_V = +1, R_F = 1.5kΩ	B	25	-	90	-	MHz
	A_V = +2, R_F = 250Ω	B	25	-	130	-	MHz
	A_V = -1, R_F = 330Ω	B	25	-	170	-	MHz
Gain Flatness (to 25MHz, V_{OUT} = 0.2V_{P-P})	A_V = +1, R_F = 1.5kΩ	B	25	-	±0.10	-	dB
	A_V = +2, R_F = 250Ω	B	25	-	±0.02	-	dB
	A_V = +2, R_F = 330Ω	B	25	-	±0.02	-	dB
Gain Flatness (to 50MHz, V_{OUT} = 0.2V_{P-P})	A_V = +1, R_F = 1.5kΩ	B	25	-	±0.22	-	dB
	A_V = +2, R_F = 250Ω	B	25	-	±0.07	-	dB
	A_V = +2, R_F = 330Ω	B	25	-	±0.03	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
OUTPUT CHARACTERISTICS R_F = 510Ω, Unless Otherwise Specified							
Output Voltage Swing	A_V = -1, R_L = 100Ω	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current	A_V = -1, R_L = 50Ω	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
Closed Loop Output Impedance	DC, A_V = +2, R_F = 250Ω	B	25	-	0.07	-	Ω
Second Harmonic Distortion (A_V = +2, R_F = 250Ω, V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Third Harmonic Distortion (A_V = +2, R_F = 250Ω, V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω (Note 4), R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 250Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P})	Rise Time	B	25	-	0.81	-	ns
	Fall Time	B	25	-	1.25	-	ns
Overshoot (Note 5) (V_{OUT} = 0 to 0.5V, V_{IN} t_{RISE} = 2.5ns)	+OS	B	25	-	3	-	%
	-OS	B	25	-	5	-	%
Overshoot (Note 5) (V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 2.5ns)	+OS	B	25	-	2	-	%
	-OS	B	25	-	10	-	%
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, R_F = 1.5kΩ)	+SR	B	25	-	875	-	V/µs
	-SR	B	25	-	510	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2, R_F = 250Ω)	+SR	B	25	-	1530	-	V/µs
	-SR	B	25	-	850	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = -1, R_F = 330Ω)	+SR	B	25	-	2300	-	V/µs
	-SR	B	25	-	1200	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step)	To 0.1%	B	25	-	15	-	ns
	To 0.05%	B	25	-	20	-	ns
	To 0.02%	B	25	-	30	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 250Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.04	-	Degrees
	R_L = 75Ω	B	25	-	0.06	-	Degrees
OUTPUT LIMITING CHARACTERISTICS A_V = +2, R_F = 250Ω, V_H = +1V, V_L = -1V, Unless Otherwise Specified							
Clamp Accuracy	V_{IN} = ±2V, A_V = -1, R_F = 510Ω	A	Full	-125	25	125	mV
Overdrive Recovery Time	V_{IN} = ±1V	B	25	-	0.8	-	ns
Negative Clamp Range		B	25	-5.0 to +2.0			V
Positive Clamp Range		B	25	-2.0 to +5.0			V
Clamp Input Bias Current		A	25	-	50	200	µA
		A	Full	-	80	200	µA
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current		A	25	6.6	6.8	7.1	mA
		A	Full	6.4	6.9	7.3	mA

NOTES:

3. Test Level: A. Production Tested.; B. Typical or Guaranteed Limit Based on Characterization.; C. Design Typical for Information Only.
4. The optimum feedback resistor for the HFA1135 at A_V = +1 is 1.5kΩ. The Production Tested parameters are tested with R_F = 510Ω because the HFA1135 shares test hardware with the HFA1105 amplifier.
5. Undershoot dominates for output signal swings below GND (e.g., 0.5V_{P-P}), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 0.5V condition.

Die Characteristics

DIE DIMENSIONS:

59 mils x 58.2 mils x 19 mils
1500µm x 1480µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

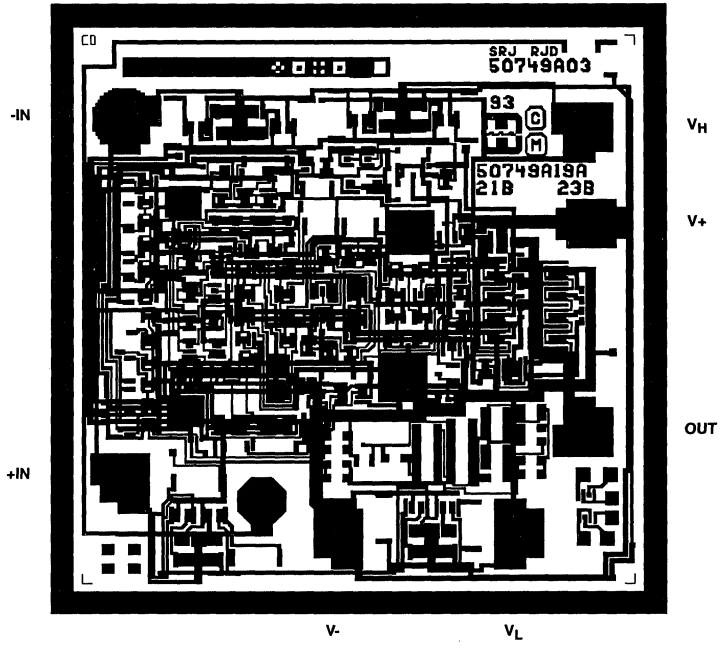
89

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HFA1135



HARRIS SEMICONDUCTOR

HFA1145

330MHz, Low Power, Current Feedback Video Operational Amplifier with Output Disable

November 1996

Features

- Low Supply Current 5.8mA
- High Input Impedance 1MΩ
- Wide -3dB Bandwidth 330MHz
- Very Fast Slew Rate 1000V/μs
- Gain Flatness (to 75MHz) ..... ±0.1dB
- Differential Gain 0.02%
- Differential Phase ..... 0.03 Degrees
- Output Enable/Disable Time 180ns/35ns
- Pin Compatible Upgrade for CLC410

Applications

- Flash A/D Drivers
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications

Description

The HFA1145 is a high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

This amplifier features a TTL/CMOS compatible disable control, pin 8, which when pulled low reduces the supply current and forces the output into a high impedance state. This allows easy implementation of simple, low power video switching and routing systems. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications.

Multiplexed A/D applications will also find the HFA1145 useful as the A/D driver/multiplexer.

The HFA1145 is a low power, high performance upgrade for the CLC410.

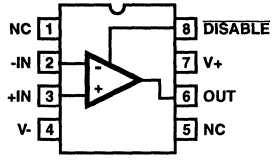
For Military grade product, please refer to the HFA1145/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1145IP	-40 to 85	8 Ld PDIP	E8.3
HFA1145IB (H1145I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1145
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 3955.2

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage. 8V
Output Current (Note 1) . . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating. . . . . >600V

Operating Conditions

Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Die Only). . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s). . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	$\mu V/^{o}C$
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	47	50	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	45	48	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	50	54	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	47	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	47	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	$nA/^{o}C$
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	0.8	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	$nA/^{o}C$
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	25	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	2	5	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	60	-	Ω

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Input Capacitance		C	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 6)	f = 100kHz	B	25	-	3.5	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	2.5	-	$pA/\sqrt{Hz}$
Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	20	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain	$A_V = -1$	C	25	-	500	-	kΩ
AC CHARACTERISTICS $R_F = 510\Omega$, Unless Otherwise Specified							
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, Note 6)	$A_V = +1$, $+R_S = 510\Omega$	B	25	-	270	-	MHz
		B	Full	-	240	-	MHz
	$A_V = -1$, $R_F = 425\Omega$	B	25	-	300	-	MHz
	$A_V = +2$	B	25	-	330	-	MHz
		B	Full	-	260	-	MHz
	$A_V = +10$, $R_F = 180\Omega$	B	25	-	130	-	MHz
		B	Full	-	90	-	MHz
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$ at $A_V = +2/-1$, $4V_{P-P}$ at $A_V = +1$, Note 6)	$A_V = +1$, $+R_S = 510\Omega$	B	25	-	135	-	MHz
	$A_V = -1$	B	25	-	140	-	MHz
	$A_V = +2$	B	25	-	115	-	MHz
Gain Flatness ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$, Note 6)	To 25MHz	B	25	-	±0.03	-	dB
		B	Full	-	±0.04	-	dB
	To 75MHz	B	25	-	±0.11	-	dB
		B	Full	-	±0.22	-	dB
Gain Flatness ($A_V = +1$, $+R_S = 510\Omega$, $V_{OUT} = 0.2V_{P-P}$, Note 6)	To 25MHz	B	25	-	±0.03	-	dB
	To 75MHz	B	25	-	±0.09	-	dB
Minimum Stable gain		A	Full	-	1	-	V/V
OUTPUT CHARACTERISTICS $A_V = +2$, $R_F = 510\Omega$, Unless Otherwise Specified							
Output Voltage Swing (Note 6)	$A_V = -1$, $R_L = 100\Omega$	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current (Note 6)	$A_V = -1$, $R_L = 50\Omega$	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
Closed Loop Output Impedance (Note 6)	DC	B	25	-	0.08	-	Ω
Second Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 6)	10MHz	B	25	-	-48	-	dBc
	20MHz	B	25	-	-44	-	dBc
Third Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 6)	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Reverse Isolation (S_{12}, Note 6)	30MHz	B	25	-	-55	-	dB
TRANSIENT CHARACTERISTICS $A_V = +2$, $R_F = 510\Omega$, Unless Otherwise Specified							
Rise and Fall Times	$V_{OUT} = 0.5V_{P-P}$	B	25	-	1.1	-	ns
		B	Full	-	1.4	-	ns

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Overshoot (Note 4) (V_{OUT} = 0 to 0.5V, V_{IN} t_{RISE} = 1ns)	+OS	B	25	-	3	-	%
	-OS	B	25	-	5	-	%
Overshoot (Note 4) (V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 1ns)	+OS	B	25	-	3	-	%
	-OS	B	25	-	11	-	%
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, +R_S = 510Ω)	+SR	B	25	-	1000	-	V/µs
		B	Full	-	975	-	V/µs
	-SR (Note 5)	B	25	-	650	-	V/µs
		B	Full	-	580	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2)	+SR	B	25	-	1400	-	V/µs
		B	Full	-	1200	-	V/µs
	-SR (Note 5)	B	25	-	800	-	V/µs
		B	Full	-	700	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = -1)	+SR	B	25	-	2100	-	V/µs
		B	Full	-	1900	-	V/µs
	-SR (Note 5)	B	25	-	1000	-	V/µs
		B	Full	-	900	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step, Note 6)	To 0.1%	B	25	-	15	-	ns
	To 0.05%	B	25	-	23	-	ns
	To 0.02%	B	25	-	30	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
DISABLE CHARACTERISTICS							
Disabled Supply Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	3	4	mA
$\overline{DISABLE}$ Input Logic Low		A	Full	-	-	0.8	V
$\overline{DISABLE}$ Input Logic High		A	25, 85	2.0	-	-	V
		A	-40	2.4	-	-	V
$\overline{DISABLE}$ Input Logic Low Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	100	200	µA
$\overline{DISABLE}$ Input Logic High Current	$V_{\overline{DISABLE}}$ = 5V	A	Full	-	1	15	µA
Output Disable Time (Note 6)	V_{IN} = ±1V, $V_{\overline{DISABLE}}$ = 2.4V to 0V	B	25	-	35	-	ns
Output Enable Time (Note 6)	V_{IN} = ±1V, $V_{\overline{DISABLE}}$ = 0V to 2.4V	B	25	-	180	-	ns
Disabled Output Capacitance	$V_{\overline{DISABLE}}$ = 0V	B	25	-	2.5	-	pF
Disabled Output Leakage	$V_{\overline{DISABLE}}$ = 0V, V_{IN} = ∓2V, V_{OUT} = ±3V	A	Full	-	3	10	µA
Off Isolation ($V_{\overline{DISABLE}}$ = 0V, V_{IN} = 1V_{P-P}, Note 6)	At 5MHz	B	25	-	-75	-	dB
	At 25MHz	B	25	-	-60	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Power Supply Current		A	25	-	5.8	6.1	mA
		A	Full	-	5.9	6.3	mA

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. Undershoot dominates for output signal swings below GND (e.g. $0.5V_{P-P}$), yielding a higher overshoot limit compared to the $V_{OUT} = 0$ to 0.5V condition. See the "Application Information" section for details.
5. Slew rates are asymmetrical if the output swings below GND (e.g. a bipolar signal). Positive unipolar output signals have symmetric positive and negative slew rates comparable to the +SR specification. See the "Application Information" section, and the pulse response graphs for details.
6. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1145 design is optimized for $R_F = 510\Omega$ at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains, however, the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For a gain of +1, a resistor ($+R_S$) in series with +IN is required to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	425	300
+1	510 ($+R_S = 510\Omega$)	270
+2	510	330
+5	200	300
+10	180	130

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

$\overline{\text{DISABLE}}$ Input TTL Compatibility

The HFA1145 derives an internal GND reference for the digital circuitry as long as the power supplies are symmetrical about GND. With symmetrical supplies the digital switching threshold ($V_{TH} = (V_{IH} + V_{IL})/2 = (2.0 + 0.8)/2$) is 1.4V, which ensures the TTL compatibility of the $\overline{\text{DISABLE}}$ input. If asymmetrical supplies (e.g. +10V, 0V) are utilized, the switching threshold becomes:

$$V_{TH} = \frac{V+ + V-}{2} + 1.4V$$

and the V_{IH} and V_{IL} levels will be $V_{TH} \pm 0.6V$, respectively.

Optional GND Pad (Die Use Only) for TTL Compatibility

The die version of the HFA1145 provides the user with a GND pad for setting the disable circuitry GND reference. With symmetrical supplies the GND pad may be left unconnected, or tied directly to GND. If asymmetrical supplies (e.g. +10V, 0V) are utilized, and TTL compatibility is desired, die users must connect the GND pad to GND. With an external GND, the $\overline{\text{DISABLE}}$ input is TTL compatible regardless of supply voltage utilized.

Pulse Undershoot and Asymmetrical Slew Rates

The HFA1145 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (See Figures 5, 8, and 11). This undershoot isn't present for small bipolar signals, or large positive signals. Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (See Figures 5, 8, and 11), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (See Figures 4, 7, and 10).

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the device's input and output connections. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 270MHz (for A_V = +1). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, the bandwidth decreases as the load capacitance increases. For example, at A_V = +1, R_S = 62Ω, C_L = 40pF, the overall bandwidth is limited to 180MHz, and bandwidth drops to 75MHz at A_V = +1, R_S = 8Ω, C_L = 400pF.

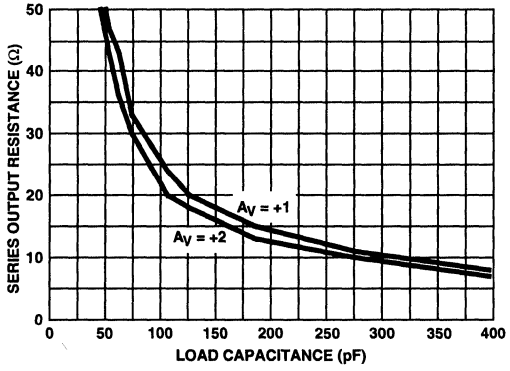


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1145 may be evaluated using the HFA11XX Evaluation Board.

The layout and schematic of the board are shown in Figure 2. The V_H connection may be used to exercise the $\overline{\text{DISABLE}}$ pin, but note that this connection has no 50Ω termination. To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

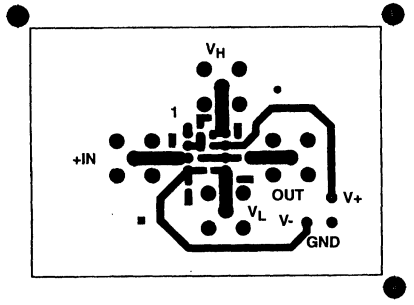


FIGURE 2A. TOP LAYOUT

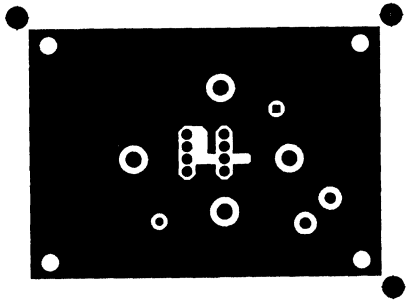


FIGURE 2B. TOP LAYOUT

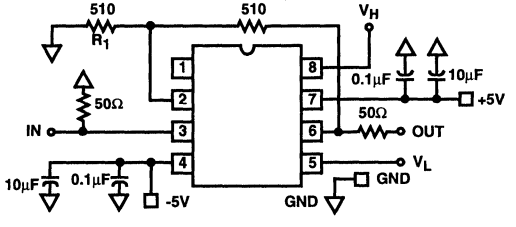


FIGURE 2C. TOP LAYOUT

FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

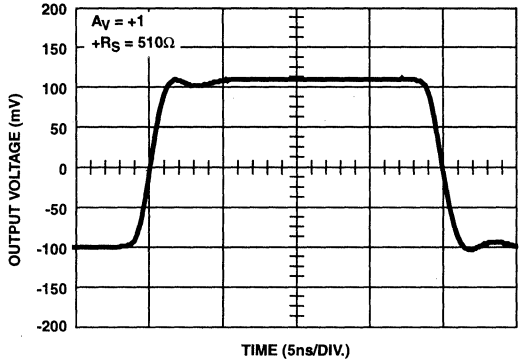


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

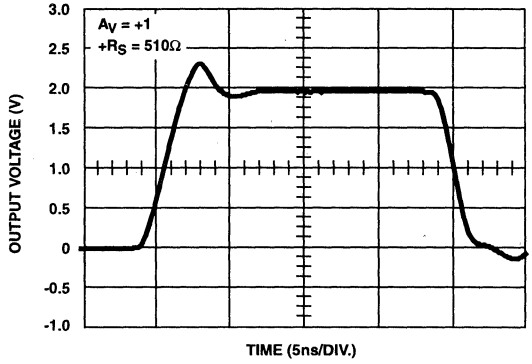


FIGURE 4. LARGE SIGNAL POSITIVE PULSE RESPONSE

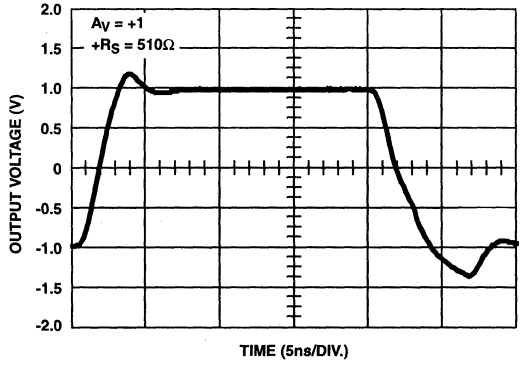


FIGURE 5. LARGE SIGNAL BIPOLAR PULSE RESPONSE

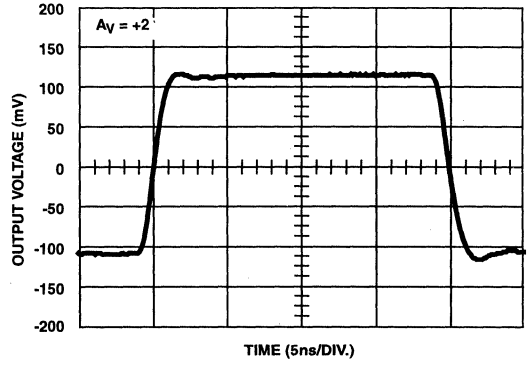


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

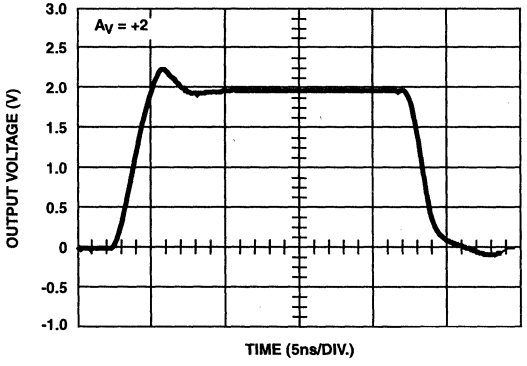


FIGURE 7. LARGE SIGNAL POSITIVE PULSE RESPONSE

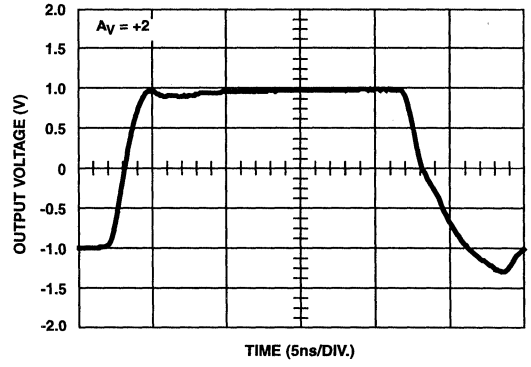


FIGURE 8. LARGE SIGNAL BIPOLAR PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

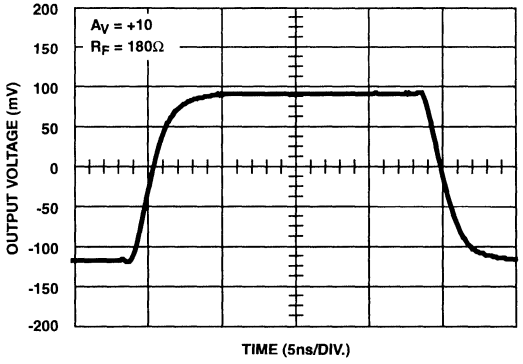


FIGURE 9. SMALL SIGNAL PULSE RESPONSE

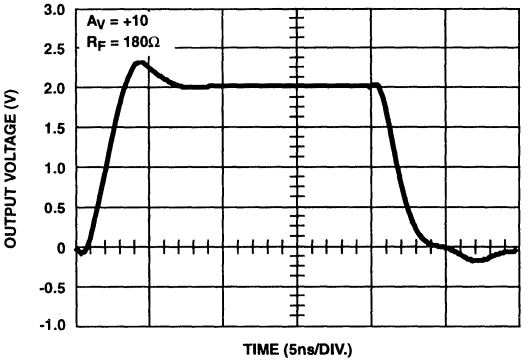


FIGURE 10. LARGE SIGNAL POSITIVE PULSE RESPONSE

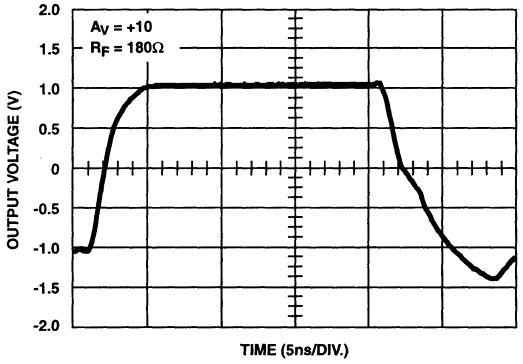


FIGURE 11. LARGE SIGNAL BIPOLAR PULSE RESPONSE

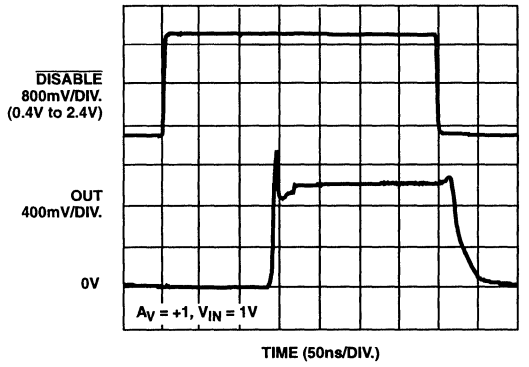


FIGURE 12. OUTPUT ENABLE AND DISABLE RESPONSE

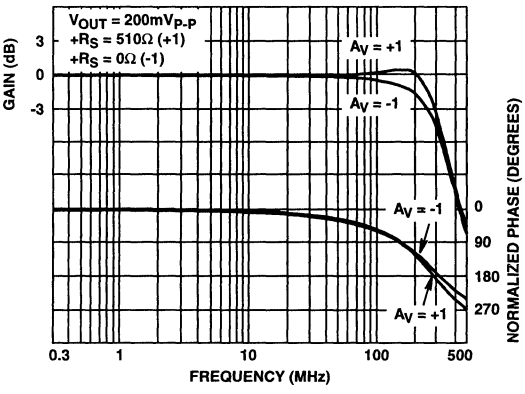


FIGURE 13. FREQUENCY RESPONSE

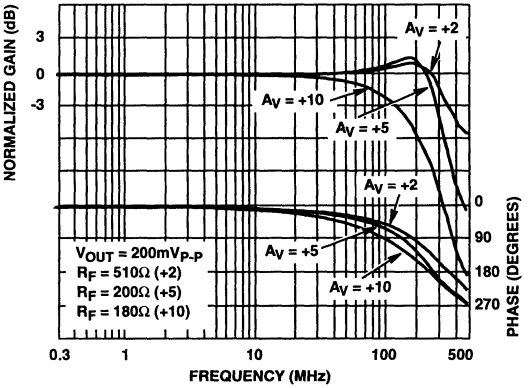


FIGURE 14. FREQUENCY RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

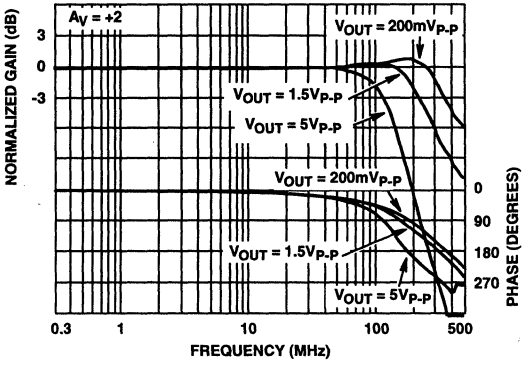


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

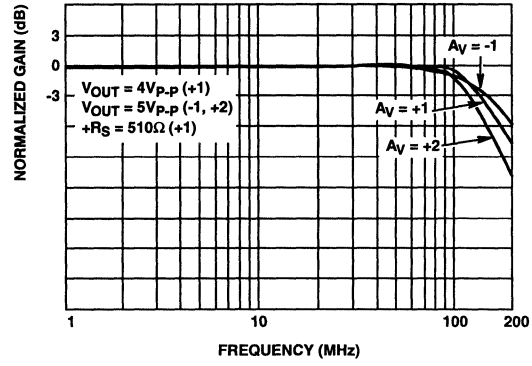


FIGURE 16. FULL POWER BANDWIDTH

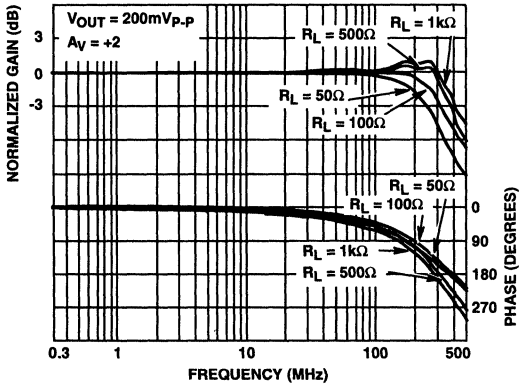


FIGURE 17. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

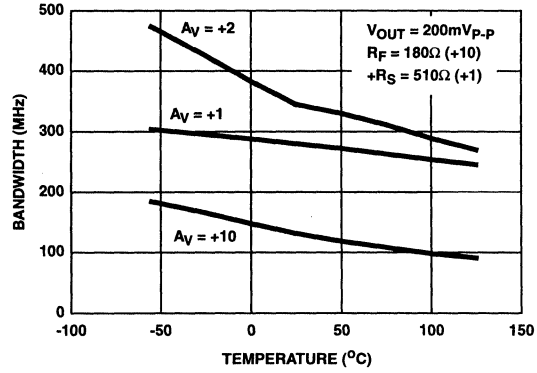


FIGURE 18. -3dB BANDWIDTH vs TEMPERATURE

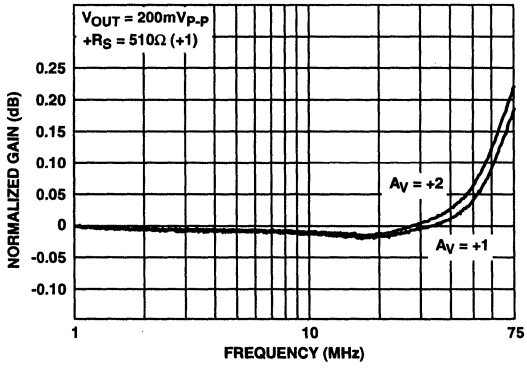


FIGURE 19. GAIN FLATNESS

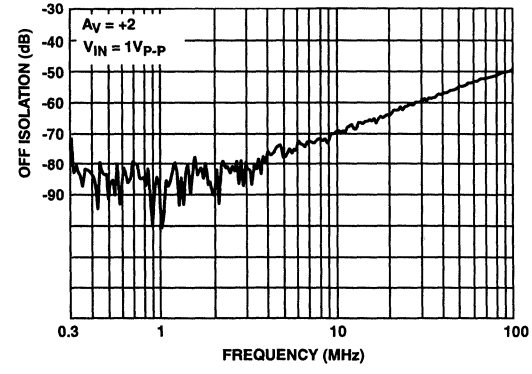


FIGURE 20. OFF ISOLATION

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

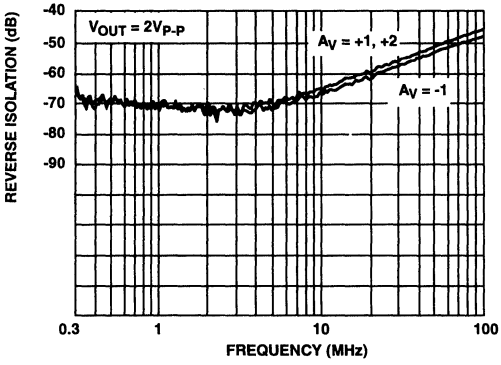


FIGURE 21. REVERSE ISOLATION (S_{12})

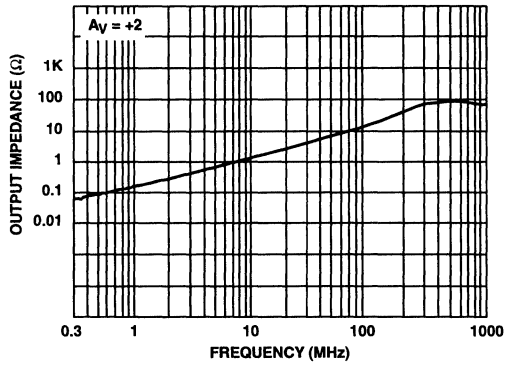


FIGURE 22. ENABLED OUTPUT IMPEDANCE

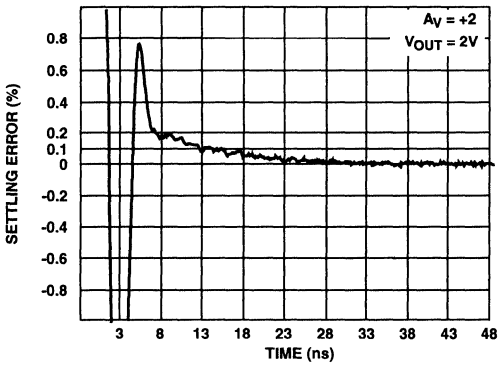


FIGURE 23. SETTLING RESPONSE

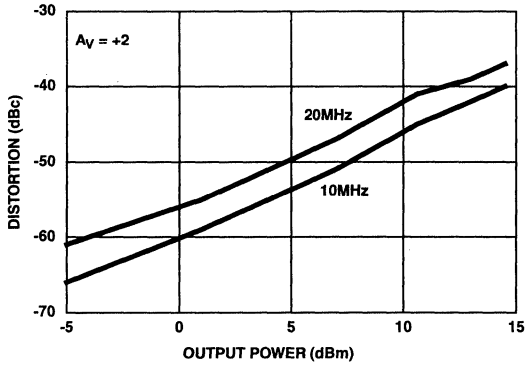


FIGURE 24. SECOND HARMONIC DISTORTION vs P_{OUT}

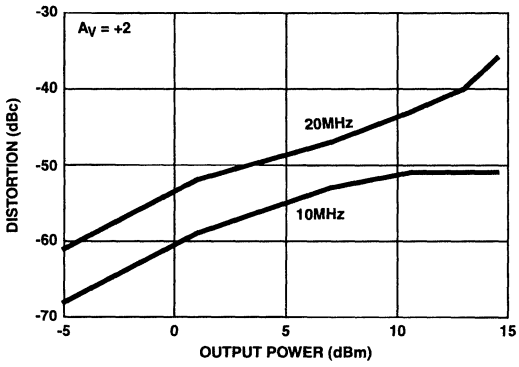


FIGURE 25. THIRD HARMONIC DISTORTION vs P_{OUT}

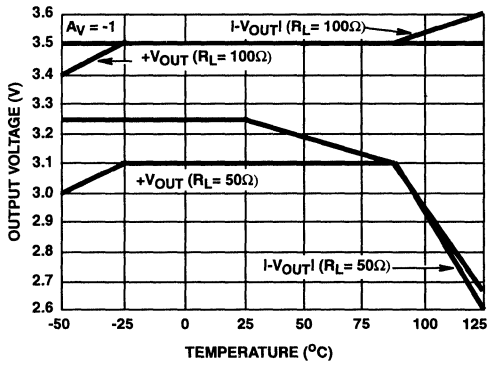


FIGURE 26. OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

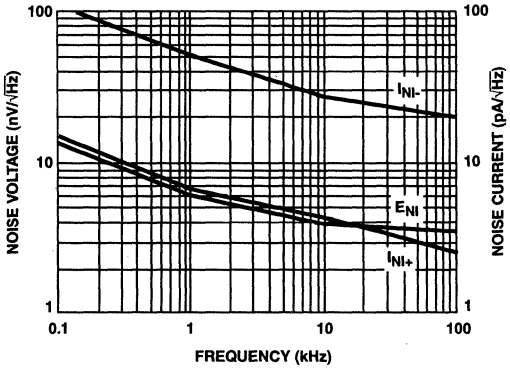


FIGURE 27. INPUT NOISE CHARACTERISTICS

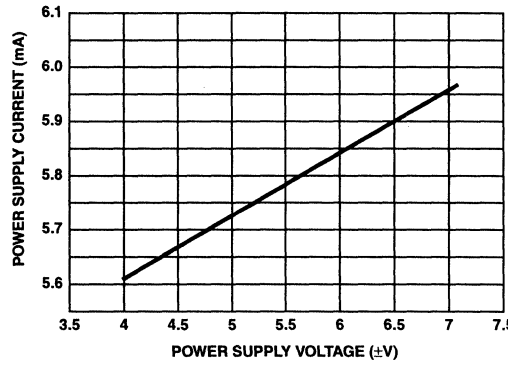


FIGURE 28. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

59 mils x 59 mils x 19 mils
1500µm x 1500µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

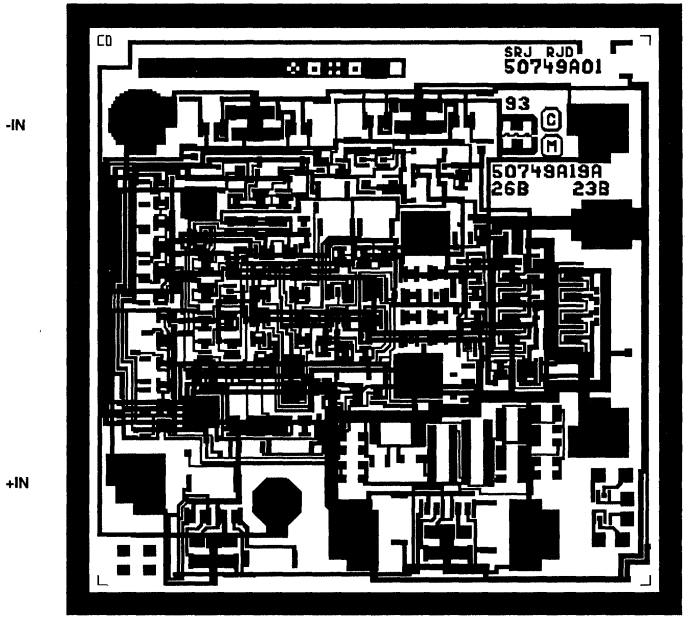
75

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1145



NOTE: This pad is not bonded out on packaged units. Die users may set a GND reference, via this pad, to ensure the TTL compatibility of the $\overline{DIS}$ input when using asymmetrical supplies (e.g. V+ = 10V, V- = 0V). See the "Application Information" section for details.

HARRIS SEMICONDUCTOR

HFA1205

Dual, 400MHz, Low Power, Video Operational Amplifier

November 1996

Features

- Low Supply Current ..... 5.8mA/Op Amp
- High Input Impedance 2MΩ
- Wide -3dB Bandwidth (A_V = +2) 400MHz
- Very Fast Slew Rate 1275V/μs
- Gain Flatness (to 50MHz) ..... ±0.03dB
- Differential Gain 0.03%
- Differential Phase ..... 0.03 Degrees
- Pin Compatible Upgrade to HA5023

Applications

- Flash A/D Drivers
- High Resolution Monitors
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- High Speed Oscilloscopes and Analyzers

Description

The HFA1205 is a dual, high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

These amplifiers deliver 400MHz bandwidth and 1275V/μs slew rate, on only 60mW of quiescent power. They are specifically designed to meet the performance, power, and cost requirements of high volume video applications. The excellent gain flatness and differential gain/phase performance make these amplifiers well suited for component or composite video applications. Video performance is maintained even when driving a back terminated cable (R_L = 150Ω), and degrades only slightly when driving two back terminated cables (R_L = 75Ω). RGB applications will benefit from the high slew rates, and high full power bandwidth.

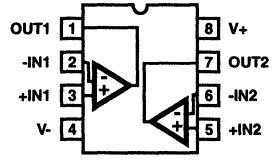
The HFA1205 is a pin compatible, low power, high performance upgrade for the popular Harris HA5023. For a dual amplifier with output disable capability, please see the HFA1245 datasheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1205IP	-40 to 85	8 Ld PDIP	E8.3
HFA1205IB (H1205I)	-40 to 85	8 Ld SOIC	M8.15
HA5023EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HFA1205
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3605.4**

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) ..... Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) ... 600V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	130
SOIC Package	160

Maximum Junction Temperature (Die Only) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range ..... -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	ΔV_{CM} = ±1.8V	A	25	45	48	-	dB
	ΔV_{CM} = ±1.8V	A	85	43	46	-	dB
	ΔV_{CM} = ±1.2V	A	-40	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV_{PS} = ±1.8V	A	25	48	52	-	dB
	ΔV_{PS} = ±1.8V	A	85	46	50	-	dB
	ΔV_{PS} = ±1.2V	A	-40	46	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	0.5	1	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	0.8	3	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±1.8V	A	25	0.8	2	-	MΩ
	ΔV_{CM} = ±1.8V	A	85	0.5	1.3	-	MΩ
	ΔV_{CM} = ±1.2V	A	-40	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	25	-	2	8.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Bias Current Common-Mode Sensitivity	ΔV_{CM} = ±1.8V	A	25	-	3	6	µA/V
	ΔV_{CM} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{CM} = ±1.2V	A	-40	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	60	-	Ω
Input Capacitance		C	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density	f = 100kHz	B	25	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain	A_V = -1	C	25	-	500	-	kΩ
AC CHARACTERISTICS A_V = +2, R_F = 464Ω, Unless Otherwise Specified							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})	A_V = +1, $+R_S$ = 432Ω	B	25	-	280	-	MHz
	A_V = +2	B	25	-	400	-	MHz
	A_V = -1, R_F = 332Ω	B	25	-	360	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1)	A_V = +1, R_S = 432Ω	B	25	-	140	-	MHz
	A_V = +2	B	25	-	125	-	MHz
	A_V = -1, R_F = 332Ω	B	25	-	180	-	MHz
Gain Flatness (A_V = +2, V_{OUT} = 0.2V_{P-P})	To 25MHz	B	25	-	±0.02	-	dB
	To 50MHz	B	25	-	±0.03	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
Crosstalk	5MHz	B	25	-	-60	-	dB
	10MHz	B	25	-	-54	-	dB
OUTPUT CHARACTERISTICS R_F = 560Ω, Unless Otherwise Specified							
Output Voltage Swing	A_V = -1, R_L = 100Ω	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current	A_V = -1, R_L = 50Ω	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
Closed Loop Output Impedance	DC, A_V = +2, R_F = 464Ω	B	25	-	0.07	-	Ω

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Second Harmonic Distortion (A_V = +2, R_F = 464Ω, V_{OUT} = $2V_{P-P}$)	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Third Harmonic Distortion (A_V = +2, R_F = 464Ω, V_{OUT} = $2V_{P-P}$)	10MHz	B	25	-	-55	-	dBc
	20MHz	B	25	-	-50	-	dBc
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 464Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = $0.5V_{P-P}$)	Rise Time	B	25	-	0.8	-	ns
	Fall Time	B	25	-	1.25	-	ns
Overshoot	V_{OUT} = $0.5V_{P-P}$, V_{IN} t_{RISE} = 2.5ns	B	25	-	5	-	%
Slew Rate (V_{OUT} = $4V_{P-P}$, A_V = +1, +R_S = 432Ω)	+SR	B	25	-	1050	-	V/µs
	-SR	B	25	-	750	-	V/µs
Slew Rate (V_{OUT} = $5V_{P-P}$, A_V = +2)	+SR	B	25	-	1375	-	V/µs
	-SR	B	25	-	875	-	V/µs
Slew Rate (V_{OUT} = $5V_{P-P}$, A_V = -1, R_F = 332Ω)	+SR	B	25	-	2250	-	V/µs
	-SR	B	25	-	1275	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step)	To 0.1%	B	25	-	15	-	ns
	To 0.05%	B	25	-	20	-	ns
	To 0.02%	B	25	-	30	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	10	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 464Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current		A	25	5.6	5.8	6.1	mA/ Op Amp
		A	Full	5.4	5.9	6.3	mA/ Op Amp

NOTE:

3. Test Level: A. Production Tested.; B. Typical or Guaranteed Limit Based on Characterization.; C. Design Typical for Information Only.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1205 design is optimized for a 464Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better. Note that a series input resistor, on +IN, is required for a gain of +1, to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	332	360
+1	464 (+R_S = 432Ω)	280
+2	464	400

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 280MHz (for A_V = +1). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth decreases as the load capacitance increases. For example, at A_V = +1, R_S = 62Ω, C_L = 40pF, the overall bandwidth is limited to 180MHz, and bandwidth drops to 70MHz at A_V = +1, R_S = 8Ω, C_L = 400pF.

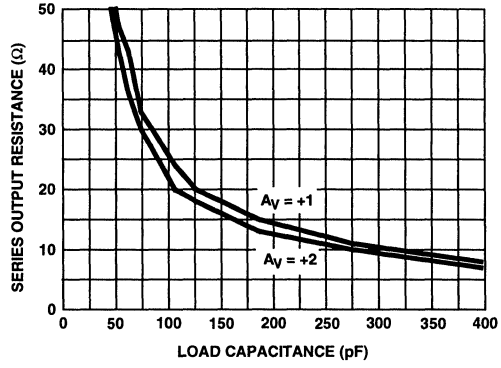


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1205 may be evaluated using the HA5023 Evaluation Board. The feedback and gain setting resistors must be replaced with the appropriate value (see "Optimum Feedback Resistor" section) for the gain being evaluated.

To order evaluation boards (Part Number HA5023EVAL), please contact your local sales office.

Typical Performance Curves

V_{SUPPLY} = ±5V, R_F = Optimum Value From "Apps Info" Table, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified

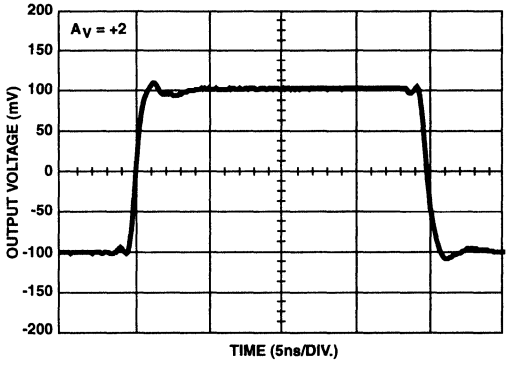


FIGURE 2. SMALL SIGNAL PULSE RESPONSE

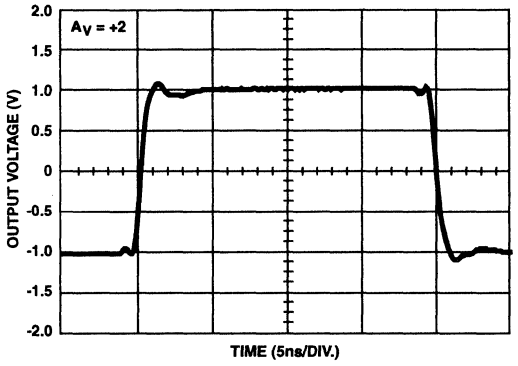


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

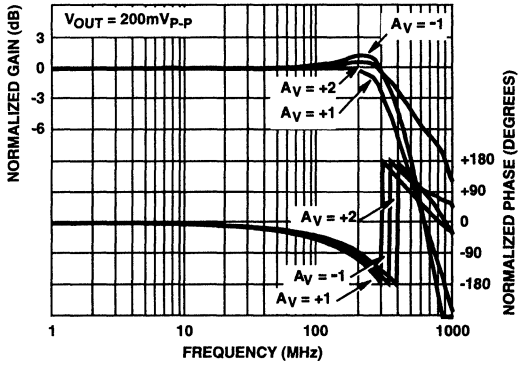


FIGURE 4. FREQUENCY RESPONSE

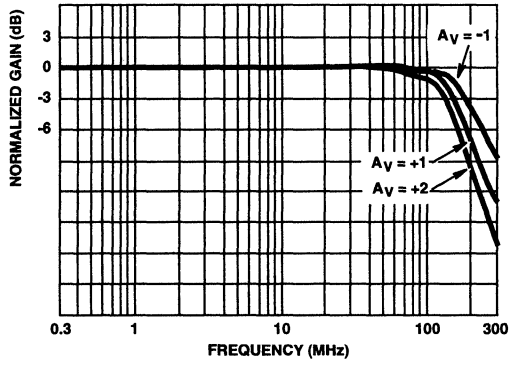


FIGURE 5. FULL POWER BANDWIDTH

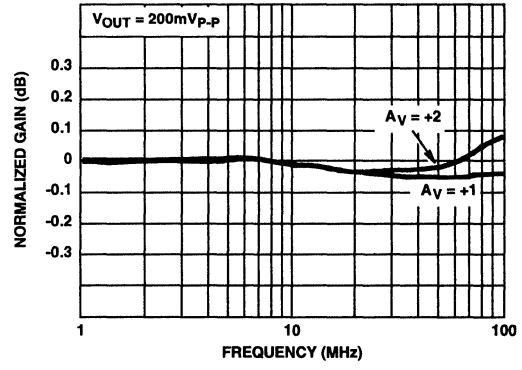


FIGURE 6. GAIN FLATNESS

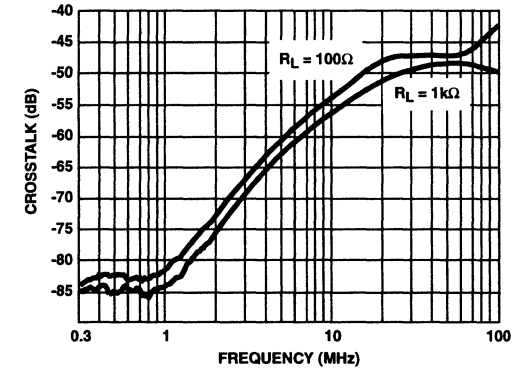


FIGURE 7. CROSSTALK vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

69 mils x 92 mils x 19 mils
1750µm x 2330µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

PASSIVATION:

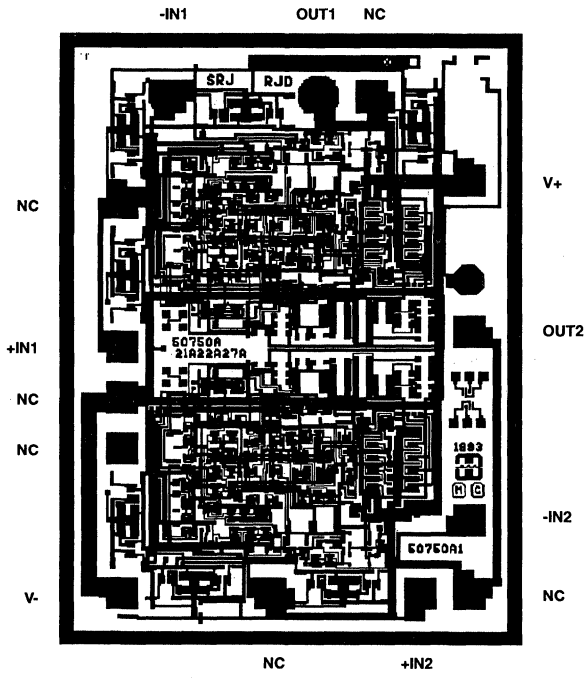
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

180

Metallization Mask Layout

HFA1205



HARRIS SEMICONDUCTOR

HFA1212

Dual 350MHz, Low Power Closed Loop Buffer Amplifier

August 1996

Features

- Differential Gain 0.025%
- Differential Phase ..... 0.03 Degrees
- Wide -3dB Bandwidth (A_V = +2) 350MHz
- Very Fast Slew Rate (A_V = -1) 1100V/µs
- Low Supply Current 6mA/Buffer
- High Output Current 60mA
- Excellent Gain Accuracy 0.99V/V
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Overdrive Recovery 8ns
- Standard Operational Amplifier Pinout

Applications

- High Resolution Monitors
- Professional Video Processing
- Medical Imaging
- Video Digitizing Boards/Systems
- RF/IF Processors
- Battery Powered Communications
- Flash Converter Drivers
- High Speed Pulse Amplifiers

Description

The HFA1212 is a dual closed loop Buffer featuring user programmable gain and high speed performance. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, these devices offer wide -3dB bandwidth of 350MHz, very fast slew rate, excellent gain flatness and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

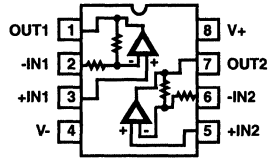
Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date. For Military product, refer to the HFA1212/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1212IP	-40 to 85	8 Ld PDIP	E8.3
HFA1212IB (H1212I)	-40 to 85	8 Ld SOIC	M8.15

Pinout

HFA1212
(PDIP, SOIC)
TOP VIEW



3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 3607.3

Absolute Maximum Rating

Supply Voltage (V+ to V-) 11V
DC Input Voltage . . . . . V_{SUPPLY}
Output Current (Note 1) . . . . . Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	130
SOIC Package	160

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Output Offset Voltage		A	25	-	2	10	mV
		A	Full	-	3	15	mV
Average Output Offset Voltage Drift		B	Full	-	22	70	µV/°C
Channel-to-Channel Output Offset Voltage Mismatch		A	25	-	-	15	mV
		A	Full	-	-	30	mV
Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	42	45	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	40	44	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	40	45	-	dB
Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	45	49	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	43	48	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	43	48	-	dB
Input Bias Current		A	25	-	1	15	µA
		A	Full	-	3	25	µA
Input Bias Current Drift		B	Full	-	30	80	nA/°C
Channel-to-Channel Input Bias Current Mismatch		A	25	-	-	15	µA
		A	Full	-	-	25	µA
Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.25V$	A	25	-	0.5	1	µA/V
		A	Full	-	-	3	µA/V
Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.1	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	1.4	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	1.3	-	MΩ
Inverting Input Resistance		C	25	-	350	-	Ω
Input Capacitance		C	25	-	2	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR and $+R_{IN}$ tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 4)	f = 100kHz	B	25	-	7	-	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 4)	f = 100kHz	B	25	-	3.6	-	$pA/\sqrt{Hz}$

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS							
Gain (V_{IN} = -1V to +1V)	A_V = -1	A	25	-0.98	0.996	-1.02	V/V
		A	Full	0.975	1.000	-1.025	V/V
	A_V = +1	A	25	0.98	0.992	1.02	V/V
		A	Full	0.975	0.993	1.025	V/V
	A_V = +2	A	25	1.96	1.988	2.04	V/V
		A	Full	1.95	1.990	2.05	V/V
Channel-to-Channel Gain Mismatch	A_V = -1	A	25	-	-	±0.02	V/V
		A	Full	-	-	±0.025	V/V
	A_V = +1	A	25	-	-	±0.025	V/V
		A	Full	-	-	±0.025	V/V
	A_V = +2	A	25	-	-	±0.04	V/V
		A	Full	-	-	±0.05	V/V
AC CHARACTERISTICS							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 4)	A_V = -1	B	25	-	300	-	MHz
	A_V = +1, +R_S = 620Ω	B	25	-	240	-	MHz
	A_V = +2	B	25	-	350	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2 or -1, V_{OUT} = 4V_{P-P} at A_V = +1, Note 4)	A_V = -1	B	25	-	165	-	MHz
	A_V = +1, +R_S = 620Ω	B	25	-	150	-	MHz
	A_V = +2	B	25	-	125	-	MHz
Gain Flatness (V_{OUT} = 0.2V_{P-P}, Note 4)	A_V = +2, To 25MHz	B	25	-	±0.03	-	dB
	A_V = +2, To 50MHz	B	25	-	±0.04	-	dB
Crosstalk (All Channels Hostile, Note 4)	5MHz	B	25	-	-65	-	dB
	10MHz	B	25	-	-60	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing (Note 4)	A_V = -1	A	25	±3.0	±3.2	-	V
		A	Full	±2.8	±3.0	-	V
Output Current (Note 4)	A_V = -1, R_L = 50Ω	A	25, 85	50	55	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	100	-	mA
DC Closed Loop Output Impedance	A_V = +2	B	25	-	0.2	-	Ω
Second Harmonic Distortion (A_V = +2, V_{OUT} = 2V_{P-P}, Note 4)	10MHz	B	25	-	-60	-	dBc
	20MHz	B	25	-	-50	-	dBc
Third Harmonic Distortion (A_V = +2, V_{OUT} = 2V_{P-P}, Note 4)	10MHz	B	25	-	-60	-	dBc
	20MHz	B	25	-	-50	-	dBc
Reverse Isolation (S_{12}, Note 4)	30MHz, A_V = +2	B	25	-	-65	-	dB
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P})	Rise Time	B	25	-	1.0	-	ns
	Fall Time	B	25	-	1.1	-	ns
Overshoot (V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 1ns, Note 5)	+OS	B	25	-	4	-	%
	-OS	B	25	-	13	-	%

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS		(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
Slew Rate (V_{OUT} = 5V_{P-P} at A_V = +2 or -1, V_{OUT} = 4V_{P-P} at A_V = +1)	A_V = -1	+SR	B	25	-	2000	-	V/µs
		-SR	B	25	-	1150	-	V/µs
	A_V = +1, +R_S = 620Ω	+SR	B	25	-	1100	-	V/µs
		-SR	B	25	-	850	-	V/µs
	A_V = +2	+SR	B	25	-	1300	-	V/µs
		-SR	B	25	-	900	-	V/µs
Settling Time (V_{OUT} = +2V to 0V Step, Note 4)	To 0.1%		B	25	-	24	-	ns
	To 0.05%		B	25	-	37	-	ns
	To 0.02%		B	25	-	60	-	ns
Overdrive Recovery Time	V_{IN} = ±2V		B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS								
Differential Gain (f = 3.58MHz, A_V = +2)	R_L = 150Ω		B	25	-	0.025	-	%
Differential Phase (f = 3.58MHz, A_V = +2)	R_L = 150Ω		B	25	-	0.03	-	Degrees
POWER SUPPLY CHARACTERISTICS								
Power Supply Range			C	25	±4.5	-	±5.5	V
Power Supply Current			A	25	-	5.9	6.1	mA/Op Amp
			A	Full	-	6.1	6.3	mA/Op Amp

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. See Typical Performance Curves for more information.
5. Negative overshoot dominates for output signal swings below GND (e.g. 0.5V_{P-P}), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 0.5V condition. See the "Application Information" section for details.

Application Information

HFA1212 Advantages

The HFA1212 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space. Implementing a dual, gain of 2, cable driver with this IC eliminates the four gain setting resistors, which frees up board space for termination resistors.

Like most newer high performance amplifiers, the HFA1212 is a current feedback amplifier (CFA). CFAs offer high bandwidth and slew rate at low supply currents, but can be difficult to use because of their sensitivity to feedback capacitance and parasitics on the inverting input (summing node). The HFA1212 eliminates these concerns by bringing the gain setting resistors on-chip. This yields the optimum placement and value of the feedback resistor, while minimizing feedback and summing node parasitics. Because there is no access to the summing node, the PCB parasitics do not impact performance at gains of +2 or -1 (see "Unity Gain Considerations" for discussion of parasitic impact on unity gain performance).

The HFA1212's closed loop gain implementation provides better gain accuracy, lower offset and output impedance, and better distortion compared with open loop buffers.

Closed Loop Gain Selection

This "buffer" operates in closed loop gains of -1, +1, or +2, with gain selection accomplished via connections to the inputs Applying the input signal to +IN and floating -IN selects a gain of +1 (see next section for layout caveats), while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded through a 50Ω resistor.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT	-INPUT
-1	50Ω to GND	Input
+1	Input	NC (Floating)
+2	Input	GND

Unity Gain Considerations

Unity gain selection is accomplished by floating the -Input of the HFA1212. Anything that tends to short the -Input to GND, such as stray capacitance at high frequencies, will cause the amplifier gain to increase toward a gain of +2. The result is excessive high frequency peaking, and possible instability. Even the minimal amount of capacitance associated with attaching the -Input lead to the PCB results in approximately 6dB of gain peaking. At a minimum this requires due care to ensure the minimum capacitance at the -Input connection.

TABLE 1. UNITY GAIN PERFORMANCE FOR VARIOUS IMPLEMENTATIONS

APPROACH	PEAKING (dB)	BW (MHz)	±0.1dB GAIN FLATNESS (MHz)
Remove -IN Pin	4.5	430	21
$+R_S = 620\Omega$	0	220	27
$+R_S = 620\Omega$ and Remove -IN Pin	0.5	215	15
Short +IN to -IN (e.g., Pins 2 and 3)	0.6	280	70
100pF Capacitor Between +IN and -IN	0.7	290	40

Table 1 lists five alternate methods for configuring the HFA1212 as a unity gain buffer, and the corresponding performance. The implementations vary in complexity and involve performance trade-offs. The easiest approach to implement is simply shorting the two input pins together, and applying the input signal to this common node. The amplifier bandwidth decreases from 430MHz to 280MHz, but excellent gain flatness is the benefit. A drawback to this approach is that the amplifier input noise voltage and input offset voltage terms see a gain of +2, resulting in higher noise and output offset voltages. Alternately, a 100pF capacitor between the inputs shorts them only at high frequencies, which prevents the increased output offset voltage but delivers less gain flatness.

Another straightforward approach is to add a 620Ω resistor in series with the amplifier's positive input. This resistor and the HFA1212 input capacitance form a low pass filter which rolls off the signal bandwidth before gain peaking occurs. This configuration was employed to obtain the data sheet AC and transient parameters for a gain of +1.

Pulse Overshoot

The HFA1212 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased overshoot on the negative portion of the output waveform (see Figure 6, Figure 9, and Figure 12). This overshoot isn't present for small bipolar signals (see Figure 4, Figure 7, and Figure 10) or large positive signals (see Figure 5, Figure 8 and Figure 11).

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board (PCB). **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section. An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 350MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth decreases as the load capacitance increases.

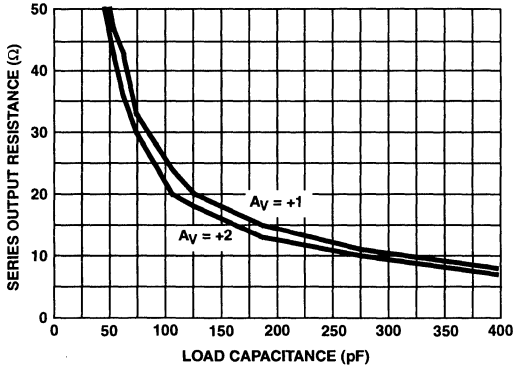


FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1212 may be evaluated using the HA5023 Evaluation Board, slightly modified as follows:

1. Remove the two feedback resistors, and leave the connections open.
2. a. For A_V = +1 evaluation, remove the gain setting resistors (R_1), and leave pins 2 and 6 floating.
   b. For A_V = +2, replace the gain setting resistors (R_1) with 0Ω resistors to GND.

The modified schematic for amplifier 1, and the board layout are shown in Figures 2 and 3.

To order evaluation boards (part number HA5023EVAL), please contact your local sales office.

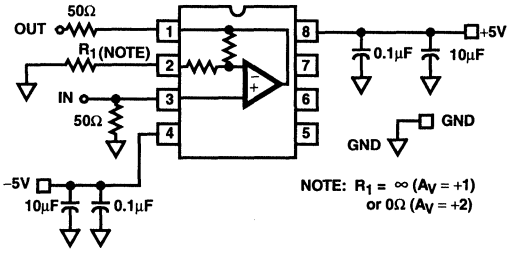


FIGURE 2. MODIFIED EVALUATION BOARD SCHEMATIC

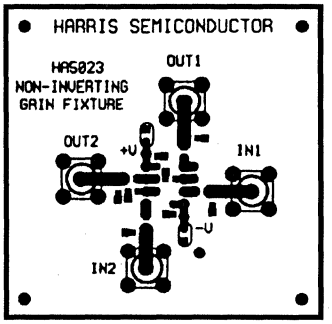


FIGURE 3A. TOP LAYOUT

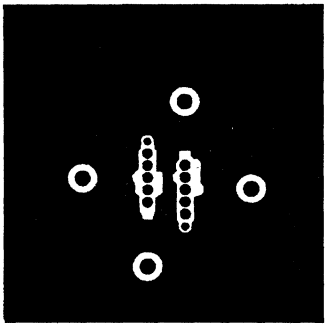


FIGURE 3B. BOTTOM LAYOUT

FIGURE 3. EVALUATION BOARD LAYOUT

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified

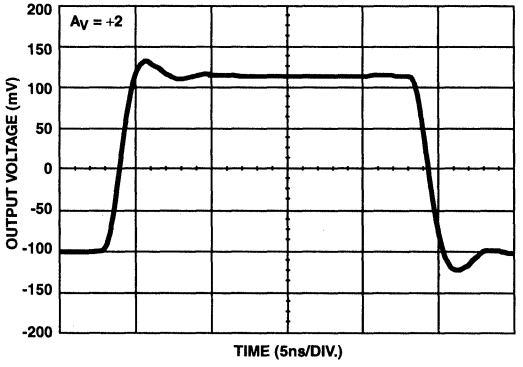


FIGURE 4. SMALL SIGNAL PULSE RESPONSE

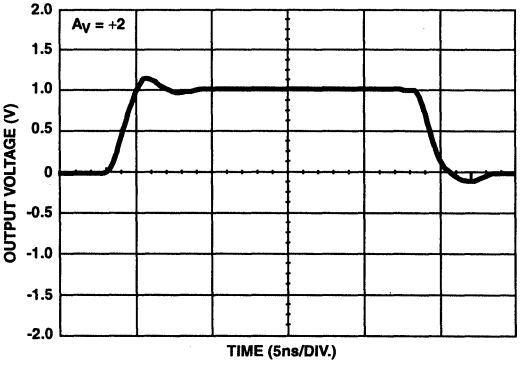


FIGURE 5. LARGE SIGNAL POSITIVE PULSE RESPONSE

Typical Performance Curves (Continued) $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

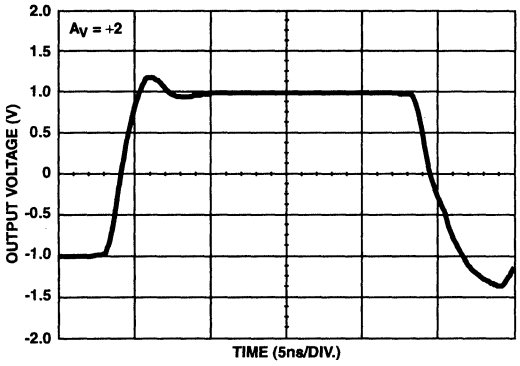


FIGURE 6. LARGE SIGNAL BIPOLAR PULSE RESPONSE

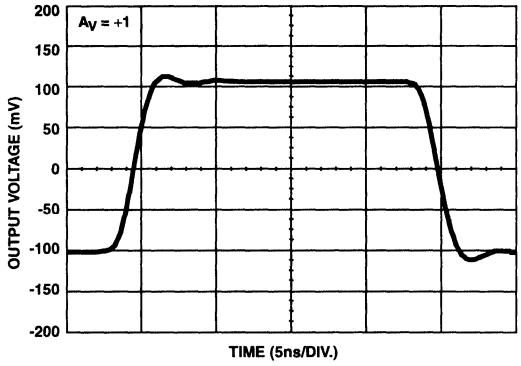


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

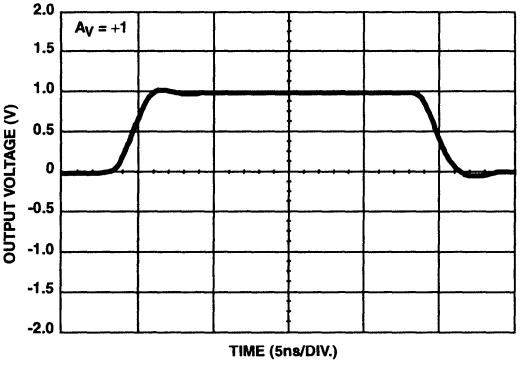


FIGURE 8. LARGE SIGNAL POSITIVE PULSE RESPONSE

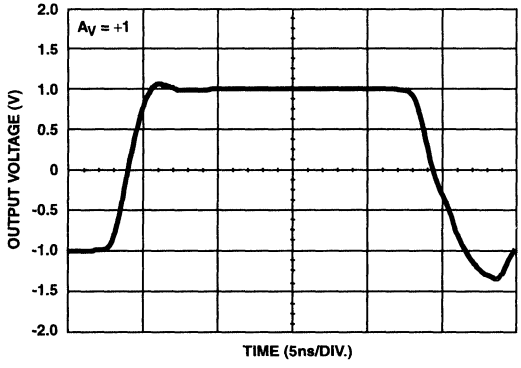


FIGURE 9. LARGE SIGNAL BIPOLAR PULSE RESPONSE

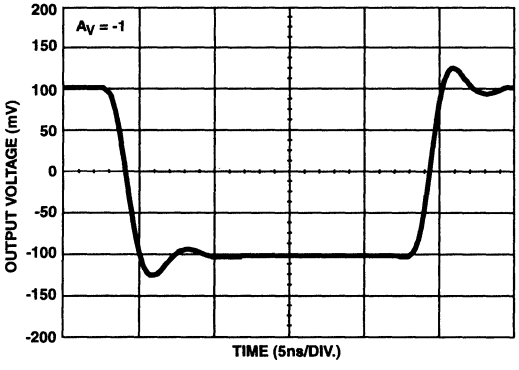


FIGURE 10. SMALL SIGNAL PULSE RESPONSE

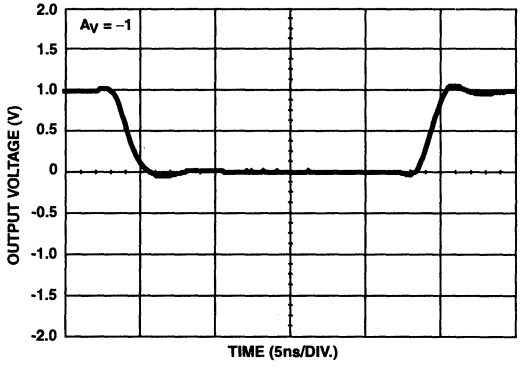


FIGURE 11. LARGE SIGNAL POSITIVE PULSE RESPONSE

Typical Performance Curves (Continued) $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

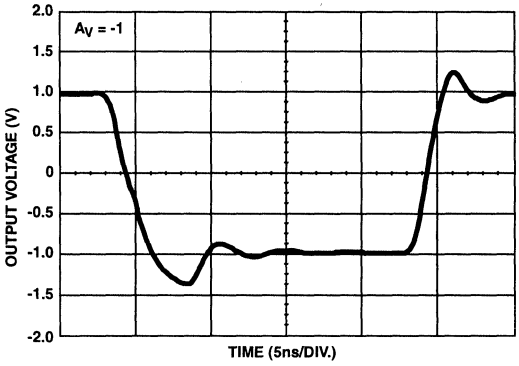


FIGURE 12. LARGE SIGNAL BIPOLAR PULSE RESPONSE

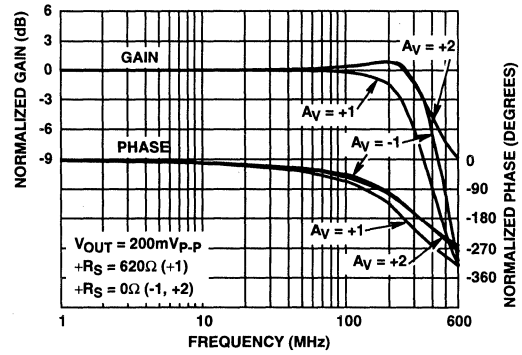


FIGURE 13. FREQUENCY RESPONSE

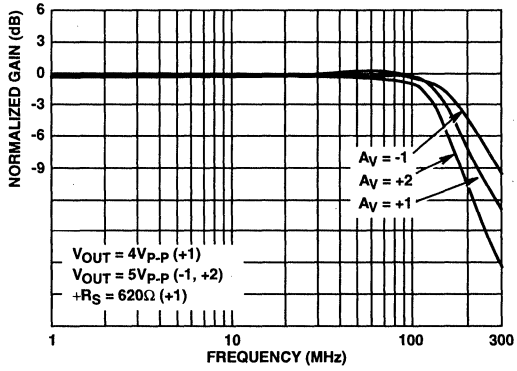


FIGURE 14. FULL POWER BANDWIDTH

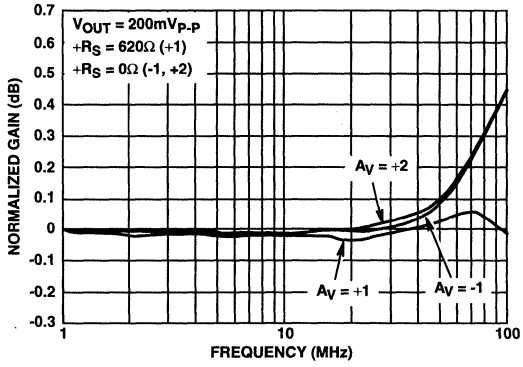


FIGURE 15. GAIN FLATNESS

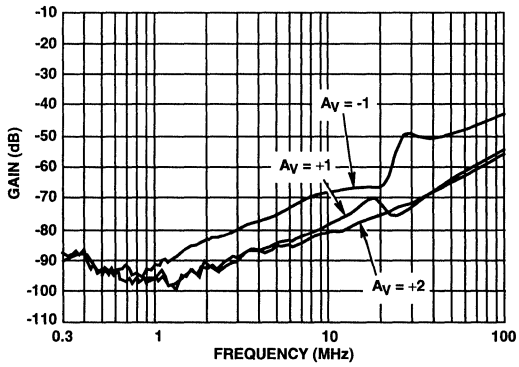


FIGURE 16. REVERSE ISOLATION

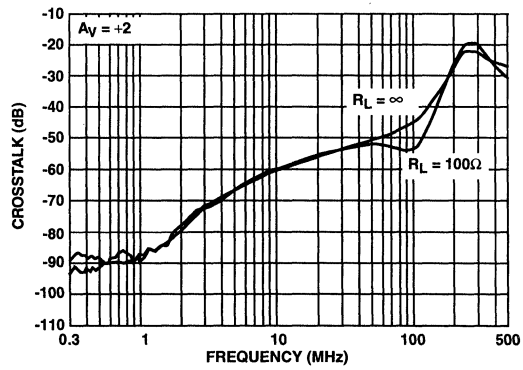


FIGURE 17. ALL HOSTILE CROSSTALK

Typical Performance Curves (Continued) $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

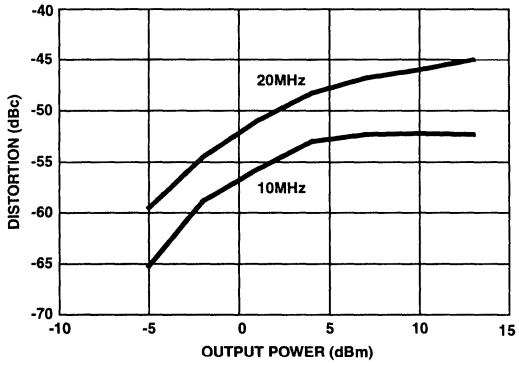


FIGURE 18. 2nd HARMONIC DISTORTION vs P_{OUT}

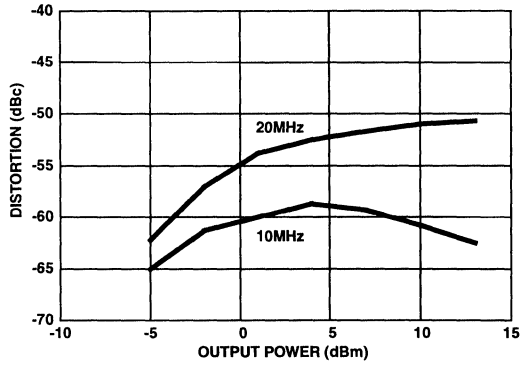


FIGURE 19. 3rd HARMONIC DISTORTION vs P_{OUT}

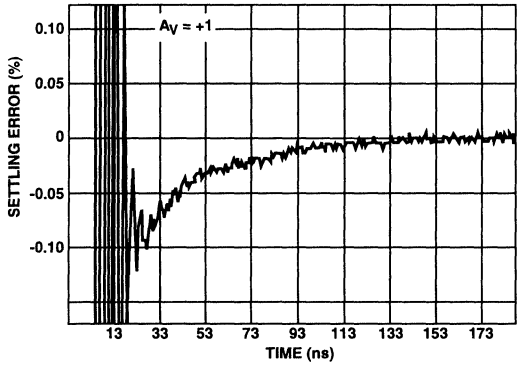


FIGURE 20. SETTLING RESPONSE

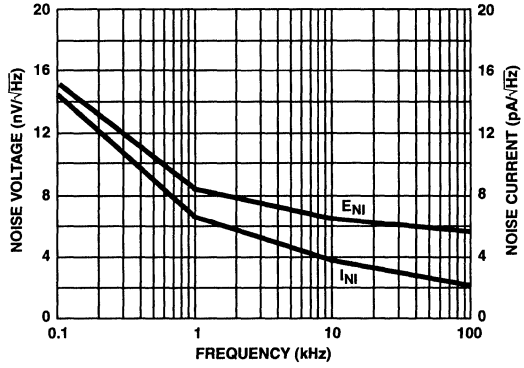


FIGURE 21. INPUT NOISE CHARACTERISTICS

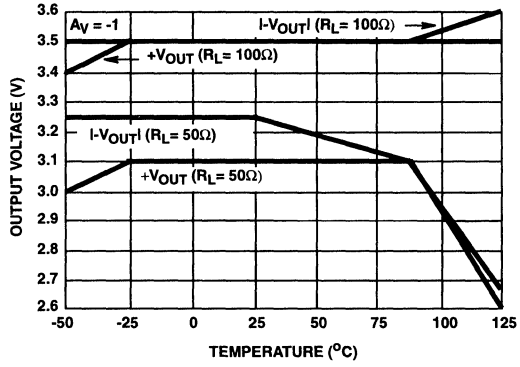


FIGURE 22. OUTPUT VOLTAGE vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

69 mils x 92 mils x 19 mils
1750µm x 2330µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

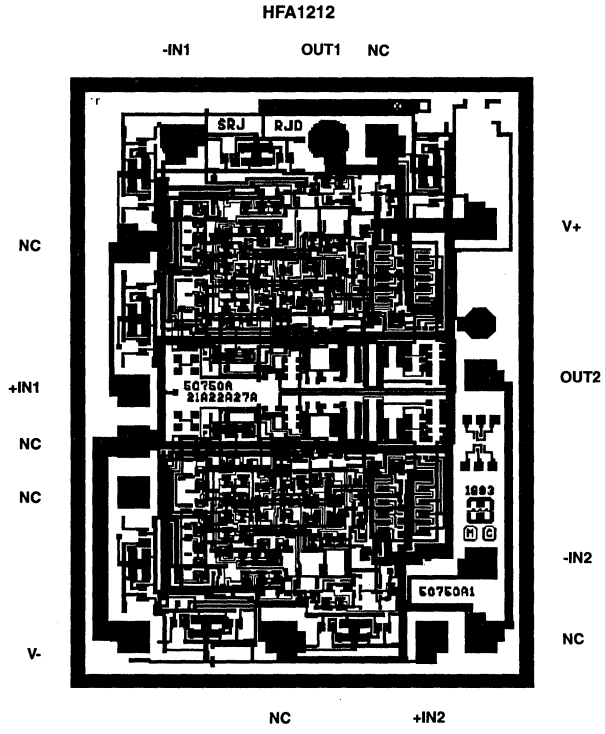
180

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1212



HARRIS SEMICONDUCTOR

HFA1245

Dual, 530MHz, Low Power, Video Operational Amplifier with Disable

November 1996

Features

- Low Supply Current . . . . . 5.8mA/Op Amp
- High Input Impedance 2MΩ
- Low Crosstalk (5MHz) . . . . . -73dB
- High Off Isolation (5MHz) . . . . . -61dB
- Wide -3dB Bandwidth (A_V = +2) 530MHz
- Very Fast Slew Rate 1050V/μs
- Gain Flatness (to 50MHz) . . . . . ±0.11dB
- Differential Gain 0.02%
- Differential Phase . . . . . 0.03 Degrees
- Individual Output Enable/Disable
- Output Enable/Disable Time 160ns/20ns
- Pin Compatible Upgrade to HA5022

Applications

- Flash A/D Drivers
- High Resolution Monitors
- Video Multiplexers
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- High Speed Oscilloscopes and Analyzers

Description

The HFA1245 is a dual, high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

The HFA1245 features individual TTL/CMOS compatible disable controls. When pulled low they disable the corresponding amplifier, which reduces the supply current and forces the output into a high impedance state. This feature allows easy implementation of simple, low power video switching and routing systems. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications.

Multiplexed A/D applications will also find the HFA1245 useful as the A/D driver/multiplexer.

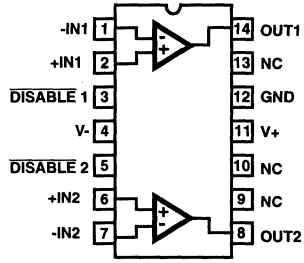
The HFA1245 is a low power, high performance upgrade for the popular Harris HA5022. For a dual amplifier without disable, in a standard 8 lead pinout, please see the HFA1205 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1245IP	-40 to 85	14 Ld PDIP	E14.3
HFA1245IB	-40 to 85	14 Ld SOIC	M14.15
HA5022EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HFA1245
(PDIP, SOIC)
TOP VIEW



3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number **3682.2**

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage. 8V
Output Current (Note 2) . . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	100
SOIC Package	120

Maximum Junction Temperature (Die). . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s). . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 560\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	45	48	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	43	46	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	48	52	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	46	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	46	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	1.3	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	25	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40	-	4	8	µA/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	40	-	Ω
Input Capacitance		C	25	-	2.5	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density	f = 100kHz	B	25	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain	A_V = -1	C	25	-	500	-	kΩ
AC CHARACTERISTICS A_V = +2, R_F = 560Ω, Unless Otherwise Specified							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})	A_V = +1, $+R_S$ = 560Ω	B	25	-	290	-	MHz
	A_V = +2	B	25	-	530	-	MHz
	A_V = -1, R_F = 510Ω	B	25	-	230	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1)	A_V = +1, $+R_S$ = 560Ω	B	25	-	150	-	MHz
	A_V = +2	B	25	-	130	-	MHz
	A_V = -1, R_F = 510Ω	B	25	-	120	-	MHz
Gain Flatness (A_V = +2, V_{OUT} = 0.2V_{P-P})	To 25MHz	B	25	-	±0.04	-	dB
	To 50MHz	B	25	-	±0.11	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
Crosstalk (Note 4)	5MHz	B	25	-	-73	-	dB
	10MHz	B	25	-	-64	-	dB
OUTPUT CHARACTERISTICS R_F = 560Ω, Unless Otherwise Specified							
Output Voltage Swing	A_V = -1, R_L = 100Ω	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current	A_V = -1, R_L = 50Ω	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
DC Closed Loop Output Impedance	A_V = +2, R_F = 560Ω	B	25	-	0.07	-	Ω
Second Harmonic Distortion (A_V = +2, R_F = 560Ω, V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Third Harmonic Distortion (A_V = +2, R_F = 560Ω, V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-55	-	dBc
	20MHz	B	25	-	-50	-	dBc
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 560Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P})	Rise Time	B	25	-	0.65	-	ns
	Fall Time	B	25	-	1.20	-	ns
Overshoot	V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 1.0ns	B	25	-	7	-	%

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, +R_S = 560Ω)	+SR	B	25	-	1050	-	V/µs
	-SR	B	25	-	800	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2)	+SR	B	25	-	1400	-	V/µs
	-SR	B	25	-	900	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = -1, R_F = 510Ω)	+SR	B	25	-	1950	-	V/µs
	-SR	B	25	-	1050	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step)	To 0.1%	B	25	-	15	-	ns
	To 0.05%	B	25	-	20	-	ns
	To 0.02%	B	25	-	30	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 560Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
DISABLE CHARACTERISTICS							
Disabled Supply Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	3	4	mA/Op Amp
$\overline{DISABLE}$ Input Logic Voltage	Low	A	Full	-	-	0.8	V
	High	A	25, 85	2.0	-	-	V
		A	-40°C	2.4	-	-	V
$\overline{DISABLE}$ Input Logic Low Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	100	200	µA
$\overline{DISABLE}$ Input Logic High Current	$V_{\overline{DISABLE}}$ = 5V	A	Full	-	1	15	µA
Output Disable Time	V_{IN} = ±1V, $V_{\overline{DISABLE}}$ = 2.4V to 0V	B	25	-	20	-	ns
Output Enable Time	V_{IN} = ±1V, $V_{\overline{DISABLE}}$ = 0V to 2.4V	B	25	-	160	-	ns
Disabled Output Capacitance	$V_{\overline{DISABLE}}$ = 0V	B	25	-	3.8	-	pF
Disabled Output Leakage	$V_{\overline{DISABLE}}$ = 0V, V_{IN} = +2V, V_{OUT} = ±3V	A	Full	-	2	10	µA
Off Isolation ($V_{DISABLE}$ = 0V, V_{IN} = 1V_{P-P}, A_V = +2)	At 5MHz	B	25	-	-61	-	dB
	At 10MHz	B	25	-	-55	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current		A	25	5.6	5.8	6.1	mA/Op Amp
		A	Full	5.4	5.9	6.3	mA/Op Amp

NOTES:

3. Test Level: A. Production Tested.; B. Typical or Guaranteed Limit Based on Characterization.; C. Design Typical for Information Only.
4. The typical use for these amplifiers is in multiplexed configurations, where one amplifier (hostile channel) is enabled, and the passive channel is disabled. The crosstalk data specified is tested in this manner, with the input signal applied to the hostile channel, while monitoring the output of the passive channel. Crosstalk performance with both the hostile and passive channels enabled is typically: -63dB at 5MHz, and -50dB at 10MHz.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1245 design is optimized for a 560Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better. Note that a series input resistor, on +IN, is required for a gain of +1, to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	510	230
+1	560 (+R_S = 560Ω)	290
+2	560	530

Non-inverting Input Source Impedance

For best operation, the DC source impedance looking out of the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Optional GND Pin for TTL Compatibility

The HFA1245 derives an internal GND reference for the digital circuitry as long as the power supplies are symmetrical about GND. The GND reference is used to ensure the TTL compatibility of the $\overline{\text{DISABLE}}$ inputs. With symmetrical supplies the GND pin (Pin 12) may be floated, or connected directly to GND. If asymmetrical supplies (e.g., +10V, 0V) are utilized, and TTL compatibility is desired, the GND pin must be connected to GND.

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 290MHz (for A_V = +1). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 62Ω, C_L = 40pF, the overall bandwidth is limited to 180MHz, and bandwidth drops to 70MHz at A_V = +1, R_S = 8Ω, C_L = 400pF.

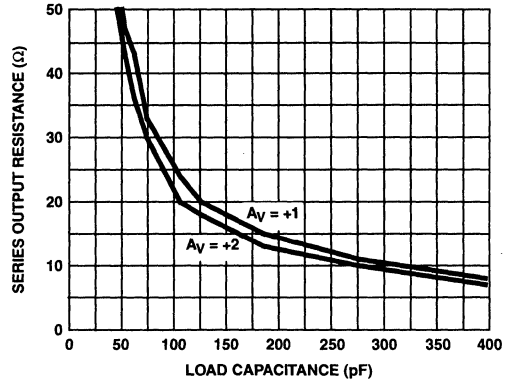


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Die Characteristics

DIE DIMENSIONS:

69 mils x 92 mils x 19 mils
1750µm x 2330µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

PASSIVATION:

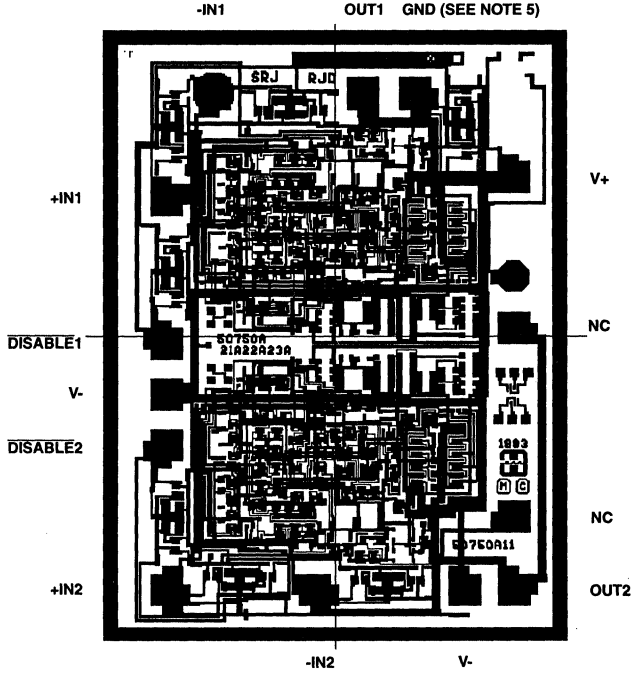
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

180

Metallization Mask Layout

HFA1245



NOTE:

5. This is an optional GND pad. Users may set a GND reference, via this pad, to ensure the TTL compatibility of the $\overline{\text{DISABLE}}$ inputs when using asymmetrical supplies (e.g., V+ = 10V, V- = 0V). See the "Application Information" section for details.

HARRIS SEMICONDUCTOR

HFA1405

Quad, 560MHz, Low Power, Video Operational Amplifier

November 1996

Features

- Low Supply Current . . . . . 5.8mA/Op Amp
- High Input Impedance 1MΩ
- Wide -3dB Bandwidth (A_V = +2) 560MHz
- Very Fast Slew Rate 1700V/μs
- Gain Flatness (to 50MHz) . . . . . ±0.03dB
- Differential Gain 0.02%
- Differential Phase . . . . . 0.03 Degrees
- All Hostile Crosstalk (5MHz) . . . . . -60dB
- Pin Compatible Upgrade to HA5025, CLC414, and CLC415

Applications

- Flash A/D Drivers
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- High Speed Oscilloscopes and Analyzers

Description

The HFA1405 is a quad, high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

These amplifiers deliver up to 560MHz bandwidth and 1700V/μs slew rate, on only 58mW of quiescent power. They are specifically designed to meet the performance, power, and cost requirements of high volume video applications. The excellent gain flatness and differential gain/phase performance make these amplifiers well suited for component or composite video applications. Video performance is maintained even when driving a back terminated cable (R_L = 150Ω), and degrades only slightly when driving two back terminated cables (R_L = 75Ω). RGB applications will benefit from the high slew rates, and high full power bandwidth.

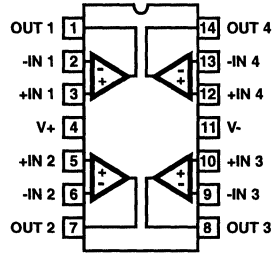
The HFA1405 is a pin compatible, low power, high performance upgrade for the popular Harris HA5025, and for the CLC414 and CLC415.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1405IB	-40 to 85	14 Ld SOIC	M14.15
HFA1405IP	-40 to 85	14 Ld PDIP	E14.3
HA5025EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HFA1405
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3604.4**

Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage. 5V
Output Current (Note 2) . . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	120
PDIP Package	100

Maximum Junction Temperature (Die) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (^oC)	HFA1405IB (SOIC)			HFA1405IP (PDIP)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS										
Input Offset Voltage		A	25	-	2	5	-	2	5	mV
		A	Full	-	3	8	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	45	48	-	45	48	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	43	46	-	43	46	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	43	46	-	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	48	52	-	48	52	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	46	48	-	46	48	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	46	48	-	46	48	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	-	6	15	µA
		A	Full	-	10	25	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	0.5	1	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	0.8	3	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	0.8	3	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.2	-	0.8	1.2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	0.8	-	0.5	0.8	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	0.8	-	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	-	2	7.5	µA
		A	Full	-	5	15	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	25	-	3	6	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	85	-	4	8	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40	-	4	8	-	4	8	µA/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (°C)	HFA1405IB (SOIC)			HFA1405IP (PDIP)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	2	5	-	2	5	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	4	8	-	4	8	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	4	8	-	4	8	µA/V
Inverting Input Resistance		C	25	-	60	-	-	60	-	Ω
Input Capacitance		B	25	-	1.4	-	-	2.2	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS Tests)		A	25, 85	±1.8	±2.4	-	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	3.5	-	-	3.5	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	2.5	-	-	2.5	-	$pA/\sqrt{Hz}$
Inverting Input Noise Current Density	f = 100kHz	B	25	-	20	-	-	20	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS										
Open Loop Transimpedance Gain	$A_V = -1$	C	25	-	500	-	-	500	-	kΩ
AC CHARACTERISTICS (Note 3)										
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, Notes 3, 5)	$A_V = -1$	B	25	-	420	-	-	360	-	MHz
	$A_V = +2$	B	25	-	560	-	-	400	-	MHz
	$A_V = +6$	B	25	-	140	-	-	100	-	MHz
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$, Notes 3, 5)	$A_V = -1$	B	25	-	260	-	-	260	-	MHz
	$A_V = +2$	B	25	-	165	-	-	165	-	MHz
	$A_V = +6$	B	25	-	140	-	-	100	-	MHz
Gain Flatness ($V_{OUT} = 0.2V_{P-P}$, Notes 3, 5)	$A_V = -1$, To 25MHz	B	25	-	±0.03	-	-	±0.04	-	dB
	$A_V = -1$, To 50MHz	B	25	-	±0.04	-	-	±0.04	-	dB
	$A_V = -1$, To 100MHz	B	25	-	-	-	-	±0.06	-	dB
	$A_V = +2$, To 25MHz	B	25	-	±0.03	-	-	±0.04	-	dB
	$A_V = +2$, To 50MHz	B	25	-	±0.03	-	-	±0.04	-	dB
	$A_V = +2$, To 100MHz	B	25	-	-	-	-	±0.06	-	dB
	$A_V = +6$, To 15MHz	B	25	-	±0.08	-	-	±0.08	-	dB
	$A_V = +6$, To 30MHz	B	25	-	±0.19	-	-	±0.27	-	dB
Minimum Stable Gain		A	Full	-	1	-	-	1	-	V/V
Crosstalk ($A_V = +2$, All Channels Hostile, Note 5)	5MHz	B	25	-	-60	-	-	-55	-	dB
	10MHz	B	25	-	-56	-	-	-52	-	dB
OUTPUT CHARACTERISTICS $A_V = +2$ (Note 3), Unless Otherwise Specified										
Output Voltage Swing (Note 5)	$A_V = -1$, $R_L = 100\Omega$	A	25	±3	±3.4	-	±3	±3.4	-	V
		A	Full	±2.8	±3	-	±2.8	±3	-	V
Output Current (Note 5)	$A_V = -1$, $R_L = 50\Omega$	A	25, 85	50	60	-	50	60	-	mA
		A	-40	28	42	-	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	-	90	-	mA
Closed Loop Output Impedance		B	25	-	0.2	-	-	0.2	-	Ω

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (°C)	HFA1405IB (SOIC)			HFA1405IP (PDIP)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Second Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 5)	10MHz	B	25	-	-51	-	-	-51	-	dBc
	20MHz	B	25	-	-46	-	-	-46	-	dBc
Third Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 5)	10MHz	B	25	-	-63	-	-	-63	-	dBc
	20MHz	B	25	-	-56	-	-	-56	-	dBc
TRANSIENT CHARACTERISTICS $A_V = +2$ (Note 3), Unless Otherwise Specified										
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$, Note 3)	$A_V = +2$	B	25	-	0.8	-	-	0.9	-	ns
	$A_V = +6$	B	25	-	2.9	-	-	4	-	ns
Overshoot ($V_{OUT} = 0.5V_{P-P}$, V_{IN} $t_{RISE} = 1ns$, Notes 3, 6)	$A_V = -1$, +OS	B	25	-	7	-	-	3	-	%
	$A_V = -1$, -OS	B	25	-	8	-	-	13	-	%
	$A_V = +2$, +OS	B	25	-	5	-	-	7	-	%
	$A_V = +2$, -OS	B	25	-	10	-	-	11	-	%
	$A_V = +6$, +OS	B	25	-	2	-	-	2	-	%
	$A_V = +6$, -OS	B	25	-	2	-	-	2	-	%
Slew Rate ($V_{OUT} = 5V_{P-P}$, Notes 3, 5)	$A_V = -1$, +SR	B	25	-	2500	-	-	2500	-	V/µs
	$A_V = -1$, -SR	B	25	-	1900	-	-	1900	-	V/µs
	$A_V = +2$, +SR	B	25	-	1700	-	-	1600	-	V/µs
	$A_V = +2$, -SR	B	25	-	1700	-	-	1400	-	V/µs
	$A_V = +6$, +SR	B	25	-	1500	-	-	1000	-	V/µs
	$A_V = +6$, -SR	B	25	-	1100	-	-	1000	-	V/µs
Settling Time (V_{OUT} = +2V to 0V Step, Note 5)	To 0.1%	B	25	-	23	-	-	23	-	ns
	To 0.05%	B	25	-	30	-	-	30	-	ns
	To 0.025%	B	25	-	37	-	-	40	-	ns
Overdrive Recovery Time	$V_{IN} = \pm2V$	B	25	-	8.5	-	-	8.5	-	ns
VIDEO CHARACTERISTICS $A_V = +2$ (Note 3), Unless Otherwise Specified										
Differential Gain (f = 3.58MHz)	$R_L = 150\Omega$	B	25	-	0.02	-	-	0.03	-	%
	$R_L = 75\Omega$	B	25	-	0.03	-	-	0.06	-	%
Differential Phase (f = 3.58MHz)	$R_L = 150\Omega$	B	25	-	0.03	-	-	0.03	-	Degrees
	$R_L = 75\Omega$	B	25	-	0.06	-	-	0.06	-	Degrees
POWER SUPPLY CHARACTERISTICS										
Power Supply Range		C	25	±4.5	-	±5.5	±4.5	-	±5.5	V
Power Supply Current (Note 5)		A	25	-	5.8	6.1	-	5.8	6.1	mA/Op Amp
		A	Full	-	5.9	6.3	-	5.9	6.3	mA/Op Amp

NOTES:

3. The optimum feedback resistor depends on closed loop gain and package type. The following resistors were used for the PDIP/SOIC characterization: $A_V = -1$, $R_F = 310\Omega/360\Omega$; $A_V = +2$, $R_F = 402\Omega/510\Omega$; $A_V = +6$, $R_F = 500\Omega/500\Omega$. See the Application Information section for more information.
4. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
5. See Typical Performance Curves for more information.
6. Undershoot dominates for output signal swings below GND (e.g., $2V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 2V condition. See the "Application Information" section for details.

Application Information

Performance Differences Between PDIP and SOIC

The amplifiers comprising the HFA1405 are high frequency current feedback amplifiers. As such, they are sensitive to feedback capacitance which destabilizes the op amp and causes overshoot and peaking. Unfortunately, the standard quad op amp pinout places the amplifier's output next to its inverting input, thus making the package capacitance an unavoidable parasitic feedback capacitor. The larger parasitic capacitance of the PDIP requires an inherently more stable amplifier, which yields a PDIP device with lower performance than the SOIC device - see Electrical Specification tables for details.

Because of these performance differences, designers should evaluate and breadboard with the same package style to be used in production.

Note that the "Typical Performance Curves" section has separate pulse and frequency response graphs for each package type. Graphs not labeled with a specific package type are applicable to both packages.

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1405 design is optimized for $R_F = 402\Omega/510\Omega$ (PDIP/SOIC) at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). However, at higher gains the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better.

OPTIMUM FEEDBACK RESISTOR

GAIN (A_{CL})	R_F (Ω) PDIP/SOIC	BANDWIDTH (MHz) PDIP/SOIC
-1	310/360	360/420
+2	402/510	400/560
+6	500/500 (Note)	100/140

NOTE: $R_F = 500\Omega$ is not the optimum value. It was chosen to match the R_F of the CLC414 and CLC415, for performance comparison purposes. Performance at $A_V = +6$ may be increased by reducing R_F below 500Ω.

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥ 50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Pulse Undershoot

The HFA1405 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (see Figure 6 and Figure 9). This undershoot isn't present for small bipolar signals, or large positive signals (see Figure 5 and Figure 8).

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and eventual instability. To reduce this capacitance the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 560MHz. By decreasing R_S as C_L increases (as illustrated in the curve), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases.

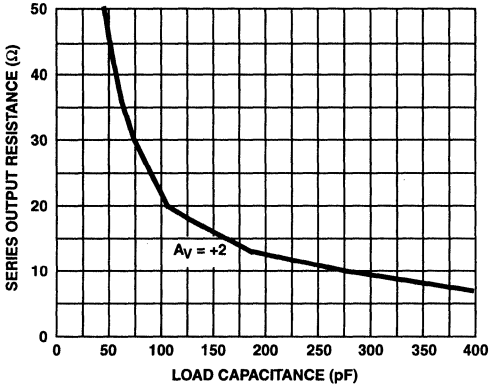


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1405 (PDIP) may be evaluated using the HA5025 Evaluation Board.

The schematic for amplifier 1 and the board layout are shown in Figure 2 and Figure 3. Resistors R_F and R_G may require a change to values applicable to the HFA1405.

To order evaluation boards (part number HA5025EVAL), please contact your local sales office.

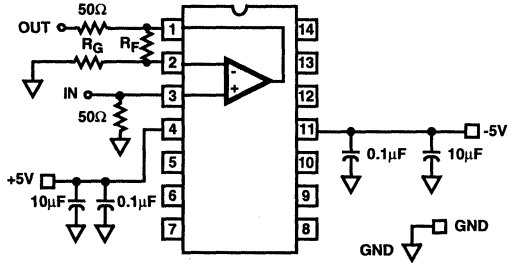
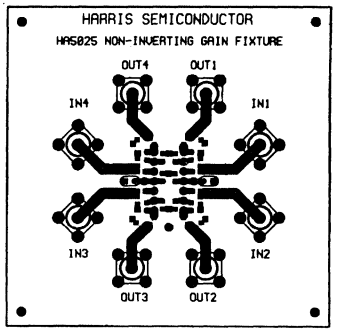


FIGURE 2. EVALUATION BOARD SCHEMATIC

TOP LAYOUT



BOTTOM LAYOUT

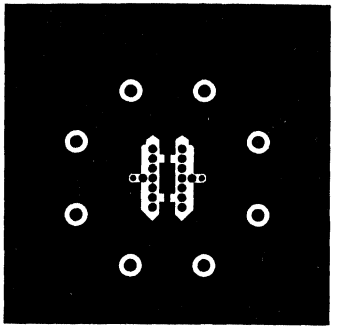


FIGURE 3. EVALUATION BOARD LAYOUT

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified

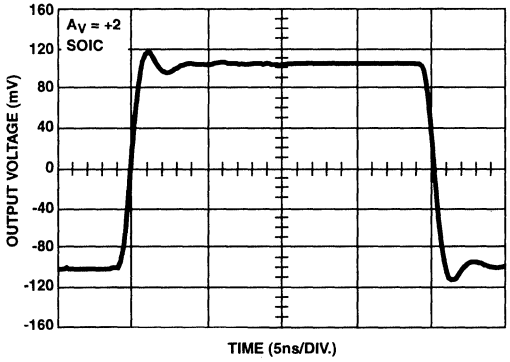


FIGURE 4. SMALL SIGNAL PULSE RESPONSE

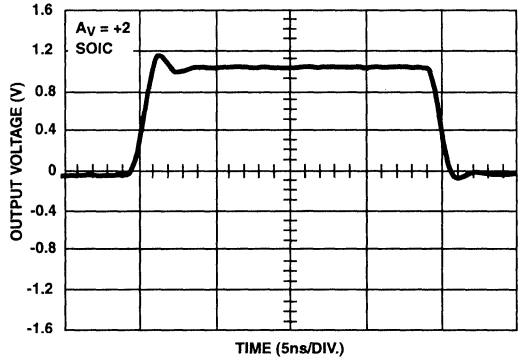


FIGURE 5. LARGE SIGNAL PULSE RESPONSE

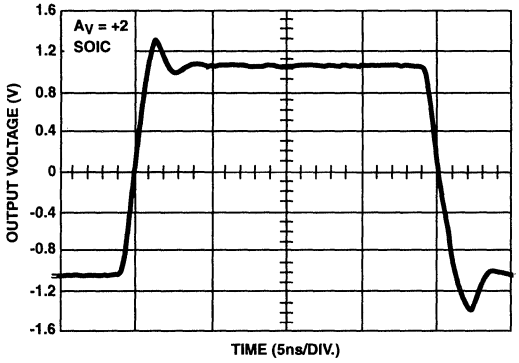


FIGURE 6. LARGE SIGNAL PULSE RESPONSE

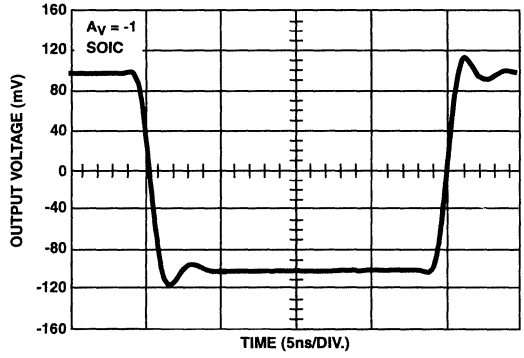


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

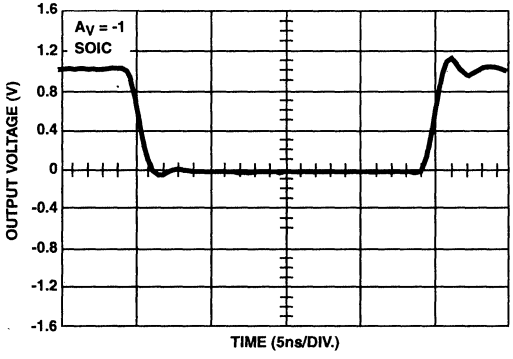


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

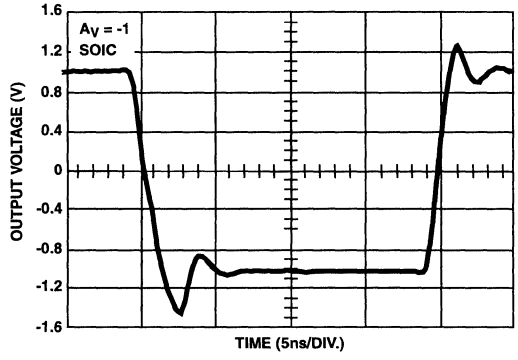


FIGURE 9. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

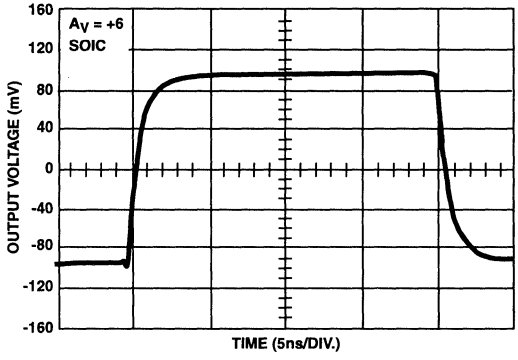


FIGURE 10. SMALL SIGNAL PULSE RESPONSE

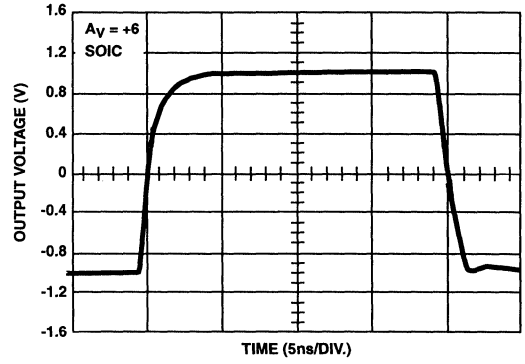


FIGURE 11. LARGE SIGNAL PULSE RESPONSE

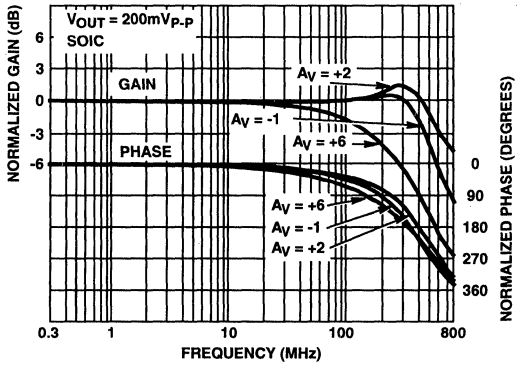


FIGURE 12. FREQUENCY RESPONSE

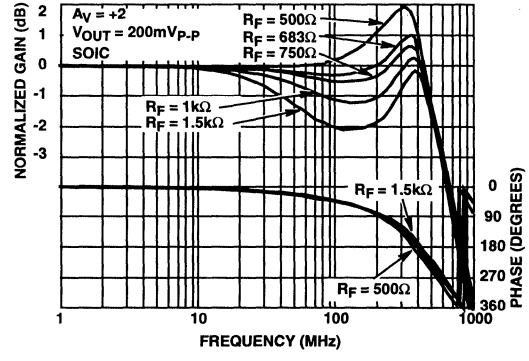


FIGURE 13. FREQUENCY RESPONSE vs FEEDBACK RESISTOR

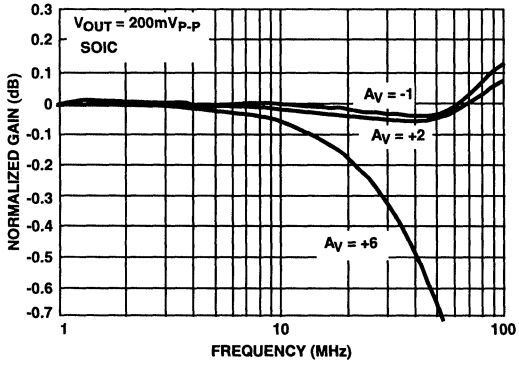


FIGURE 14. GAIN FLATNESS

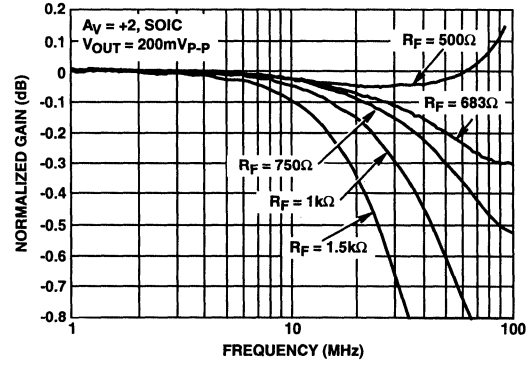


FIGURE 15. GAIN FLATNESS vs FEEDBACK RESISTOR

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

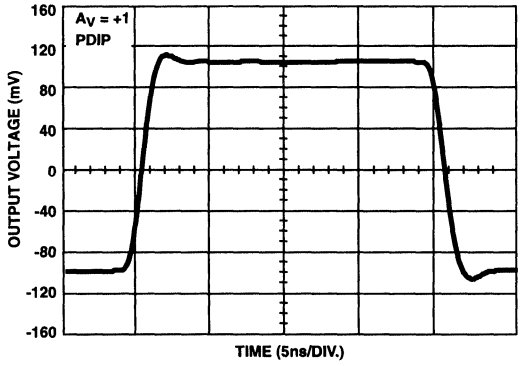


FIGURE 16. SMALL SIGNAL PULSE RESPONSE

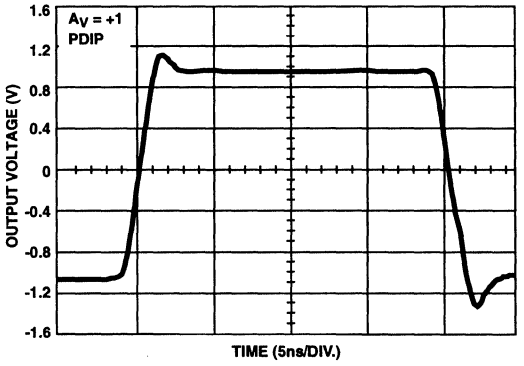


FIGURE 17. LARGE SIGNAL PULSE RESPONSE

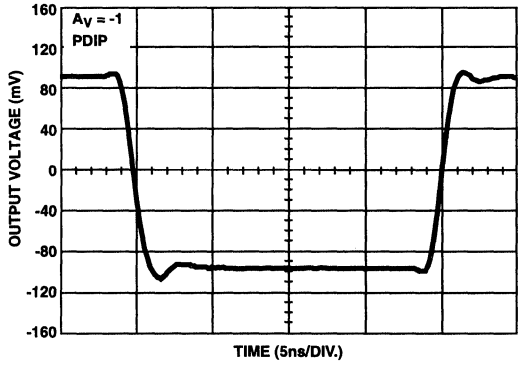


FIGURE 18. SMALL SIGNAL PULSE RESPONSE

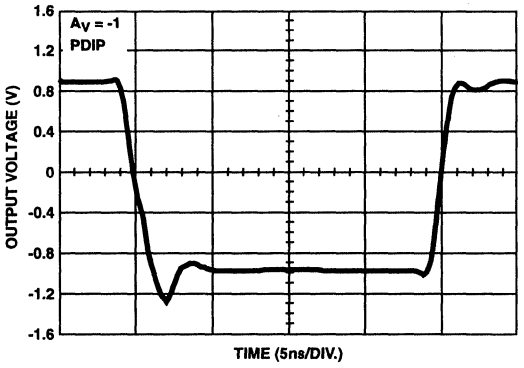


FIGURE 19. LARGE SIGNAL PULSE RESPONSE

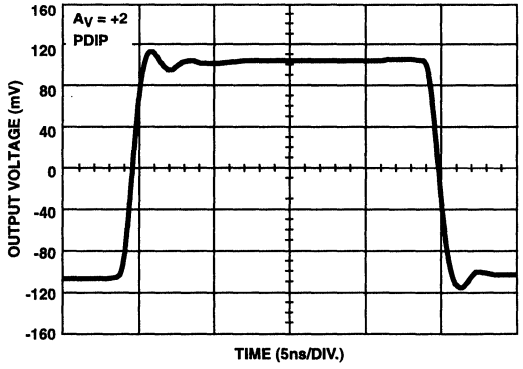


FIGURE 20. SMALL SIGNAL PULSE RESPONSE

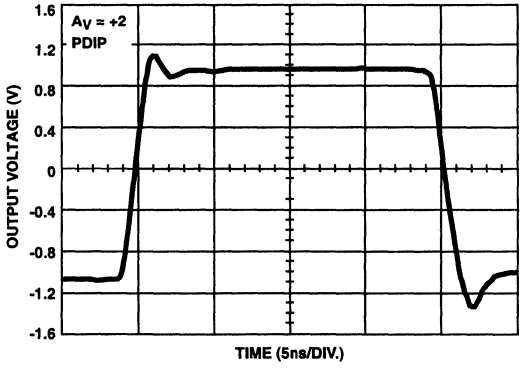


FIGURE 21. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

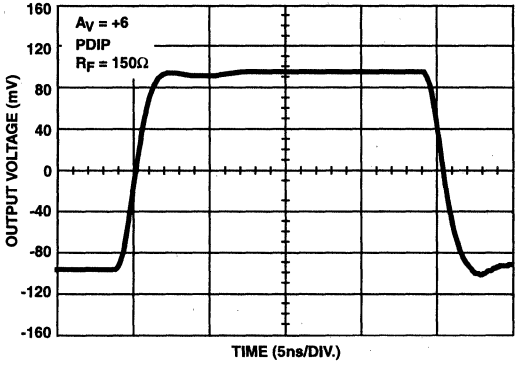


FIGURE 22. SMALL SIGNAL PULSE RESPONSE

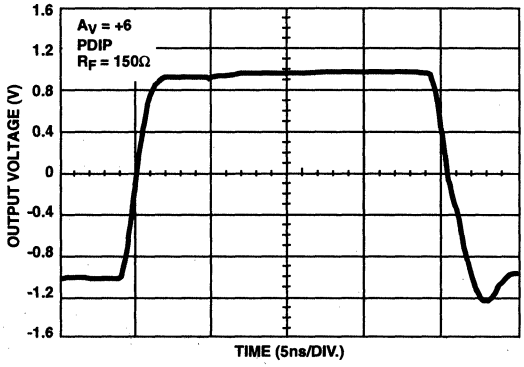


FIGURE 23. LARGE SIGNAL PULSE RESPONSE

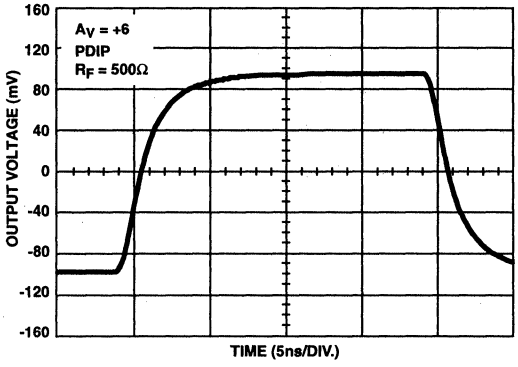


FIGURE 24. SMALL SIGNAL PULSE RESPONSE

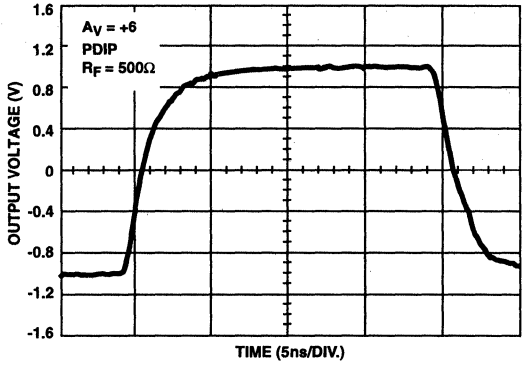


FIGURE 25. LARGE SIGNAL PULSE RESPONSE

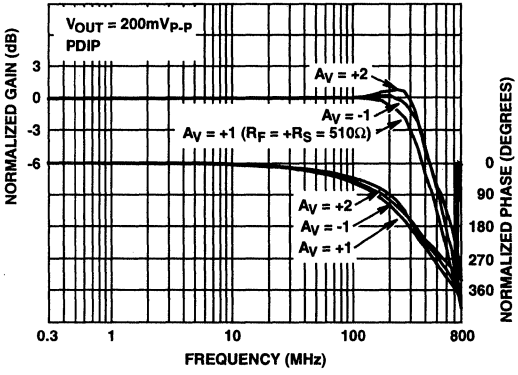


FIGURE 26. FREQUENCY RESPONSE

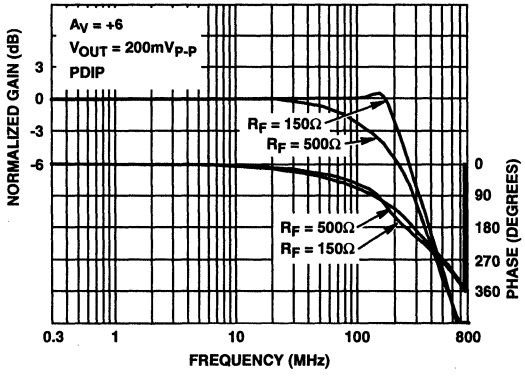


FIGURE 27. FREQUENCY RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

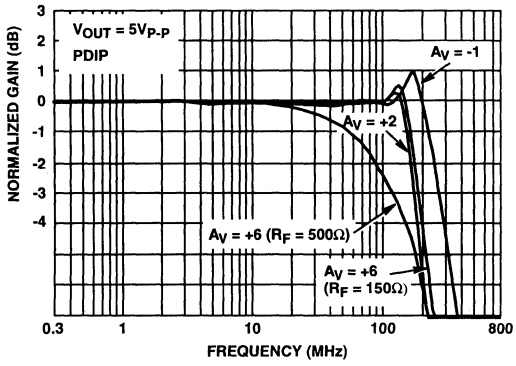


FIGURE 28. FULL POWER BANDWIDTH

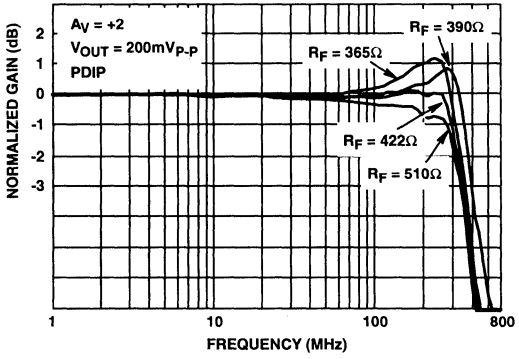


FIGURE 29. FREQUENCY RESPONSE vs FEEDBACK RESISTOR

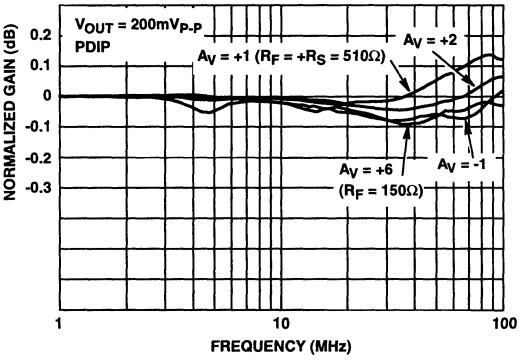


FIGURE 30. GAIN FLATNESS

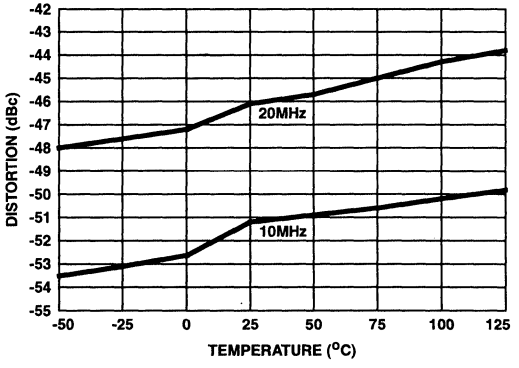


FIGURE 31. 2nd HARMONIC DISTORTION vs TEMPERATURE

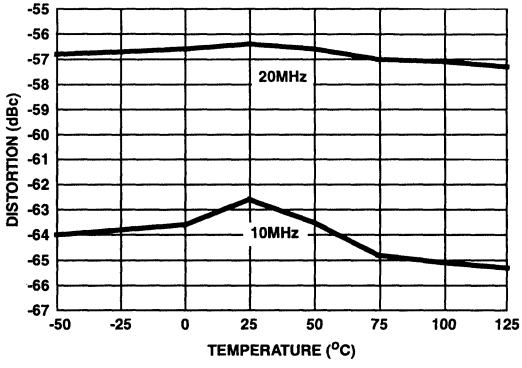


FIGURE 32. 3rd HARMONIC DISTORTION vs TEMPERATURE

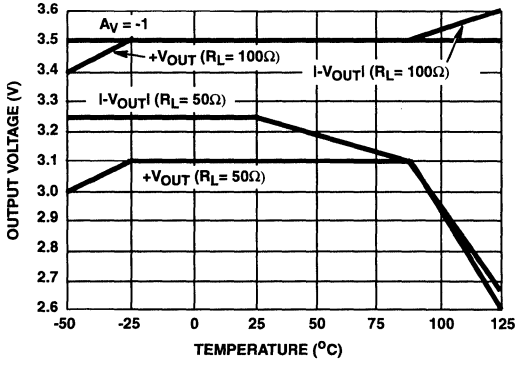


FIGURE 33. OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

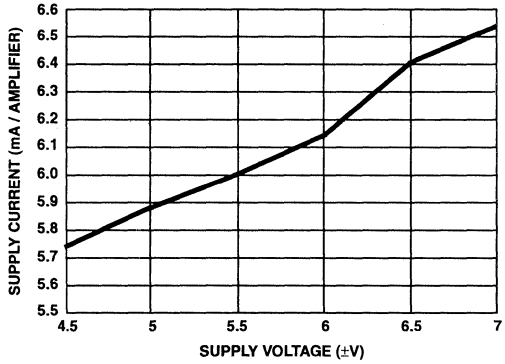


FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

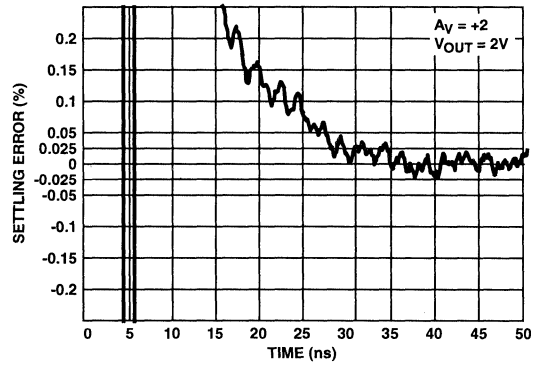


FIGURE 35. SETTLING RESPONSE

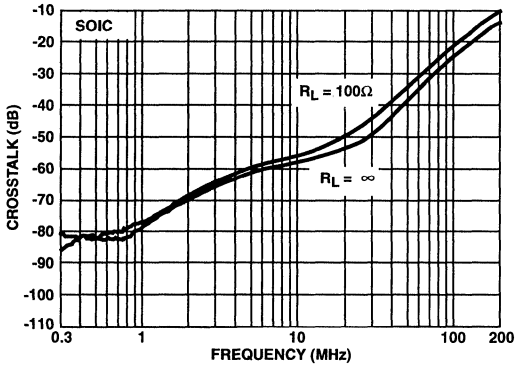


FIGURE 36. ALL HOSTILE CROSSTALK

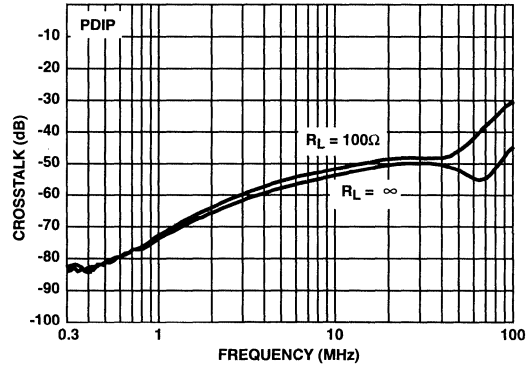


FIGURE 37. ALL HOSTILE CROSSTALK

Die Characteristics

DIE DIMENSIONS:

79 mils x 118 mils x 19 mils
2000µm x 3000µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

PASSIVATION:

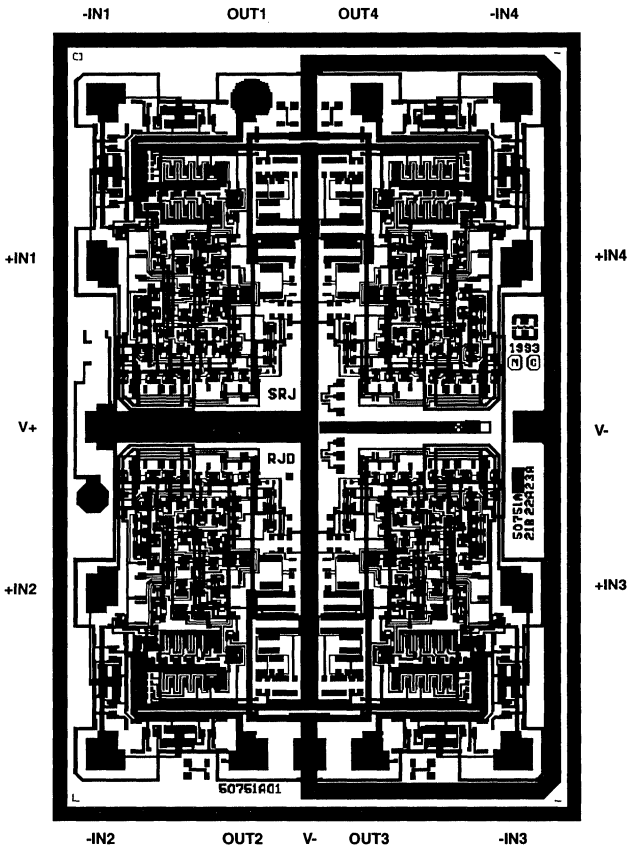
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

320

Metallization Mask Layout

HFA1405



HARRIS SEMICONDUCTOR

HFA1412

Quad, 350MHz, Low Power, Programmable Gain Buffer Amplifier

November 1996

Features

- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Wide -3dB Bandwidth 350MHz
- Low Supply Current..... 6mA/Buffer
- Excellent Gain Flatness (to 100MHz)..... ±0.08dB
- Low Differential Gain and Phase .. 0.03%/0.02 Degree
- Very Fast Slew Rate 1650V/µs
- Fast Settling Time (0.1%) 28ns
- High Output Current 55mA
- Excellent Gain Accuracy..... 0.99V/V
- Overdrive Recovery..... <10ns
- Standard Operational Amplifier Pinout

Applications

- Video Distribution Amps
- Flash A/D Drivers
- Video Cable Drivers
- Video Switchers and Routers
- Medical Imaging Systems
- RGB Video Processing
- High Speed Oscilloscopes and Analyzers

Description

The HFA1412 is a quad closed loop Buffer featuring user programmable gain and high speed video performance.

A unique feature of the HFA1412's pinout allows the user to select a voltage gain of +1, -1, or +2 (see the "Application Information" section). The on-chip gain setting resistors eliminate eight external resistors, thus saving board space or freeing up space for termination resistors. The on-chip feedback resistor is preset at the optimum value, and also eliminates worries about parasitic feedback capacitance. Additionally, the capacitance sensitive summing node is buried inside the package where it is unaffected by PCB parasitics. Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

The HFA1412 is an excellent choice for component and composite video systems as indicated by the excellent gain flatness, and 0.03%/0.02 Degree Differential Gain/Phase specifications (R_L = 150Ω). Its ability to deliver a gain of +2 with no external resistors makes it particularly desirable for applications driving double terminated cables.

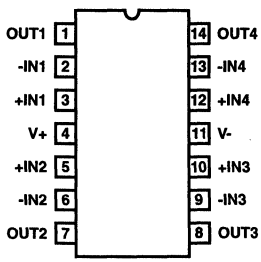
For Military product, refer to the HFA1412/883 data sheet.

Ordering Information

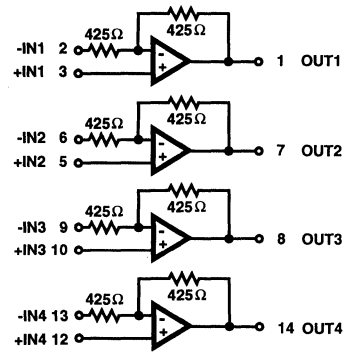
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1412IP	-40 to 85	14 Ld PDIP	E14.3
HFA1412IB	-40 to 85	14 Ld SOIC	M14.15
HA5025EVAL	DIP Evaluation Board For Quad Op Amp		

Pinout

HFA1412
(PDIP, SOIC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **4152.1**

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage ..... V_{SUPPLY}
Output Current (Note 1) ..... Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) ... 600V

Operating Conditions

Temperature Range ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 100
SOIC Package 120
Maximum Junction Temperature (Die) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Output Offset Voltage		A	25	-	2	10	mV
		A	Full	-	3	15	mV
Average Output Offset Voltage Drift		B	Full	-	22	70	µV/°C
Channel-to-Channel Output Offset Voltage Mismatch		A	25	-	-	15	mV
		A	Full	-	-	30	mV
Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	42	45	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	40	44	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	40	45	-	dB
Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	45	49	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	43	48	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	43	48	-	dB
Non-Inverting Input Bias Current		A	25	-	1	15	µA
		A	Full	-	3	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	30	80	nA/°C
Channel-to-Channel Non-Inverting Input Bias Current Mismatch		A	25	-	-	15	µA
		A	Full	-	-	25	µA
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.25V$	A	25	-	0.5	1	µA/V
		A	Full	-	-	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.1	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	1.4	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	1.3	-	MΩ
Inverting Input Resistance		C	25	-	425	-	Ω
Input Capacitance (either input)		C	25	-	2	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR and $+R_{IN}$ tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 4)	f = 100kHz	B	25	-	7	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density (Note 4)	f = 100kHz	B	25	-	3	-	$pA/\sqrt{Hz}$

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS							
Gain (V_{IN} = -1V to +1V)	A_V = -1	A	25	-0.98	-0.996	-1.02	V/V
		A	Full	-0.975	-1.000	-1.025	V/V
	A_V = +1	A	25	0.98	0.992	1.02	V/V
		A	Full	0.975	0.993	1.025	V/V
	A_V = +2	A	25	1.96	1.988	2.04	V/V
		A	Full	1.95	1.990	2.05	V/V
Channel-to-Channel Gain Mismatch	A_V = -1	A	25	-	-	±0.02	V/V
		A	Full	-	-	±0.025	V/V
	A_V = +1	A	25	-	-	±0.025	V/V
		A	Full	-	-	±0.025	V/V
	A_V = +2	A	25	-	-	±0.04	V/V
		A	Full	-	-	±0.05	V/V
AC CHARACTERISTICS							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 4)	A_V = -1	B	25	200	320	-	MHz
		B	Full	190	280	-	MHz
	A_V = +1, $+R_S$ = 620Ω	B	25	160	230	-	MHz
		B	Full	150	210	-	MHz
	A_V = +2	B	25	220	350	-	MHz
		B	Full	190	300	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2 or -1, V_{OUT} = 4V_{P-P} at A_V = +1, Note 4)	A_V = -1	B	25	-	225	-	MHz
	A_V = +1, $+R_S$ = 620Ω	B	25	-	190	-	MHz
	A_V = +2	B	25	-	160	-	MHz
Gain Flatness (V_{OUT} = 0.2V_{P-P}, Note 4)	A_V = +1, to 25MHz, $+R_S$ = 620Ω	B	25	-	±0.10	±0.18	dB
		B	Full	-	±0.12	±0.20	dB
	A_V = -1, to 50MHz	B	25	-	±0.06	±0.10	dB
		B	Full	-	±0.08	±0.16	dB
	A_V = -1, to 100MHz	B	25	-	±0.08	±0.20	dB
		B	Full	-	±0.13	±0.30	dB
	A_V = +2, to 50MHz	B	25	-	±0.05	±0.09	dB
		B	Full	-	±0.06	±0.10	dB
	A_V = +2, to 100MHz	B	25	-	±0.08	±0.16	dB
		B	Full	-	±0.16	±0.30	dB
Crosstalk (All Channels Hostile, Note 4)	5MHz	B	25	-	-53	-	dB
	10MHz	B	25	-	-50	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing (Note 4)	A_V = -1	A	25	±3.0	±3.2	-	V
		A	Full	±2.8	±3.0	-	V
Output Current (Note 4)	A_V = -1, R_L = 50Ω	A	25, 85	50	55	-	mA
		A	-40	28	42	-	mA

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
Output Short Circuit Current		B	25	-	100	-	mA
DC Closed Loop Output Impedance	A_V = +2	B	25	-	0.2	-	Ω
Second Harmonic Distortion (A_V = +2, V_{OUT} = $2V_{P-P}$, Note 4)	10MHz	B	25	-47	-50	-	dBc
		B	Full	-45	-48	-	dBc
	20MHz	B	25	-40	-43	-	dBc
		B	Full	-39	-41	-	dBc
Third Harmonic Distortion (A_V = +2, V_{OUT} = $2V_{P-P}$, Note 4)	10MHz	B	25	-55	-60	-	dBc
		B	Full	-55	-60	-	dBc
	20MHz	B	25	-46	-53	-	dBc
		B	Full	-46	-50	-	dBc
Reverse Isolation (S_{12}, Note 4)	30MHz, A_V = +2	B	25	-	-65	-	dB
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = $0.5V_{P-P}$)	Rise Time	B	25	-	1.0	-	ns
	Fall Time	B	25	-	1.25	-	ns
Overshoot (V_{OUT} = $0.5V_{P-P}$, V_{IN} t_{RISE} = 500ps, Notes 4, 5)	+OS	B	25	-	3	-	%
	-OS	B	25	-	9	-	%
Slew Rate (V_{OUT} = $5V_{P-P}$ at A_V = +2 or -1, V_{OUT} = $4V_{P-P}$ at A_V = +1)	A_V = -1	B	25	1150	1700	-	V/µs
		B	Full	1100	1650	-	V/µs
	A_V = +1, $+R_S$ = 620Ω	B	25	700	1000	-	V/µs
		B	Full	650	950	-	V/µs
	A_V = +2	B	25	900	1250	-	V/µs
		B	Full	800	1150	-	V/µs
Settling Time (V_{OUT} = +2V to 0V Step, Note 4)	To 0.1%	B	25	-	28	-	ns
	To 0.05%	B	25	-	33	-	ns
	To 0.02%	B	25	-	38	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (f = 3.58MHz, A_V = +2)	R_L = 150Ω	B	25	-	0.03	-	%
	R_L = 75Ω	B	25	-	0.05	-	%
Differential Phase (f = 3.58MHz, A_V = +2)	R_L = 150Ω	B	25	-	0.02	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current (Note 4)		A	25	-	5.9	6.1	mA/Op Amp
		A	Full	-	6.1	6.3	mA/Op Amp

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. See Typical Performance Curves for more information.
5. Negative overshoot dominates for output signal swings below GND (e.g. $0.5V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 0.5V condition. See the "Application Information" section for details.

Application Information

HFA1412 Advantages

The HFA1412 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space. Implementing a quad, gain of 2, cable driver with this IC eliminates the eight gain setting resistors, which frees up board space for termination resistors.

Like most newer high performance amplifiers, the HFA1412 is a current feedback amplifier (CFA). CFAs offer high bandwidth and slew rate at low supply currents, but can be difficult to use because of their sensitivity to feedback capacitance and parasitics on the inverting input (summing node). The HFA1412 eliminates these concerns by bringing the gain setting resistors on-chip. This yields the optimum placement and value of the feedback resistor, while minimizing feedback and summing node parasitics. Because there is no access to the summing node, the PCB parasitics do not impact performance at gains of +2 or -1 (see "Unity Gain Considerations" for discussion of parasitic impact on unity gain performance).

The HFA1412's closed loop gain implementation provides better gain accuracy, lower offset and output impedance, and better distortion compared with open loop buffers.

Closed Loop Gain Selection

This "buffer" operates in closed loop gains of -1, +1, or +2, with gain selection accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1 (see next section for layout caveats), while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded through a 50Ω resistor.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT	-INPUT
-1	50Ω to GND	Input
+1	Input	NC (Floating)
+2	Input	GND

Unity Gain Considerations

Unity gain selection is accomplished by floating the -Input of the HFA1412. Anything that tends to short the -Input to GND, such as stray capacitance at high frequencies, will cause the amplifier gain to increase toward a gain of +2. The result is excessive high frequency peaking, and possible instability. Even the minimal amount of capacitance associated with attaching the -Input lead to the PCB results in approximately 6dB of gain peaking. At a minimum this requires due care to ensure the minimum capacitance at the -Input connection.

Table 1 lists five alternate methods for configuring the HFA1412 as a unity gain buffer, and the corresponding performance. The implementations vary in complexity and involve performance trade-offs. The easiest approach to implement is simply shorting the two input pins together, and applying the input signal to this common node. The amplifier bandwidth decreases from 550MHz to 370MHz, but excellent gain flatness is the benefit. A drawback to this approach is that the amplifier input noise voltage and input offset voltage terms see a gain of +2, resulting in higher noise and output offset voltages. Alternately, a 100pF capacitor between the inputs shorts them only at high frequencies, which prevents the increased output offset voltage but delivers less gain flatness.

Another straightforward approach is to add a 620Ω resistor in series with the amplifier's positive input. This resistor and the HFA1412 input capacitance form a low pass filter which rolls off the signal bandwidth before gain peaking occurs. This configuration was employed to obtain the data sheet AC and transient parameters for a gain of +1.

Pulse Overshoot

The HFA1412 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased overshoot on the negative portion of the output waveform (see Figure 5, Figure 7, and Figure 9). This overshoot isn't present for small bipolar signals (see Figure 4, Figure 6, and Figure 8) or large positive signals. Figure 28 through Figure 31 illustrate the amplifier's overshoot dependency on input transition time, and signal polarity.

TABLE 1. UNITY GAIN PERFORMANCE FOR VARIOUS IMPLEMENTATIONS

APPROACH	PEAKING (dB)	BW (MHz)	SR (V/μs)	±0.1dB GAIN FLATNESS (MHz)
Remove -IN Pin	5.0	550	1300	18
$+R_S$ = 620Ω	1.0	230	1000	25
$+R_S$ = 620Ω and Remove -IN Pin	0.7	225	1000	28
Short +IN to -IN (e.g., Pins 2 and 3)	0.1	370	500	170
100pF Capacitor Between +IN and -IN	0.3	380	550	130

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board (PCB). **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 350MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth decreases as the load capacitance increases. For example, at $A_V = +2$, $R_S = 22\Omega$, $C_L = 100pF$, the overall bandwidth is 125MHz, and bandwidth drops to 100MHz at $R_S = 12\Omega$, $C_L = 220pF$.

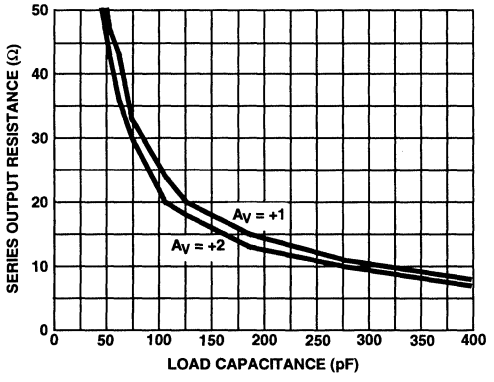


FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1412 may be evaluated using the HA5025 Evaluation Board, slightly modified as follows:

1. Remove the four feedback resistors, and leave the connections open.
2. a. For $A_V = +1$ evaluation, remove the gain setting resistors (R_1), and leave pins 2, 6, 9, and 13 floating.
   b. For $A_V = +2$, replace the gain setting resistors (R_1) with 0Ω resistors to GND.

The modified schematic for amplifier 1, and the board layout are shown in Figures 2 and 3.

To order evaluation boards (part number HA5025EVAL), please contact your local sales office.

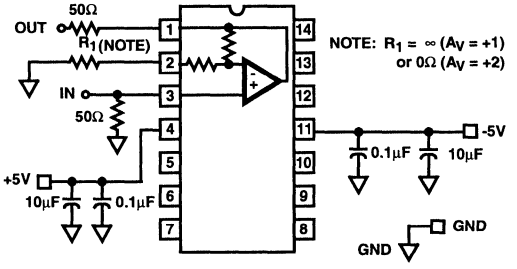


FIGURE 2. MODIFIED EVALUATION BOARD SCHEMATIC

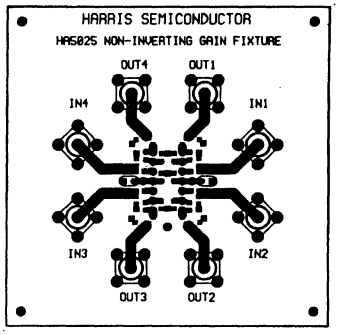


FIGURE 3A. TOP LAYOUT

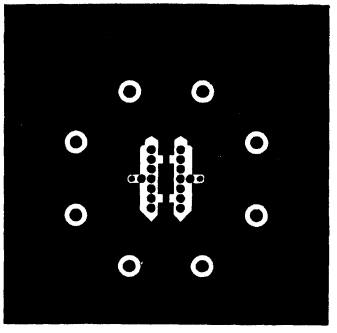


FIGURE 3B. BOTTOM LAYOUT

FIGURE 3. EVALUATION BOARD LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

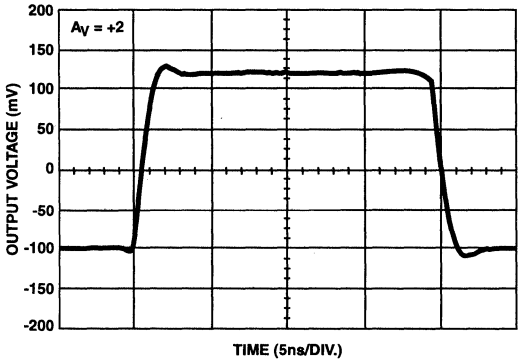


FIGURE 4. SMALL SIGNAL PULSE RESPONSE

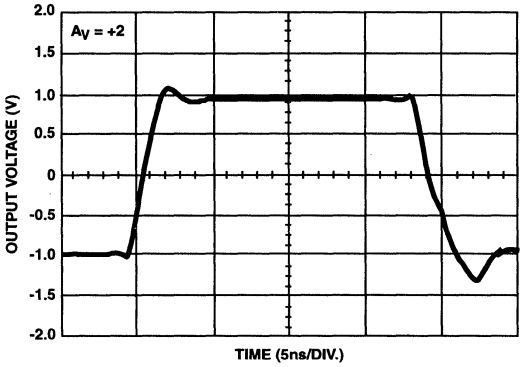


FIGURE 5. LARGE SIGNAL PULSE RESPONSE

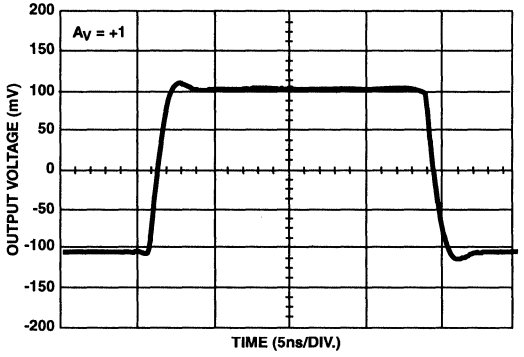


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

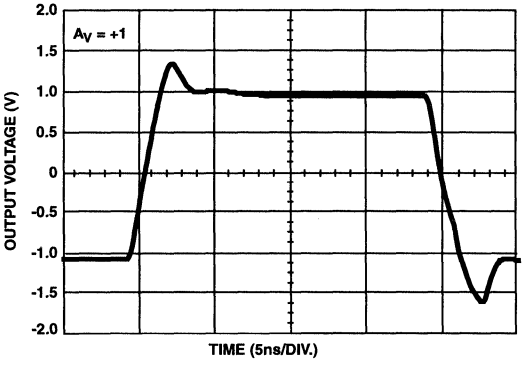


FIGURE 7. LARGE SIGNAL PULSE RESPONSE

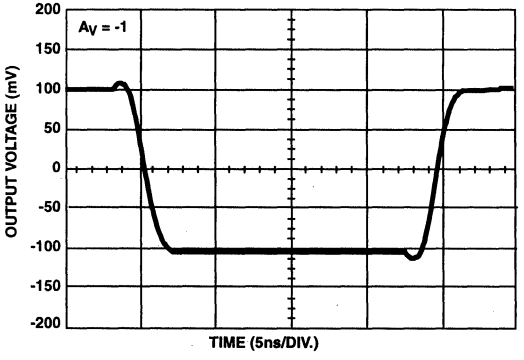


FIGURE 8. SMALL SIGNAL PULSE RESPONSE

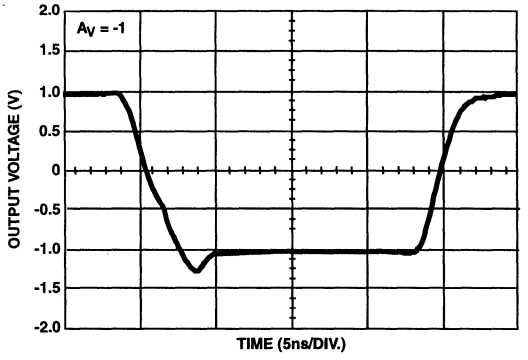


FIGURE 9. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

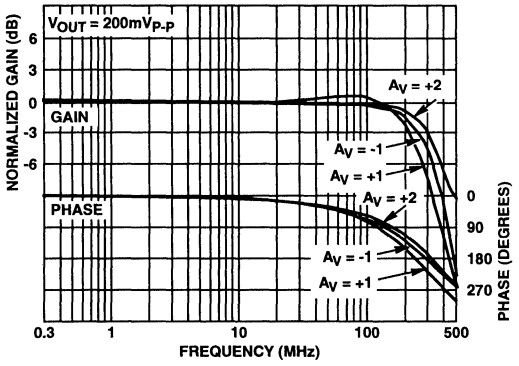


FIGURE 10. FREQUENCY RESPONSE

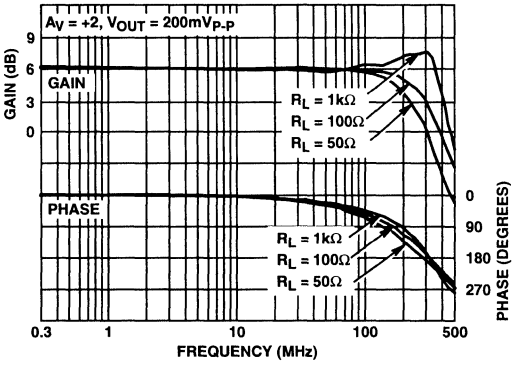


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

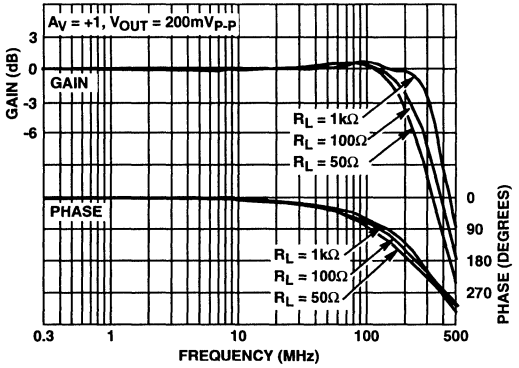


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

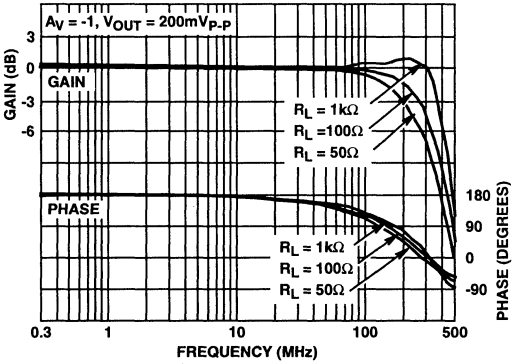


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

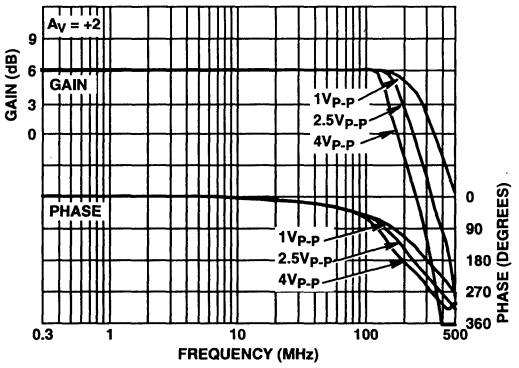


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

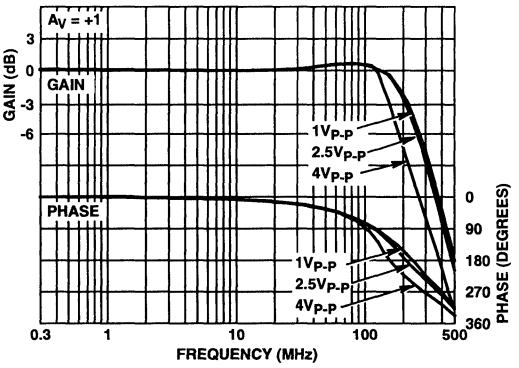


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

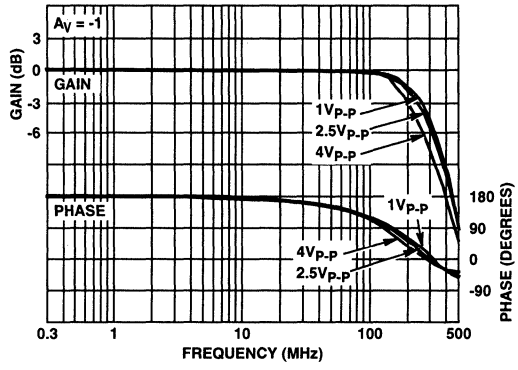


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

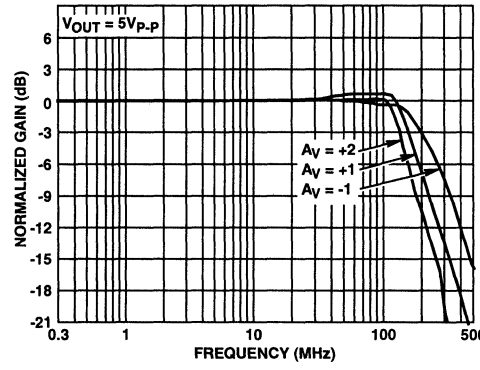


FIGURE 17. FULL POWER BANDWIDTH

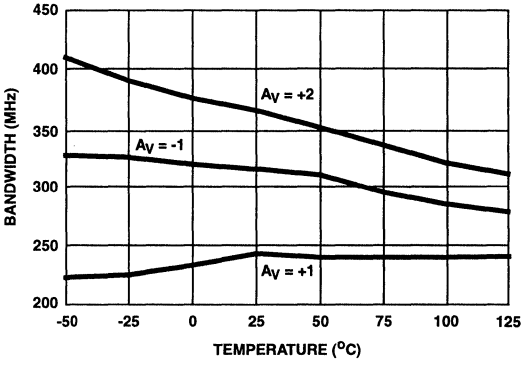


FIGURE 18. -3dB BANDWIDTH vs TEMPERATURE

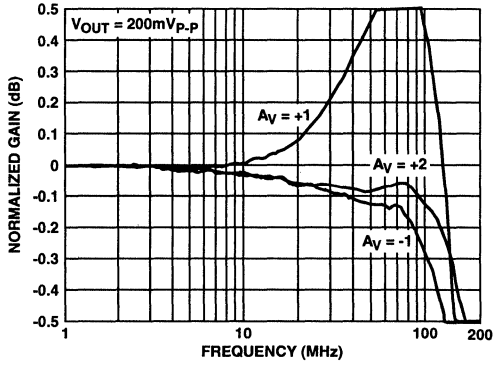


FIGURE 19. GAIN FLATNESS

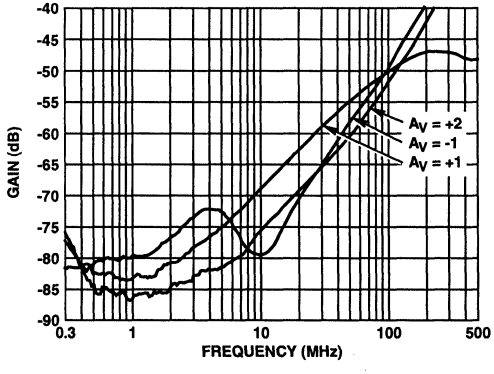


FIGURE 20. REVERSE ISOLATION (S_{12})

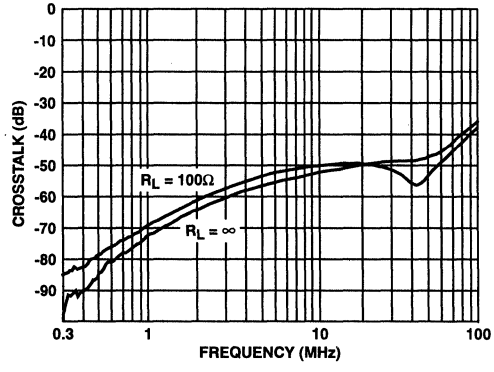


FIGURE 21. ALL HOSTILE CROSSTALK

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

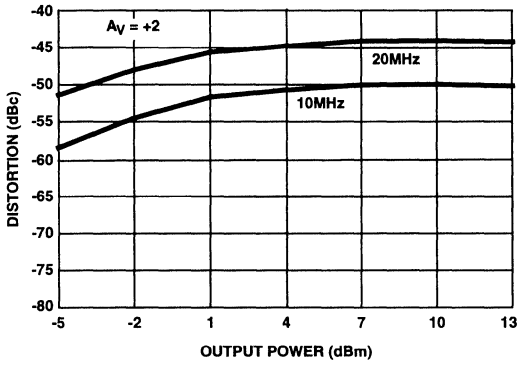


FIGURE 22. 2nd HARMONIC DISTORTION vs P_{OUT}

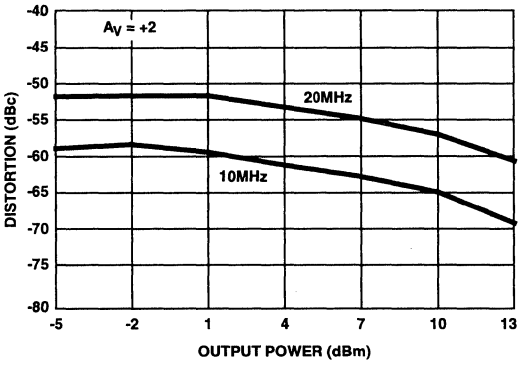


FIGURE 23. 3rd HARMONIC DISTORTION vs P_{OUT}

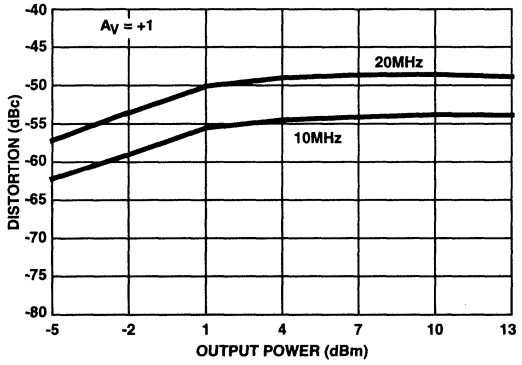


FIGURE 24. 2nd HARMONIC DISTORTION vs P_{OUT}

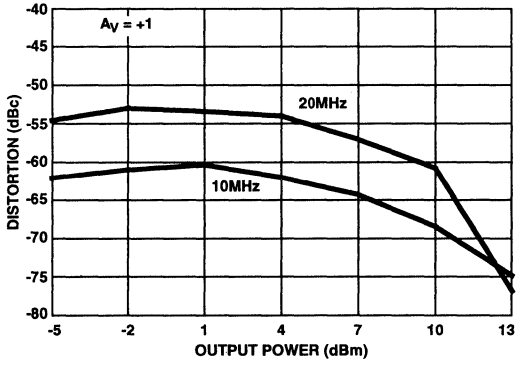


FIGURE 25. 3rd HARMONIC DISTORTION vs P_{OUT}

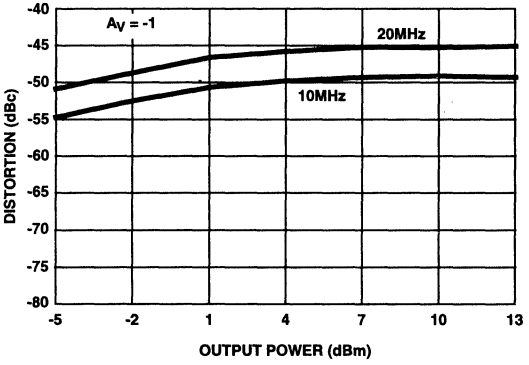


FIGURE 26. 2nd HARMONIC DISTORTION vs P_{OUT}

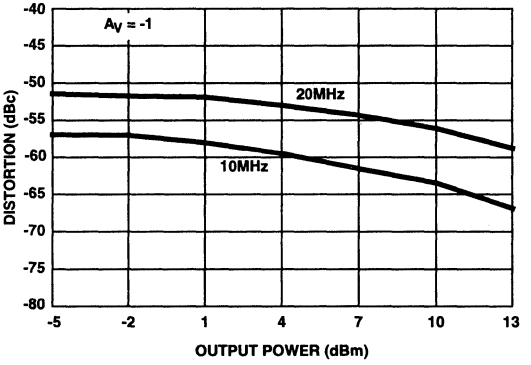


FIGURE 27. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

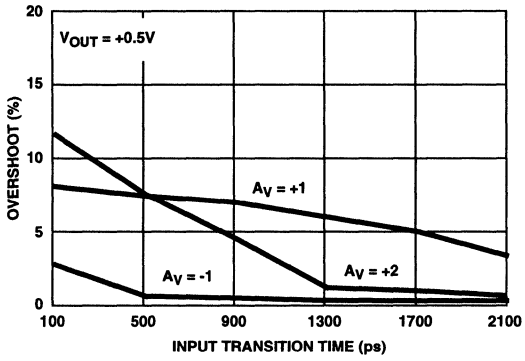


FIGURE 28. OVERSHOOT vs TRANSITION TIME

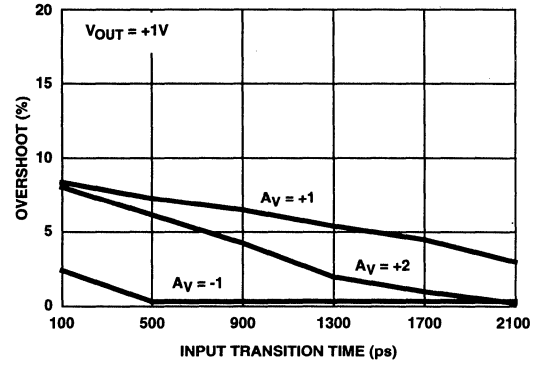


FIGURE 29. OVERSHOOT vs TRANSITION TIME

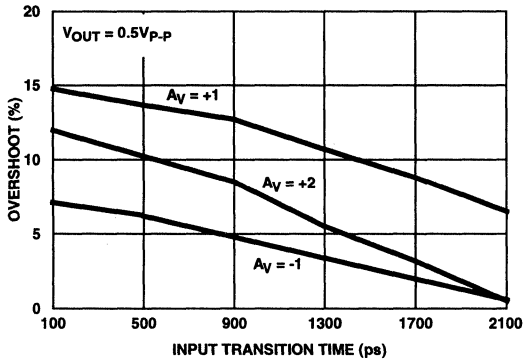


FIGURE 30. OVERSHOOT vs TRANSITION TIME

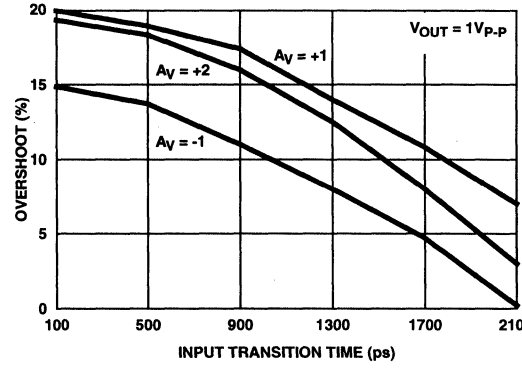


FIGURE 31. OVERSHOOT vs TRANSITION TIME

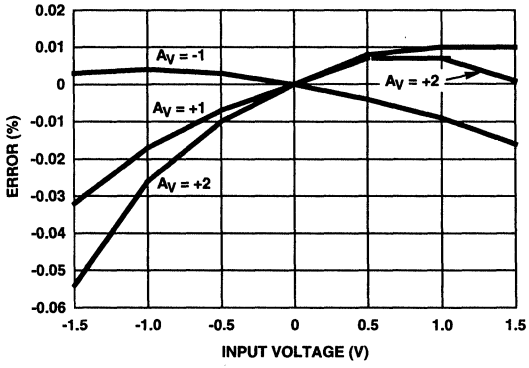


FIGURE 32. INTEGRAL LINEARITY ERROR

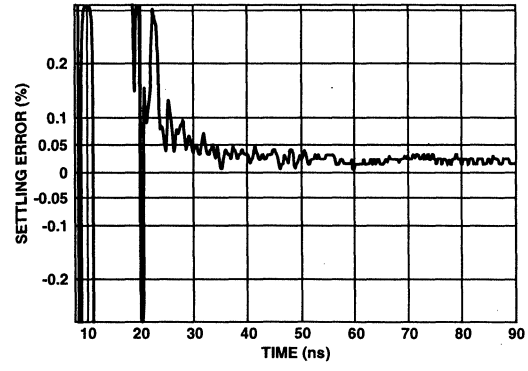


FIGURE 33. SETTLING RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

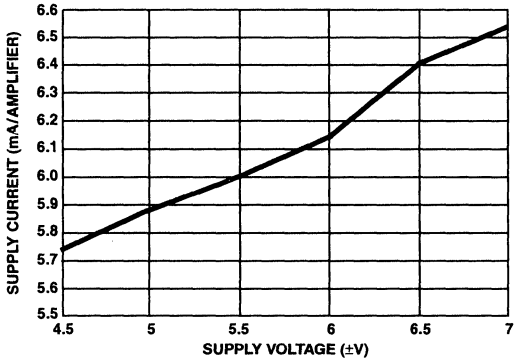


FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

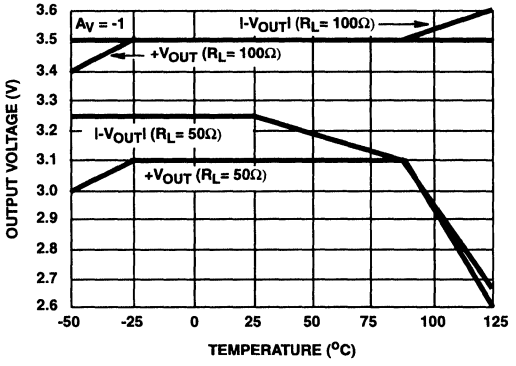


FIGURE 35. OUTPUT VOLTAGE vs TEMPERATURE

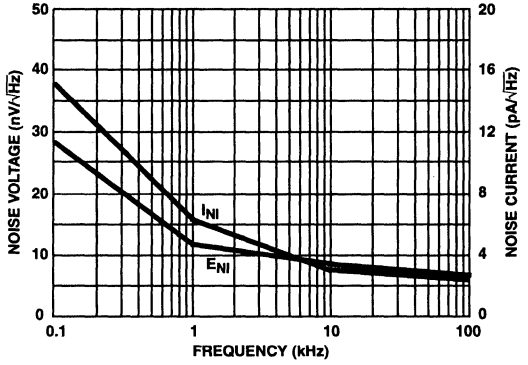


FIGURE 36. INPUT NOISE CHARACTERISTICS

Die Characteristics

DIE DIMENSIONS:

79 mils x 118 mils x 19 mils
2000µm x 3000µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

PASSIVATION:

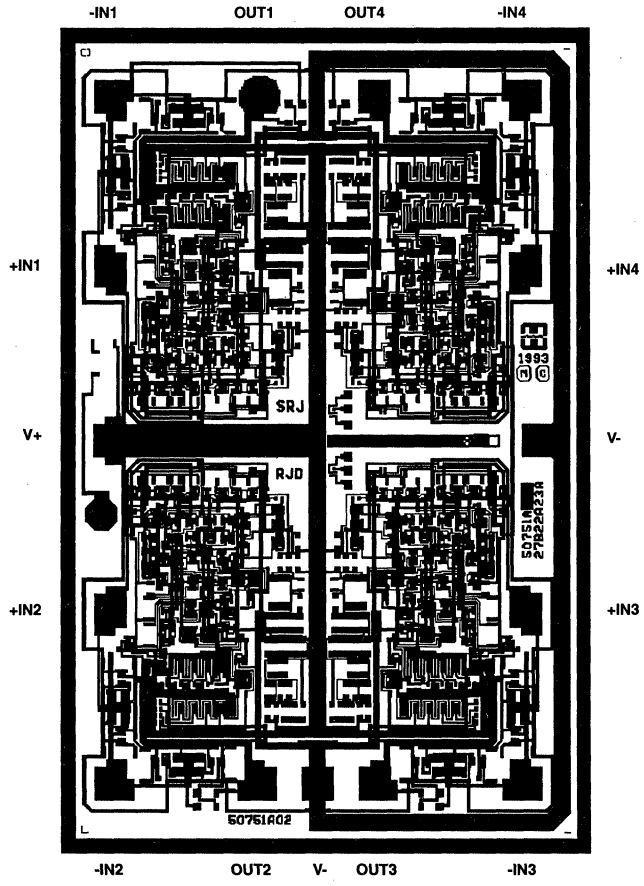
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

320

Metallization Mask Layout

HFA1412



HARRIS SEMICONDUCTOR

ICL7611, ICL7612

1.4MHz, Low Power CMOS Operational Amplifiers

November 1996

Features

- **Wide Operating Voltage Range..... ±1V to ±8V**
- **High Input Impedance..... $10^{12}\Omega$**
- **Programmable Power Consumption ... Low as 20μW**
- **Input Current Lower Than BIFETs..... 1pA (Typ)**
- **Output Voltage Swing..... V+ and V-**
- **Input Common Mode Voltage Range Greater Than Supply Rails (ICL7612)**

Applications

- **Portable Instruments**
- **Telephone Headsets**
- **Hearing Aid/Microphone Amplifiers**
- **Meter Amplifiers**
- **Medical Instruments**
- **High Impedance Buffers**

Description

The ICL761X/762X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from ±1V to ±8V, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1mA, 100μA, or 10μA, with no external components. This results in power consumption as low as 20μW. The output swing ranges to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1pA) input current, input noise current of $0.01pA/\sqrt{Hz}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

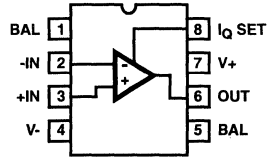
The inputs are internally protected. Outputs are fully protected against short circuits to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/μs, and unity gain bandwidth of 1MHz at I_Q = 1mA.

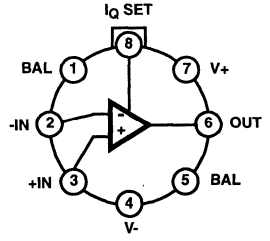
Because of the low power dissipation, junction temperature rise and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

Pinouts (See Ordering Information on Next Page)

ICL7611, ICL7612
(PDIP, SOIC)
TOP VIEW



ICL7611, ICL7612
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2919.2**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL7611ACPA	0 to 70	8 Ld PDIP - A Grade	E8.3
ICL7611BCPA	0 to 70	8 Ld PDIP - B Grade	E8.3
ICL7611DCPA	0 to 70	8 Ld PDIP - D Grade	E8.3
ICL7611ACTV	0 to 70	8 Pin Metal Can - A Grade	T8.C
ICL7611BCTV	0 to 70	8 Pin Metal Can - B Grade	T8.C
ICL7611DCTV	0 to 70	8 Pin Metal Can - D Grade	T8.C
ICL7611AMTV	-55 to 125	8 Pin Metal Can - A Grade	T8.C
ICL7611BMTV	-55 to 125	8 Pin Metal Can - B Grade	T8.C
ICL7611DMTV	-55 to 125	8 Pin Metal Can - D Grade	T8.C
ICL7611DCBA	0 to 70	8 Ld SOIC - D Grade	M8.15
ICL7611DCBA-T	0 to 70	8 Ld SOIC - D Grade - Tape and Reel	M8.15
ICL7612ACPA	0 to 70	8 Ld PDIP - A Grade	E8.3
ICL7612BCPA	0 to 70	8 Ld PDIP - B Grade	E8.3
ICL7612DCPA	0 to 70	8 Ld PDIP - D Grade	E8.3
ICL7612BCTV	0 to 70	8 Ld Metal Can - B Grade	T8.C
ICL7612DCTV	0 to 70	8 Ld Metal Can - D Grade	T8.C
ICL7612AMTV	-55 to 125	8 Ld Metal Can - A Grade	T8.C
ICL7612BMTV	-55 to 125	8 Ld Metal Can - B Grade	T8.C
ICL7612DMTV	-55 to 125	8 Ld Metal Can - D Grade	T8.C
ICL7612DCBA	0 to 70	8 Ld SOIC - D Grade	M8.15
ICL7612DCBA-T	0 to 70	8 Ld SOIC - D Grade - Tape and Reel	M8.15

Absolute Maximum Ratings

Supply Voltage V+ to V- 18V
Input Voltage . . . . . V- -0.3 to V+ +0.3V
Differential Input Voltage (Note 1) . . . . . [(V+ +0.3) - (V- -0.3)]V
Duration of Output Short Circuit (Note 2) . . . . . Unlimited

Operating Conditions

Temperature Range
ICL76XXM . . . . . -55°C to 125°C
ICL76XXC . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	130	N/A
SOIC Package	170	N/A
Metal Can Package	160	75

Maximum Junction Temperature (Can Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
2. The outputs may be shorted to ground or to either supply, for $V_{SUPPLY} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 5V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611A, ICL7612A			ICL7611B, ICL7612B			ICL7611D, ICL7612D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	25	-	-	2	-	-	5	-	-	15	mV
			Full	-	-	3	-	-	7	-	-	20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$	-	-	10	-	-	15	-	-	25	-	µV/°C
Input Offset Current	I_{OS}		25	-	0.5	30	-	0.5	30	-	0.5	30	pA
			0 to 70	-	-	300	-	-	300	-	-	300	pA
			-55 to 125	-	-	800	-		800	-		800	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	-	1.0	50	-	1.0	50	pA
			0 to 70	-	-	400	-	-	400	-	-	400	pA
			-55 to 125	-	-	4000	-	-	4000	-	-	4000	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}	$I_Q = 10\mu A$	25	±4.4	-	-	±4.4	-	-	±4.4	-	-	V
		$I_Q = 100\mu A$	25	±4.2	-	-	±4.2	-	-	±4.2	-	-	V
		$I_Q = 1mA$	25	±3.7	-	-	±3.7	-	-	±3.7	-	-	V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}	$I_Q = 10\mu A$	25	±5.3	-	-	±5.3	-	-	±5.3	-	-	V
		$I_Q = 100\mu A$	25	+5.3, -5.1	-	-	+5.3, -5.1	-	-	+5.3, -5.1	-	-	V
		$I_Q = 1mA$	25	+5.3, -4.5	-	-	+5.3, -4.5	-	-	+5.3, -4.5	-	-	V
Output Voltage Swing	V_{OUT}	$I_Q = 10\mu A$, $R_L = 1M\Omega$	25	±4.9	-	-	±4.9	-	-	±4.9	-	-	V
			0 to 70	±4.8	-	-	±4.8	-	-	±4.8	-	-	V
			-55 to 125	±4.7	-	-	±4.7	-	-	±4.7	-	-	V
		$I_Q = 100\mu A$, $R_L = 100k\Omega$	25	±4.9	-	-	±4.9	-	-	±4.9	-	-	V
			0 to 70	±4.8	-	-	±4.8	-	-	±4.8	-	-	V
			-55 to 125	±4.5	-	-	±4.5	-	-	±4.5	-	-	V
		$I_Q = 1mA$, $R_L = 10k\Omega$	25	±4.5	-	-	±4.5	-	-	±4.5	-	-	V
			0 to 70	±4.3	-	-	±4.3	-	-	±4.3	-	-	V
			-55 to 125	±4.0	-	-	±4.0	-	-	±4.0	-	-	V

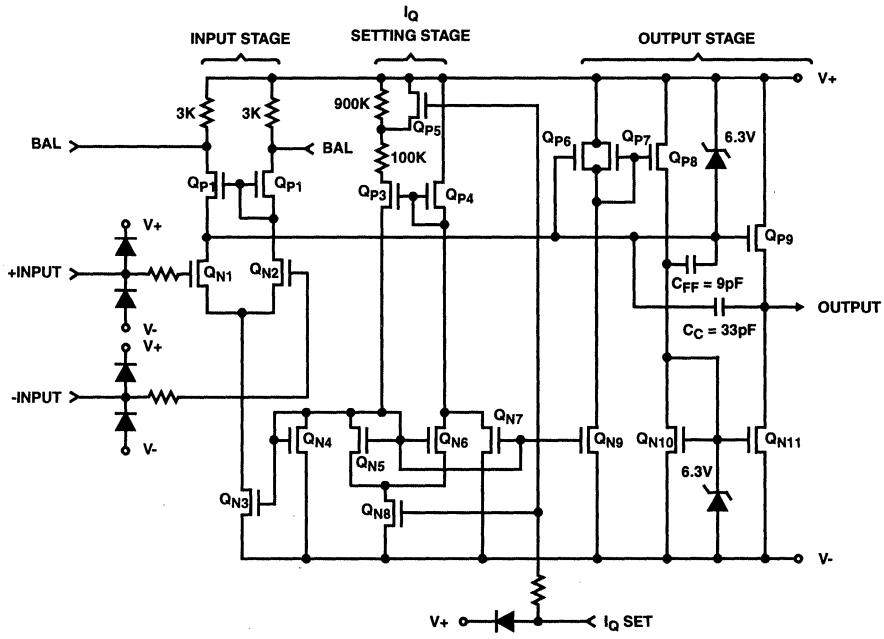
Electrical Specifications V_{SUPPLY} = ±5V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611A, ICL7612A			ICL7611B, ICL7612B			ICL7611D, ICL7612D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Voltage Gain	A_{VOL}	V_O = ±4.0V, R_L = 1MΩ, I_Q = 10µA	25	86	104	-	80	104	-	80	104	-	dB
			0 to 70	80	-	-	75	-	-	75	-	-	dB
			-55 to 125	74	-	-	68	-	-	68	-	-	dB
		V_O = ±4.0V, R_L = 100kΩ, I_Q = 100µA	25	86	102	-	80	102	-	80	102	-	dB
			0 to 70	80	-	-	75	-	-	75	-	-	dB
			-55 to 125	74	-	-	68	-	-	68	-	-	dB
		V_O = ±4.0V, R_L = 10kΩ, I_Q = 1mA	25	80	83	-	76	83	-	76	83	-	dB
			0 to 70	76	-	-	72	-	-	72	-	-	dB
			-55 to 125	72	-	-	68	-	-	68	-	-	dB
Unity Gain Bandwidth	GBW	I_Q = 10µA	25	-	0.044	-	-	0.044	-	-	0.044	-	MHz
		I_Q = 100µA	25	-	0.48	-	-	0.48	-	-	0.48	-	MHz
		I_Q = 1mA	25	-	1.4	-	-	1.4	-	-	1.4	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	R_S ≤ 100kΩ, I_Q = 10µA	25	76	96	-	70	96	-	70	96	-	dB
		R_S ≤ 100kΩ, I_Q = 100µA	25	76	91	-	70	91	-	70	91	-	dB
		R_S ≤ 100kΩ, I_Q = 1mA	25	66	87	-	60	87	-	60	87	-	dB
Power Supply Rejection Ratio (V_{SUPPLY} = ±8V to ±2V)	PSRR	R_S ≤ 100kΩ, I_Q = 10µA	25	80	94	-	80	94	-	80	94	-	dB
		R_S ≤ 100kΩ, I_Q = 100µA	25	80	86	-	80	86	-	80	86	-	dB
		R_S ≤ 100kΩ, I_Q = 1mA	25	70	77	-	70	77	-	70	77	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz	25	-	100	-	-	100	-	-	100	-	nV/√Hz
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz	25	-	0.01	-	-	0.01	-	-	0.01	-	pA/√Hz
Supply Current (No Signal, No Load)	I_{SUPPLY}	I_Q SET = +5V, Low Bias	25	-	0.01	0.02	-	0.01	0.02	-	0.01	0.02	mA
		I_Q SET = 0V, Medium Bias	25	-	0.1	0.25	-	0.1	0.25	-	0.1	0.25	mA
		I_Q SET = -5V, High Bias	25	-	1.0	2.5	-	1.0	2.5	-	1.0	2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_V = 100	25	-	120	-	-	120	-	-	120	-	dB
Slew Rate (A_V = 1, C_L = 100pF, V_{IN} = $8V_{P-P}$)	SR	I_Q = 10µA, R_L = 1MΩ	25	-	0.016	-	-	0.016	-	-	0.016	-	V/µs
		I_Q = 100µA, R_L = 100kΩ	25	-	0.16	-	-	0.16	-	-	0.16	-	V/µs
		I_Q = 1mA, R_L = 10kΩ	25	-	1.6	-	-	1.6	-	-	1.6	-	V/µs
Rise Time (V_{IN} = 50mV, C_L = 100pF)	t_R	I_Q = 10µA, R_L = 1MΩ	25	-	20	-	-	20	-	-	20	-	µs
		I_Q = 100µA, R_L = 100kΩ	25	-	2	-	-	2	-	-	2	-	µs
		I_Q = 1mA, R_L = 10kΩ	25	-	0.9	-	-	0.9	-	-	0.9	-	µs
Overshoot Factor (V_{IN} = 50mV, C_L = 100pF)	OS	I_Q = 10µA, R_L = 1MΩ	25	-	5	-	-	5	-	-	5	-	%
		I_Q = 100µA, R_L = 100kΩ	25	-	10	-	-	10	-	-	10	-	%
		I_Q = 1mA, R_L = 10kΩ	25	-	40	-	-	40	-	-	40	-	%

Electrical Specifications $V_{SUPPLY} = \pm 1V$, $I_Q = 10\mu A$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611A, ICL7612A			ICL7611B, ICL7612B			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	25	-	-	2	-	-	5	mV
			Full	-	-	3	-	-	7	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$	-	-	10	-	-	15	-	$\mu V/^oC$
Input Offset Current	I_{OS}		25	-	0.5	30	-	0.5	30	pA
			0 to 70	-	-	300	-	-	300	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	-	1.0	50	pA
			0 to 70	-	-	500	-	-	500	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}		25	±0.6	-	-	±0.6	-	-	V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}		25	+0.6 to -1.1	-	-	+0.6 to -1.1	-	-	V
Output Voltage Swing	V_{OUT}	$R_L = 1M\Omega$	25	±0.98	-	-	±0.98	-	-	V
			0 to 70	±0.96	-	-	±0.96	-	-	V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 0.1V$, $R_L = 1M\Omega$	25	-	90	-	-	90	-	dB
			0 to 70	-	80	-	-	80	-	dB
Unity Gain Bandwidth	GBW		25	-	0.044	-	-	0.044	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$	25	-	80	-	-	80	-	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 100k\Omega$	25	-	80	-	-	80	-	dB
Input Referred Noise Voltage	e_N	$R_S = 100\Omega$, f = 1kHz	25	-	100	-	-	100	-	$nV/\sqrt{Hz}$
Input Referred Noise Current	i_N	$R_S = 100\Omega$, f = 1kHz	25	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
Supply Current	I_{SUPPLY}	No Signal, No Load	25	-	6	15	-	6	15	μA
Slew Rate	SR	$A_V = 1$, $C_L = 100pF$, $V_{IN} = 0.2V_{P-P}$, $R_L = 1M\Omega$	25	-	0.016	-	-	0.016	-	$V/\mu s$
Rise Time	t_R	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$	25	-	20	-	-	20	-	μs
Overshoot Factor	OS	$V_{IN} = 50mV$, $C_L = 100pF$, $R_L = 1M\Omega$	25	-	5	-	-	5	-	%

Schematic Diagram



Application Information

Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (PNPN) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

Choosing the Proper I_Q

The ICL7611 and ICL7612 have a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10µA, 100µA or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12 have an external I_Q control terminal, permitting user selection of quiescent current. To set the I_Q connect the I_Q terminal as follows:

I_Q = 10µA - I_Q pin to V+

I_Q = 100µA - I_Q pin to ground. If this is not possible, any voltage from V+ - 0.8 to V- +0.8 can be used.

I_Q = 1mA - I_Q pin to V-

NOTE: The output current available is a function of the quiescent current setting. For maximum peak-to-peak output voltage swings into low impedance loads, IQ of 1mA should be selected.

Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1MΩ, 100kΩ, and 10kΩ, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

Input Offset Nulling

Offset nulling may be achieved by connecting a 25K pot between the BAL terminals with the wiper connected to V+. At quiescent currents of 1mA and 100µA the nulling range provided is adequate for all V_{OS} selections; however with I_Q = 10µA, nulling may not be possible with higher values of V_{OS}.

Frequency Compensation

The ICL7611 and ICL7612 are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF.

Extended Common Mode Input Range

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1V for applications where $V_{SUPP} \geq \pm 1.5V$. For those applications where $V_{SUPP} \leq \pm 1.5V$ the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1V in the negative direction (e.g., for $V_{SUPPLY} = \pm 1V$, the input CMVR would be +0.6V to -1.1V).

Operation At $V_{SUPPLY} = \pm 1V$

Operation at $V_{SUPPLY} = \pm 1V$ is guaranteed at I_Q = 10µA for A and B grades only.

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1M\Omega$. Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to -0.7V at $V_{SUPPLY} = \pm 1V$. For applications where greater common mode range is desirable, refer to the description of ICL7612 above.

Typical Applications

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

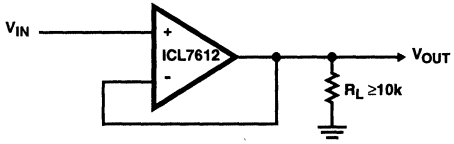
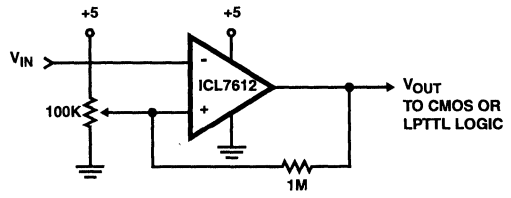


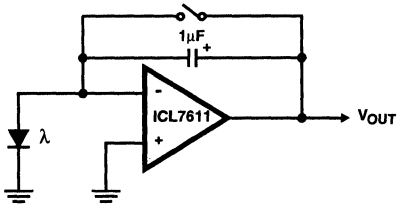
FIGURE 1. SIMPLE FOLLOWER (NOTE 4)



NOTE:

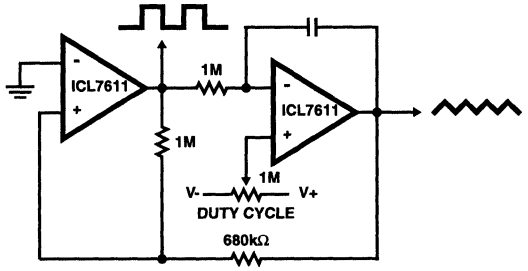
4. By using the ICL7612 in this application, the circuit will follow rail to rail inputs.

FIGURE 2. LEVEL DETECTOR (NOTE 4)



NOTE: Low leakage currents allow integration times up to several hours.

FIGURE 3. PHOTOCURRENT INTEGRATOR



WAVEFORM GENERATOR

NOTE: Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

FIGURE 4. PRECISE TRIANGLE/SQUARE WAVE GENERATOR

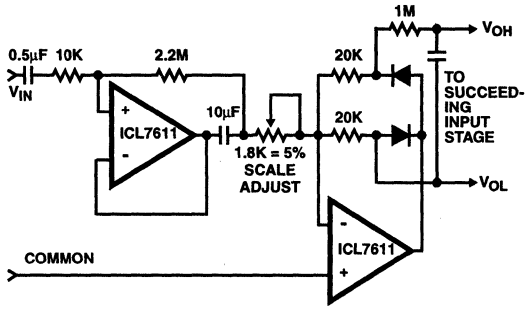


FIGURE 5. AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS ICL7106, ICL7107, ICL7109, ICL7116, ICL7117

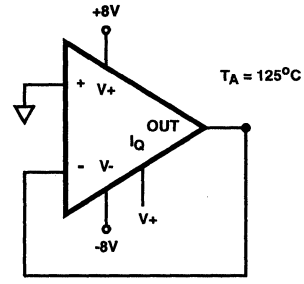


FIGURE 6. BURN-IN AND LIFE TEST CIRCUIT

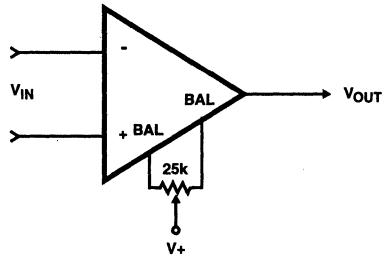
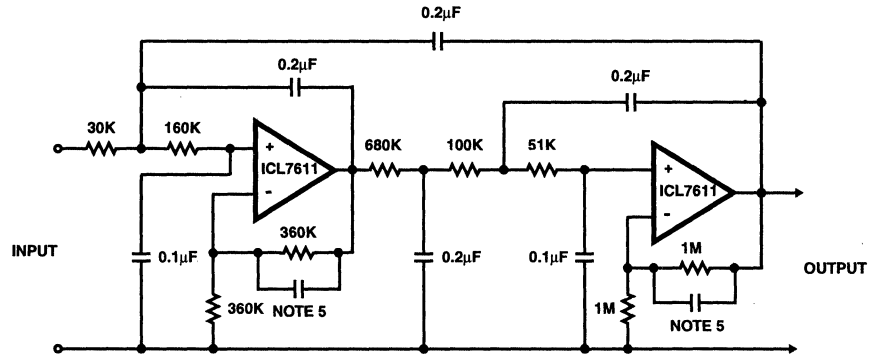


FIGURE 7. V_{OS} NULL CIRCUIT



NOTES:

5. Note that small capacitors (25pF to 50pF) may be needed for stability in some cases.
6. The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. f_C = 10Hz, A_{VCL} = 4, Passband ripple = 0.1dB.

FIGURE 8. FIFTH ORDER CHEBYCHEV MULTIPLE FEEDBACK LOW PASS FILTER

Typical Performance Curves

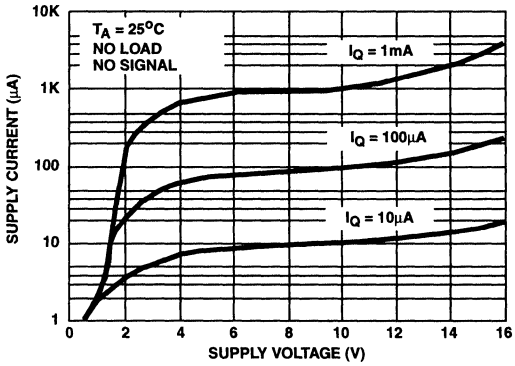


FIGURE 9. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

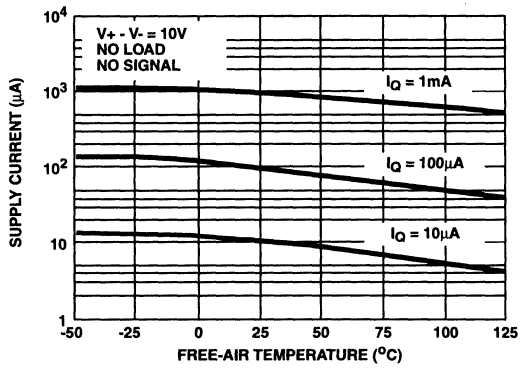


FIGURE 10. SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

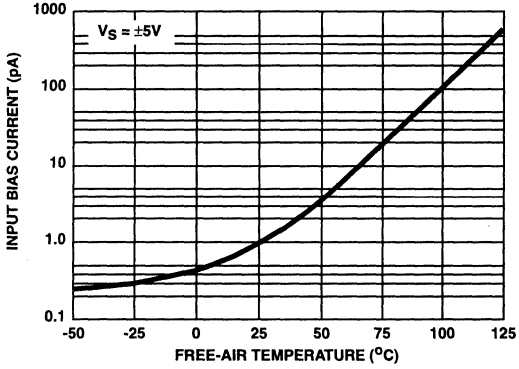


FIGURE 11. INPUT BIAS CURRENT vs TEMPERATURE

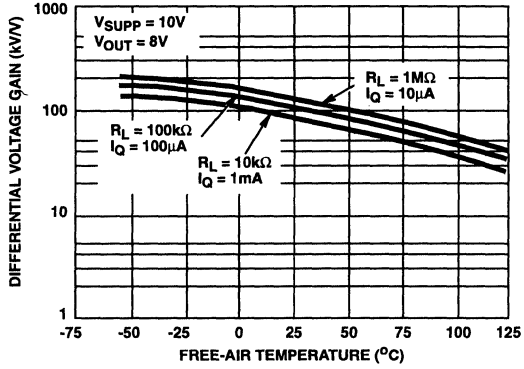


FIGURE 12. LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN vs FREE-AIR TEMPERATURE

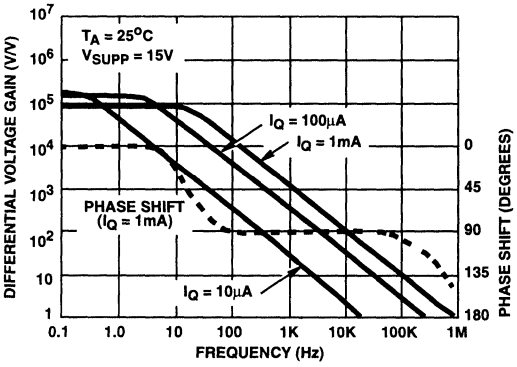


FIGURE 13. LARGE SIGNAL FREQUENCY RESPONSE

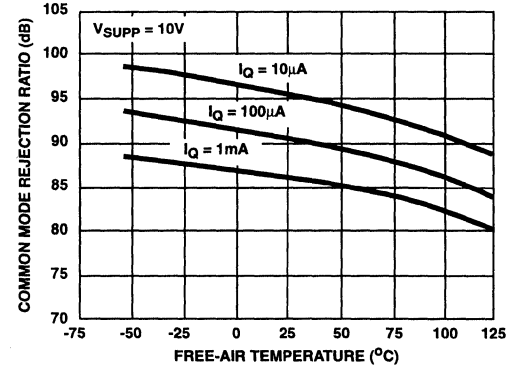


FIGURE 14. COMMON MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

Typical Performance Curves (Continued)

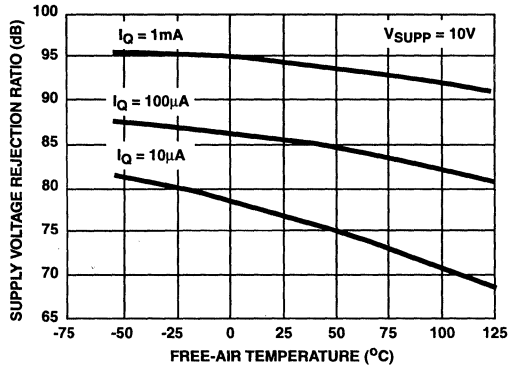


FIGURE 15. POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

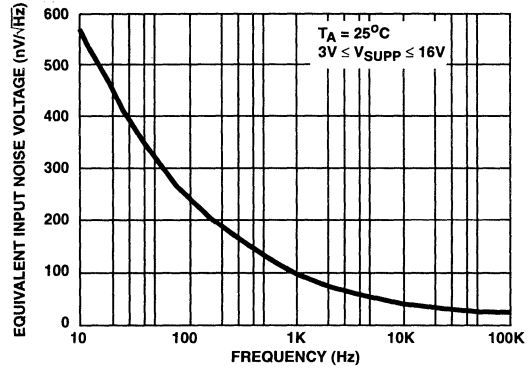


FIGURE 16. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

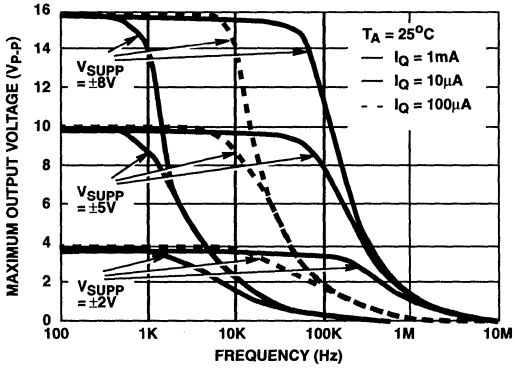


FIGURE 17. OUTPUT VOLTAGE vs FREQUENCY

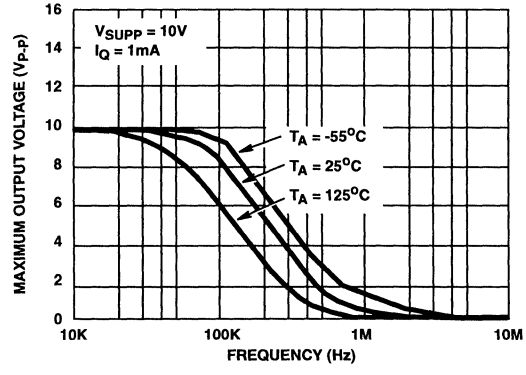


FIGURE 18. OUTPUT VOLTAGE vs FREQUENCY

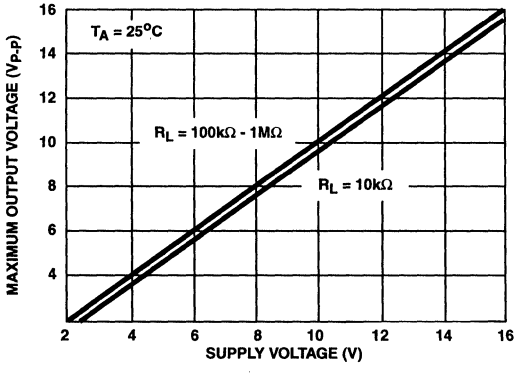


FIGURE 19. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

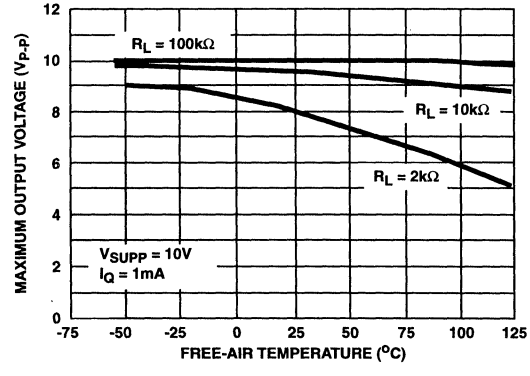


FIGURE 20. OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

Typical Performance Curves (Continued)

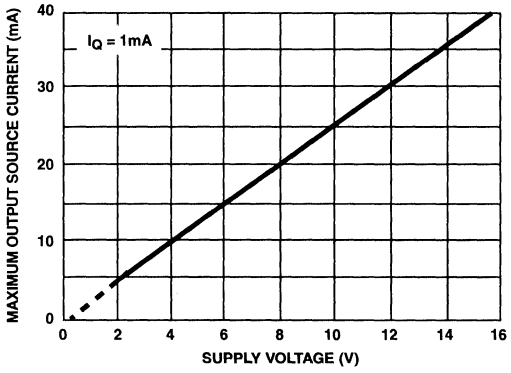


FIGURE 21. OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE

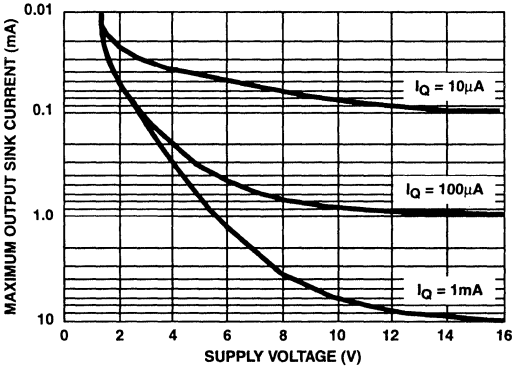


FIGURE 22. OUTPUT SINK CURRENT vs SUPPLY VOLTAGE

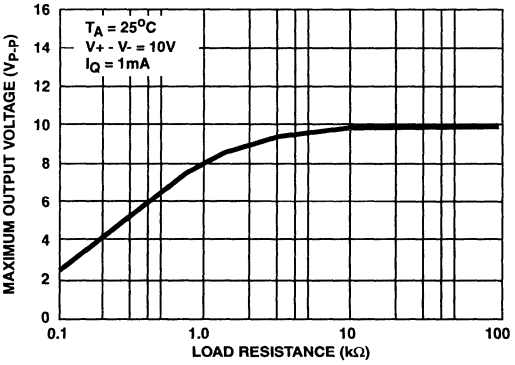


FIGURE 23. OUTPUT VOLTAGE vs LOAD RESISTANCE

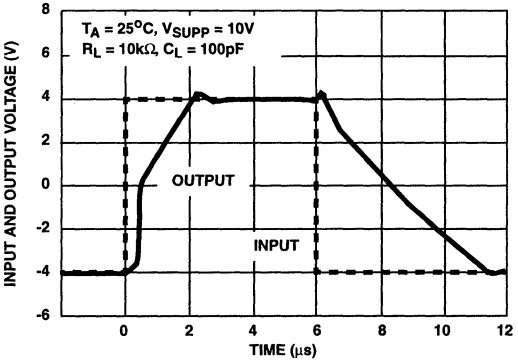


FIGURE 24. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 1mA)

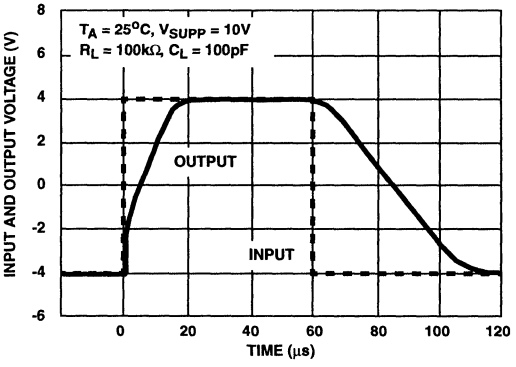


FIGURE 25. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 100µA)

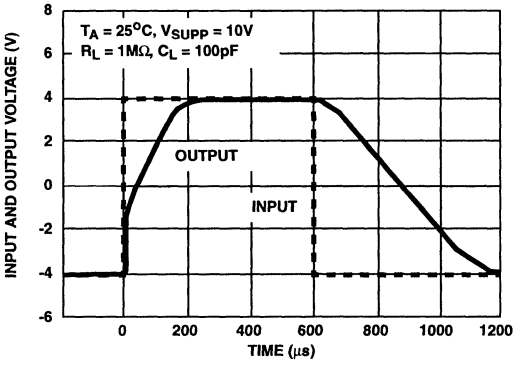


FIGURE 26. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 10µA)

HARRIS SEMICONDUCTOR

ICL7621, ICL7641, ICL7642

Dual/Quad, Low Power CMOS Operational Amplifiers

November 1996

Features

- Wide Operating Voltage Range..... ±1V to ±8V
- High Input Impedance .....$10^{12}\Omega$
- Input Current Lower Than BIFETs .....1pA (Typ)
- Output Voltage Swing .....V+ and V-
- Available as Duals and Quads (Refer to ICL7611 for Singles)
- Low Power Replacement for Many Standard Op Amps

Applications

- Portable Instruments
- Telephone Headsets
- Hearing Aid/Microphone Amplifiers
- Meter Amplifiers
- Medical Instruments
- High Impedance Buffers

Description

The ICL761X/762X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents. They are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from ±1V to ±8V, and may be operated from a single Lithium cell. The output swing ranges to within a few millivolts of the supply voltages.

The quiescent supply current of these amplifiers is set to 3 different ranges at the factory. Both amps of the dual ICL7621 are set to an I_Q of 100µA, while each amplifier of the quad ICL7641 and ICL7642 are set to an I_Q of 1mA and 10µA respectively. This results in power consumption as low as 20µW per amplifier.

Of particular significance is the extremely low (1pA) input current, input noise current of $0.01pA/\sqrt{Hz}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

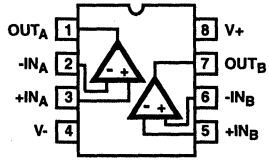
The inputs are internally protected. Outputs are fully protected against short circuits to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/µs, and unity gain bandwidth of 1MHz at I_Q = 1mA.

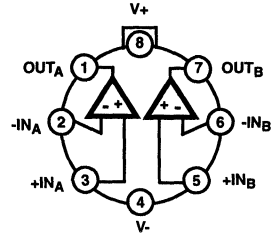
Because of the low power dissipation, junction temperature rise and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

Pinouts (See Ordering Information on Next Page)

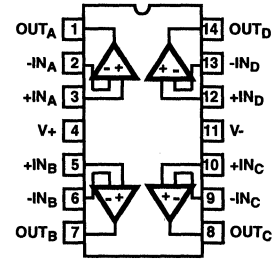
ICL7621 (PDIP, SOIC) TOP VIEW



ICL7621 (METAL CAN) TOP VIEW



ICL7641 (PDIP)
ICL7642 (PDIP) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **3403.1**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL7621ACPA	0 to 70	8 Ld PDIP - A Grade - I_Q = 100µA	E8.3
ICL7621BCPA	0 to 70	8 Ld PDIP - B Grade - I_Q = 100µA	E8.3
ICL7621DCPA	0 to 70	8 Ld PDIP - D Grade - I_Q = 100µA	E8.3
ICL7621BCTV	0 to 70	8 Pin Metal Can - B Grade - I_Q = 100µA	T8.C
ICL7621DCTV	0 to 70	8 Pin Metal Can - D Grade - I_Q = 100µA	T8.C
ICL7621AMTV	-55 to 125	8 Pin Metal Can - A Grade - I_Q = 100µA	T8.C
ICL7621BMTV	-55 to 125	8 Pin Metal Can - B Grade - I_Q = 100µA	T8.C
ICL7621DMTV	-55 to 125	8 Pin Metal Can - D Grade - I_Q = 100µA	T8.C
ICL7621DCBA	0 to 70	8 Ld SOIC - D Grade - I_Q = 100µA	M8.15
ICL7621DCBA-T	0 to 70	8 Ld SOIC - D Grade - Tape and Reel - I_Q = 100µA	M8.15
ICL7641CCPD	0 to 70	14 Ld PDIP - C Grade - I_Q = 1mA	E14.3
ICL7641ECPD	0 to 70	14 Ld PDIP - E Grade - I_Q = 1mA	E14.3
ICL7642CCPD	0 to 70	14 Ld PDIP - C Grade - I_Q = 10µA	E14.3
ICL7642ECPD	0 to 70	14 Ld PDIP - E Grade - I_Q = 10µA	E14.3

Absolute Maximum Ratings

Supply Voltage V+ to V- 18V
Input Voltage . . . . . V- -0.3 to V+ +0.3V
Differential Input Voltage (Note 1) . . . . . [(V+ +0.3) - (V- -0.3)]V
Duration of Output Short Circuit (Note 2) . . . . . Unlimited

Operating Conditions

Temperature Range
ICL76XXM . . . . . -55°C to 125°C
ICL76XXC . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package	160	N/A
Metal Can Package	160	75
8 Lead PDIP Package	120	N/A
14 Lead PDIP Package	80	N/A

Maximum Junction Temperature (Hermetic Packages) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
2. The outputs may be shorted to ground or to either supply, for $V_{SUPPLY} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 5V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	ICL7621A			ICL7621B			ICL7621D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	25	-	-	2	-	-	5	-	-	15	mV
			Full	-	-	3	-	-	7	-	-	20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$	-	-	10	-	-	15	-	-	25	-	µV/°C
Input Offset Current	I_{OS}		25	-	0.5	30	-	0.5	30	-	0.5	30	pA
			0 to 70	-	-	300	-	-	300	-	-	300	pA
			-55 to 125	-	-	800	-		800	-		800	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	-	1.0	50	-	1.0	50	pA
			0 to 70	-	-	400	-	-	400	-	-	400	pA
			-55 to 125	-	-	4000	-	-	4000	-	-	4000	pA
Common Mode Voltage Range	V_{CMR}	$I_Q = 100\mu A$	25	±4.2	-	-	±4.2	-	-	±4.2	-	-	V
Output Voltage Swing	V_{OUT}	$I_Q = 100\mu A$, $R_L = 100k\Omega$,	25	±4.9	-	-	±4.9	-	-	±4.9	-	-	V
			0 to 70	±4.8	-	-	±4.8	-	-	±4.8	-	-	V
			-55 to 125	±4.5	-	-	±4.5	-	-	±4.5	-	-	V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 4.0V$, $R_L = 100k\Omega$, $I_Q = 100\mu A$	25	86	102	-	80	102	-	80	102	-	dB
			0 to 70	80	-	-	75	-	-	75	-	-	dB
			-55 to 125	74	-	-	68	-	-	68	-	-	dB
Unity Gain Bandwidth	GBW	$I_Q = 100\mu A$	25	-	0.48	-	-	0.48	-	-	0.48	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$, $I_Q = 100\mu A$	25	76	91	-	70	91	-	70	91	-	dB
Power Supply Rejection Ratio ($V_{SUPPLY} = \pm 8V$ to $\pm 2V$)	PSRR	$R_S \leq 100k\Omega$, $I_Q = 100\mu A$	25	80	86	-	80	86	-	80	86	-	dB
Input Referred Noise Voltage	e_N	$R_S = 100\Omega$, f = 1kHz	25	-	100	-	-	100	-	-	100	-	$nV/\sqrt{Hz}$

Electrical Specifications V_{SUPPLY} = ±5V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	ICL7621A			ICL7621B			ICL7621D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz	25	-	0.01	-	-	0.01	-	-	0.01	-	pA/√Hz
Supply Current (Per Amplifier)	I_{SUPPLY}	No Signal, No Load, I_Q = 100µA	25	-	0.1	0.25	-	0.1	0.25	-	0.1	0.25	mA
Channel Separation	V_{O1}/V_{O2}	A_V = 100	25	-	120	-	-	120	-	-	120	-	dB
Slew Rate	SR	A_V = 1, C_L = 100pF, V_{IN} = $8V_{P-P}$, I_Q = 100µA, R_L = 100kΩ	25	-	0.16	-	-	0.16	-	-	0.16	-	V/µs
Rise Time	t_R	V_{IN} = 50mV, C_L = 100pF, I_Q = 100µA, R_L = 100kΩ	25	-	2	-	-	2	-	-	2	-	µs
Overshoot Factor	OS	V_{IN} = 50mV, C_L = 100pF, I_Q = 100µA, R_L = 100kΩ	25	-	10	-	-	10	-	-	10	-	%

Electrical Specifications V_{SUPPLY} = ±5V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	ICL7641C, ICL7642C			ICL7641E, ICL7642E			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	25	-	-	10	-	-	20	mV
			Full	-	-	15	-	-	25	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$	-	-	20	-	-	30	-	µV/°C
Input Offset Current	I_{OS}		25	-	0.5	30	-	0.5	30	pA
			0 to 70	-	-	300	-	-	300	pA
			-55 to 125	-	-	800	-		800	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	-	1.0	50	pA
			0 to 70	-	-	500	-	-	500	pA
			-55 to 125	-	-	4000	-	-	4000	pA
Common Mode Voltage Range	V_{CMR}	I_Q = 10µA, ICL7642	25	±4.4	-	-	±4.4	-	-	V
		I_Q = 1mA, ICL7641	25	±3.7	-	-	±3.7	-	-	V
Output Voltage Swing	V_{OUT}	ICL7642, I_Q = 10µA, R_L = 1MΩ	25	±4.9	-	-	±4.9	-	-	V
			0 to 70	±4.8	-	-	±4.8	-	-	V
			-55 to 125	±4.7	-	-	±4.7	-	-	V
		ICL7641, I_Q = 1mA, R_L = 10kΩ	25	±4.5	-	-	±4.5	-	-	V
			0 to 70	±4.3	-	-	±4.3	-	-	V
			-55 to 125	±4.0	-	-	±4.0	-	-	V

Electrical Specifications V_{SUPPLY} = ±5V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	ICL7641C, ICL7642C			ICL7641E, ICL7642E			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Voltage Gain	A_{VOL}	ICL7642, V_O = ±4V, R_L = 1MΩ, I_Q = 10µA	25	80	104	-	80	104	-	dB
			0 to 70	75	-	-	75	-	-	dB
			-55 to 125	68	-	-	68	-	-	dB
		ICL7641, V_O = ±4V, R_L = 10kΩ, I_Q = 1mA	25	76	98	-	76	98	-	dB
			0 to 70	72	-	-	72	-	-	dB
			-55 to 125	68	-	-	68	-	-	dB
Unity Gain Bandwidth	GBW	ICL 7642, I_Q = 10µA	25	-	0.044	-	-	0.044	-	MHz
		ICL 7641, I_Q = 1mA	25	-	1.4	-	-	1.4	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	ICL7642, R_S ≤ 100kΩ, I_Q = 10µA	25	70	96	-	70	96	-	dB
		ICL7641, R_S ≤ 100kΩ, I_Q = 1mA	25	60	87	-	60	87	-	dB
Power Supply Rejection Ratio (V_{SUPPLY} = ±8V to ±2V)	PSRR	ICL7642, R_S ≤ 100kΩ, I_Q = 10µA	25	80	94	-	80	94	-	dB
		ICL7641, R_S ≤ 100kΩ, I_Q = 1mA	25	70	77	-	70	77	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz	25	-	100	-	-	100	-	$nV/\sqrt{Hz}$
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz	25	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
Supply Current (Per Amplifier) (No Signal, No Load)	I_{SUPPLY}	ICL7642, I_Q = 10µA Low Bias	25	-	0.01	0.03	-	0.01	0.03	mA
		ICL7641, I_Q = 1mA High Bias	25	-	1.0	2.5	-	1.0	2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_V = 100	25	-	120	-	-	120	-	dB
Slew Rate (A_V = 1, C_L = 100pF, V_{IN} = $8V_{P-P}$)	SR	ICL7642, I_Q = 10µA, R_L = 1MΩ	25	-	0.016	-	-	0.016	-	V/µs
		ICL7641, I_Q = 1mA, R_L = 10kΩ	25	-	1.6	-	-	1.6	-	V/µs
Rise Time (V_{IN} = 50mV, C_L = 100pF)	t_R	ICL7642, I_Q = 10µA, R_L = 1MΩ	25	-	20	-	-	20	-	µs
		ICL7641, I_Q = 1mA, R_L = 10kΩ	25	-	0.9	-	-	0.9	-	µs
Overshoot Factor (V_{IN} = 50mV, C_L = 100pF)	OS	ICL7642, I_Q = 10µA, R_L = 1MΩ	25	-	5	-	-	5	-	%
		ICL7641, I_Q = 1mA, R_L = 10kΩ	25	-	40	-	-	40	-	%

Electrical Specifications V_{SUPPLY} = ±1V, I_Q = 10µA, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	TEMP. (°C)	ICL7642C			UNITS
				MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	R_S ≤ 100kΩ	25	-	-	10	mV
			Full	-	-	12	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	R_S ≤ 100kΩ	-	-	20	-	µV/°C
Input Offset Current	I_{OS}		25	-	0.5	30	pA
			0 to 70	-	-	300	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	pA
			0 to 70	-	-	500	pA
Common Mode Voltage Range	V_{CMR}		25	±0.6	-	-	V

Electrical Specifications V_{SUPPLY} = ±1V, I_Q = 10µA, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	TEMP. (°C)	ICL7642C MIN	ICL7642C TYP	ICL7642C MAX	UNITS
Output Voltage Swing	V_{OUT}	R_L = 1MΩ	25	-	±0.98	-	V
			0 to 70	-	±0.96	-	V
Large Signal Voltage Gain	A_{VOL}	V_O = ±0.1V, R_L = 1MΩ	25	-	90	-	dB
			0 to 70	-	80	-	dB
Unity Gain Bandwidth	GBW		25	-	0.044	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$	25	-	80	-	dB
Power Supply Rejection Ratio	PSRR		25	-	80	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz	25	-	100	-	nV/√Hz
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz	25	-	0.01	-	pA/√Hz
Supply Current (Per Amplifier)	I_{SUPPLY}	No Signal, No Load	25	-	6	15	µA
Channel Separation	V_{O1}/V_{O2}	A_V = 100	25	-	120	-	dB
Slew Rate	SR	A_V = 1, C_L = 100pF, V_{IN} = 0.2V_{P-P}, R_L = 1MΩ	25	-	0.016	-	V/µs
Rise Time	t_R	V_{IN} = 50mV, C_L = 100pF R_L = 1MΩ	25	-	20	-	µs
Overshoot Factor	OS	V_{IN} = 50mV, C_L = 100pF, R_L = 1MΩ	25	-	5	-	%

Schematic Diagram

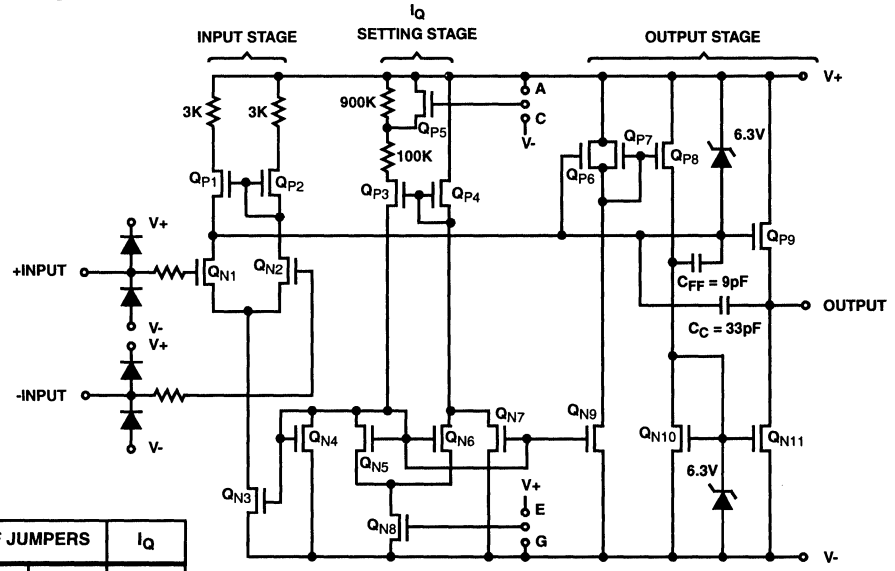


TABLE OF JUMPERS		I_Q
ICL7621	C, E	100µA
ICL7641	C, G	1mA
ICL7642	A, E	10µA

Application Information

Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (PNPN) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

Choosing the Proper I_Q

Each device in the ICL76XX family has a similar I_Q setup scheme, which allows the amplifier to be set to nominal quiescent currents of 10µA, 100µA or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. The ICL7621 and ICL7641/7642 have fixed I_Q settings:

ICL7621 (Dual) - I_Q = 100µA

ICL7641 (Quad) - I_Q = 1mA

ICL7642 (Quad) - I_Q = 10µA

NOTE: The output current available is a function of the quiescent current setting. For maximum peak-to-peak output voltage swings into low impedance loads, I_Q of 1mA should be selected.

Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1MΩ, 100kΩ, and 10kΩ, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

Frequency Compensation

The ICL76XX are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF.

Operation At V_{SUPPLY} = ±1V

Operation at V_{SUPPLY} = ±1V is guaranteed for the ICL7642C only.

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1M\Omega$. Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to -0.7V at V_{SUPPLY} = ±1V. For applications where greater common mode range is desirable, refer to the ICL7612 data sheet.

Typical Applications

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

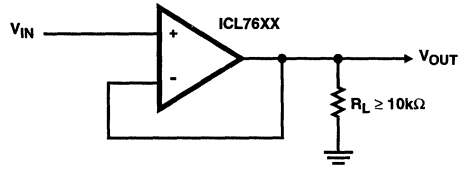


FIGURE 1. SIMPLE FOLLOWER

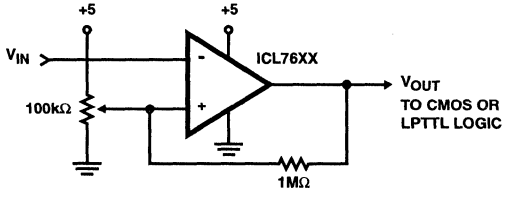
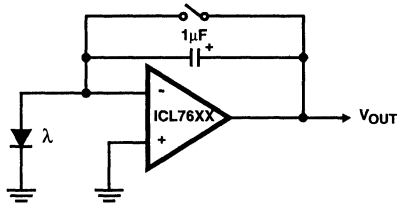
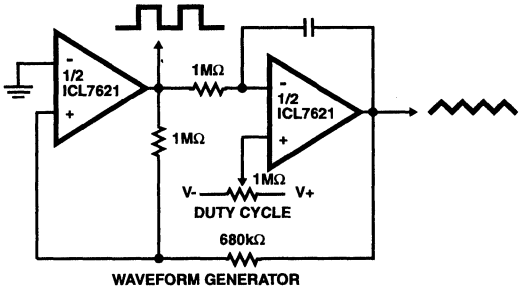


FIGURE 2. LEVEL DETECTOR



NOTE: Low leakage currents allow integration times up to several hours.

FIGURE 3. PHOTOCURRENT INTEGRATOR



NOTE: Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

FIGURE 4. TRIANGLE/SQUARE WAVE GENERATOR

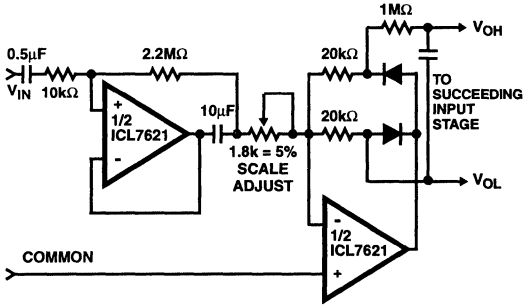


FIGURE 5. AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS ICL7106, ICL7107, ICL7109, ICL7116, ICL7117

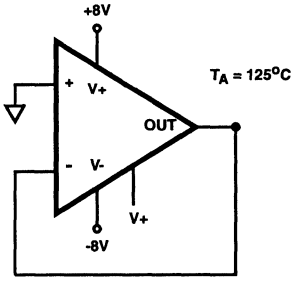
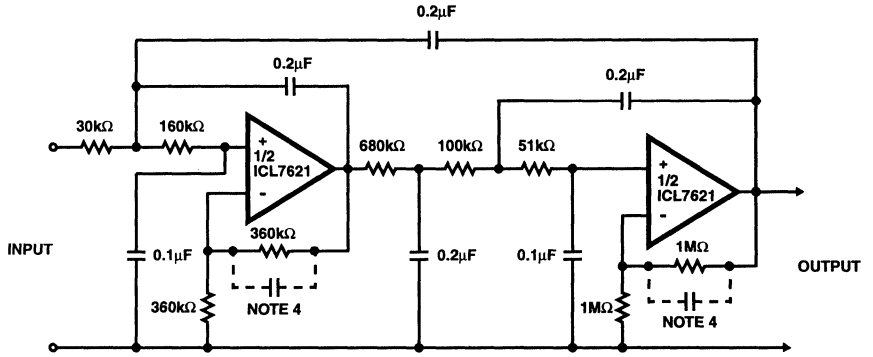


FIGURE 6. BURN-IN AND LIFE TEST CIRCUIT



NOTES:

4. Small capacitors (25 - 50pF) may be needed for stability in some cases.
5. The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. f_C = 10Hz, A_{VCL} = 4, Passband ripple = 0.1dB.

FIGURE 7. FIFTH ORDER CHEBYCHEV MULTIPLE FEEDBACK LOW PASS FILTER

Typical Performance Curves

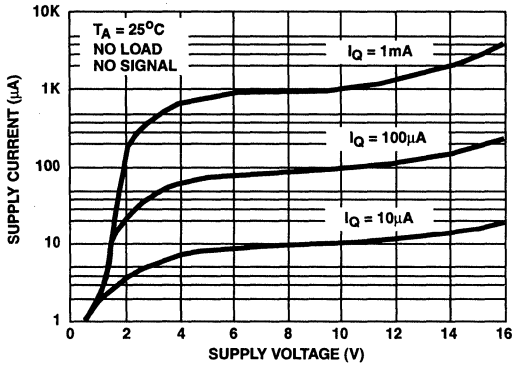


FIGURE 8. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

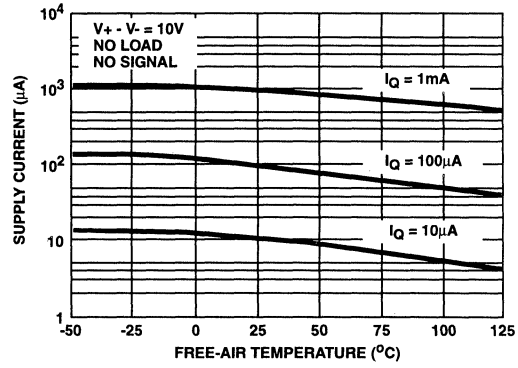


FIGURE 9. SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

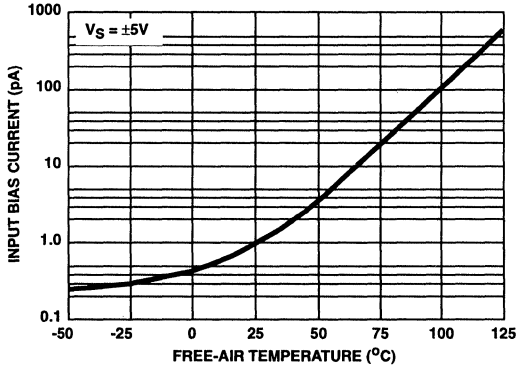


FIGURE 10. INPUT BIAS CURRENT vs TEMPERATURE

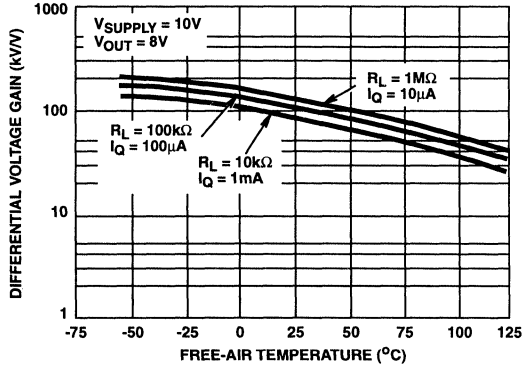


FIGURE 11. LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN vs FREE-AIR TEMPERATURE

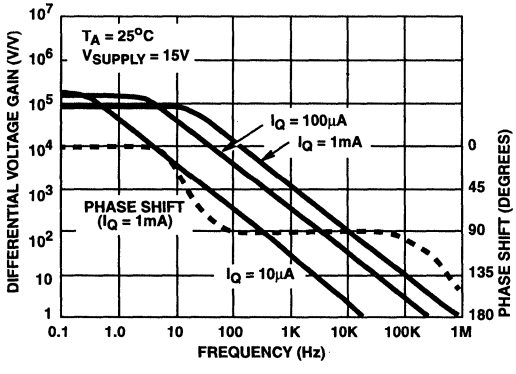


FIGURE 12. LARGE SIGNAL FREQUENCY RESPONSE

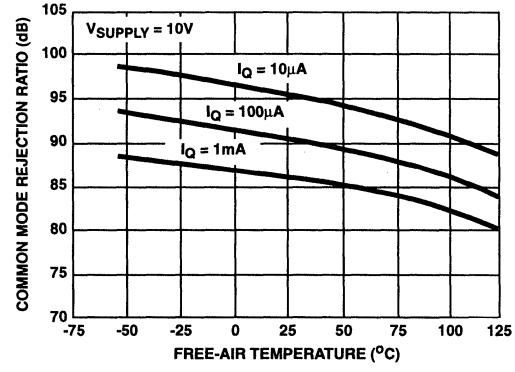


FIGURE 13. COMMON MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

Typical Performance Curves (Continued)

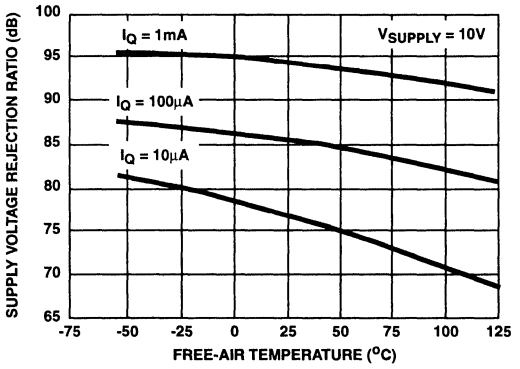


FIGURE 14. POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

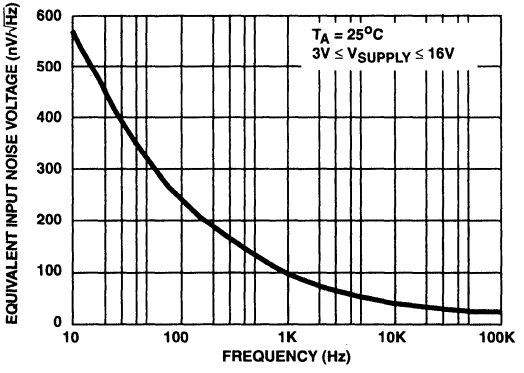


FIGURE 15. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

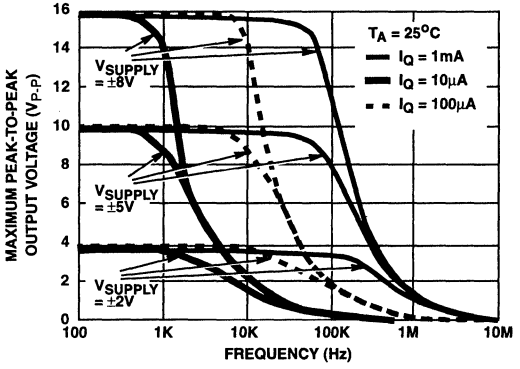


FIGURE 16. OUTPUT VOLTAGE vs FREQUENCY

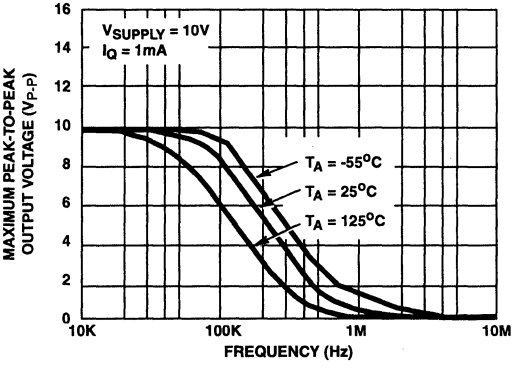


FIGURE 17. OUTPUT VOLTAGE vs FREQUENCY

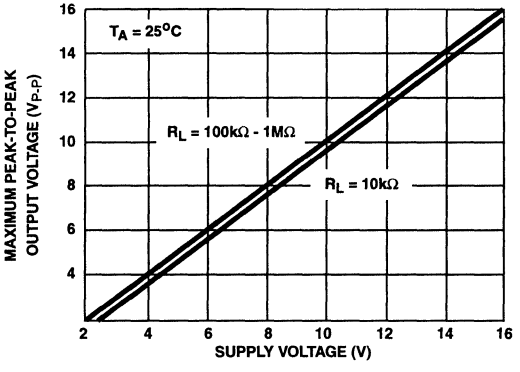


FIGURE 18. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

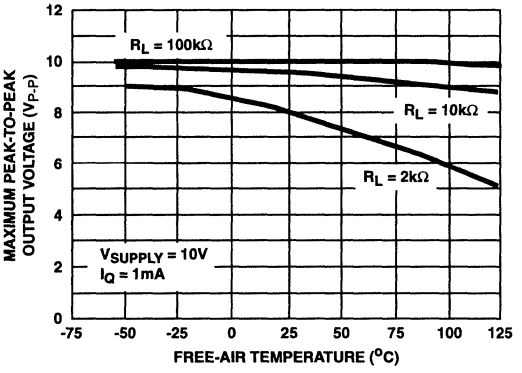


FIGURE 19. OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

3 OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued)

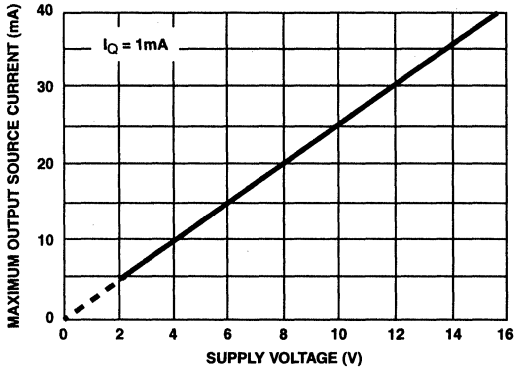


FIGURE 20. OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE

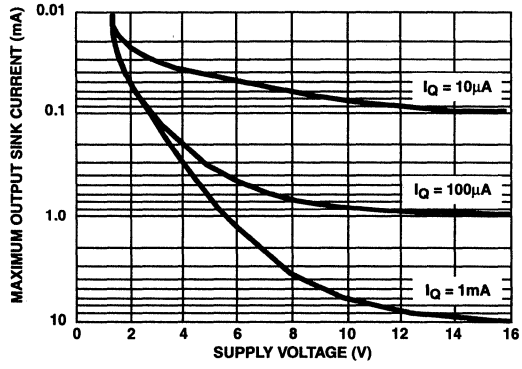


FIGURE 21. OUTPUT SINK CURRENT vs SUPPLY VOLTAGE

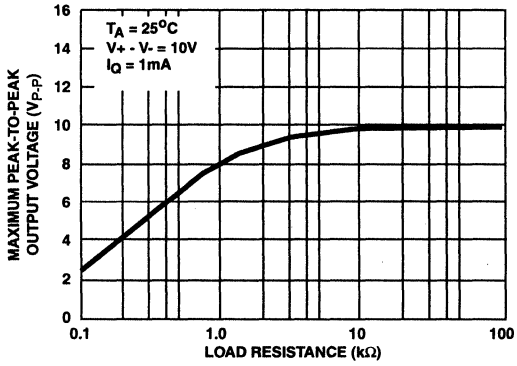


FIGURE 22. OUTPUT VOLTAGE vs LOAD RESISTANCE

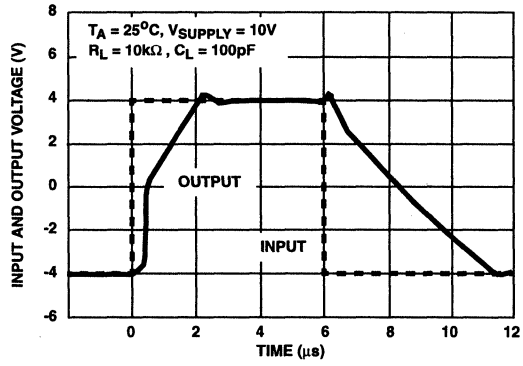


FIGURE 23. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 1mA)

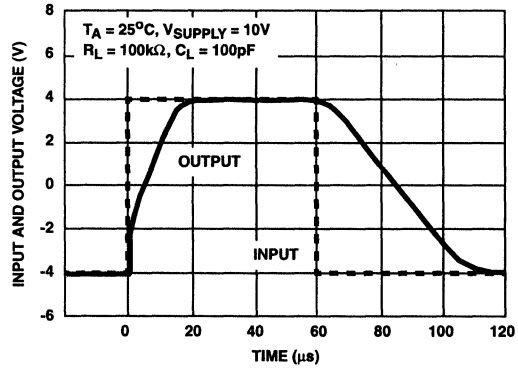


FIGURE 24. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 100µA)

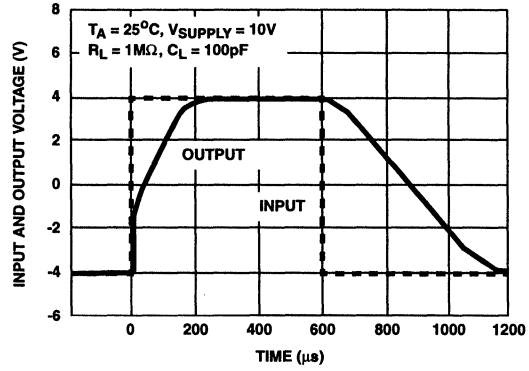


FIGURE 25. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 10µA)

HARRIS SEMICONDUCTOR

ICL7650S

2MHz, Super Chopper-Stabilized Operational Amplifier

November 1996

Features

- ***Guaranteed*** **Max Input Offset Voltage for *All* Temperature Ranges**
- **Low Long-Term and Temperature Drifts of Input Offset Voltage**
- ***Guaranteed*** **Max Input Bias Current. 10pA**
- ***Extremely Wide*** **Common Mode Voltage Range: +3.5V to -5V**
- ***Reduced*** **Supply Current. 2mA**
- ***Guaranteed*** **Minimum Output Source/Sink Current**
- **Extremely High Gain 150dB**
- **Extremely High CMRR and PSRR. 140dB**
- **High Slew Rate. 2.5V/μs**
- **Wide Bandwidth. 2MHz**
- **Unity-Gain Compensated**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use**
- **Extremely Low Chopping Spikes at Input and Output**
- **Characterized Fully *Over All* Temperature Ranges**
- ***Improved, Direct*** **Replacement for Industry-Standard ICL7650 and other Second-Source Parts**

Description

The ICL7650S Super Chopper-Stabilized Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7650 offering ***improved*** input offset voltage, ***lower*** input offset voltage temperature coefficient, ***reduced*** input bias current, and ***wider*** common mode voltage range. All improvements are highlighted in ***bold italics*** in the Electrical Characteristics section. ***Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.***

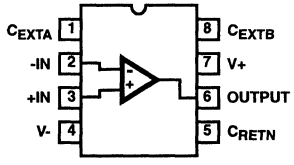
Harris' unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

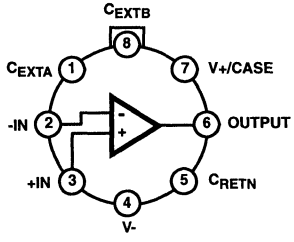
The clock oscillator and all the other control circuitry is entirely self-contained. However the 14 lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650S is internally compensated for unity-gain operation.

Pinouts (See Ordering Information on Next Page)

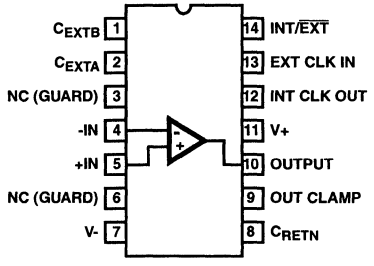
ICL7650S (PDIP, SOIC) TOP VIEW



ICL7650S (METAL CAN) TOP VIEW



ICL7650S (PDIP, CERDIP, SOIC) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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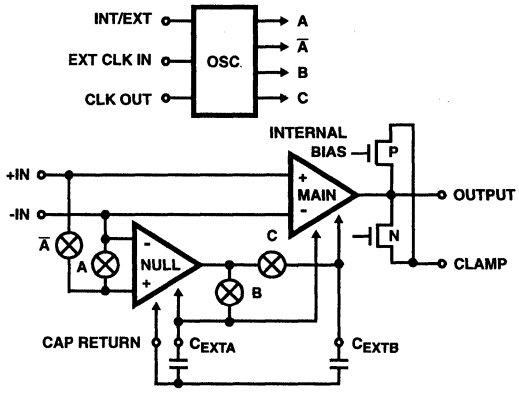
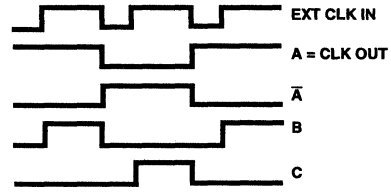
File Number **2920.2**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL7650SCPA-1	0 to 70	8 Ld PDIP	E8.3
ICL7650SCBD	0 to 70	14 Ld SOIC	M14.15
ICL7650SCPD	0 to 70	14 Ld PDIP	E14.3
ICL7650SCBA-1	0 to 70	8 Ld SOIC	M8.15
ICL7650SCTV-1	0 to 70	8 Pin Metal Can	T8.C
ICL7650SIPA-1	-25 to 85	8 Ld PDIP	E8.3
ICL7650SIPD	-25 to 85	14 Ld PDIP	E14.3
ICL7650SIJD	-25 to 85	14 Ld CERDIP	F14.3
ICL7650SITV-1	-25 to 85	8 Pin Metal Can	T8.C
ICL7650SMJD	-55 to 125	14 Ld CERDIP	F14.3
ICL7650SMTV-1	-55 to 125	8 Pin Metal Can	T8.C

Functional Diagram





Absolute Maximum Ratings

Supply Voltage (V+ to V-) 18V
Input Voltage. . . . . (V+ +0.3) to (V- -0.3)
Voltage on Oscillator Control Pins . . . . . V+ to V-
Duration of Output Short Circuit . . . . . Indefinite
Current to Any Pin 10mA
While Operating (Note 1) 100µA

Operating Conditions

Temperature Range
ICL7650SC . . . . . 0°C to 70°C
ICL7650SI . . . . . -25°C to 85°C
ICL7650SM . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Lead PDIP Package	120	N/A
14 Lead PDIP Package	80	N/A
8 Lead SOIC Package	160	N/A
14 Lead SOIC Package	120	N/A
CERDIP Package	75	20
Metal Can Package	160	75

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -55°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Limiting input current to 100µA is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±5V. See Test Circuit, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	V_{OS}		25	-	±0.7	±5	µV
			0 to 70	-	±1	±8	µV
			-25 to 85	-	±2	±10	µV
			-55 to 125	-	±4	±20	µV
Average Temperature Coefficient of Input Offset Voltage (Note 3)	$\Delta V_{OS}/\Delta T$		0 to 70	-	0.02	-	µV/°C
			-25 to 85	-	0.02	-	µV/°C
			-55 to 125	-	0.03	0.1	µV/°C
Change in Input Offset with Time	$\Delta V_{OS}/\Delta T$		25	-	100	-	$nV/\sqrt{month}$
Input Bias Current |I(+)|, |I(-)|	I_{BIAS}		25	-	4	10	pA
			0 to 70	-	5	20	pA
			-25 to 85	-	20	50	pA
			-55 to 125	-	20	50	pA
			85 to 125	-	100	500	pA
Input Offset Current |I(-), I(+)|	I_{OS}		25	-	8	20	pA
			0 to 70	-	10	40	pA
			-25 to 85	-	20	40	pA
			-55 to 125	-	20	40	pA
			85 to 125	-	20	50	pA
Input Resistance	R_{IN}		25	-	10^{12}	-	Ω
Large Signal Voltage Gain (Note 3)	A_{VOL}	R_L = 10kΩ, V_O = ±4V	25	135	150	-	dB
			0 to 70	130	-	-	dB
			-25 to 85	130	-	-	dB
			-55 to 125	120	-	-	dB
Output Voltage Swing (Note 4)	V_{OUT}	R_L = 10kΩ	25	±4.7	±4.85	-	V
		R_L = 100kΩ	25	-	±4.95	-	V
Common Mode Voltage Range (Note 3)	CMVR		25	-5	-5.2 to +4	3.5	V
			0 to 70	-5	-	3.5	V
			-25 to 85	-5	-	3.5	V
			-55 to 125	-5	-	3.5	V

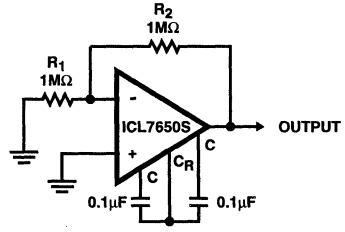
Electrical Specifications V_{SUPPLY} = ±5V. See Test Circuit, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Common Mode Rejection Ratio (Note 3)	***CMRR***	CMVR = -5V to +3.5V	25	***120***	***140***	-	dB
			0 to 70	***120***	-	-	dB
			-25 to 85	***115***	-	-	dB
			-55 to 125	***110***	-	-	dB
Power Supply Rejection Ratio	***PSRR***	V_S = ±3V to ±8V	25	120	***140***	-	dB
Input Noise Voltage	e_N	R_S = 100Ω, f = DC to 10Hz	25	-	2	-	μV_{P-P}
Input Noise Current	i_N	f = 10Hz	25	-	0.01	-	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP		25	-	2	-	MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ	25	-	2.5	-	V/µs
Rise Time	t_R		25	-	0.2	-	µs
Overshoot	OS		25	-	20	-	%
Operating Supply Range	V+ to V-		25	4.5	-	16	V
Supply Current	I_{SUPP}	No Load	25	-	2	***3***	mA
			0 to 70	-	-	***3.2***	mA
			-25 to 85	-	-	***3.5***	mA
			-55 to 125	-	-	***4***	mA
Output Source Current	$I_{O\ SOURCE}$		25	2.9	4.5	-	mA
			0 to 70	2.3	-	-	mA
			-25 to 85	2.2	-	-	mA
			-55 to 125	2	-	-	mA
Output Sink Current	$I_{O\ SINK}$		25	25	30	-	mA
			0 to 70	20	-	-	mA
			-25 to 85	19	-	-	mA
			-55 to 125	17	-	-	mA
Internal Chopping Frequency	f_{CH}	Pins 13 and 14 Open	25	120	250	375	Hz
Clamp ON Current (Note 5)		R_L = 100kΩ	25	25	70	-	µA
Clamp OFF Current (Note 5)		-4V ≤ V_{OUT} ≤ +4V	25	-	***0.001***	***5***	nA
			0 to 70	-	-	***10***	nA
			-25 to 85	-	-	***10***	nA
			-55 to 125	-	-	***15***	nA

NOTES:

3. These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.
4. OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
5. See OUTPUT CLAMP under detailed description.
6. All significant improvements over the industry-standard ICL7650 are highlighted in ***bold italics***.

Test Circuit



Application Information

Detailed Description

Amplifier

The functional diagram shows the major elements of the ICL7650S. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feed forward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650S by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650S, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null/storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN}.

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differentials are avoided, together with the consequent charge buildup on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7650S has an internal oscillator, giving a chopping frequency of 200Hz, available at the CLOCK OUT pin on the 14 pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{\text{EXT}}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50% - 80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V+ and V-. The logic threshold will be at about 2.5V below V+. Note also that a signal of about 400 Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/s, and relatively long measurements can be made with little change in offset.

Component Selection

The two required capacitors, C_{EXTA} and C_{EXTB}, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1μF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high quality film type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1μV.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

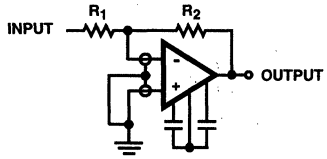


FIGURE 1A. INVERTING AMPLIFIER

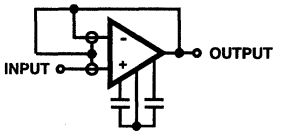
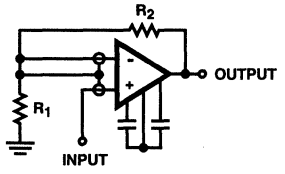


FIGURE 1B. FOLLOWER



NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ SHOULD BE LOW IMPEDANCE FOR OPTIMUM GUARDING

FIGURE 1C. NON-INVERTING AMPLIFIER

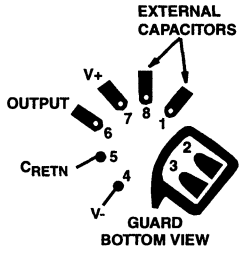


FIGURE 1D. BOARD LAYOUT FOR INPUT GUARDING WITH TO-99 PACKAGE

FIGURE 1. CONNECTION OF INPUT GUARDS

Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (PNPN) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18kΩ), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10 degrees in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of mV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-efficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650S. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-pin TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14 pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

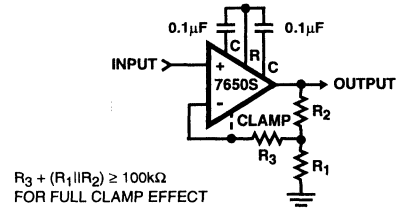
Pin Compatibility

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V+, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, µA748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650S.

Typical Applications

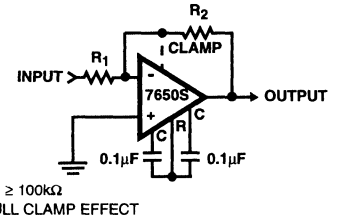
Clearly the applications of the ICL7650S will mirror those of other op-amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650S is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 2 and 3. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650S are the supply voltage (±8V Max) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 4, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650S. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.



NOTE: $R_1 \| R_2$ indicates the parallel combination of R_1 and R_2.

FIGURE 2. NON INVERTING AMPLIFIER WITH OPTIONAL CLAMP

Figure 5 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current ≈ V_{IN}/R without disturbing other portions of the system.



NOTE: $R_1 \| R_2$ indicates the parallel combination of R_1 and R_2.

FIGURE 3. INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650S to offset-null the ICL8048, as shown in Figure 6. The same concept can also be used with such devices as the HA2500 or HA2600 families of op-amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

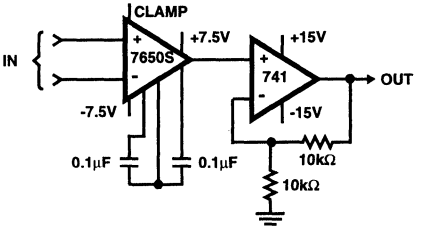


FIGURE 4. USING 741 TO BOOST OUTPUT DRIVE CAPACITY

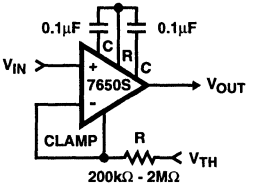
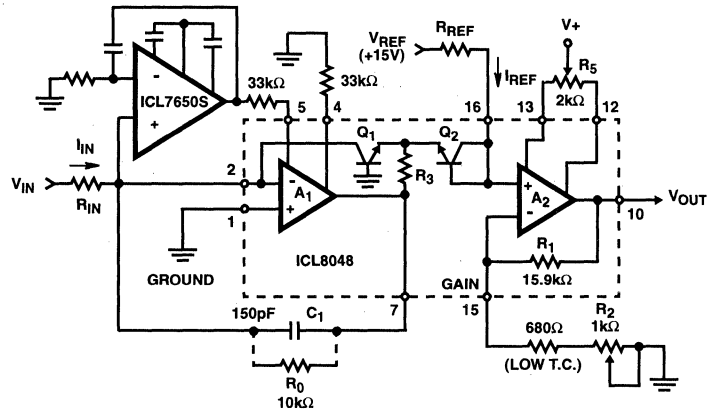


FIGURE 5. LOW OFFSET COMPARATOR



NOTE: For further Applications Assistance, see A053 and R017.

FIGURE 6. ICL8048 OFFSET NULLED BY ICL7650S

Typical Performance Curves

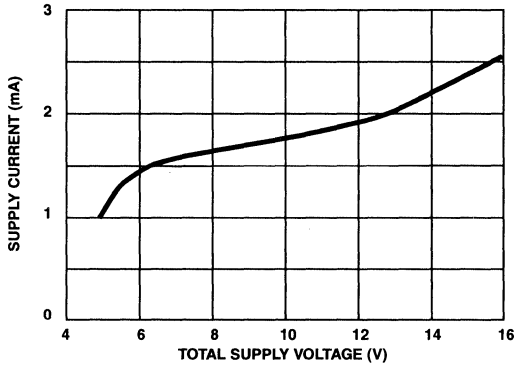


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

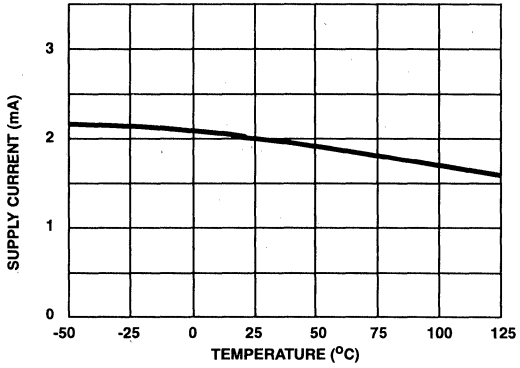


FIGURE 8. SUPPLY CURRENT vs AMBIENT TEMPERATURE

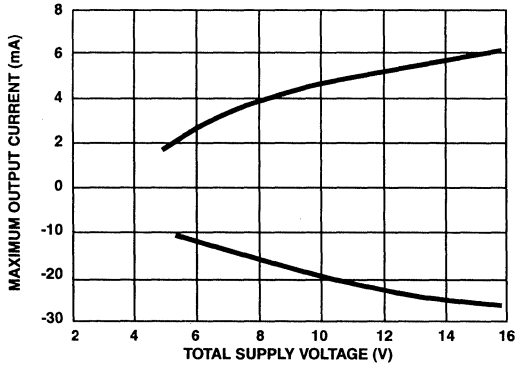


FIGURE 9. MAXIMUM OUTPUT CURRENT vs SUPPLY VOLTAGE

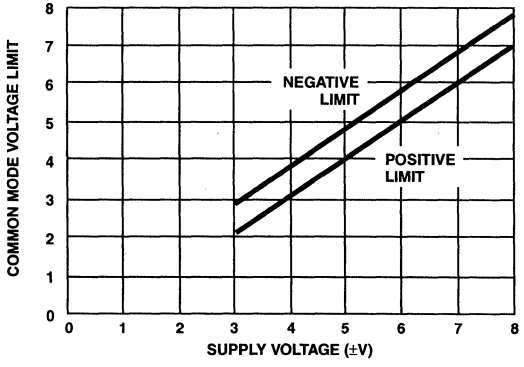


FIGURE 10. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

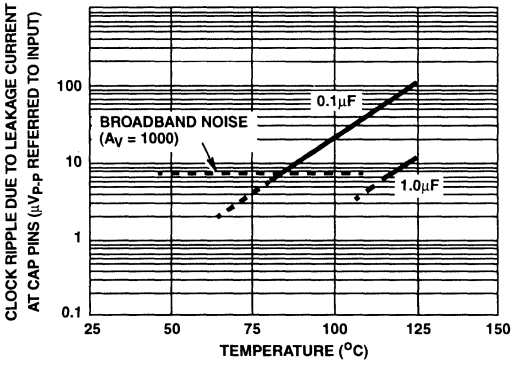


FIGURE 11. CLOCK RIPPLE REFERRED TO THE INPUT vs TEMPERATURE

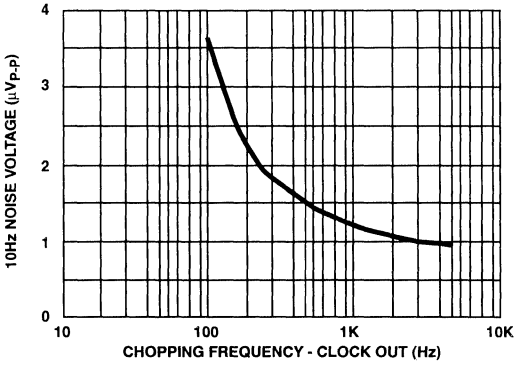


FIGURE 12. 10Hz NOISE VOLTAGE vs CHOPPING FREQUENCY

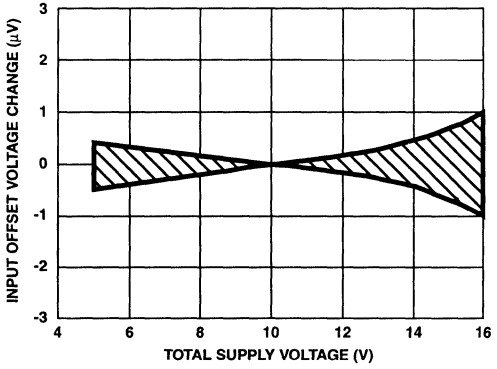


FIGURE 13. INPUT OFFSET VOLTAGE CHANGE vs SUPPLY VOLTAGE

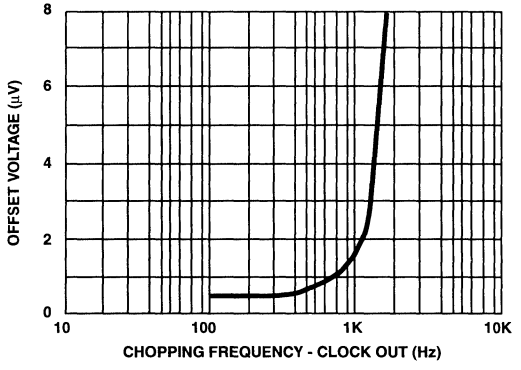


FIGURE 14. INPUT OFFSET VOLTAGE vs CHOPPING FREQUENCY

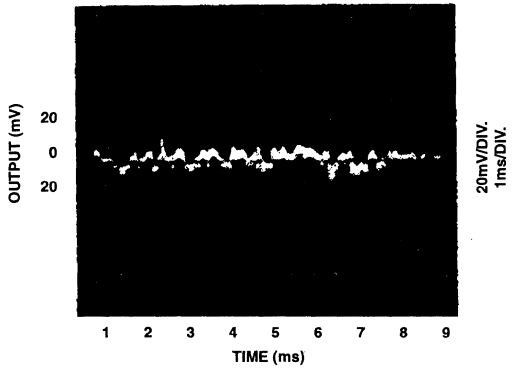


FIGURE 15. OUTPUT WITH ZERO INPUT; GAIN = 1000; BALANCED SOURCE IMPEDANCE = 10kΩ

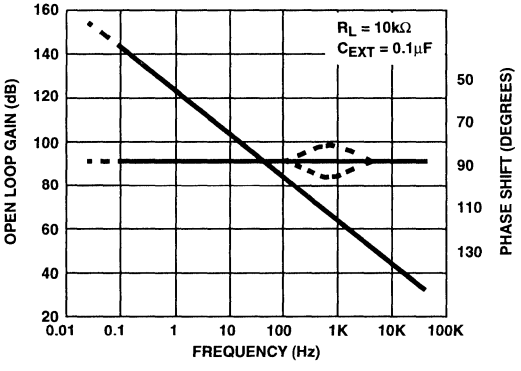


FIGURE 16. OPEN LOOP GAIN AND PHASE SHIFT vs FREQUENCY

Typical Performance Curves (Continued)

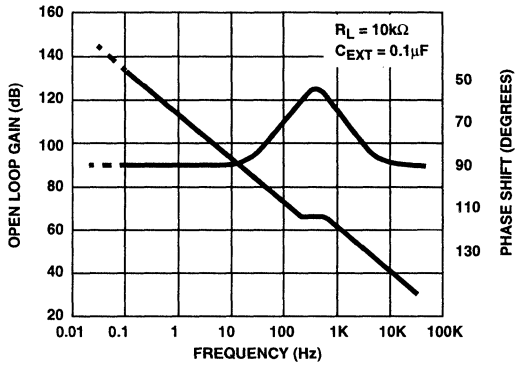
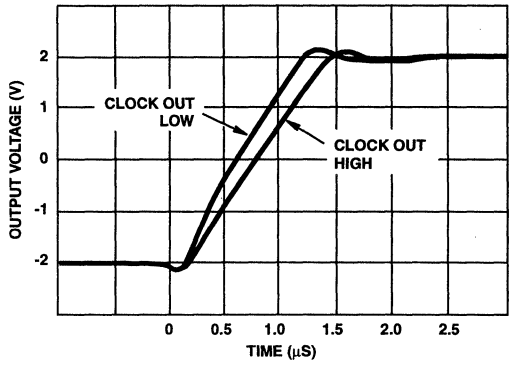
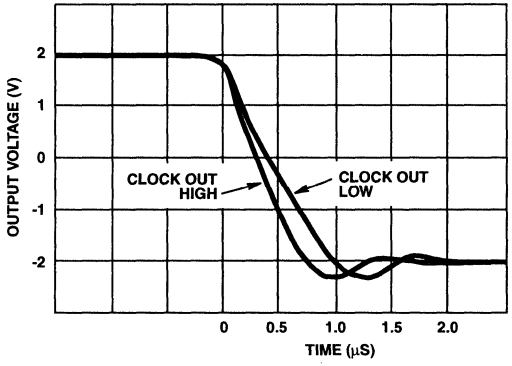


FIGURE 17. OPEN LOOP GAIN AND PHASE SHIFT vs FREQUENCY



NOTE: The two different responses correspond to the two phases of the clock.

FIGURE 18. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (NOTE)



NOTE: The two different responses correspond to the two phases of the clock.

FIGURE 19. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (NOTE)

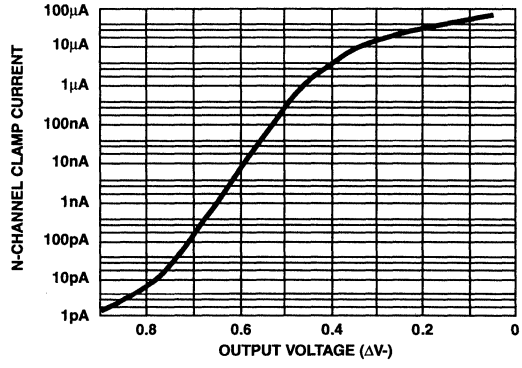


FIGURE 20. N-CHANNEL CLAMP CURRENT vs OUTPUT VOLTAGE

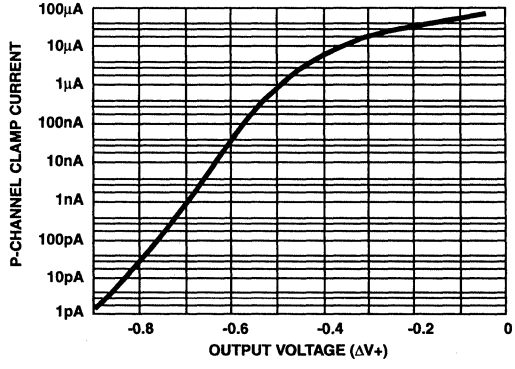


FIGURE 21. P-CHANNEL CLAMP CURRENT vs OUTPUT VOLTAGE

Operational Amplifiers Glossary of Terms

AVERAGE INPUT OFFSET CURRENT DRIFT - The average change in offset current between room (25°C) and high temperature (125°C, 85°C or 75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

AVERAGE OFFSET VOLTAGE DRIFT - The average change in offset voltage between room (25°C) and high temperature (125°C, 85°C or 75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

CHANNEL SEPARATION - The ratio of the output of a driven amplifier to the output (referred to input) of an adjacent undriven amplifier.

COMMON MODE INPUT VOLTAGE (V_{IC}) - The average of the voltages present at the differential input terminals.

COMMON MODE INPUT VOLTAGE RANGE (V_{ICR}) - The range of voltage that if exceeded at either input terminal will cause the amplifier to cease operating properly.

COMMON MODE REJECTION RATIO (CMRR) - The ratio of change in input offset voltage to change in input common mode voltage, expressed in dB.

$$CMRR = 20 \times \log_{10}\left[\frac{V_{IO}}{V_{CM}}\right]$$

COMMON MODE RESISTANCE (r_{IC}) - The ratio of change in input common mode voltage to the resulting change in input current.

DIFFERENTIAL INPUT RESISTANCE (r_{ID}) - The ratio of change in input differential voltage (small signal, assumes amplifier operating linearly) to the resulting change in differential input current.

FULL POWER BANDWIDTH (FPBW) - The maximum frequency at which a full scale undistorted (THD < 1%) sine wave can be obtained at the output of the amplifier.

GAIN BANDWIDTH PRODUCT (GBWP) - The open loop gain of an op amp (in V/V) at a mid-band, linear region frequency (usually between 1kHz and 10kHz) times that frequency (in Hz). GBWP = $[A_{VOL}] \bullet f$.

INPUT BIAS CURRENT (I_{BIAS}) - The average of the currents flowing into or out of the input terminals when the output is at zero volts.

INPUT CAPACITANCE (C_{IN}) - The equivalent capacitance seen looking into either input terminal.

INPUT NOISE CURRENT (i_N) - The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

INPUT OFFSET CURRENT (I_{OS}) - The difference in the currents flowing into the two input terminals when the output is at zero volts.

INPUT OFFSET VOLTAGE (V_{IO}) - The differential DC voltage required to zero the output voltage with no input signal or load. Input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT NOISE VOLTAGE (e_N) - The input noise voltage that would reproduce the noise seen at the output if all the amplifier noise sources and source resistances were set to zero.

LARGE SIGNAL VOLTAGE GAIN (A_V) - The ratio of the peak to peak output voltage swing (over a specified range) to the change in input voltage required to drive the output.

OUTPUT CURRENT (I_{OUT}) - The output current available from the amplifier at some specified output voltage.

OUTPUT RESISTANCE (R_O) - The ratio of the change in output voltage to the change in output current.

OUTPUT SHORT CIRCUIT CURRENT (I_{SC}) - The output current available from the amplifier with the output shorted to ground (or other specified potential).

OUTPUT VOLTAGE SWING (V_{OUT}) - The maximum output voltage swing, referred to ground, that can be obtained under specified loading conditions.

OVERSHOOT - Peak excursion above final value of an output step response.

POWER SUPPLY REJECTION RATIO (PSRR) - The ratio of the change in input offset voltage to the change in power supply voltage producing it.

RISE TIME (t_R) - The time required for an output voltage step to change from 10% to 90% of its final value, when the input is subjected to a small signal voltage pulse.

SETTLING TIME (t_{SET}) - The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE (SR) - The rate of change of the output under large signal conditions. Slew rate may be specified separately for both positive and negative going changes.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the amplifier with no load and the output at zero volts.

SUPPLY VOLTAGE RANGE - The range of power supply voltage over which the amplifier may be safely operated.

UNITY GAIN BANDWIDTH - The frequency range from DC to that frequency where the amplifier's open loop gain is unity.

LINEAR 4

COMPARATORS

Selection Guide

COMPARATORS: Electrical Characteristics, $T_A = 25^oC$

TYPE	V_{IO} MAX (mV)	INPUT CURRENT MAX (nA)	SUPPLY CURRENT MAX (mA)	SUPPLY VOLTAGE RANGE V+, V- TYP (V)	A_{OL} MIN (dB)	RESPONSE TIME TYP (ns)	(NOTE 1) LEAD COUNT AND PACKAGE TYPE	COMMENTS
DUAL UNIT TYPES								
CA3290	20	50pA	3	+5, 0 to +18, -18	88	t_R = 1200 t_F = 200	8PDIP, 8Can	Low Cost
CA3290A	10	40pA	3	+5, 0 to +18, -18	88		8PDIP, 14PDIP, 8Can	
QUAD UNIT TYPES								
CA139	5	100	8	+2.5, 0 to +18, -18	-	t_R = 1300 t_F = 750	14PDIP, 14CERDIP, 14SOIC	Mil Temp Range
CA139A	2	100	8	+2.5, 0 to +18, -18	94		14PDIP, 14SOIC	Mil Temp Range
CA239	5	250	2	+2.5, 0 to +18, -18	-		14PDIP, 14CERDIP, 14SOIC	Ind Temp Range
CA239A	2	250	2	+2.5, 0 to +18, -18	94		14PDIP, 14CERDIP, 14SOIC	Ind Temp Range
CA339	5	250	2	+2.5, 0 to +18, -18	-		14PDIP, 14SOIC	Low Cost
CA339A	2	250	2	+2.5, 0 to +18, -18	94		14PDIP, 14SOIC	
LM339	5	250	2	+2.5, 0 to +18, -18	-		14PDIP	Low Cost
LM339A	2	250	2	+2.5, 0 to +18, -18	94		14PDIP	
LM2901	7	250	2	+2.5, 0 to +18, -18	-		14SOIC, 14PDIP	Low Cost, Ind Temp
LM3302	20	500	2	+2.5, 0 to +18, -18	-		14SOIC, 14PDIP	Low Cost, Ind Temp
HA-4900	2	75	+20, -8, +4 (Note 2)	+5, 0 to +16.5, -16.5	112	130	16CERDIP	Single or Dual Supply. Analog and Logic Supplies Separated for Easier Interface and Noise Immunity
HA-4902	2	150	+20, -8, +4 (Note 2)	+5, 0 to +16.5, -16.5	112	130	16CERDIP	
HA-4905	4	150	+20, -8, +4 (Note 2)	+5, 0 to +16.5, -16.5	112	130	16PDIP, 16CERDIP, 16SOIC (300 mil), 20PLCC	

NOTE:

1. See Linear Package Selection Guide in Section 11.
2. Positive Supply Current, Negative Supply Current, Logic Supply Current.

HARRIS SEMICONDUCTOR

CA139, CA139A, CA239, CA239A, CA339, CA339A, LM339, LM339A, LM2901, LM3302

Quad Voltage Comparators for Industrial, Commercial and Military Applications

November 1996

Features

- Operation from Single or Dual Supplies
- Common Mode Input Voltage Range to GND
- Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS
- Differential Input Voltage Range Equal to the Supply Voltage
- Maximum Input Offset Voltage (V_{IO})
  - CA139A, CA239A, CA339A 2mV
  - CA139, CA239, CA339 ..... 5mV
  - LM2901 ..... 7mV
  - LM3302 ..... 20mV
- Replacement for Industry Types 139, 239, 339, 139A, 239A, 339A, 2901, 3302

Applications

- Square Wave Generator
- Time Delay Generators
- Pulse Generators
- Multivibrators
- High Voltage Digital Logic Gates
- A/D Converters
- MOS Clock Timers

Description

The devices in this series consist of four independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground even when operated from a single supply, and the low power supply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and CMOS.

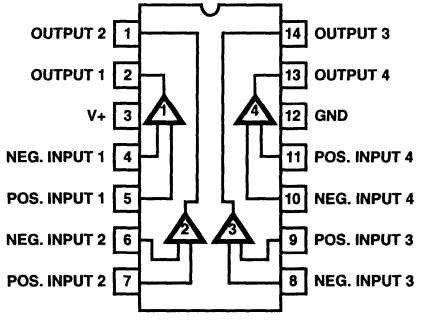
Types CA139A, CA239A, and CA339A have all the features and characteristics of their prototype counterparts CA139, CA239, and CA339 plus an even lower input offset voltage characteristic. All the SOIC parts are available on tape and reel. Replace the M suffix in the part number with M96 when ordering (e.g. CA0339AM96). The CA339 is also available in chip form (H suffix).

Ordering Information

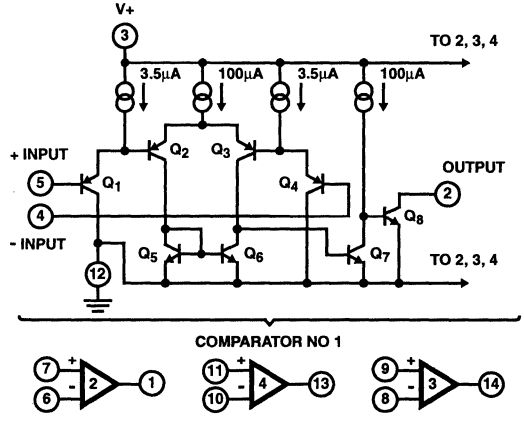
PART NO. (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA0139E	-55 to 125	14 Ld PDIP	E14.3
CA0139F	-55 to 125	14 Ld CERDIP	E14.3
CA0139M, AM (139, 139A)	-55 to 125	14 Ld SOIC	M14.15
CA0239E, AE	-25 to 85	14 Ld PDIP	E14.3
CA0239F, AF	-25 to 85	14 Ld CERDIP	E14.3
CA0239M, (239)	-25 to 85	14 Ld SOIC	M14.15
CA0339E, AE	0 to 70	14 Ld PDIP	E14.3
CA0339M, (339)	0 to 70	14 Ld SOIC	M14.15
LM339N, AN	0 to 70	14 Ld PDIP	E14.3
LM2901M (2901)	-40 to 85	14 Ld SOIC	M14.15
LM2901N	-40 to 85	14 Ld PDIP	E14.3
LM3302M (3302)	-40 to 85	14 Ld SOIC	M14.15
LM3302N	-40 to 85	14 Ld PDIP	E14.3

Pinout

CA139, CA239, CA239A (PDIP, CERDIP, SOIC)
CA139A, CA339, CA339A, LM2901, LM3302 (PDIP, SOIC)
LM339, LM339A (PDIP)
TOP VIEW



Schematic Diagram



4 COMPARATORS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **795.3**

Absolute Maximum Ratings

Supply Voltage . . . . . 36V or ±18V
Differential Input Voltage. 36V
Input Voltage. . . . . -0.3V to +36V
Input Current (V_I < -0.3V, Note 1). 50mA
Output Short Circuit Duration (Single Supply, Note 2) . . Continuous

Operating Conditions

Temperature Range
CA139, CA139A . . . . . -55°C to 125°C
CA239, CA239A . . . . . -25°C to 80°C
CA339, CA339A, LM339, LM339A . . . . . 0°C to 70°C
LM2901, LM3302 . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	90	30
PDIP Package	100	N/A
SOIC Package	175	N/A

Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s). . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Inputs must not go more negative than -0.3V.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current independent of V+ is approximately 20mA.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V+ = 5V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	CA139			CA139A			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_{REF} = 1.4V, R_S = 0, Output Switch Point V ≅ 1.4V	T_A = 25	-	2	5	-	1	2	mV
			Note 4	-	-	9	-	-	4	mV
Differential Input Voltage	V_{ID}	Keep All Inputs ≥0V, or V- (if used), (Note 5)	Note 4	-	-	36	-	-	36	V
Saturation Voltage	V_{SAT}	V_I- = 1V, V_I+ = 0V, I_{SINK} ≤ 4mA	T_A = 25	-	250	400	-	250	400	mV
			Note 4	-	-	700	-	-	700	mV
Common Mode Input Voltage Range	V_{ICR}	Note 6	T_A = 25	0	-	V+ -1.5	0	-	V+ -1.5	V
			Note 4	0	-	V+ -2	0	-	V+ -2	V
Input Offset Current	I_{IO}	I_I+ - I_I-	T_A = 25	-	3	25	-	3	25	nA
			Note 4	-	-	100	-	-	100	nA
Input Bias Current	I_{IB}	I_I+ or I_I- with Output in Linear Range	T_A = 25	-	25	100	-	25	100	nA
			Note 4	-	-	300	-	-	300	nA
Total Supply Current	I+	R_L = ∞ On All Comparators	T_A = 25	-	0.8	2	-	0.8	2	mA
Output Leakage Current		V_I+ ≥ 1V, V_I- = 0V, V_O = 5V	T_A = 25	-	0.1	-	-	0.1	-	nA
		V_I+ ≥ 1V, V_I- = 0V, V_O = 30V	Note 4	-	-	1	-	-	1	µA
Output Sink Current		V_I- ≥ 1V, V_I+ = 0V, V_O ≤ 1.5V	T_A = 25	6	16	-	6	16	-	mA
Voltage Gain	A_{OL}	R_L ≥ 15kΩ, V+ = 15V	T_A = 25	-	200	-	50	200	-	V/mV

Electrical Specifications V+ = 5V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	CA139			CA139A			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Response Time		V_I = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ	T_A = 25	-	300	-	-	300	-	ns
Response Time (Figures 3, 4)		V_{RL} = 5V, R_L = 5.1kΩ	T_A = 25	-	1.3	-	-	1.3	-	µs

Electrical Specifications V+ = 5V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	CA239, CA339, LM339			CA239A, CA339A, LM339A			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_{REF} = 1.4V, R_S = 0, Output Switch Point V ≅ 1.4V	T_A = 25	-	2	5	-	1	2	mV
			Note 4	-	-	9	-	-	4	mV
Differential Input Voltage	V_{ID}	Keep All Inputs ≥ 0V, or V- (if used), (Note 5)	Note 4	-	-	36	-	-	36	V
Saturation Voltage	V_{SAT}	V_I- = 1V, V_I+ = 0V, I_{SINK} ≤ 4mA	T_A = 25	-	250	400	-	250	400	mV
			Note 4	-	-	700	-	-	700	mV
Common Mode Input Voltage Range	V_{ICR}	Note 6	T_A = 25	0	-	V+ -1.5	0	-	V+ -1.5	V
			Note 4	0	-	V+ - 2	0	-	V+ -2	V
Input Offset Current	I_{IO}	I_I+ - I_I-	T_A = 25	-	5	50	-	5	50	nA
			Note 4	-	-	150	-	-	150	nA
Input Bias Current	I_{IB}	I_I+ or I_I- with Output in Linear Range	T_A = 25	-	25	250	-	25	250	nA
			Note 4	-	-	400	-	-	400	nA
Total Supply Current	I+	R_L = ∞ on All Comparators	T_A = 25	-	0.8	2	-	0.8	2	mA
Output Leakage Current		V_I+ ≥ 1V, V_I- = 0V, V_O = 5V	T_A = 25	-	0.1	-	-	0.1	-	nA
		V_I+ ≥ 1V, V_I- = 0V, V_O = 30V	Note 4	-	-	1	-	-	1	µA
Output Sink Current		V_I- ≥ 1V, V_I+ = 0V, V_O ≤ 1.5V	T_A = 25	6	16	-	6	16	-	mA
Voltage Gain	A_{OL}	R_L ≥ 15kΩ, V+ = 15V	T_A = 25	50	200	-	50	200	-	V/mV
Large Signal Response Time		V_I = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ	T_A = 25	-	300	-	-	300	-	ns
Response Time (Figures 3, 4)		V_{RL} = 5V, R_L = 5.1kΩ	T_A = 25	-	1.3	-	-	1.3	-	µs

NOTES:

4. Ambient Temperature (T_A) applicable over operating temperature range as shown below. CA139, CA139A = -55°C to 125°C; CA239, CA239A = -25°C to 85°C; CA339, CA339A, LM339, LM339A = 0°C to 70°C; LM2901, LM3302 = -40°C to 85°C.
5. The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common mode voltage range. The low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
6. The upper end of the common mode voltage range is (V+) - 1.5V, but either or both inputs can go to +30V without damage.

Electrical Specifications V+ = 5V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	LM2901			LM3302			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_{REF} = 1.4V, R_S = 0, Output Switch Point V ≅ 1.4V	T_A = 25	-	2	7	-	1	20	mV
			Note 4	-	-	15	-	-	40	mV
Differential Input Voltage	V_{ID}	Keep All Inputs ≥ 0V, or V- (if used), (Note 5)	Note 4	-	-	36	-	-	28	V
Saturation Voltage	V_{SAT}	V_{I}- = 1V, V_{I}+ = 0V, I_{SINK} ≤ 4mA	T_A = 25	-	250	400	-	250	500	mV
			Note 4	-	-	700	-	-	700	mV
Common Mode Input Voltage Range	V_{ICR}	Note 6	T_A = 25	0	-	V+ - 1.5	0	-	V+ -1.5	V
			Note 4	0	-	V+ - 2	0	-	V+ -2	V
Input Offset Current	I_{IO}	I_{I}+ - I_{I}-	T_A = 25	-	5	50	-	3	100	nA
			Note 4	-	-	200	-	-	300	nA
Input Bias Current	I_{IB}	I_{I}+ or I_{I}- with Output in Linear Range	T_A = 25	-	25	250	-	25	500	nA
			Note 4	-	-	500	-	-	1000	nA
Total Supply Current	I+	R_L = ∞ on All Comparators	T_A = 25	-	0.8	2	-	0.8	2	mA
Output Leakage Current		V_{I}+ ≥ 1V, V_{I}- = 0V, V_O = 5V	T_A = 25	-	0.1	-	-	0.1	-	nA
		V_{I}+ ≥ 1V, V_{I}- = 0V, V_O = 30V	Note 4	-	-	1	-	-	1	µA
Output Sink Current		V_{I}- ≥ 1V, V_{I}+ = 0V, V_O ≤ 1.5V	T_A = 25	6	16	-	6	16	-	mA
Voltage Gain	A_{OL}	R_L ≥ 15kΩ, V+ = 15V	T_A = 25	25	100	-	2	30	-	V/mV
Large Signal Response Time		V_I = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ	T_A = 25	-	300	-	-	300	-	ns
Response Time (Figures 3, 4)		V_{RL} = 5V, R_L = 5.1kΩ	T_A = 25	-	1.3	-	-	1.3	-	µs

Typical Performance Curves

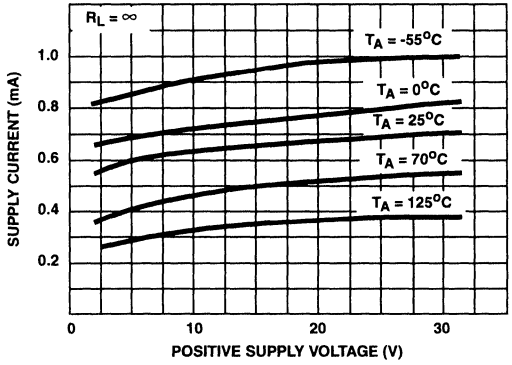


FIGURE 1. SUPPLY CURRENT vs SUPPLY VOLTAGE

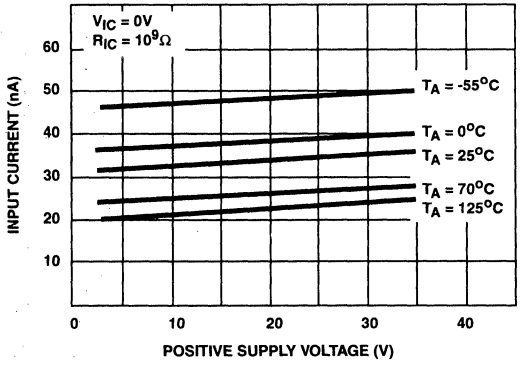


FIGURE 2. INPUT CURRENT vs SUPPLY VOLTAGE

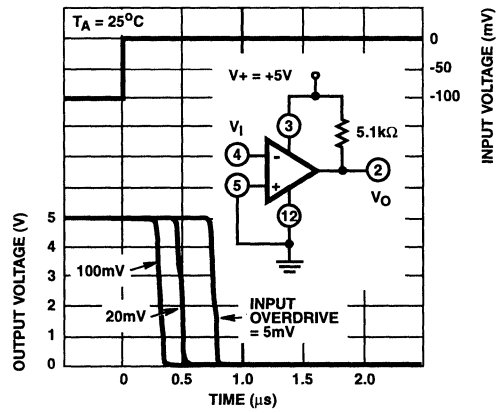


FIGURE 3. RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - NEGATIVE TRANSITION

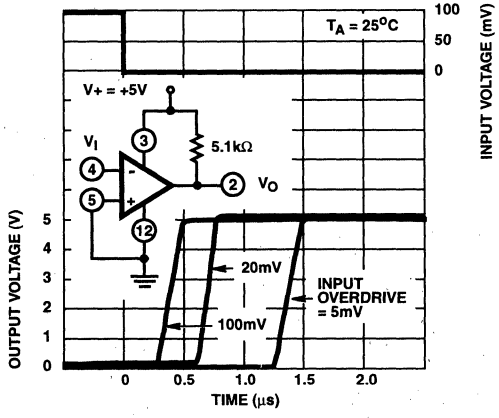


FIGURE 4. RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES - POSITIVE TRANSITION

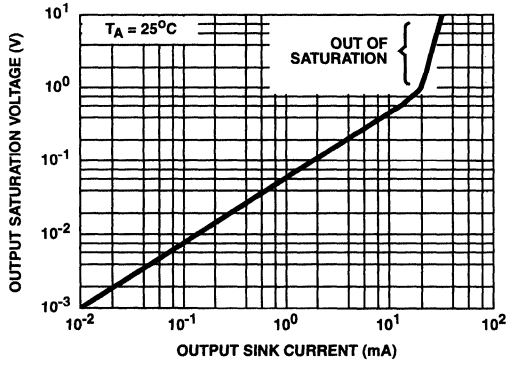
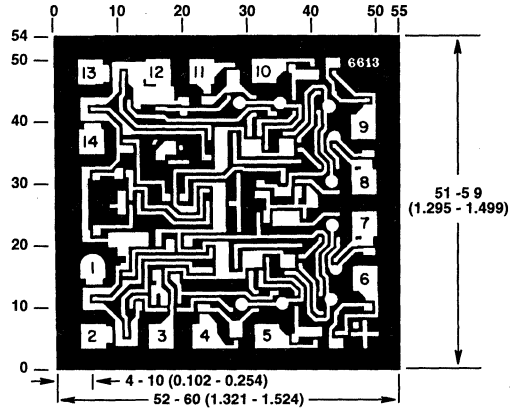


FIGURE 5. OUTPUT SATURATION VOLTAGE vs OUTPUT SINK CURRENT

Metallization Mask Layout



NOTE: Dimensions in parentheses are in mm and are derived from the basic in. dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HARRIS SEMICONDUCTOR

CA3098

Programmable Schmitt Trigger with Memory, Dual Input Precision Level Detector

November 1996

Features

- Programmable Operating Current
- Micropower Standby Dissipation
- Direct Control of Currents Up to 150mA
- Low Input On/Off Current of Less Than 1nA for Programmable Bias Current of 1μA
- Built-in Hysteresis ..... 20mV (Max)

Applications

- Control of Relays, Heaters, LEDs, Lamps, Photosensitive Devices, Thyristors, Solenoids, etc.
- Signal Reconditioning
- Phase and Frequency Modulators
- On/Off Motor Switching
- Schmitt Triggers, Level Detectors
- Time Delays
- Overvoltage, Overcurrent, Overtemperature Protection
- Battery-Operated Equipment
- Square and Triangular-Wave Generators

Ordering Information

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. NO.
CA3098E	-55 to 125	8 Ld PDIP	E8.3

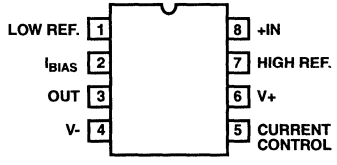
Description

The CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high operating current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16V, or a dual power supply with maximum operating voltage of ±8V. It can directly control currents up to 150mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30mA. The CA3098 contains the following major circuit function features (see Block Diagram):

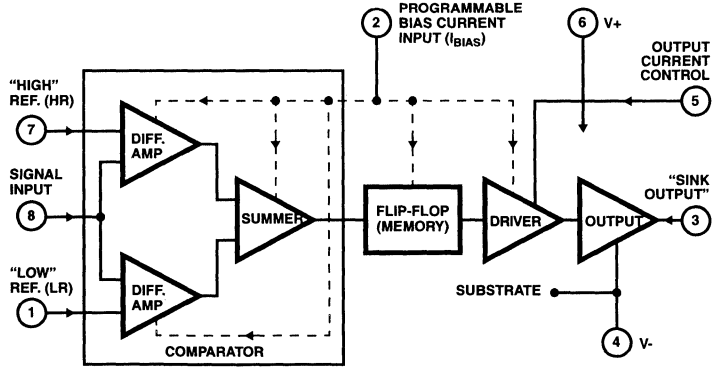
1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and output stages: these stages permit the circuit to "sink" maximum peak load currents up to 150mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

Pinout

CA3098
(PDIP)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 896.3

CA3290, CA3290A

BiMOS Dual Voltage Comparators with MOSFET Input, Bipolar Output

November 1996

Features

- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}). . . . . 1.7TΩ (Typ)
  - Very Low Input Current at V+ = 5V . . . . . 3.5pA (Typ)
  - Wide Common Mode Input Voltage Range (V_{ICR}) Can Be Swung 1.5V (Typ) Below Negative Supply Voltage Rail
  - Virtually Eliminates Errors Due to Flow of Input Currents
- Output Voltage Compatible with TTL, DTL, ECL, MOS, and CMOS Logic Systems in Most Applications

Applications

- High Source Impedance Voltage Comparators
- Long Time Delay Circuits
- Square Wave Generators
- A/D Converters
- Window Comparators

Description

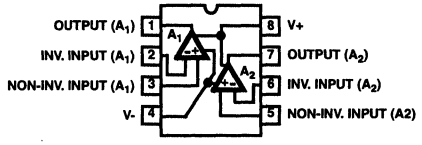
The CA3290A and CA3290 types consist of a dual voltage comparator on a single monolithic chip. The common mode input voltage range includes ground even when operated from a single supply. The low supply current drain makes these comparators suitable for battery operation; their extremely low input currents allow their use in applications that employ sensors with extremely high source impedances. Package options are shown in the table below.

Ordering Information

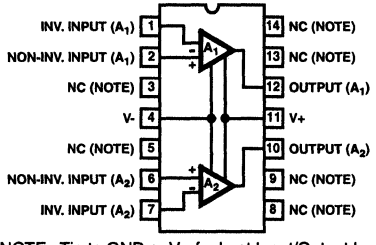
PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. NO.
CA3290AE	-55 to 125	8 Ld PDIP	E8.3
CA3290AE1	-55 to 125	14 Ld PDIP	E14.3
CA3290AT	-55 to 125	8 Pin Metal Can	T8.C
CA3290E	-55 to 125	8 Ld PDIP	E8.3
CA3290T	-55 to 125	8 Pin Metal Can	T8.C

Pinouts

CA3290/A (PDIP)
TOP VIEW

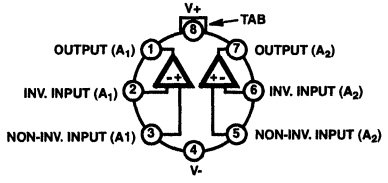


CA3290A (PDIP)
TOP VIEW



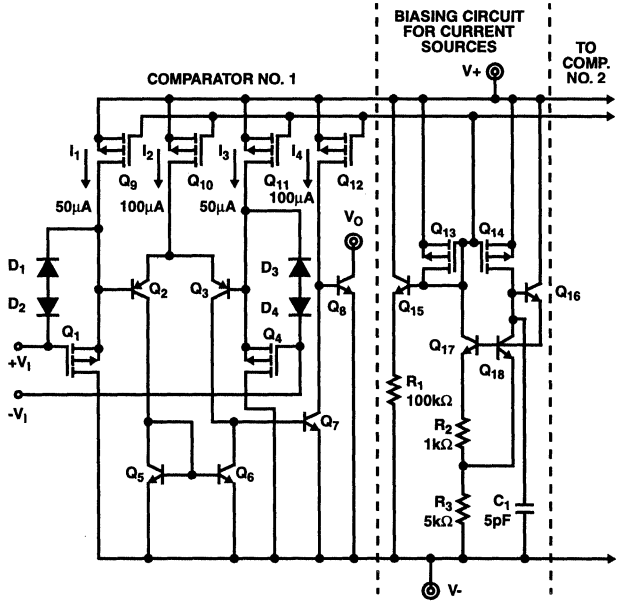
NOTE: Tie to GND or V+ for best Input/Output Isolation.

CA3290A, CA3290 (METAL CAN)
TOP VIEW



Schematic Diagram

(ONLY ONE IS SHOWN)



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1049.2**

Absolute Maximum Ratings

Supply Voltage
- Single Supply ..... +36V
- Dual Supply ..... ±18V

Differential Input Voltage ..... 36V or [(V+ - V-) +5V] (whichever is less)
DC Input Voltage ..... V+ +5V to V- -5V
Output to V- Short Circuit Duration (Note 1) ..... Continuous
Input Current 1mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Lead PDIP Package	100	N/A
8 Lead PDIP Package	120	N/A
8 Pin Metal Can Package	155	67

Maximum Junction Temperature (Can) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C

Operating Conditions

Temperature Range ..... -55 to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuits from the output to V+ can cause excessive heating and eventual destruction of the device.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

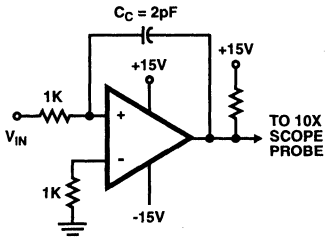
V- = 0V, Unless Otherwise Specified

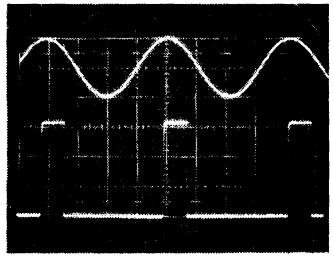
PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	CA3290A			CA3290			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	$V_{CM} = V_O = 1.4V$, $V+ = 5V$	Full	-	4.5	-	-	8.5	-	mV
		$V_{CM} = V_O = 0V$, $V+ = +15V$, $V- = -15V$	Full	-	8.5	-	-	8.5	-	mV
		$V_{CM} = V_O = 1.4V$, $V+ = 5V$	25	-	4.0	10	-	7.5	20	mV
		$V_{CM} = V_O = 0V$, $V+ = +15V$, $V- = -15V$	25	-	4.0	10	-	7.5	20	mV
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$			-	8	-	-	8	-	µV/°C
Input Offset Current	I_{IO}	$V_{CM} = 1.4V$, $V+ = 5V$	Full	-	2	28	-	2	32	nA
		$V_{CM} = 0V$, $V+ = +15V$, $V- = -15V$	Full	-	7	28	-	7	32	nA
		$V_{CM} = 1.4V$, $V+ = 5V$	25	-	2	25	-	2	30	pA
		$V_{CM} = 0V$, $V+ = +15V$, $V- = -15V$	25	-	7	25	-	7	30	pA
Input Current	I_I	$V_{CM} = 1.4V$, $V+ = 5V$	125	-	2.8	45	-	2.8	55	nA
		$V_{CM} = 0V$, $V+ = +15V$, $V- = -15V$	125	-	13	45	-	13	55	nA
		$V_{CM} = 1.4V$, $V+ = 5V$	25	-	3.5	40	-	3.5	50	pA
		$V_{CM} = 0V$, $V+ = +15V$, $V- = -15V$	25	-	12	40	-	12	50	pA

Electrical Specifications V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	CA3290A			CA3290			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I+	$R_L = \infty$, V+ = 5V	-55	-	0.85	1.0	-	0.85	1.6	mA
		$R_L = \infty$, V+ = 30V	-55	-	1.62	3.0	-	1.62	3.5	mA
		$R_L = \infty$, V+ = 5V	25	-	0.8	1.4	-	0.8	1.4	mA
		$R_L = \infty$, V+ = 30V	25	-	1.35	3.0	-	1.35	3.0	mA
Voltage Gain	A_{OL}	R_L = 15kΩ, V+ = +15V, V- = -15V	Full	-	150	-	-	150	-	V/mV
				-	103	-	-	103	-	dB
		R_L = 15kΩ, V+ = +15V, V- = -15V	25	25	800	-	25	800	-	V/mV
				88	118	-	88	118	-	dB
Saturation Voltage	V_{SAT}	I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	125	-	0.22	0.7	-	0.22	0.7	V
		I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	-55	-	0.1	-	-	0.1	-	V
		I_{SINK} = 4mA, V+ = 5V, $+V_I$ = 0V, $-V_I$ = 1V	25	-	0.12	0.4	-	0.12	0.4	V
Output Leakage Current	I_{OL}	V+ = 15V	Full	-	65	-	-	65	-	nA
		V+ = 36V	Full	-	130	1k	-	130	1k	nA
		V+ = 15V	25	-	100	-	-	100	-	pA
		V+ = 36V	25	-	500	-	-	500	-	pA
Common Mode Input Voltage Range	V_{ICR}	V_O = 1.4V, V+ = 5V	25	V+-3.5 V-	V+-3.1 V- -1.5	-	V+-3.5 V-	V+-3.1 V- -1.5	-	V
		V_O = 0V, V+ = +15V, V- = -15V	25	V+-3.8 V-	V+-3.4 V- -1.6	-	V+-3.8 V-	V+-3.4 V- -1.6	-	V
Common Mode Rejection Ratio	CMRR	V+ = +15V, V- = -15V	25	-	44	562	-	44	562	µV/V
		V+ = 5V	25	-	100	562	-	100	562	µV/V
Power Supply Rejection Ratio	PSRR	V+ = +15V, V- = -15V	25	-	15	316	-	15	316	µV/V
Output Sink Current		V_O = 1.4V, V+ = 5V	25	6	30	-	6	30	-	mA
Response Time Rising Edge	t_r	R_L = 5.1kΩ, V+ = 15V	25	-	1.2	-	-	1.2	-	µs
Response Time Falling Edge	t_f	R_L = 5.1kΩ, V+ = 15V	25	-	200	-	-	200	-	ns
Large Signal Response Time		R_L = 5.1kΩ, V+ = 15V	25	-	500	-	-	500	-	ns
		R_L = 5.1kΩ, V+ = 5V	25	-	400	-	-	400	-	ns

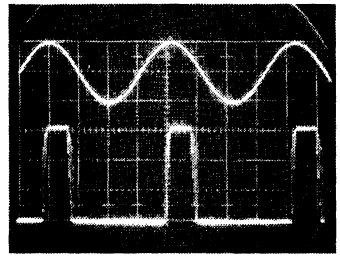
Test Circuits and Waveforms





WITH C_C

Top Trace ≈ 4.5mV/Div. = V_{IN}
Bottom Trace = 10V/Div. = V_{OUT}
Time Scale = 5µs/Div.



WITHOUT C_C

Top Trace ≈ 4.5mV/Div.
Bottom Trace = 10V/Div.
Time Scale = 5µs/Div.

FIGURE 1. PARASITIC OSCILLATIONS TEST CIRCUIT AND WAVEFORMS

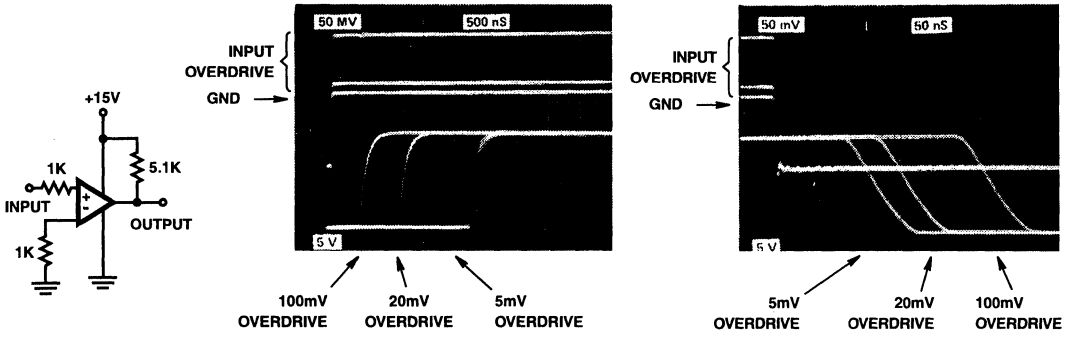


FIGURE 2. NON-INVERTING COMPARATOR RESPONSE TIME TEST CIRCUIT AND WAVEFORMS

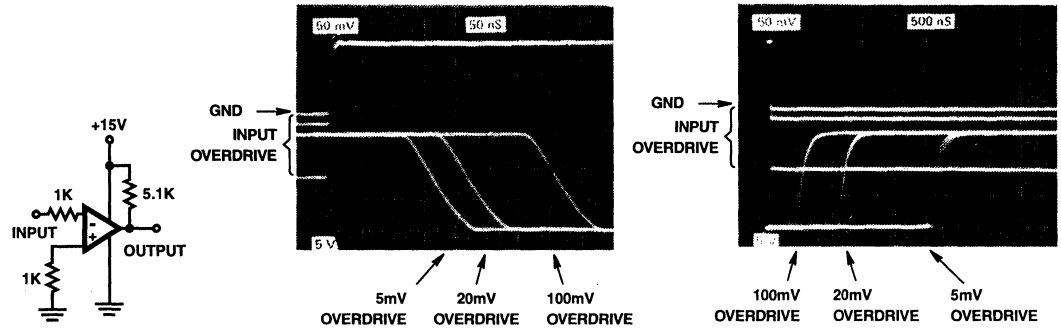


FIGURE 3. INVERTING COMPARATOR RESPONSE TIME TEST CIRCUIT AND WAVEFORMS

Circuit Description

The Basic Comparator

Figure 4 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry type "139" comparators, with PMOS transistors replacing PNP transistors as input stage elements. Transistors Q_1 through Q_4 comprise the differential input stage, with Q_5 and Q_6 serving as a mirror connected active load and differential-to-single-ended converter. The differential input at Q_1 and Q_4 is amplified so as to toggle Q_6 in accordance with the input signal polarity. For example, if $+V_{IN}$ is greater than $-V_{IN}$, Q_1, Q_2, and current mirror transistors Q_5 and Q_6 will be turned off; Transistors Q_3, Q_4, and Q_7 will be turned on, causing Q_8 to be turned off. The output is pulled positive when a load resistor is connected between the output and V+.

In essence, Q_1 and Q_4 function as source followers to drive Q_2 and Q_3, respectively, with zener diodes D_1 through D_4 providing gate oxide protection against input voltage transients (e.g., static electricity). The current flow in Q_1 and Q_4 is established at approximately 50μA by constant current sources I_1 and I_3, respectively. Since Q_1 and Q_4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode range.

As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential DC voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q_7 and Q_8. The collector of Q_8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink current capability.

The detailed schematic diagram for one comparator and the common current source biasing is shown on the front page. PMOS transistors Q_9 through Q_{12} are the current source elements identified in Figure 4 as I_1 through I_4, respectively. Their gate source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right hand portion of the Schematic Diagram. The currents supplied by Q_{10} and Q_{12} are twice those supplied by Q_9 and Q_{11}. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q_9 through Q_{12}.

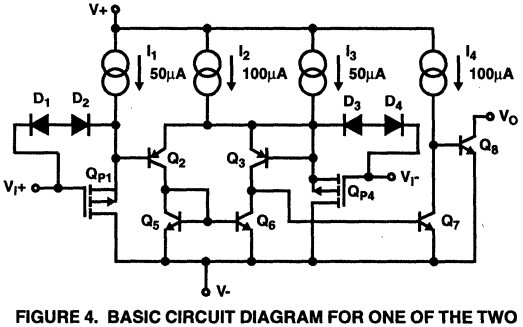


FIGURE 4. BASIC CIRCUIT DIAGRAM FOR ONE OF THE TWO COMPARATORS

Operating Considerations

Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra high input impedance (≅1.7TΩ);
2. The availability of common mode rejection for input signals at potentials below that of the negative power supply rail;
3. Retention of the in phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input terminal currents should not exceed 1mA. Appropriate series connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the V+ terminal of the CA3290.

Parasitic Oscillations

The ideal comparator has, among other features, ultra high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1mV to 10mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8 lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, switching rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1kΩ a capacitor (≥1pF - 2pF) be connected between the appropriate input terminal and the output terminal. (See Figure 1.)

The CA3290A is also supplied in a 14 lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the V+ or V- supply rail. If either comparator is unused, its input terminals should also be tied to either the V+ or V- supply rail.

Typical Applications

Light Controlled One-Shot Timer

In Figure 5 one comparator (A_1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A_2) is configured as a one-shot timer and is triggered by the output of A_1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R_1 and R_2. The ratio of R_1 to R_2 should be constant to insure constant reverse voltage bias on the photo diode.

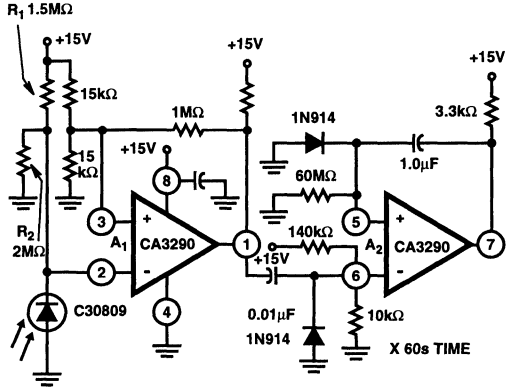


FIGURE 5. LIGHT CONTROLLED ONE-SHOT TIMER

Low-Frequency Multivibrator

In this application, one half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R_1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading. R_P is the parallel combination of the two 1MΩ resistors connected between +15V and GND.

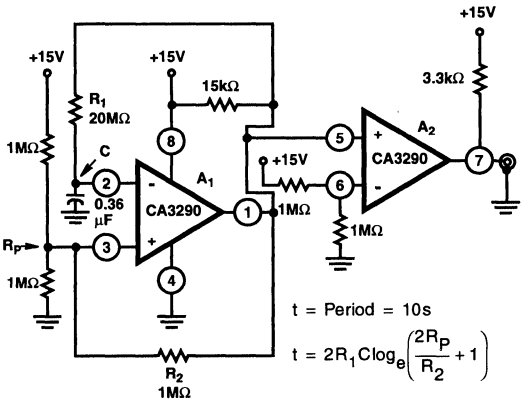


FIGURE 6. LOW FREQUENCY MULTIVIBRATOR

Window Comparator

Both halves of the CA3290 can be used in a high input impedance window comparator as shown in Figure 7. The LED will be turned "on" whenever the input signal is above the lower limit (V_L) but below the upper limit (V_U), as determined by the $R_1/R_2/R_3$ resistor divider.

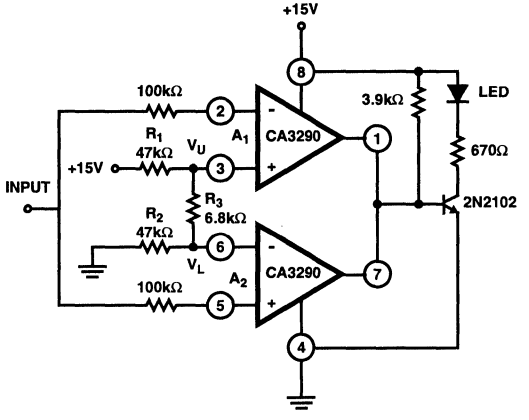


FIGURE 7. WINDOW COMPARATOR

Typical Performance Curves

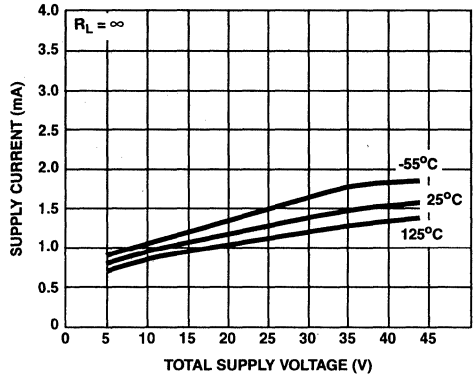


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE (BOTH AMPLIFIERS)

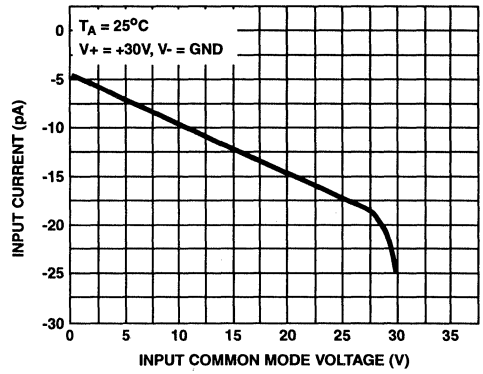


FIGURE 9. INPUT CURRENT vs INPUT COMMON MODE VOLTAGE

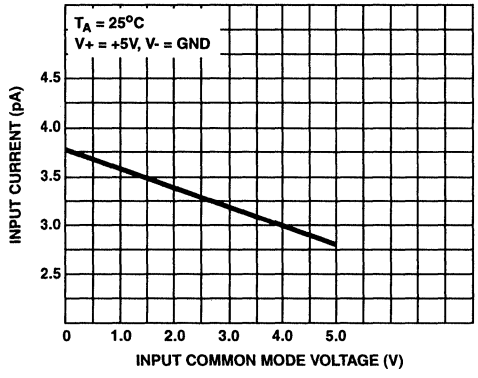


FIGURE 10. INPUT CURRENT vs INPUT COMMON MODE VOLTAGE

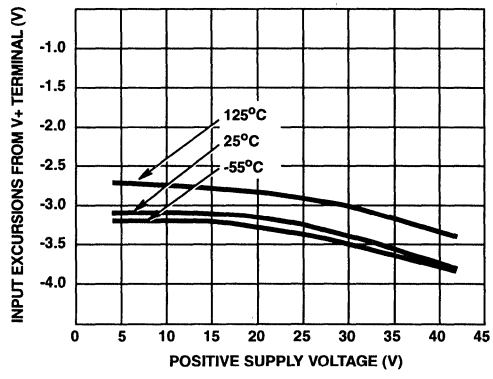


FIGURE 11. POSITIVE COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

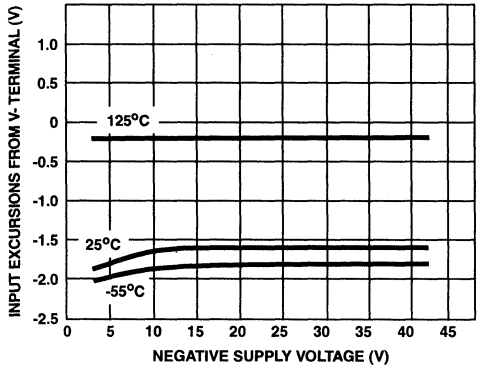


FIGURE 12. NEGATIVE COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

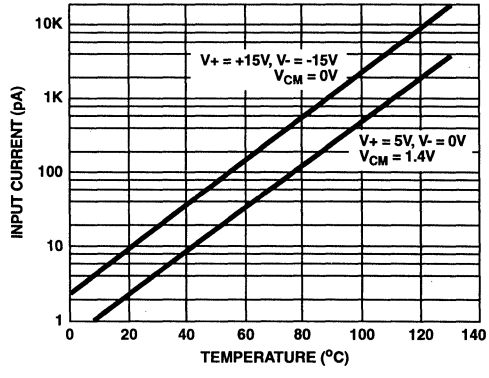


FIGURE 13. INPUT CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

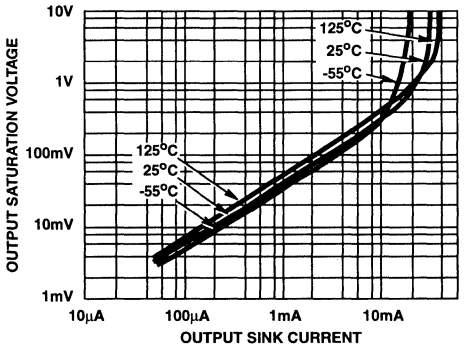
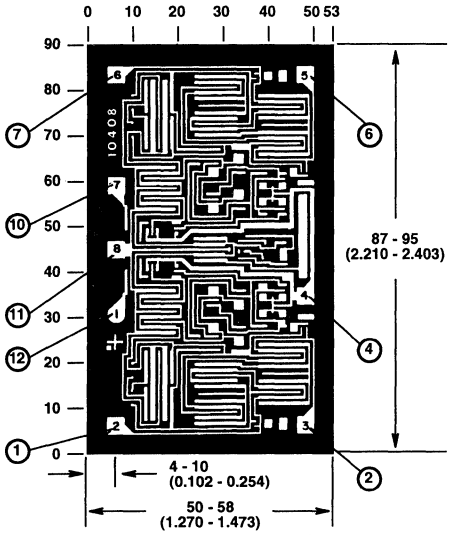


FIGURE 14. OUTPUT SATURATION VOLTAGE vs OUTPUT SINK CURRENT

Metallization Mask Layout



The photographs and dimensions of each chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7mils (0.17mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

NOTE: Numbers in pads are for 8 lead DIP and TO-5 Can and numbers outside of chip are for 14 lead DIP.

HA-4900, HA-4902, HA-4905

November 1996

Precision Quad Comparators

Features

- Fast Response Time 130ns
- Low Offset Voltage. 2.0mV
- Low Offset Current 10nA
- Single or Dual Voltage Supply Operation
- Selectable Output Logic Levels
- Active Pull-Up/Pull-Down Output Circuit. No External Resistors Required

Applications

- Threshold Detector
- Zero Crossing Detector
- Window Detector
- Analog Interfaces for Microprocessors
- High Stability Oscillators
- Logic System Interfaces

Ordering Information

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. NO.
HA1-4900-2	-55 to 125	16 Ld CERDIP	F16.3
HA1-4902-2	-55 to 125	16 Ld CERDIP	F16.3
HA1-4905-5	0 to 75	16 Ld CERDIP	F16.3
HA3-4905-5	0 to 75	16 Ld PDIP	E16.3
HA4P4905-5	0 to 75	20 Ld PLCC	N20.35
HA9P4905-5	0 to 75	16 Ld SOIC	M16.3

Description

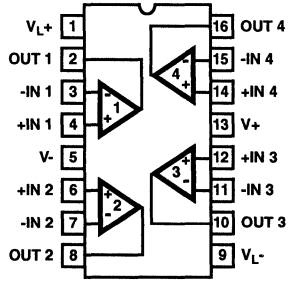
The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5V supply (digital systems) or from dual supplies (analog networks) up to ±15V. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies (V_{LOGIC}+ and V_{LOGIC}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

These comparators' combination of features make them ideal components for signal detection and processing in data acquisition systems, test equipment and microprocessor/analog signal interface networks.

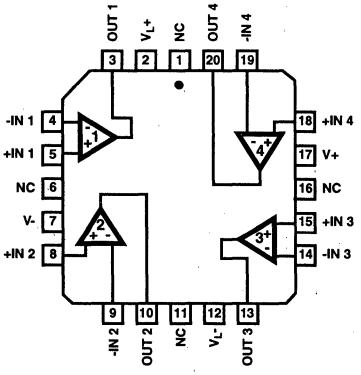
For military grade product, refer to the HA-4902/883 data sheet.

Pinouts

HA-4900, HA-4902 (CERDIP)
HA-4905 (PDIP, CERDIP, SOIC)
TOP VIEW



HA-4905
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2855.2**

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 33V
Differential Input Voltage 15V
Voltage Between V_{LOGIC}+ and V_{LOGIC}- 18V
Output Current 50mA
Power Dissipation (Notes 1, 2)

Operating Conditions

Temperature Range
HA-4900-2, HA-4902-2 . . . . . -55°C to 125°C
HA-4905-5 . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	85	25
PDIP Package	90	N/A
SOIC Package	100	N/A
PLCC Package	75	N/A

Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC and SOIC - Lead Tips Only)

Die Characteristics

Back Side Potential . . . . . V-
Number of Transistors 137
Die Size . . . . . 95 mils x 105 mils

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below 175°C for ceramic packages, and below 150°C for plastic packages.
2. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{LOGIC} shown in curves of Power Dissipation vs Supply Voltages (see Performance Curves). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T.P.D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{LOGIC}+, V_{LOGIC}-) gives a T.P.D. of 350mW, the combination +15V, -15V, +15V, 0V gives a T.P.D. of 450mW.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15V, V_{LOGIC}+ = 5V, V_{LOGIC}- = GND

PARAMETER	TEMP (°C)	HA-4900-2 -55°C to 125°C			HA-4902-2 -55°C to 125°C			HA-4905-5 0°C to 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 4)	25	-	2	3	-	2	5	-	4	7.5	mV
	Full	-	-	4	-	-	8	-	-	10	mV
Offset Current	25	-	10	25	-	10	35	-	25	50	nA
	Full	-	-	35	-	-	45	-	-	70	nA
Bias Current (Note 5)	25	-	50	75	-	50	150	-	100	150	nA
	Full	-	-	150	-	-	200	-	-	300	nA
Input Sensitivity (Note 6)	25	-	-	V_{IO} + 0.3	-	-	V_{IO} + 0.5	-	-	V_{IO} + 0.5	mV
	Full	-	-	V_{IO} + 0.4	-	-	V_{IO} + 0.6	-	-	V_{IO} + 0.7	mV
Common Mode Range	Full	V-	-	(V+) - 2.4	V-	-	(V+) - 2.6	V-	-	(V+) - 2.4	V
Differential Input Resistance	25	-	250	-	-	250	-	-	250	-	MΩ
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	25	-	400	-	-	400	-	-	400	-	kV/V
Response Time ($t_{PD}(0)$) (Note 7)	25	-	130	200	-	130	200	-	130	200	ns
Response Time ($t_{PD}(1)$) (Note 7)	25	-	180	215	-	180	215	-	180	215	ns

Electrical Specifications $V_{SUPPLY} = \pm15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = GND$ **(Continued)**

PARAMETER	TEMP (°C)	HA-4900-2 -55°C to 125°C			HA-4902-2 -55°C to 125°C			HA-4905-5 0°C to 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS											
Output Voltage Level											
Logic "Low State" (V_{OL}) (Note 8)	Full	-	0.2	0.4	-	0.2	0.4	-	0.2	0.4	V
Logic "High State" (V_{OH}) (Note 8)	Full	3.5	4.2	-	3.5	4.2	-	3.5	4.2	-	V
Output Current											
I_{SINK}	Full	3.0	-	-	3.0	-	-	3.0	-	-	mA
I_{SOURCE}	Full	3.0	-	-	3.0	-	-	3.0	-	-	mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{PS} (+)	25	-	6.5	20	-	6.5	20	-	7	20	mA
Supply Current, I_{PS} (-)	25	-	4	8	-	4	8	-	5	8	mA
Supply Current, I_{PS} (Logic)	25	-	3.5	4	-	3.5	4	-	3.5	4	mA
Supply Voltage Range											
$V_{LOGIC}+$ (Note 2)	Full	0	-	+15.0	0	-	+15.0	0	-	+15.0	V
$V_{LOGIC}-$ (Note 2)	Full	-15.0	-	0	-15.0	-	0	-15.0	-	0	V

NOTES:

4. Minimum differential input voltage required to ensure a defined output state.
5. Input bias currents are essentially constant with differential input voltages up to ±9V. With differential input voltages from ±9V to ±15V, bias current on the more negative input can rise to approximately 500µA. This will also cause higher supply currents.
6. $V_{CM} = 0V$. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter includes the effects of offset voltage and voltage gain.
7. For $t_{PD}(1)$; 100mV input step, -10mV overdrive. For $t_{PD}(0)$; -100mV input step, 10mV overdrive. Frequency ≈ 100Hz; Duty Cycle ≈ 50%; Inverting input driven. See Figure 1 for Test Circuit. All unused inverting inputs tied to +5V.
8. For V_{OH} and V_{OL}: $I_{SINK} = I_{SOURCE} = 3.0mA$. For other values of V_{LOGIC}; V_{OH} (Min) = V_{LOGIC} + -1.5V.

Test Circuit and Waveform

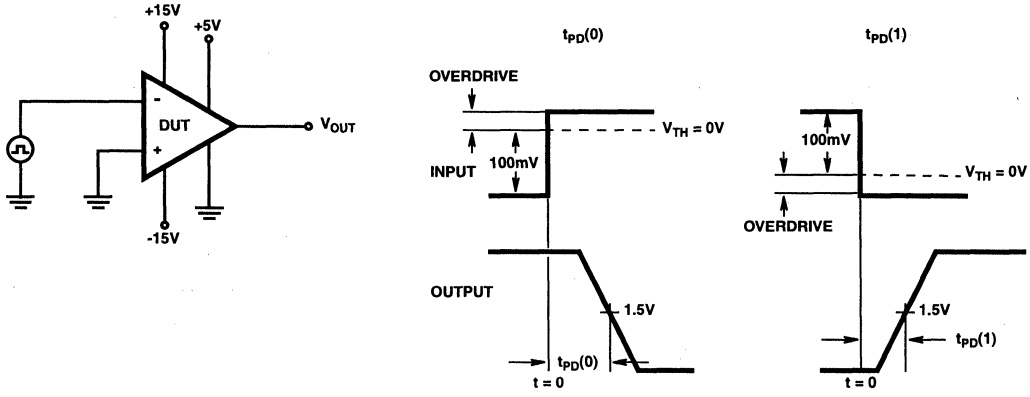
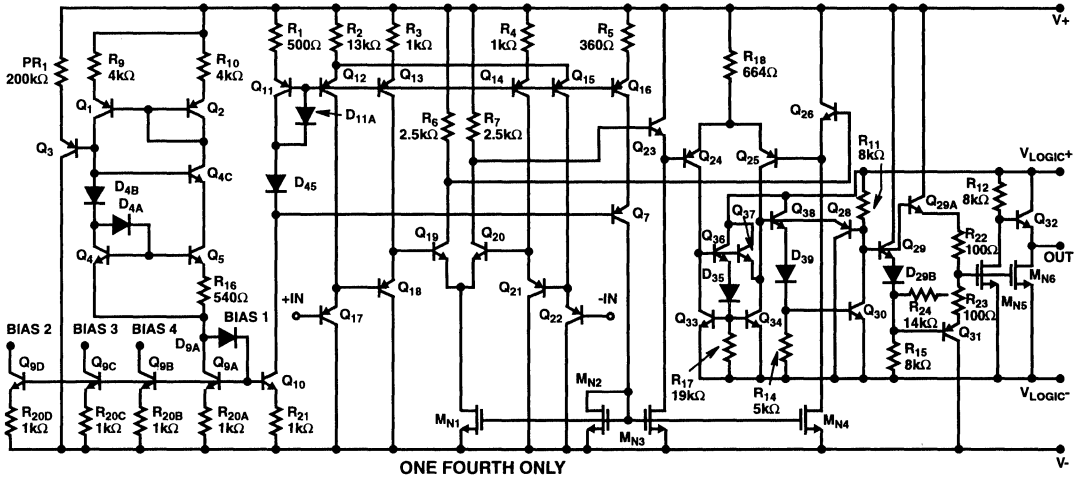


FIGURE 1.

Schematic Diagram



Applying the HA-4900 Series Comparators

Supply Connections

This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{LOGIC}+ and V_{LOGIC}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings ($15V_{P-P}$, Max) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to 15V), V+ and V_{LOGIC}+ may be connected together to the positive supply while V- and V_{LOGIC}- are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to < 5mA since the C-B junction of the input transistor would be forward biased.

Unused Inputs

Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter."

Crosstalk

Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

Power Supply Decoupling

Decouple all power supply lines with 0.01µF ceramic capacitors to ground line located near the package to reduce coupling between channels or from external sources.

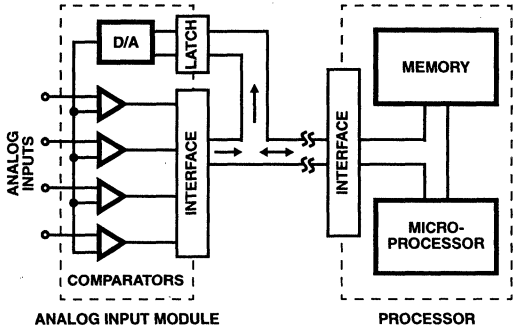
Response Time

Fast rise time (<200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.

Typical Applications

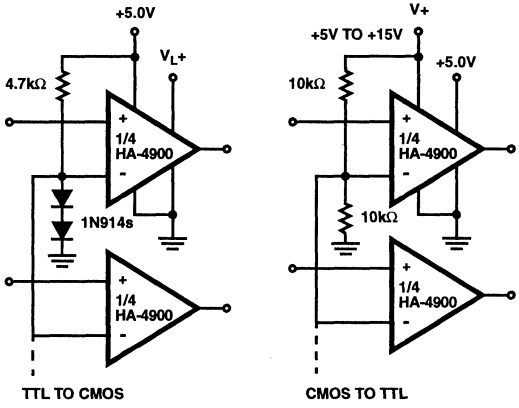
Data Acquisition System

In this circuit the HA-4900 series is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs. To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



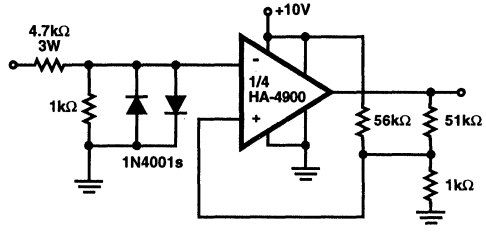
Logic Level Translators

The HA-4900 series comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections. If separate supplies are used for V- and V_{LOGIC}-, these logic level translators will tolerate several volts of ground line differential noise.



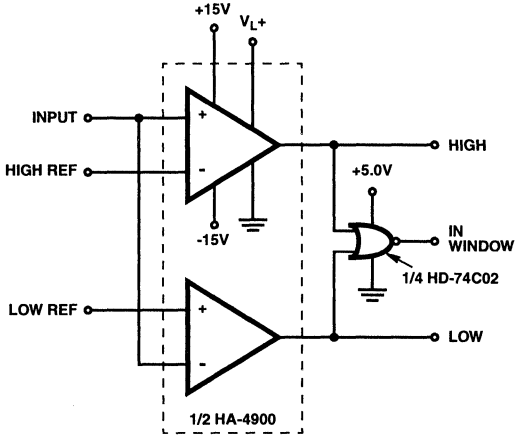
RS-232 To CMOS Line Receiver

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1V input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3W input resistor will protect the inputs under these conditions.



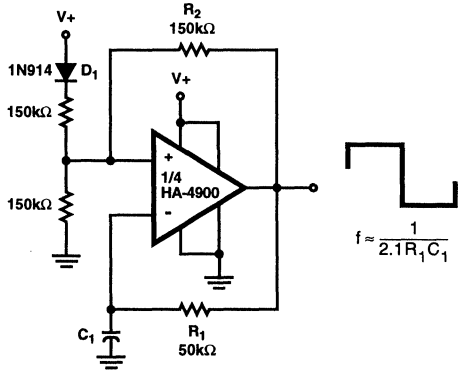
Window Detector

The high switching speed, low offset current and low offset voltage of the HA-4900 series makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.



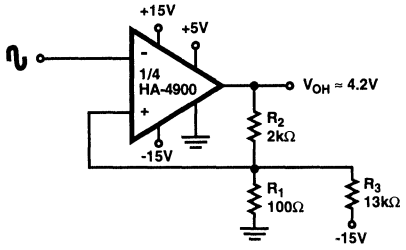
Oscillator/Clock Generator

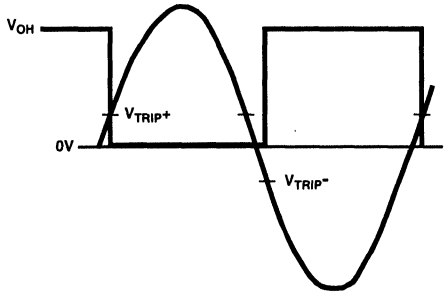
This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{SUPPLY}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



Schmitt Trigger (Zero Crossing Detector With Hysteresis)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.





INPUT TO OUTPUT WAVEFORM SHOWING HYSTERESIS TRIP POINTS

Typical Performance Curves $T_A = 25^oC$, $V_S = \pm15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = 0V$, Unless Otherwise Specified

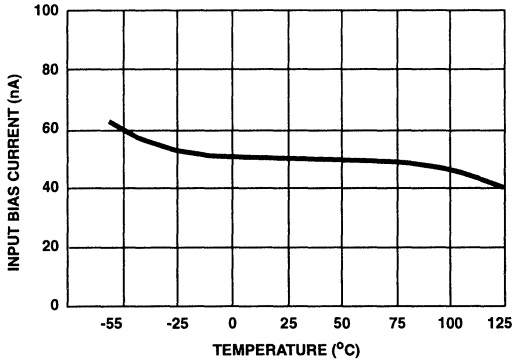


FIGURE 2. INPUT BIAS CURRENT vs TEMPERATURE

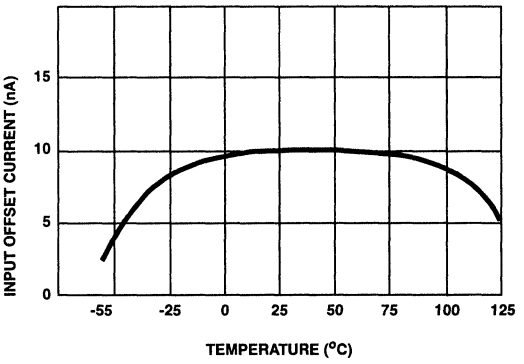


FIGURE 3. INPUT OFFSET CURRENT vs TEMPERATURE

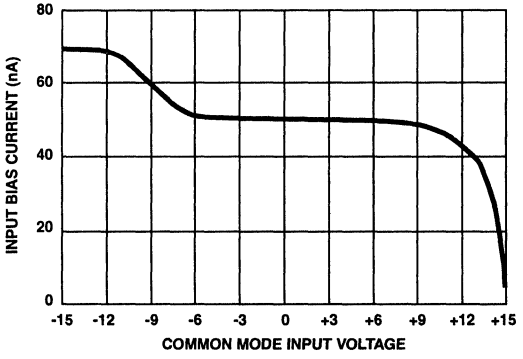


FIGURE 4. INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE (V_{DIFF} = 0V)

Typical Performance Curves $T_A = 25^oC$, $V_S = \pm15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = 0V$, Unless Otherwise Specified (Continued)

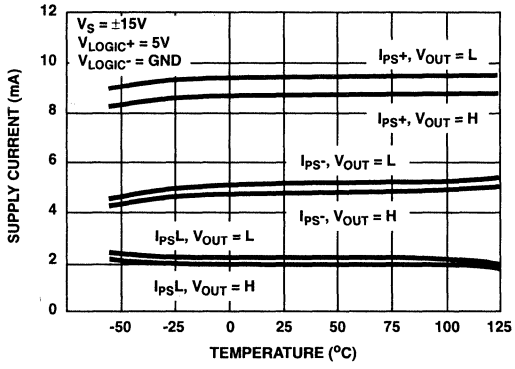


FIGURE 5. SUPPLY CURRENT vs TEMPERATURE (FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY)

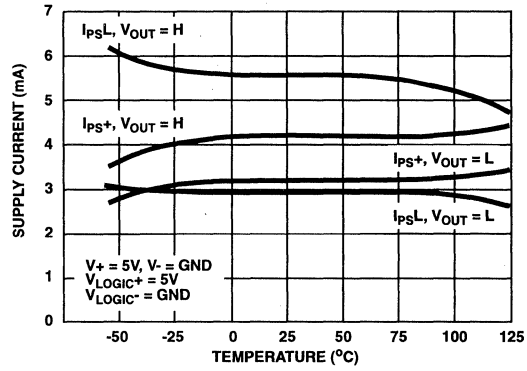
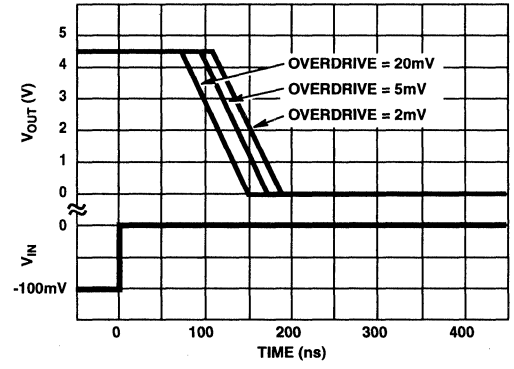


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE (FOR SINGLE +5V OPERATION)



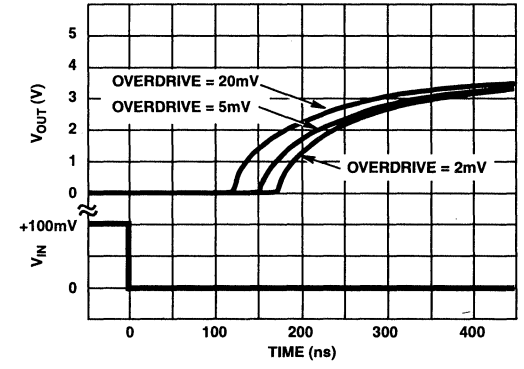


FIGURE 7. RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

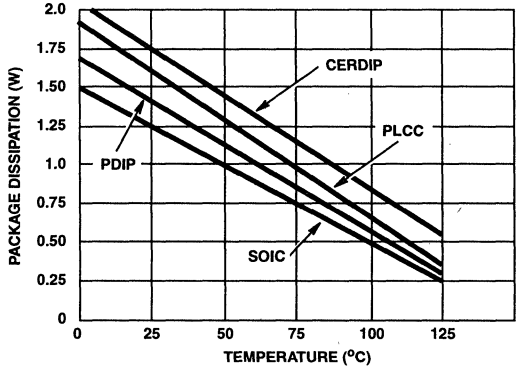


FIGURE 8. MAXIMUM PACKAGE DISSIPATION vs AMBIENT TEMPERATURE

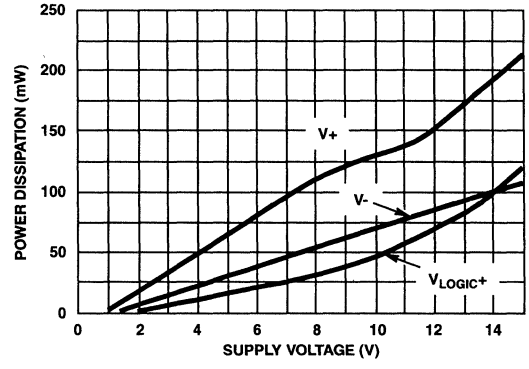


FIGURE 9. POWER DISSIPATION vs SUPPLY VOLTAGE (NO LOAD CONDITION)

LINEAR 5

SAMPLE AND HOLD AMPLIFIERS

Selection Guide

SAMPLE AND HOLD AMPLIFIERS: Typical Values at 25°C, Unless Otherwise Specified

TYPE	SAMPLE/HOLD TYPE	TEMP. RANGE (°C)	(NOTE 1) LEAD COUNT AND PACKAGE TYPE	ACQUISITION TIME (TO 0.01%)	HOLD STEP ERROR	APERTURE TIME	GAIN BANDWIDTH PRODUCT
HA1-2420-2	External Hold Cap, Low Cost	-55 to 125	14 CERDIP	3.2µs	10mV	30ns	2.5MHz (C_H = 1000pF)
HA1-2425-5		0 to 75	14 CERDIP				
HA3-2425-5		0 to 75	14 PDIP				
HA4P2425-5		0 to 75	20 PLCC				
HA9P2425-5		0 to 75	14 SOIC				
HA1-5320-2	High Speed, Low Charge, Transfer, Precision, Includes Hold Capacitor	-55 to 125	14 CERDIP	1µs (C_H = Internal)	1mV	25ns	2.0MHz (C_H = 100pF)
HA1-5320-5		0 to 75	14 CERDIP				
HA1-5320/883		-55 to 125	14 CERDIP				
HA3-5320-5		0 to 75	14 PDIP				
HA4-5320/883		-55 to 125	20 CLCC				
HA9P5320-5		0 to 75	16 SOIC (300 mil)				
HA9P5320-9		-40 to 85	16 SOIC (300 mil)				
HA1-5330-5	Very High Speed, Precision, Monolithic, Includes Hold Capacitor	0 to 75	14 CERDIP	650ns	0.5mV	20ns	4.5MHz
HA1-5330-4		-25 to 85	14 CERDIP				
HA1-5330-2		-55 to 125	14 CERDIP				
HA1-5330/883		-55 to 125	14 CERDIP				
HA3-5330-5		0 to 75	14 PDIP				
HA4-5330/883		-55 to 125	20 CLCC				
HA1-5340-5	High Speed, Low Distortion, Includes Hold Capacitor	0 to 75	14 CERDIP	700ns	15mV	15ns	10MHz
HA1-5340-9		-40 to 85	14 CERDIP				
HA1-5340/883		-55 to 125	14 CERDIP				
HA3-5340-5		0 to 75	14 PDIP				
HA3-5340-9		-40 to 85	14 PDIP				
HA4-5340/883		-55 to 125	20 CLCC				
HA9P5340-5		0 to 75	16 SOIC (300 mil)				
HA5351IP	Ultra High Speed and Low Power, Includes Hold Capacitor, Low Pin Count	-40 to 85	8 PDIP	64ns	10mV	10ns	40MHz
HA5351IB		-40 to 85	8 SOIC				

NOTE:

1. See Linear Package Selection Guide in Section 11.

HA-2420, HA-2425

November 1996

3.2μs Sample and Hold Amplifiers

Features

- **Maximum Acquisition Time**
  - **10V Step to 0.1%..... 4μs (Max)**
  - **10V Step to 0.01%..... 6μs (Max)**
- **Low Droop Rate (C_H = 1000pF)..... 5μV/ms (Typ)**
- **Gain Bandwidth Product ..... 2.5MHz (Typ)**
- **Low Effective Aperture Delay Time ..... 30ns (Typ)**
- **TTL Compatible Control Input**
- **±12V to ±15V Operation**

Applications

- **12-Bit Data Acquisition**
- **Digital to Analog Deglitcher**
- **Auto Zero Systems**
- **Peak Detector**
- **Gated Operational Amplifier**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-2420-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-2425-5	0 to 75	14 Ld CERDIP	F14.3
HA3-2425-5	0 to 75	14 Ld PDIP	E14.3
HA4P2425-5	0 to 75	20 Ld PLCC	N20.35
HA9P2425-5	0 to 75	14 Ld SOIC	M14.15

Description

The HA-2420 and HA-2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and JFET input unity gain amplifier.

With an external hold capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

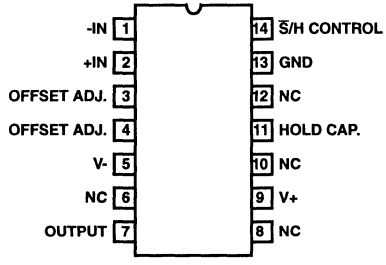
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note AN517.

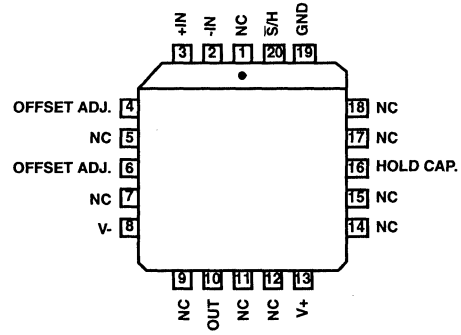
The MIL-STD-883 data sheet for this device is available on request.

Pinouts

HA-2420 (CERDIP)
HA-2425 (CERDIP, PDIP, SOIC)
TOP VIEW



HA-2425
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2856.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage. 24V
Digital Input Voltage (Sample and Hold Pin) . . . . . +8V, -15V
Output Current . . . . . Short Circuit Protected

Operating Conditions

Temperature Range
HA-2420-2. . . . . -55°C to 125°C
HA-2425-5. . . . . 0°C to 75°C
Supply Voltage Range (Typical) . . . . . ±12V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	90	35
PDIP Package	100	N/A
PLCC Package	75	N/A
SOIC Package	120	N/A

Maximum Junction Temperature (Ceramic Packages) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC and SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±15.0V; C_H = 1000pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to Negative Input)

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-2420-2			HA-2425-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Input Voltage Range		Full	±10	-	-	±10	-	-	V
Offset Voltage		25	-	2	4	-	3	6	mV
		Full	-	3	6	-	4	8	mV
Bias Current		25	-	40	200	-	40	200	nA
		Full	-	-	400	-	-	400	nA
Offset Current		25	-	10	50	-	10	50	nA
		Full	-	-	100	-	-	100	nA
Input Resistance		25	5	10	-	5	10	-	MΩ
Common Mode Range		Full	±10	-	-	±10	-	-	V
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	R_L = 2kΩ, V_O = 20V_{P-P}	Full	25	50	-	25	50	-	kV/V
Common Mode Rejection	V_{CM} = ±10V	Full	80	90	-	74	90	-	dB
Hold Mode Feedthrough Attenuation (Note 2)	f_{IN} ≤ 100kHz	Full	-	-76	-	-	-76	-	dB
Gain Bandwidth Product (Note 2)		25	-	2.5	-	-	2.5	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 2kΩ	Full	±10	-	-	±10	-	-	V
Output Current		25	±15	-	-	±15	-	-	mA
Full Power Bandwidth (Note 2)	V_O = 20V_{P-P}	25	-	100	-	-	100	-	kHz
Output Resistance	DC	25	-	0.15	-	-	0.15	-	Ω
TRANSIENT RESPONSE									
Rise Time (Note 2)	V_O = 200mV_{P-P}	25	-	75	100	-	75	100	ns
Overshoot (Note 2)	V_O = 200mV_{P-P}	25	-	25	40	-	25	40	%
Slew Rate (Note 2)	V_O = 10V_{P-P}	25	3.5	5	-	3.5	5	-	V/µs
DIGITAL INPUT CHARACTERISTICS									
Digital Input Current	V_{IN} = 0V	Full	-	-	-0.8	-	-	-0.8	mA
	V_{IN} = 5V	Full	-	-	20	-	-	20	µA
Digital Input Voltage	Low	Full	-	-	0.8	-	-	0.8	V
	High	Full	2.0	-	-	2.0	-	-	V
SAMPLE AND HOLD CHARACTERISTICS									
Acquisition Time (Note 2)	To 0.1% 10V Step	25	-	2.3	4	-	2.3	4	µs

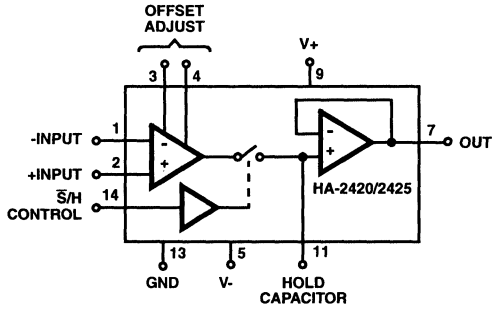
Electrical Specifications Test Conditions (Unless Otherwise Specified) $V_{SUPPLY} = \pm 15.0V$; $C_H = 1000pF$; Digital Input: $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold), Unity Gain Configuration (Output tied to Negative Input) **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-2420-2			HA-2425-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Acquisition Time (Note 2)	To 0.01% 10V Step	25	-	3.2	6	-	3.2	6	µs
Hold Step Error	$V_{IN} = 0V$	25	-	10	20	-	10	20	mV
Hold Mode Settling Time	To ±1mV	25	-	860	-	-	860	-	ns
Aperture Time (Note 3)		25	-	30	-	-	30	-	ns
Effective Aperture Delay Time		25	-	30	-	-	30	-	ns
Aperture Uncertainty		25	-	5	-	-	5	-	ns
Drift Current (Note 2)	$V_{IN} = 0V$	25	-	5	-	-	5	-	pA
HA1-2420		Full	-	1.8	10	-	-	-	nA
HA1-2425		Full	-	-	-	-	0.1	1.0	nA
HA3-2425, HA4P2425, HA9P2425		Full	-	-	-	-	7.5	10.0	nA
POWER SUPPLY CHARACTERISTICS									
Supply Current (+)		25	-	3.5	5.5	-	3.5	5.5	mA
Supply Current (-)		25	-	2.5	3.5	-	2.5	3.5	mA
Power Supply Rejection		Full	80	90	-	74	90	-	dB

NOTES:

2. $A_V = \pm 1$, $R_L = 2k\Omega$, $C_L = 50pF$.
3. Derived from computer simulation only; not tested.

Functional Diagram



Test Circuits and Waveforms

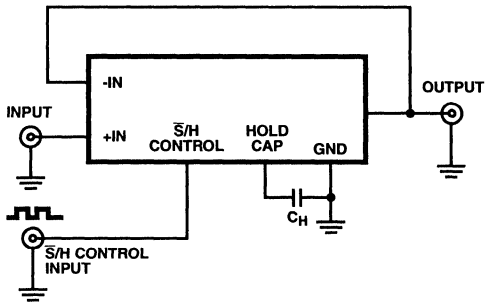
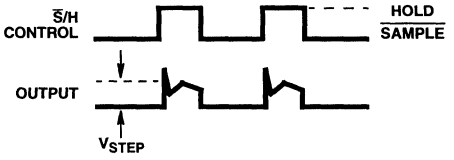


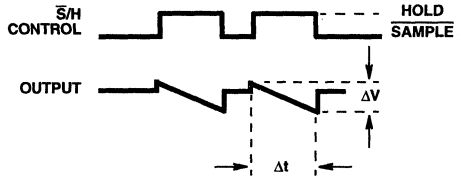
FIGURE 1. HOLD STEP ERROR AND DRIFT CURRENT



NOTE: Set rise/fall times of S/H Control to approximately 20ns.

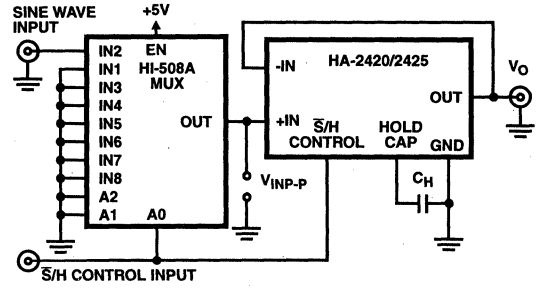
FIGURE 2. HOLD STEP ERROR TEST

Test Circuits and Waveforms (Continued)



NOTE: Measure the slope of the output during hold, $\Delta V/\Delta t$, and compute drift current from: $I_D = C_H \Delta V/\Delta t$.

FIGURE 3. DRIFT CURRENT TEST



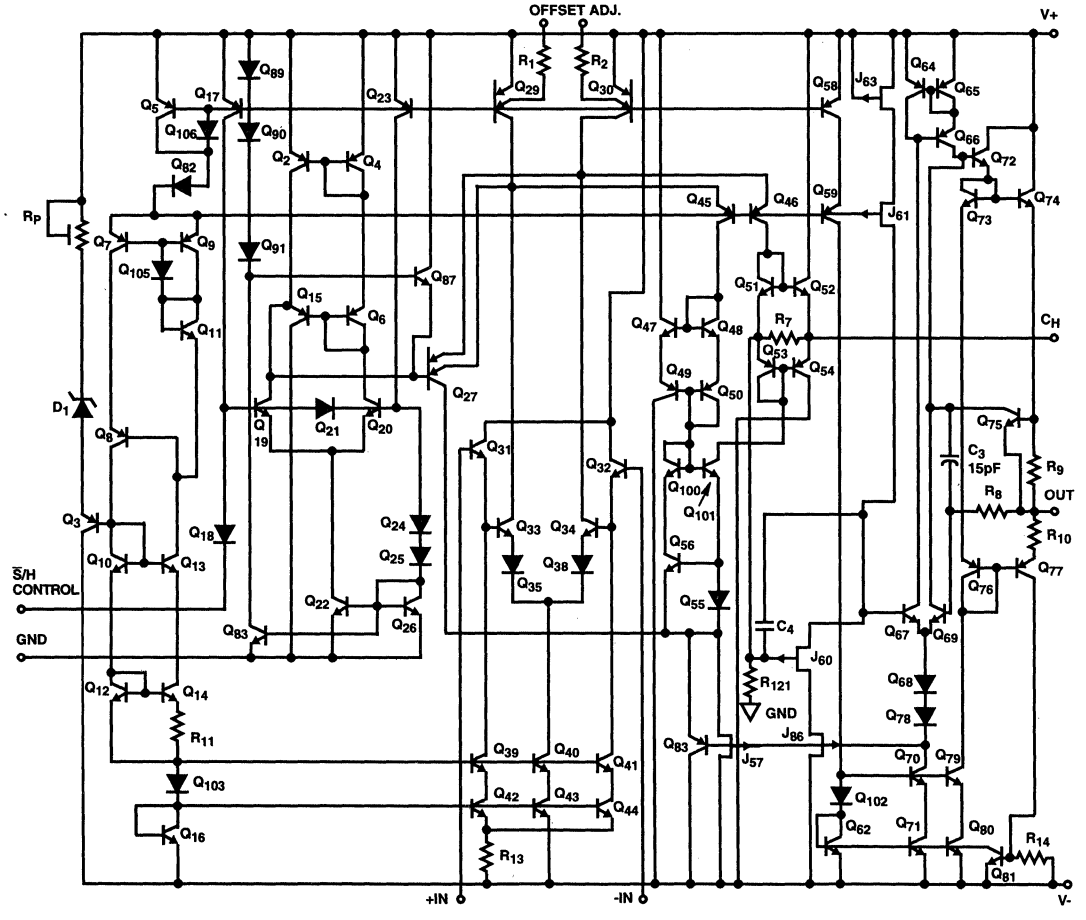
NOTE: Compute hold mode feedthrough attenuation from the formula:

$$\text{Feedthrough Attenuation} = 20\log\frac{V_{OUT}HOLD}{V_{IN}HOLD}$$

Where $V_{OUT}HOLD$ = Peak-to-Peak value of output sinewave during the hold mode.

FIGURE 4. HOLD MODE FEEDTHROUGH ATTENUATION

Schematic Diagram



Application Information

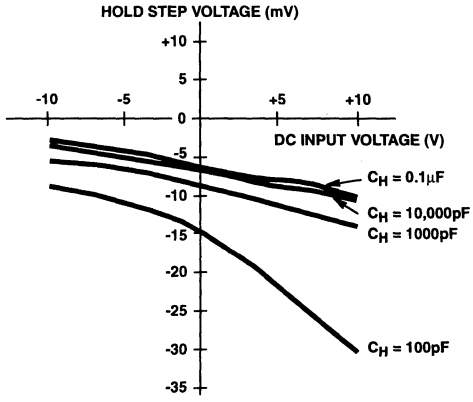


FIGURE 5. HOLD STEP vs INPUT VOLTAGE

Offset Adjustment

The offset voltage of the HA-2420 and HA-2425 may be adjusted using a 100kΩ trim pot, as shown in Figure 8. The recommended adjustment procedure is:

Apply 0V to the sample-and-hold input, and a square wave to the $\overline{S}$/H control.

Adjust the trim pot for 0V output in the hold mode.

Gain Adjustment

The linear variation in pedestal voltage with sample-and- hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10NOMINAL}$). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10NOMINAL}) + (-10V)}{2}$$

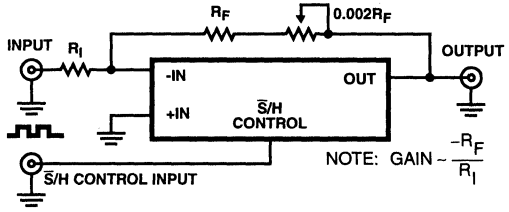


FIGURE 6. INVERTING CONFIGURATION

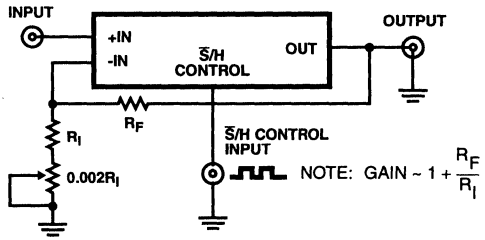


FIGURE 7. NON-INVERTING CONFIGURATION

Figure 8 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

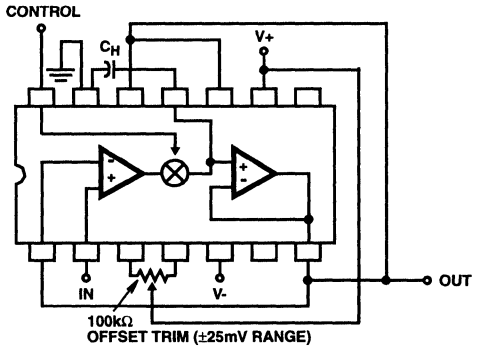


FIGURE 8. BASIC SAMPLE-AND-HOLD (TOP VIEW)

The method used to reduce leakage paths on the PC board and the device package is shown in Figure 9. This guard ring is recommended to minimize the drift during hold mode.

The hold capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below 85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note AN517, or the factory applications group.

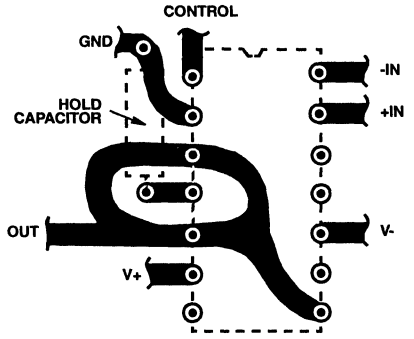


FIGURE 9. GUARD RING LAYOUT (BOTTOM VIEW)

Glossary of Terms

Acquisition Time

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the S/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\ (pA) = C_H\ (pF) \times \frac{\Delta V}{\Delta t}\ (V/s)$$

Typical Performance Curves

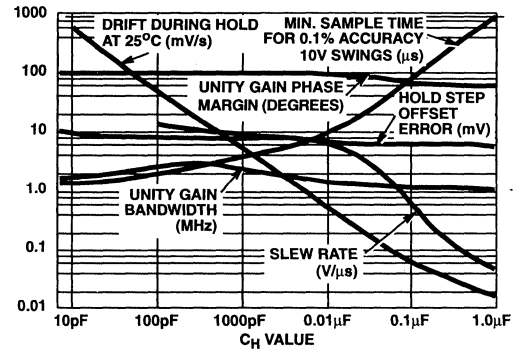


FIGURE 10. TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR

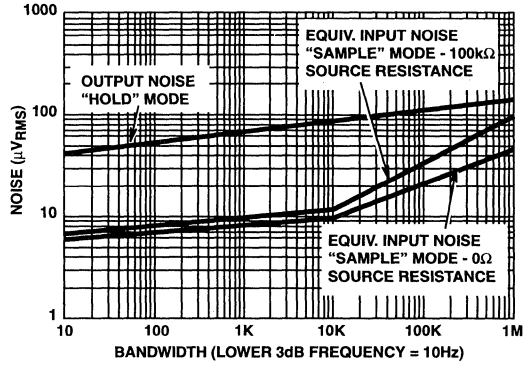


FIGURE 11. BROADBAND NOISE CHARACTERISTICS

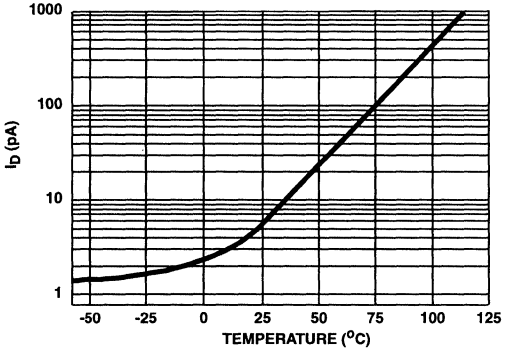


FIGURE 12. DRIFT CURRENT vs TEMPERATURE

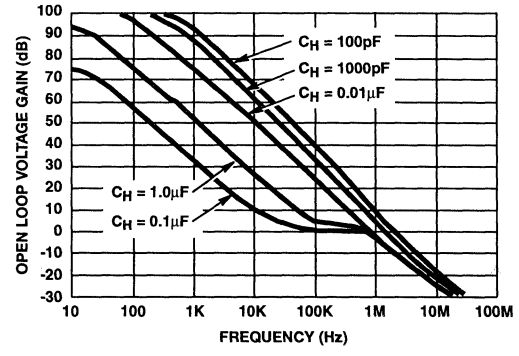


FIGURE 13. OPEN LOOP FREQUENCY RESPONSE

Typical Performance Curves (Continued)

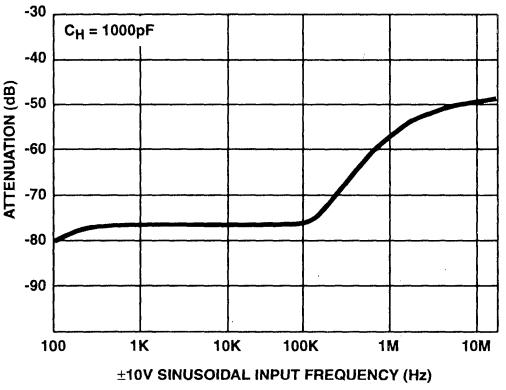


FIGURE 14. HOLD MODE FEED THROUGH ATTENUATION

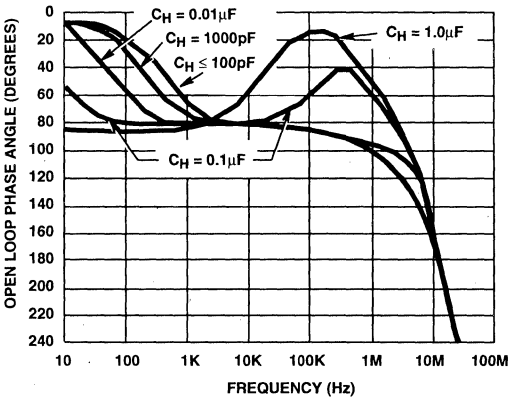


FIGURE 15. OPEN LOOP PHASE RESPONSE

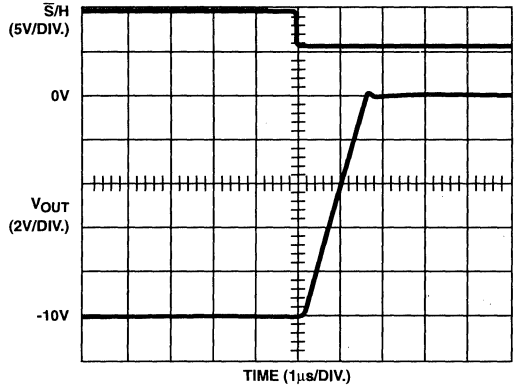


FIGURE 16. ACQUISITION TIME (C_H = 1000pF)

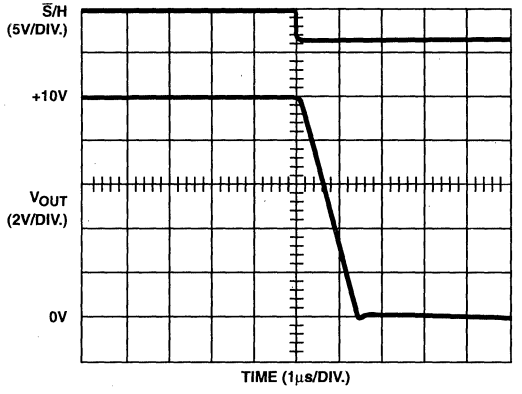


FIGURE 17. ACQUISITION TIME (C_H = 1000pF)

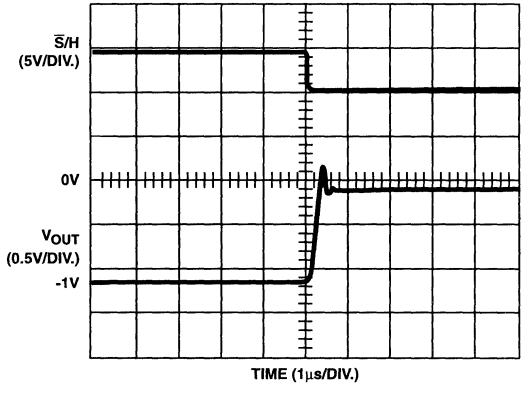


FIGURE 18. ACQUISITION TIME (C_H = 1000pF)

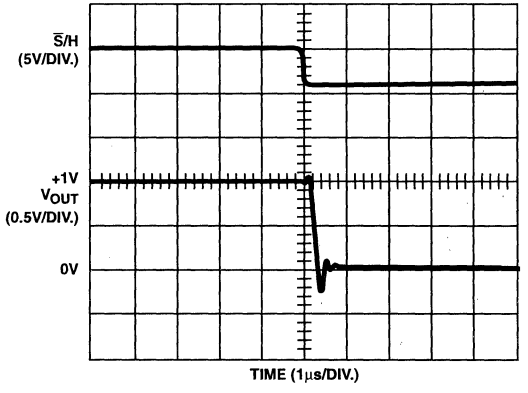


FIGURE 19. ACQUISITION TIME (C_H = 1000pF)

5 SAMPLE/HOLD AMPLIFIERS

Typical Performance Curves (Continued)

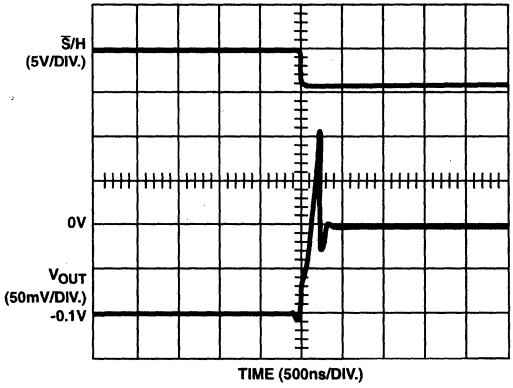


FIGURE 20. ACQUISITION TIME (C_H = 1000pF)

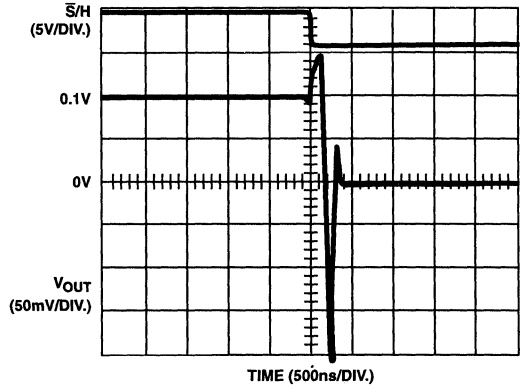


FIGURE 21. ACQUISITION TIME (C_H = 1000pF)

Die Characteristics

DIE DIMENSIONS:
102 mils x 61 mils x 19 mils
2590µm x 1550µm x 483µm

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL:
V-

BACKSIDE FINISH:
Gold, Nickel, Silicon, etc.

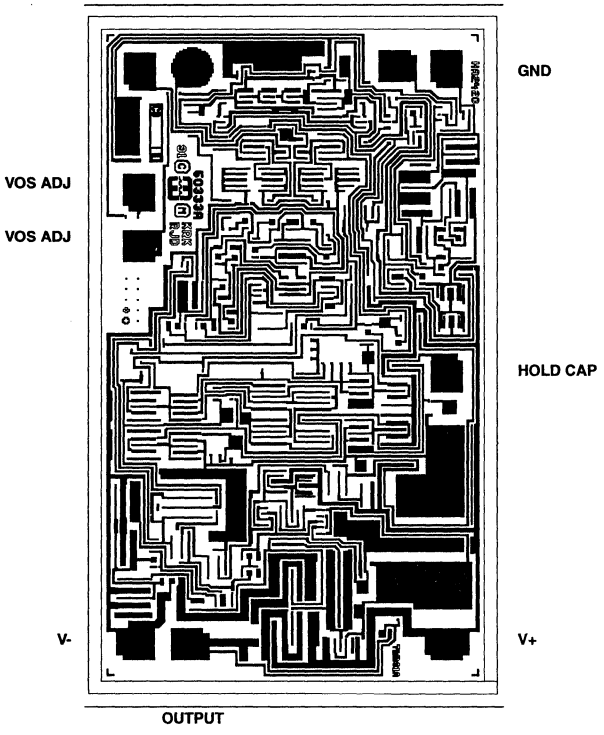
PASSIVATION:
Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:
78

PROCESS:
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2420, HA-2425



HARRIS SEMICONDUCTOR

HA-5320

1μs Precision Sample and Hold Amplifier

November 1996

Features

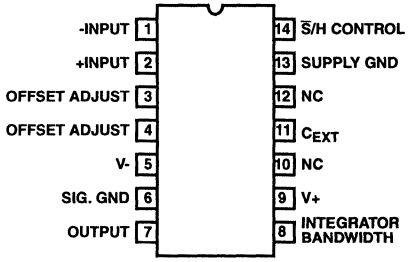
- Gain, DC . . . . . 2×10^6 V/V
- Acquisition Time 1.0μs (0.01%)
- Droop Rate . . . . . 0.08μV/μs (25°C)
  17μV/μs (Full Temperature)
- Aperture Time 25ns
- Hold Step Error (See Glossary) 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Applications

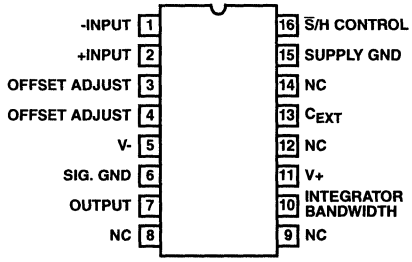
- Precision Data Acquisition Systems
- Digital to Analog Converter Deglitcher
- Auto Zero Circuits
- Peak Detector

Pinouts

HA-5320
(PDIP, CERDIP)
TOP VIEW



HA-5320
(SOIC)
TOP VIEW



Description

The HA-5320 was designed for use in precision, high speed data acquisition systems.

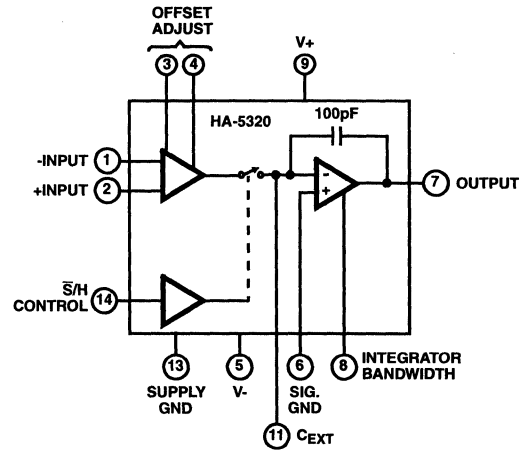
The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCRs. This allows higher speed and latch-free operation. For further information, please see Application Note AN538. For Military grade product refer to the HA-5320/883 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-5320-2	-55 to 25	14 Ld CERDIP	F14.3
HA1-5320-5	0 to 75	14 Ld CERDIP	F14.3
HA3-5320-5	0 to 75	14 Ld PDIP	E14.3
HA9P5320-5	0 to 75	16 Ld SOIC	M16.3
HA9P5320-9	-40 to 85	16 Ld SOIC	M16.3

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2857.3**

Absolute Maximum Ratings

Supply Voltage 40V
Differential Input Voltage. 24V
Digital Input Voltage . . . . . +8V, -15V
Output Current, Continuous (Note 1) . . . . . ±20mA

Operating Conditions

Temperature Range
HA-5320-2. . . . . -55°C to 125°C
HA-5320-5. . . . . 0°C to 75°C
HA-5320-9. . . . . -40°C to 85°C
Supply Voltage Range (Typical, Note 2) . . . . . ±13.5V to ±20V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	66	16
PDIP Package	90	N/A
SOIC Package	95	N/A

Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Internal Power Dissipation may limit Output Current below 20mA.
2. Specification based on a one time characterization. This parameter is not guaranteed.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15.0V; C_H = Internal; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5320-2/-9			HA-5320-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Input Voltage Range		Full	±10	-	-	±10	-	-	V
Input Resistance		25	1	5	-	1	5	-	MΩ
Input Capacitance		25	-	-	5	-	-	5	pF
Offset Voltage		25	-	0.2	-	-	0.5	-	mV
		Full	-	-	2.0	-	-	1.5	mV
Bias Current		25	-	70	200	-	100	300	nA
		Full	-	-	200	-	-	300	nA
Offset Current		25	-	30	100	-	30	300	nA
		Full	-	-	100	-	-	300	nA
Common Mode Range		Full	±10	-	-	±10	-	-	V
CMRR	V_{CM} = ±5V	25	80	90	-	72	90	-	dB
Offset Voltage Temperature Coefficient		Full	-	5	15	-	5	20	µV/°C
TRANSFER CHARACTERISTICS									
Gain	DC, (Note 12)	25	10^6	2×10^6	-	3×10^5	2×10^6	-	V/V
Gain Bandwidth Product (A_V = +1, Note 5)	C_H = 100pF	25	-	2.0	-	-	2.0	-	MHz
	C_H = 1000pF	25	-	0.18	-	-	0.18	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage		Full	±10	-	-	±10	-	-	V
Output Current		25	±10	-	-	±10	-	-	mA
Full Power Bandwidth	Note 4	25	-	600	-	-	600	-	kHz
Output Resistance	Hold Mode	25	-	1.0	-	-	1.0	-	Ω
Total Output Noise (DC to 10MHz)	Sample	25	-	125	200	-	125	200	μV_{RMS}
	Hold	25	-	125	200	-	125	200	μV_{RMS}
TRANSIENT RESPONSE									
Rise Time	Note 5	25	-	100	-	-	100	-	ns

Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5320-2/-9			HA-5320-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Overshoot	Note 5	25	-	15	-	-	15	-	%
Slew Rate	Note 6	25	-	45	-	-	45	-	V/µs
DIGITAL INPUT CHARACTERISTICS									
Input Voltage	V_{IH}	Full	2.0	-	-	2.0	-	-	V
	V_{IL}	Full	-	-	0.8	-	-	0.8	V
Input Current	V_{IL} = 0V	25	-	-	4	-	-	4	µA
		Full	-	-	10	-	-	10	µA
	V_{IH} = +5V	Full	-	-	0.1	-	-	0.1	µA
SAMPLE AND HOLD CHARACTERISTICS									
Acquisition Time (Note 7)	To 0.1%	25	-	0.8	1.2	-	0.8	1.2	µs
	To 0.01%	25	-	1.0	1.5	-	1.0	1.5	µs
Aperture Time (Note 8)		25	-	25	-	-	25	-	ns
Effective Aperture Delay Time		25	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty		25	-	0.3	-	-	0.3	-	ns
Droop Rate		25	-	0.08	0.5	-	0.08	0.5	µV/µs
		Full	-	17	100	-	1.2	100	µV/µs
Drift Current	Note 9	25	-	8	50	-	8	50	pA
		Full	-	1.7	10	-	0.12	10	nA
Charge Transfer	Note 9	25	-	0.5	1.1	-	0.5	1.1	pC
Hold Step Error	Note 9	25	-	5	11	-	5	11	mV
Hold Mode Settling Time	To 0.01%	Full	-	165	350	-	165	350	ns
Hold Mode Feedthrough	$10V_{P-P}$, 100kHz	Full	-	2	-	-	2	-	mV
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current	Note 10	25	-	11	13	-	11	13	mA
Negative Supply Current	Note 10	25	-	-11	-13	-	-11	-13	mA
Supply Voltage Range	Note 2		±13.5	–	±20	±13.5	-	±20	V
Power Supply Rejection	V+, Note 11	Full	80	-	-	80	-	-	dB
	V-, Note 11	Full	65	-	-	65	-	-	dB

NOTES:

4. $V_O = 20V_{P-P}$; $R_L = 2k\Omega$; $C_L = 50pF$; unattenuated output.
5. $V_O = 200mV_{P-P}$; $R_L = 2k\Omega$; $C_L = 50pF$.
6. V_O = 20V Step; $R_L = 2k\Omega$; $C_L = 50pF$.
7. V_O = 10V Step; $R_L = 2k\Omega$; $C_L = 50pF$.
8. Derived from computer simulation only; not tested.
9. V_{IN} = 0V, V_{IH} = +3.5V, t_R < 20ns (V_{IL} to V_{IH}).
10. Specified for a zero differential input voltage between +IN and -IN. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±46mA at 20V.
11. Based on a 1V delta in each supply, i.e. 15V $\pm 0.5V_{DC}$.
12. $R_L = 1k\Omega$, $C_L = 30pF$.

Test Circuits and Waveforms

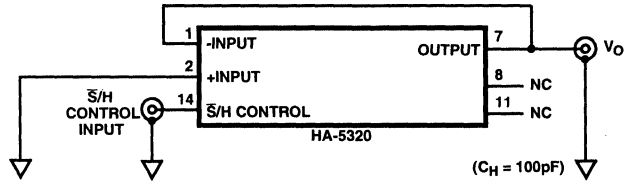
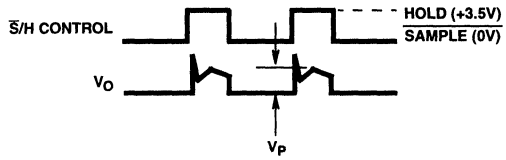


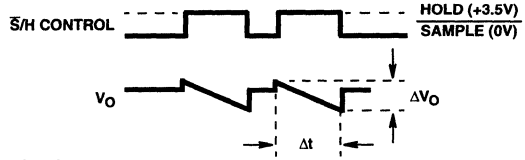
FIGURE 1. CHARGE TRANSFER AND DRIFT CURRENT



NOTES:

13. Observe the "hold step" voltage V_P.
14. Compute charge transfer: $Q = V_P C_H$.

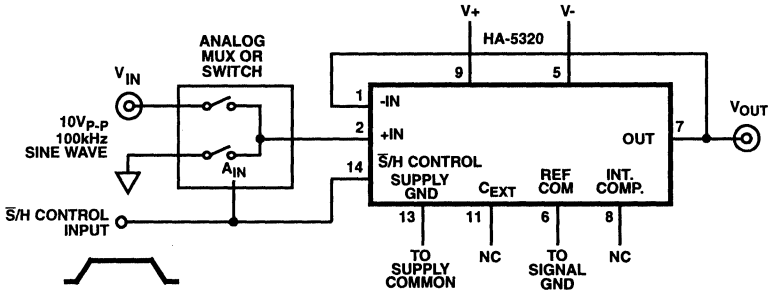
FIGURE 2. CHARGE TRANSFER TEST



NOTES:

15. Observe the voltage "droop", $\Delta V_O/\Delta t$.
16. Measure the slope of the output during hold, $\Delta V_O/\Delta t$, and compute drift current: $I_D = C_H \Delta V_O/\Delta t$.

FIGURE 3. DRIFT CURRENT TEST



NOTE:

Feedthrough in

$$dB = 20\log\frac{V_{OUT}}{V_{IN}}$$ where:

$V_{OUT} = V_{P-P}$, Hold Mode,
$V_{IN} = V_{P-P}$.

FIGURE 4. HOLD MODE FEEDTHROUGH ATTENUATION

Application Information

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note AN517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01mF to 0.1mF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5320 includes a 100pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor).

Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor C_{EXT} is used, then a noise bandwidth capacitor of value $0.1C_{EXT}$ should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor C_{EXT} should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to 85°C. Teflon® and glass dielectrics offer good performance to 125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

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Typical Application

Figure 5 shows the HA-5320 connected as a unity gain non-inverting amplifier - its most widely used configuration. As an input device for a fast successive - approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5320's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The application may call for an external hold capacitor C_{EXT} as shown. As mentioned earlier, $0.1C_{EXT}$ is then recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

Glossary of Terms

Acquisition Time

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Charge Transfer

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the HOLD mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

Charge Transfer (pC) = C_H (pF) x Hold Step Error (V)

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is the interval between the conditions of 10% open and 90% open.

Hold Step Error

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{Hold Step (V)} = \frac{\text{Charge Transfer (pC)}}{\text{Hold Capacitance (pF)}}$$

See Performance Curves.

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the S/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D \text{ (pA)} = C_H\text{(pF)} \times \frac{\Delta V}{\Delta t} \text{ (V/s)}$$

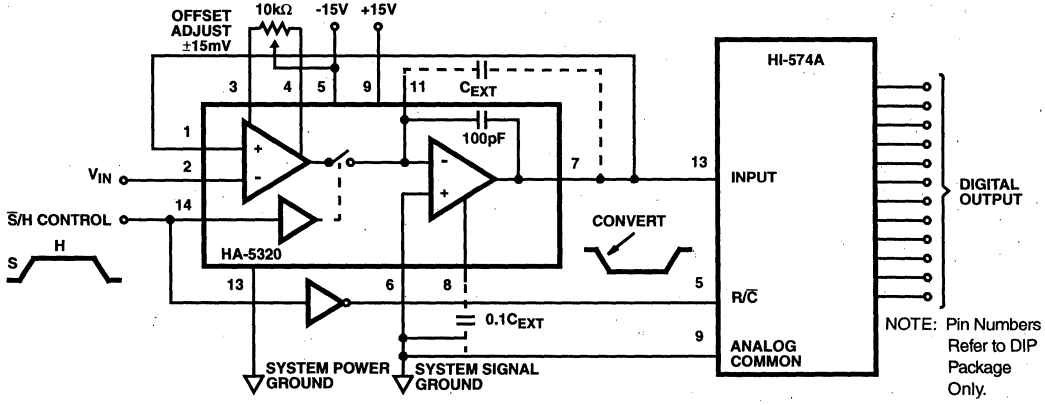


FIGURE 5. TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE

Typical Performance Curves

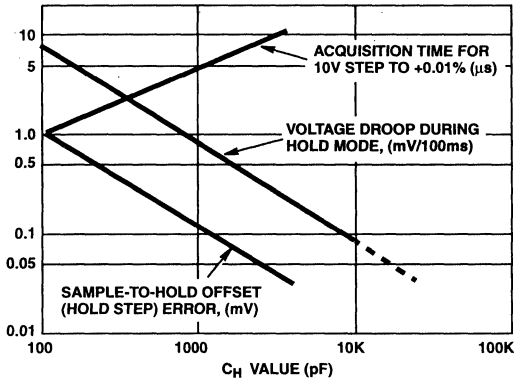


FIGURE 6. TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLD CAPACITOR

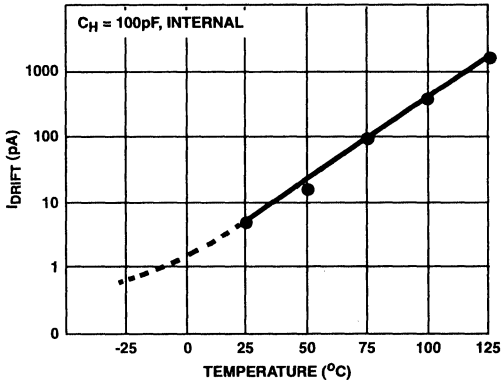


FIGURE 7. DRIFT CURRENT vs TEMPERATURE

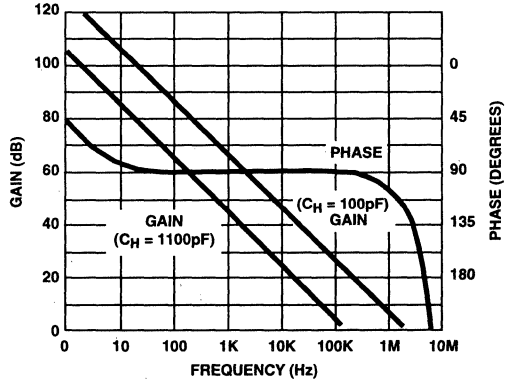


FIGURE 8. OPEN LOOP GAIN AND PHASE RESPONSE

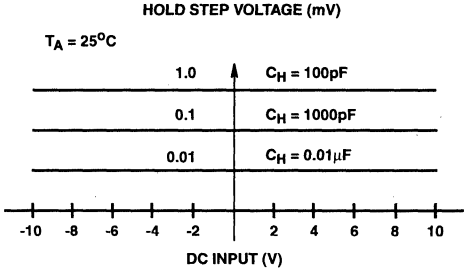


FIGURE 9A. HOLD STEP vs INPUT VOLTAGE

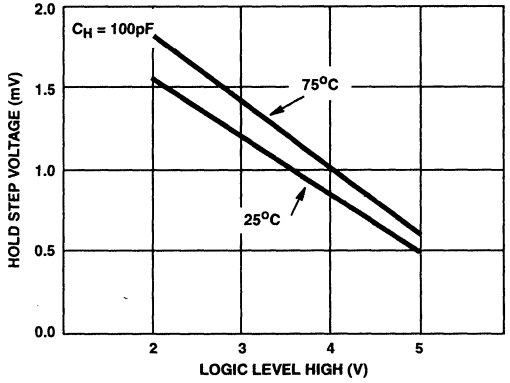


FIGURE 9B. HOLD STEP vs LOGIC (V_{IH}) VOLTAGE

FIGURE 9. TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR

Die Characteristics

DIE DIMENSIONS:

92 mils x 152 mils x 19 mils

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

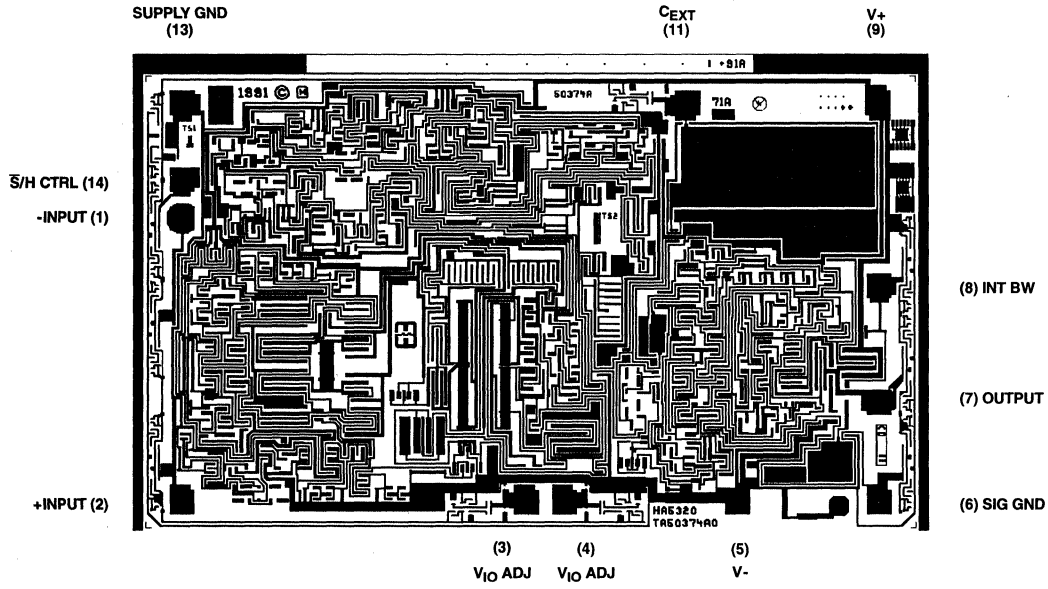
184

SUBSTRATE POTENTIAL:

V-

Metallization Mask Layout

HA-5320



HARRIS SEMICONDUCTOR

HA-5330

650ns Precision Sample and Hold Amplifier

November 1996

Features

- Very Fast Acquisition 500ns (0.1%) 650ns (0.01%)
- Low Droop Rate 0.01μV/μs
- Very Low Offset 0.2mV
- High Slew Rate. 90V/μs
- Wide Supply Range. . . . . ±10V to ±20V
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

Description

The HA-5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 650ns acquisition time to 12-bit accuracy and a droop rate of 0.01μV/μs. The circuit consists of an input transconductance amplifier capable of producing large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{IN}. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

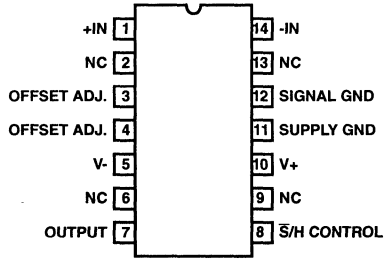
The HA-5330 will operate at reduced supply voltages (to ±10V) with a reduced signal range. The MIL-STD-883 data sheet for this device is available on request.

Ordering Information

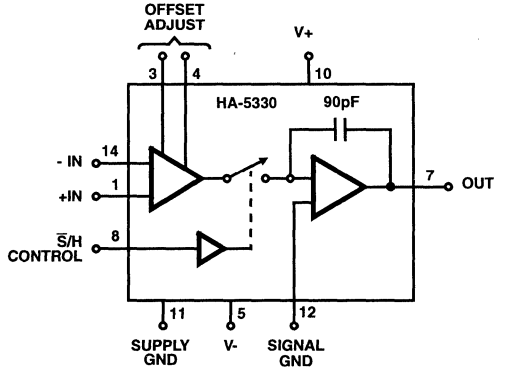
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-5330-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-5330-4	-25 to 85	14 Ld CERDIP	F14.3
HA1-5330-5	0 to 75	14 Ld CERDIP	F14.3
HA3-5330-5	0 to 75	14 Ld PDIP	E14.3

Pinout

HA-5330
(PDIP, CERDIP)
TOP VIEW



Functional Diagram



5 SAMPLE/HOLD AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2858.2**

Absolute Maximum Ratings

Voltage between V+ and SUPPLY/SIG GND . . . . . +20V
Voltage between V- and SUPPLY/SIG GND . . . . . -20V
Voltage between SUPPLY GND and SIG GND . . . . . ±2.0V
Voltage between $\overline{S}$/H Control and SUPPLY/SIG GND . . . . +8V, -6V
Differential Input Voltage 24V
Output Current, Continuous (Note 1) . . . . . ±17mA

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	66	16
PDIP Package	90	N/A

Maximum Junction Temperature (Ceramic Package, Note 2) . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range
HA-5330-2 . . . . . -55°C to 125°C
HA-5330-4 . . . . . -25°C to 85°C
HA-5330-5 . . . . . 0°C to 75°C
Supply Voltage Range (Typical) . . . . . ±10V to ±20V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Internal Power Dissipation may limit Output Current below ±17mA.
2. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below 175°C for the ceramic package, and below 150°C for the plastic package.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15V; $\overline{S}$/H Control V_{IL} = +0.8V (Sample): V_{IH} = +2.0V (Hold); SIG GND = SUPPLY GND, Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5330-2, -4			HA-5330-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Input Voltage Range		Full	±10	-	-	±10	-	-	V
Input Resistance (Note 4)		25	5	15	-	5	15	-	MΩ
Input Capacitance		25	-	3	-	-	3	-	pF
Offset Voltage		25	-	0.2	-	-	0.2	-	mV
		Full	-	-	2.0	-	-	1.5	mV
Offset Voltage Temperature Coefficient		Full	-	1	10	-	1	10	µV/°C
Bias Current		25	-	±20	-	-	±20	-	nA
		Full	-	-	±500	-	-	±300	nA
Offset Current		25	-	20	-	-	20	-	nA
		Full	-	-	500	-	-	300	nA
Common Mode Range		Full	±10	-	-	±10	-	-	V
CMRR	V_{CM} = ±10V	Full	86	100	-	86	100	-	dB
TRANSFER CHARACTERISTICS									
Gain	DC	Full	2×10^6	2×10^7	-	2×10^6	2×10^7	-	V/V
Gain Bandwidth Product	Note 12	25	-	4.5	-	-	4.5	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage		Full	±10	-	-	±10	-	-	V
Output Current		Full	±10	-	-	±10	-	-	mA
Full Power Bandwidth (Note 6)		25	-	1.4	-	-	1.4	-	MHz
Output Resistance	Hold Mode	25	-	0.2	-	-	0.2	-	Ω
	Sample Mode	25	-	10^{-5}	0.001	-	10^{-5}	0.001	Ω

Electrical Specifications V_{SUPPLY} = ±15V; $\overline{S}$/H Control V_{IL} = +0.8V (Sample): V_{IH} = +2.0V (Hold); SIG GND = SUPPLY GND, Unity Gain Configuration (Output tied to -Input), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5330-2, -4			HA-5330-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Total Output Noise, DC to 4MHz	Sample Mode		-	230	-	-	230	-	μV_{RMS}
	Hold Mode	25	-	190	-	-	190	-	μV_{RMS}
TRANSIENT RESPONSE									
Rise Time	Note 5	25	-	70	-	-	70	-	ns
Overshoot	Note 5	25	-	10	-	-	10	-	%
Slew Rate	Note 7	25	-	90	-	-	90	-	V/µs
DIGITAL INPUT CHARACTERISTICS									
Input Voltage	V_{IH}	Full	2.0	-	-	2.0	-	-	V
	V_{IL}	Full	-	-	0.8	-	-	0.8	V
Input Current	V_{IL} = 0V	Full	-	10	40	-	10	40	µA
	V_{IH} = 5V	Full	-	10	40	-	10	40	µA
SAMPLE/HOLD CHARACTERISTICS									
Acquisition Time	To 0.1%, Note 8	25	-	500	-	-	500	-	ns
		Full	-	-	700	-	-	700	ns
	To 0.01%, Note 8	25	-	650	-	-	650	-	ns
		Full	-	-	900	-	-	900	ns
Aperture Time (Note 4)		25	-	20	-	-	20	-	ns
Effective Aperture Delay Time		25	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty		25	-	0.1	-	-	0.1	-	ns
Droop Rate (Note 9)		25	-	0.01	-	-	0.01	-	µV/µs
		Full	-	-	100	-	-	10	µV/µs
Hold Step Error	Note 10	25	-	0.5	-	-	0.5	-	mV
Hold Mode Settling Time	To 0.01%	25	-	100	200	-	100	200	ns
Hold Mode Feedthrough	$20V_{P-P}$, 100kHz	Full	-	-88	-	-	-88	-	dB
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current		Full	-	18	22	-	18	24	mA
Negative Supply Current		Full	-	19	23	-	19	25	mA
Power Supply Rejection	Note 11	Full	86	100	-	86	100	-	dB

NOTES:

4. Derived from computer simulation only; not tested.
5. V_I = 200mV Step; R_L = 2kΩ; C_L = 50pF.
6. Full power bandwidth based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$. Distortion of wave shape occurs beyond 100kHz due to slew rate enhancement circuitry.
7. V_O = 20V Step; R_L = 2kΩ; C_L = 50pF.
8. V_O = 10V Step; R_L = 2kΩ; C_L = 50pF.
9. This parameter is measured at ambient temperature extremes in a high speed test environment. Consequently, steady state heating effects from internal power dissipation are not included.
10. V_{IN} = 0V; V_{IH} = +3.5V; t_R = 22ns (V_{IL} to V_{IH}). See graph.
11. Based on a 3V delta in each supply, i.e. 15V ±1.5V_{DC}.
12. V_{OUT} = $200mV_{P-P}$, R_L = 2kΩ, C_L = 50pF.

Application Information

The HA-5330 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuit ideas. See the Harris Application Note AN517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01μF to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply GND Terminal on pin 11.

Typical Applications

The HA-5330 is configured as a unity gain noninverting amplifier by simply connecting the output (pin 7) to the inverting input (pin 14). As an input device for a fast successive - approximation A/D converter, it offers an extremely high throughput rate. Also, the HA-5330's pedestal error is adjustable to zero by using an Offset Adjust potentiometer (10K to 50K) center tapped to V-.

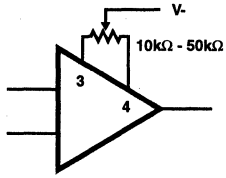


FIGURE 1. HA-5330 OFFSET ADJUST

The ideal ground connections are pin 11 (Supply Ground) directly to the system Supply Common, and pin 12 (Signal Ground) directly to the system Signal Ground (Analog Ground).

Hold Capacitor

The HA-5330 includes a 90pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on the internal capacitor).

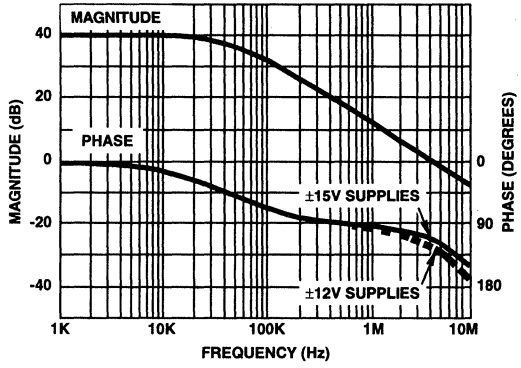


FIGURE 2. MAGNITUDE AND PHASE RESPONSE (CLOSED LOOP GAIN = 100)

Output Stage

The HA-5330 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the $\overline{S}$/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

Glossary of Terms

Acquisition Time

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error

Hold step error is the output shift due to charge transfer from the sample to the hold mode. It is also referred to as "offset step" or "pedestal error".

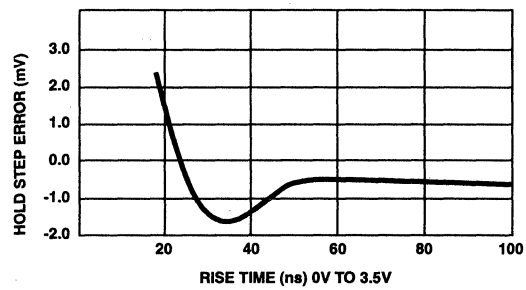


FIGURE 3. HOLD STEP ERROR vs $\overline{S}$/H CONTROL RISE TIME

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the $\overline{S}$/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Die Characteristics

DIE DIMENSIONS:

99 mils x 166 mils x 19 mils
2510µm x 4210µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Signal GND

TRANSISTOR COUNT:

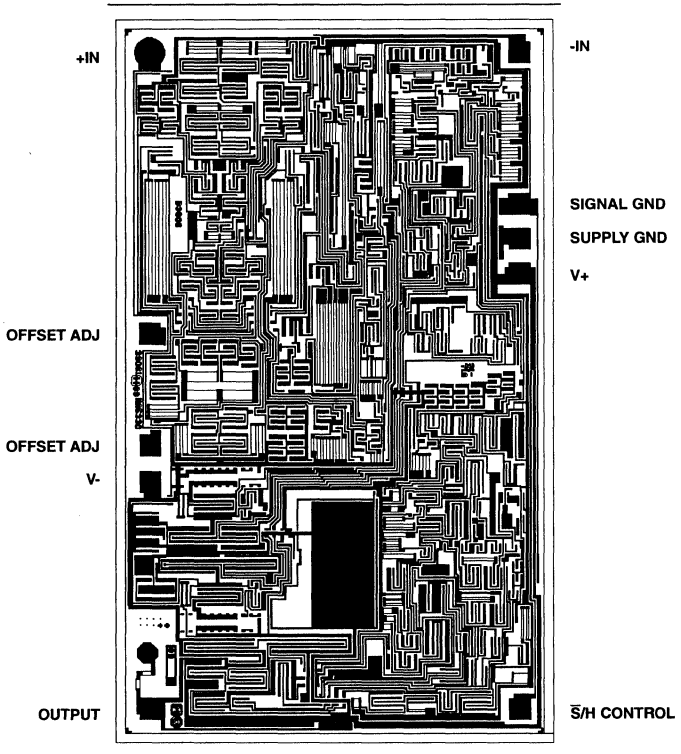
205

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5330



HARRIS SEMICONDUCTOR

HA-5340

700ns, Low Distortion, Precision Sample and Hold Amplifier

November 1996

Features

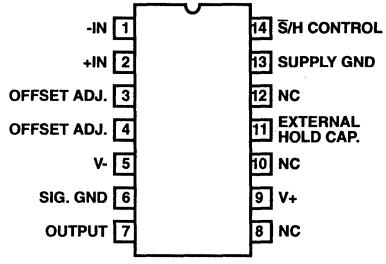
- Fast Acquisition Time (0.01%) 700ns
- Fast Hold Mode Settling Time (0.01%) 200n
- Low Distortion (Hold Mode) . . . . . -72dBc
- (V_{IN} = 200kHz, f_S = 450kHz, $5V_{P-P}$)
- Bandwidth Minimally Affected By External C_H
- Fully Differential Analog Inputs
- Built-In 135pF Hold Capacitor
- Pin Compatible with HA-5320

Applications

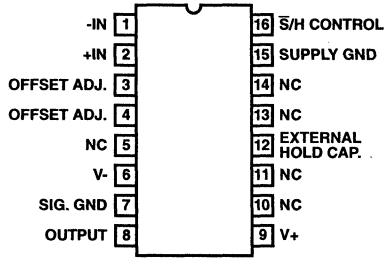
- High Bandwidth Precision Data Acquisition Systems
- Inertial Navigation and Guidance Systems
- Ultrasonics
- SONAR
- RADAR

Pinouts

HA-5340
(PDIP, CERDIP)
TOP VIEW



HA-5340
(SOIC)
TOP VIEW



Description

The HA-5340 combines the advantages of two sample/ hold architectures to create a new generation of monolithic sample/hold. High amplitude, high frequency signals can be sampled with very low distortion being introduced. The combination of exceptionally fast acquisition time and specified/characterized hold mode distortion is an industry first. Additionally, the AC performance is only minimally affected by additional hold capacitance.

To achieve this level of performance, the benefits of an integrating output stage have been combined with the advantages of a buffered hold capacitor. To the user this translates to a front-end stage that has high bandwidth due to charging only a small capacitive load and an output stage with constant pedestal error which can be nulled out using the offset adjust pins. Since the performance penalty for additional hold capacitance is low, the designer can further minimize pedestal error and droop rate without sacrificing speed.

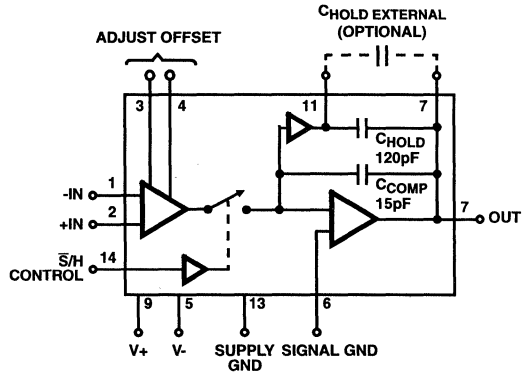
Low distortion, fast acquisition, and low droop rate are the result, making the HA-5340 the obvious choice for high speed, high accuracy sampling systems.

For a Military temperature range version request the HA-5340/883 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA1-5340-5	0 to 75	14 Ld CERDIP	F14.3
HA1-5340-9	-40 to 85	14 Ld CERDIP	F14.3
HA3-5340-5	0 to 75	14 Ld PDIP	E14.3
HA3-5340-9	-40 to 85	14 Ld PDIP	E14.3
HA9P5340-5	0 to 75	16 Ld SOIC	M16.3

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2859.2**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
Differential Input Voltage. 24V
Digital Input Voltage . . . . . +8V, -6V
Output Current, Continuous . . . . . ±20mA

Operating Conditions

Temperature Range
HA-5340-9. . . . . -40°C to 85°C
HA-5340-5. . . . . 0°C to 75°C
Supply Voltage Range (Typical) . . . . . ±12V to ±18V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	66	16
PDIP Package	90	N/A
SOIC Package	95	N/A

Maximum Junction Temperature (Ceramic Package, Note 1) . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation must be designed to maintain the junction temperature below 175°C for the ceramic package, and below 150°C for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2kΩ, C_L = 60pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5340-9, HA-5340-5			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Input Voltage Range		Full	-10	-	+10	V
Input Resistance (Note 3)		25	-	1	-	MΩ
Input Capacitance		25	-	-	3	pF
Input Offset Voltage		25	-	-	1.5	mV
		Full	-	-	3.0	mV
Offset Voltage Temperature Coefficient		Full	-	-	30	µV/°C
Bias Current		25	-	±70	-	nA
		Full	-	-	±350	nA
Offset Current		25	-	±50	-	nA
		Full	-	-	±350	nA
Common Mode Range		Full	-10	-	+10	V
CMRR	±10V, Note 4	25	-	83	-	dB
		Full	72	-	-	dB
TRANSFER CHARACTERISTICS						
Gain	DC	25	110	140	-	dB
Gain Bandwidth Product	C_H External = 0pF	Full	-	10	-	MHz
	C_H External = 100pF	Full	-	9.6	-	MHz
	C_H External = 1000pF	Full	-	6.7	-	MHz
TRANSIENT RESPONSE						
Rise Time	200mV Step	25	-	20	30	ns
Overshoot	200mV Step	25	-	35	50	%
Slew Rate	10V Step	25	40	60	-	V/µs
DIGITAL INPUT CHARACTERISTICS						
Input Voltage	V_{IH}	Full	2.0	-	-	V
	V_{IL}	Full	-	-	0.8	V
Input Current	V_{IL} = 0V	Full	-	7	40	µA
	V_{IH} = 5V	Full	-	4	40	µA

Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2kΩ, C_L = 60pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5340-9, HA-5340-5			UNITS
			MIN	TYP	MAX	
OUTPUT CHARACTERISTICS						
Output Voltage		Full	-10	-	+10	V
Output Current		Full	-10	-	+10	mA
Full Power Bandwidth (Note 5)		Full	0.6	0.9	-	MHz
Output Resistance	Hold Mode	25	-	0.05	0.1	Ω
		Full	-	0.07	0.15	Ω
Total Output Noise DC to 10MHz	Sample Mode	25	-	325	400	μV_{RMS}
	Hold Mode	25	-	325	400	μV_{RMS}
DISTORTION CHARACTERISTICS						
SAMPLE MODE Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = 200kHz, $20V_{P-P}$	Full	-	115	-	dB
Total Harmonic Distortion	V_{IN} = 200kHz, $5V_{P-P}$	Full	-90	-100	-	dBc
	V_{IN} = 200kHz, $10V_{P-P}$	Full	-76	-82	-	dBc
	V_{IN} = 200kHz, $20V_{P-P}$	Full	-70	-74	-	dBc
	V_{IN} = 500kHz, $5V_{P-P}$	Full	-66	-75	-	dBc
Intermodulation Distortion	V_{IN} = $10V_{P-P}$, f_1 = 20kHz, f_2 = 21kHz	Full	-78	-83	-	dBc
HOLD MODE (50% Duty Cycle S/H) Signal to Noise Ratio (RMS Signal to RMS Noise) f_S = 450kHz	V_{IN} = 200kHz, $5V_{P-P}$	25	-	76	-	dB
	V_{IN} = 200kHz, $10V_{P-P}$	25	-	76	-	dB
Total Harmonic Distortion f_S = 450kHz	V_{IN} = 200kHz, $5V_{P-P}$	25	-	-72	-	dBc
	V_{IN} = 200kHz, $10V_{P-P}$	25	-	-66	-	dBc
	V_{IN} = 200kHz, $20V_{P-P}$	25	-	-56	-	dBc
f_S = 450kHz	V_{IN} = 100kHz, $5V_{P-P}$	25	-	-84	-	dBc
	V_{IN} = 100kHz, $10V_{P-P}$	25	-	-71	-	dBc
	V_{IN} = 100kHz, $20V_{P-P}$	25	-	-61	-	dBc
$f_S = 2f_{IN}$(Nyquist)	V_{IN} = 20kHz, $5V_{P-P}$	25	-	-95	-	dBc
	V_{IN} = 50kHz, $5V_{P-P}$	25	-	-91	-	dBc
	V_{IN} = 100kHz, $5V_{P-P}$	25	-	-82	-	dBc
Intermodulation Distortion f_S = 450kHz	V_{IN} = $10V_{P-P}$ (f_1 = 20kHz, f_2 = 21kHz)	25	-	-79	-	dBc
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time	10V Step to 0.01%	25	-	700	-	ns
		Full	-	-	900	ns
	10V Step to 0.1%	25	-	430	600	ns
Droop Rate	C_H = Internal	25	-	0.1	-	μV/μs
		Full	-	-	95	μV/μs
Hold Step Error	V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns	25	-	15	-	mV
Hold Mode Settling Time	To ±1mV	Full	-	200	300	ns
Hold Mode Feedthrough	$20V_{P-P}$, 200kHz, Sine	Full	-	-76	-	dB
EADT (Effective Aperture Delay Time)		25	-	-15	-	ns

Electrical Specifications $V_{SUPPLY} = \pm 15.0V$; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), $R_L = 2k\Omega$, C_L = 60pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5340-9, HA-5340-5			UNITS
			MIN	TYP	MAX	
Aperture Uncertainty		25	-	0.2	-	ns
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current		Full	-	19	25	mA
Negative Supply Current		Full	-	19	25	mA
PSRR	10% Delta	Full	75	82	-	dB

NOTES:

3. Derived from Computer Simulation only, not tested.
4. +CMRR is measured from 0V to +10V, -CMRR is measured from 0V to -10V.
5. Based on the calculation FPBW = Slew Rate/$2\pi V_{PEAK}$ (V_{PEAK} = 10V).

Test Circuits and Waveforms

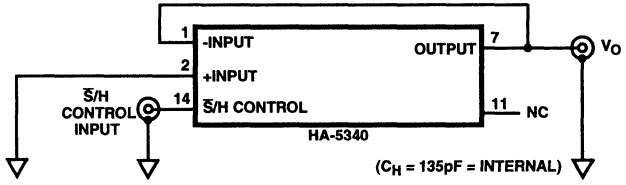
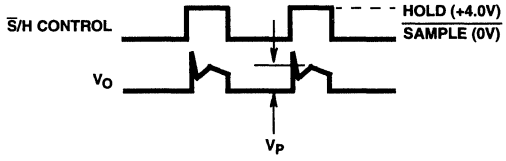


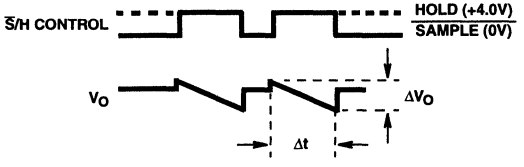
FIGURE 1. HOLD STEP ERROR AND DROOP RATE



NOTE:

6. Observe the "hold step" voltage V_P.

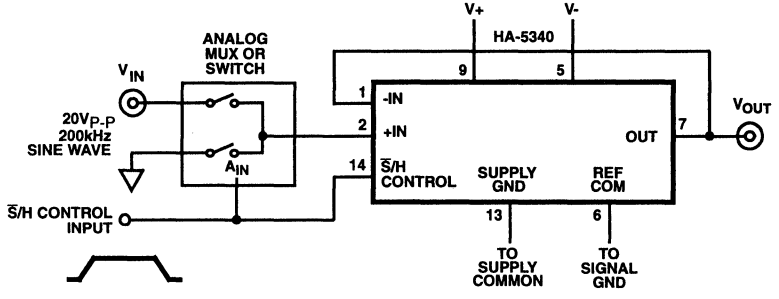
FIGURE 2. HOLD STEP ERROR



NOTES:

7. Observe the voltage "droop", $\Delta V_O/\Delta t$.
8. Measure the slope of the output during hold, $\Delta V_O/\Delta t$.
9. Droop can be positive or negative - usually to one rail or the other not to GND.

FIGURE 3. DROOP RATE TEST



NOTE:

10. Feedthrough in

$$dB = 20\log\frac{V_{OUT}}{V_{IN}}$$ where:

$V_{OUT} = V_{P-P}$, Hold Mode,
$V_{IN} = V_{P-P}$

FIGURE 4. HOLD MODE FEED THROUGH ATTENUATION

Application Information

The HA-5340 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note AN517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01µF to 0.1µF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. GND) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5340 includes a 135pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Teflon®, polystyrene and polypropylene dielectric capacitor types offer good performance over the specified operating temperature range.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

®Teflon is a registered Trademark of Dupont Corporation.

Typical Application

Figure 5 shows the HA-5340 connected as a unity gain non-inverting amplifier - its most widely used configuration. As an input device for a fast successive - approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5340's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The HA-5340 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

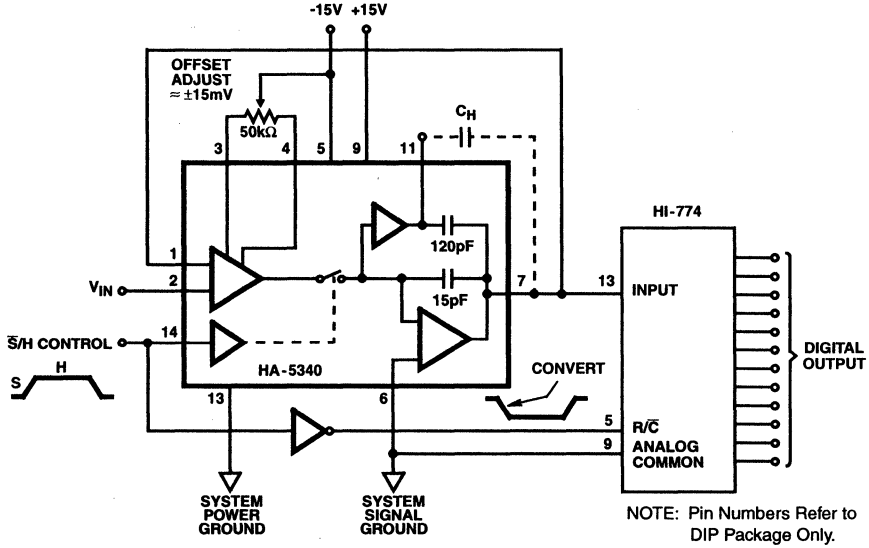


FIGURE 5. TYPICAL HA-5340 CONNECTIONS; NONINVERTING UNITY GAIN MODE

Typical Performance Curves $T_A = 25^oC$, $V_S = \pm15V$, Unless Otherwise Specified

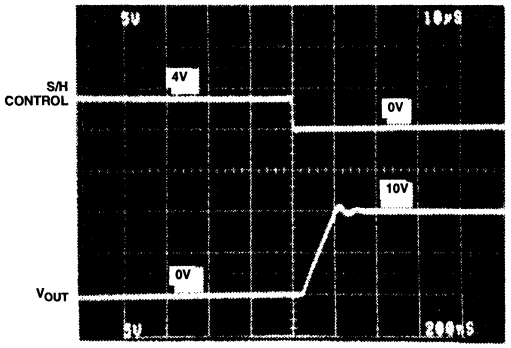


FIGURE 6. T_{ACQ} POS 0 TO +10 STEP

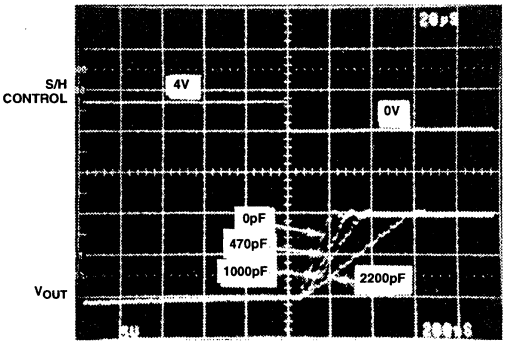


FIGURE 7. T_{ACQ} vs ADDITIONAL C_H

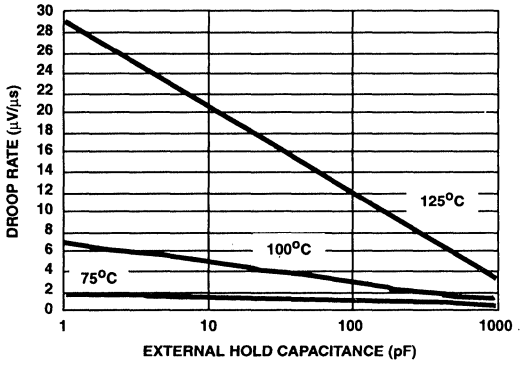


FIGURE 8. DROOP RATE vs HOLD CAPACITANCE

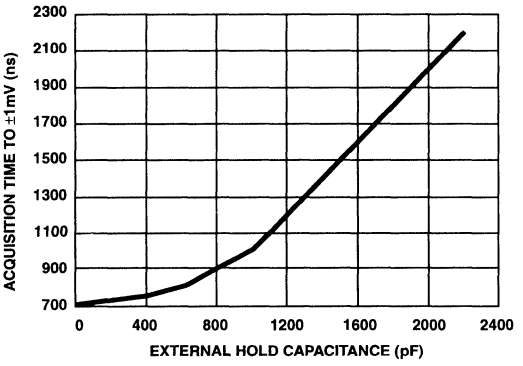


FIGURE 9. ACQUISITION TIME (0.01%) vs HOLD CAPACITANCE

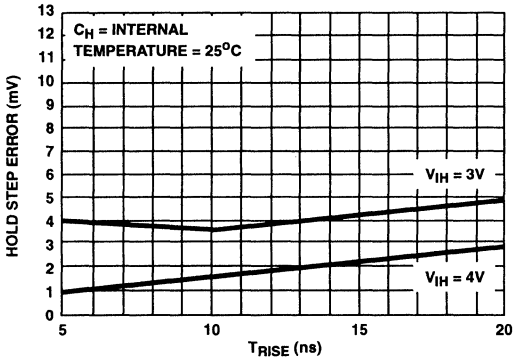


FIGURE 10. HOLD STEP ERROR vs T_{RISE}

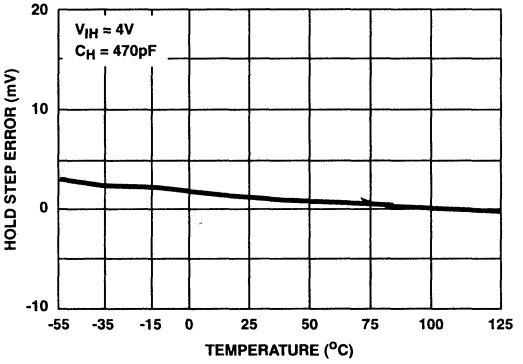


FIGURE 11. HOLD STEP ERROR vs TEMPERATURE

Typical Performance Curves $T_A = 25^oC$, $V_S = \pm15V$, Unless Otherwise Specified (Continued)

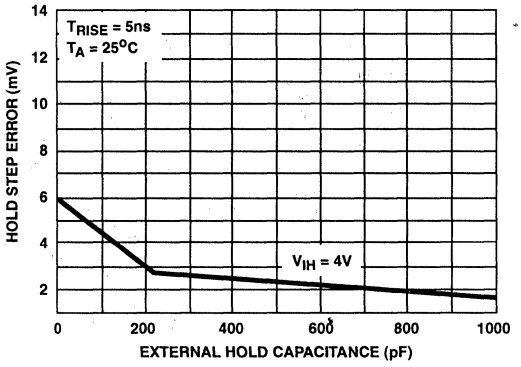


FIGURE 12. HOLD STEP ERROR vs HOLD CAPACITANCE

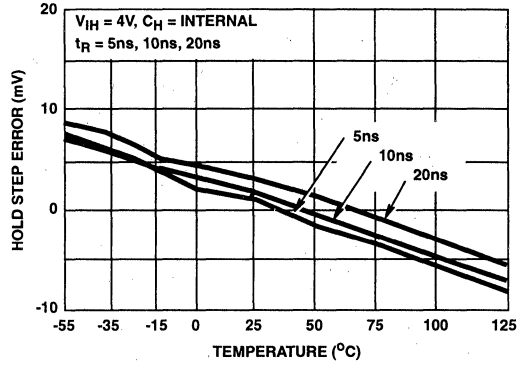
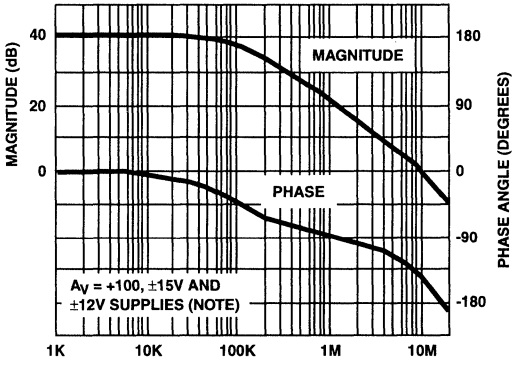


FIGURE 13. HOLD STEP ERROR vs TEMPERATURE



NOTE: ±15V and ±12V supplies trace the same line within the width of the line, therefore only one line is shown.

FIGURE 14. CLOSED LOOP PHASE/GAIN

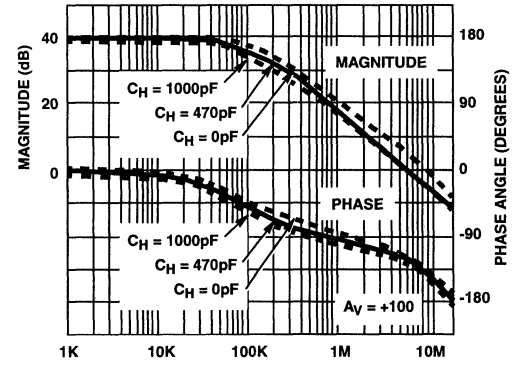


FIGURE 15. CLOSED LOOP PHASE/GAIN

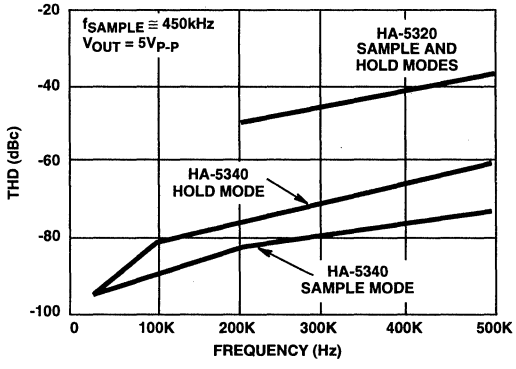


FIGURE 16. THD vs FREQUENCY

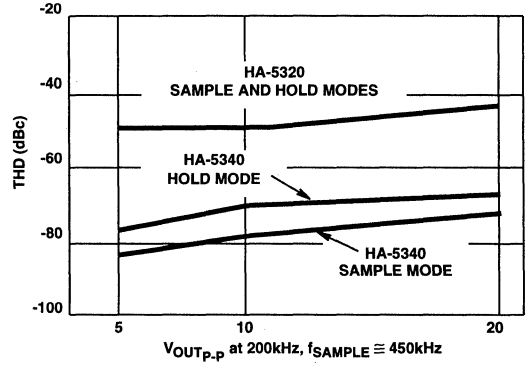


FIGURE 17. THD vs V_{OUT}

Die Characteristics

DIE DIMENSIONS:

84mils x 139mils x 19mils

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ± 2.0kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

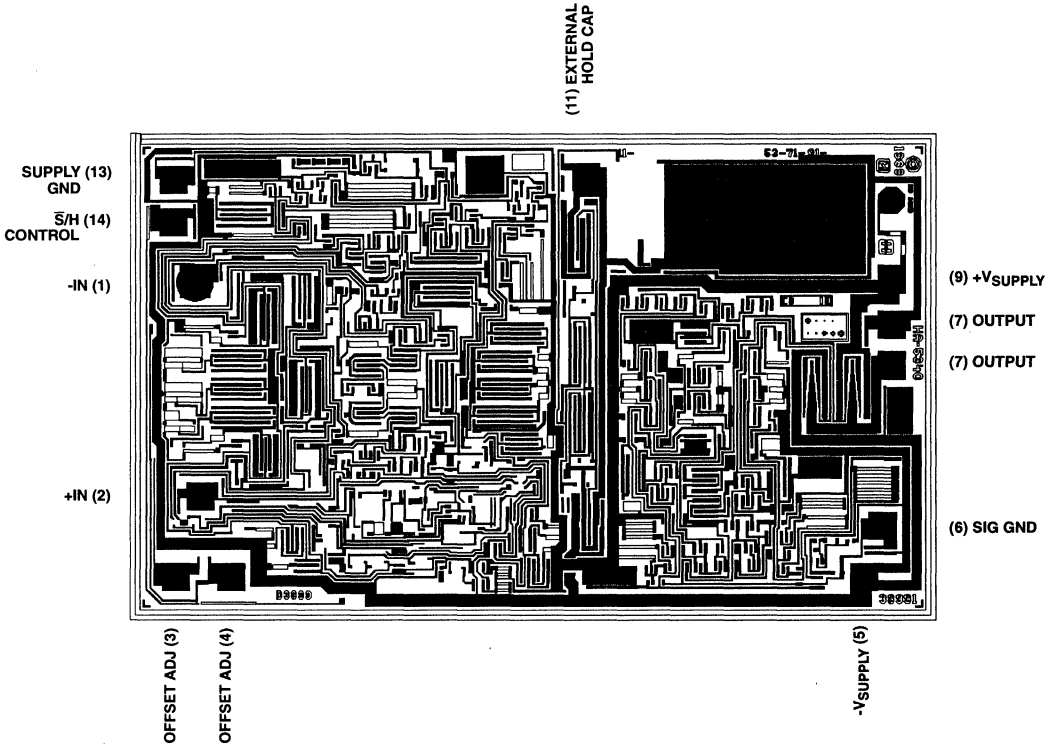
V-

TRANSISTOR COUNT:

196

Metallization Mask Layout

HA-5340



HARRIS SEMICONDUCTOR

HA5351

November 1996

64ns Sample and Hold Amplifier

Features

- Fast Acquisition to 0.01% . . . . . 70ns (Max)
- Low Offset Error . . . . . ±2mV (Max)
- Low Pedestal Error . . . . . ±10mV (Max)
- Low Droop Rate . . . . . 2μV/μs (Max)
- Wide Unity Gain Bandwidth 40MHz
- Low Power Dissipation . . . . . 220mW (Max)
- Total Harmonic Distortion (Hold Mode) . . . . . -72dBc (V_{IN} = $5V_{P-P}$ at 1MHz)
- Fully Differential Inputs
- On Chip Hold Capacitor

Applications

- Synchronous Sampling
- Wide Bandwidth A/D Conversion
- Deglitching
- Peak Detection
- High Speed DC Restore

Description

The HA5351 is a fast acquisition, wide bandwidth sample and hold amplifier, built with the Harris HBC-10 BiCMOS process. This sample and hold amplifier offers a combination of desirable features; fast acquisition time (70ns to 0.01% maximum), excellent DC precision and extremely low power dissipation, making it ideal for use in systems that sample multiple signals and require low power. For systems with multiple channels, consider the Dual HA5352 sample and hold amplifier.

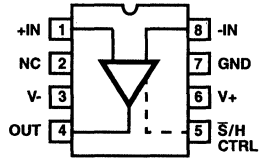
The HA5351 is in an open loop configuration with fully differential inputs providing flexibility for user defined feedback. In unity gain the HA5351 is completely self-contained and requires no external components. The on-chip 15pF hold capacitor is completely isolated to minimizing droop rate and reduce sensitivity to pedestal error. The HA5351 is available in 8 lead PDIP and SOIC packages for minimizing board space and ease of layout.

Ordering Information

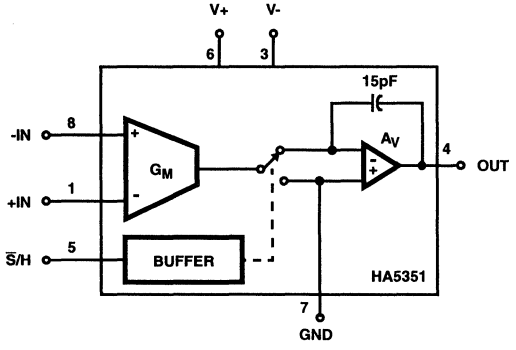
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA5351IP	-40 to 85	8 Ld PDIP	E8.3
HA5351IB	-40 to 85	8 Ld SOIC	M8.15

Pinout

HA5351
(PDIP, SOIC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1996

File Number **3690.5**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals . . . . . +11V
Differential Input Voltage. 6V
Voltage Between Sample and Hold Control and Ground . . . . .+5.5V
Output Current, Continuous . . . . . ±37mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PDIP Package 120
SOIC Package 160
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA5351I			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Input Voltage Range		Full	-2.5	-	+2.5	V
Input Resistance (Note 2)		25	100	500	-	kΩ
Input Capacitance		25	-	-	5	pF
Input Offset Voltage		25	-2	-	2	mV
		Full	-3.0	-	3.0	mV
Offset Voltage Temperature Coefficient		Full	-	15	-	µV/°C
Bias Current		Full	-	2.5	5	µA
Offset Current		Full	-1.5	-	+1.5	µA
Common Mode Range		Full	-2.5	-	+2.5	V
Common Mode Rejection	±2.5V, Note 3	Full	60	80	-	dB
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	V_{OUT} = ±2.5V	25	95	108	-	dB
		Full	85	-	-	dB
Unity Gain -3dB Bandwidth		25	-	40	-	MHz
TRANSIENT RESPONSE						
Rise Time	200mV Step	25	-	8.5	-	ns
Overshoot	200mV Step	25	0	-	30	%
Slew Rate	5V Step	Full	88	105	-	V/µs
DIGITAL INPUT CHARACTERISTICS						
Input Voltage	V_{IH}	25, 85	2.1	-	5.0	V
		-40	2.4	-	5.0	V
	V_{IL}	Full	0	-	0.8	V
Input Current	V_{IL} = 0V	Full	-1.0	-	1.0	µA
	V_{IH} = 5V	Full	-1.0	-	1.0	µA
OUTPUT CHARACTERISTICS						
Output Voltage	R_L = 510Ω	Full	-3.0	-	+3.0	V
Output Current	R_L = 100Ω	25, 85	20	25	-	mA
		-40	15	-	-	mA

Electrical Specifications Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA5351I			UNITS
			MIN	TYP	MAX	
Full Power Bandwidth	$5V_{P-P}$, A_V = +1, -3dB	Full	-	13	-	MHz
Output Resistance	Hold Mode	25	-	0.02	-	Ω
Total Output Noise (DC to 10MHz)	Sample Mode	25	-	325	-	μV_{RMS}
	Hold Mode	25	-	325	-	μV_{RMS}
DISTORTION CHARACTERISTICS						
SAMPLE MODE						
Total Harmonic Distortion	$V_{IN} = 4.5V_{P-P}$, f_{IN} = 100kHz	25	-	-80	-76	dBc
	$V_{IN} = 5V_{P-P}$, f_{IN} = 1MHz	25	-	-74	-69	dBc
	$V_{IN} = 1V_{P-P}$, f_{IN} = 10MHz	25	-	-57	-52	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	$V_{IN} = 4.5V_{P-P}$, f_{IN} = 100kHz	25	-	73	-	dB
HOLD MODE (50% Duty Cycle S/H)						
Total Harmonic Distortion	$V_{IN} = 4.5V_{P-P}$, f_{IN} = 100kHz, $f_S \cong$ 100kHz	25	-	-78	-74	dBc
	$V_{IN} = 5V_{P-P}$, f_{IN} = 1MHz, $f_S \cong$ 1MHz	25	-	-72	-67	dBc
	$V_{IN} = 1V_{P-P}$, f_{IN} = 10MHz, $f_S \cong$ 1MHz	25	-	-51	-47	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	$V_{IN} = 4.5V_{P-P}$, f_{IN} = 100kHz, $f_S \cong$ 100kHz	25	-	70	-	dB
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time	0V to 2.0V Step to ±1mV	25	-	53	-	ns
	0V to 2.0V Step to 0.01% (±200μV)	25	-	64	70	ns
	-2.5V to +2.5V Step to 0.01% (±500μV)	25	-	90	100	ns
Droop Rate		25	-	0.3	-	μV/μs
		Full	-2	-	2	μV/μs
Hold Step Error	V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns	Full	-10	-	+10	mV
Hold Mode Settling Time	To ±1mV	25	-	50	-	ns
Hold Mode Feedthrough	$5V_{P-P}$, 500kHz, Sine	25	-	72	-	dB
EADT (Effective Aperture Delay Time)		25	-	+1	-	ns
Aperture Time (Note 2)		25	-	10	-	ns
Aperture Uncertainty		25	-	10	20	ps
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current		Full	-	20	22	mA
Negative Supply Current		Full	-	20	22	mA
PSRR	10% Delta	Full	60	74	-	dB

NOTES:

2. Derived from Computer Simulation only, not tested.
3. +CMRR is measured from 0V to +2.5V, -CMRR is measured from 0V to -2.5V.

Typical Performance Curves

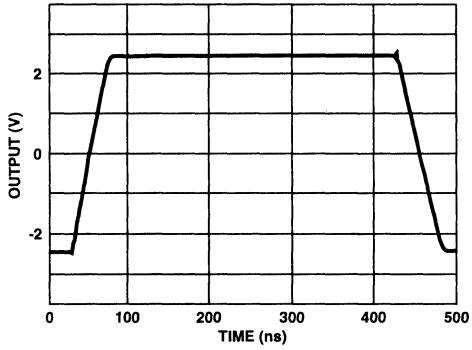


FIGURE 1. LARGE SIGNAL RESPONSE

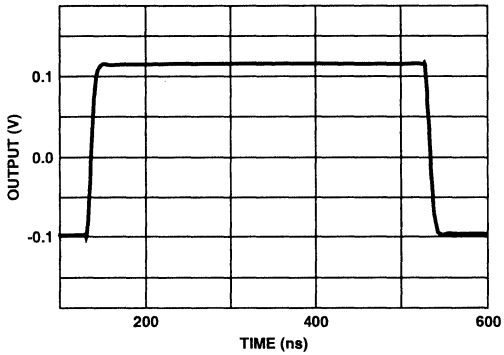


FIGURE 2. SMALL SIGNAL RESPONSE

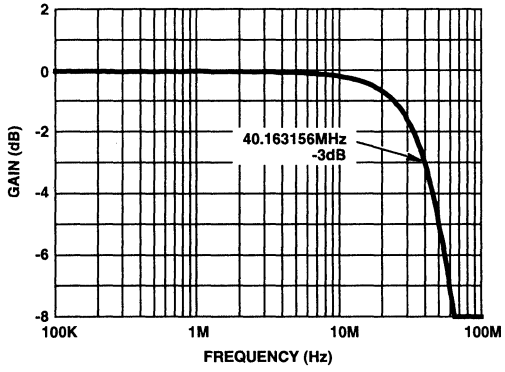


FIGURE 3. UNITY GAIN FREQUENCY RESPONSE

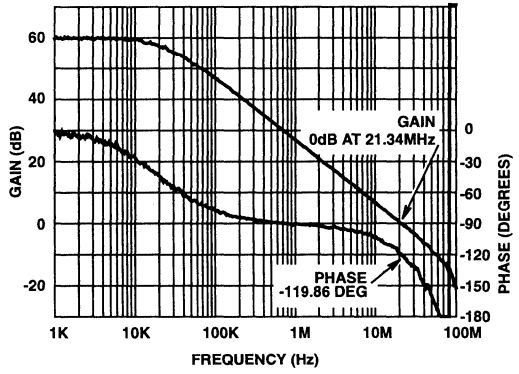


FIGURE 4. CLOSED LOOP GAIN/PHASE A_V = +1000

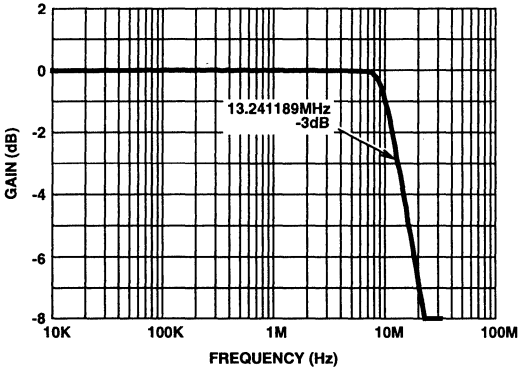


FIGURE 5. $5V_{P-P}$ FULL POWER FREQUENCY RESPONSE

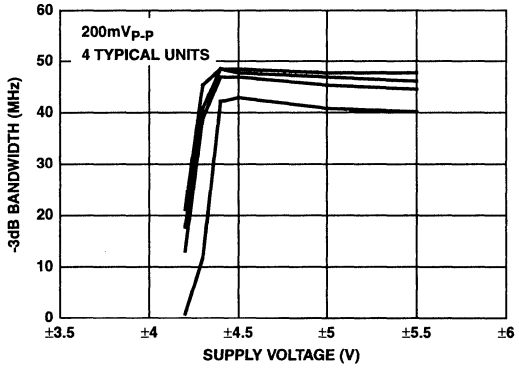


FIGURE 6. -3dB BANDWIDTH vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

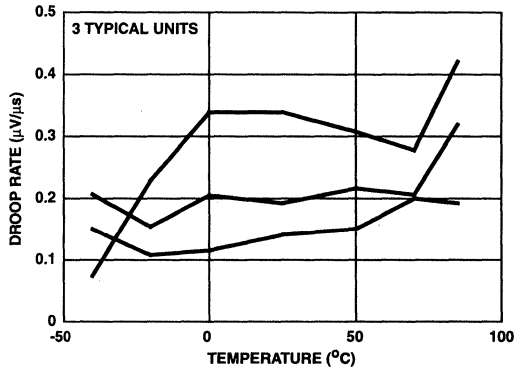


FIGURE 7. DROOP RATE vs TEMPERATURE

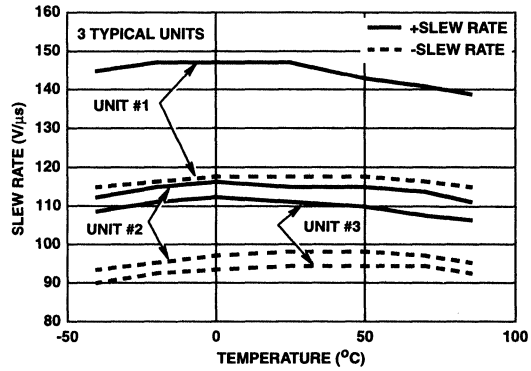


FIGURE 8. SLEW RATE vs TEMPERATURE

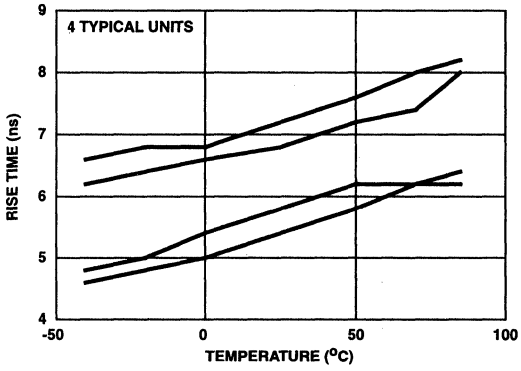


FIGURE 9. RISE TIME vs TEMPERATURE

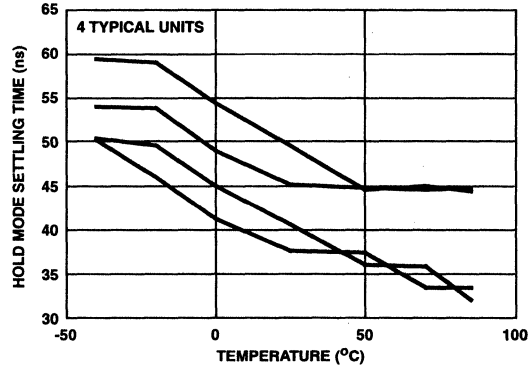


FIGURE 10. HOLD MODE SETTLING vs TEMPERATURE

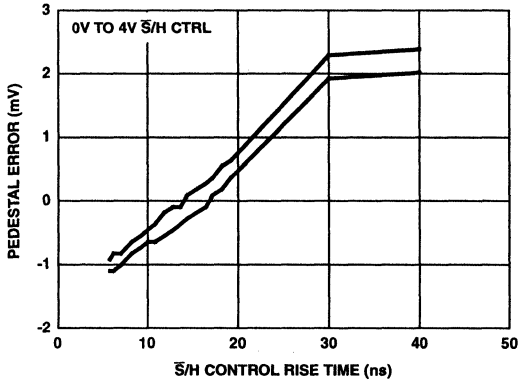


FIGURE 11. PEDESTAL vs S/H CONTROL RISE TIME

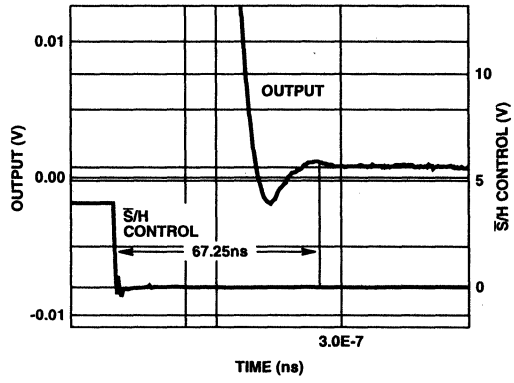


FIGURE 12. ACQUISITION TIME (0.01%, 0V TO 2V STEP)

Typical Performance Curves (Continued)

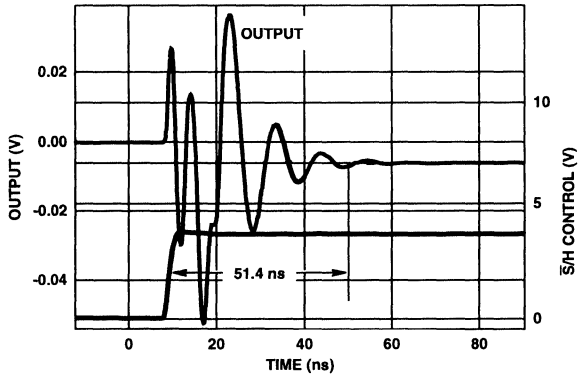


FIGURE 13. HOLD MODE SETTLING TIME (±200μV)

Die Characteristics

DIE DIMENSIONS:

2530µm x 1760µm x 525µm
100 mils x 69 mils x 19 mils

METALLIZATION:

Type: Metal 1: AlSiCu/TiW
Thickness: Metal 1: 6kÅ ±750Å

Type: Metal 2: AlSiCu
Thickness: Metal 2: 16kÅ ±1.1kÅ

PASSIVATION:

Type: Sandwich Passivation
Nitride - 4kÅ, Undoped Si Glass (USG) - 8kÅ,
Total - 12kÅ ±2kÅ

SUBSTRATE POTENTIAL:

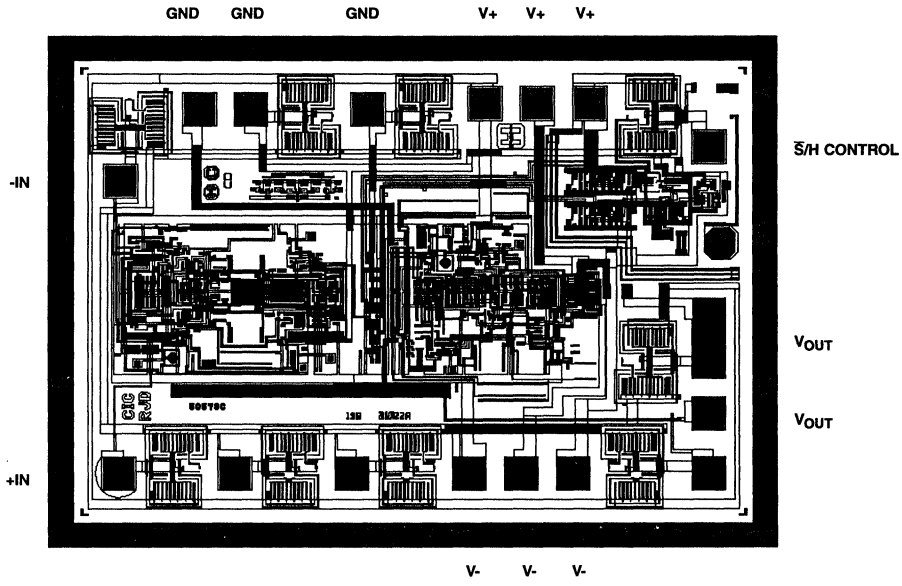
V-

TRANSISTOR COUNT:

156

Metallization Mask Layout

HA5351



LINEAR 6

VIDEO CROSSPOINT SWITCHES

Selection Guide

VIDEO CROSSPOINT SWITCHES: Typical Values at 25°C, Unless Otherwise Specified

(NOTE 2) DEVICE	FEATURES	DIF. GAIN (%)	DIF. PHASE (DEG)	0.1dB FLAT GAIN (MHz)	BW (MHz)	SLEW RATE (V/µs)	10MHz CROSSTALK (dB)	SUPPLY VOLTAGE RANGE (±V)	SUPPLY CURRENT (mA)
CROSSPOINT SWITCHES									
HA4600	**1 x 1**	**0.01**	**0.01**	**250**	**480**	**1700**	**-85** (Note 1)	**4.5 - 5.5**	**10.5**
HA4201	**1 x 1 with Tally Output**	**0.01**	**0.01**	**250**	**480**	**1700**	**-85** (Note 1)	**4.5 - 5.5**	**10.5**
HA4244	**1 x 1 with Latched Control Signal**	**0.01**	**0.01**	**250**	**480**	**1700**	**-85** (Note 1)	**4.5 - 5.5**	**10.5**
HA4314B	**4 x 1**	**0.01**	**0.01**	**100**	**400**	**1400**	**-90**	**4.5 - 5.5**	**10.5**
HA4404B	**4 x 1 with Tally Outputs**	**0.01**	**0.01**	**165**	**330**	**1250**	**-90**	**4.5 - 5.5**	**10.5**
HA4344B	**4 x 1 with Latched Control Signals**	**0.01**	**0.01**	**150**	**350**	**1400**	**-90**	**4.5 - 5.5**	**10.5**
HA455	**High Performance 8 x 8, A_V = +1**	**0.02**	**0.02**	**TBD**	**130**	**250**	**-60**	**4.5 - 5.5**	**88**
HA456	**Low Power 8 x 8, A_V = +1**	**0.04**	**0.20**	**TBD**	**80**	**170**	**-60**	**4.5 - 5.5**	**56**
HA457	**High Performance 8 x 8, A_V = +2**	**0.01**	**0.02**	**TBD**	**170**	**350**	**-60**	**4.5 - 5.5**	**88**

NOTES:

1. Off Isolation at 100MHz.
2. Bold type indicates a new product from Harris.

HARRIS SEMICONDUCTOR

HA4201

480MHz, 1 x 1 Video Crosspoint Switch with Tally Output

November 1996

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1700V/μs
- 0.1dB Gain Flatness..... 250MHz
- Off Isolation (100MHz)..... 85dB
- Differential Gain..... 0.01%
- Differential Phase..... 0.01 Degrees
- High ESD Rating ..... >2000V
- TTL Compatible Enable Input
- Open Collector Tally Output
- Improved Replacement for GX4201

Applications

- Professional Video Switching and Routing
- Video Multiplexers
- HDTV
- Computer Graphics
- RF Switching and Routing
- PCM Data Routing

Description

The HA4201 is a very wide bandwidth 1 x 1 crosspoint switch ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation (105mW Enabled, 1mW Disabled), excellent differential gain and phase, and very high off isolation. When disabled, the output is switched to a high impedance state, making the HA4201 ideal for routing matrix equipment.

The HA4201 requires no external current source, and features fast switching and symmetric slew rates. The tally output is an open collector PNP transistor to V_{CC}, and is activated whenever EN = 1 to provide an indication of crosspoint selection.

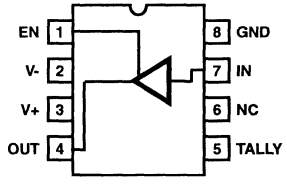
For applications which don't require a Tally output, please refer to the HA4600 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA4201CP	0 to 70	8 Ld PDIP	E8.3
HA4201CB (4201CB)	0 to 70	8 Ld SOIC	M8.15

Pinout

HA4201
(PDIP, SOIC)
TOP VIEW



Truth Table

EN	OUT	TALLY
0	High Z	Off
1	Active	On

6 VIDEO CROSS-POINT SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 3680.3

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage..... V_{SUPPLY}
Digital Input Current (Note 2) ..... ±25mA
Output Current 20mA

Operating Conditions

Temperature Range ..... 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Die)..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s)..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to this maximum value.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, V_{EN} = 2.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	V_{EN} = 2.0V	25, 70	-	10.5	13	mA
	V_{EN} = 2.0V	0	-	-	14.5	mA
	V_{EN} = 0.8V	25, 70	-	100	115	µA
	V_{EN} = 0.8V	0	-	100	125	µA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping	$V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$	25, 70	±2.7	±2.8	-	V
		0	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	µA
Output Offset Voltage		25	-10	-	10	mV
Output Offset Voltage Drift (Note 3)		Full	-	25	50	µV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		25	-	160	-	ns
Turn-Off Time		25	-	320	-	ns
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
EN Input Current	V_{EN} = 0 to 4V	Full	-2	-	2	µA
Tally Output High Voltage	I_{OH} = 1mA	Full	4.7	4.8	-	V
Tally Off Leakage Current	V_{TALLY} = 0V, -5V	Full	-20	-	20	µA
AC CHARACTERISTICS						
Insertion Loss	$1V_{P-P}$	Full	-	0.04	0.05	dB
-3dB Bandwidth	R_S = 82Ω, C_L = 10pF		-	480	-	MHz
	R_S = 43Ω, C_L = 15pF	25	-	380	-	MHz
	R_S = 36Ω, C_L = 21pF	25	-	370	-	MHz

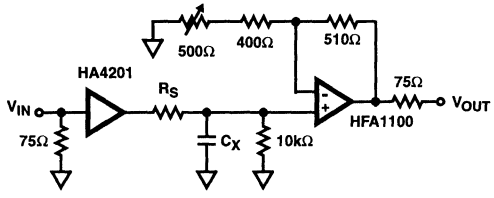
Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, V_{EN} = 2.0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
±0.1dB Flat Bandwidth	R_S = 82Ω, C_L = 10pF	25	-	250	-	MHz
	R_S = 43Ω, C_L = 15pF	25	-	175	-	MHz
	R_S = 36Ω, C_L = 21pF	25	-	170	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.0	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance	V_{EN} = 0.8V	Full	-	2.0	-	pF
Differential Gain	4.43MHz, Note 3	25	-	0.01	0.02	%
Differential Phase	4.43MHz, Note 3	25	-	0.01	0.02	Degrees
Off Isolation	1V_{P-P}, 100MHz, V_{EN} = 0.8V, R_L = 10Ω	Full	-	85	-	dB
Slew Rate (1.5V_{P-P}, +SR/-SR)	R_S = 82Ω, C_L = 10pF	25	-	1750/1770	-	V/µs
	R_S = 43Ω, C_L = 15pF	25	-	1460/1360	-	V/µs
	R_S = 36Ω, C_L = 21pF	25	-	1410/1360	-	V/µs
Total Harmonic Distortion (Note 3)		Full	-	0.01	0.1	%
Disabled Output Resistance		Full	-	12	-	MΩ

NOTE:

3. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.

AC Test Circuit



NOTE: C_L = C_X + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

Application Information

General

The HA4201 is a 1 x 1 crosspoint switch that is ideal for the matrix element in small, high input-to-output isolation switchers and routers. It also excels as an input buffer for routers with a large number of outputs (i.e. each input must connect to a large number of outputs) and delivers performance superior to most video amplifiers at a fraction of the cost. As an input buffer, the HA4201's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor. This crosspoint contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled (EN = 0).

Frequency Response

Most applications utilizing the HA4201 require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. As an example, -3dB bandwidth decreases to 160MHz for C_L = 100pF, R_S = 0Ω. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs (see Figure 2), or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

EN - The ENABLE input is a TTL/CMOS compatible, active high input. When driven low this input forces the output to a true high impedance state and reduces the power dissipation by two orders of magnitude. The EN input has no on-chip pull-up resistor, so it must be connected to a logic high (recommend V+) if the enable function isn't utilized.

Tally - The Tally output is an open collector PNP transistor connected to V+. When EN = 1, the PNP transistor is enabled and current is delivered to the load. When the crosspoint is disabled, the Tally output presents a very high impedance to the external circuitry. Several Tally outputs may be wire OR'd together to generate complex control signals, as shown with the HA4404 in the application circuits below. The Tally load may be terminated to GND or to V- as long as the continuous output current doesn't exceed 3mA (6mA at 50% duty cycle, etc.).

Switcher/Router Applications

Figure 1 illustrates one possible implementation of a wideband, low power, 4 x 4 switcher/router. A 4 x 4 switcher/router allows any of the four outputs to be driven by any one of the four inputs (e.g. each of the four inputs may connect to a different output, or an input may connect to multiple outputs). This application utilizes the HA4201 for the input buffer, the HA4404 (4 x 1 crosspoint switch) as the switch matrix, and the HFA1112 (programmable gain buffer) as the gain of two output driver. Figure 2 details a 16 x 1 switcher (basically a 16:1 mux) which uses the HA4201 in a cascaded stage configuration to minimize capacitive loading at each output node, thus increasing system bandwidth.

Power Up Considerations

No signals should be applied to the analog or digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 1 x 1 and 4 x 1 crosspoint switches. In addition to the HA4201, the 1 x 1 family includes the HA4600 which is an essentially similar device but without the Tally output. The 4 x 1 family is comprised of the HA4314, HA4404, and HA4344. The HA4314 is a 14 lead basic 4 x 1 crosspoint. The HA4404 is a 16 lead device with Tally outputs to indicate the selected channel. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, $\overline{CS}$). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

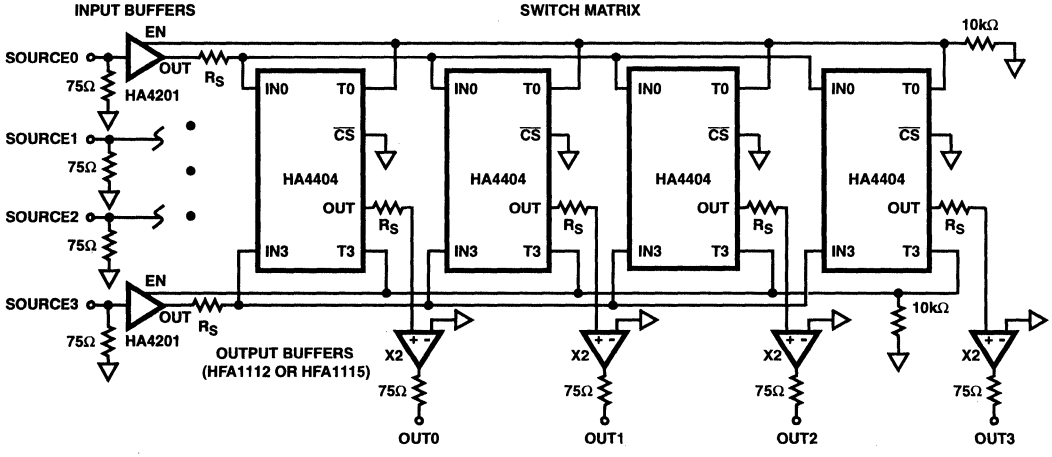


FIGURE 1. 4 x 4 SWITCHER/ROUTER APPLICATION

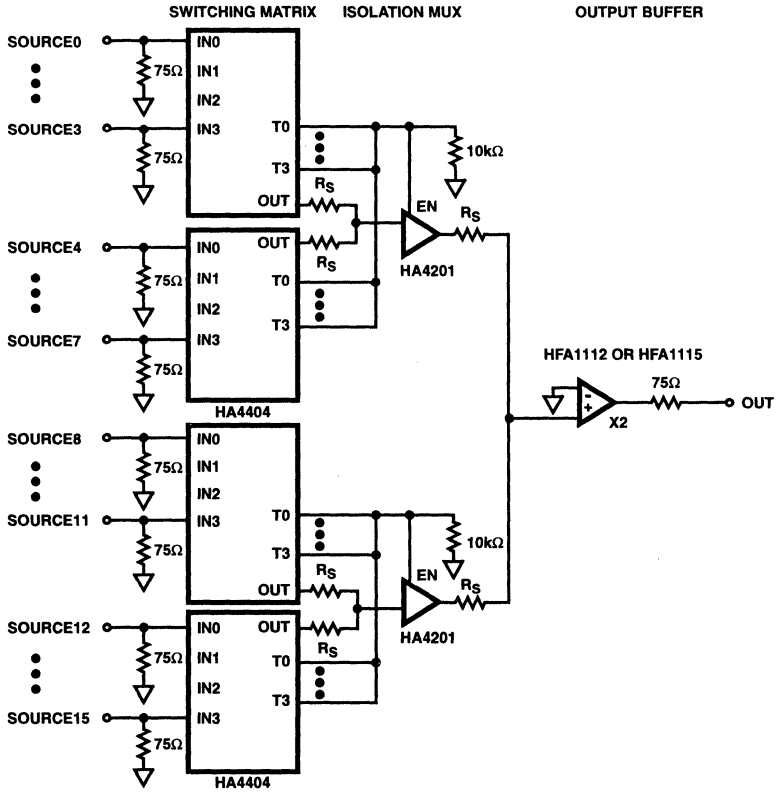


FIGURE 2. 16 x 1 SWITCHER APPLICATION

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 10kΩ, Unless Otherwise Specified

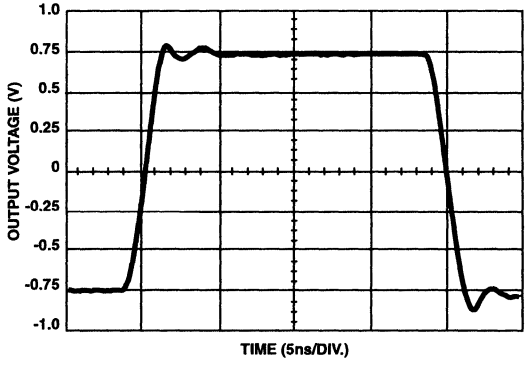


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

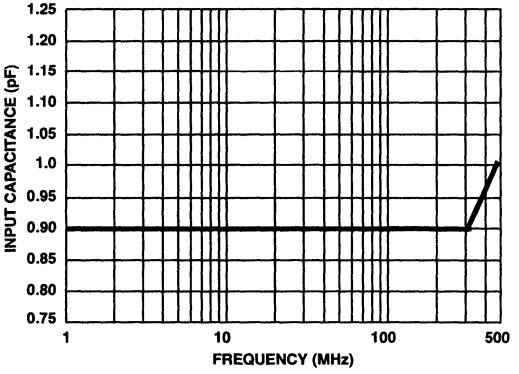


FIGURE 4. INPUT CAPACITANCE vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified (Continued)

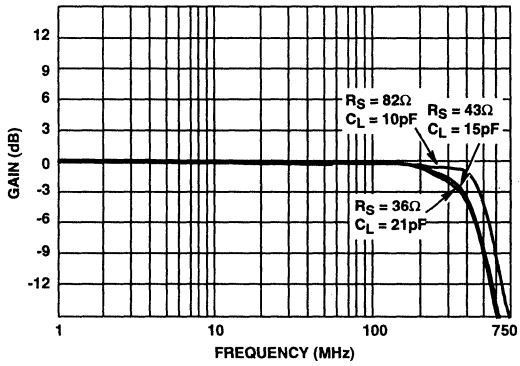


FIGURE 5. FREQUENCY RESPONSE

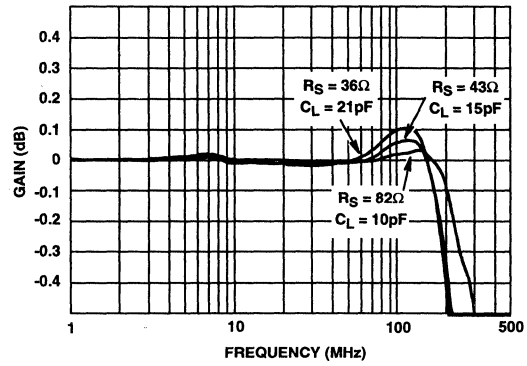


FIGURE 6. GAIN FLATNESS

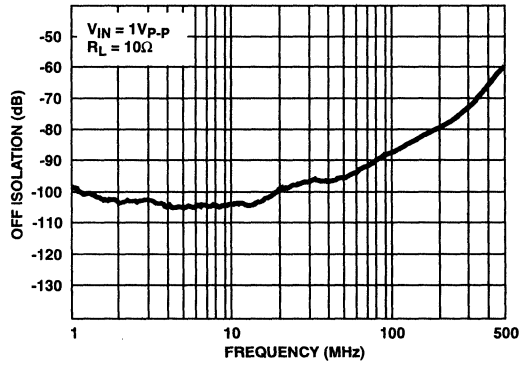


FIGURE 7. OFF ISOLATION

Die Characteristics

DIE DIMENSIONS:

51 mils x 36 mils x 19 mils
1290µm x 910µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)/TiW
Thickness: Metal 1: 6kÅ ±0.8kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±1.1kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

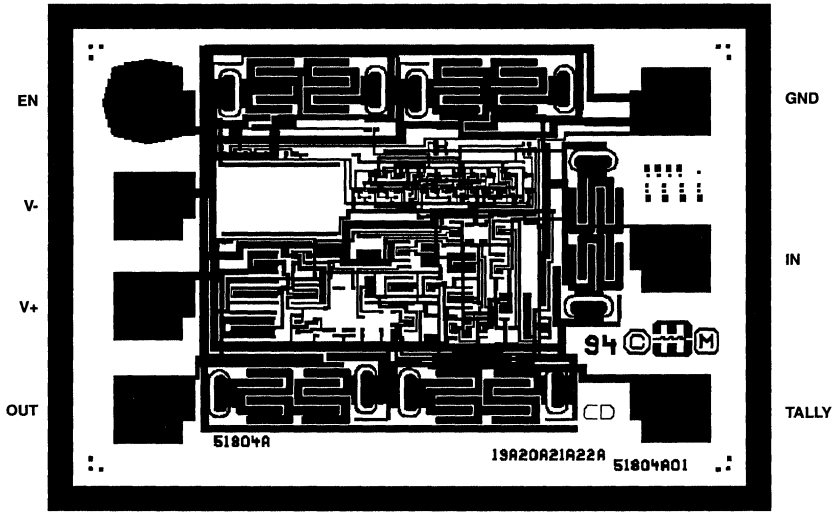
53

SUBSTRATE POTENTIAL (Powered Up):

V-

Metallization Mask Layout

HA4201



HARRIS SEMICONDUCTOR

HA4244

480MHz, 1 x 1 Video Crosspoint Switch with Synchronous Enable

November 1996

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1700V/μs
- 0.1dB Gain Flatness..... 250MHz
- -3dB Bandwidth 480MHz
- Off Isolation (100MHz)..... 85dB
- Differential Gain and Phase ..... 0.01%/0.01 Degrees
- High ESD Rating ..... >2000V
- TTL Compatible Control Signals
- Latched Enable Input for Synchronous Switching
- Powers-Up in Disabled State; Avoids Bus Contention

Applications

- Professional Video Switching and Routing
- Video Multiplexers
- Computer Graphics
- RF Switching and Routing
- PCM Data Routing

Description

The HA4244 is a very wide bandwidth 1 x 1 crosspoint switch ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation, excellent differential gain and phase, high off isolation, symmetric slew rates, fast switching, and a latched enable signal. When disabled, the output is switched to a high impedance state, making the HA4244 ideal for routing matrix equipment.

The latched enable input allows for synchronized channel switching. When CLK is low the master control latch loads the next EN, while the closed slave control latch maintains the crosspoint in its current state. CLK switching high closes the master latch, loads the now open slave latch, and enables or disables the HA4244 according to the current state of the EN input.

This crosspoint's design ensures that it powers up in the disabled state to eliminate bus contention concerns, and to minimize supply current draw at power up.

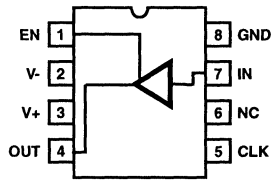
For applications requiring an asynchronous crosspoint switch, please refer to the HA4201 and HA4600 data sheets.

Ordering Information

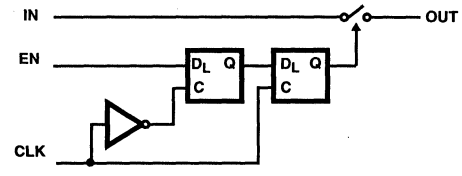
PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HA4244CB (H4244C)	0 to 70	8 Ld SOIC	M8.15

Pinout

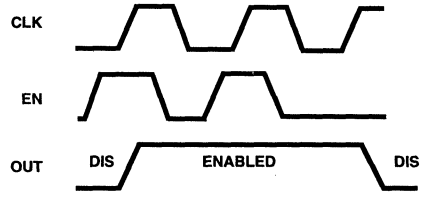
HA4244
(SOIC)
TOP VIEW



Functional Diagram



Timing Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **4078.1**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage ..... V_{SUPPLY}
Digital Input Current (Note 2) ..... ±25mA
Output Current 20mA

Operating Conditions

Temperature Range ..... 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SOIC Package 158
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to this maximum value.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, V_{EN} = 2.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA4244 MIN	HA4244 TYP	HA4244 MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	V_{EN} = 2.0V	25, 70	-	10.5	13	mA
	V_{EN} = 2.0V	0	-	-	14.5	mA
	V_{EN} = 0.8V	25, 70	-	-	275	µA
	V_{EN} = 0.8V	0	-	-	325	µA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping	$V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$	25, 70	±2.7	±2.8	-	V
		0	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	µA
Output Offset Voltage		25	-10	-	10	mV
Output Offset Voltage Drift (Note 3)		Full	-	25	50	µV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		25	-	160	-	ns
Turn-Off Time		25	-	320	-	ns
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
EN Input Current	V_{EN} = 0 to 4V	Full	-2	-	2	µA
CLK Input Current	V_{CLK} = 0 to 4V	Full	-10	-	10	µA
EN Setup Time to CLK Rising Edge		Full	-	25	-	ns
EN Hold Time after CLKRising Edge		Full	-	10	-	ns
AC CHARACTERISTICS						
Insertion Loss	$1V_{P-P}$	Full	-	0.04	0.05	dB

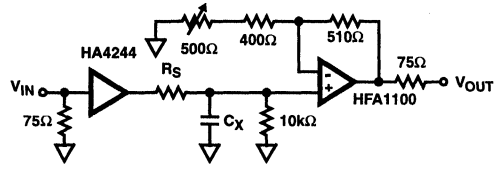
Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, V_{EN} = 2.0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA4244			UNITS
			MIN	TYP	MAX	
-3dB Bandwidth	R_S = 82Ω, C_L = 10pF	25	-	480	-	MHz
	R_S = 43Ω, C_L = 15pF	25	-	380	-	MHz
	R_S = 36Ω, C_L = 21pF	25	-	370	-	MHz
±0.1dB Flat Bandwidth	R_S = 82Ω, C_L = 10pF	25	-	250	-	MHz
	R_S = 43Ω, C_L = 15pF	25	-	175	-	MHz
	R_S = 36Ω, C_L = 21pF	25	-	170	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.0	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance	V_{EN} = 0.8V	Full	-	2.0	-	pF
Differential Gain	4.43MHz, Note 3	25	-	0.01	0.02	%
Differential Phase	4.43MHz, Note 3	25	-	0.01	0.02	Degrees
Off Isolation	$1V_{P-P}$, 100MHz, V_{EN} = 0.8V, R_L = 10Ω	Full	-	85	-	dB
Slew Rate ($1.5V_{P-P}$, +SR/-SR)	R_S = 82Ω, C_L = 10pF	25	-	1750/1770	-	V/µs
	R_S = 43Ω, C_L = 15pF	25	-	1460/1360	-	V/µs
	R_S = 36Ω, C_L = 21pF	25	-	1410/1360	-	V/µs
Total Harmonic Distortion	Note 3	Full	-	0.01	0.1	%
Disabled Output Resistance		Full	-	12	-	MΩ

NOTE:

3. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.

AC Test Circuit



NOTE: $C_L = C_X$ + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

Application Information

General

The HA4244 is a synchronous 1 x 1 crosspoint switch that is ideal for the matrix element in small, high input-to-output isolation switchers and routers. The HA4244's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor. This crosspoint contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled (EN = 0).

Synchronizing Latches

The HA4244 contains two latches which gate the EN input, thereby allowing all the crosspoints in a matrix to switch states synchronously. The latches also allow the EN input to be changed without affecting the current state of the

HA4244. Thus, the next channel switch can be set up, and isn't acted upon until the next rising CLK edge. As long as the EN signals meet a setup and hold time relative to the rising CLK edge, all of the HA4244s will assume their new state at the same time.

Power-Up Disable Function

The double latched EN signal, and single CLK input prevent the user from controlling the crosspoint state at power-up. To rectify this situation, the HA4244 incorporates power-up circuitry to ensure that the crosspoint powers up in the disabled state. Disabling the HA4244 prevents bus contention between multiplexed outputs, and minimizes the switching matrix supply current during power-up. Consider, for example, a matrix of 625 crosspoints that power-up randomly. If 50% of them power-up enabled, the required matrix supply current is 3.3A (313 x 10.5mA), neglecting output current. If HA4244s are utilized the power-up current is reduced to 0.125A (625 x 200µA).

Frequency Response

Most applications utilizing the HA4244 require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. As an example, -3dB bandwidth decreases to 160MHz for C_L = 100pF, R_S = 0Ω. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs, or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

EN - The ENABLE input is a TTL/CMOS compatible, active high input. When driven low this input forces the output to a true high impedance state and reduces the power dissipation by two orders of magnitude.

CLK - An active high, TTL/CMOS compatible input that controls the synchronizing latches. When CLK transistions low, the current state of the EN input is latched in the IC. This allows the EN input to be changed to the value corresponding to the next channel switch, without affecting the HA4244's current state. The HA4244 assumes the new state on the next rising edge of CLK.

Power Up Considerations

No signals should be applied to the digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 1 x 1 and 4 x 1 crosspoint switches. In addition to the HA4244, the 1 x 1 family includes the HA4600, which is an essentially similar device but without the synchronizing latches, and the HA4201 asynchronous crosspoint with a Tally output (enable indicator). The 4 x 1 family is comprised of the HA4314, HA4404, and HA4344. The HA4314 is a 14 lead basic 4 x 1 crosspoint. The HA4404 is a 16 lead device with Tally outputs to indicate the selected channel. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, $\overline{CS}$). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 10kΩ, Unless Otherwise Specified

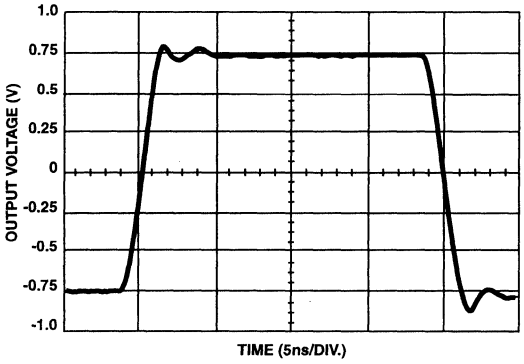


FIGURE 1. LARGE SIGNAL PULSE RESPONSE

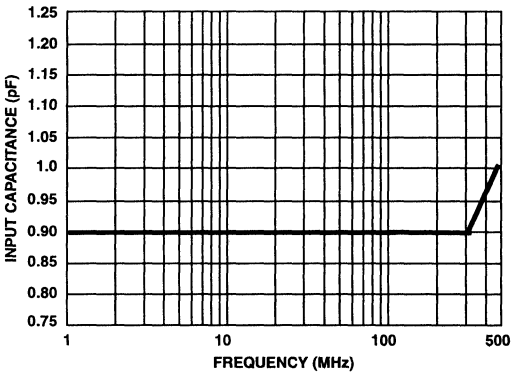


FIGURE 2. INPUT CAPACITANCE vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified

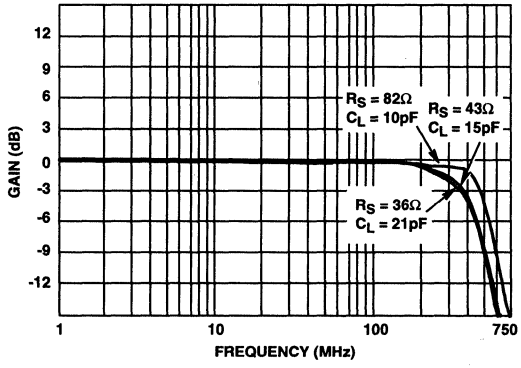


FIGURE 3. FREQUENCY RESPONSE

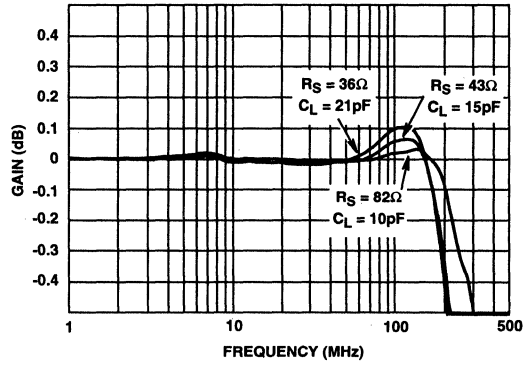


FIGURE 4. GAIN FLATNESS

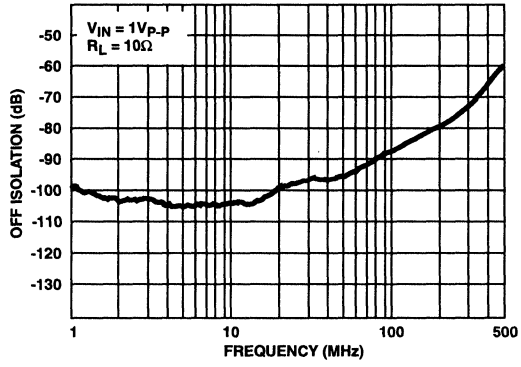


FIGURE 5. OFF ISOLATION

Die Characteristics

DIE DIMENSIONS:

51 mils x 36 mils x 19 mils
1290µm x 910µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)/TiW
Thickness: Metal 1: 6kÅ ±0.8kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±1.1kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

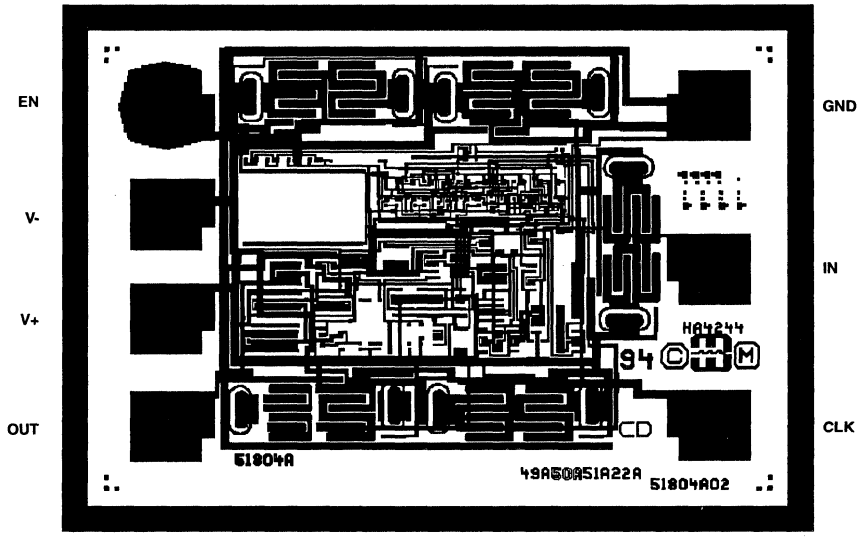
53

SUBSTRATE POTENTIAL (Powered Up):

V-

Metallization Mask Layout

HA4244



HARRIS SEMICONDUCTOR

HA4314B

400MHz, 4 x 1 Video Crosspoint Switch

November 1996

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1400V/µs
- 0.1dB Gain Flatness..... 100MHz
- -3dB Bandwidth 400MHz
- Off Isolation (100MHz)..... 70dB
- Crosstalk Rejection (30MHz)..... 80dB
- Differential Gain and Phase ..... 0.01%/0.01 Degrees
- High ESD Rating ..... >2000V
- TTL Compatible Control Inputs
- Improved Replacement for GX4314 and GX4314L

Applications

- Professional Video Switching and Routing
- HDTV
- Computer Graphics
- RF Switching and Routing
- PCM Data Routing

Description

The HA4314B is a very wide bandwidth 4 x 1 crosspoint switch ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation (105mW Enabled, 4mW Disabled), excellent differential gain and phase, and very high off isolation. When disabled, the output is switched to a high impedance state, making the HA4314B ideal for routing matrix equipment.

The HA4314B requires no external current source, and features fast switching and symmetric slew rates.

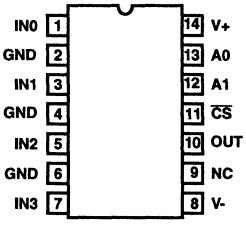
For a 4 x 1 crosspoint with Tally outputs (channel indicators) or with synchronous control signals, please refer to the HA4404B and HA4344B data sheets, respectively.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA4314BCP	0 to 70	14 Ld PDIP	E14.3
HA4314BCB	0 to 70	14 Ld SOIC	M14.15

Pinout

HA4314B
(PDIP, SOIC)
TOP VIEW



Truth Table

$\overline{CS}$	A1	A0	OUT
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	X	X	HIGH - Z

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 3679.4

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage ..... V_{SUPPLY}
Digital Input Current (Note 2) ..... ±25mA
Analog Input Current (Note 2) ..... ±5mA
Output Current 20mA

Operating Conditions

Temperature Range ..... 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	100
SOIC Package	120

Maximum Junction Temperature (Die) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP. (°C)	MIN	TYP	MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	$V_{\overline{CS}}$ = 0.8V	25, 70	-	10.5	13	mA
	$V_{\overline{CS}}$ = 0.8V	0	-	-	15.5	mA
	$V_{\overline{CS}}$ = 2.0V	25, 70	-	400	450	µA
	$V_{\overline{CS}}$ = 2.0V	0	-	400	580	µA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping	$V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$	25, 70	±2.7	±2.8	-	V
		0	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	µA
Output Offset Voltage		Full	-10	-	10	mV
Output Offset Voltage Drift (Note 3)		Full	-	25	50	µV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		25	-	160	-	ns
Turn-Off Time		25	-	320	-	ns
Output Glitch During Switching		25	-	±10	-	mV
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
Input Current	0V to 4V	Full	-2	-	2	µA
AC CHARACTERISTICS						
Insertion Loss	$1V_{P-P}$	25	-	0.055	0.063	dB
		Full	-	0.07	0.08	dB
Channel-to-Channel Insertion Loss Match		Full	-	±0.004	±0.006	dB
-3dB Bandwidth	R_S = 50Ω, C_L = 10pF	25	-	400	-	MHz
	R_S = 20Ω, C_L = 20pF	25	-	280	-	MHz
	R_S = 16Ω, C_L = 36pF	25	-	140	-	MHz
	R_S = 13Ω, C_L = 49pF	25	-	110	-	MHz

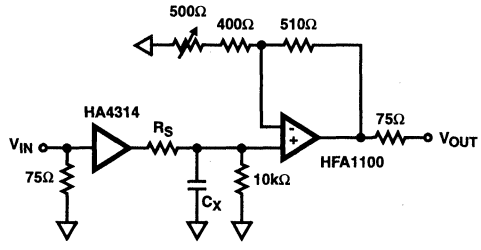
Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP. (°C)	MIN	TYP	MAX	UNITS
±0.1dB Flat Bandwidth	R_S = 50Ω, C_L = 10pF	25	-	100	-	MHz
	R_S = 20Ω, C_L = 20pF	25	-	100	-	MHz
	R_S = 16Ω, C_L = 36pF	25	-	85	-	MHz
	R_S = 13Ω, C_L = 49pF	25	-	75	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.5	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance	$V_{\overline{CS}}$ = 2.0V	Full	-	2.5	-	pF
Differential Gain	4.43MHz, Note 3	25	-	0.01	0.02	%
Differential Phase	4.43MHz, Note 3	25	-	0.01	0.02	Degrees
Off Isolation	$1V_{P-P}$, 100MHz, $V_{\overline{CS}}$ = 2.0V, R_L = 10Ω	Full	-	70	-	dB
Crosstalk Rejection	$1V_{P-P}$, 30MHz	Full	-	80	-	dB
Slew Rate ($1.5V_{P-P}$, +SR/-SR)	R_S = 50Ω, C_L = 10pF	25	-	1425/1450	-	V/µs
	R_S = 20Ω, C_L = 20pF	25	-	1010/1010	-	V/µs
	R_S = 16Ω, C_L = 36pF	25	-	725/750	-	V/µs
	R_S = 13Ω, C_L = 49pF	25	-	600/650	-	V/µs
Total Harmonic Distortion	10MHz, R_L = 1kΩ, Note 3	Full	-	0.01	0.1	%
Disabled Output Resistance	$V_{\overline{CS}}$ = 2.0V	Full	-	12	-	MΩ

NOTES:

3. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
4. Units are 100% tested at 25°C; Guaranteed but not tested at 0°C and 70°C.

AC Test Circuit



NOTE: $C_L = C_X$ + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

Application Information

General

The HA4314B is a 4 x 1 crosspoint switch that is ideal for the matrix element of high performance switchers and routers. This crosspoint's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor. Nevertheless, if several HA4314B inputs are connected together, the use of an input buffer should be considered (see Figure 1). This crosspoint contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled ($\overline{CS}$ = 1).

Ground Connections

All GND pins are connected to a common point on the die, so any one of them will suffice as the functional GND connection. For the best isolation and crosstalk rejection, however, all GND pins must connect to the GND plane.

Frequency Response

Most applications utilizing the HA4314B require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multi-

plexed outputs (see Figure 2), or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

$\overline{CS}$ - This is a TTL/CMOS compatible, active low Chip Select input. When driven high, $\overline{CS}$ forces the output to a true high impedance state and reduces the power dissipation by a factor of 25. The $\overline{CS}$ input has no on-chip pull-down resistor, so it must be connected to a logic low (recommend GND) if the enable function isn't utilized.

A0, A1 - These are binary coded, TTL/CMOS compatible address inputs that select which one of the four inputs connect to the crosspoint output.

Switcher/Router Applications

Figure 1 illustrates one possible implementation of a wideband, low power, 4 x 4 switcher/router utilizing the HA4314B for the switch matrix. A 4 x 4 switcher/router allows any of the four outputs to be driven by any one of the four inputs (e.g., each of the four inputs may connect to a different output, or an input may connect to multiple outputs). This application utilizes the HA4600 (video buffer with output disable) for the input buffer, the HA4314B as the switch matrix, and the HFA1112 (programmable gain buffer) as the gain of two output driver. Figure 2 details a 16 x 1 switcher (basically a 16:1 mux) which uses the HA4201 (1 x 1 crosspoint) and the HA4314B in a cascaded stage configuration to minimize capacitive loading at each output node, thus increasing system bandwidth.

Power Up Considerations

No signals should be applied to the analog or digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 4 x 1 and 1 x 1 crosspoint switches. In addition to the HA4314B, the 4 x 1 family includes the HA4404 and HA4344. The HA4404 is a 16 lead device with Tally outputs to indicate the selected channel. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, $\overline{CS}$). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

The 1 x 1 family is comprised of the HA4201 and HA4600. They are essentially similar devices, but the HA4201 includes a Tally output (enable indicator). The 1 x 1s are useful as high performance video input buffers, or in a switch matrix requiring very high off isolation.

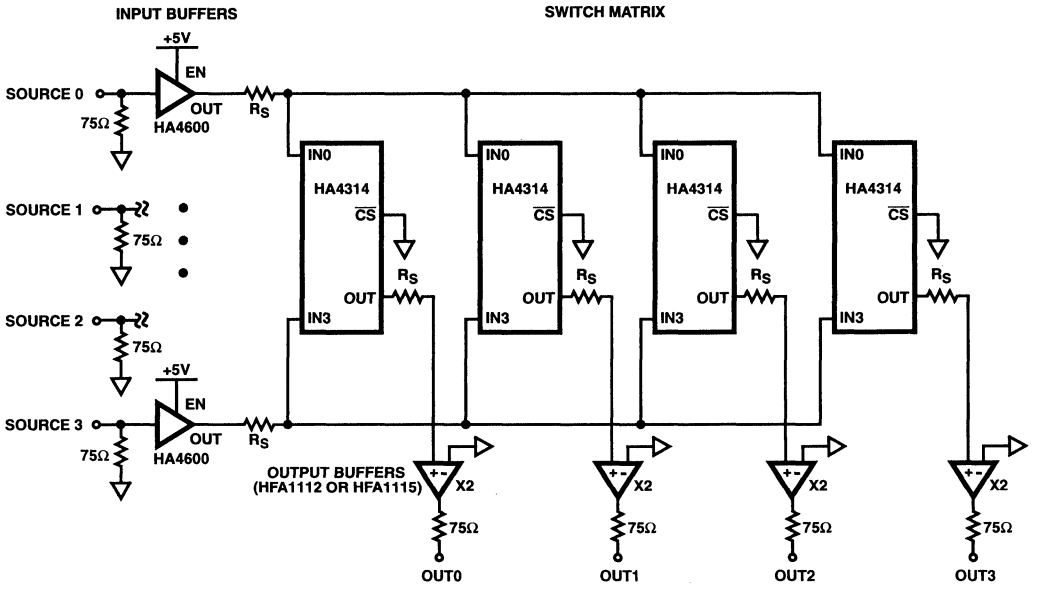


FIGURE 1. 4 x 4 SWITCHER/ROUTER APPLICATION

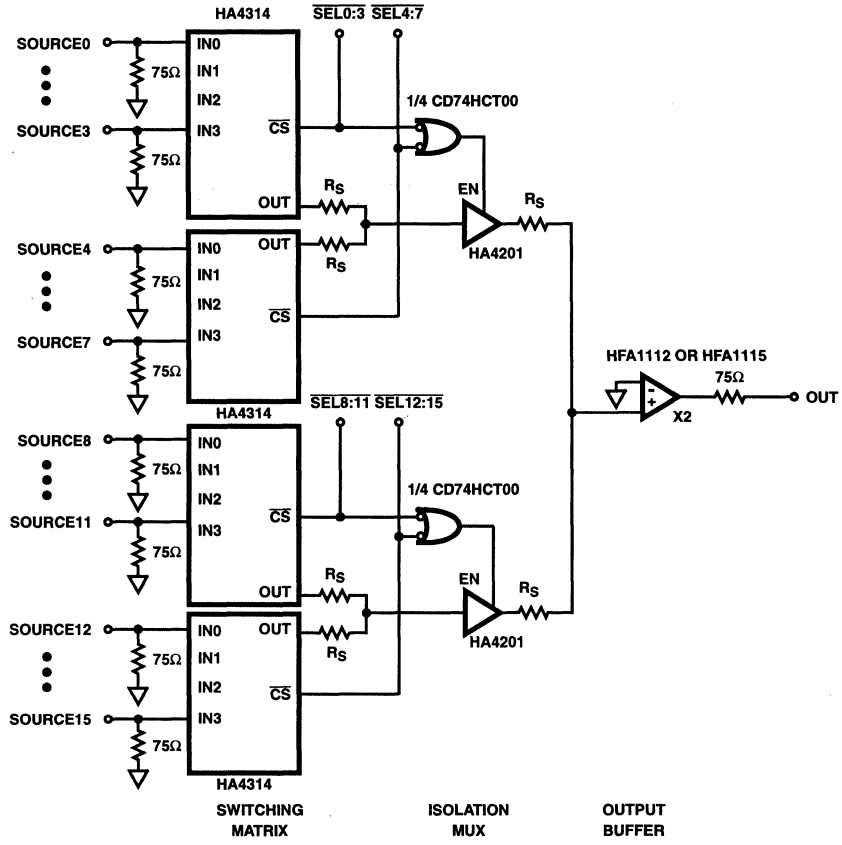


FIGURE 2. 16 x 1 SWITCHER APPLICATION

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 10kΩ, Unless Otherwise Specified

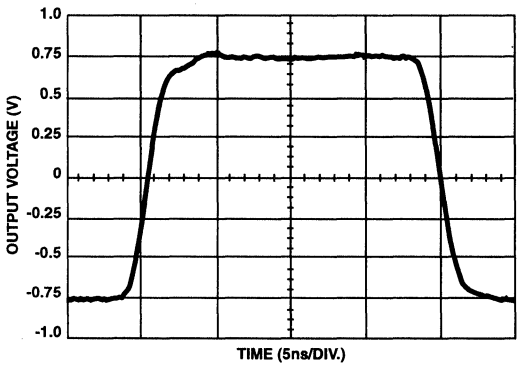


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

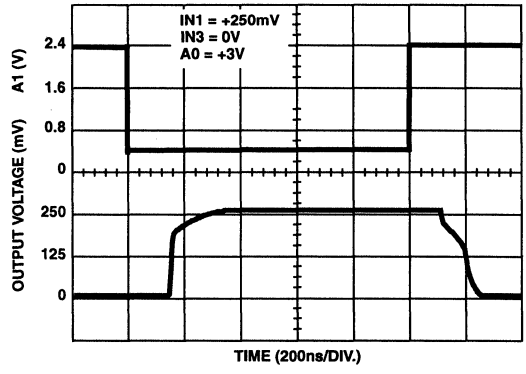


FIGURE 4. CHANNEL-TO-CHANNEL SWITCHING RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified (Continued)

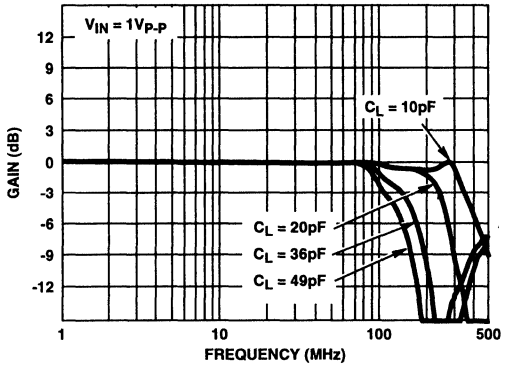


FIGURE 5. FREQUENCY RESPONSE

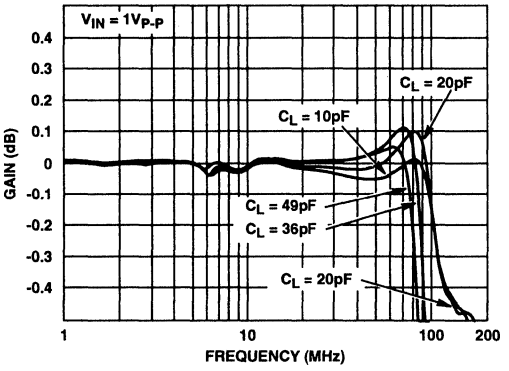


FIGURE 6. GAIN FLATNESS

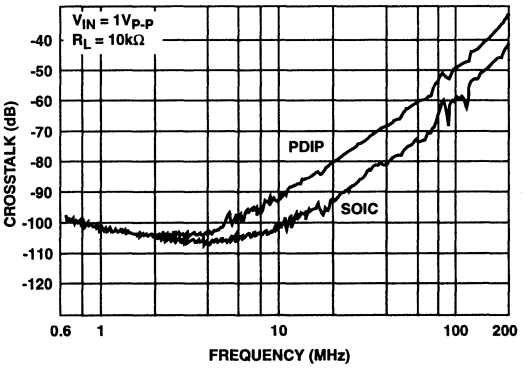


FIGURE 7. ALL HOSTILE CROSSTALK REJECTION

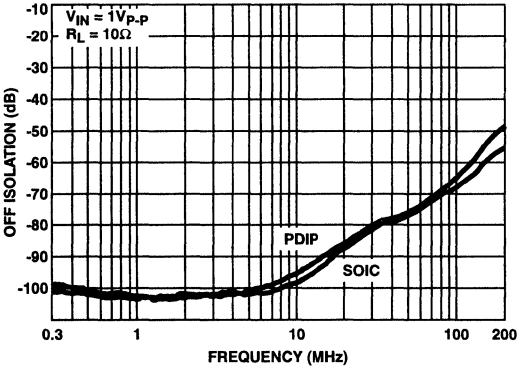


FIGURE 8. ALL HOSTILE OFF ISOLATION

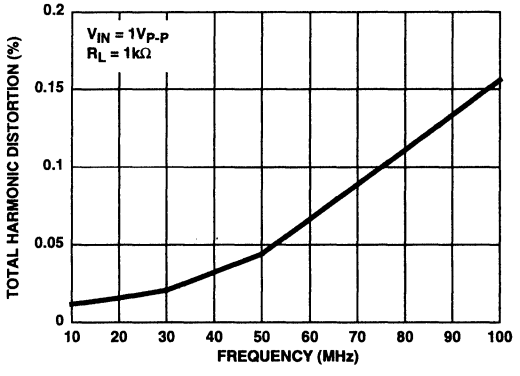


FIGURE 9. TOTAL HARMONIC DISTORTION vs FREQUENCY

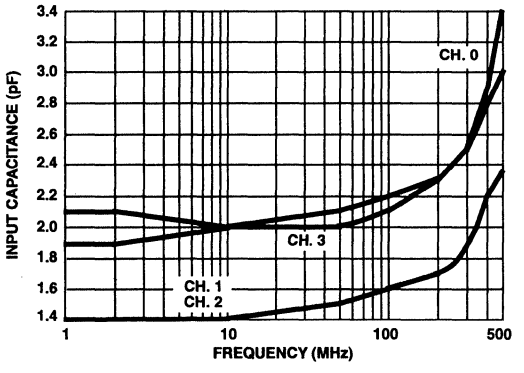


FIGURE 10. INPUT CAPACITANCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

65 mils x 118 mils x 19 mils
1640µm x 3000µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)/TiW
Thickness: Metal 1: 6kÅ ±0.8kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±1.1kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

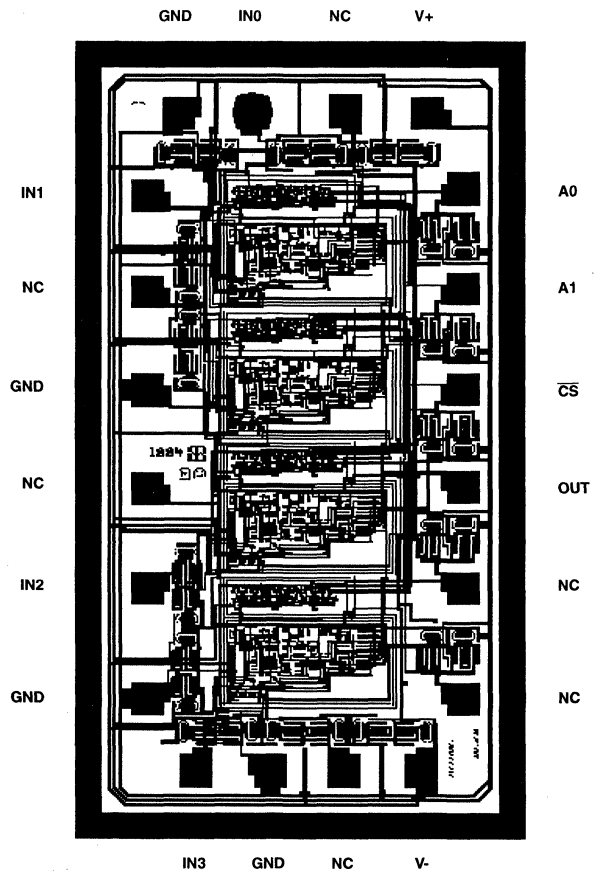
200

SUBSTRATE POTENTIAL (Powered Up):

V-

Metallization Mask Layout

HA4314B



HARRIS SEMICONDUCTOR

HA4344B

350MHz, 4 x 1 Video Crosspoint Switch with Synchronous Controls

November 1996

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1400V/μs
- 0.1dB Gain Flatness..... 100MHz
- -3dB Bandwidth 350MHz
- Off Isolation (100MHz)..... 70dB
- Crosstalk Rejection (30MHz)..... 80dB
- Differential Gain and Phase 0.01%/0.01Degrees
- High ESD Rating ..... >2000V
- TTL Compatible Control Signals
- Latched Control Lines for Synchronous Switching

Applications

- Professional Video Switching and Routing
- RGB Video Distribution Systems
- Computer Graphics
- RF Switching and Routing

Description

The HA4344B is a very wide bandwidth 4 x 1 crosspoint switch ideal for professional video switching, HDTV, computer display routing, and other high performance applications. This circuit features very low power dissipation, excellent differential gain and phase, high off isolation, symmetric slew rates, fast switching, and latched control signals. When disabled, the output is switched to a high impedance state, making the HA4344B ideal for matrix routers.

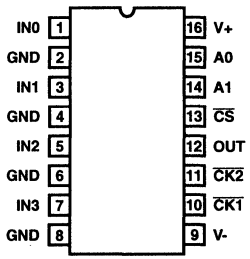
The latched control signals allow for synchronized channel switching. When $\overline{CK1}$ is low the master control latch loads the next switching address (A0, A1, $\overline{CS}$), while the closed (assuming $\overline{CK2}$ is the inverse of $\overline{CK1}$) slave control latch maintains the crosspoint in its current state. $\overline{CK2}$ switching low closes the master latch (with previous assumption), loads the now open slave latch, and switches the crosspoint to the newly selected channel. Channel selection is asynchronous (changes with any control signal change) if both $\overline{CK1}$ and $\overline{CK2}$ are low.

Ordering Information

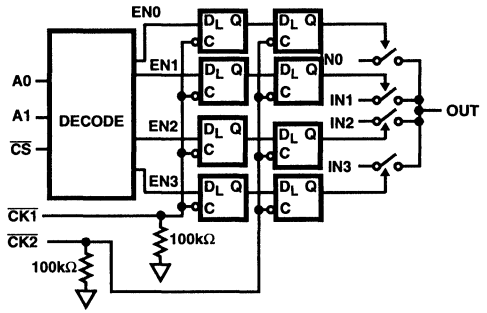
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA4344BCP	0 to 70	16 Ld PDIP	E16.3
HA4344BCB	0 to 70	16 Ld SOIC	M16.15

Pinout

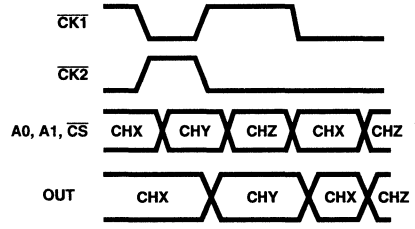
HA4344B
(PDIP, SOIC)
TOP VIEW



Functional Diagram



Timing Diagram



6 VIDEO CROSS-POINT SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1996

File Number 3956.1

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage. . . . . V_{SUPPLY}
Digital Input Current (Note 2) . . . . . ±25mA
Analog Input Current (Note 2) . . . . . ±5mA
Output Current 20mA

Operating Conditions

Temperature Range . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	115

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP. (°C)	MIN	TYP	MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	$V_{\overline{CS}}$ = 0.8V	25, 70	-	10.5	13	mA
	$V_{\overline{CS}}$ = 0.8V	0	-	-	15.5	mA
	$V_{\overline{CS}}$ = 2.0V	25, 70	-	400	450	µA
	$V_{\overline{CS}}$ = 2.0V	0	-	400	580	µA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing Without Clipping	$V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$	25, 70	±2.7	±2.8	-	V
		0	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	µA
Output Offset Voltage		Full	-10	-	10	mV
Output Offset Voltage Drift (Note 3)		Full	-	25	50	µV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		25	-	160	-	ns
Turn-Off Time		25	-	320	-	ns
Output Glitch During Switching		25	-	±10	-	mV
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
$\overline{CLK1}$, $\overline{CLK2}$ Input Current	0 to 4V	Full	-	40	50	µA
$\overline{CS}$, A0, A1 Input Current	0 to 4V	Full	-2	-	2	µA
AC CHARACTERISTICS						
Insertion Loss	$1V_{P-P}$	25	-	0.055	0.063	dB
		Full	-	0.07	0.08	dB
Channel-to-Channel Insertion Loss Match		Full	-	±0.004	±0.006	dB

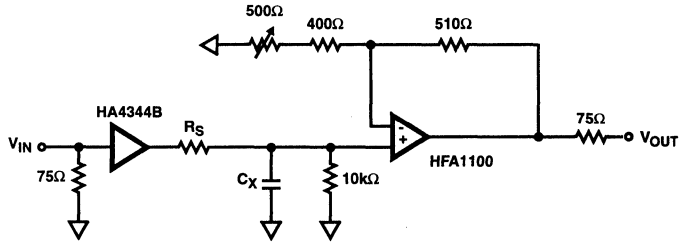
Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP. (°C)	MIN	TYP	MAX	UNITS
-3dB Bandwidth	R_S = 47Ω, C_L = 10pF	25	-	350	-	MHz
	R_S = 29Ω, C_L = 20pF	25	-	300	-	MHz
	R_S = 16Ω, C_L = 33pF	25	-	220	-	MHz
	R_S = 9Ω, C_L = 52pF	25	-	160	-	MHz
±0.1dB Flat Bandwidth	R_S = 47Ω, C_L = 10pF	25	-	150	-	MHz
	R_S = 29Ω, C_L = 20pF	25	-	110	-	MHz
	R_S = 16Ω, C_L = 33pF	25	-	100	-	MHz
	R_S = 9Ω, C_L = 52pF	25	-	70	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.5	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance	$V_{\overline{CS}}$ = 2.0V	Full	-	2.5	-	pF
Differential Gain	4.43MHz, Note 3	25	-	0.01	0.02	%
Differential Phase	4.43MHz, Note 3	25	-	0.01	0.02	Degrees
Off Isolation	$1V_{P-P}$, 100MHz, $V_{\overline{CS}}$ = 2.0V	Full	-	70	-	dB
Crosstalk Rejection	$1V_{P-P}$, 30MHz	Full	-	80	-	dB
Slew Rate ($1.5V_{P-P}$, +SR/-SR)	R_S = 47Ω, C_L = 10pF	25	-	1400/1490	-	V/µs
	R_S = 29Ω, C_L = 20pF	25	-	1200/1260	-	V/µs
	R_S = 16Ω, C_L = 33pF	25	-	870/940	-	V/µs
	R_S = 9Ω, C_L = 52pF	25	-	750/710	-	V/µs
Total Harmonic Distortion (Note 3)		Full	-	0.01	0.1	%
Disabled Output Resistance	$V_{\overline{CS}}$ = 2.0V	Full	-	12	-	MΩ

NOTES:

3. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
4. Units are 100% tested at 25°C; guaranteed, but not tested at 0°C and 70°C.

AC Test Circuit



NOTE: $C_L = C_X$ + Test Fixture Capacitance.

HARRIS SEMICONDUCTOR

HA4404B

330MHz, 4 x 1 Video Crosspoint Switch with Tally Outputs

November 1996

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1250V/µs
- 0.1dB Gain Flatness..... 165MHz
- -3dB Bandwidth 330MHz
- Off Isolation (100MHz)..... 70dB
- Crosstalk Rejection (30MHz)..... 80dB
- Differential Gain and Phase ..... 0.01%/0.01 Degrees
- High ESD Rating ..... >2000V
- TTL Compatible Control Inputs
- Open Collector Tally Outputs
- Improved Replacement for GX4404

Applications

- Professional Video Switching and Routing
- HDTV
- Computer Graphics
- RF Switching and Routing

Description

The HA4404B is a very wide bandwidth 4 x 1 crosspoint switch ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation (105mW Enabled, 4mW Disabled), excellent differential gain and phase, and very high off isolation. When disabled, the output is switched to a high impedance state, making the HA4404B ideal for routing matrix equipment.

The HA4404B requires no external current source, and features fast switching and symmetric slew rates. The tally outputs are open collector PNP transistors to V+ to provide an indication of crosspoint selection.

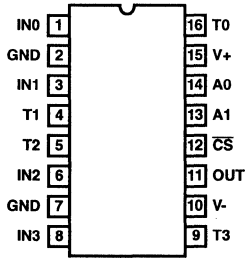
For a 4 x 1 crosspoint without Tally outputs or with synchronous control signals, please refer to the HA4314B and HA4344B Data Sheets, respectively.

Ordering Information

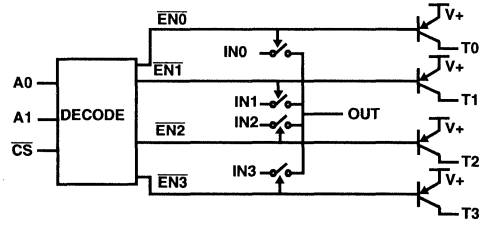
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA4404BCP	0 to 70	16 Ld PDIP	E16.3
HA4404BCB	0 to 70	16 Ld SOIC	M16.15

Pinout

HA4404B
(PDIP, SOIC)
TOP VIEW



Functional Diagram



TRUTH TABLE

CS	A1	A0	OUT	ACTIVE TALLY OUTPUT
0	0	0	IN0	T0
0	0	1	IN1	T1
0	1	0	IN2	T2
0	1	1	IN3	T3
1	X	X	High - Z	None, All High - Z

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3678.4**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage ..... V_{SUPPLY}
Digital Input Current (Note 2) ..... ±25mA
Analog Input Current (Note 2) ..... ±5mA
Output Current 20mA

Operating Conditions

Temperature Range ..... 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	90
SOIC Package	115

Maximum Junction Temperature (Die) ..... 175^oC
Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP. (^oC)	MIN	TYP	MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	$V_{\overline{CS}}$ = 0.8V	25, 70	-	10.5	13	mA
	$V_{\overline{CS}}$ = 0.8V	0	-	-	15.5	mA
	$V_{\overline{CS}}$ = 2.0V	25, 70	-	400	450	µA
	$V_{\overline{CS}}$ = 2.0V	0	-	400	580	µA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping	$V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$	25, 70	±2.7	±2.8	-	V
		0	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	µA
Output Offset Voltage		Full	-10	-	10	mV
Output Offset Voltage Drift (Note 3)		Full	-	25	50	µV/^oC
SWITCHING CHARACTERISTICS						
Turn-On Time		25	-	160	-	ns
Turn-Off Time		25	-	320	-	ns
Output Glitch During Switching		25	-	±10	-	mV
DIGITAL DC CHARACTERISTICS						
Input Logic Voltage	High	Full	2	-	-	V
	Low	Full	-	-	0.8	V
Input Current	0V to 4V	Full	-2	-	2	µA
Tally Output High Voltage	I_{OH} = 1mA	Full	4.7	4.8	-	V
Tally Off Leakage Current	V_{TALLY} = 0V	Full	-20	-	20	µA
AC CHARACTERISTICS						
Insertion Loss	$1V_{P-P}$	25	-	0.055	0.063	dB
		Full	-	0.07	0.08	dB
Channel-to-Channel Insertion Loss Match		Full	-	±0.004	±0.006	dB
-3dB Bandwidth	R_S = 50Ω, C_L = 11pF	25	-	330	-	MHz
	R_S = 24Ω, C_L = 19pF	25	-	290	-	MHz
	R_S = 15Ω, C_L = 34pF	25	-	210	-	MHz
	R_S = 11Ω, C_L = 49pF	25	-	170	-	MHz

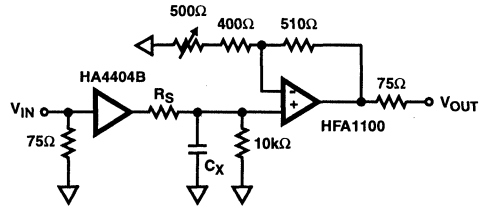
Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP. (°C)	MIN	TYP	MAX	UNITS
±0.1dB Flat Bandwidth	R_S = 50Ω, C_L = 11pF	25	-	165	-	MHz
	R_S = 24Ω, C_L = 19pF	25	-	130	-	MHz
	R_S = 15Ω, C_L = 34pF	25	-	137	-	MHz
	R_S = 11Ω, C_L = 49pF	25	-	100	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.5	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance	$V_{\overline{CS}}$ = 2.0V	Full	-	2.5	-	pF
Differential Gain	4.43MHz, Note 3	25	-	0.01	0.02	%
Differential Phase	4.43MHz, Note 3	25	-	0.01	0.02	Degrees
Off Isolation	$1V_{P-P}$, 100MHz, $V_{\overline{CS}}$ = 2.0V, R_L = 10Ω	Full	-	70	-	dB
Crosstalk Rejection	$1V_{P-P}$, 30MHz	Full	-	80	-	dB
Slew Rate ($1.5V_{P-P}$, +SR/-SR)	R_S = 50Ω, C_L = 11pF	25	-	1280/1260	-	V/µs
	R_S = 24Ω, C_L = 19pF	25	-	1190/1170	-	V/µs
	R_S = 15Ω, C_L = 34pF	25	-	960/930	-	V/µs
	R_S = 11Ω, C_L = 49pF	25	-	810/790	-	V/µs
Total Harmonic Distortion	10MHz, R_L = 1kΩ, Note 3	Full	-	0.01	0.1	%
Disabled Output Resistance	$V_{\overline{CS}}$ = 2.0V	Full	-	12	-	MΩ

NOTES:

3. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
4. Units are 100% tested at 25°C; guaranteed, but not tested at 0°C and 70°C.

AC Test Circuit



NOTE: $C_L = C_X$ + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

Application Information

General

The HA4404B is a 4 x 1 crosspoint switch that is ideal for the matrix element of high performance switchers and routers. This crosspoint's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor. Nevertheless, if several HA4404B inputs are connected together, the use of an input buffer should be considered (see Figure 1). This crosspoint contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled ($\overline{CS}$ = 1).

Ground Connections

All GND pins are connected to a common point on the die, so any one of them will suffice as the functional GND connection. For the best isolation and crosstalk rejection, however, all GND pins must connect to the GND plane.

Frequency Response

Most applications utilizing the HA4404B require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs (see

Figure 2), or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

$\overline{CS}$ - This is a TTL/CMOS compatible, active low Chip Select input. When driven high, $\overline{CS}$ forces the output to a true high impedance state and reduces the power dissipation by a factor of 25. The $\overline{CS}$ input has no on-chip pull-down resistor, so it must be connected to a logic low (recommend GND) if the enable function isn't utilized.

A0, A1 - These are binary coded, TTL/CMOS compatible address inputs that select which one of the four inputs connect to the crosspoint output.

T0-T3 - The Tally outputs are open collector PNP transistors connected to V+. When $\overline{CS} = 0$, the PNP transistor associated with the selected input is enabled and current is delivered to the load. When the crosspoint is disabled, or the channel is unselected, the Tally output(s) present a very high impedance to the external circuitry. Several Tally outputs may be wire OR'd together to generate complex control signals, as shown in the application circuits below. The Tally load may be terminated to GND or to V- as long as the continuous output current doesn't exceed 3mA (6mA at 50% duty cycle, etc.).

Switcher/Router Applications

Figure 1 illustrates one possible implementation of a wideband, low power, 4 x 4 switcher/router utilizing the HA4404B for the switch matrix. A 4 x 4 switcher/router allows any of the four outputs to be driven by any one of the four inputs (e.g., each of the four inputs may connect to a different output, or an input may connect to multiple outputs). This application utilizes the HA4600 (video buffer with output disable) for the input buffer, the HA4404B as the switch matrix, and the HFA1112 (programmable gain buffer) as the gain of two output driver. Figure 2 details a 16 x 1 switcher (basically a 16:1 mux) which uses the HA4201 (1 x 1 crosspoint) and the HA4404B in a cascaded stage configuration to minimize capacitive loading at each output node, thus increasing system bandwidth.

Power Up Considerations

No signals should be applied to the analog or digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 4 x 1 and 1 x 1 crosspoint switches. In addition to the HA4404B, the 4 x 1 family includes the HA4314 and HA4344. The HA4314 is a basic 14 lead device without Tally outputs. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, $\overline{CS}$). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

The 1 x 1 family is comprised of the HA4201 and HA4600. They are essentially similar devices, but the HA4201 includes a Tally output. The 1 x 1s are useful as high performance video input buffers, or in a switch matrix requiring very high off isolation.

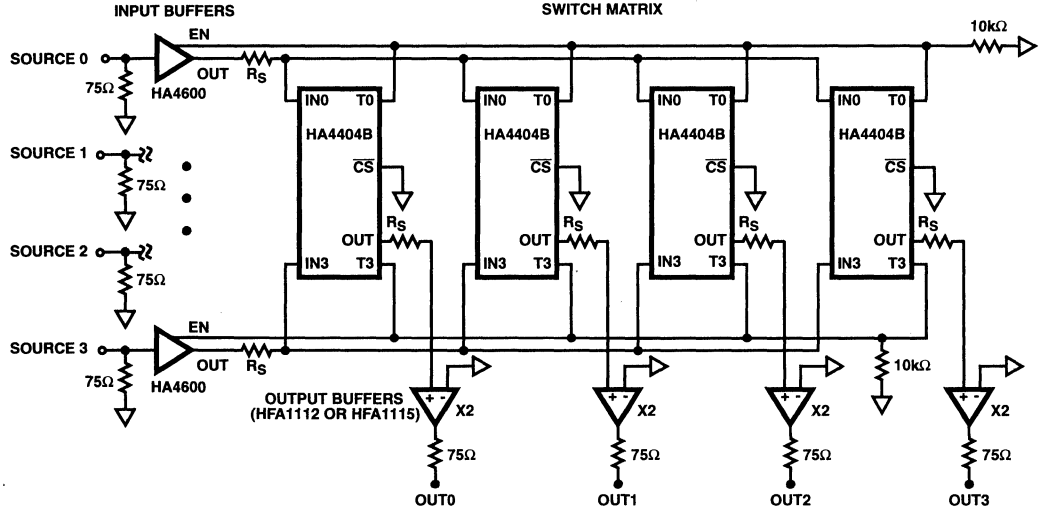


FIGURE 1. 4 X 4 SWITCHER/ROUTER APPLICATION

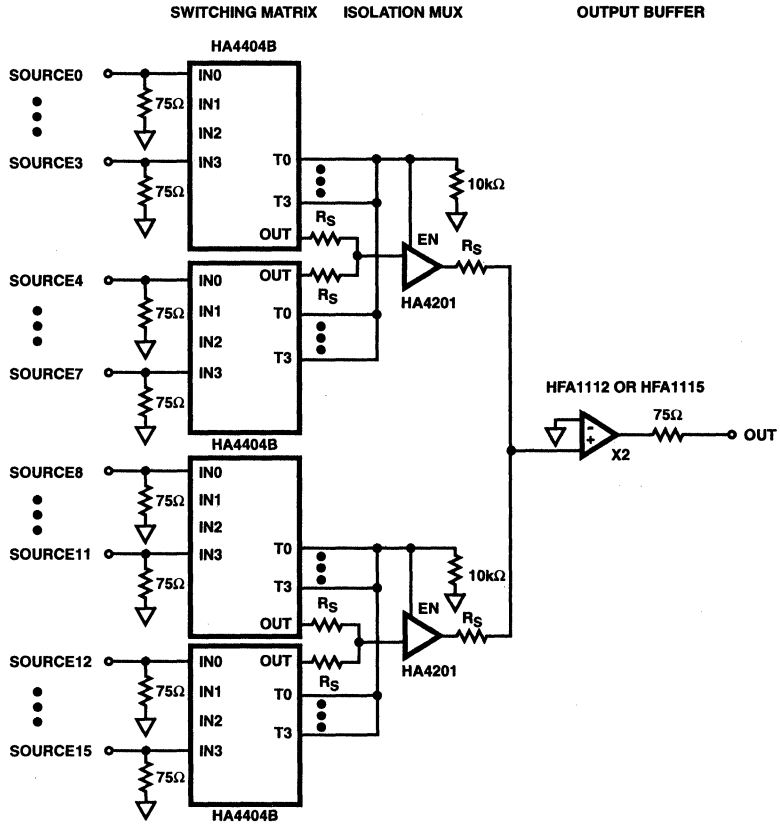


FIGURE 2. 16 X 1 SWITCHER APPLICATION

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified

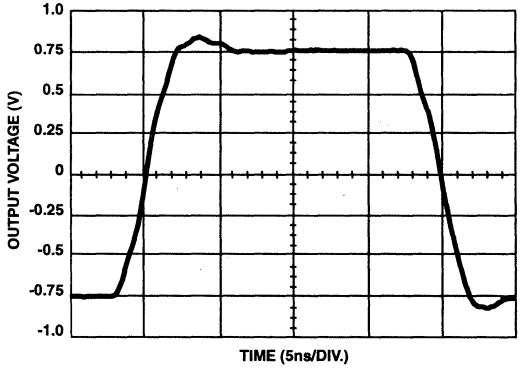


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

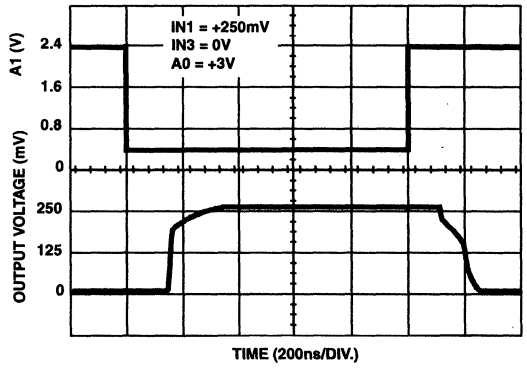


FIGURE 4. CHANNEL-TO-CHANNEL SWITCHING RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified (Continued)

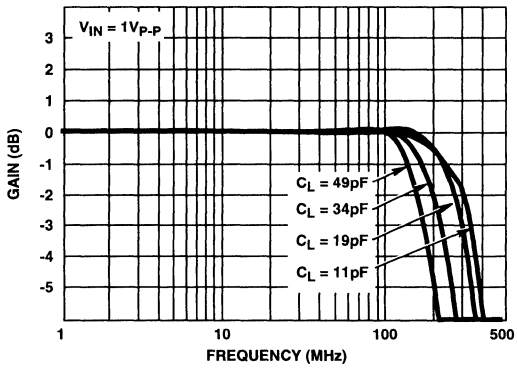


FIGURE 5. FREQUENCY RESPONSE

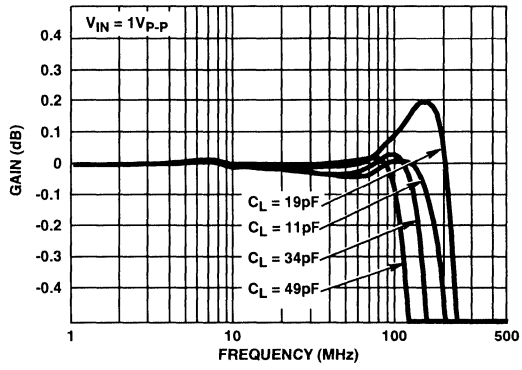


FIGURE 6. GAIN FLATNESS

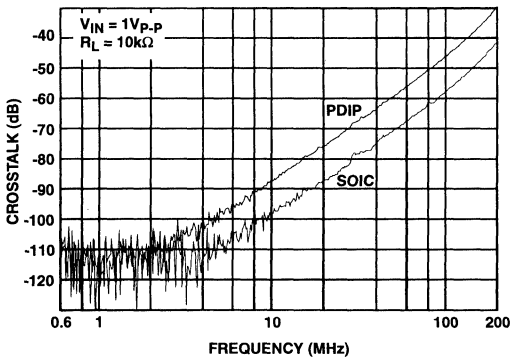


FIGURE 7. ALL HOSTILE CROSSTALK REJECTION

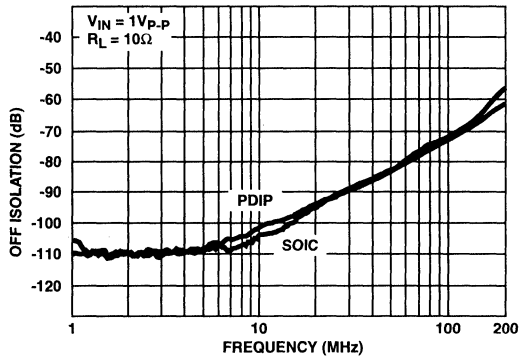


FIGURE 8. ALL HOSTILE OFF ISOLATION

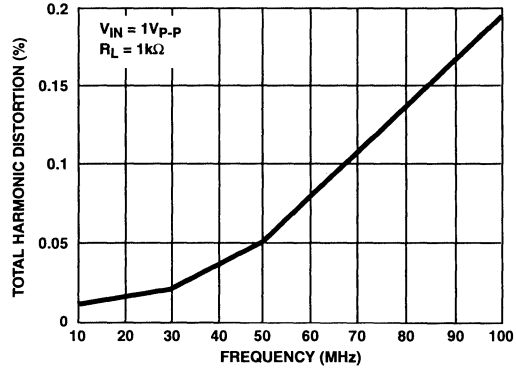


FIGURE 9. TOTAL HARMONIC DISTORTION vs FREQUENCY

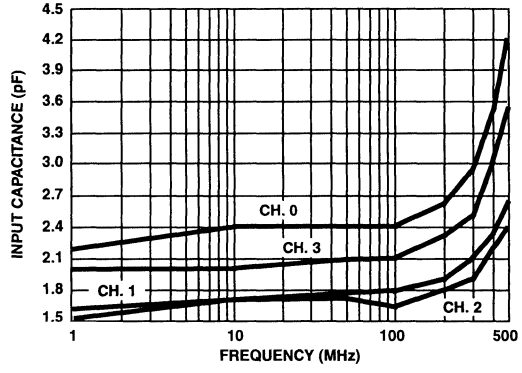


FIGURE 10. INPUT CAPACITANCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

65 mils x 118 mils x 19 mils
1640µm x 3000µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)/TiW
Thickness: Metal 1: 6kÅ ±0.8kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±1.1kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

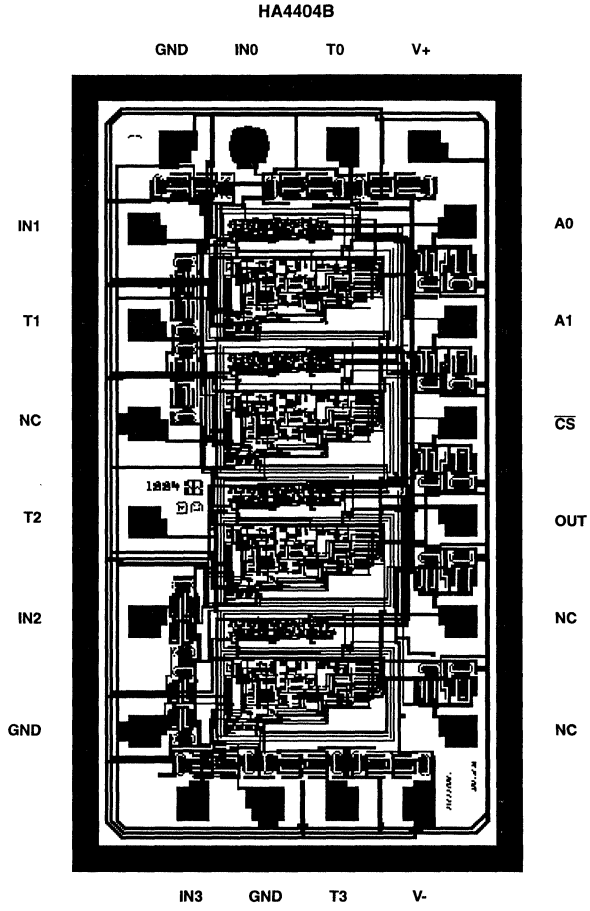
TRANSISTOR COUNT:

200

SUBSTRATE POTENTIAL (Powered Up):

V-

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HA455

ADVANCE INFORMATION

November 1996

130MHz, 8 x 8 Video Crosspoint Switch

Features

- Fully Buffered Inputs and Outputs (A_V = +1)
- Routes Any Input Channel to Any Output Channel
- Switches Standard and High Resolution Video Signals
- Serial or Parallel Digital Interface
- Expandable for Larger Switch Matrices
- Wide Bandwidth 130MHz
- High Slew Rate 250V/µs
- Low Differential Gain/Phase . . . . . 0.02%/0.02 Degrees
- Low Crosstalk at 10MHz . . . . . -60dB

Applications

- Professional Video Switching and Routing
- Security and Video Editing Systems

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA455CN	0 to 70	44 Ld MQFP	M44.10x10

Description

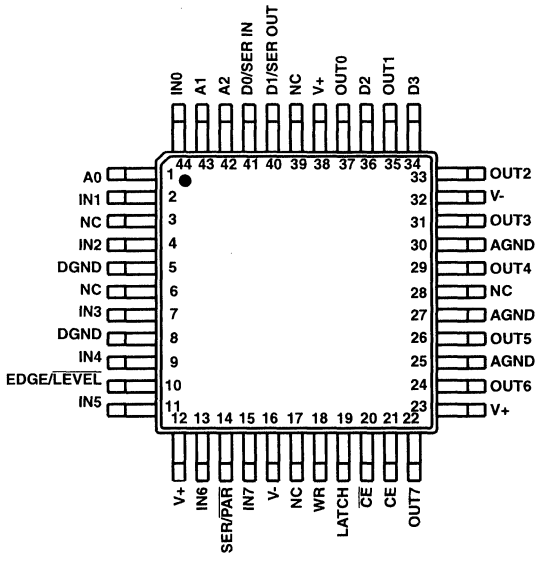
The HA455 is the first 8 x 8 video crosspoint switch suitable for high performance video systems. Its high level of integration significantly reduces component count, board space, and cost. The crosspoint switch contains a digitally controlled matrix of 64 fully buffered switches that connect eight video input signals to any, or all, matrix outputs. Each matrix output connects to an internal, high-speed (250V/µs), unity gain buffer capable of driving 400Ω and 20pF to ±2V.

For applications requiring gain or increased drive capability, the HA455 outputs can be connected directly to two HFA1412 quad, gain of two video buffers, which are capable of driving 75Ω loads. Another option which also provides gain capability is the HA457 170MHz, gain of two 8 x 8 crosspoint.

This crosspoint's true high impedance three-state output capability, makes it feasible to parallel multiple HA455s and form larger switch matrices.

Pinout

HA455 (MQFP)
TOP VIEW



6 VIDEO CROSS-POINT SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number 4264

HARRIS SEMICONDUCTOR

HA456

ADVANCE INFORMATION

November 1996

80MHz, Low Power, 8 x 8 Video Crosspoint Switch

Features

- Fully Buffered Inputs and Outputs (A_V = +1)
- Routes Any Input Channel to Any Output Channel
- Switches Standard and High Resolution Video Signals
- Serial or Parallel Digital Interface
- Expandable for Larger Switch Matrices
- Wide Bandwidth 80MHz
- High Slew Rate 170V/µs
- Low Differential Gain/Phase . . . . . 0.04%/0.2 Degrees
- Low Crosstalk at 10MHz . . . . . -60dB

Applications

- Professional Video Switching and Routing
- Security and Video Editing Systems

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA456CN	0 to 70	44 Ld MQFP	M44.10x10
HA456CM	0 to 70	44 Ld PLCC	N44.65

Description

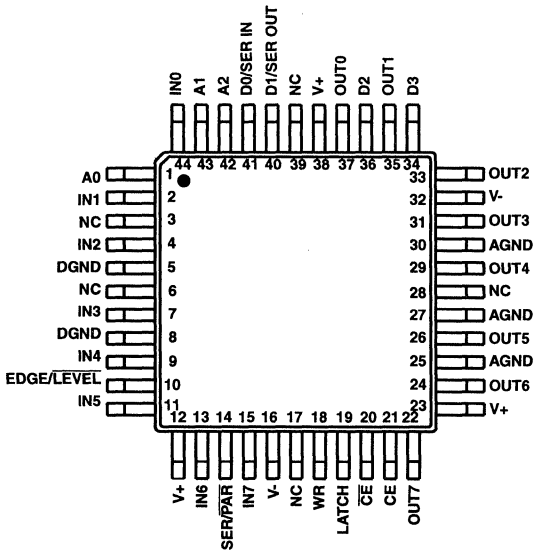
The HA456 is the first 8 x 8 video crosspoint switch suitable for high performance video systems. Its high level of integration significantly reduces component count, board space, and cost. The crosspoint switch contains a digitally controlled matrix of 64 fully buffered switches that connect eight video input signals to any, or all, matrix outputs. Each matrix output connects to an internal, high-speed (170V/µs), unity gain buffer capable of driving 400Ω and 20pF to ±2V.

For applications requiring gain or increased drive capability, the HA456 outputs can be connected directly to two HFA1412 quad, gain of two video buffers, which are capable of driving 75Ω loads. Another option which also provides gain capability is the HA457 170MHz, gain of two 8 x 8 crosspoint.

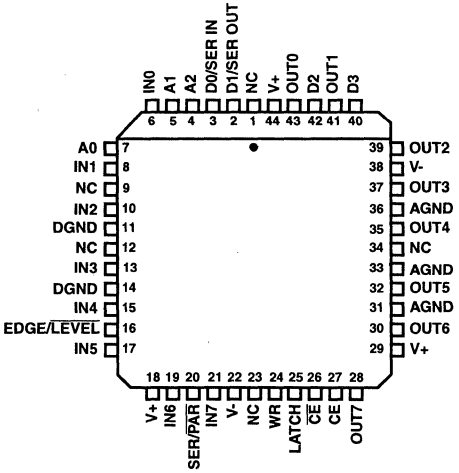
This crosspoint's true high impedance three-state output capability, makes it feasible to parallel multiple HA456s and form larger switch matrices.

Pinouts

HA456 (MQFP)
TOP VIEW



HA456 (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **4153**

HARRIS SEMICONDUCTOR

HA457

ADVANCE INFORMATION

November 1996

170MHz, A_V = +2, 8 x 8 Video Crosspoint Switch

Features

- Fully Buffered Inputs and Outputs (A_V = +2)
- Routes Any Input Channel to Any Output Channel
- Switches Standard and High Resolution Video Signals
- Serial or Parallel Digital Interface
- Expandable for Larger Switch Matrices
- Wide Bandwidth 170MHz
- High Slew Rate 350V/µs
- Low Differential Gain/Phase . . . . . 0.01%/0.02 Degrees
- Low Crosstalk at 10MHz . . . . . -60dB

Applications

- Professional Video Switching and Routing
- Security Systems
- Video Editing

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA457CN	0 to 70	44 Ld MQFP	M44.10x10

Description

The HA457 is the first 8 x 8 video crosspoint switch suitable for high performance video systems. Its high level of integration significantly reduces component count, board space, and cost. The crosspoint switch contains a digitally controlled matrix of 64 fully buffered switches that connect eight video input signals to any, or all, matrix outputs. Each output connects to eight internal, high-speed (350V/µs), gain of two buffers capable of driving 150Ω and 20pF to ±2.0V.

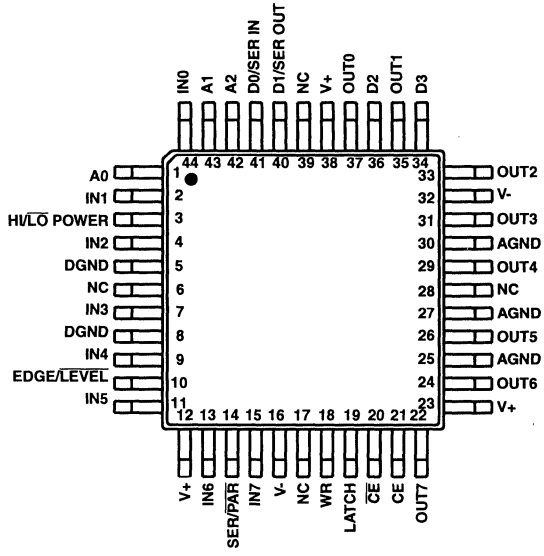
The HI/$\overline{\text{LO}}$POWER lead may be strapped to GND for power critical applications that don't require "broadcast quality" video performance. In this low power mode, power dissipation decreases from 880mW to 560mW.

The HA457 will directly drive a double terminated video cable with some degradation of differential gain and phase. Applications demanding the best composite video performance should drive the cable with a unity gain video buffer, such as the HFA1412 quad buffer.

This crosspoint's three-state output capability, makes it feasible to parallel multiple HA457s and form larger switch matrices.

Pinout

HA457
(MQFP)
TOP VIEW



6 VIDEO CROSS-POINT SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 4231

HARRIS SEMICONDUCTOR

HA4600

480MHz, Video Buffer with Output Disable

November 1996

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1700V/μs
- 0.1dB Gain Flatness..... 250MHz
- Off Isolation (100MHz)..... 85dB
- Differential Gain and Phase ..... 0.01%/0.01 Degrees
- High ESD Rating ..... >2000V
- TTL Compatible Enable Input
- Improved Replacement for GB4600

Applications

- Professional Video Switching and Routing
- Video Multiplexers
- HDTV
- Computer Graphics
- RF Switching and Routing
- PCM Data Routing

Description

The HA4600 is a very wide bandwidth, unity gain buffer ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation (105mW Enabled, 1mW Disabled), excellent differential gain and phase, and very high off isolation. When disabled, the output is switched to a high impedance state, making the HA4600 ideal for routing matrix equipment and video multiplexers.

The HA4600 also features fast switching and symmetric slew rates. A typical application for the HA4600 is interfacing Harris' wide range of video crosspoint switches.

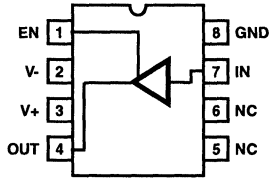
For applications requiring a tally output (enable indicator), please refer to the HA4201 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA4600CP	0 to 70	8 Ld PDIP	E8.3
HA4600CB (4600CB)	0 to 70	8 Ld SOIC	M8.15

Pinout

HA4600
(PDIP, SOIC)
TOP VIEW



Truth Table

EN	OUT
0	High Z
1	Active

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 3990.2

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage. . . . . V_{SUPPLY}
Digital Input Current (Note 2) . . . . . ±25mA
Output Current 20mA

Operating Conditions

Temperature Range . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to this maximum value.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, V_{EN} = 2.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	V_{EN} = 2V	25, 70	-	10.5	13	mA
	V_{EN} = 2V	0	-	-	14.5	mA
	V_{EN} = 0.8V	25, 70	-	100	115	µA
	V_{EN} = 0.8V	0	-	100	125	µA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping	$V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$	25, 70	±2.7	±2.8	-	V
		0	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	µA
Output Offset Voltage		25	-10	-	10	mV
Output Offset Voltage Drift (Note 3)		Full	-	25	50	µV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		25	-	160	-	ns
Turn-Off Time		25	-	320	-	ns
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
EN Input Current	0V to 4V	Full	-2	-	2	µA
AC CHARACTERISTICS						
Insertion Loss	$1V_{P-P}$	Full	-	0.04	0.05	dB
-3dB Bandwidth	R_S = 82Ω, C_L = 10pF	25	-	480	-	MHz
	R_S = 43Ω, C_L = 15pF	25	-	380	-	MHz
	R_S = 36Ω, C_L = 21pF	25	-	370	-	MHz
±0.1dB Flat Bandwidth	R_S = 82Ω, C_L = 10pF	25	-	250	-	MHz
	R_S = 43Ω, C_L = 15pF	25	-	175	-	MHz
	R_S = 36Ω, C_L = 21pF	25	-	170	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.0	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance	V_{EN} = 0.8V	Full	-	2.0	-	pF
Differential Gain (Note 3)	4.43MHz	25	-	0.01	0.02	%

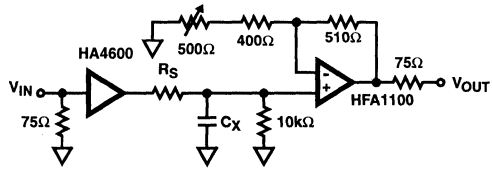
Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, V_{EN} = 2.0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Differential Phase (Note 3)	4.43MHz	25	-	0.01	0.02	Degrees
Off Isolation	$1V_{P-P}$, 100MHz, V_{EN} = 0.8V, R_L = 10Ω	Full	-	85	-	dB
Slew Rate ($1.5V_{P-P}$, +SR/-SR)	R_S = 82Ω, C_L = 10pF	25	-	1750/1770	-	V/µs
	R_S = 43Ω, C_L = 15pF	25	-	1460/1360	-	V/µs
	R_S = 36Ω, C_L = 21pF	25	-	1410/1360	-	V/µs
Total Harmonic Distortion (Note 3)		Full	-	0.01	0.1	%
Disabled Output Resistance		Full	-	12	-	MΩ

NOTE:

3. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.

AC Test Circuit



NOTE: $C_L = C_X$ + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

Application Information

General

The HA4600 is a unity gain buffer that is optimized for high performance video applications. The output disable function makes it ideal for the matrix element in small, high input-to-output isolation switchers and routers. This buffer contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled (EN = 0). The HA4600 also excels as an input buffer for routers with a large number of outputs (i.e. each input must connect to a large number of outputs) and delivers performance superior to most video amplifiers at a fraction of the cost. As an input buffer, the HA4600's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor.

Frequency Response

Most applications utilizing the HA4600 require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. As an example, -3dB bandwidth decreases to 160MHz for C_L = 100pF, R_S = 0Ω. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs (see Figure 2), or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

EN - The ENABLE input is a TTL/CMOS compatible, active high input. When driven low this input forces the output to a true high impedance state and reduces the power dissipation by two orders of magnitude. The EN input has no on-chip pull-up resistor, so it must be connected to a logic high (recommend V+) if the enable function isn't utilized.

Switcher/Router Applications

Figure 1 illustrates one possible implementation of a wideband, low power, 4 x 4 switcher/router. A 4 x 4 switcher/router allows any of the four outputs to be driven by any one of the four inputs (e.g. each of the four inputs may connect to a different output, or an input may connect to multiple outputs). This application utilizes the HA4600 for the input buffer, the HA4404 (4 x 1 crosspoint switch) as the switch matrix, and the HFA1112 (programmable gain buffer) as the gain of two output driver. Figure 2 details a 16 x 1 switcher (basically a 16:1 mux) which uses the HA4600 in a cascaded stage configuration to minimize capacitive loading at each output node, thus increasing system bandwidth.

Power Up Considerations

No signals should be applied to the analog or digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 1 x 1 and 4 x 1 crosspoint switches. In addition to the HA4600, the 1 x 1 family includes the HA4201 which is an essentially similar device that includes a Tally output (enable indicator). The 4 x 1 family is comprised of the HA4314, HA4404, and HA4344. The HA4314 is a 14 lead basic 4 x 1 crosspoint. The HA4404 is a 16 lead device with Tally outputs

to indicate the selected channel. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, CS). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

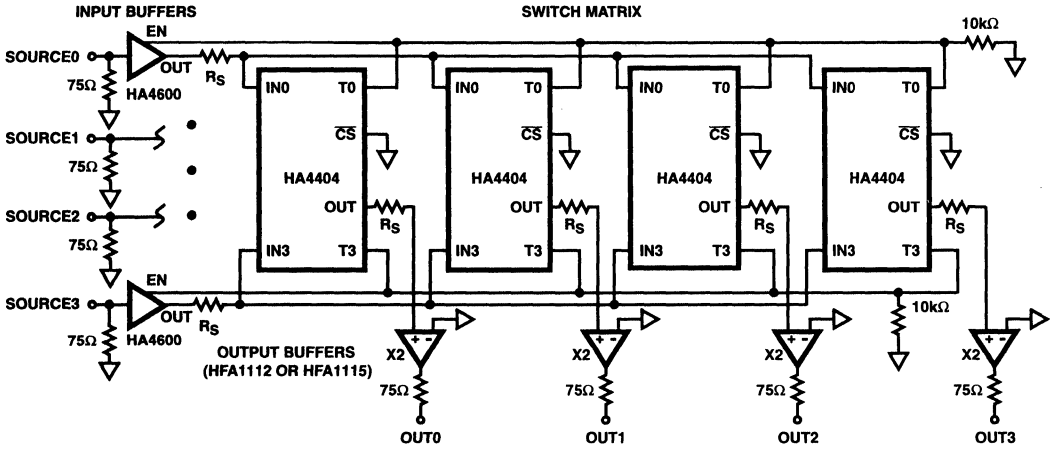


FIGURE 1. 4 x 4 SWITCHER/ROUTER APPLICATION

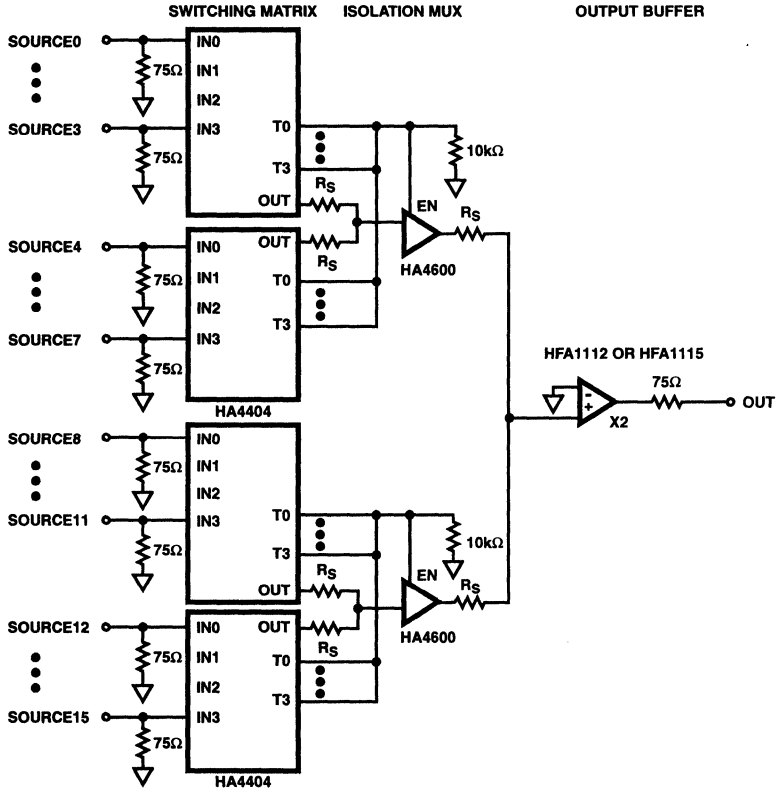


FIGURE 2. 16 x 1 SWITCHER APPLICATION

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified

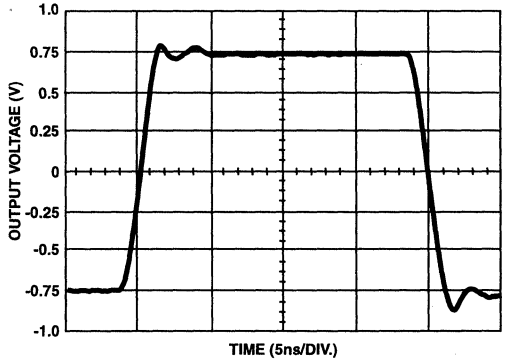


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

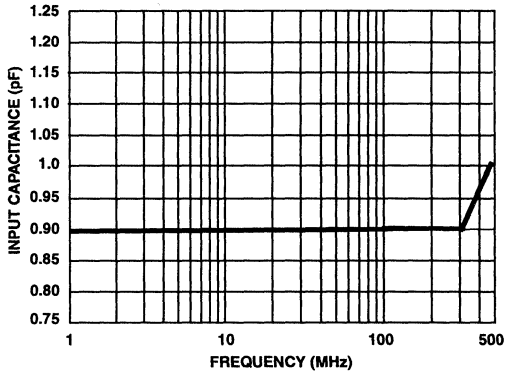


FIGURE 4. INPUT CAPACITANCE vs FREQUENCY

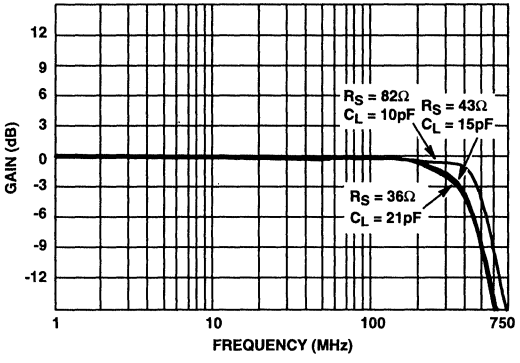


FIGURE 5. FREQUENCY REPONSE

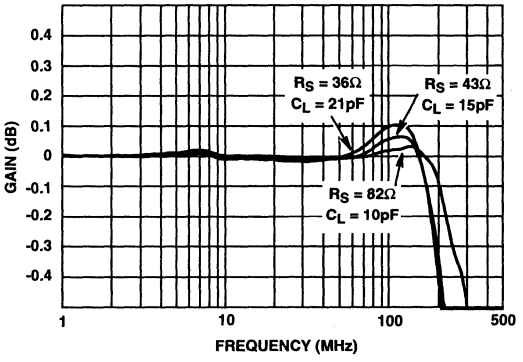


FIGURE 6. GAIN FLATNESS

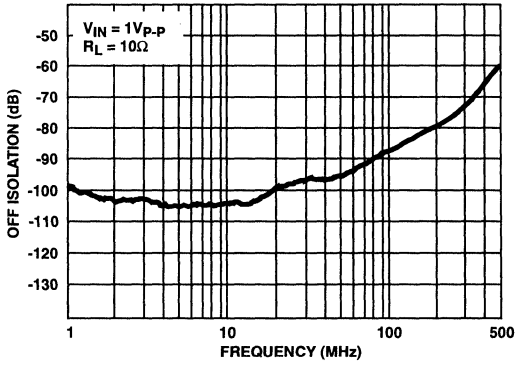


FIGURE 7. OFF ISOLATION

Die Characteristics

DIE DIMENSIONS:

51 mils x 36 mils x 19 mils
1290µm x 910µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)/TiW
Thickness: Metal 1: 6kÅ ±0.8kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±1.1kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

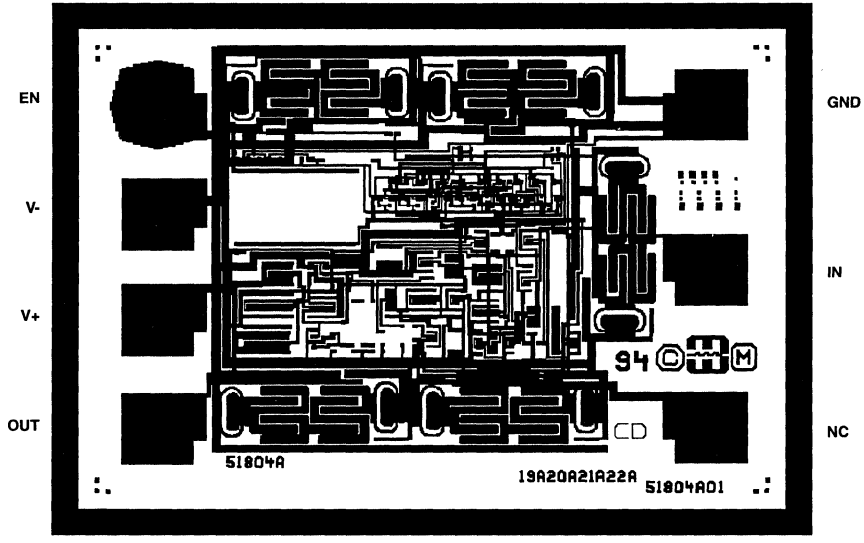
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

53

Metallization Mask Layout

HA4600



LINEAR 7

TRANSISTOR AND DIODE ARRAYS, AND DIFFERENTIAL AMPLIFIERS

Selection Guide

DIFFERENTIAL AMPLIFIERS: Typical Values, Unless Otherwise Specified

TYPE	DESCRIPTION	(NOTE 4) FEATURES	FREQ. RANGE DC TO (MHz)	VOLTAGE GAIN (dB)	BW (3dB POINT) (MHz)	1/F NF (dB)	AGC RANGE (dB)	(NOTE 5) LEAD CT AND PKG TYPE
CA3028A	Differential/ Cascode Amplifiers	• Balanced Differential Amplifier Configuration with Controlled Constant Current Source • RF, IF and Video Frequency Capability • Balanced AGC Capability • Operation from DC to 500MHz • CA3028B is Controlled for Input Offset Voltage, Current, and Input Bias Current, and is Intended for "Balance" Requirements • Push-Pull Inputs and Outputs • CA3028 and CA3053 are Identical Except for 100MHz Noise Specification	120	40 (Note 1)	-	7.2	62	8 PDIP, 8 SOIC, 8 Metal Can
CA3028B			120	40	8	7.2	62	
CA3049	Dual High Frequency		500	22	1.35 (Note 2)	4.6	75	12 Metal Can
CA3053	Differential/Cascode Amplifier		120	40	Recommended for IF Amplifier Applications			8 PDIP, 8 Metal Can
CA3054	Dual Independent		120	32	550 (Note 3)	3.25	75	14 PDIP, 14 SOIC
CA3102	Dual High Frequency		500	22	1.35 (Note 2)	4.6	75	14 PDIP, 14 SOIC

NOTES:

1. Power Gain (G_P) Min. at 100MHz: Cascode = 16dB; Differential Amplifier = 14dB.
2. GHz.
3. f_T (MHz).
4. T_A Range: -55°C to 125°C except for type CA3054 (0°C to 85°C).
5. See Linear Package Selection Guide in Section 11.

TRANSISTOR ARRAYS: Electrical Characteristics $T_A = 25°C$

TYPE	DESCRIPTION	$V_{(BR)\ CEO}$ (MIN) V	$V_{(BR)\ CBO}$ (MIN) V	h_{FE} (MIN)	I_C (MAX) mA	(NOTE 1) LEAD COUNT AND PACKAGE TYPE
CA3045	Three Transistors Plus a Differential Pair	15	20	40	50	14 CERDIP, 14 SBDIP
CA3046		15	20	40	50	14 PDIP, 14 SOIC
		f_T > 300MHz. 2 matched pairs ±5mV				
CA3081	General-Purpose NPN High-Current Transistors	16	20	40	100	16 PDIP, 16 CERDIP, 16 SOIC (150 mil)
		Seven Common-Emitter				
CA3082		16	20	40	100	16 PDIP, 16 CERDIP, 16 SOIC (150 mil)
		Seven Common-Collector				
CA3083		15	20	40	100	16 PDIP, 16 CERDIP, 16 SOIC (150 mil)
		Five independent transistors. Q_1 and Q_2 matched; I_{IO} (at 1mA) 2.5µA Max				
CA3086	Three Isolated Transistors Plus a Differential Pair	15	20	40	50	14 PDIP, 14 CERDIP, 14 SOIC
		f_T > 550MHz Typ Operation from DC to 120MHz				
CA3127	Five Independent Transistors	15	20	40	20	16 PDIP, 16 SOIC (150 mil)
		f_T > 1GHz. Operation from DC to 500MHz				
CA3146	Three Transistors Plus a Differential Pair	30	40	30	50	14 PDIP, 14 SOIC
CA3146A		40	50	30	50	
		f_T > 500MHz Typ Operation from DC to 120MHz				

TRANSISTOR ARRAYS: Electrical Characteristics $T_A = 25^oC$ **(Continued)**

TYPE	DESCRIPTION	$V_{(BR)\ CEO}$ (MIN) V	$V_{(BR)\ CBO}$ (MIN) V	h_{FE} (MIN)	I_C (MAX) mA	(NOTE 1) LEAD COUNT AND PACKAGE TYPE
CA3183	Five High-Current Transistors	30	40	40	75	16 PDIP, 16 SOIC (150 mil)
CA3183A		40	50	40	75	
		High-Voltage Versions of CA3083 Transistors Q_1 and Q_2 Matched at 1mA				
CA3227	Five Independent Transistors	8	12	40	20	16 PDIP, 16 SOIC (150 mil)
		f_T = 3GHz Typ Operation from DC to 1.5GHz				
CA3246	Three Independent Transistors Plus a Differential Pair	8	12	40	20	14 PDIP, 14 SOIC
		f_T = 3GHz Typ Operation from DC to 1.5GHz				

TYPE	DESCRIPTION	$V_{(BR)\ CEO}$ (MIN) V NPN/PNP	$V_{(BR)\ CBO}$ (MIN) V NPN/PNP	h_{FE} (MIN) NPN/PNP	I_C (MAX) NPN/PNP	(NOTE 1) LEAD COUNT AND PACKAGE TYPE
CA3096	Five Independent Transistors, 3 NPN, 2 PNP	35/-40	45/-40	150/20	50/-10	16 PDIP, 16 SOIC (150 mil)
CA3096A		35/-40	45/-40	150/20	50/-10	
CA3096C		24/-24	30/-24	100/15	50/-10	16 PDIP
		NPN		PNP		
		$\|V_{IO}\|$ = 5mV Max		5mV Max		
		$\|I_{IO}\|$ = 0.6µA Max		0.25µA Max		
HFA3046	Three 8GHz NPN Transistors Plus an NPN Differential Pair	8	12	40	15	14 SOIC
		$\|V_{IO}\|$ = 5mV Max				
HFA3096	Three 8GHz NPN Transistors Plus Two 5.5GHz PNP Transistors	8	12/10	40/25	15	16 SOIC (150 mil)
		NF = 3.5dB at 1GHz				
HFA3127	Five Independent 8GHz NPN Transistors	8	12	40	15	16 SOIC (150 mil)
		NF = 3.5dB at 1GHz				
HFA3128	Five Independent 5.5GHz PNP Transistors	8	10	25	15	16 SOIC (150 mil)
		NF = 3.5dB at 1GHz				

NOTE:

1. See Linear Package Selection Guide in Section 11.

DIODE ARRAYS: $T_A = 25^oC$. Apply for Each Diode

TYPE	DESCRIPTION	$V_{(BR)\ R}$ (MIN) V	I_R (MAX) µA	C_D (TYP) pF	$V_{F1} - V_{F2}$ (MAX) mV	(NOTE 1) PIN COUNT AND PACKAGE TYPE
CA3039	6 Individual	5	0.1	0.65	5 (I_F =1mA)	14 SOIC, 12 Metal Can
		ULTRA-FAST LOW-CAPACITANCE MATCHED DIODES				

NOTES:

1. See Linear Package Selection Guide in Section 11.
2. Six connected to form 3 common-cathode pairs. Four connected to form 2 common-anode diode pairs.

CA3018, CA3018A

NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

November 1996

General Purpose Transistor Arrays

Features

- Matched Monolithic General Purpose Transistors
- h_{FE} Matched ..... ±10%
- V_{BE} Matched
  - CA3018A ..... ±2mV
  - CA3018 ..... ±5mV
- Operation From DC to 120MHz
- Wide Operating Current Range
- CA3018A Performance Characteristics Controlled from 10μA to 10mA
- Low Noise Figure ..... 3.2dB (Typ) at 1kHz
- Full Military Temperature Range ..... -55°C to 125°C

Applications

- Two Isolated Transistors and a Darlington Connected Transistor Pair for Low Power Applications at Frequencies from DC through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated Circuit Transistor Array" for Suggested Applications

Description

The CA3018 and CA3018A consist of four general purpose silicon NPN transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

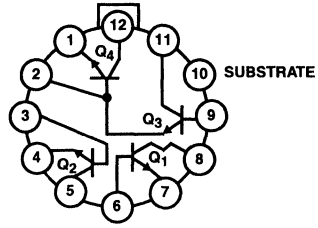
The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3018	-55 to 125	12 Pin Metal Can	T12.B
CA3018A	-55 to 125	12 Pin Metal Can	T12.B

Pinout

CA3018, CA3018A
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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HARRIS SEMICONDUCTOR

CA3028A, CA3028B, CA3053

Differential/Cascode Amplifiers for Commercial and Industrial Equipment from DC to 120MHz

November 1996

Features

- Controlled for Input Offset Voltage, Input Offset Current and Input Bias Current (CA3028 Series Only)
- Balanced Differential Amplifier Configuration with Controlled Constant Current Source
- Single-Ended and Dual-Ended Operation

Applications

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator
- Mixer
- Limiter
- Related Literature
  - Application Note AN5337 "Application of the CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations

Description

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from DC to 120MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical DC and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

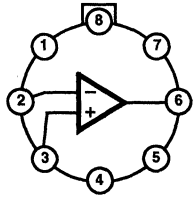
The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

Ordering Information

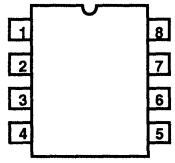
PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3028A	-55 to 125	8 Pin Metal Can	T8.C
CA3028AE	-55 to 125	8 Ld PDIP	E8.3
CA3028AM (3028A)	-55 to 125	8 Ld SOIC	M8.15
CA3028AM96 (3028A)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA3028B	-55 to 125	8 Pin Metal Can	T8.C
CA3028BE	-55 to 125	8 Ld PDIP	E8.3
CA3028BM (3028B)	-55 to 125	8 Ld SOIC	M8.15
CA3053	-55 to 125	8 Pin Metal Can	T8.C
CA3053E	-55 to 125	8 Ld PDIP	E8.3

Pinouts

CA3028A/B, CA3053 (METAL CAN)
TOP VIEW

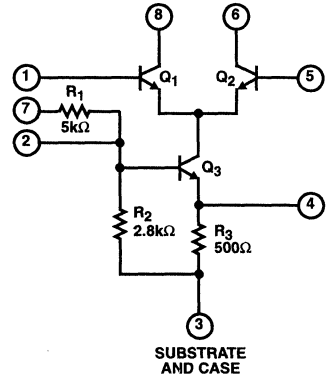


CA3028A/B, (PDIP, SOIC) CA3053 (PDIP)
TOP VIEW



Schematic Diagram

(Terminal Numbers Apply to All Packages)



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **382.3**

Operating Conditions

Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	225	140
PDIP Package	155	N/A
SOIC Package	185	N/A

Maximum Junction Temperature (Metal Can Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Absolute Maximum Voltage Ratings $T_A = 25°C$

The following chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal Terminal 4 with respect to Terminal 2 is -1V to +5V.

TERM NO.	1	2	3	4	5	6	7	8
1		0 to -15 (Note 4)	0 to -15 (Note 4)	0 to -15 (Note 4)	+5 to -5	Note 3	Note 3	+20 to 0 (Note 5)
2			+5 to -11	+5 to -1	+15 to 0 (Note 6)	Note 3	+15 to 0 (Note 6)	Note 3
3 (Note 2)				+10 to 0	+15 to 0 (Note 6)	+30 to 0 (Note 7)	+15 to 0 (Note 6)	+30 to 0 (Note 7)
4					+15 to 0 (Note 6)	Note 3	Note 3	Note 3
5						+20 to 0 (Note 5)	Note 3	Note 3
6							Note 3	Note 3
7								Note 3
8								

Absolute Maximum Current Ratings

TERM NO.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

NOTES:

2. Terminal No. 3 is connected to the substrate and case.
3. Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.
4. Limit is -12V for CA3053.
5. Limit is +15V for CA3053.
6. Limit is +12V for CA3053.
7. Limit is +24V for CA3028A and +18V for CA3053.

Electrical Specifications $T_A = 25°C$

PARAMETER	SYMBOL	TEST CONDITIONS	CA3028A			CA3028B			CA3053			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS												
Input Offset Voltage (Figures 1, 14)	V_{IO}	V_{CC} = 6V, V_{EE} = -6V	-	-	-	-	0.98	5.0	-	-	-	mV
		V_{CC} = 12V, V_{EE} = -12V	-	-	-	-	0.89	5.0	-	-	-	mV
Input Offset Current (Figures 2, 14)	I_{IO}	V_{CC} = 6V, V_{EE} = -6V	-	-	-	-	0.56	5.0	-	-	-	µA
		V_{CC} = 12V, V_{EE} = -12V	-	-	-	-	1.06	6.0	-	-	-	µA
Input Bias Current (Figures 2, 3, 15, 16)	I_I	V_{CC} = 6V, V_{EE} = -6V	-	16.6	70	-	16.6	40	-	-	-	µA
		V_{CC} = 12V, V_{EE} = -12V	-	36	106	-	36	80	-	-	-	µA
		V_{CC} = 9V		-	-	-	-	-	-	29	85	µA
		V_{CC} = 12V	-	-	-	-	-	-	-	36	125	µA

Electrical Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		CA3028A MIN	CA3028A TYP	CA3028A MAX	CA3028B MIN	CA3028B TYP	CA3028B MAX	CA3053 MIN	CA3053 TYP	CA3053 MAX	UNIT
Quiescent Operating Current (Figures 2, 3, 17, 18, 19)	I_6, I_8	V_{CC} = 6V, V_{EE} = -6V		0.8	1.25	2.0	1.0	1.25	1.5	-	-	-	mA
		V_{CC} = 12V, V_{EE} = -12V		2.0	3.3	5.0	2.5	3.3	4.0	-	-	-	mA
		V_{CC} = 9V		-	-	-	-	-	-	1.2	2.2	3.5	mA
		V_{CC} = 12V		-	-	-	-	-	-	2.0	3.3	5.0	mA
AGC Bias Current (Into Constant Current Source Terminal 7) (Figures 4, 20)	I_7	V_{CC} = 12V, V_{AGC} = 9V		-	1.28	-	-	1.28	-	-	-	-	mA
		V_{CC} = 12V, V_{AGC} = 12V		-	1.65	-	-	1.65	-	-	-	-	mA
		V_{CC} = 9V		-	-	-	-	-	-	-	1.15	-	mA
		V_{CC} = 12V		-	-	-	-	-	-	-	1.55	-	mA
Input Current (Terminal 7)	I_7	V_{CC} = 6V, V_{EE} = -6V		0.5	0.85	1.0	0.5	0.85	1.0	-	-	-	mA
		V_{CC} = 12V, V_{EE} = -12V		1.0	1.65	2.1	1.0	1.65	2.1	-	-	-	mA
Power Dissipation (Figures 2, 3, 21)	P_T	V_{CC} = 6V, V_{EE} = -6V		24	36	54	24	36	42	-	-	-	mW
		V_{CC} = 12V, V_{EE} = -12V		120	175	260	120	175	220	-	-	-	mW
		V_{CC} = 9V		-	-	-	-	-	-	-	50	80	mW
		V_{CC} = 12V		-	-	-	-	-	-	-	100	150	mW
DYNAMIC CHARACTERISTICS													
Power Gain (Figures 5, 6, 7, 22, 24, 26)	G_P	f = 100MHz	Cascode	16	20	-	16	20	-	-	-	-	dB
		V_{CC} = 9V	Diff. Amp.	14	17	-	14	17	-	-	-	-	dB
		f = 10.7MHz	Cascode (Note 8)	35	39	-	35	39	-	35	39	-	dB
		V_{CC} = 9V	Diff. Amp. (Note 8)	28	32	-	28	32	-	28	32	-	dB
Noise Figure (Figures 5, 6, 7, 23, 25, 26)	NF	f = 100MHz, V_{CC} = 9V	Cascode	-	7.2	9.0	-	7.2	9.0	-	-	-	dB
			Diff. Amp.	-	6.7	9.0	-	6.7	9.0	-	-	-	dB
Input Admittance (Figures 27, 28)	Y_{11}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	0.6 + j1.6	-	-	0.6 + j1.6	-	-	0.6 + j1.6	-	mS
			Diff. Amp.	-	0.5 + j0.5	-	-	0.5 + j0.5	-	-	0.5 + j0.5	-	mS
Reverse Transfer Admittance (Figures 29, 30)	Y_{12}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	0.0003 - j0	-	-	0.0003 - j0	-	-	0.0003 - j0	-	mS
			Diff. Amp.	-	0.01 - j0.0002	-	-	0.01 - j0.0002	-	-	0.01 - j0.0002	-	mS
Forward Transfer Admittance (Figures 31, 32)	Y_{21}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	99 - j18	-	-	99 - j18	-	-	99 - j18	-	mS
			Diff. Amp.	-	-37 + j0.5	-	-	-37 + j0.5	-	-	-37 + j0.5	-	mS
Output Admittance (Figures 33, 34)	Y_{22}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	0 + j0.08	-	-	0 + j0.08	-	-	0 + j0.08	-	mS
			Diff. Amp.	-	0.04 + j0.23	-	-	0.04 + j0.23	-	-	0.04 + j0.23	-	mS
Output Power (Untuned) (Figures 8, 35)	P_O	f = 10.7MHz, V_{CC} = 9V	Diff. Amp., 50Ω Input-Output	-	5.7	-	-	5.7	-	-	-	-	µW
AGC Range (Maximum Power Gain to Full Cut-off) (Figures 9, 36)	AGC	f = 10.7MHz, V_{CC} = 9V	Diff. Amp.	-	62	-	-	62	-	-	-	-	dB
Voltage Gain (Figures 10, 11, 37, 38)	A	f = 10.7MHz, V_{CC} = 9V, R_L = 1kΩ	Cascode	-	40	-	-	40	-	-	40	-	dB
			Diff. Amp.	-	30	-	-	30	-	-	30	-	dB
Differential Voltage Gain at f = 1kHz (Figure 12)	A	V_{CC} = 6V, V_{EE} = -6V, R_L = 2kΩ		-	-	-	35	38	42	-	-	-	dB
		V_{CC} = 12V, V_{EE} = -12V, R_L = 1.6kΩ		-	-	-	40	42.5	45	-	-	-	dB

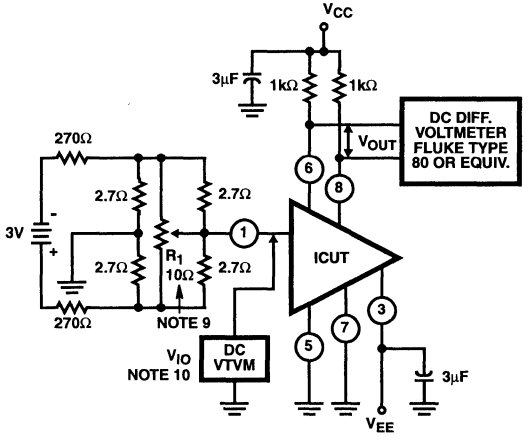
Electrical Specifications $T_A = 25^oC$ (Continued)

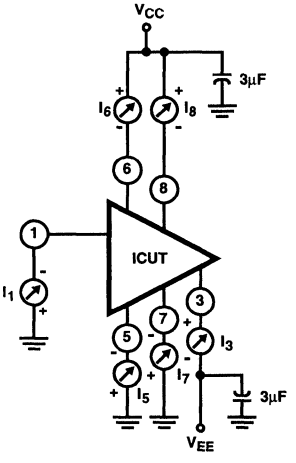
PARAMETER	SYMBOL	TEST CONDITIONS		CA3028A MIN	CA3028A TYP	CA3028A MAX	CA3028B MIN	CA3028B TYP	CA3028B MAX	CA3053 MIN	CA3053 TYP	CA3053 MAX	UNIT
Max Peak-to-Peak Output Voltage at f = 1kHz (Figure 12)	V_O(P-P)	V_{CC} = 6V, V_{EE} = -6V, R_L = 2kΩ		-	-	-	7.0	11.5	-	-	-	-	V_{P-P}
		V_{CC} = 12V, V_{EE} = -12V, R_L = 1.6kΩ		-	-	-	15	23	-	-	-	-	V_{P-P}
Bandwidth at -3dB Point (Figure 12)	BW	V_{CC} = 6V, V_{EE} = -6V, R_L = 2kΩ		-	-	-	-	7.3	-	-	-	-	MHz
		V_{CC} = 12V, V_{EE} = -12V, R_L = 1.6kΩ		-	-	-	-	8.0	-	-	-	-	MHz
Common Mode Input Voltage Range (Figure 13)	V_{CMR}	V_{CC} = 6V, V_{EE} = -6V		-	-	-	-2.5	-3.2 to -4.5	4	-	-	-	V
		V_{CC} = 12V, V_{EE} = -12V		-	-	-	-5.0	-7 to -9	7	-	-	-	V
Common Mode Rejection Ratio (Figure 13)	CMRR	V_{CC} = 6V, V_{EE} = -6V		-	-	-	60	110	-	-	-	-	dB
		V_{CC} = 12V, V_{EE} = -12V		-	-	-	60	90	-	-	-	-	dB
Input Impedance at f = 1kHz	Z_{IN}	V_{CC} = 6V, V_{EE} = -6V		-	-	-	-	5.5	-	-	-	-	kΩ
		V_{CC} = 12V, V_{EE} = -12V		-	-	-	-	3.0	-	-	-	-	kΩ
Peak-to-Peak Output Current	I_{P-P}	f = 10.7MHz, e_{IN} = 400mV, Diff. Amp.	V_{CC} = 9V	2.0	4.0	7.0	2.5	4.0	6.0	2.0	4.0	7.0	mA
			V_{CC} = 12V	3.5	6.0	10	4.5	6.0	8.0	3.5	6.0	10	mA

NOTE:

8. Does not apply to CA3053.

Test Circuits





NOTES:

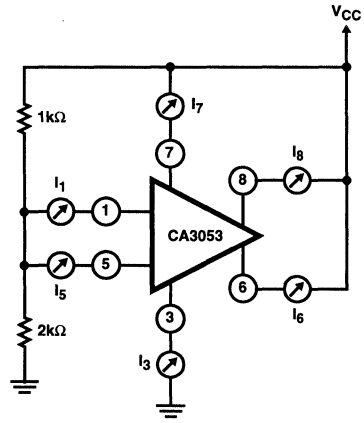
9. Adjust R_1 for V_{OUT} = 0V ±0.1V.
10. Record Input Offset Voltage.

FIGURE 1. INPUT OFFSET VOLTAGE TEST CIRCUIT FOR CA3028B

NOTE: Power Dissipation = $I_3V_{EE} + (I_6 + I_8)V_{CC}$.

FIGURE 2. INPUT OFFSET CURRENT, INPUT BIAS CURRENT, POWER DISSIPATION, AND QUIESCENT OPERATING CURRENT TEST CIRCUIT FOR CA3028A AND CA3028B

Test Circuits (Continued)



NOTE: Power Dissipation = $V_{CC}I_3$.

FIGURE 3. INPUT BIAS CURRENT, POWER DISSIPATION AND QUIESCENT OPERATING CURRENT TEST CIRCUIT FOR CA3053

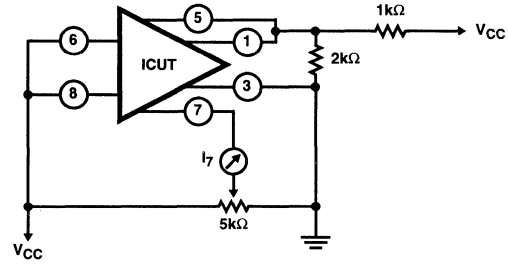
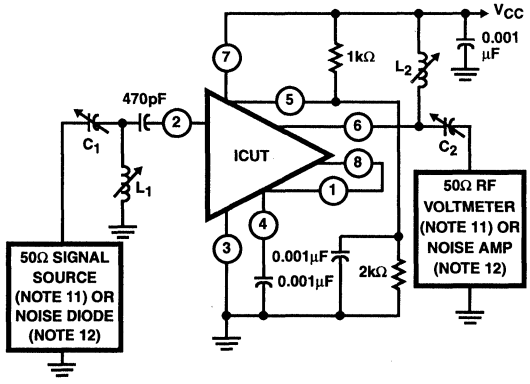


FIGURE 4. AGC BIAS CURRENT TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

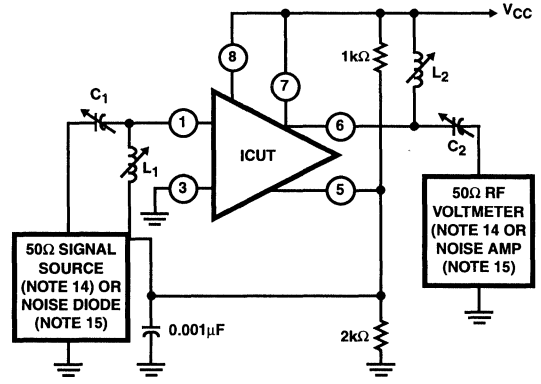


f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (µH)	L_2 (µH)
10.7	20 - 60	20 - 60	3 - 5	3 - 5
100	3 - 30	3 - 30	0.1 - 0.25	0.15 - 0.3

NOTES:

11. For Power Gain Test.
12. For Noise Figure Test.
13. 10.7MHz Power Gain Test Only.

FIGURE 5. POWER GAIN AND NOISE FIGURE TEST CIRCUIT (CASCODE CONFIGURATION) FOR CA3028A, CA3028B AND CA3053 (NOTE 3)



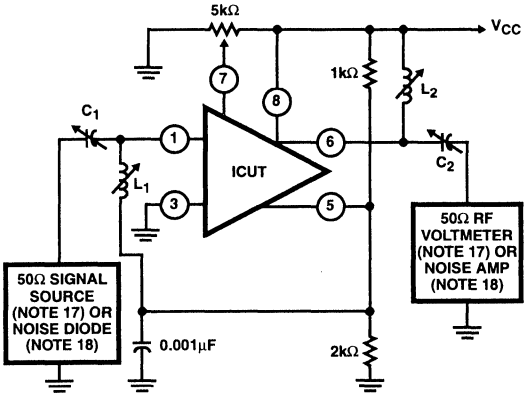
f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (µH)	L_2 (µH)
10.7	30 - 60	20 - 50	3 - 6	3 - 6
100	2 - 15	2 - 15	0.2 - 0.5	0.2 - 0.5

NOTES:

14. For Power Gain Test.
15. For Noise Figure Test.
16. 10.7MHz Power Gain Test Only.

FIGURE 6. POWER GAIN AND NOISE FIGURE TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION AND TERMINAL 7 CONNECTED TO VCC) FOR CA3028A, CA3028B AND CA3053 (NOTE 3)

Test Circuits (Continued)



f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (μH)	L_2 (μH)
10.7	30 - 60	20 - 50	3 - 6	3 - 6
100	2 - 15	2 - 15	0.2 - 0.5	0.2 - 0.5

NOTES:

17. For Power Gain Test.

18. For Noise Figure Test.

FIGURE 7. POWER GAIN AND NOISE FIGURE TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

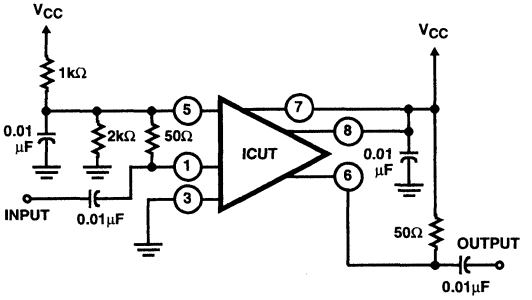
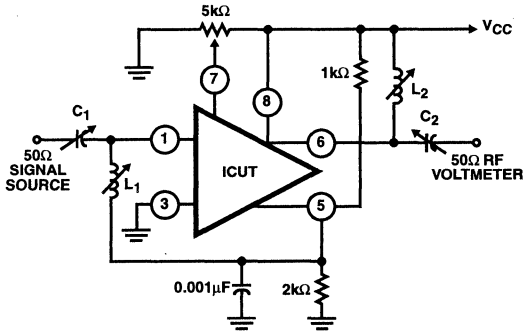


FIGURE 8. OUTPUT POWER TEST CIRCUIT FOR CA3028A AND CA3028B



f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (μH)	L_2 (μH)
10.7	30 - 60	20 - 50	3 - 6	3 - 6
100	2 - 15	2 - 15	0.2 - 0.5	0.2 - 0.5

FIGURE 9. AGC RANGE TEST CIRCUIT (DIFFERENTIAL AMPLIFIER) FOR CA3028A AND CA3028B

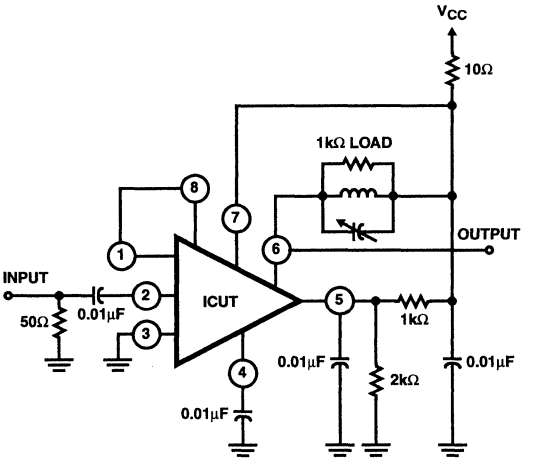


FIGURE 10. TRANSFER CHARACTERISTIC (VOLTAGE GAIN) TEST CIRCUIT (10.7MHz) CASCODE CONFIGURATION FOR CA3028A, CA3028B AND CA3053

Test Circuits (Continued)

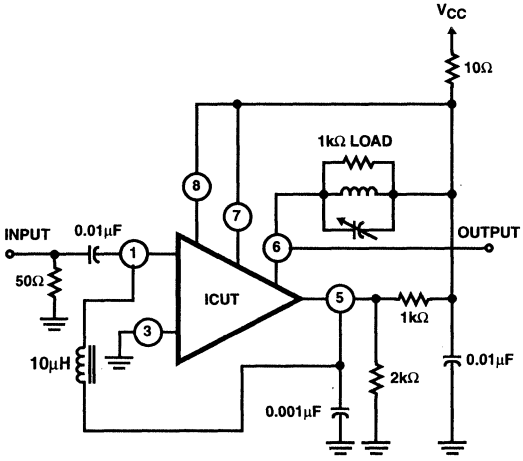
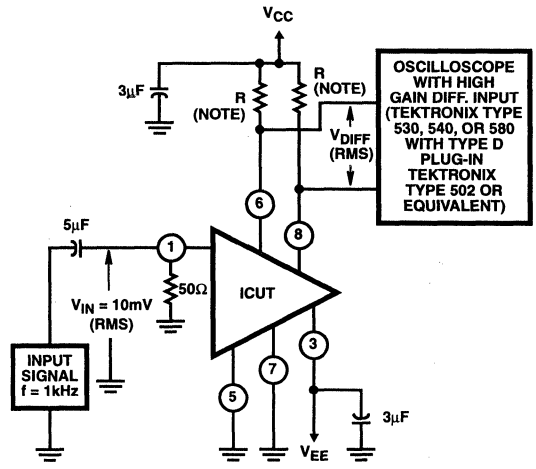
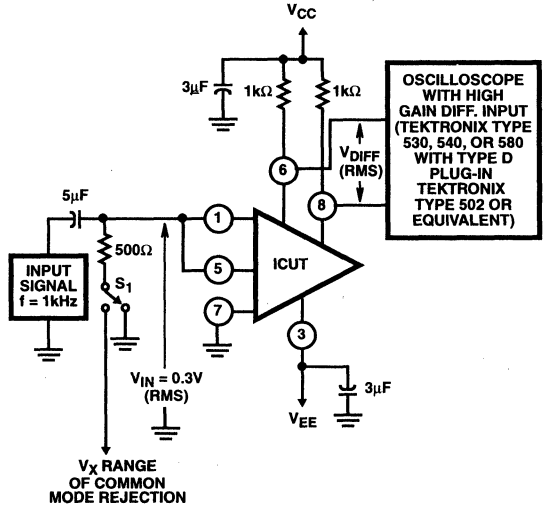


FIGURE 11. TRANSFER CHARACTERISTIC (VOLTAGE GAIN) TEST CIRCUIT (10.7MHz) DIFFERENTIAL AMPLIFIER CONFIGURATION FOR CA3028A, CA3028B AND CA3053



NOTE: For R = 1.6kΩ: V_{CC} = 12V, V_{EE} = -12V
For R = 2.0kΩ: V_{CC} = 6V, V_{EE} = -6V.

FIGURE 12. DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AND BANDWIDTH TEST CIRCUIT FOR CA3028B



NOTES:

19. For CMR test: S_1 to GND.
20. For Input Common Mode Voltage Range Test: S_1 to V_X.
21. Common Mode Rejection Ratio = $20\log_{10}\frac{(A)(2)(0.3)}{V_{DIFF(RMS)}}$

A = Single-Ended Voltage Gain.

FIGURE 13. COMMON MODE REJECTION RATIO AND COMMON MODE INPUT VOLTAGE RANGE TEST CIRCUIT FOR CA3028B

Typical Performance Curves

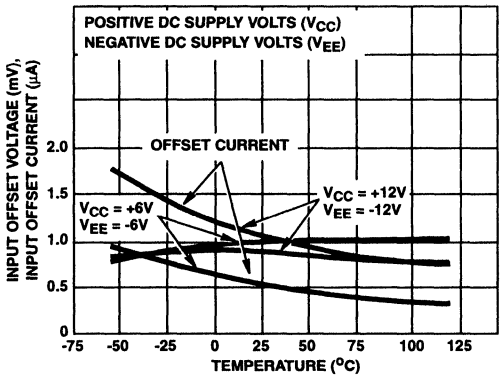


FIGURE 14. INPUT OFFSET VOLTAGE AND INPUT OFFSET CURRENT FOR CA3028B vs TEMPERATURE

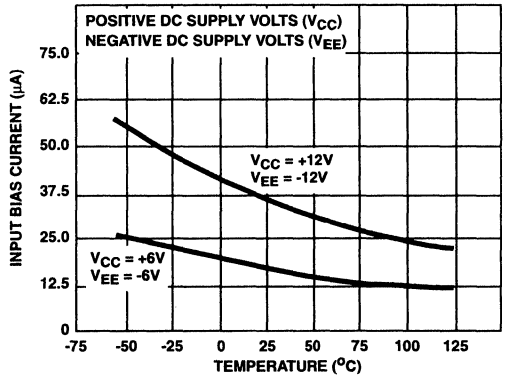


FIGURE 15. INPUT BIAS CURRENT vs TEMPERATURE FOR CA3028A AND CA3028B

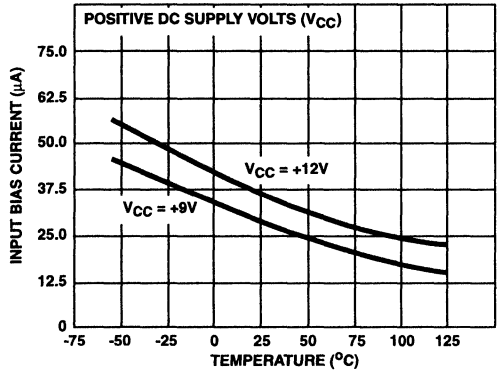


FIGURE 16. INPUT BIAS CURRENT vs TEMPERATURE FOR CA3053

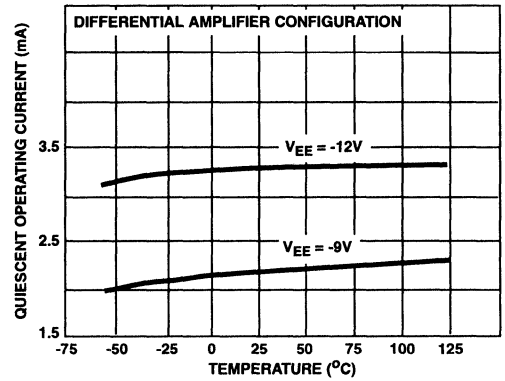


FIGURE 17. QUIESCENT OPERATING CURRENT vs TEMPERATURE FOR CA3028A AND CA3028B

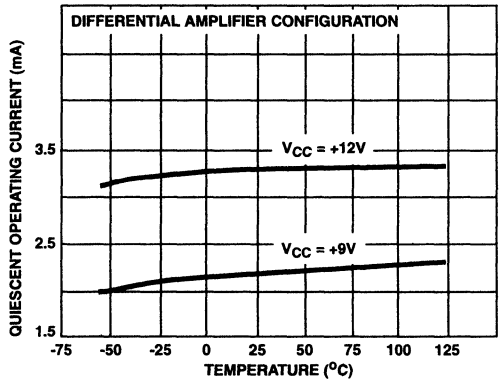


FIGURE 18. QUIESCENT OPERATING CURRENT vs TEMPERATURE FOR CA3053

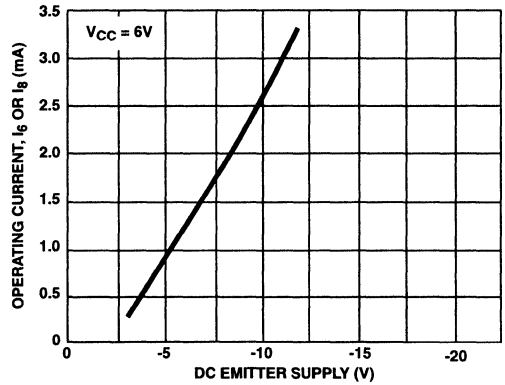


FIGURE 19. OPERATING CURRENT vs V_{EE} VOLTAGE FOR CA3028A AND CA3028B

Typical Performance Curves (Continued)

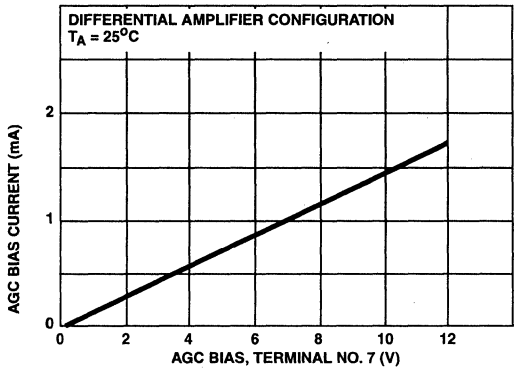


FIGURE 20. AGC BIAS CURRENT vs BIAS VOLTAGE (TERMINAL 7) FOR CA3028A AND CA3028B

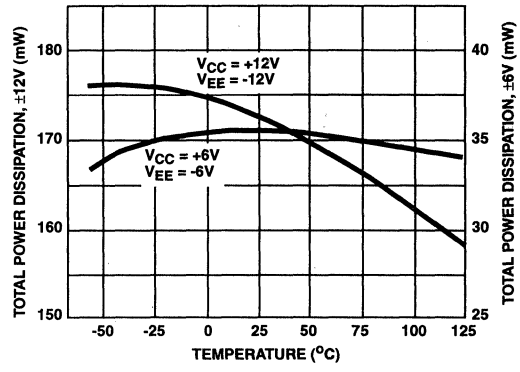


FIGURE 21. POWER DISSIPATION vs TEMPERATURE FOR CA3028A AND CA3028B

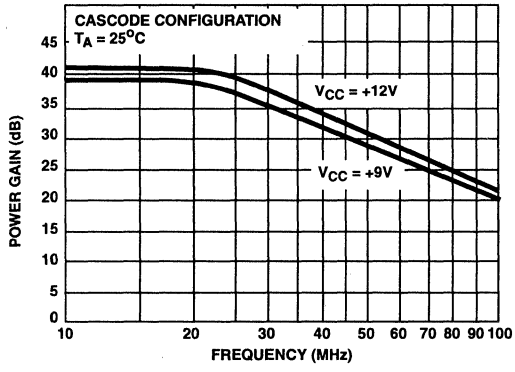


FIGURE 22. POWER GAIN vs FREQUENCY (CASCODE CONFIGURATION) FOR CA3028A AND CA3028B

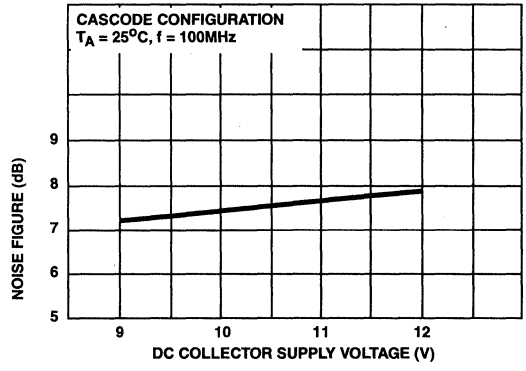


FIGURE 23. 100MHz NOISE FIGURE vs COLLECTOR SUPPLY VOLTAGE (CASCODE CONFIGURATION) FOR CA3028A AND CA3028B

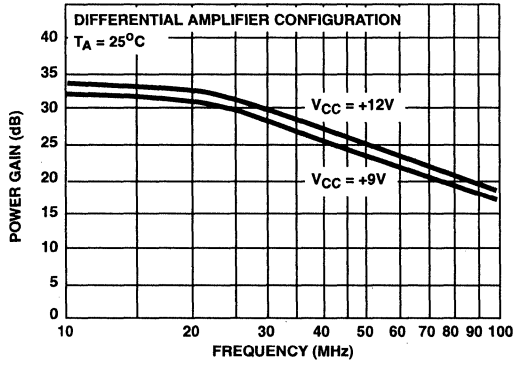


FIGURE 24. POWER GAIN vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

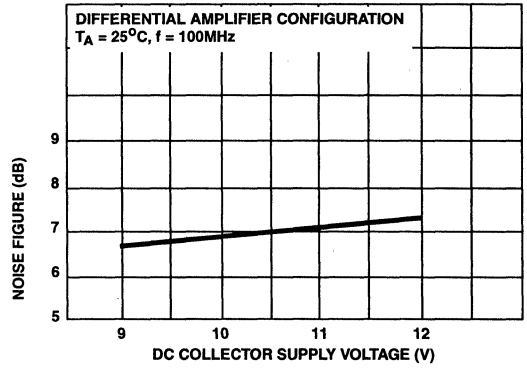


FIGURE 25. 100MHz NOISE FIGURE vs COLLECTOR SUPPLY VOLTAGE (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

Typical Performance Curves (Continued)

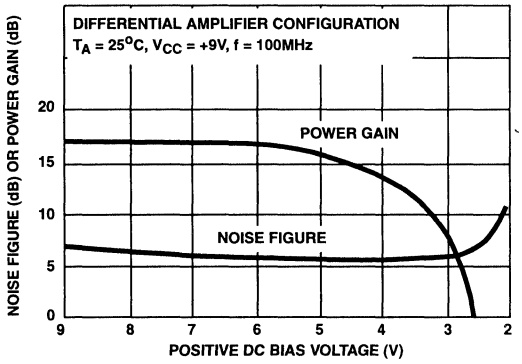


FIGURE 26. 100MHz NOISE FIGURE AND POWER GAIN vs BASE-TO-EMITTER BIAS VOLTAGE (TERMINAL 7) FOR CA3028A AND CA3028B

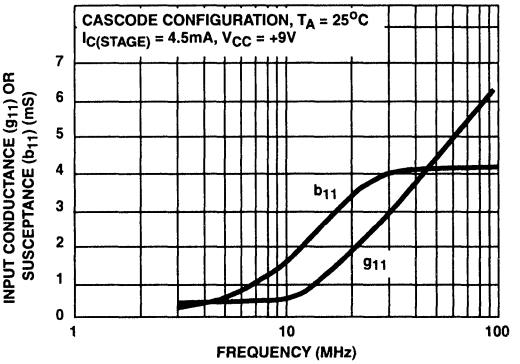


FIGURE 27. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY (CASCODE CONFIGURATION)

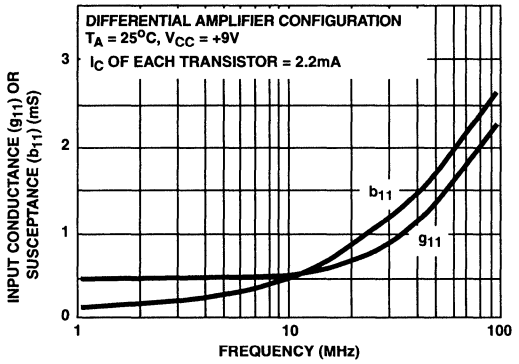


FIGURE 28. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

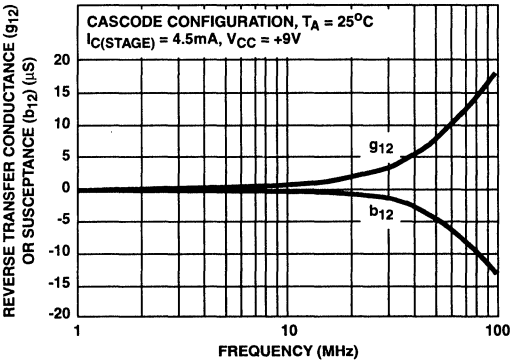


FIGURE 29. REVERSE TRANSADMITTANCE (Y_{12}) vs FREQUENCY (CASCODE CONFIGURATION)

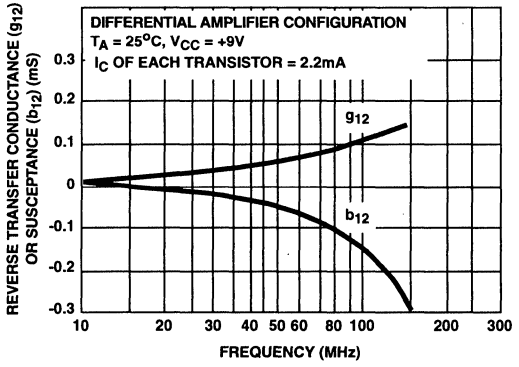


FIGURE 30. REVERSE TRANSADMITTANCE (Y_{12}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

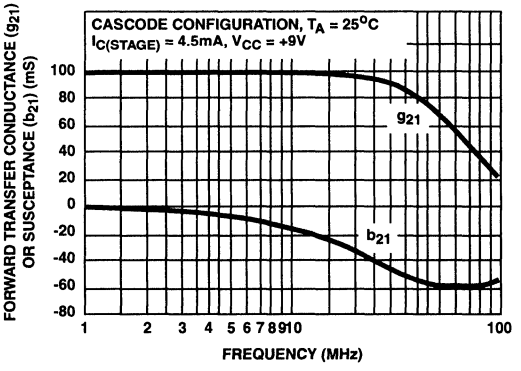


FIGURE 31. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY (CASCODE CONFIGURATION)

Typical Performance Curves (Continued)

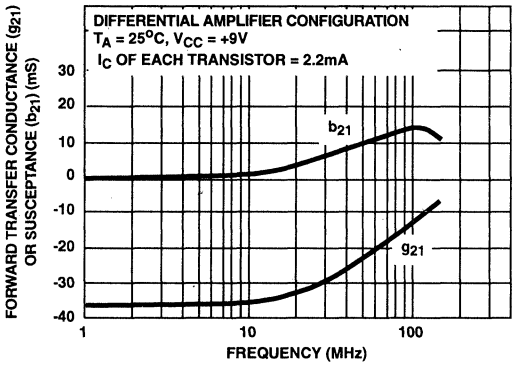


FIGURE 32. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

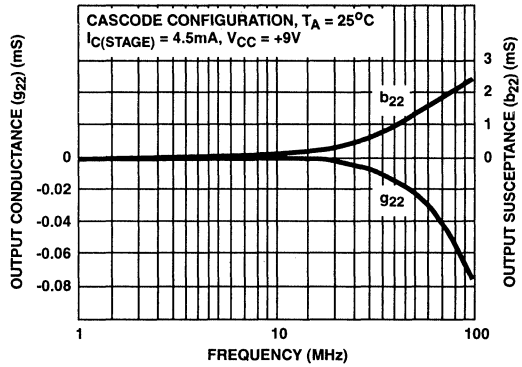


FIGURE 33. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY (CASCODE CONFIGURATION)

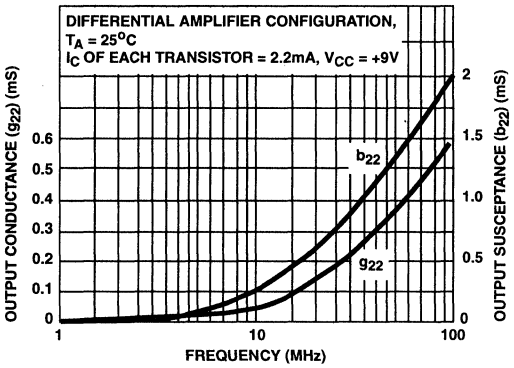


FIGURE 34. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

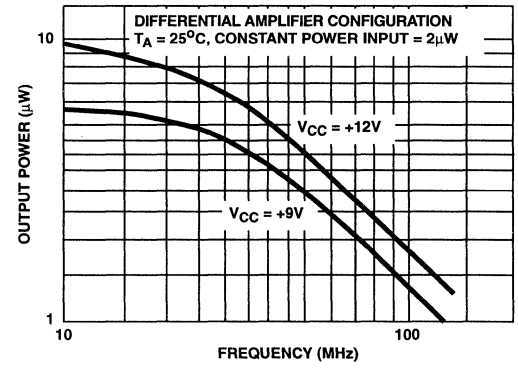


FIGURE 35. OUTPUT POWER vs FREQUENCY - 50Ω INPUT AND 50Ω OUTPUT (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

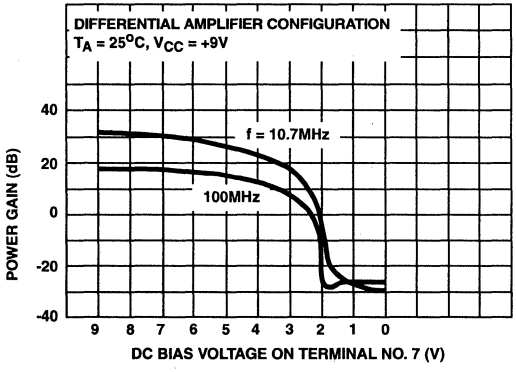


FIGURE 36. AGC CHARACTERISTICS FOR CA3028A AND CA3028B

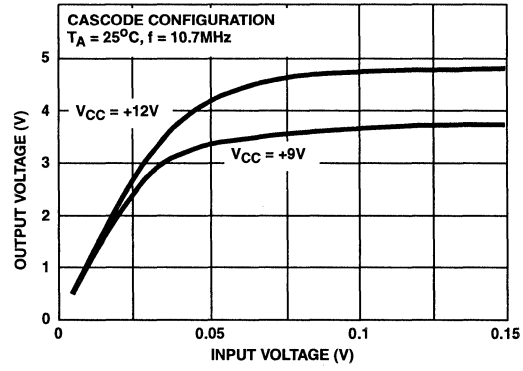


FIGURE 37. TRANSFER CHARACTERISTICS (CASCODE CONFIGURATION)

Typical Performance Curves (Continued)

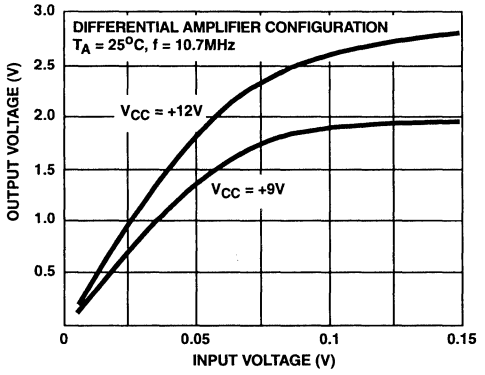


FIGURE 38. TRANSFER CHARACTERISTICS (DIFFERENTIAL AMPLIFIER CONFIGURATION)

Glossary of Terms

AGC Bias Current

The current drawn by the device from the AGC voltage source, at maximum AGC voltage.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

Common Mode Rejection Ratio

The ratio of the full differential voltage gain to the common mode voltage gain.

Power Dissipation

The total power drain of the device with no signal applied and no external load current.

Input Bias Current

The average value (one half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Voltage

The difference in the DC voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Quiescent Operating Current

The average (DC) value of the current in either output terminal.

Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at AC ground.

HARRIS SEMICONDUCTOR

CA3039

November 1996

Diode Array

Features

- Six Matched Diodes on a Common Substrate
- Excellent Reverse Recovery Time . . . . . 1ns (Typ)
- V_F Match . . . . . 5mV (Max)
- Low Capacitance . . . . . C_D = 0.65pF (Typ) at V_R = -2V

Applications

- Ultra-Fast Low Capacitance Matched Diodes for Applications in Communications and Switching Systems
- Balanced Modulators or Demodulators
- Ring Modulators
- High Speed Diode Gates
- Analog Switches

Description

The CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

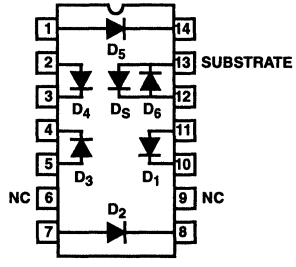
For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

Ordering Information

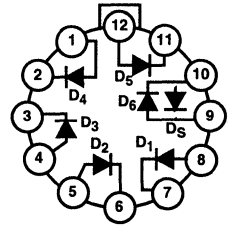
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3039	-55 to 125	12 Pin Metal Can	T12.B
CA3039M	-55 to 125	14 Ld SOIC	M14.15
CA3039M96	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinouts

CA3039
(SOIC)
TOP VIEW



CA3039
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Inverse Voltage (PIV) for: D_1 - D_5 ..... 5V
D_6 ..... 0.5V
Diode-to-Substrate Voltage (V_{DI}) for D_1 - D_5 ..... 20V, -1V
(Terminal 1, 4, 5, 8 or 12 to Terminal 10)
DC Forward Current (I_F) 25mA
Recurrent Forward Current (I_F) 100mA
Forward Surge Current ($I_{F(SURGE)}$) 100mA

Operating Conditions

Temperature Range ..... -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	200	120
SOIC Package	220	N/A

Maximum Power Dissipation (Any One Diode) 100mW
Maximum Junction Temperature (Metal Can Package) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25°C; Characteristics apply for each diode unit, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Forward Voltage Drop (Figure 1)	V_F	I_F = 50µA	-	0.65	0.69	V
		I_F = 1mA	-	0.73	0.78	V
		I_F = 3mA	-	0.76	0.80	V
		I_F = 10mA	-	0.81	0.90	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = -10µA	5	7	-	V
DC Reverse Breakdown Voltage Between Any Diode Unit and Substrate	$V_{(BR)R}$	I_R = -10µA	20	-	-	V
DC Reverse (Leakage) Current (Figure 2)	I_R	V_R = -4V	-	0.016	100	nA
DC Reverse (Leakage) Current Between Any Diode Unit and Substrate (Figure 3)	I_R	V_R = -10V	-	0.022	100	nA
Magnitude of Diode Offset Voltage (Note 2) (Figure 1)	$\lvert V_{F1} - V_{F2} \rvert$	I_F = 1mA	-	0.5	5.0	mV
Temperature Coefficient of $\lvert V_{F1} - V_{F2} \rvert$ (Figure 4)	$\frac{\Delta \lvert V_{F1} - V_{F2} \rvert}{\Delta T}$	I_F = 1mA	-	1.0	-	µV/°C
Temperature Coefficient of Forward Drop (Figure 5)	$\frac{\Delta V_F}{\Delta T}$	I_F = 1mA	-	-1.9	-	mV/°C
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1mA	-	0.65	-	V
Reverse Recovery Time	t_{RR}	I_F = 10mA, I_R = -10mA	-	1.0	-	ns
Diode Resistance (Figure 6)	R_D	f = 1kHz, I_F = 1mA	25	30	45	Ω
Diode Capacitance (Figure 7)	C_D	V_R = -2V, I_F = 0	-	0.65	-	pF
Diode-to-Substrate Capacitance (Figure 8)	C_{DI}	V_{DI} = 4V, I_F = 0	-	3.2	-	pF

NOTE:

2. Magnitude of Diode Offset Voltage is the difference in DC Forward Voltage Drops of any two diode units.

Typical Performance Curves

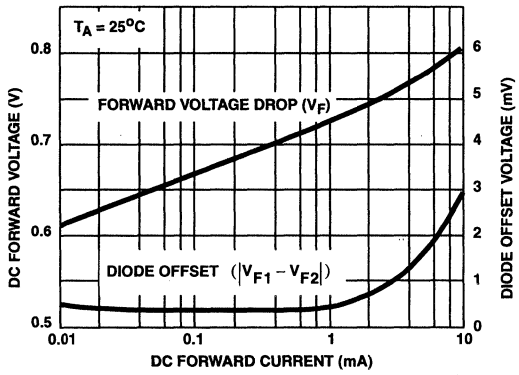


FIGURE 1. DC FORWARD VOLTAGE DROP (ANY DIODE) AND DIODE OFFSET VOLTAGE vs DC FORWARD CURRENT

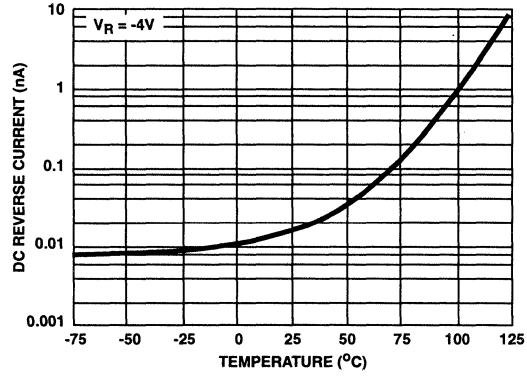


FIGURE 2. DC REVERSE (LEAKAGE) CURRENT (D_1 - D_5) vs TEMPERATURE

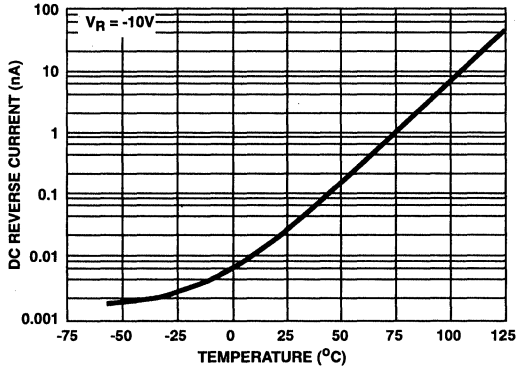


FIGURE 3. DC REVERSE (LEAKAGE) CURRENT BETWEEN D_1, D_2, D_3, D_4, D_5 AND SUBSTRATE vs TEMPERATURE

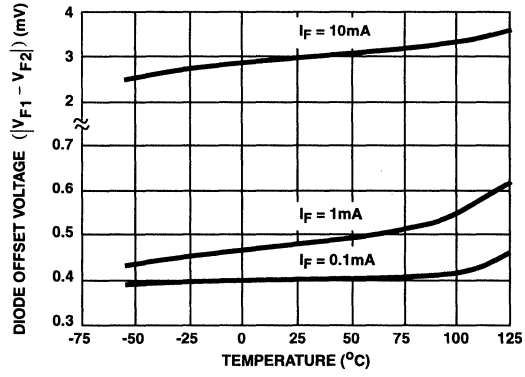


FIGURE 4. DIODE OFFSET VOLTAGE (ANY DIODE) vs TEMPERATURE

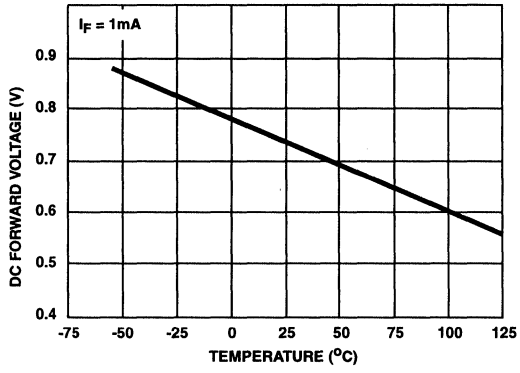


FIGURE 5. DC FORWARD VOLTAGE DROP (ANY DIODE) vs TEMPERATURE

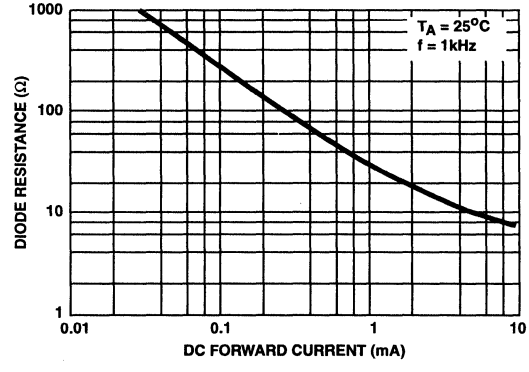


FIGURE 6. DIODE RESISTANCE (ANY DIODE) vs DC FORWARD CURRENT

Typical Performance Curves (Continued)

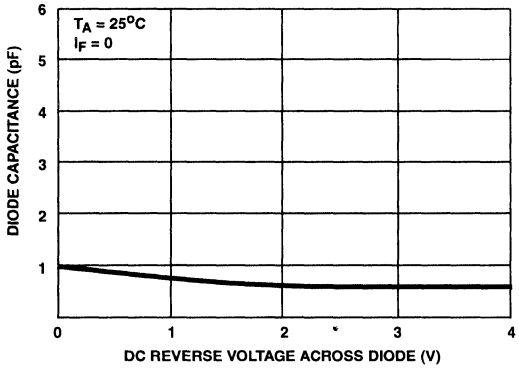


FIGURE 7. DIODE CAPACITANCE (D_1 - D_5) vs REVERSE VOLTAGE

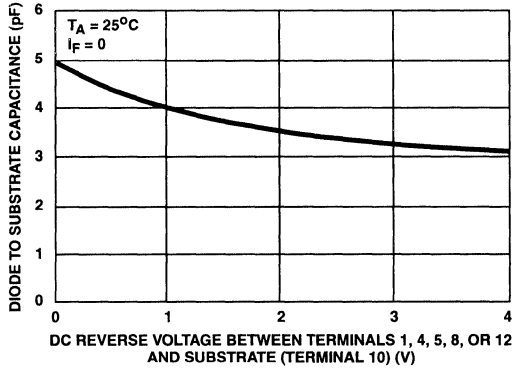


FIGURE 8. DIODE-TO-SUBSTRATE CAPACITANCE vs REVERSE VOLTAGE

HARRIS SEMICONDUCTOR

CA3045, CA3046

General Purpose NPN Transistor Arrays

November 1996

Features

- Two Matched Transistors
  - V_{BE} Match ..... ±5mV
  - I_{IO} Match ..... 2μA (Max)
- Low Noise Figure ..... 3.2dB (Typ) at 1kHz
- 5 General Purpose Monolithic Transistors
- Operation From DC to 120MHz
- Wide Operating Current Range
- Full Military Temperature Range

Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair for Low Power Applications at Frequencies from DC Through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

Description

The CA3045 and CA3046 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

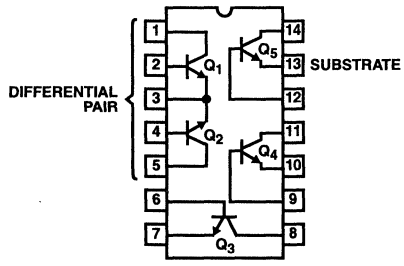
The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3045	-55 to 125	14 Ld SBDIP	D14.3
CA3045F	-55 to 125	14 Ld CERDIP	F14.3
CA3046	-55 to 125	14 Ld PDIP	E14.3
CA3046M (3046)	-55 to 125	14 Ld SOIC	M14.15
CA3046M96 (3046)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinout

CA3045, (CERDIP, SBDIP)
CA3046 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Collector-to-Emitter Voltage (V_{CEO}) 15V
Collector-to-Base Voltage (V_{CBO}) 20V
Collector-to-Substrate Voltage (V_{CIO}, Note 1) 20V
Emitter-to-Base Voltage (V_{EBO}) 5V
Collector Current (I_C) 50mA

Operating Conditions

Temperature Range ..... -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	180	N/A
CERDIP Package	150	75
SBDIP Package	125	60
SOIC Package	220	N/A

Maximum Power Dissipation (Any One Transistor) 300mW
Maximum Junction Temperature (Hermetic Packages) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$T_A = 25°C$, characteristics apply for each transistor in CA3045 and CA3046 as specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$		20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$		15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$		5	7	-	V
Collector Cutoff Current (Figure 1)	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$		-	0.002	40	nA
Collector Cutoff Current (Figure 2)	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$		-	See Fig. 2	0.5	µA
Forward Current Transfer Ratio (Static Beta) (Note 3) (Figure 3)	h_{FE}	$V_{CE} = 3V$	$I_C = 10mA$	-	100	-	-
			$I_C = 1mA$	40	100	-	-
			$I_C = 10\mu A$	-	54	-	-
Input Offset Current for Matched Pair Q_1 and Q_2. $\|I_{IO1} - I_{IO2}\|$ (Note 3) (Figure 4)		$V_{CE} = 3V$, $I_C = 1mA$		-	0.3	2	µA
Base-to-Emitter Voltage (Note 3) (Figure 5)	V_{BE}	$V_{CE} = 3V$	$I_E = 1mA$	-	0.715	-	V
			$I_E = 10mA$	-	0.800	-	V
Magnitude of Input Offet Voltage for Differential Pair $\|V_{BE1} - V_{BE2}\|$ (Note 3) (Figures 5, 7)		$V_{CE} = 3V$, $I_C = 1mA$		-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\|V_{BE3} - V_{BE4}\|$, $\|V_{BE4} - V_{BE5}\|$, $\|V_{BE5} - V_{BE3}\|$ (Note 3) (Figures 5, 7)		$V_{CE} = 3V$, $I_C = 1mA$		-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 3V$, $I_C = 1mA$		-	-1.9	-	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1mA$, $I_C = 10mA$		-	0.23	-	V
Temperature Coefficient: Magnitude of Input Offset Voltage (Figure 7)	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$	$V_{CE} = 3V$, $I_C = 1mA$		-	1.1	-	µV/°C

Electrical Specifications $T_A = 25^oC$, characteristics apply for each transistor in CA3045 and CA3046 as specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Low Frequency Noise Figure (Figure 9)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, Source Resistance = 1kΩ	-	3.25	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics						
Forward Current Transfer Ratio (Figure 11)	h_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	110	-	-
Short Circuit Input Impedance (Figure 11)	h_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 11)	h_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	15.6	-	μS
Open Circuit Reverse Voltage Transfer Ratio (Figure 11)	h_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	1.8×10^{-4}	-	-
Admittance Characteristics						
Forward Transfer Admittance (Figure 12)	Y_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	31 - j1.5	-	-
Input Admittance (Figure 13)	Y_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	0.3 + j0.04	-	-
Output Admittance (Figure 14)	Y_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	0.001 + j0.03	-	-
Reverse Transfer Admittance (Figure 15)	Y_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	See Fig. 14	-	-
Gain Bandwidth Product (Figure 16)	f_T	V_{CE} = 3V, I_C = 3mA	300	550	-	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3V, I_C = 0	-	2.8	-	pF

NOTE:

3. Actual forcing current is via the emitter for this test.

Typical Performance Curves

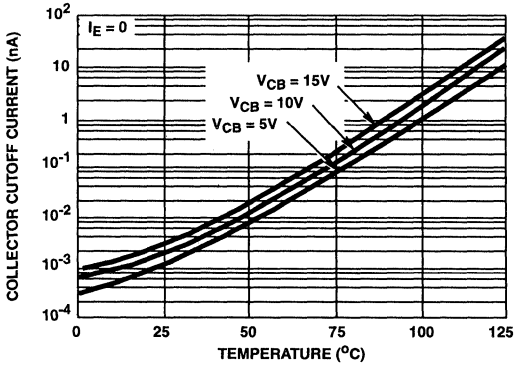


FIGURE 1. TYPICAL COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

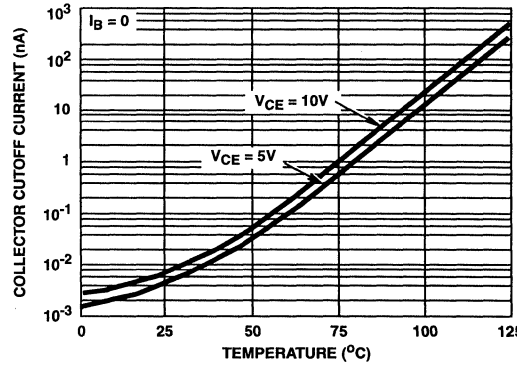


FIGURE 2. TYPICAL COLLECTOR-TO-EMITTER CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

Typical Performance Curves (Continued)

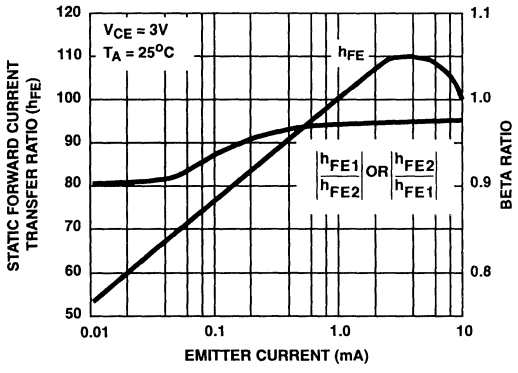


FIGURE 3. TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO AND BETA RATIO FOR Q_1 AND Q_2 vs EMITTER CURRENT

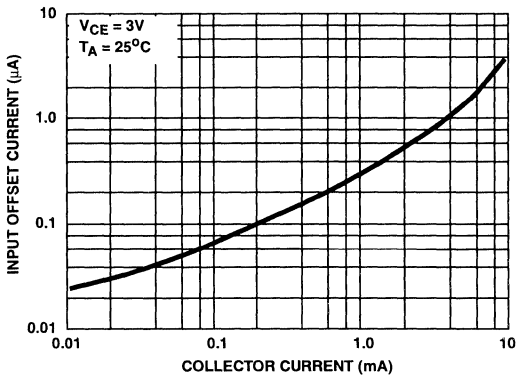


FIGURE 4. TYPICAL INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q_1Q_2 vs COLLECTOR CURRENT

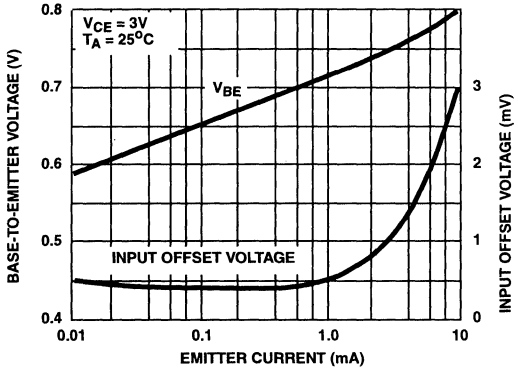


FIGURE 5. TYPICAL STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTICS AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs EMITTER CURRENT

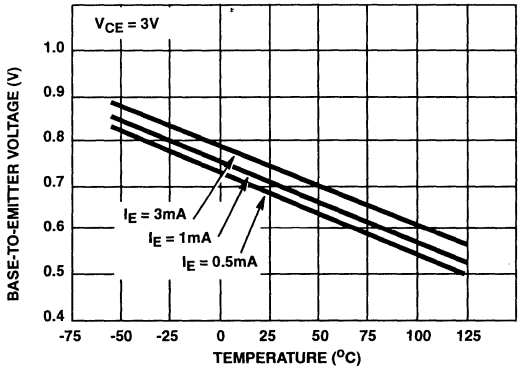


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC vs TEMPERATURE FOR EACH TRANSISTOR

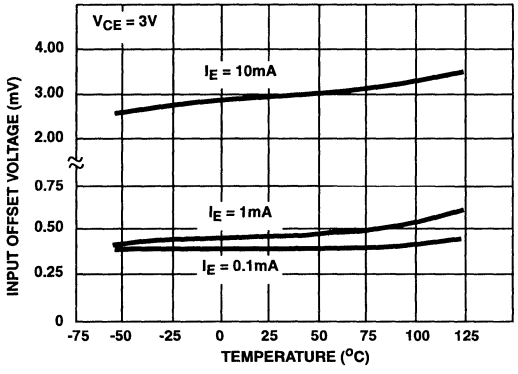


FIGURE 7. TYPICAL INPUT OFFSET VOLTAGE CHARACTERISTICS FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs TEMPERATURE

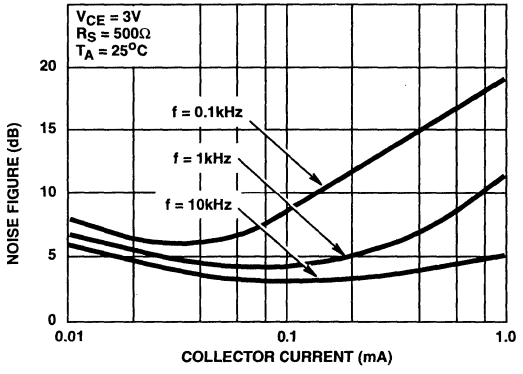


FIGURE 8. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

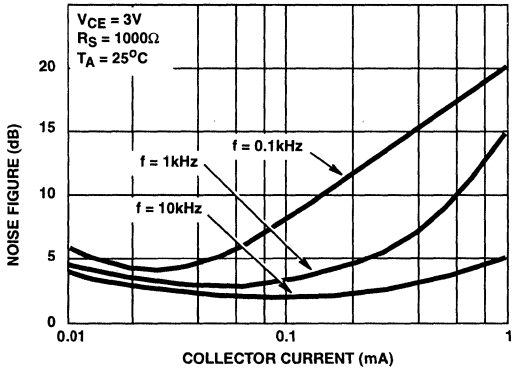


FIGURE 9. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

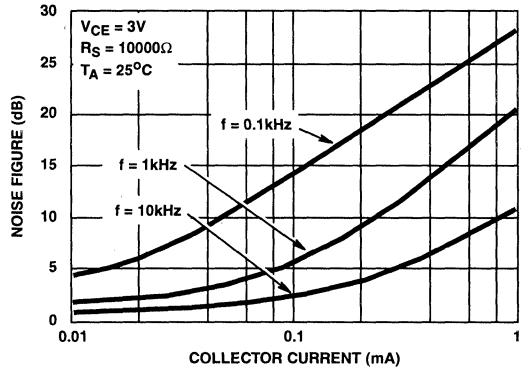


FIGURE 10. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

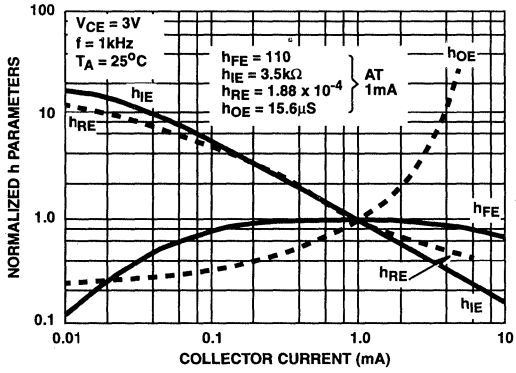


FIGURE 11. TYPICAL NORMALIZED FORWARD CURRENT TRANSFER RATIO, SHORT CIRCUIT INPUT IMPEDANCE, OPEN CIRCUIT OUTPUT IMPEDANCE, AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER RATIO vs COLLECTOR CURRENT

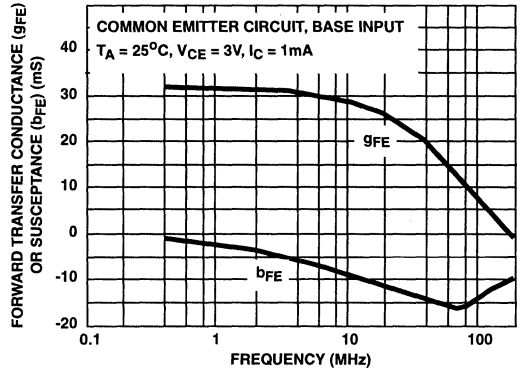


FIGURE 12. TYPICAL FORWARD TRANSFER ADMITTANCE vs FREQUENCY

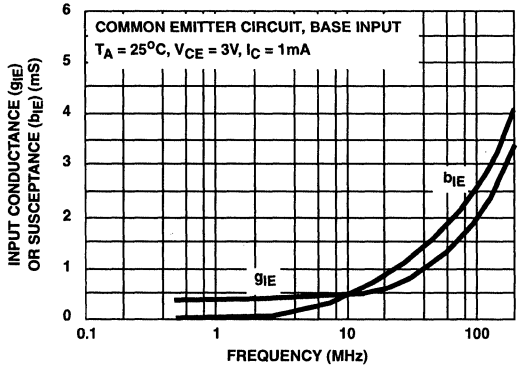


FIGURE 13. TYPICAL INPUT ADMITTANCE vs FREQUENCY

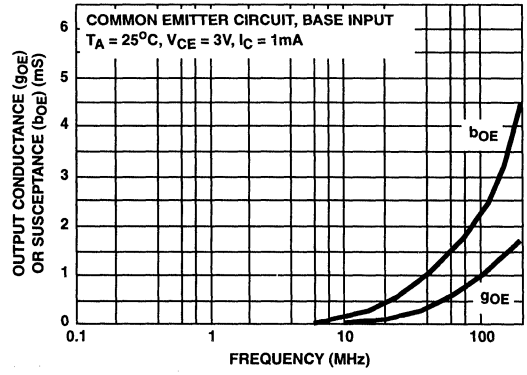


FIGURE 14. TYPICAL OUTPUT ADMITTANCE vs FREQUENCY

Typical Performance Curves (Continued)

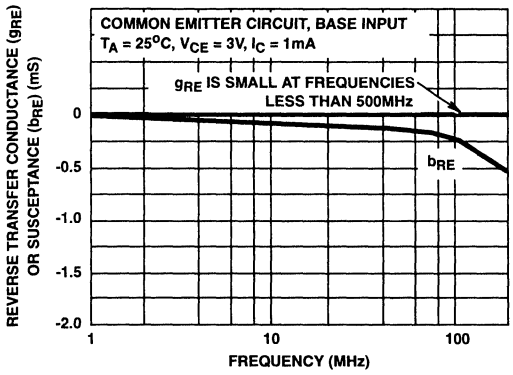


FIGURE 15. TYPICAL REVERSE TRANSFER ADMITTANCE vs FREQUENCY

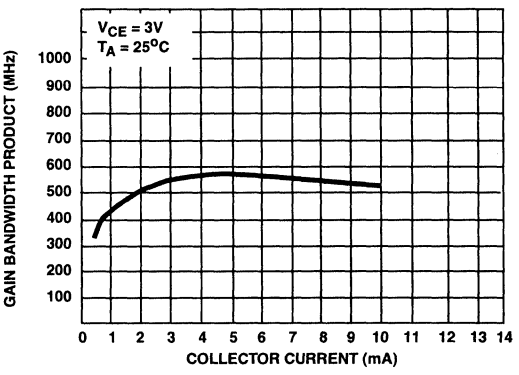


FIGURE 16. TYPICAL GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

HARRIS SEMICONDUCTOR

CA3049, CA3102

Dual High Frequency Differential Amplifiers For Low Power Applications Up to 500MHz

November 1996

Features

- Power Gain 23dB (Typ) 200MHz
- Noise Figure 4.6dB (Typ)..... 200MHz
- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Full Military Temperature Range ..... -55°C to 125°C

Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations - RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Balanced Mixers
- Synthesizers
- Balanced (Push-Pull) Cascode Amplifiers
- Sense Amplifiers

Description

The CA3049T and CA3102 consist of two independent differential amplifiers with associated constant current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 1GHz. These feature make the CA3049T and CA3102 useful from DC to 500MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3049T and CA3102 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

The CA3102 is like the CA3049T except that it has a separate substrate connection for greater design flexibility.

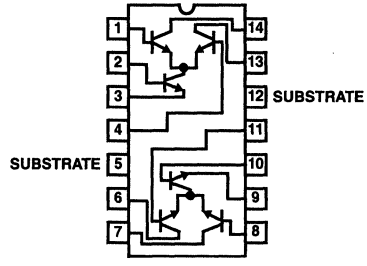
Formerly Developmental Type No. TA6228.

Ordering Information

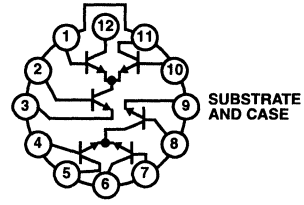
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3049T	-55 to 125	12 Pin Metal Can	T12.B
CA3102E	-55 to 125	14 Ld PDIP	E14.3
CA3102M (3102)	-55 to 125	14 Ld SOIC	M14.15
CA3102M96 (3102)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinouts

CA3102
(PDIP, SOIC)
TOP VIEW



CA3049
(METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, I_C 50mA

Operating Conditions

Temperature Range ..... -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
Metal Can Package	225
PDIP Package	130
SOIC Package	140

Maximum Power Dissipation (Any One Transistor) 300mW
Maximum Junction Temperature (Can Package) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3049T and CA3102 is isolated from the substrate by an integral diode. The substrate (Terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25°C$

PARAMETER	SYMBOL	TEST CONDITIONS	CA3102 MIN	CA3102 TYP	CA3102 MAX	CA3049 MIN	CA3049 TYP	CA3049 MAX	UNIT
DC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER									
Input Offset Voltage (Figures 1, 4)	V_{IO}		-	0.25	5.0	-	0.25	-	mV
Input Offset Current (Figure 1)	I_{IO}	$I_3 = I_9 = 2mA$	-	0.3	3.0	-	0.3	-	µA
Input Bias Current (Figures 1, 5)	I_B		-	13.5	33	-	13.5	33	µA
Temperature Coefficient Magnitude of Input Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	1.1	-	-	1.1	-	µV/°C
DC CHARACTERISTICS FOR EACH TRANSISTOR									
DC Forward Base-to-Emitter Voltage (Figure 6)	VBE	$V_{CE} = 6V$, $I_C = 1mA$	674	774	874	-	774	-	mV
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 6V$, $I_C = 1mA$	-	-0.9	-	-	-0.9	-	mV/°C
Collector Cutoff Current (Figure 7)	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	0.0013	100	-	0.0013	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	15	24	-	15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10µA$, $I_E = 0$	20	60	-	20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10µA$, $I_B = I_E = 0$	20	60	-	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10µA$, $I_C = 0$	5	7	-	5	7	-	V
DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER									
1/f Noise Figure (For Single Transistor) (Figure 12)	NF	$f = 100kHz$, $R_S = 500Ω$, $I_C = 1mA$	-	1.5	-	-	1.5	-	dB
Gain Bandwidth Product (For Single Transistor) (Figure 11)	f_T	$V_{CE} = 6V$, $I_C = 5mA$	-	1.35	-	-	1.35	-	GHz
Collector-Base Capacitance (Figure 8)	C_{CB}	$I_C = 0$, $V_{CB} = 5V$, Note 3	-	0.28	-	-	0.28	-	pF
		$I_C = 0$, $V_{CB} = 5V$, Note 4	-	0.15	-	-	0.28	-	pF
Collector-Substrate Capacitance (Figure 8)	C_{CI}	$I_C = 0$, $V_{CI} = 5V$	-	1.65	-	-	1.65	-	pF

Electrical Specifications $T_A = 25^oC$ **(Continued)**

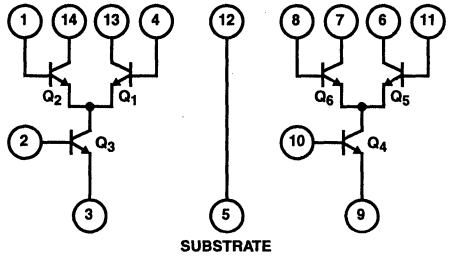
PARAMETER	SYMBOL	TEST CONDITIONS		CA3102 MIN	CA3102 TYP	CA3102 MAX	CA3049 MIN	CA3049 TYP	CA3049 MAX	UNIT
Common Mode Rejection Ratio	CMRR	$I_3 = I_9 = 2mA$		-	100	-	-	100	-	dB
AGC Range, One Stage (Figure 2)	AGC	Bias Voltage = -6V		-	75	-	-	75	-	dB
Voltage Gain, Single-Ended Output (Figures 2, 9, 10)	A	Bias Voltage = -4.2V, f = 10MHz		18	22	-	-	22	-	dB
Insertion Power Gain (Figure 3)	G_P	V_{CC} = 12V, For Cascode Configuration $I_3 = I_9 = 2mA$. For Diff. Amp. Configuration $I_3 = I_9 = 4mA$ (Each Collector $I_C \cong 2mA$) f = 200MHz	Cascode	-	23	-	-	23	-	dB
Noise Figure (Figure 3)	NF		Cascode	-	4.6	-	-	4.6	-	dB
Input Admittance	Y_{11}		Cascode (Figures 14, 16, 18)	-	1.5 + j2.45	-	-	1.5 + j2.45	-	mS
			Diff. Amp. (Figures 15, 17, 19)	-	0.878 + j1.3	-	-	0.878 + j1.3	-	mS
Reverse Transfer Admittance	Y_{12}		Cascode	-	0.0 - j0.008	-	-	0.0 - j0.008	-	mS
			Diff. Amp.	-	0.0 - j0.013	-	-	0.0 - j0.013	-	mS
Forward Transfer Admittance	Y_{21}		Cascode (Figures 26, 28, 30)	-	17.9 - j30.7	-	-	17.9 - j30.7	-	mS
			Diff. Amp. (Figures 27, 29, 31)	-	-10.5 + j13	-	-	-10.5 + j13	-	mS
Output Admittance	Y_{22}		Cascode (Figures 20, 22, 24)	-	-0.503 - j15	-	-	-0.503 - j15	-	mS
			Diff. Amp. (Figures 21, 23, 25)	-	0.071 + j0.62	-	-	0.071 + j0.62	-	mS

NOTES:

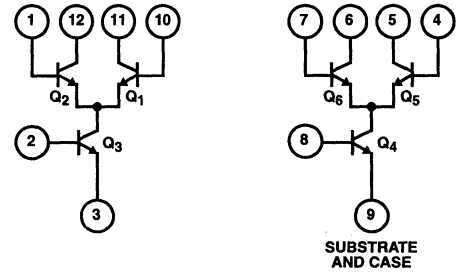
3. Terminals 1 and 14 or 7 and 8 (CA3102). Terminals 1 and 12 or 6 and 7 (CA3049T).
4. Terminals 13 and 4 or 6 and 11 (CA3102). Terminals 10 and 11 or 4 and 5 (CA3049T).

Schematic Diagrams

CA3102E, CA3102M



CA3049T



Test Circuits

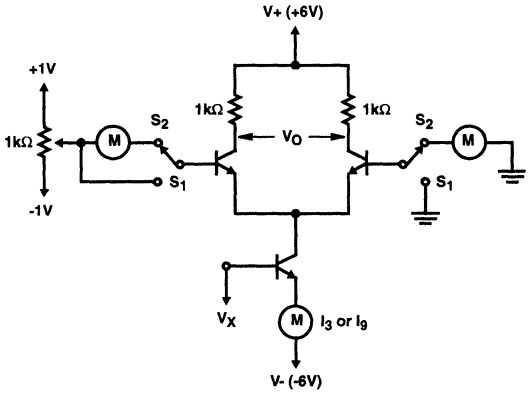


FIGURE 1. DC CHARACTERISTICS TEST CIRCUIT FOR CA3102

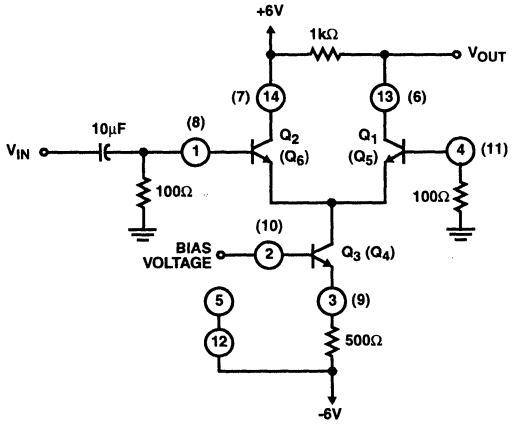
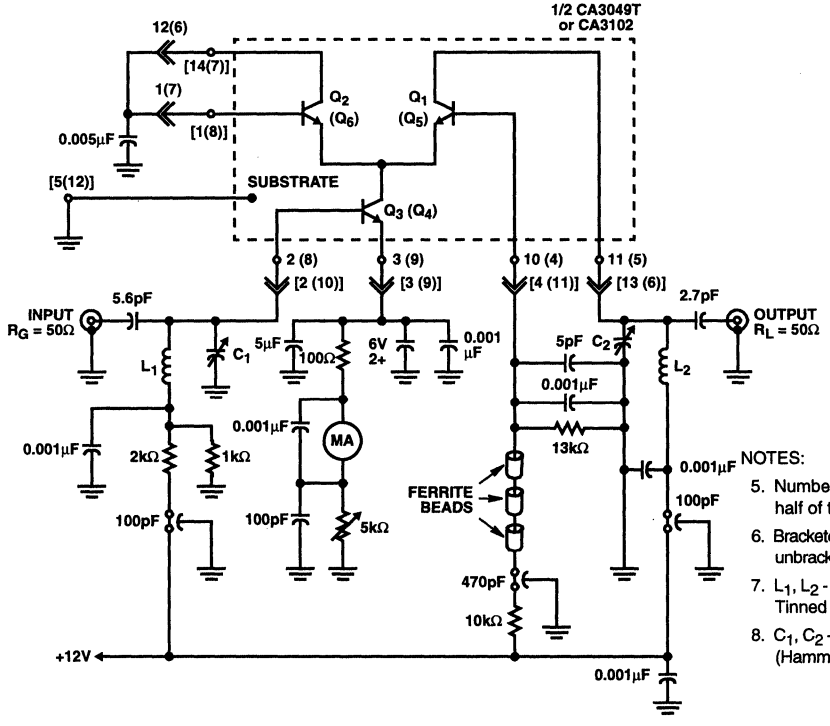


FIGURE 2. AGC RANGE AND VOLTAGE GAIN TEST CIRCUIT FOR CA3102



NOTES:

5. Numbers in parentheses refer to other half of the CA3049T or CA3102.
6. Bracketed numbers refer to CA3102, unbracketed numbers refer to CA3049T.
7. L_1, L_2 - Approximately $^1/_2$ Turn #18 Tinned Copper Wire, 5/8" Diameter.
8. C_1, C_2 - 15pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent).

FIGURE 3. 200MHz CASCODE POWER GAIN AND NOISE FIGURE TEST CIRCUIT

Typical Performance Curves

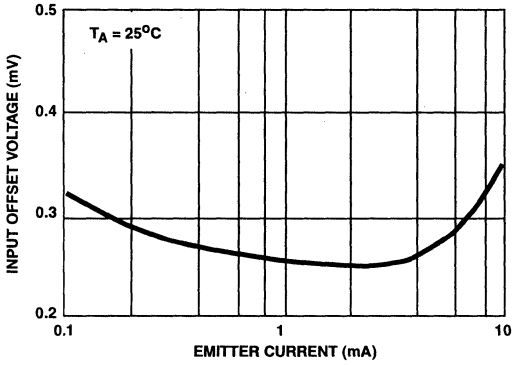


FIGURE 4. INPUT OFFSET VOLTAGE vs EMITTER CURRENT

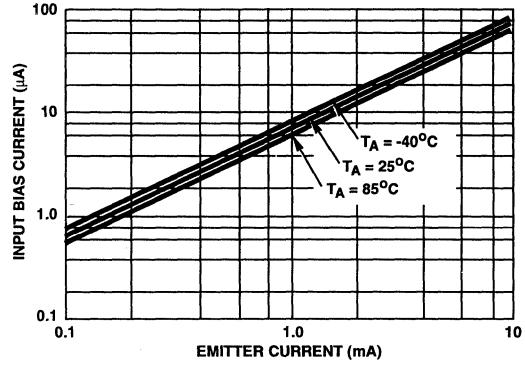


FIGURE 5. INPUT BIAS CURRENT vs EMITTER CURRENT

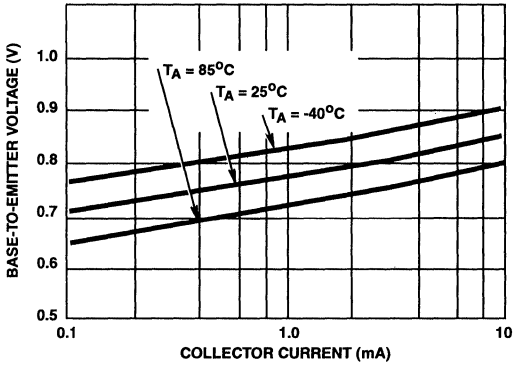


FIGURE 6. BASE-TO-EMITTER VOLTAGE vs COLLECTOR CURRENT

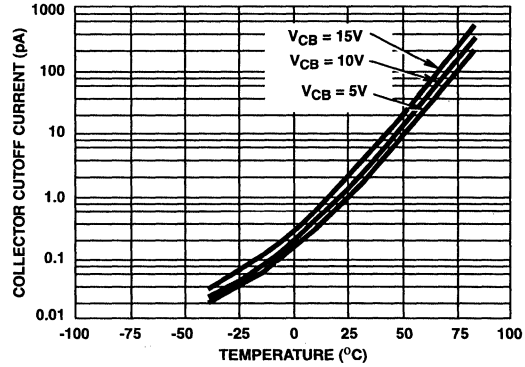


FIGURE 7. COLLECTOR CUTOFF CURRENT vs TEMPERATURE

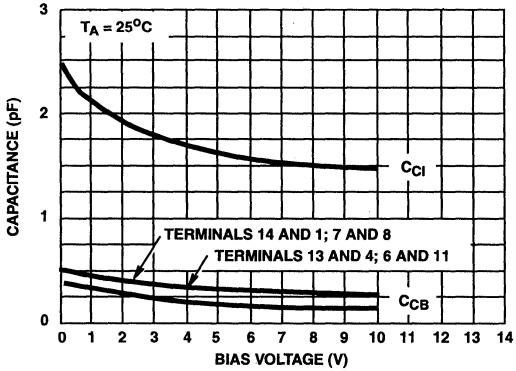


FIGURE 8. CAPACITANCE vs DC BIAS VOLTAGE

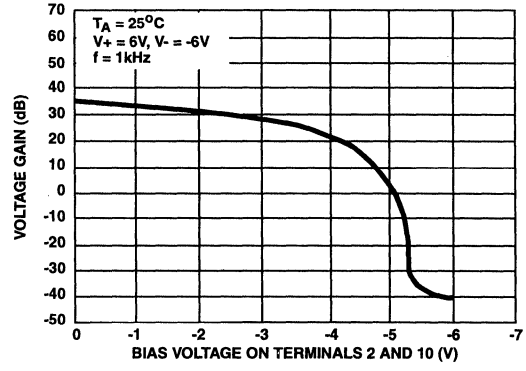


FIGURE 9. VOLTAGE GAIN vs DC BIAS VOLTAGE

Typical Performance Curves (Continued)

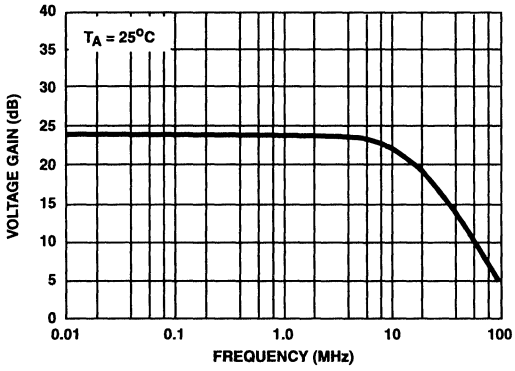


FIGURE 10. VOLTAGE GAIN vs FREQUENCY

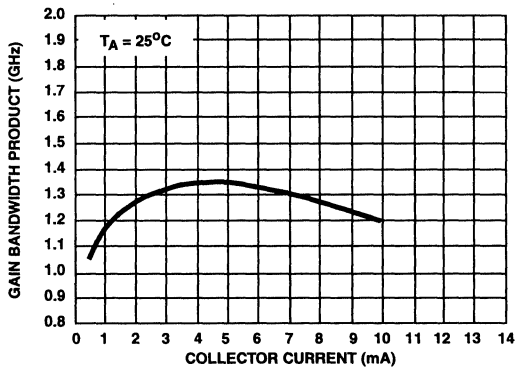


FIGURE 11. GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

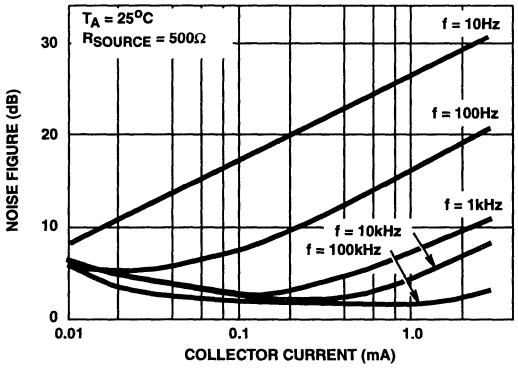


FIGURE 12. 1/f NOISE FIGURE vs COLLECTOR CURRENT

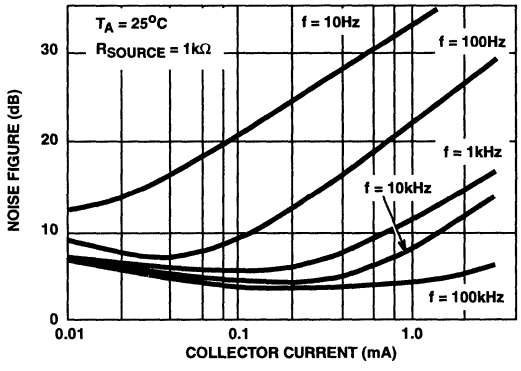


FIGURE 13. 1/f NOISE FIGURE vs COLLECTOR CURRENT

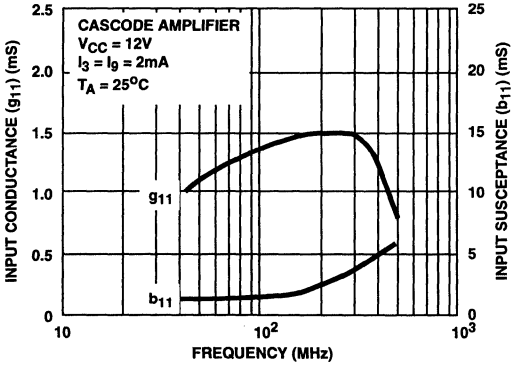


FIGURE 14. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

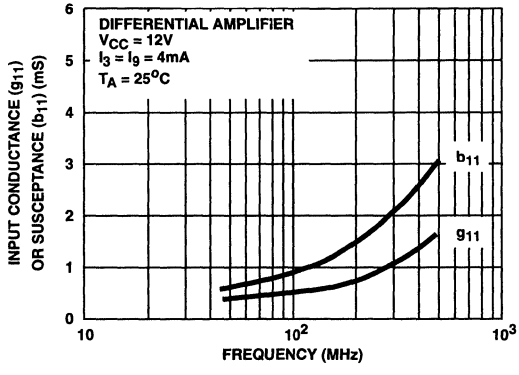


FIGURE 15. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

Typical Performance Curves (Continued)

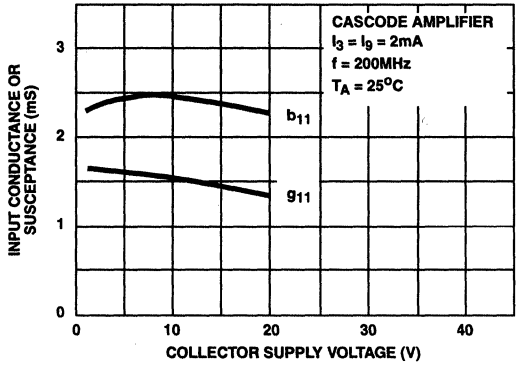


FIGURE 16. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR SUPPLY VOLTAGE

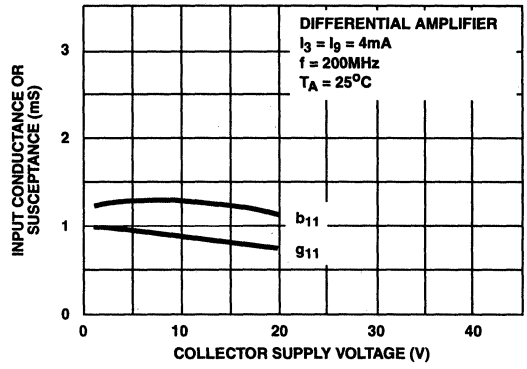


FIGURE 17. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR SUPPLY VOLTAGE

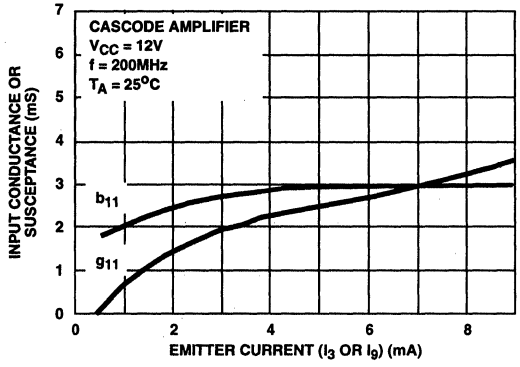


FIGURE 18. INPUT ADMITTANCE (Y_{11}) vs EMITTER CURRENT

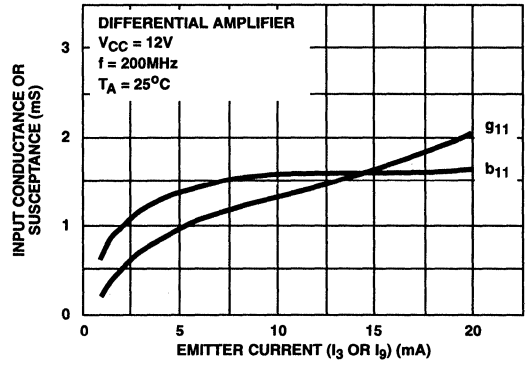


FIGURE 19. INPUT ADMITTANCE (Y_{11}) vs EMITTER CURRENT

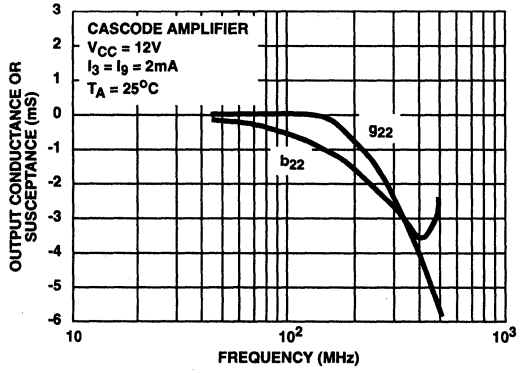


FIGURE 20. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

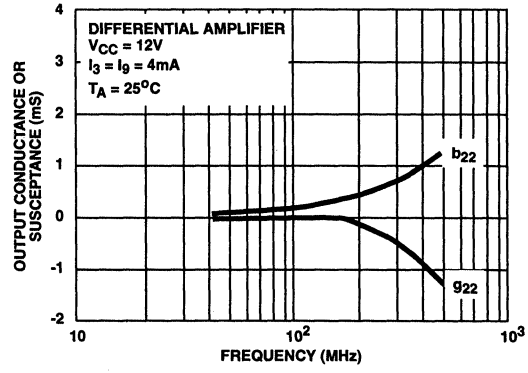


FIGURE 21. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

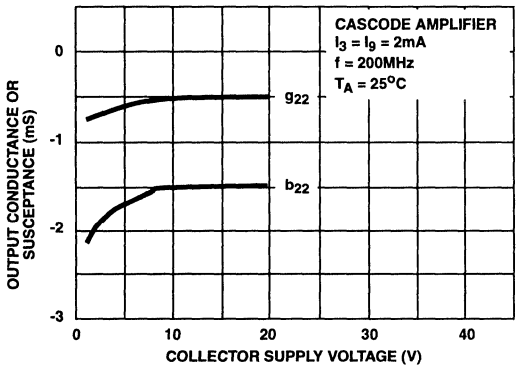


FIGURE 22. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR SUPPLY VOLTAGE

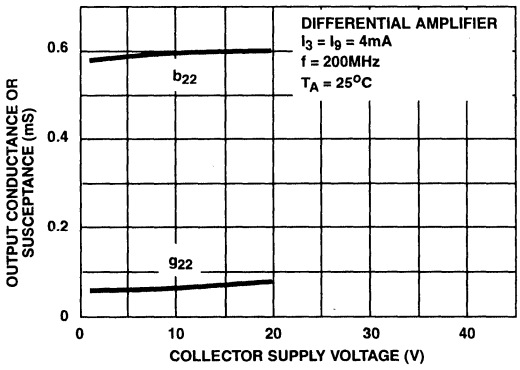


FIGURE 23. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR SUPPLY VOLTAGE

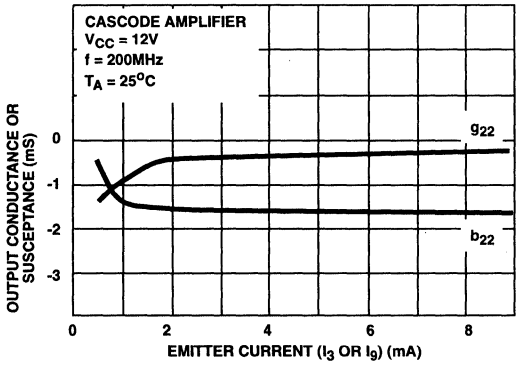


FIGURE 24. OUTPUT ADMITTANCE (Y_{22}) vs EMITTER CURRENT

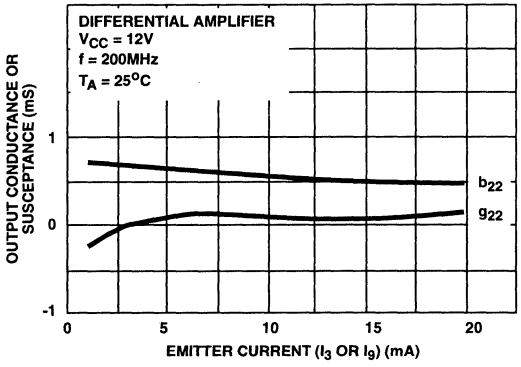


FIGURE 25. OUTPUT ADMITTANCE (Y_{22}) vs EMITTER CURRENT

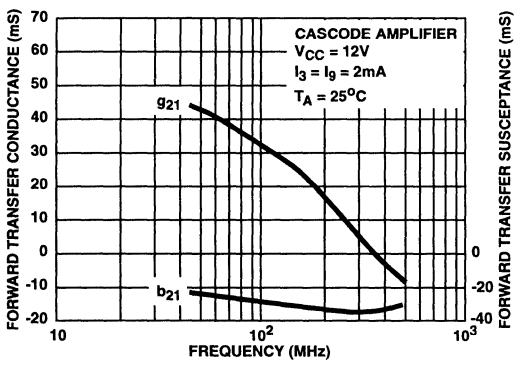


FIGURE 26. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

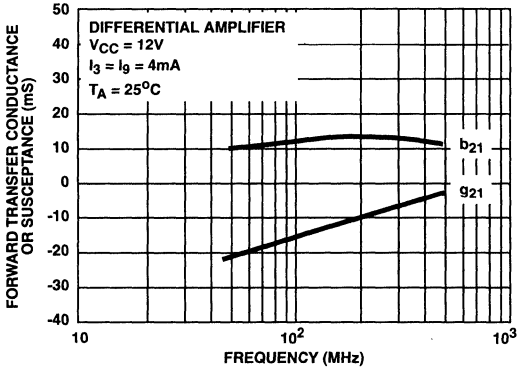


FIGURE 27. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

Typical Performance Curves (Continued)

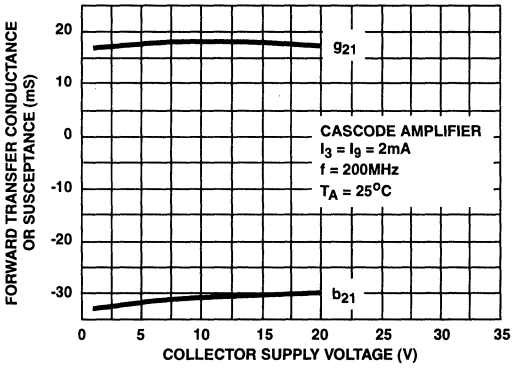


FIGURE 28. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs COLLECTOR SUPPLY VOLTAGE

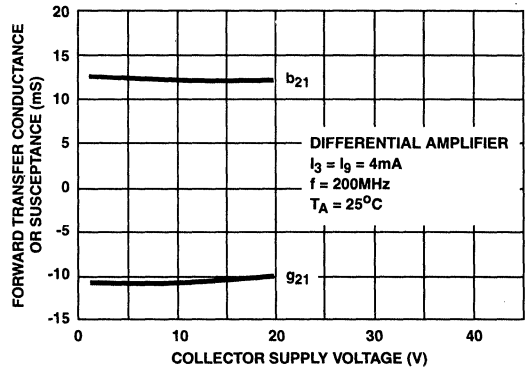


FIGURE 29. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs COLLECTOR SUPPLY VOLTAGE

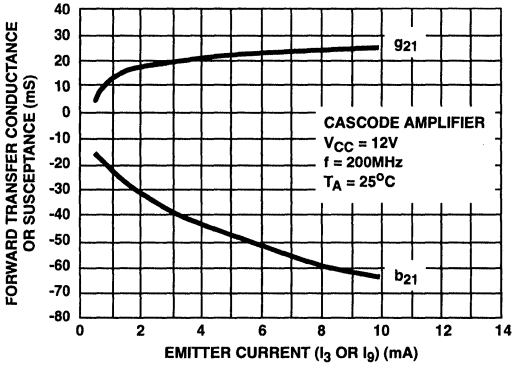


FIGURE 30. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs EMITTER CURRENT

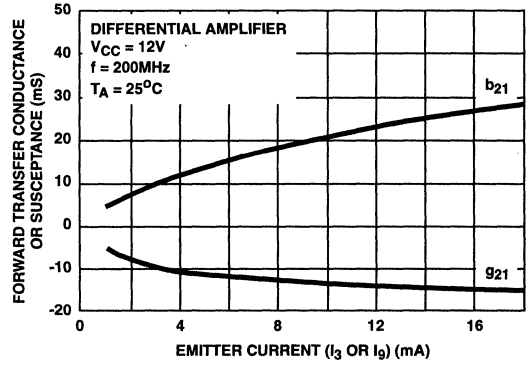


FIGURE 31. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs EMITTER CURRENT

HARRIS SEMICONDUCTOR

CA3054

Dual Independent Differential Amp for Low Power Applications from DC to 120MHz

November 1996

Features

- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Maximum Input Offset Voltage . . . . . ±5mV
- Temperature Range . . . . . 0°C to 85°C

Applications

- Dual Sense Amplifiers
- Dual Schmitt Triggers
- Multifunction Combinations
  - RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Pairs of Balanced Mixers
- Synthesizer Mixers
- Balanced (Push-Pull) Cascode Amplifiers

Description

The CA3054 consists of two independent differential amplifiers with associated constant current transistors on a common monolithic substrate. The six NPN transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300MHz. These feature make the CA3054 useful from DC to 120MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

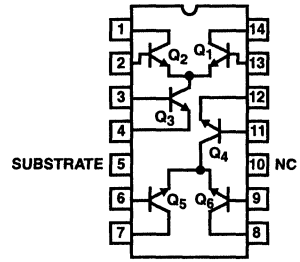
The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3054	0 to 85	14 Ld PDIP	E14.3
CA3054M (3054)	0 to 85	14 Ld SOIC	M14.15
CA3054M96 (3054)	0 to 85	14 Ld SOIC Tape and Reel	M14.15

Pinout

CA3054
(PDIP, SOIC)
TOP VIEW



7 ARRAYS AND DIFF. AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 388.3

Absolute Maximum Ratings $T_A = 25^oC$

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, I_C 50mA

Operating Conditions

Temperature Range ..... 0^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	130
SOIC Package	140

Maximum Junction Temperature (Die) ..... 175^oC
Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)
Maximum Power Dissipation (Any One Transistor) 300mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3054 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical Terminal 2 with respect to Terminal 4 is +15V to -5V.

(NOTE 4) TERM NO.	13	14	1	2	3	4	6	7	8	9	11	12	5
13		0, -20	Note 3	+5, -5	Note 3	+15, -5	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
14			Note 3	Note 3	Note 3	+20, 0	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	+20, 0
1				+20, 0	Note 3	+20, 0	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	+20, 0
2					Note 3	+15, -5	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
3						+1, -5	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
4							Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
6								0, -20	Note 3	+5, -5	Note 3	+15, -5	Note 3
7									Note 3	Note 3	Note 3	Note 3	+20, 0
8										+20, 0	Note 3	Note 3	+20, 0
9											Note 3	+15, -5	Note 3
11												-1, -5	Note 3
12													Note 3
5													Ref. Substrate

Maximum Current Ratings

(NOTE 4) TERM NO.	I_{IN} mA	I_{OUT} mA
13	5	0.1
14	50	0.1
1	50	0.1
2	5	0.1
3	5	0.1
4	0.1	50
6	5	0.1
7	50	0.1
8	50	0.1
9	5	0.1
11	5	0.1
12	0.1	50

NOTES:

3. Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.
4. Terminal No. 10 of CA3054 is not used.

Electrical Specifications $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS For Each Differential Amplifier						
Input Offset Voltage (Figure 8)	V_{IO}	$V_{CB}=3V, I_{E(Q3)}=I_{E(Q4)}=2mA$	-	0.45	5	mV
Input Offset Current (Figure 9)	I_{IO}	$V_{CB}=3V, I_{E(Q3)}=I_{E(Q4)}=2mA$	-	0.3	2	µA
Input Bias Current (Figure 5)	I_I	$V_{CB}=3V, I_{E(Q3)}=I_{E(Q4)}=2mA$	-	10	24	µA
Quiescent Operating Current Ratio (Figure 5)	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$	$V_{CB}=3V, I_{E(Q3)}=I_{E(Q4)}=2mA$	-	0.98 to 1.02	-	-
Temperature Coefficient Magnitude of Input Offset Voltage (Figure 7)	$\frlvert\frac{\Delta V_{IO}}{\Delta T}\frrvert$	$V_{CB}=3V, I_{E(Q3)}=I_{E(Q4)}=2mA$	-	1.1	-	µV/°C

Electrical Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
FOR EACH TRANSISTOR							
DC Forward Base-to-Emitter Voltage (Figure 8)	V_{BE}	V_{CB} = 3V	I_C = 50μA	-	0.630	0.700	V
			I_C = 1mA	-	0.715	0.800	V
			I_C = 3mA	-	0.750	0.850	V
			I_C = 10mA	-	0.800	0.900	V
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3V, I_C = 1mA		-	-1.9	-	μV/°C
Collector Cutoff Current (Figure 4)	I_{CBO}	V_{CB} = 10V, I_E = 0		-	0.002	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10μA, I_E = 0		20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μA, I_{CI} = 0		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0		5	7	-	V
DYNAMIC CHARACTERISTICS							
Common Mode Rejection Ratio for each Amplifier (Figures 1, 10)	CMRR	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	100	-	dB
AGC Range, One Stage (Figures 2, 11)	AGC	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	75	-	dB
Voltage Gain, Single Stage Double-Ended Output (Figures 2, 11)	A	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	32	-	dB
AGC Range, Two Stage (Figures 3, 12)	AGC	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	105	-	dB
Voltage Gain, Two Stage Double-Ended Output (Figures 3, 12)	A	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	60	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics (For Single Transistor)							
Forward Current Transfer Ratio (Figure 13)	h_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	110	-	-
Short Circuit Input Impedance (Figure 13)	h_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 13)	h_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	15.6	-	μS
Open Circuit Reverse Voltage Transfer Ratio (Figure 13)	h_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	1.8×10^{-4}	-	-
1/f Noise Figure for Single Transistor	NF	f = 1kHz, V_{CE} = 3V		-	3.25	-	dB
Gain Bandwidth Product for Single Transistor (Figure 14)	f_T	V_{CE} = 3V, I_C = 3mA		-	550	-	MHz
Admittance Characteristics; Differential Circuit Configuration (For Each Amplifier)							
Forward Transfer Admittance (Figure 15)	Y_{21}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	-20 + j0	-	mS
Input Admittance (Figure 16)	Y_{11}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	0.22 + j0.1	-	mS
Output Admittance (Figure 17)	Y_{22}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	0.01 + j0	-	mS
Reverse Transfer Admittance (Figure 18)	Y_{12}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	-0.003 + j0	-	mS

Electrical Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Admittance Characteristics; Cascode Circuit Configuration (For Each Amplifier)						
Forward Transfer Admittance (Figure 19)	Y_{21}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	68 - j0	-	mS
Input Admittance (Figure 20)	Y_{11}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	0.55 + j0	-	mS
Output Admittance (Figure 21)	Y_{22}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	0 + j0.02	-	mS
Reverse Transfer Admittance (Figure 22)	Y_{12}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	0.004 - j0.005	-	µS
Noise Figure	NF	f = 100MHz	-	8	-	dB

Test Circuits

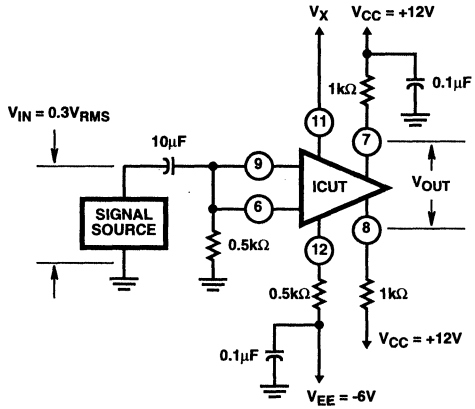


FIGURE 1. COMMON MODE REJECTION RATIO TEST SETUP

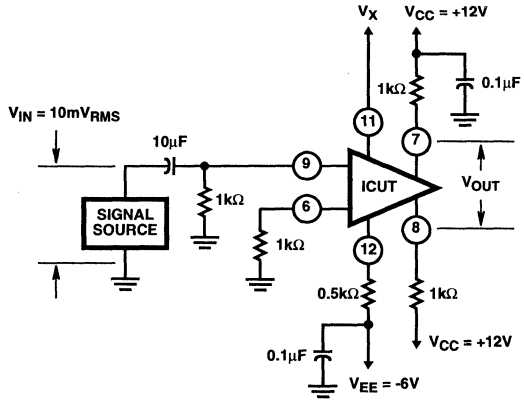


FIGURE 2. SINGLE STAGE VOLTAGE GAIN TEST SETUP

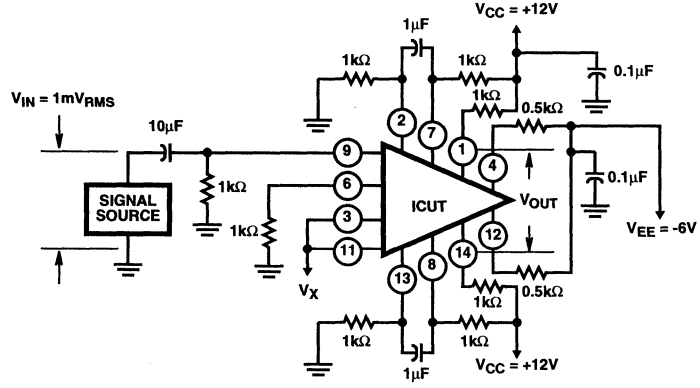
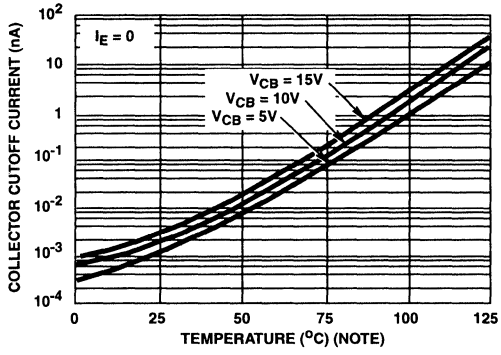


FIGURE 3. TWO STAGE VOLTAGE GAIN TEST SETUP

Typical Performance Curves



NOTE: For CA3054 use data from 0°C to 85°C only.

FIGURE 4. COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

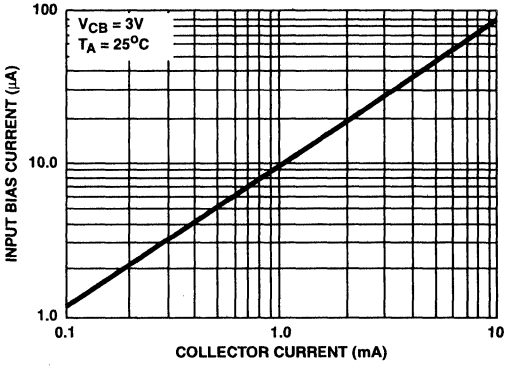
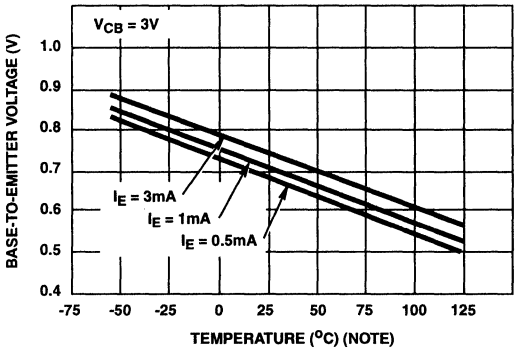
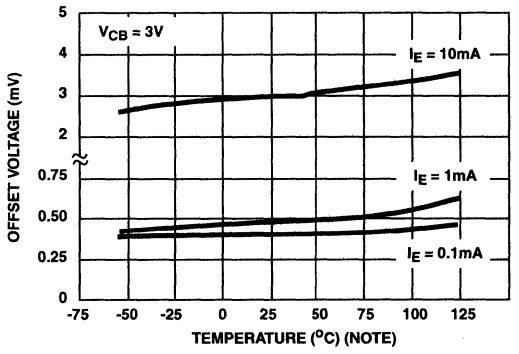


FIGURE 5. INPUT BIAS CURRENT vs COLLECTOR CURRENT FOR EACH TRANSISTOR



NOTE: For CA3054 use data from 0°C to 85°C only.

FIGURE 6. BASE-TO-EMITTER VOLTAGE FOR EACH TRANSISTOR vs TEMPERATURE



NOTE: For CA3054 use data from 0°C to 85°C only.

FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE FOR DIFFERENTIAL PAIRS

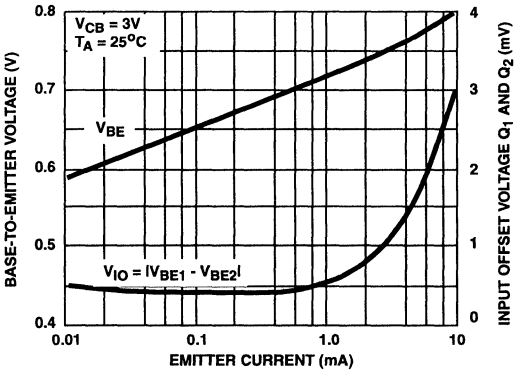


FIGURE 8. STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIRS vs EMITTER CURRENT

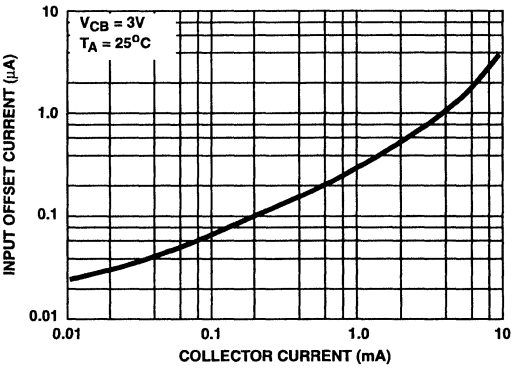


FIGURE 9. INPUT OFFSET CURRENT FOR MATCHED DIFFERENTIAL PAIRS vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

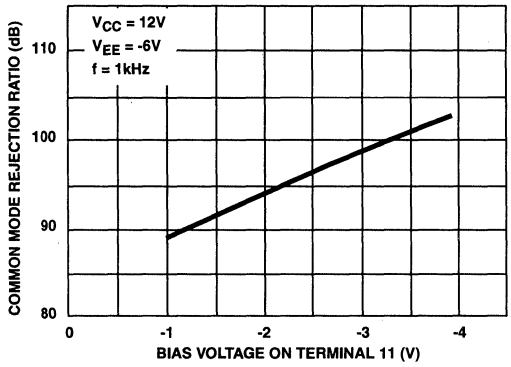


FIGURE 10. COMMON MODE REJECTION RATIO CHARACTERISTIC

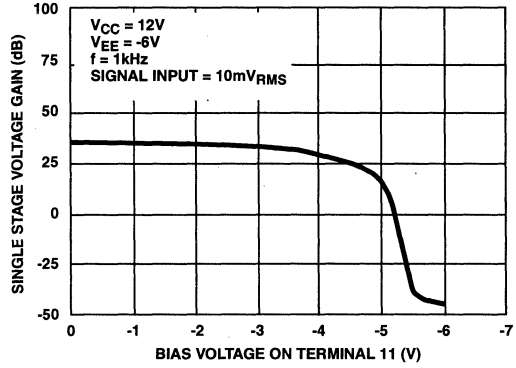


FIGURE 11. SINGLE STAGE VOLTAGE GAIN CHARACTERISTIC

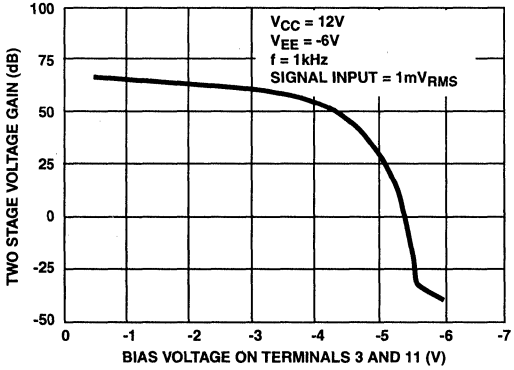


FIGURE 12. TWO STAGE VOLTAGE GAIN CHARACTERISTIC

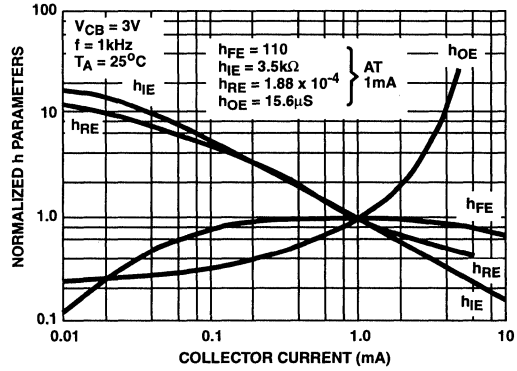


FIGURE 13. FORWARD CURRENT TRANSFER RATIO (h_{FE}), SHORT CIRCUIT INPUT IMPEDANCE (h_{IE}), OPEN CIRCUIT OUTPUT IMPEDANCE (h_{OE}), AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER RATIO (h_{RE}) vs COLLECTOR CURRENT FOR EACH TRANSISTOR

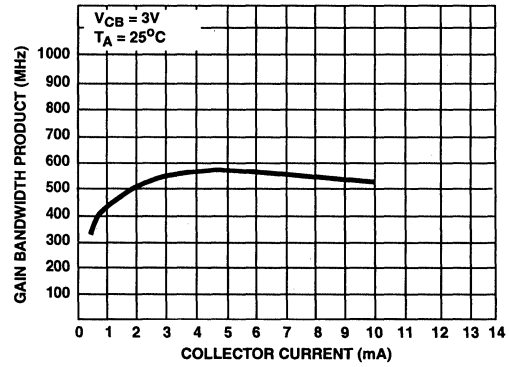


FIGURE 14. GAIN BANDWIDTH PRODUCT (f_T) vs COLLECTOR CURRENT

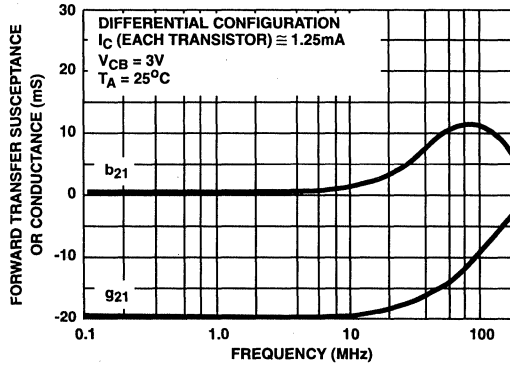


FIGURE 15. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

Typical Performance Curves (Continued)

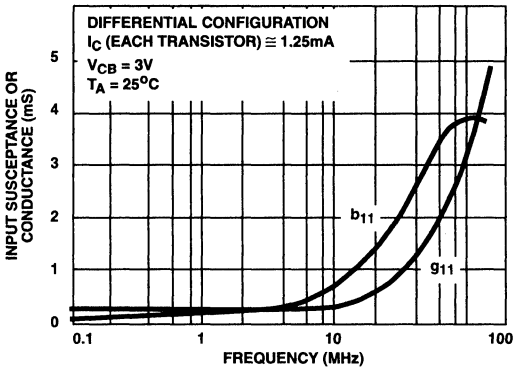


FIGURE 16. INPUT ADMITTANCE (Y_{11})

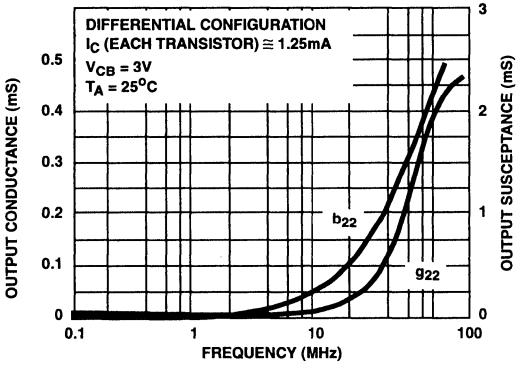


FIGURE 17. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

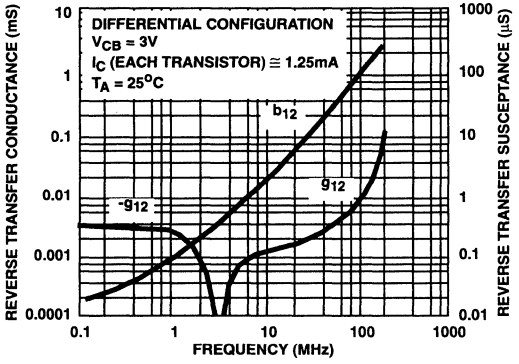


FIGURE 18. REVERSE TRANSFER ADMITTANCE (Y_{12}) vs FREQUENCY

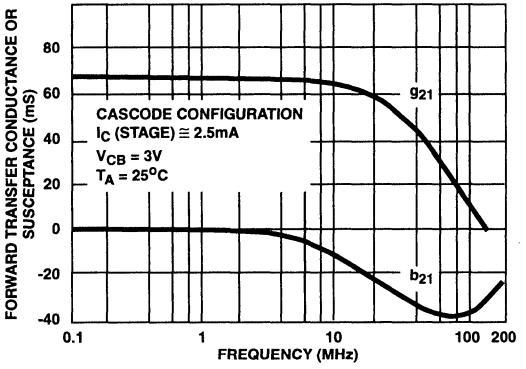


FIGURE 19. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

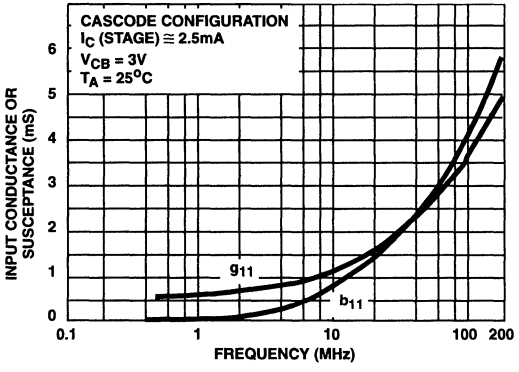


FIGURE 20. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

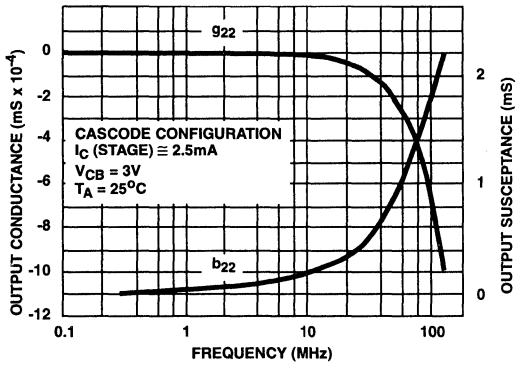


FIGURE 21. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

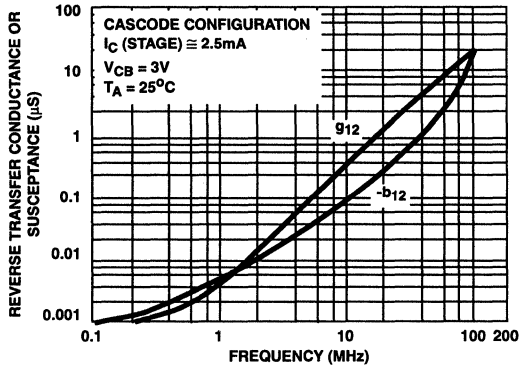


FIGURE 22. REVERSE TRANSFER ADMITTANCE (Y_{12}) vs FREQUENCY

HARRIS SEMICONDUCTOR

CA3081, CA3082

General Purpose High Current NPN Transistor Arrays

November 1996

Features

- CA3081 - Common Emitter Array
- CA3082 - Common Collector Array
- Directly Drive Seven Segment Incandescent Displays and Light Emitting Diode (LED) Display
- 7 Transistors Permit a Wide Range of Applications in Either a Common Emitter (CA3081) or Common Collector (CA3082) Configuration
- High I_C ..... 100mA (Max)
- Low V_{CESAT} (at 50mA) ..... 0.4V (Typ)

Applications

- Drivers for
  - Incandescent Display Devices
  - LED Displays
  - Relay Control
- Thyristor Firing

Description

CA3081 and CA3082 consist of seven high current (to 100mA) silicon NPN transistors on a common monolithic substrate. The CA3081 is connected in a common emitter configuration and the CA3082 is connected in a common collector configuration.

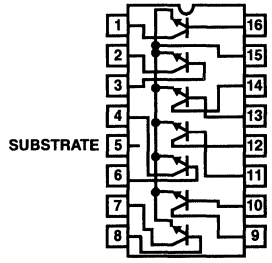
The CA3081 and CA3082 are capable of directly driving seven segment displays, and light emitting diode (LED) displays. These types are also well suited for a variety of other drive applications, including relay control and thyristor firing.

Ordering Information

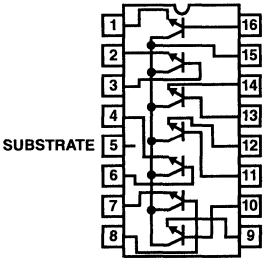
PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3081	-55 to 125	16 Ld PDIP	E16.3
CA3081F	-55 to 125	16 Ld CERDIP	F16.3
CA3081M (3081)	-55 to 125	16 Ld SOIC	M16.15
CA3081M96 (3081)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3082	-55 to 125	16 Ld PDIP	E16.3
CA3082F	-55 to 125	16 Ld CERDIP	F16.3
CA3082M (3082)	-55 to 125	16 Ld SOIC	M16.15
CA3082M96 (3082)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Pinouts

CA3081
COMMON EMITTER CONFIGURATION
(PDIP, CERDIP, SOIC)
TOP VIEW



CA3082
COMMON COLLECTOR CONFIGURATION
(PDIP, CERDIP, SOIC)
TOP VIEW



7 ARRAYS AND DIFF. AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **480.3**

Absolute Maximum Ratings $T_A = 25^oC$

Collector-to-Emitter Voltage (V_{CEO}) 16V
Collector-to-Base Voltage (V_{CBO}) 20V
Collector-to-Substrate Voltage (V_{CIO}, Note 1) 20V
Emitter-to-Base Voltage (V_{EBO}) 5V
Collector Current (I_C) 100mA
Base Current (I_B) 20mA

Operating Conditions

Temperature Range ..... -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	135	65
PDIP Package	135	N/A
SOIC Package	200	N/A

Maximum Power Dissipation (Any One Transistor) 500mW
Maximum Junction Temperature (Ceramic Package) ..... 175^oC
Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications For Equipment Design at $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 500\mu A$, $I_E = 0$	20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 500\mu A$, $I_B = 0$	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	16	24	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_C = 500\mu A$	5.0	6.9	-	V
DC Forward Current Transfer Ratio	h_{FE}	$V_{CE} = 0.5V$, $I_C = 30mA$	30	68	-	-
		$V_{CE} = 0.8V$, $I_C = 50mA$	40	70	-	-
Base-to-Emitter Saturation Voltage (Figure 4)	V_{BESAT}	$I_C = 30mA$, $I_B = 1mA$	-	0.87	1.2	V
Collector-to-Emitter Saturation Voltage	V_{CESAT}					
CA3081, CA3082		$I_C = 30mA$, $I_B = 1mA$	-	0.27	0.5	V
CA3081 (Figure 5)		$I_C = 50mA$, $I_B = 5mA$	-	0.4	0.7	V
CA3082 (Figure 5)		$I_C = 50mA$, $I_B = 5mA$	-	0.4	0.8	V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	-	10	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	-	1.0	μA

Typical Read - Out Driver Applications

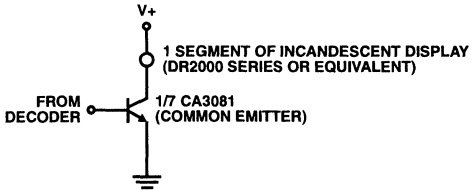
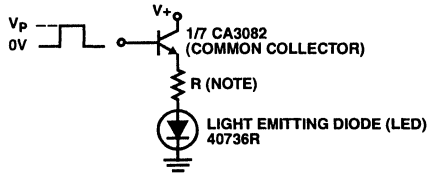


FIGURE 1. SCHEMATIC DIAGRAM SHOWING ONE TRANSISTOR OF THE CA3081 DRIVING ONE SEGMENT OF AN INCANDESCENT DISPLAY



NOTE: The Resistance for R is determined by the relationship:

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I(LED)}$$

$R = 0$ for $V_P = V_{BE} + V_F(LED)$

Where: V_P = Input Pulse Voltage
V_F = Forward Voltage Drop Across the Diode

FIGURE 2. SCHEMATIC DIAGRAM SHOWING ONE TRANSISTOR OF THE CA3082 DRIVING A LIGHT EMITTING DIODE (LED)

Typical Performance Curves

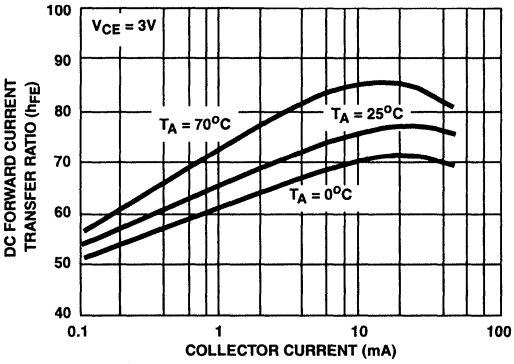


FIGURE 3. DC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

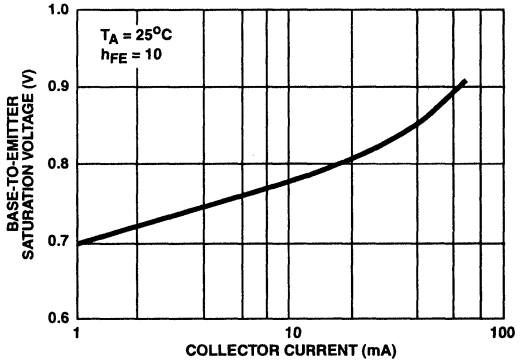


FIGURE 4. BASE-TO-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

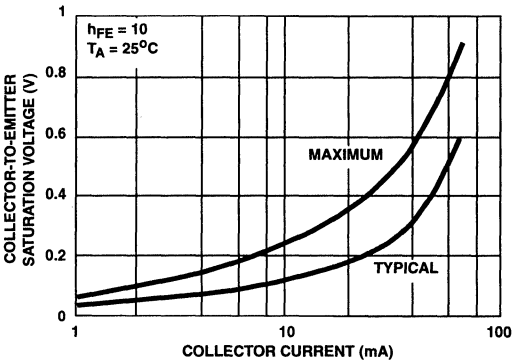


FIGURE 5. COLLECTOR-TO-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

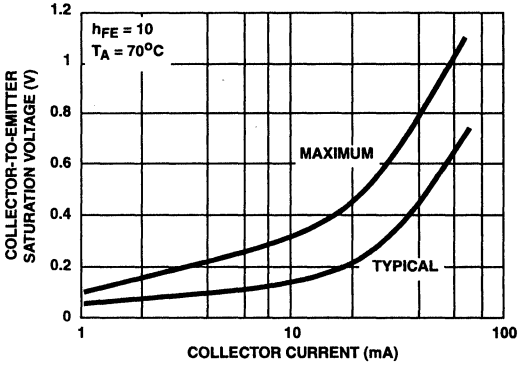


FIGURE 6. COLLECTOR-TO-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

HARRIS SEMICONDUCTOR

CA3083

General Purpose High Current NPN Transistor Array

September 1996

Features

- High I_C ..... 100mA (Max)
- Low $V_{CE\ sat}$ (at 50mA) ..... 0.7V (Max)
- Matched Pair (Q_1 and Q_2)
  - V_{IO} (V_{BE} Match) ..... ±5mV (Max)
  - I_{IO} (at 1mA) ..... 2.5μA (Max)
- 5 Independent Transistors Plus Separate Substrate Connection

Applications

- Signal Processing and Switching Systems Operating from DC to VHF
- Lamp and Relay Driver
- Differential Amplifier
- Temperature Compensated Amplifier
- Thyristor Firing
- See Application Note AN5296 "Applications of the CA3018 Circuit Transistor Array" for Suggested Applications

Description

The CA3083 is a versatile array of five high current (to 100mA) NPN transistors on a common monolithic substrate. In addition, two of these transistors (Q_1 and Q_2) are matched at low current (i.e., 1mA) for applications in which offset parameters are of special importance.

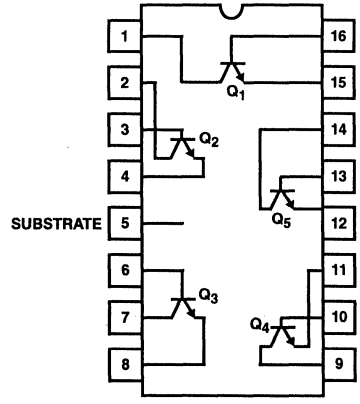
Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3083	-55 to 125	16 Ld PDIP	E16.3
CA3083F	-55 to 125	16 Ld CERDIP	F16.3
CA3083M (3083)	-55 to 125	16 Ld SOIC	M16.15
CA3083M96 (3083)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Pinout

CA3083
(PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 481.3

Absolute Maximum Ratings

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current (I_C) 100mA
Base Current (I_B) 20mA

Operating Conditions

Temperature Range ..... -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	135	65
PDIP Package	135	N/A
SOIC Package	200	N/A

Maximum Power Dissipation (Any One Transistor) 500mW
Maximum Junction Temperature (Hermetic Package) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate Terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications For Equipment Design, $T_A = 25°C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FOR EACH TRANSISTOR						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\mu A$, $I_E = 0$	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100\mu A$, $I_B = 0$, $I_E = 0$	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 500\mu A$, $I_C = 0$	5	6.9	-	V
Collector-Cutoff-Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	-	10	µA
Collector-Cutoff-Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	-	1	µA
DC Forward-Current Transfer Ratio (Note 3) (Figure 1)	h_{FE}	$V_{CE} = 3V$, $I_C = 10mA$	40	76	-	
		$I_C = 50mA$	40	75	-	
Base-to-Emitter Voltage (Figure 2)	V_{BE}	$V_{CE} = 3V$, $I_C = 10mA$	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage (Figures 3, 4)	$V_{CE\ SAT}$	$I_C = 50mA$, $I_B = 5mA$	-	0.40	0.70	V
Gain Bandwidth Product	f_T	$V_{CE} = 3V$, $I_C = 10mA$	-	450	-	MHz
FOR TRANSISTORS Q_1 AND Q_2 (As a Differential Amplifier)						
Absolute Input Offset Voltage (Figure 6)	$\lvert V_{IO}\rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	1.2	5	mV
Absolute Input Offset Current (Figure 7)	$\lvert I_{IO}\rvert$	$V_{CE} = 3V$, $I_C = 1mA$	-	0.7	2.5	µA

NOTE:

3. Actual forcing current is via the emitter for this test.

Typical Performance Curves

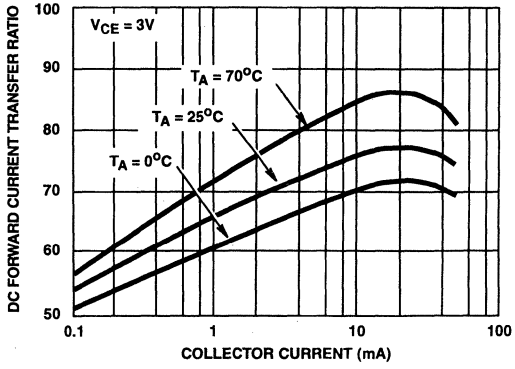


FIGURE 1. h_{FE} vs I_C

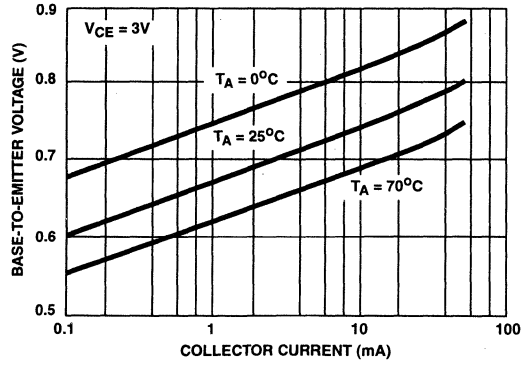


FIGURE 2. V_{BE} vs I_C

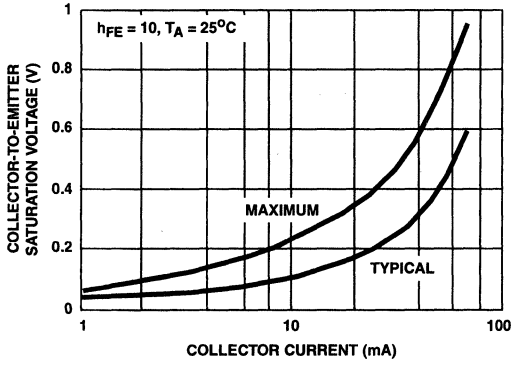


FIGURE 3. $V_{CE\ SAT}$ vs I_C

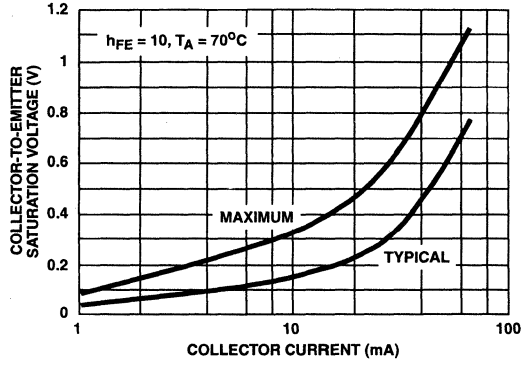


FIGURE 4. $V_{CE\ SAT}$ vs I_C

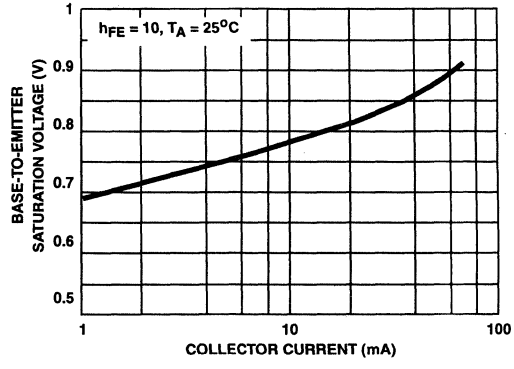


FIGURE 5. $V_{BE\ SAT}$ vs I_C

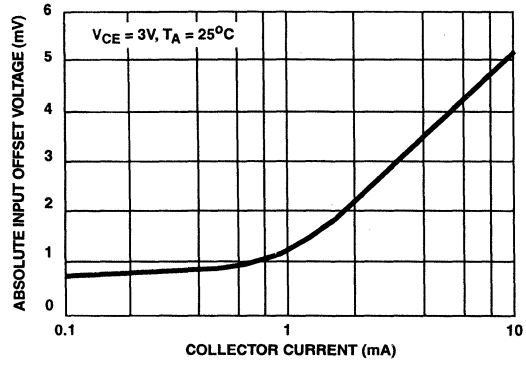


FIGURE 6. V_{IO} vs I_C (TRANSISTORS Q_1 AND Q_2 AS A DIFFERENTIAL AMPLIFIER)

Typical Performance Curves (Continued)

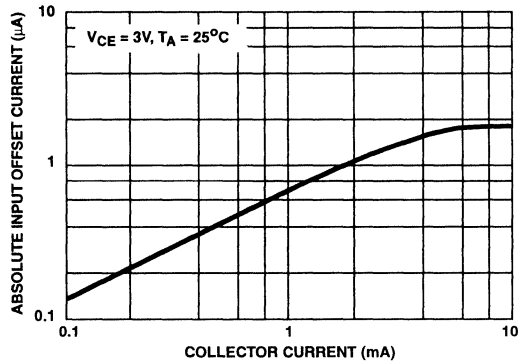


FIGURE 7. I_{IO} vs I_C (TRANSISTORS Q_1 AND Q_2 AS A DIFFERENTIAL AMPLIFIER)

HARRIS SEMICONDUCTOR

CA3086

General Purpose NPN Transistor Array

November 1996

Applications

- **Three Isolated Transistors and One Differentially Connected Transistor Pair For Low-Power Applications from DC to 120MHz**
- **General-Purpose Use in Signal Processing Systems Operating in the DC to 190MHz Range**
- **Temperature Compensated Amplifiers**
- **See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications**

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3086	-55 to 125	14 Ld PDIP	E14.3
CA3086M (3086)	-55 to 125	14 Ld SOIC	M14.15
CA3086M96 (3086)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15
CA3086F	-55 to 125	14 Ld CERDIP	F14.3

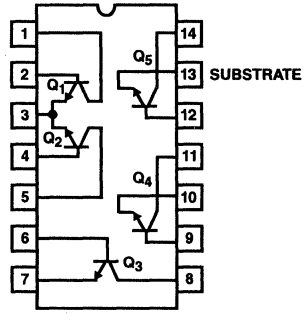
Description

The CA3086 consists of five general-purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching

Pinout

CA3086
(PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

The following ratings apply for each transistor in the device:

- Collector-to-Emitter Voltage, V_{CEO} 15V
- Collector-to-Base Voltage, V_{CBO} 20V
- Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
- Emitter-to-Base Voltage, V_{EBO} 5V
- Collector Current, I_C 50mA

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	150	75
PDIP Package	180	N/A
SOIC Package	220	N/A

Maximum Power Dissipation (Any one transistor) 300mW
Maximum Junction Temperature (Hermetic Packages) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (Terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, For Equipment Design

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	5	7	-	V
Collector-Cutoff Current (Figure 1)	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$,	-	0.002	100	nA
Collector-Cutoff Current (Figure 2)	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$,	-	(Figure 2)	5	μA
DC Forward-Current Transfer Ratio (Figure 3)	h_{FE}	$V_{CE} = 3V$, $I_C = 1mA$	40	100	-	

Electrical Specifications $T_A = 25^oC$, Typical Values Intended Only for Design Guidance

PARAMETER	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio (Figure 3)	h_{FE}	$V_{CE} = 3V$	$I_C = 10mA$	100	
			$I_C = 10\mu A$	54	
Base-to-Emitter Voltage (Figure 4)	V_{BE}	$V_{CE} = 3V$	$I_E = 1$ mA	0.715	V
			$I_E = 10mA$	0.800	V
V_{BE} Temperature Coefficient (Figure 5)	$\Delta V_{BE}/\Delta T$	$V_{CE} = 3V$, $I_C = 1$ mA		-1.9	$mV/^oC$
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	$I_B = 1mA$, $I_C = 10mA$		0.23	V
Noise Figure (Low Frequency)	NF	$f = 1kHz$, $V_{CE} = 3V$, $I_C = 100\mu A$, $R_S = 1k\Omega$		3.25	dB

Electrical Specifications $T_A = 25^oC$, Typical Values Intended Only for Design Guidance **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:		f = 1kHz, V_{CE} = 3V, I_C = 1mA		
Forward Current-Transfer Ratio (Figure 6)	h_{FE}		100	-
Short-Circuit Input Impedance (Figure 6)	h_{IE}		3.5	kΩ
Open-Circuit Output Impedance (Figure 6)	h_{OE}		15.6	µS
Open-Circuit Reverse-Voltage Transfer Ratio (Figure 6)	h_{RE}		1.8×10^{-4}	-
Admittance Characteristics:		f = 1MHz, V_{CE} = 3V, I_C = 1mA		
Forward Transfer Admittance (Figure 7)	y_{FE}		31 - j1.5	mS
Input Admittance (Figure 8)	y_{IE}		0.3 + j0.04	mS
Output Admittance (Figure 9)	y_{OE}		0.001 + j0.03	mS
Reverse Transfer Admittance (Figure 10)	y_{RE}		See Figure 10	-
Gain-Bandwidth Product (Figure 11)	f_T	V_{CE} = 3V, I_C = 3mA	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0	2.8	pF

Typical Performance Curves

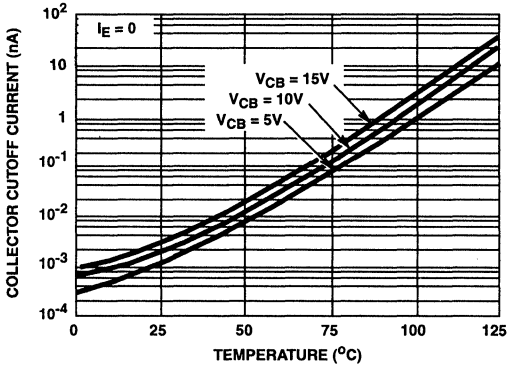


FIGURE 1. I_{CBO} vs TEMPERATURE

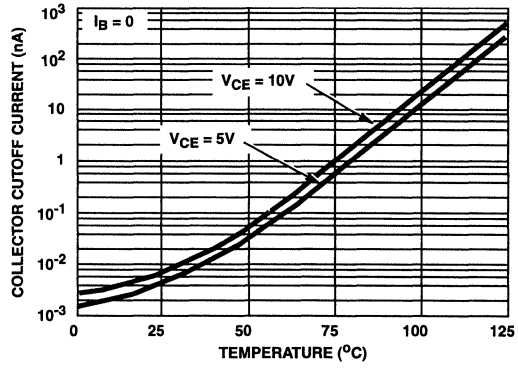


FIGURE 2. I_{CEO} vs TEMPERATURE

Typical Performance Curves (Continued)

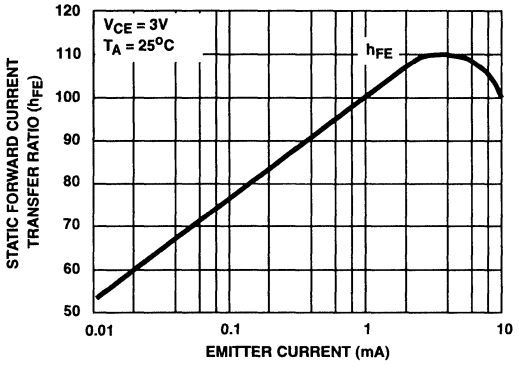


FIGURE 3. h_{FE} vs I_E

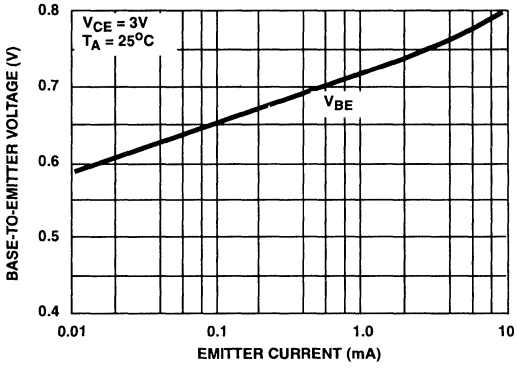


FIGURE 4. V_{BE} vs I_E

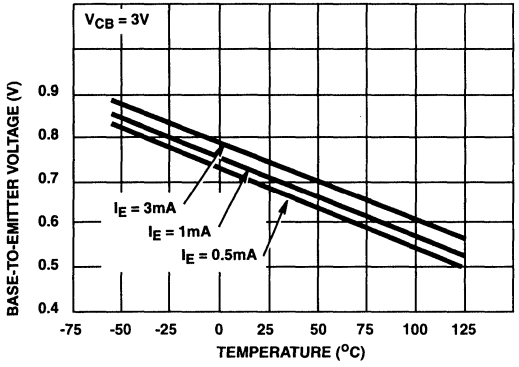


FIGURE 5. V_{BE} vs TEMPERATURE

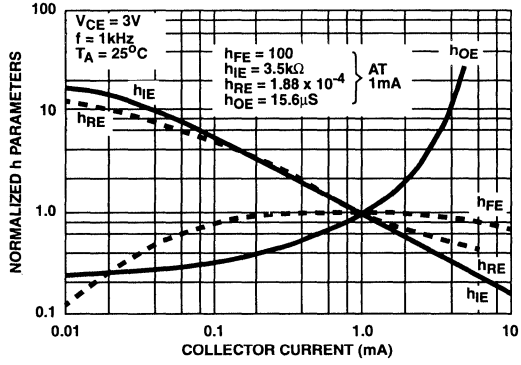


FIGURE 6. NORMALIZED h_{FE}, h_{IE}, h_{RE}, h_{OE} vs I_C

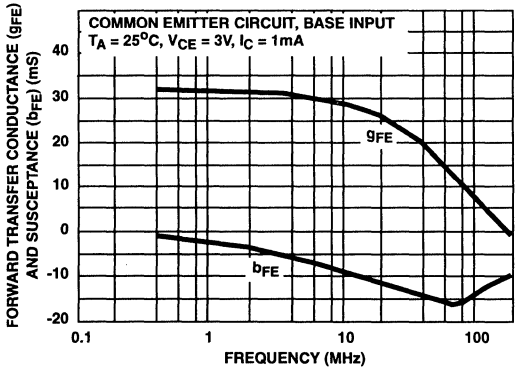


FIGURE 7. y_{FE} vs FREQUENCY

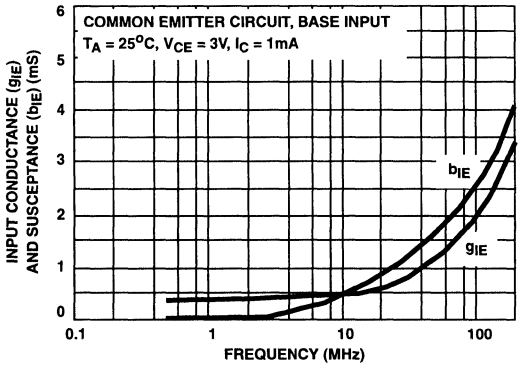


FIGURE 8. y_{IE} vs FREQUENCY

Typical Performance Curves (Continued)

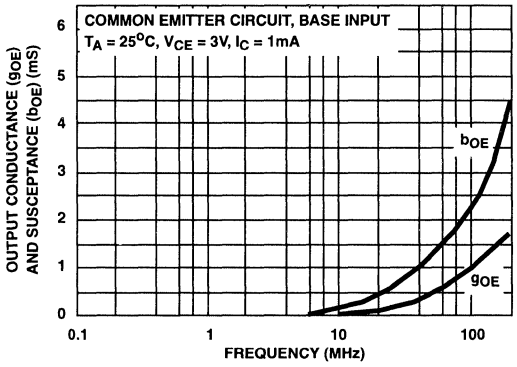


FIGURE 9. y_{OE} vs FREQUENCY

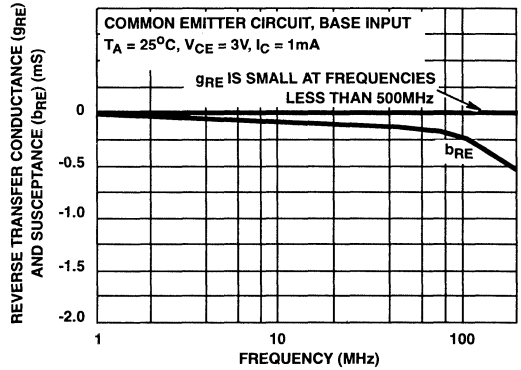


FIGURE 10. y_{RE} vs FREQUENCY

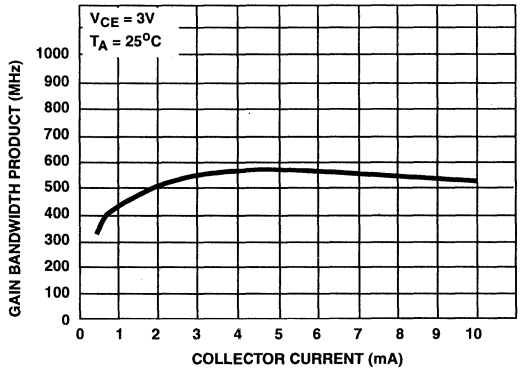


FIGURE 11. f_T vs I_C

HARRIS SEMICONDUCTOR

CA3096, CA3096A, CA3096C

August 1996

NPN/PNP Transistor Arrays

Applications

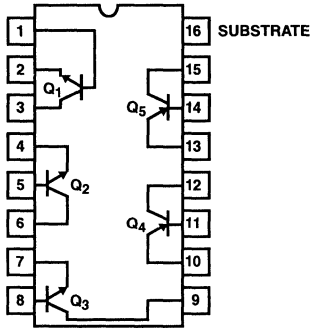
- **Five-Independent Transistors**
  - **Three NPN and**
  - **Two PNP**
- **Differential Amplifiers**
- **DC Amplifiers**
- **Sense Amplifiers**
- **Level Shifters**
- **Timers**
- **Lamp and Relay Drivers**
- **Thyristor Firing Circuits**
- **Temperature Compensated Amplifiers**
- **Operational Amplifiers**

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3096AE	-55 to 125	16 Ld PDIP	E16.3
CA3096AM (3096A)	-55 to 125	16 Ld SOIC	M16.15
CA3096AM96 (3096A)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3096CE	-55 to 125	16 Ld PDIP	E16.3
CA3096E	-55 to 125	16 Ld PDIP	E16.3
CA3096M (3096)	-55 to 125	16 Ld SOIC	M16.15
CA3096M96 (3096)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Pinout

CA3096, CA3096A, CA3096C
(PDIP, SOIC)
TOP VIEW



Description

The CA3096C, CA3096, and CA3096A are general purpose high voltage silicon transistor arrays. Each array consists of five independent transistors (two PNP and three NPN types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096A, CA3096, and CA3096C are identical, except that the CA3096A specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and V_{CE}(SAT). The CA3096C is a relaxed version of the CA3096.To type this body text, simply triple click this paragraph and begin typing. The paragraph tag for this area is called body.

CA3096, CA3096A, CA3096C Essential Differences

CHARACTERISTIC		CA3096A	CA3096	CA3096C
$V_{(BR)CEO}$ (V) (Min)				
	NPN	35	35	24
	PNP	-40	-40	-24
$V_{(BR)CBO}$ (V) (Min)				
	NPN	45	45	30
	PNP	-40	-40	-24
h_{FE} at 1mA				
	NPN	150-500	150-500	100-670
	PNP	20-200	20-200	15-200
h_{FE} at 100µA				
	PNP	40-250	40-250	30-300
I_{CBO} (nA) (Max)				
	NPN	40	100	100
	PNP	-40	-100	-100
I_{CEO} (nA) (Max)				
	NPN	100	1000	1000
	PNP	-100	-1000	-1000
$V_{CE\ SAT}$ (V) (Max)				
	NPN	0.5	0.7	0.7
$\|V_{IO}\|$ (mV) (Max)				
	NPN	5	-	-
	PNP	5	-	-
$\|I_{IO}\|$ (µA) (Max)				
	NPN	0.6	-	-
	PNP	0.25	-	-

7 ARRAYS AND DIFF. AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **595.3**

Absolute Maximum Ratings

	NPN	PNP
Collector-to-Emitter Voltage, V_{CEO}		
CA3096, CA3096A	35V	-40V
CA3096C	24V	-24V
Collector-to-Base Voltage, V_{CBO}		
CA3096, CA3096A	45V	-40V
CA3096C	30V	-24V
Collector-to-Substrate Voltage, V_{CIO} (Note 1)		
CA3096, CA3096A	45V	-
CA3096C	30V	-
Emitter-to-Substrate Voltage, V_{EIO}		
CA3096, CA3096A	-	-40V
CA3096C	-	-24V
Emitter-to-Base Voltage, V_{EBO}		
CA3096, CA3096A	6V	-40V
CA3096C	6V	-24V
Collector Current, I_C (All Types)	50mA	-10mA

Operating Conditions

Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	170

Maximum Power Dissipation (Each Transistor, Note 3) 200mW
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3096 is isolated from the substrate by an integral diode. The substrate (Terminal 16) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. Care must be taken to avoid exceeding the maximum junction temperature. Use the total power dissipation (all transistors) and thermal resistances to calculate the junction temperature.

Electrical Specifications For Equipment Design, At $T_A = 25°C$

PARAMETER	TEST CONDITIONS	CA3096			CA3096A			CA3096C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS FOR EACH NPN TRANSISTOR											
I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	0.001	100	-	0.001	40	-	0.001	100	nA
I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	0.006	1000	-	0.006	100	-	0.006	1000	nA
$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	35	50	-	35	50	-	24	35	-	V
$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	45	100	-	45	100	-	30	80	-	V
$V_{(BR)CIO}$	$I_{CI} = 10\mu A$, $I_B = I_E = 0$	45	100	-	45	100	-	30	80	-	V
$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	6	8	-	6	8	-	6	8	-	V
V_Z	$I_Z = 10\mu A$	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE\ SAT}$	$I_C = 10mA$, $I_B = 1mA$	-	0.24	0.7	-	0.24	0.5	-	0.24	0.7	V
V_{BE} (Note 4)	$I_C = 1mA$, $V_{CE} = 5V$	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE} (Note 4)		150	390	500	150	390	500	100	390	670	
$\lvert\Delta V_{BE}/\Delta T\rvert$ (Note 4)	$I_C = 1mA$, $V_{CE} = 5V$	-	1.9	-	-	1.9	-	-	1.9	-	mV/°C
DC CHARACTERISTICS FOR EACH PNP TRANSISTOR											
I_{CBO}	$V_{CB} = -10V$, $I_E = 0$	-	-0.06	-100	-	-0.006	-40	-	-0.06	-100	nA

Electrical Specifications For Equipment Design, At $T_A = 25^oC$ (Continued)

PARAMETER	TEST CONDITIONS	CA3096			CA3096A			CA3096C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEO}	V_{CE} = -10V, I_B = 0	-	-0.12	-1000	-	-0.12	-100	-	-0.12	-1000	nA
$V_{(BR)CEO}$	I_C = -100μA, I_B = 0	-40	-75	-	-40	-75	-	-24	-30	-	V
$V_{(BR)CBO}$	I_C = -10μA, I_E = 0	-40	-80	-	-40	-80	-	-24	-60	-	V
$V_{(BR)EBO}$	I_E = -10μA, I_C = 0	-40	-100	-	-40	-100	-	-24	-80	-	V
$V_{(BR)EIO}$	I_{EI} = 10μA, $I_B = I_C$ = 0	40	100	-	40	100	-	24	80	-	V
$V_{CE\ SAT}$	I_C = -1mA, I_B = -100μA	-	-0.16	-0.4	-	-0.16	-0.4	-	-0.16	-0.4	V
V_{BE} (Note 4)	I_C = -100μA, V_{CE} = -5V	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	V
h_{FE} (Note 4)	I_C = -100μA, V_{CE} = -5V	40	85	250	40	85	250	30	85	300	
	I_C = -1mA, V_{CE} = -5V	20	47	200	20	47	200	15	47	200	
$\lvert\Delta V_{BE}/\Delta T\rvert$ (Note 4)	I_C = -100μA, V_{CE} = -5V	-	2.2	-	-	2.2	-	-	2.2	-	mV/°C

I_{CBO} Collector-Cutoff Current

I_{CEO} Collector-Cutoff Current

$V_{(BR)CEO}$ Collector-to-Emitter Breakdown Voltage

$V_{(BR)CBO}$ Collector-to-Base Breakdown Voltage

$V_{(BR)CIO}$ Collector-to-Substrate Breakdown Voltage

$V_{(BR)EBO}$ Emitter-to-Base Breakdown Voltage

V_Z Emitter-to-Base Zener Voltage

$V_{CE\ SAT}$ Collector-to-Emitter Saturation Voltage

V_{BE} Base-to-Emitter Voltage

h_{FE} DC Forward-Current Transfer Ratio

$\lvert\Delta V_{BE}/\Delta T\rvert$ Magnitude of Temperature Coefficient: (for each transistor)

NOTE:

4. Actual forcing current is via the emitter for this test.

Electrical Specifications For Equipment Design At $T_A = 25^oC$ (CA3096A Only)

PARAMETER	SYMBOL	TEST CONDITIONS	CA3096A			UNITS
			MIN	TYP	MAX	
FOR TRANSISTORS Q_1 AND Q_2 (AS A DIFFERENTIAL AMPLIFIER)						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 5V, I_C = 1mA	-	0.3	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		-	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	1.1	-	μV/°C
FOR TRANSISTORS Q_4 AND Q_5 (AS A DIFFERENTIAL AMPLIFIER)						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = -5V, I_C = -100μA, R_S = 0	-	0.15	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		-	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	0.54	-	μV/°C

Electrical Specifications

Typical Values Intended Only for Design Guidance At $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
DYNAMIC CHARACTERISTICS FOR EACH NPN TRANSISTOR				
Noise Figure (Low Frequency)	NF	f = 1kHz, V_{CE} = 5V, I_C = 1mA, R_S = 1kΩ	2.2	dB
Low-Frequency, Input Resistance	R_I	f = 1.0kHz, V_{CE} = 5V I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance	R_O	f = 1.0kHz, V_{CE} = 5V I_C = 1 mA	80	kΩ
Admittance Characteristics				
Forward Transfer Admittance	y_{FE} g_{FE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	7.5	mS
	y_{FE} b_{FE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	-j13	mS
Input Admittance	y_{IE} g_{IE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	2.2	mS
	y_{IE} b_{IE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	j3.1	mS
Output Admittance	y_{OE} g_{OE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	0.76	mS
	y_{OE} b_{OE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	j2.4	mS
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 1.0mA	280	MHz
		V_{CE} = 5V, I_C = 5mA	335	MHz
Emitter-To-Base Capacitance	C_{EB}	V_{EB} = 3V	0.75	pF
Collector-To-Base Capacitance	C_{CB}	V_{CB} = 3V	0.46	pF
Collector-To-Substrate Capacitance	C_{CI}	V_{CI} = 3V	3.2	pF
DYNAMIC CHARACTERISTICS FOR EACH PNP TRANSISTOR				
Noise Figure (Low Frequency)	NF	f = 1kHz, I_C = 100μA, R_S = 1kΩ	3	dB
Low-Frequency Input Resistance	R_I	f = 1kHz, V_{CE} = 5V, I_C = 100μA	27	kΩ
Low-Frequency Output Resistance	R_O	f = 1kHz, V_{CE} = 5V, I_C = 100μA	680	kΩ
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 100μA	6.8	MHz
Emitter-To-Base Capacitance	C_{EB}	V_{EB} = -3V	0.85	pF
Collector-To-Base Capacitance	C_{CB}	V_{CB} = -3V	2.25	pF
Base-To-Substrate Capacitance	C_{BI}	V_{BI} = 3V	3.05	pF

Typical Applications

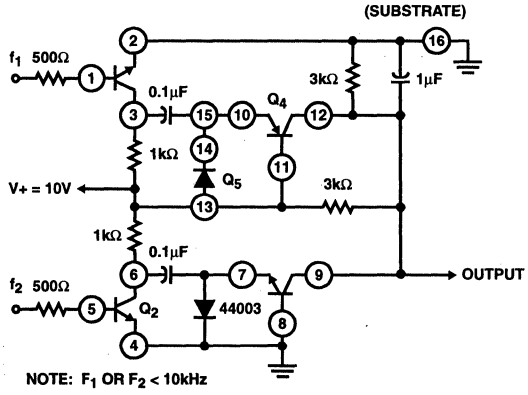


FIGURE 1. FREQUENCY COMPARATOR USING CA3096

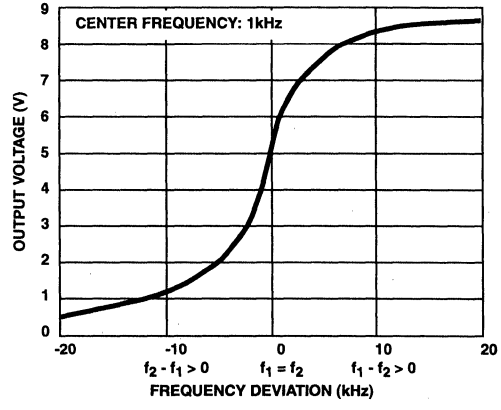


FIGURE 2. FREQUENCY COMPARATOR CHARACTERISTICS

Typical Applications (Continued)

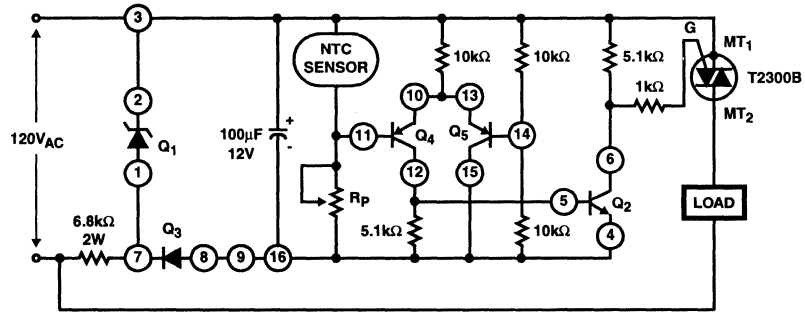


FIGURE 3. LINE-OPERATED LEVEL SWITCH USING CA3096A OR CA3096

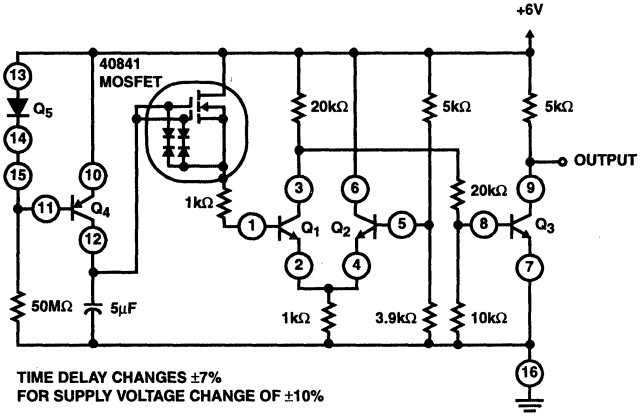
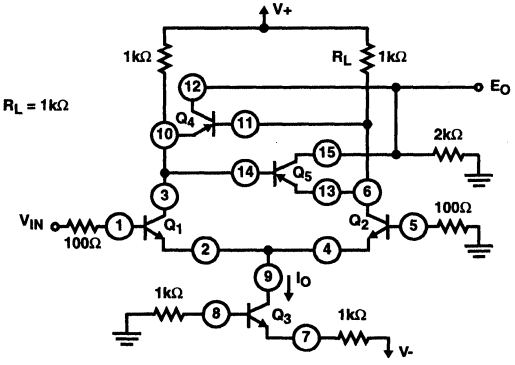


FIGURE 4. ONE-MINUTE TIMER USING CA3096A AND A MOSFET

$$V_T = \pm \frac{36}{I_O R_L}$$

IF I_O = 1mA AND R_L = 1kΩ
V_T = ± 36mV



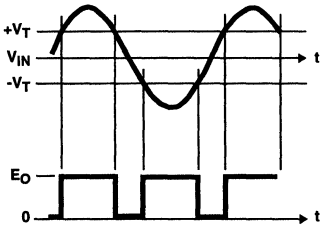


FIGURE 5. CA3096A SMALL-SIGNAL ZERO VOLTAGE DETECTOR HAVING NOISE IMMUNITY

Typical Applications (Continued)

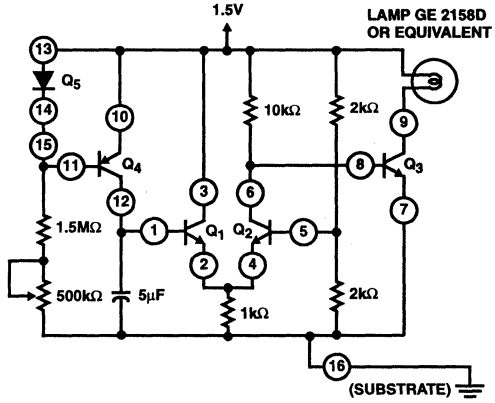
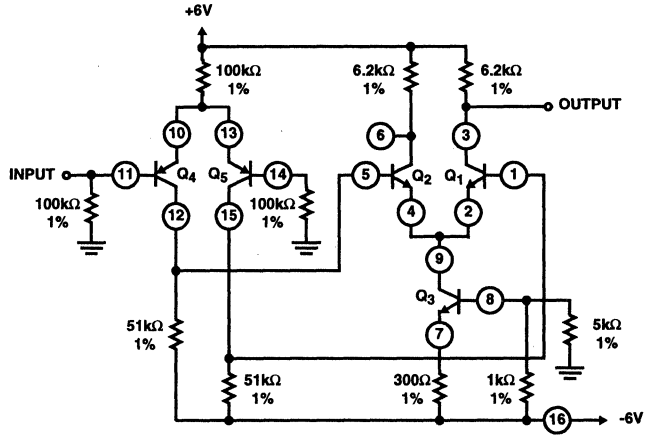


FIGURE 6. TEN-SECOND TIMER OPERATED FROM 1.5V SUPPLY USING CA3096



NOTES:

5. Can be operated with either dual supply or single supply.
6. Wide-input common mode range +5V to -5V.
7. Low bias current: <1μA.

FIGURE 7. CASCADE OF DIFFERENTIAL AMPLIFIERS USING CA3096A

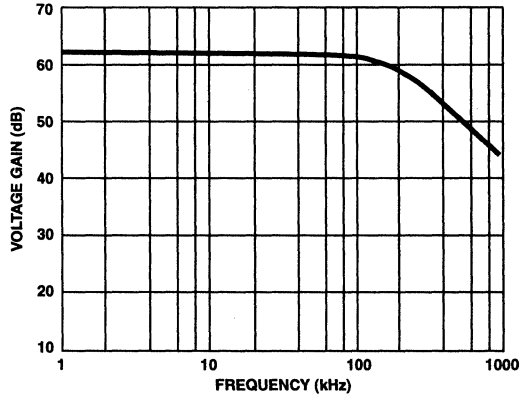


FIGURE 8. FREQUENCY RESPONSE

Typical Performance Curves

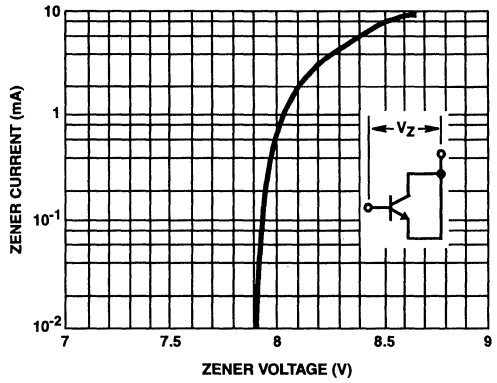


FIGURE 9. BASE-TO-EMITTER ZENER CHARACTERISTIC (NPN)

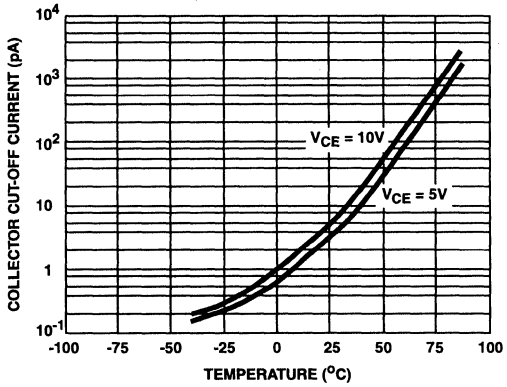


FIGURE 10. COLLECTOR CUT-OFF CURRENT (I_{CEO}) vs TEMPERATURE (NPN)

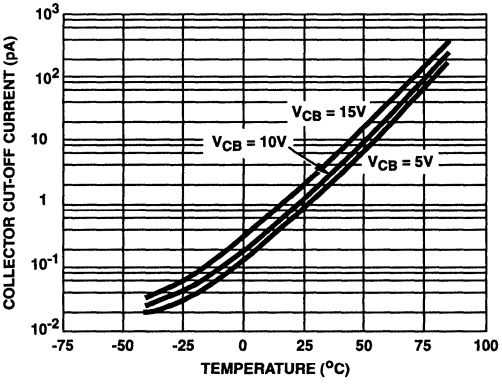


FIGURE 11. COLLECTOR CUT-OFF CURRENT (I_{CBO}) vs TEMPERATURE (NPN)

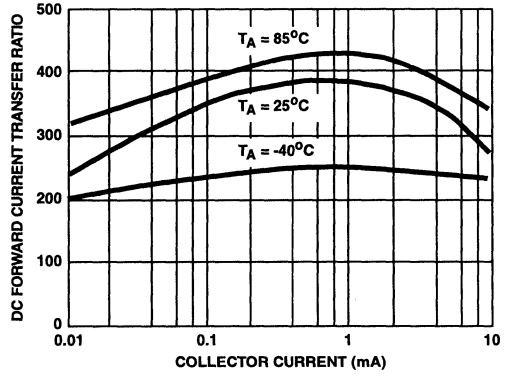


FIGURE 12. TRANSISTOR (NPN) h_{FE} vs COLLECTOR CURRENT

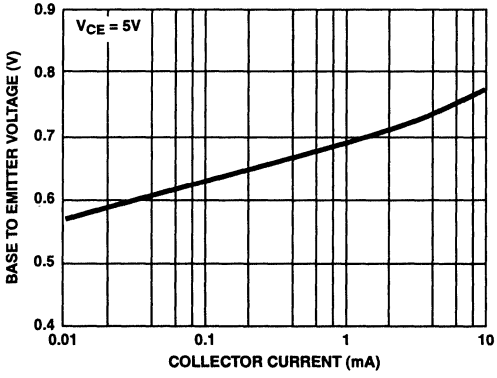


FIGURE 13. V_{BE} (NPN) vs COLLECTOR CURRENT

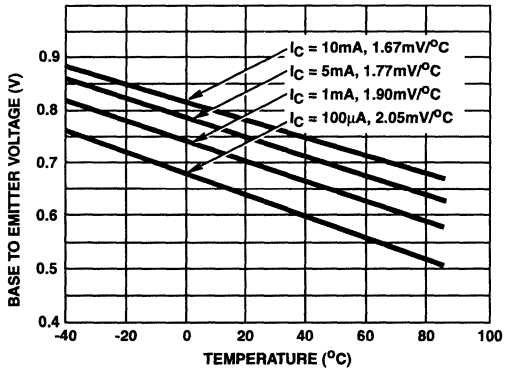


FIGURE 14. V_{BE} (NPN) vs TEMPERATURE

Typical Performance Curves (Continued)

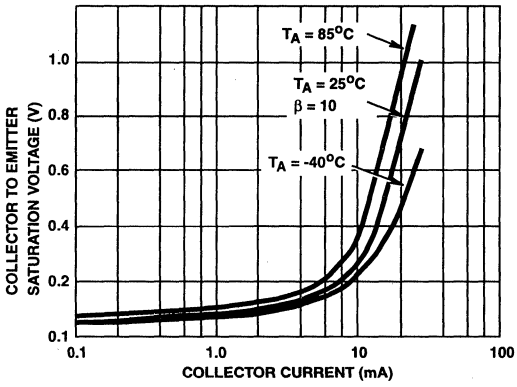


FIGURE 15. $V_{CE\ SAT}$ (NPN) vs COLLECTOR CURRENT

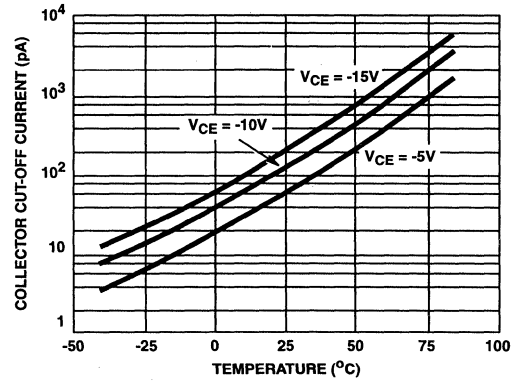


FIGURE 16. COLLECTOR CUT-OFF CURRENT (I_{CEO}) vs TEMPERATURE (PNP)

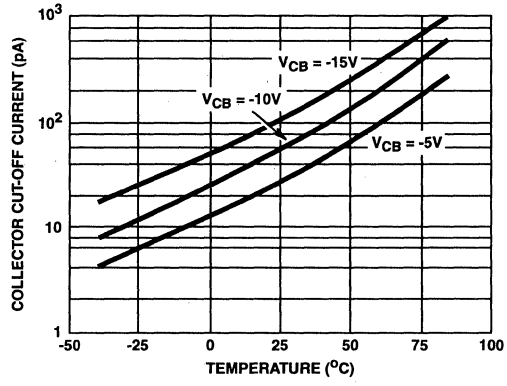


FIGURE 17. COLLECTOR CUT-OFF CURRENT (I_{CBO}) vs TEMPERATURE (PNP)

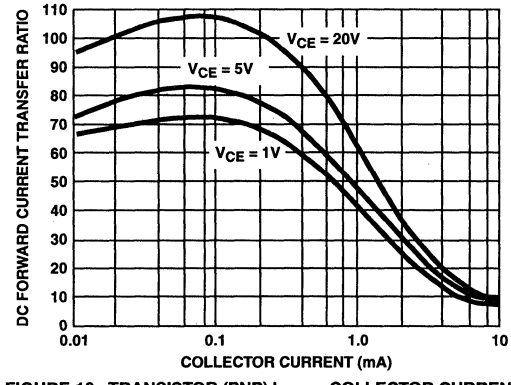


FIGURE 18. TRANSISTOR (PNP) h_{FE} vs COLLECTOR CURRENT

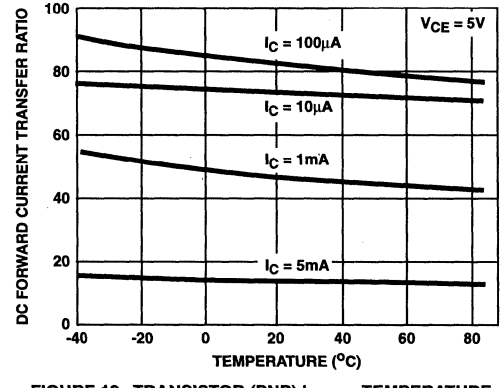


FIGURE 19. TRANSISTOR (PNP) h_{FE} vs TEMPERATURE

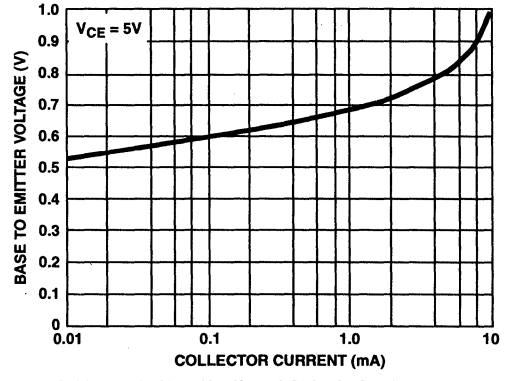


FIGURE 20. V_{BE} (PNP) vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

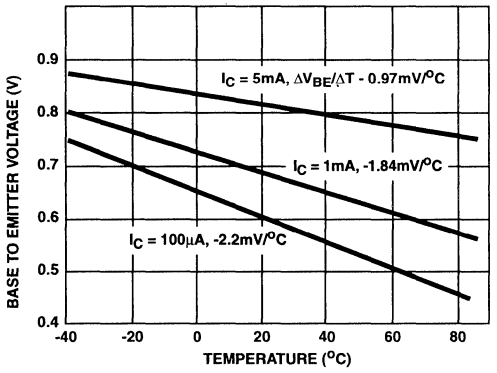


FIGURE 21. V_{BE} (PNP) vs TEMPERATURE

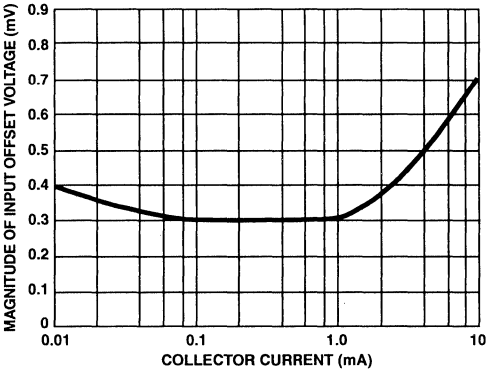


FIGURE 22. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR NPN TRANSISTOR Q_1 - Q_2

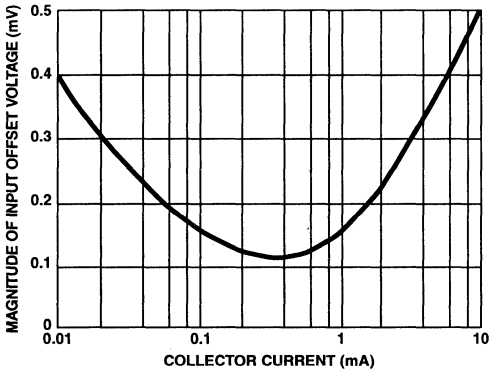


FIGURE 23. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR PNP TRANSISTOR Q_4 - Q_5

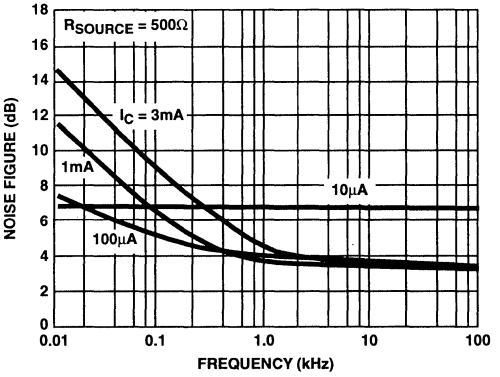


FIGURE 24. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

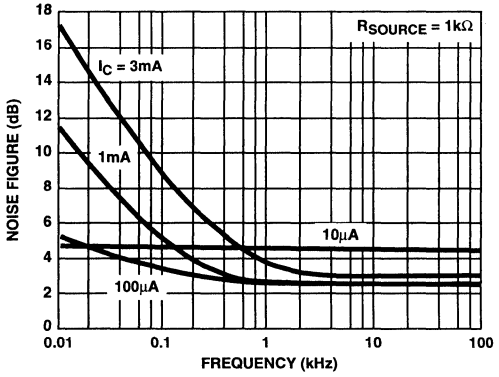


FIGURE 25. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

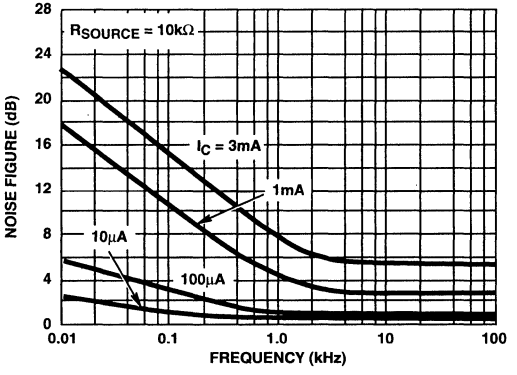


FIGURE 26. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

Typical Performance Curves (Continued)

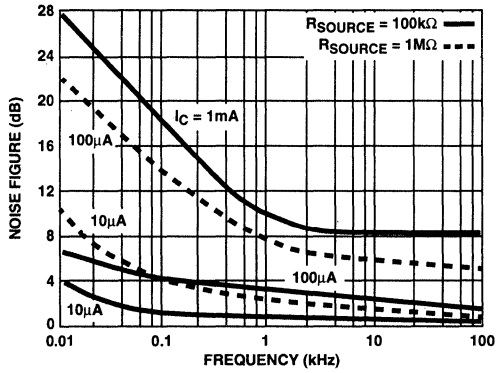


FIGURE 27. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

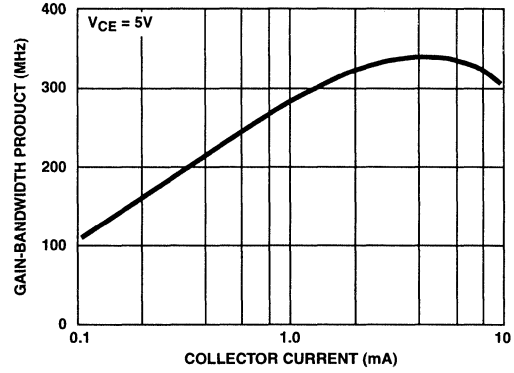


FIGURE 28. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (NPN)

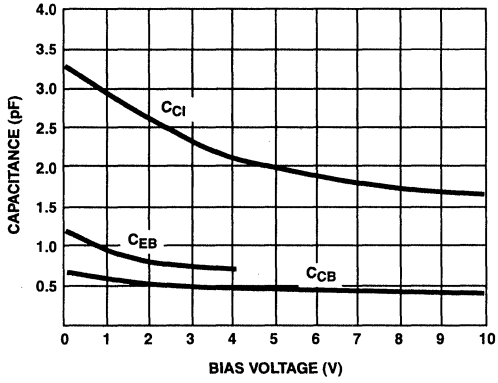


FIGURE 29. CAPACITANCE vs BIAS VOLTAGE (NPN)

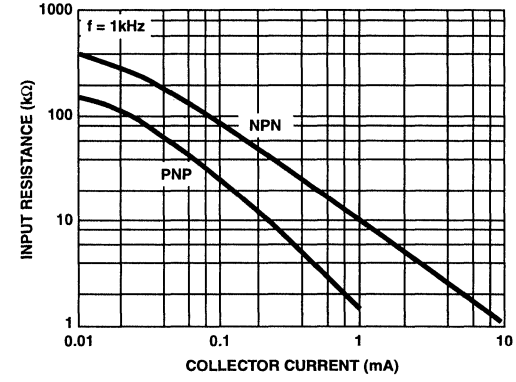


FIGURE 30. INPUT RESISTANCE vs COLLECTOR CURRENT

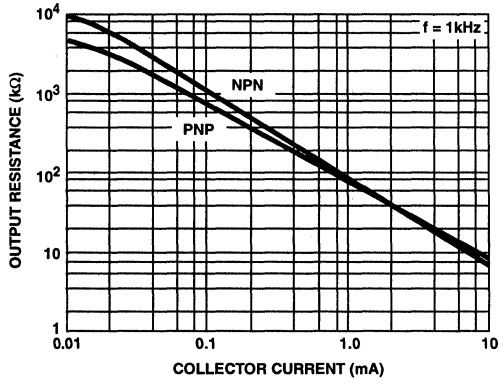


FIGURE 31. OUTPUT RESISTANCE vs COLLECTOR CURRENT

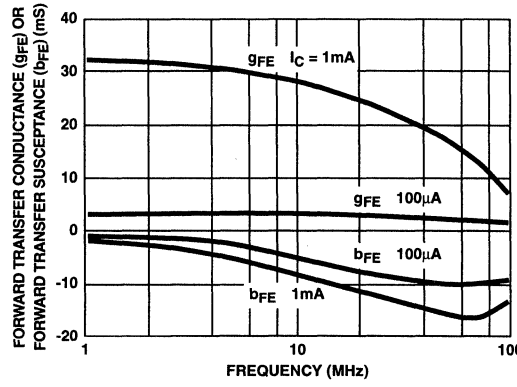


FIGURE 32. FORWARD TRANSCONDUCTANCE vs FREQUENCY

Typical Performance Curves (Continued)

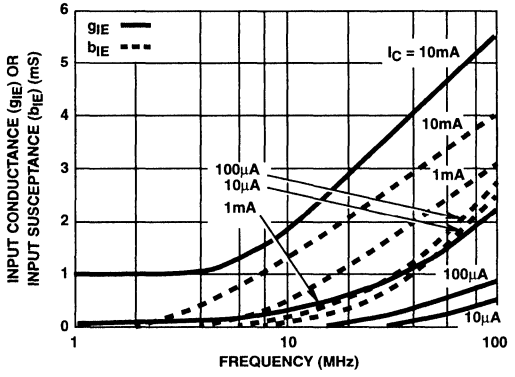


FIGURE 33. INPUT ADMITTANCE vs FREQUENCY

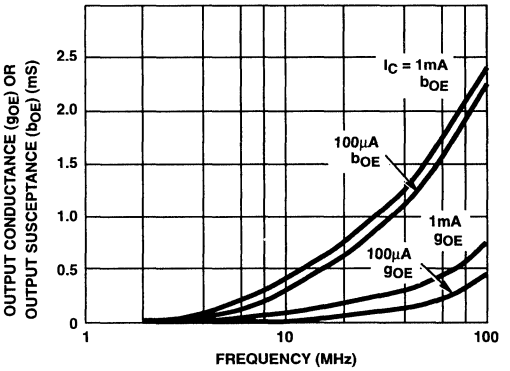


FIGURE 34. OUTPUT ADMITTANCE vs FREQUENCY

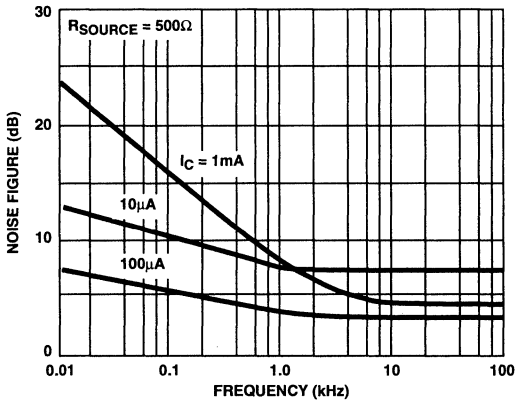


FIGURE 35. NOISE FIGURE vs FREQUENCY (PNP)

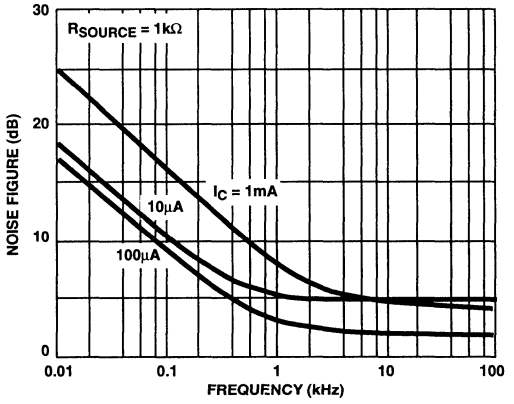


FIGURE 36. NOISE FIGURE vs FREQUENCY (PNP)

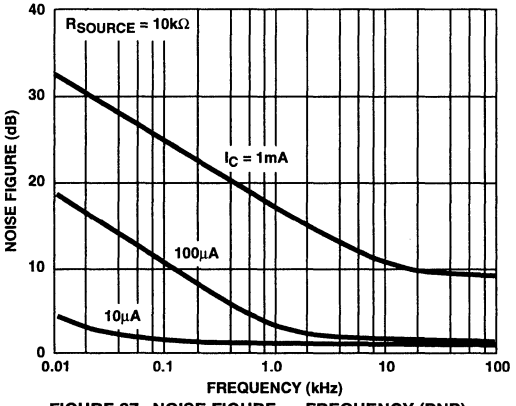


FIGURE 37. NOISE FIGURE vs FREQUENCY (PNP)

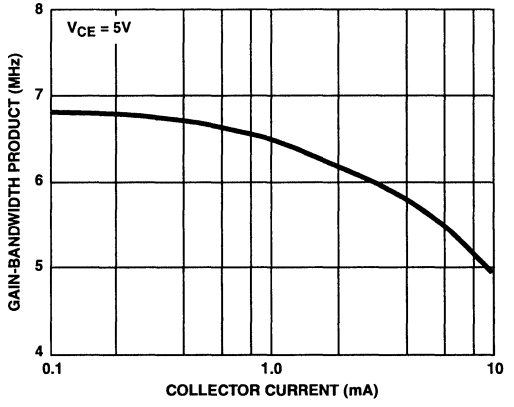


FIGURE 38. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (PNP)

Typical Performance Curves (Continued)

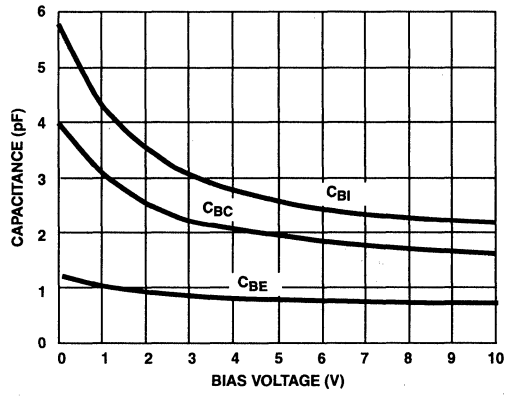
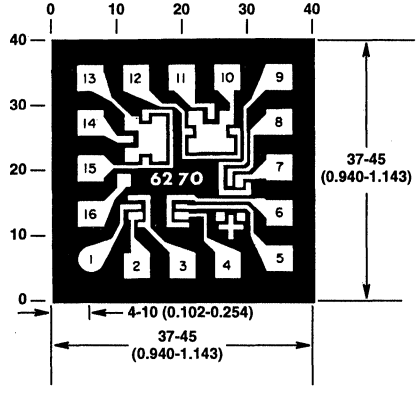


FIGURE 39. CAPACITANCE vs BIAS VOLTAGE (PNP)

Metallization Mask Layout

CA3096H



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57 degrees instead of 90 degrees with respect to the face of the chip. Therefore, the isolated chip is actually 7mils (0.17mm) larger in both dimensions.

HARRIS SEMICONDUCTOR

CA3127

August 1996

High Frequency NPN Transistor Array

Features

- Gain Bandwidth Product (f_T) . . . . . >1GHz
- Power Gain . . . . . 30dB (Typ) at 100MHz
- Noise Figure . . . . . 3.5dB (Typ) at 100MHz
- Five Independent Transistors on a Common Substrate

Applications

- VHF Amplifiers
- Multifunction Combinations - RF/Mixer/Oscillator
- Sense Amplifiers
- Synchronous Detectors
- VHF Mixers
- IF Converter
- IF Amplifiers
- Synthesizers
- Cascade Amplifiers

Description

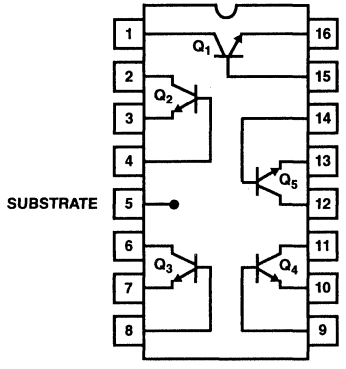
The CA3127 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1GHz, making the CA3127 useful from DC to 500MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3127E	-55 to 125	16 Ld PDIP	E16.3
CA3127M (3127)	-55 to 125	16 Ld SOIC	M16.15
CA3127M96 (3127)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Pinout

CA3127
(PDIP, SOIC)
TOP VIEW



7 ARRAYS AND DIFF. AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 662.3

Absolute Maximum Ratings

The following ratings apply for each transistor in the device

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Collector Current, I_C 20mA

Operating Conditions

Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 175
Maximum Power Dissipation, P_D (Any One Transistor) 85mW
Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Packages) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (Terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25°C$

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (For Each Transistor)						
Collector-to-Base Breakdown Voltage	$I_C = 10\mu A$, $I_E = 0$		20	32	-	V
Collector-to-Emitter Breakdown Voltage	$I_C = 1mA$, $I_B = 0$		15	24	-	V
Collector-to-Substrate Breakdown-Voltage	$I_{C1} = 10\mu A$, $I_B = 0$, $I_E = 0$		20	60	-	V
Emitter-to-Base Breakdown Voltage (Note 3)	$I_E = 10\mu A$, $I_C = 0$		4	5.7	-	V
Collector-Cutoff-Current	$V_{CE} = 10V$ $I_B = 0$		-	-	0.5	µA
Collector-Cutoff-Current	$V_{CB} = 10V$, $I_E = 0$		-	-	40	nA
DC Forward-Current Transfer Ratio	$V_{CE} = 6V$	$I_C = 5mA$	35	88	-	
		$I_C = 1mA$	40	90	-	
		$I_C = 0.1mA$	35	85	-	
Base-to-Emitter Voltage	$V_{CE} = 6V$	$I_C = 5mA$	0.71	0.81	0.91	V
		$I_C = 1mA$	0.66	0.76	0.86	V
		$I_C = 0.1mA$	0.60	0.70	0.80	V
Collector-to-Emitter Saturation Voltage	$I_C = 10mA$, $I_B = 1mA$		-	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 and Q_2 Matched $V_{CE} = 6V$, $I_C = 1mA$		-	0.5	5	mV
Magnitude of Difference in I_B			-	0.2	3	µA
DYNAMIC CHARACTERISTICS						
Noise Figure	$f = 100kHz$, $R_S = 500\Omega$, $I_C = 1mA$		-	2.2	-	dB
Gain-Bandwidth Product	$V_{CE} = 6V$, $I_C = 5mA$		-	1.15	-	GHz
Collector-to-Base Capacitance	$V_{CB} = 6V$, $f = 1MHz$		-	See Fig. 5	-	pF
Collector-to-Substrate Capacitance	$V_{CI} = 6V$, $f = 1MHz$		-		-	pF
Emitter-to-Base Capacitance	$V_{BE} = 4V$, $f = 1MHz$		-		-	pF
Voltage Gain	$V_{CE} = 6V$, $f = 10MHz$, $R_L = 1k\Omega$, $I_C = 1mA$		-	28	-	dB
Power Gain	Cascode Configuration $f = 100MHz$, $V+ = 12V$, $I_C = 1mA$		27	30	-	dB
Noise Figure			-	3.5	-	dB
Input Resistance	Common-Emitter Configuration $V_{CE} = 6V$, $I_C = 1mA$, $f = 200$ MHz		-	400	-	Ω
Output Resistance			-	4.6	-	kΩ
Input Capacitance			-	3.7	-	pF
Output Capacitance			-	2	-	pF
Magnitude of Forward Transadmittance			-	24	-	mS

NOTE:

3. When used as a zener for reference voltage, the device must not be subjected to more than 0.1mJ of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10mA.

Test Circuits

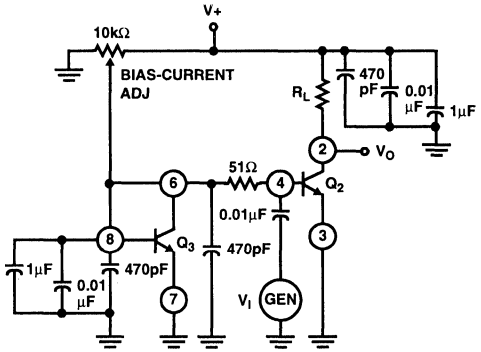
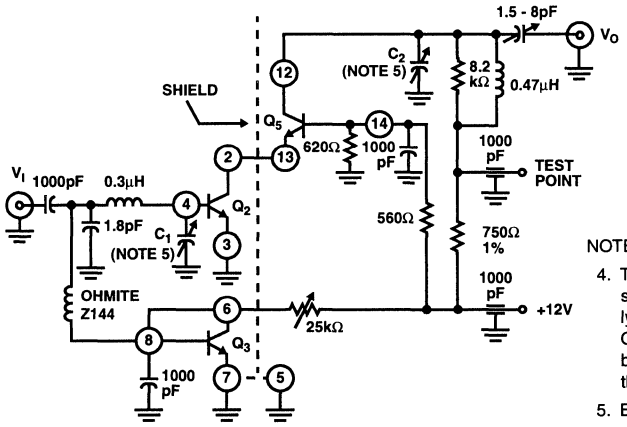


FIGURE 1. VOLTAGE-GAIN TEST CIRCUIT USING CURRENT-MIRROR BIASING FOR Q_2



NOTES:

4. This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q_3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.
5. E.F. Johnson number 160-104-1 or equivalent.

FIGURE 2. 100MHz POWER-GAIN AND NOISE-FIGURE TEST CIRCUIT

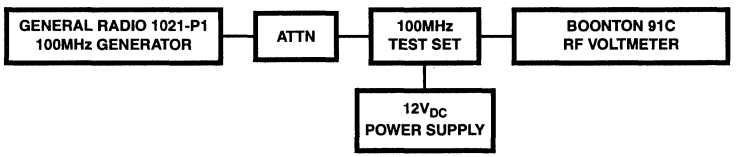


FIGURE 3A. POWER GAIN SET-UP

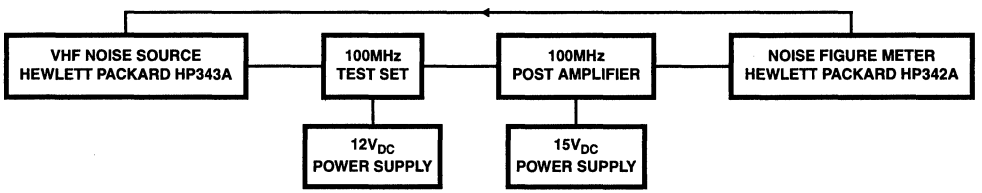


FIGURE 3B. NOISE FIGURE SET-UP

FIGURE 3. BLOCK DIAGRAMS OF POWER-GAIN AND NOISE-FIGURE TEST SET-UPS

Typical Performance Curves

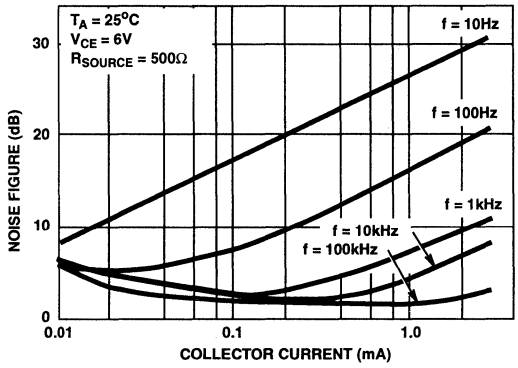


FIGURE 4. NOISE FIGURE vs COLLECTOR CURRENT

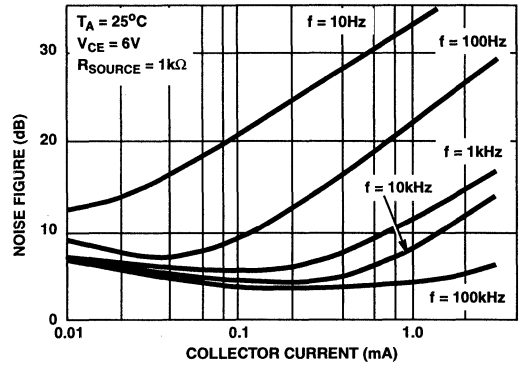


FIGURE 5. NOISE FIGURE vs COLLECTOR CURRENT

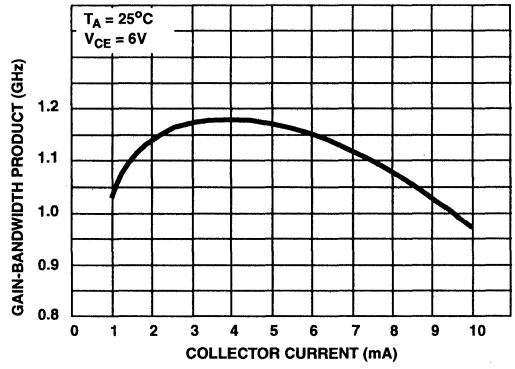


FIGURE 6. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT

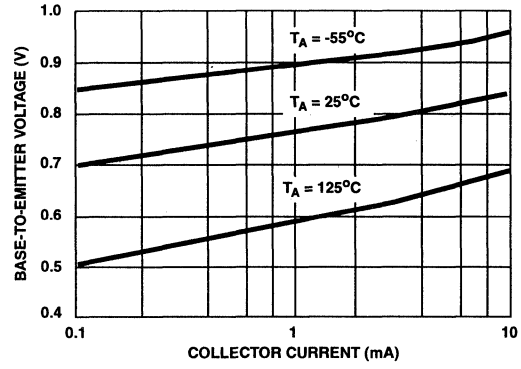


FIGURE 7. BASE-TO-EMITTER VOLTAGE vs COLLECTOR CURRENT

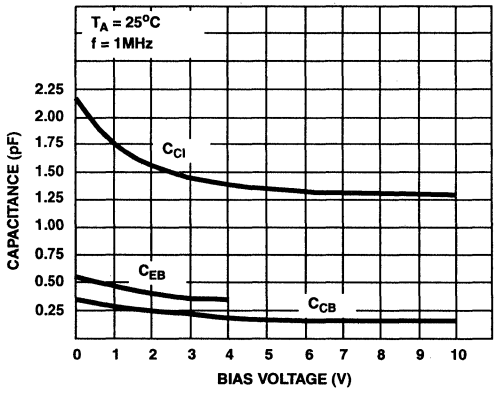


FIGURE 8A. CAPACITANCE vs BIAS VOLTAGE FOR Q_2

TRANSISTOR	CAPACITANCE (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	PKG	TOTAL	PKG	TOTAL	PKG	TOTAL	PKG	TOTAL
BIAS (V)	-	6V	-	6V	-	4V	-	6V
Q_1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q_2	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q_3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q_4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q_5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

FIGURE 8B. TYPICAL CAPACITANCE VALUES AT f = 1MHz. THREE TERMINAL MEASUREMENT. GUARD ALL TERMINALS EXCEPT THOSE UNDER TEST.

Typical Performance Curves (Continued)

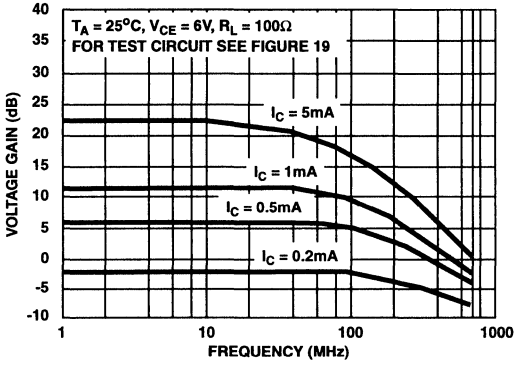


FIGURE 9. VOLTAGE GAIN vs FREQUENCY

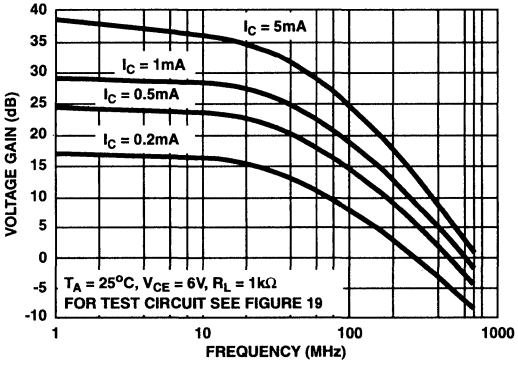


FIGURE 10. VOLTAGE GAIN vs FREQUENCY

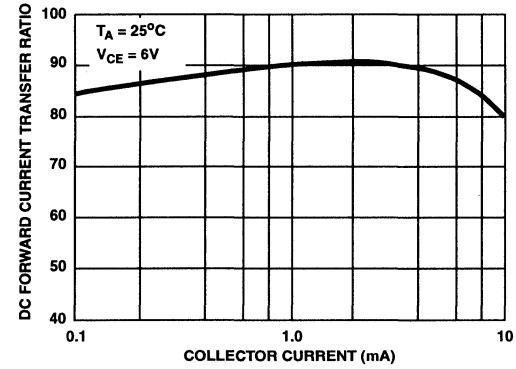


FIGURE 11. DC FORWARD-CURRENT TRANSFER RATIO (h_{FE}) vs COLLECTOR CURRENT

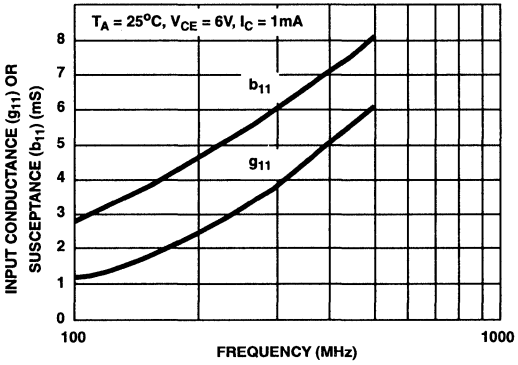


FIGURE 12. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

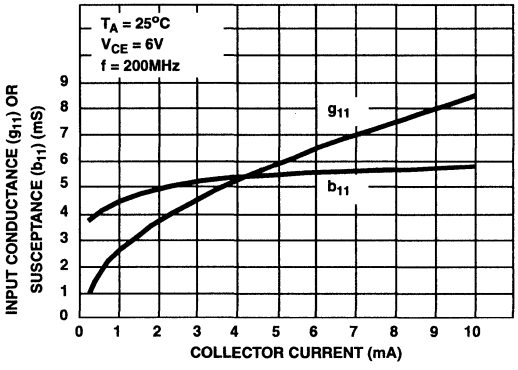


FIGURE 13. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR CURRENT

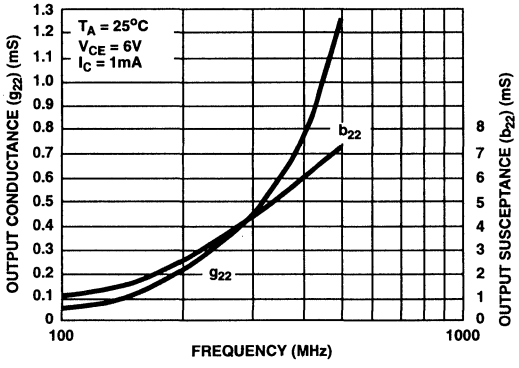


FIGURE 14. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

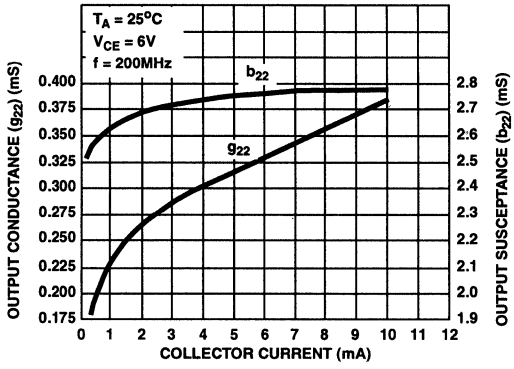


FIGURE 15. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR CURRENT

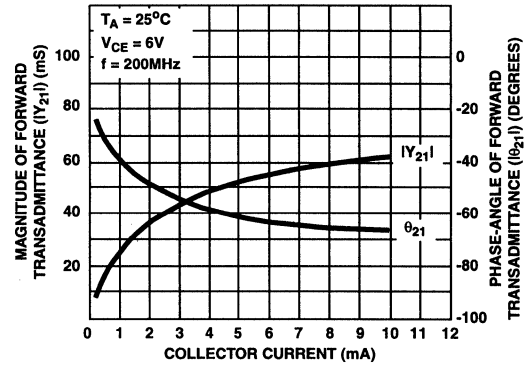


FIGURE 16. FORWARD TRANSADMITTANCE (Y_{21}) vs COLLECTOR CURRENT

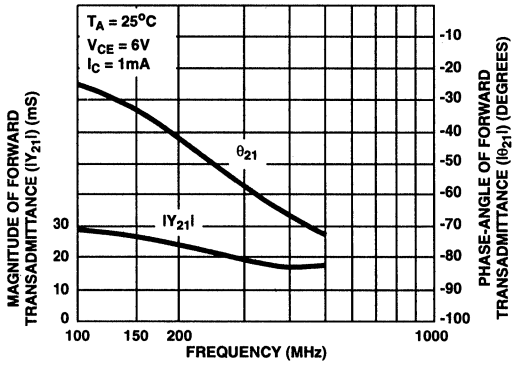


FIGURE 17. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY

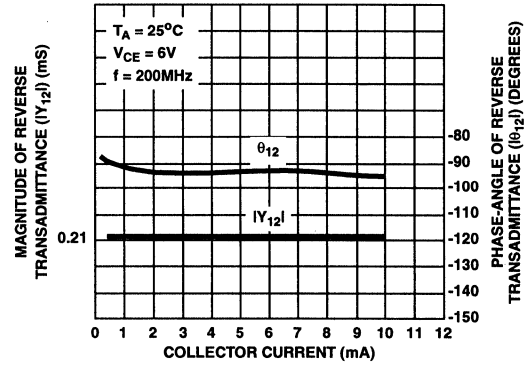


FIGURE 18. REVERSE TRANSADMITTANCE (Y_{12}) vs COLLECTOR CURRENT

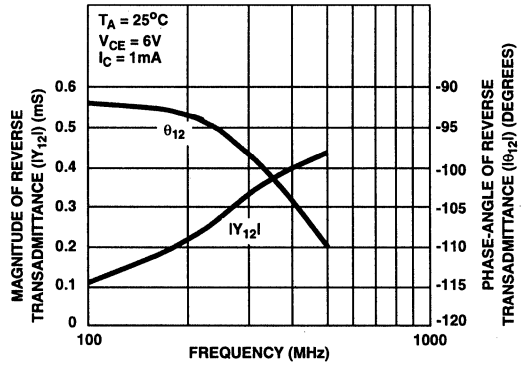


FIGURE 19. REVERSE TRANSADMITTANCE (Y_{12}) vs FREQUENCY

NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section

HARRIS SEMICONDUCTOR

CA3141

November 1996

High-Voltage Diode Array For Commercial, Industrial and Military Applications

Features

- **Matched Monolithic Construction**
  - **V_F Match (Each Diode Pair).... 0.55mV At I_F = 1mA**
- **Low Diode Capacitance..... 0.3pF (Typ) at V_R = 2V**
- **High Diode-to-Substrate Breakdown..... 30V (Min)**
- **Low Reverse (Leakage) Current ..... 100nA (Max)**

Applications

- **Balanced Modulators or Demodulators**
- **Analog Switches**
- **High-Voltage Diode Gates**
- **Current Ratio Detectors**

Ordering Information

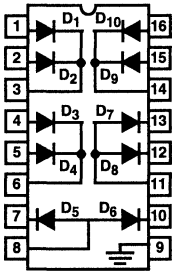
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3141E	-55 to 125	16 Ld PDIP	E16.3

Description

The CA3141E High Voltage Diode Array Consists of ten general purpose high reverse breakdown diodes. Six diodes are internally connected to form three common cathode diode pairs, and the remaining four diodes are internally connected to form two common anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141 extremely useful for a wide variety of applications in communications and switching systems.

Pinout

CA3141
(PDIP)
TOP VIEW



7 ARRAYS AND DIFF. AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **906.3**

HARRIS SEMICONDUCTOR

CA3146, CA3146A, CA3183, CA3183A

August 1996

High-Voltage Transistor Arrays

Features

- Matched General Purpose Transistors
  - V_{BE} Match ..... ±5mV (Max)
- Operation from DC to 120MHz (CA3146, CA3146A)
- Low Noise Figure 3.2dB (CA3146, CA3146A)
- High I_C ..... 75mA (Max) (CA3183, CA3183A)

Applications

- General Use in Signal Processing Systems in DC through VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- Lamp and Relay Drivers (CA3183, CA3183A)
- Thyristor Firing (CA3183, CA3183A)

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3146AE	-40 to 85	14 Ld PDIP	E14.3
CA3146AM (3146A)	-40 to 85	14 Ld SOIC	M14.15
CA3146AM96 (3146A)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15
CA3146E	-40 to 85	14 Ld PDIP	E14.3
CA3146M (3146)	-40 to 85	14 Ld SOIC	M14.15
CA3146M96 (3146)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15
CA3183AE	-40 to 85	16 Ld PDIP	E16.3
CA3183AM (3183A)	-40 to 85	16 Ld SOIC	M16.15
CA3183AM96 (3183A)	-40 to 85	16 Ld SOIC Tape and Reel	M16.15
CA3183E	-40 to 85	16 Ld PDIP	E16.3
CA3183M (3183)	-40 to 85	16 Ld SOIC	M16.15
CA3183M96 (3183)	-40 to 85	16 Ld SOIC Tape and Reel	M16.15

Description

The CA3146A, CA3146, CA3183A, and CA3183 are general purpose high voltage silicon NPN transistor arrays on a common monolithic substrate.

Types CA3146A and CA3146 consist of five transistors with two of the transistors connected to form a differentially connected pair. These types are recommended for low power applications in the DC through VHF range. (CA3146A and CA3146 are high voltage versions of the popular predecessor type CA3046.)

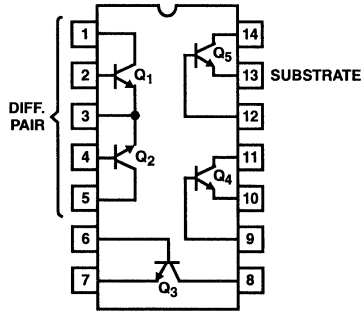
Types CA3183A and CA3183 consist of five high current transistors with independent connections for each transistor. In addition two of these transistors (Q_1 and Q_2) are matched at low current (i.e., 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. (CA3183A and CA3183 are high voltage versions of the popular predecessor type CA3083.)

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

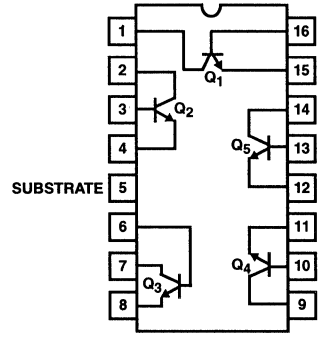
For detailed application information, see companion Application Note AN5296 "Application of the CA3018 Integrated Circuit Transistor Array."

Pinouts

CA3146, CA3146A (PDIP, SOIC)
TOP VIEW



CA3183, CA3183A (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **532.3**

Absolute Maximum Ratings

Collector-to-Emitter Voltage (V_{CEO}):
- CA3146A, CA3183A 40V
- CA3146, CA3183 ..... 30V

Collector-to-Base Voltage (V_{CBO}):
- CA3146A, CA3183A 50V
- CA3146, CA3183 ..... 40V

Collector-to-Substrate Voltage (V_{CIO}, Note 1)
- CA3146A, CA3183A 50V
- CA3146, CA3183 ..... 40V

Emitter-to-Base Voltage (V_{EBO}) all types 5V

Collector Current
- CA3146A, CA3146 ..... 50mA
- CA3183A, CA3183 ..... 75mA

Base Current (I_B) - CA3183A, CA3183 ..... 20mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
14 Ld PDIP Package	100
14 Ld SOIC Package	185
16 Ld PDIP Package	90
16 Ld SOIC Package	175

Maximum Power Dissipation (Any One Transistor, Note 3)
- CA3146A, CA3146 ..... 300mW
- CA3183A, CA3183 ..... 500mW

Maximum Junction Temperature (Die) ..... 175°C

Maximum Junction Temperature (Plastic Package) ..... 150°C

Maximum Storage Temperature Range (all types) . . -65°C to 150°C

Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range ..... -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transisters, and to provide for normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. Care must be taken to avoid exceeding the maximum junction temperature. Use the total power dissipation (all transistors) and thermal resistances to calculate the junction temperature.

Electrical Specifications CA3146 Series

PARAMETER	SYMBOL	TEST CONDITIONS $T_A = 25°C$	TYPICAL PERF. CURVE FIG. NO.	CA3146 MN	CA3146 TYP	CA3146 MAX	CA3146A MIN	CA3146A TYP	CA3146A MAX	UNITS
DC CHARACTERISTICS FOR EACH TRANSISTOR										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	-	40	72	-	50	72	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	-	30	56	-	40	56	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 10\mu A$, $I_B = 0$, $I_E = 0$	-	40	72	-	50	72	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	-	5	7	-	5	7	-	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	1	-	See Curve	5	-	See Curve	5	µA
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	2	-	0.002	100	-	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 5V$, $I_C = 10mA$	3	-	85	-	-	85	-	-
		$V_{CE} = 5V$, $I_C = 1mA$	3	30	100	-	30	100	-	-
		$V_{CE} = 5V$, $I_C = 10\mu A$	3	-	90	-	-	90	-	-
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 1mA$	4	0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	$I_C = 10mA$, $I_B = 1mA$	5	-	0.33	-	-	0.33	-	V

Electrical Specifications CA3146 Series **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS $T_A = 25^oC$	TYPICAL PERF. CURVE FIG. NO.	CA3146 MN	CA3146 TYP	CA3146 MAX	CA3146A MIN	CA3146A TYP	CA3146A MAX	UNITS
DC CHARACTERISTICS FOR TRANSISTORS Q_1 AND Q_2 (AS A DIFFERENTIAL AMPLIFIER)										
Magnitude of Input Offset Voltage $\|V_{BE1} - V_{BE2}\|$	$\|V_{IO}\|$	V_{CE} = 5V, I_E = 1mA	6, 7	-	0.48	5	-	0.48	5	mV
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\|\frac{\Delta V_{BE}}{\Delta T}\right\|$	V_{CE} = 5V, I_E = 1mA	-	-	1.9	-	-	1.9	-	mV/°C
Magnitude of V_{IO} ($V_{BE1} - V_{BE2}$) Temperature Coefficient	$\left\|\frac{\Delta V_{IO}}{\Delta T}\right\|$	V_{CE} = 5V, $I_{C1} = I_{C2}$ = 1mA	-	-	1.1	-	-	1.1	-	µV/°C
Magnitude of Input Offset Current $\|I_{IO1} - I_{IO2}\|$ (CA3146AE and CA3146E Only)	I_{IO}	V_{CE} = 5V, $I_{C1} = I_{C2}$ = 1mA	8	-	0.3	2	-	0.3	2	µA
DYNAMIC CHARACTERISTICS										
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100µA, Source Resistance = 1kΩ	10	-	3.25	-	-	3.25	-	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward-Current Transfer Ratio	h_{FE}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	12	-	100	-	-	100	-	-
Short-Circuit Input Impedance	h_{IE}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	12	-	3.5	-	-	2.7	-	kΩ
Open-Circuit Output Impedance	h_{OE}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	12	-	15.6	-	-	15.6	-	µS
Open-Circuit Reverse Voltage Transfer Ratio	h_{RE}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	12	-	1.8×10^{-4}	-	-	1.8×10^{-4}	-	-
Admittance Characteristics:										
Forward Transfer Admittance	Y_{FE}	f = 1MHz, V_{CE} = 5V, I_C = 1 mA	13	-	31-j1.5	-	-	31-j1.5	-	mS
Input Admittance	Y_{IE}	f = 1MHz, V_{CE} = 5V, I_C = 1 mA	14	-	0.3 + j0.04	-	-	0.35 + j0.04	-	mS
Output Admittance	Y_{OE}	f = 1MHz, V_{CE} = 5V, I_C = 1 mA	15	-	0.001+ j0.03	-	-	0.001+ j0.03	-	mS
Reverse Transfer Admittance	Y_{RE}	f = 1MHz, V_{CE} = 5V, I_C = 1 mA	16		See Curve			See Curve		mS
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	17	300	500	-	300	500	-	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	18	-	0.70	-	-	0.70	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	18	-	0.37	-	-	0.37	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	18	-	2.2	-	-	2.2	-	pF

Electrical Specifications CA3183 Series

PARAMETER	SYMBOL	TEST CONDITIONS $T_A = 25^oC$	TYPICAL PERF. CURVE FIG. NO.	CA3183 MIN	CA3183 TYP	CA3183 MAX	CA3183A MIN	CA3183A TYP	CA3183A MAX	UNITS
DC CHARACTERISTICS FOR EACH TRANSISTOR										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\mu A$, $I_E = 0$	-	40	-	-	50	-	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	-	30	-	-	40	-	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100\mu A$, $I_B = 0$, $I_E = 0$	-	40	-	-	50	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 500\mu A$, $I_C = 0$	-	5	-	-	5	-	-	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	19	-	-	10	-	-	10	μA
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	20	-	-	1	-	-	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 3V$, $I_C = 10mA$	21, 22	40	-	-	40	-	-	-
		$V_{CE} = 5V$, $I_C = 50mA$	-	40	-	-	40	-	-	-
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 10mA$	23	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$ (Note 3)	$I_C = 50mA$, $I_B = 5mA$	24	-	1.7	3.0	-	1.7	3.0	V
FOR TRANSISTORS Q_1 AND Q_2 (AS A DIFFERENTIAL AMPLIFIER)										
Absolute Input Offset Voltage	$\lvert V_{IO} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	25	-	0.47	5	-	0.47	5	mV
Absolute Input Offset Current	$\lvert I_{IO} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	26	-	0.78	2.5	-	0.78	2.5	μA

Typical Performance Curves DC Characteristics - CA3146 Series

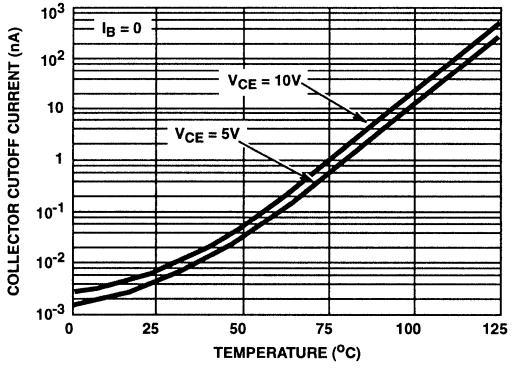


FIGURE 1. I_{CEO} vs TEMPERATURE FOR ANY TRANSISTOR

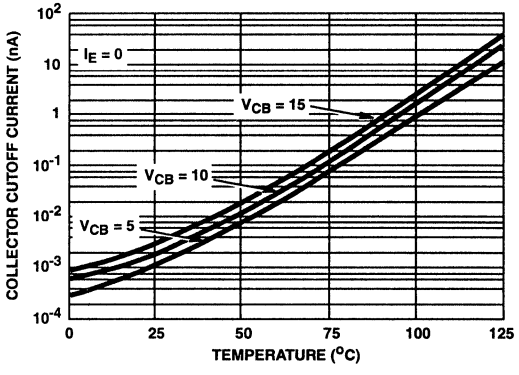


FIGURE 2. I_{CBO} vs TEMPERATURE FOR ANY TRANSISTOR

Typical Performance Curves DC Characteristics - CA3146 Series (Continued)

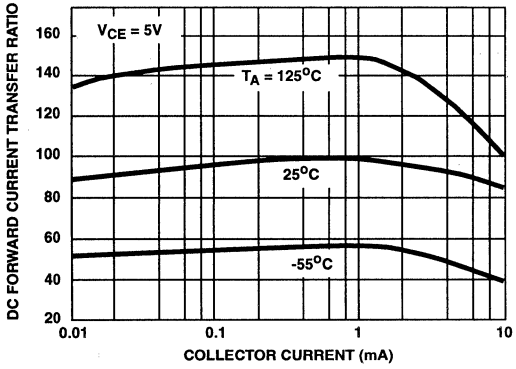


FIGURE 3. h_{FE} vs I_C FOR ANY TRANSISTOR

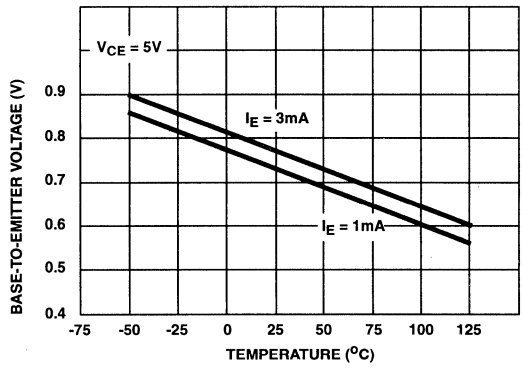


FIGURE 4. V_{BE} vs TEMPERATURE FOR ANY TRANSISTOR

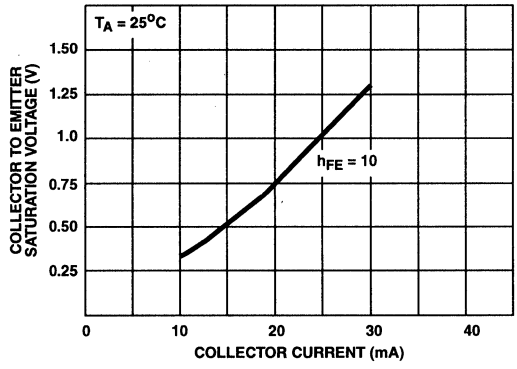


FIGURE 5. $V_{CE\ SAT}$ vs I_C FOR ANY TRANSISTOR

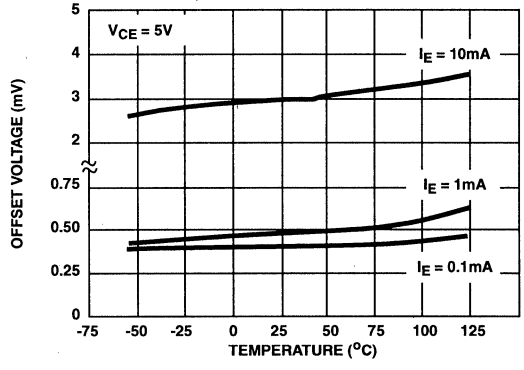


FIGURE 6. V_{IO} vs TEMPERATURE FOR Q_1 AND Q_2

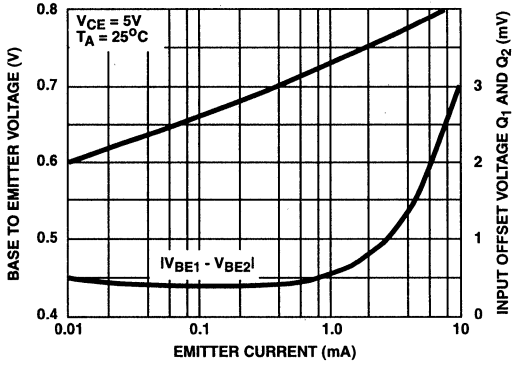


FIGURE 7. V_{BE} AND V_{IO} vs I_E FOR Q_1 AND Q_2

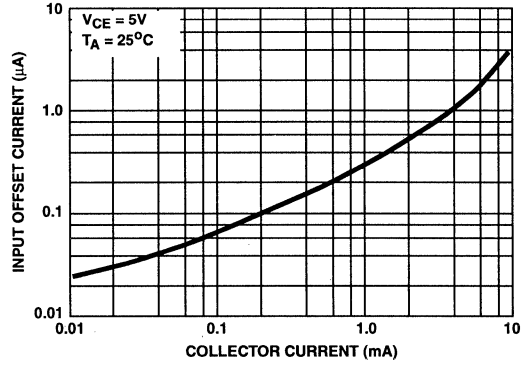


FIGURE 8. I_{IO} vs I_C FOR Q_1 AND Q_2

Typical Performance Curves Dynamic Characteristics (For Any Transistor) - CA3146 Series

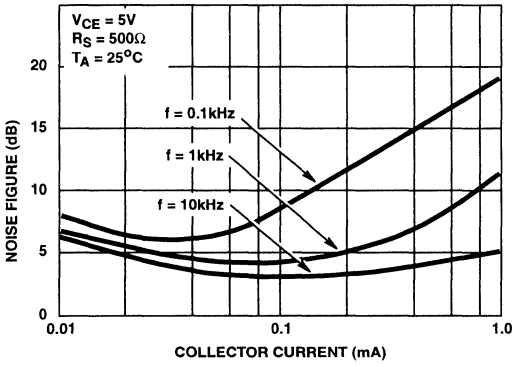


FIGURE 9. NF vs I_C AT R_S = 500Ω

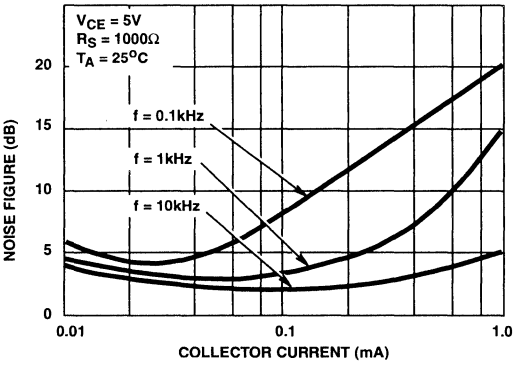


FIGURE 10. NF vs I_C AT R_S = 1kΩ

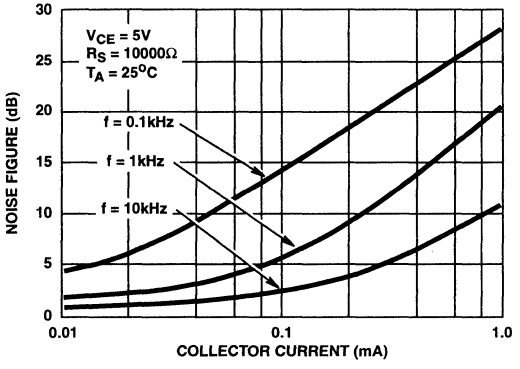


FIGURE 11. NF vs I_C AT R_S = 10kΩ

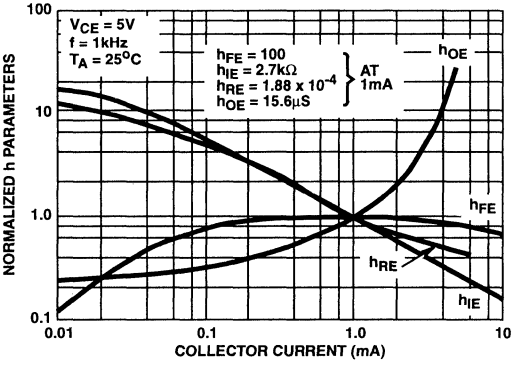


FIGURE 12. h_{FE}, h_{IE}, h_{OE}, h_{RE} vs I_C

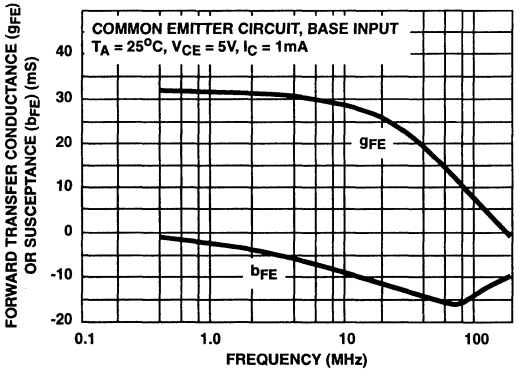


FIGURE 13. y_{FE} vs FREQUENCY

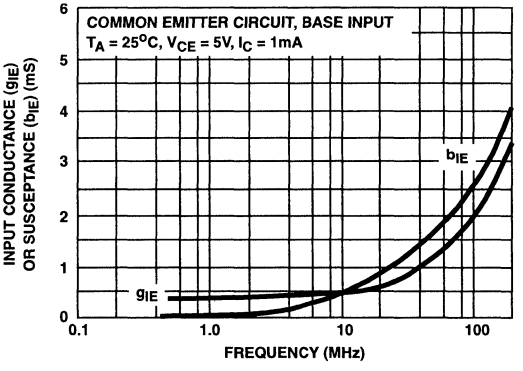


FIGURE 14. y_{IE} vs FREQUENCY

Typical Performance Curves Dynamic Characteristics (For Any Transistor) - CA3146 Series (Continued)

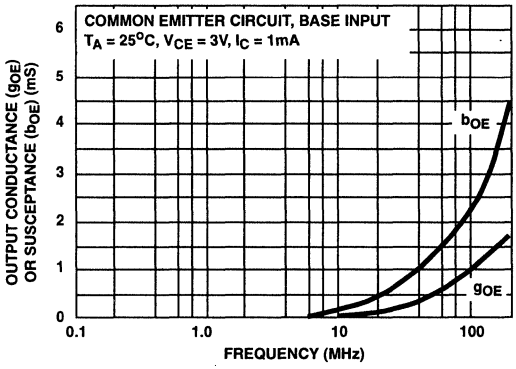


FIGURE 15. FIGURE 15. y_{OE} vs FREQUENCY

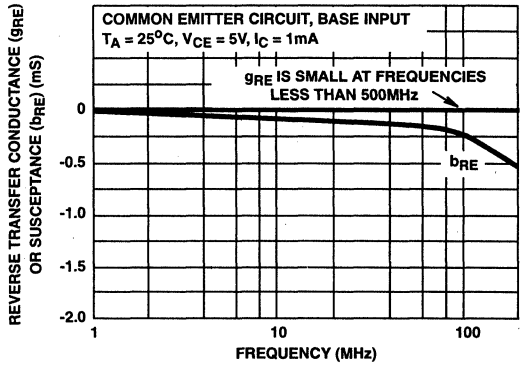


FIGURE 16. FIGURE 16. y_{RE} vs FREQUENCY

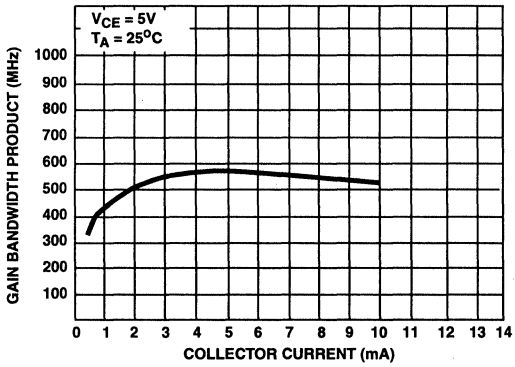


FIGURE 17. f_T vs I_C

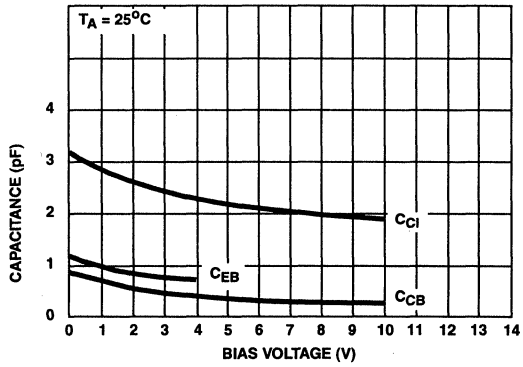


FIGURE 18. C_{EB}, C_{CB}, C_{CI} vs BIAS VOLTAGE

Typical Performance Curves DC Characteristics - CA3183 Series

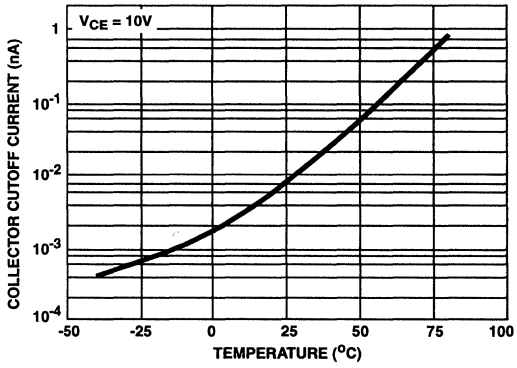


FIGURE 19. I_{CEO} vs TEMPERATURE FOR ANY TRANSISTOR

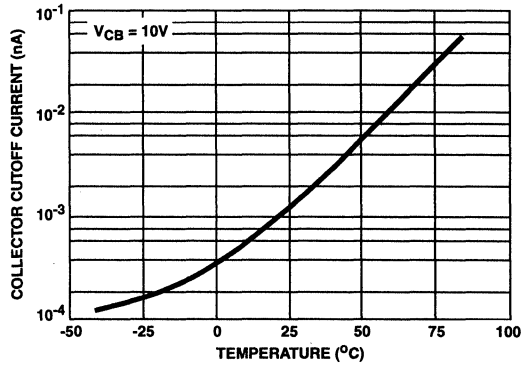


FIGURE 20. I_{CBO} vs TEMPERATURE FOR ANY TRANSISTOR

Typical Performance Curves DC Characteristics - CA3183 Series (Continued)

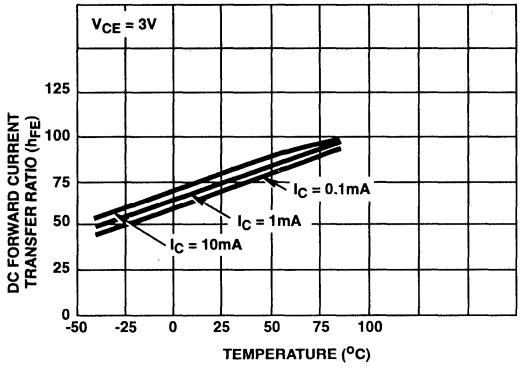


FIGURE 21. h_{FE} vs TEMPERATURE FOR ANY TRANSISTOR

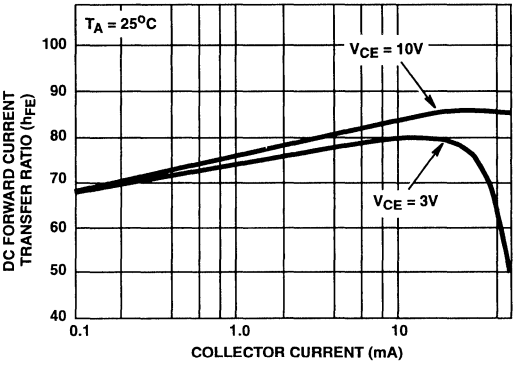


FIGURE 22. h_{FE} vs I_C FOR ANY TRANSISTOR

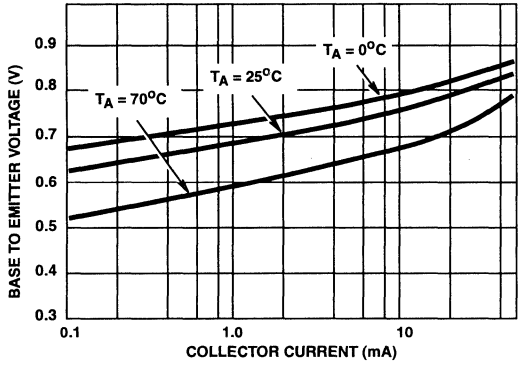


FIGURE 23. V_{BE} vs I_C FOR ANY TRANSISTOR

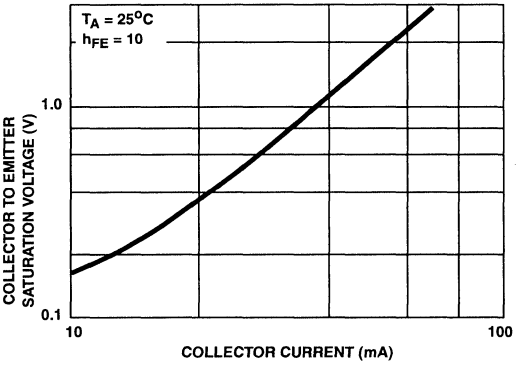


FIGURE 24. $V_{CE\ SAT}$ vs I_C FOR ANY TRANSISTOR

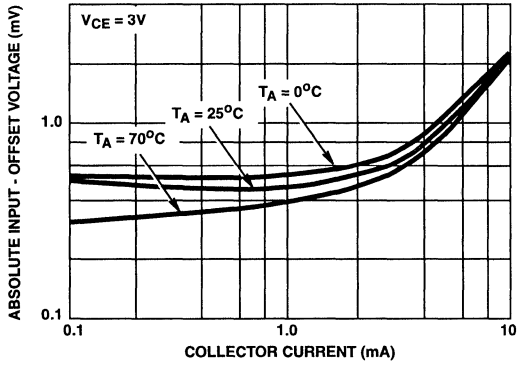


FIGURE 25. $|V_{IO}|$ vs I_C FOR DIFFERENTIAL AMPLIFIER (Q_1 AND Q_2)

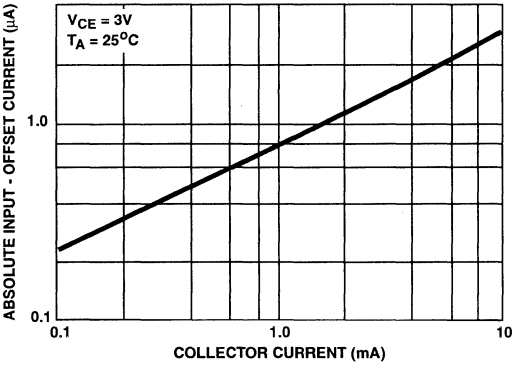


FIGURE 26. $|I_{IO}|$ vs I_C FOR DIFFERENTIAL AMPLIFIER (Q_1 AND Q_2)

HARRIS SEMICONDUCTOR

CA3227, CA3246

High-Frequency NPN Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz

August 1996

Features

- Gain-Bandwidth Product (f_T) . . . . . >3GHz
- Five Transistors on a Common Substrate

Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations - RF/Mixer/Oscillator
- IF Converter
- IF Amplifiers
- Sense Amplifiers
- Synthesizers
- Synchronous Detectors
- Cascade Amplifiers

Description

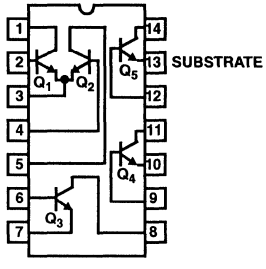
The CA3227 and CA3246 consist of five general purpose silicon NPN transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3GHz, making them useful from DC to 1.5GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

Ordering Information

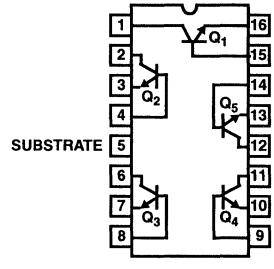
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3227E	-55 to 125	16 Ld PDIP	E16.3
CA3227M (3227)	-55 to 125	16 Ld SOIC	M16.15
CA3227M96 (3227)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3246E	-55 to 125	14 Ld PDIP	E14.3
CA3246M (3246)	-55 to 125	14 Ld SOIC	M14.15
CA3246M96 (3246)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinouts

CA3246
(PDIP, SOIC)
TOP VIEW



CA3227
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1345.3**

Absolute Maximum Ratings

Collector-to-Emitter Voltage (V_{CEO}) 8V
Collector-to-Base Voltage (V_{CBO}) 12V
Collector-to-Substrate Voltage (V_{CIO}, Note 1) 20V
Collector Current (I_C) 20mA

Operating Conditions

Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
14 Ld PDIP Package	100
14 Ld SOIC Package	185
16 Ld PDIP Package	90
16 Ld SOIC Package	175

Maximum Power Dissipation (Any One Transistor) 85mW
Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (Terminal 5 (CA3227) and Terminal 13 (CA3246)) must be connected to the most negative point in the external circuit to maintain isolation be tween transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25°C$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS FOR EACH TRANSISTOR							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$		12	20	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$		8	10	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{C1} = 10\mu A$, $I_B = 0$, $I_E = 0$		20	-	-	V
Emitter-Cutoff-Current (Note 3)	I_{EBO}	$V_{EB} = 4.5V$, $I_C = 0$		-	-	10	µA
Collector-Cutoff-Current	I_{CEO}	$V_{CE} = 5V$, $I_B = 0$		-	-	1	µA
Collector-Cutoff-Current	I_{CBO}	$V_{CB} = 8V$, $I_E = 0$		-	-	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 6V$	$I_C = 10mA$	-	110	-	
			$I_C = 1mA$	40	150	-	
			$I_C = 0.1mA$	-	150	-	
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6V$	$I_C = 1mA$	0.62	0.71	0.82	V
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	$I_C = 10mA$, $I_B = 1mA$		-	0.13	0.50	V
Base-to-Emitter Saturation Voltage	$V_{BE\ SAT}$	$I_C = 10mA$, $I_B = 1mA$		0.74	-	0.94	V

NOTES:

3. On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the h_{FE}. Hence, the use of I_{EBO} rather than $V_{(BR)EBO}$. These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.

Electrical Specifications

$T_A = 25^oC$, 200MHz, Common Emitter, Typical Values Intended Only for Design Guidance

PARAMETER	SYMBOL		TEST CONDITION	TYPICAL VALUES	UNITS
DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR					
Input Admittance	Y_{11}	b_{11}	I_C = 1mA, V_{CE} = 5V	4	mS
		g_{11}		0.75	mS
Output Admittance	Y_{22}	b_{22}	I_C = 1mA, V_{CE} = 5V	2.7	mS
		g_{22}		0.13	mS
Forward Transfer Admittance	Y_{21}	Y_{21}	I_C = 1mA, V_{CE} = 5V	29.3	mS
		θ_{21}		-33	Degrees
Reverse Transfer Admittance	Y_{12}	Y_{12}	I_C = 1mA, V_{CE} = 5V	0.38	mS
		θ_{12}		-97	Degrees
Input Admittance	Y_{11}	b_{11}	I_C = 10mA, V_{CE} = 5V	4.8	mS
		g_{11}		2.85	mS
Output Admittance	Y_{22}	b_{22}	I_C = 10mA, V_{CE} = 5V	2.75	mS
		g_{22}		0.9	mS
Forward Transfer Admittance	Y_{21}	Y_{21}	I_C = 10mA, V_{CE} = 5V	95	mS
		θ_{21}		-62	Degrees
Reverse Transfer Admittance	Y_{12}	Y_{12}	I_C = 10mA, V_{CE} = 5V	0.39	mS
		θ_{12}		-97	Degrees
Small Signal Forward Current Transfer Ratio	h_{21}		I_C = 1mA, V_{CE} = 5V	7.1	
			I_C = 10mA, V_{CE} = 5V	17	
TYPICAL CAPACITANCE AT 1MHz, THREE-TERMINAL MEASUREMENT					
Collector-to-Base Capacitance	C_{CB}		V_{CB} = 6V	0.3	pF
Collector-to-Substrate Capacitance	C_{CI}		V_{CI} = 6V	1.6	pF
Collector-to-Emitter Capacitance	C_{CE}		V_{CE} = 6V	0.4	pF
Emitter-to-Base Capacitance	C_{EB}		V_{EB} = 3V	0.75	pF

Spice Model (Spice 2G.6)

.model NPN

+	BF = 2.610E + 02	BR = 4.401E + 00	IS = 6.930E - 16	RB = 130.0E + 00
+	RC = 1.000E + 01	RE = 7.396E - 01	VA = 6.300E + 01	VB = 2.208E + 00
+	IK = 1.000E - 01	ISE = 1.87E - 14	NE = 1.653E + 00	IKR = 1.000E - 02
+	ISC = 9.25E - 14	NC = 1.333E + 00	TF = 1.775E - 11	TR = 1.000E - 09
+	CJS = 1.800E - 12	CJE = 1.010E - 12	PE = 8.350E - 01	ME = 4.460E - 01
+	CJC = 9.100E - 13	PC = 3.850E - 01	MC = 2.740E - 01	KF = 0.000E + 00
+	AF = 1.000E + 00	EF = 1.000E + 00	FC = 5.000E - 01	PJS = 5.410E - 01
+	MJS = 3.530E - 01	RBM = 30.00	RBV = 100	IRB = 0.00

Please Note: No measurements have been made to model the reverse AC operation (tr is an estimation).

Typical Performance Curves

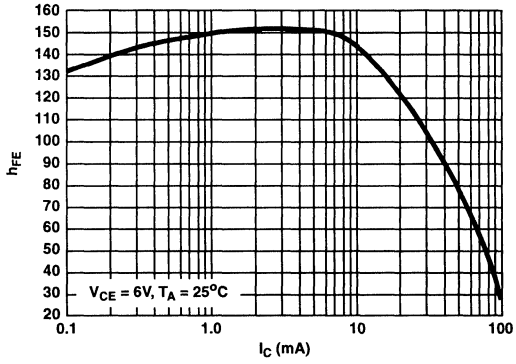


FIGURE 1. h_{FE} vs COLLECTOR CURRENT

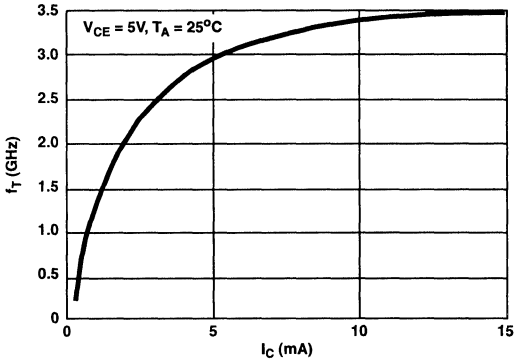


FIGURE 2. f_T vs COLLECTOR CURRENT

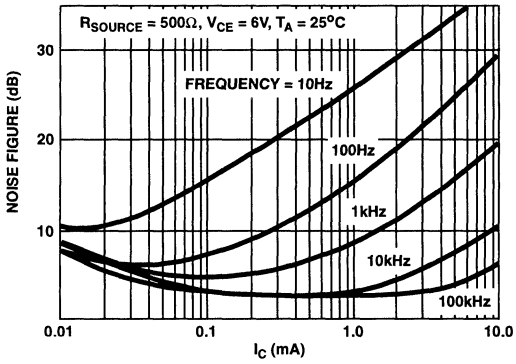


FIGURE 3. NOISE FIGURE vs COLLECTOR CURRENT

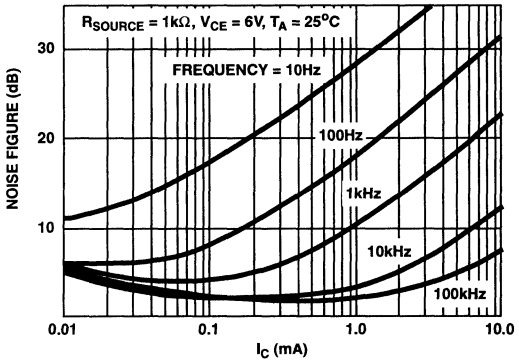


FIGURE 4. NOISE FIGURE vs COLLECTOR CURRENT

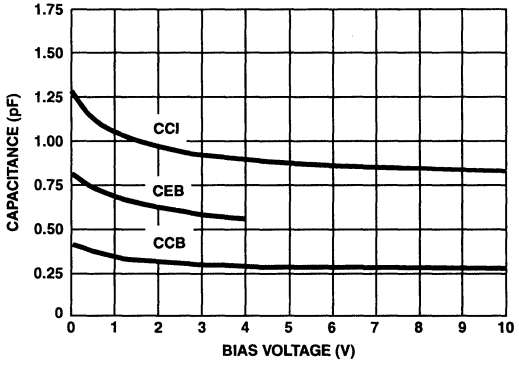


FIGURE 5. CAPACITANCE vs BIAS VOLTAGE

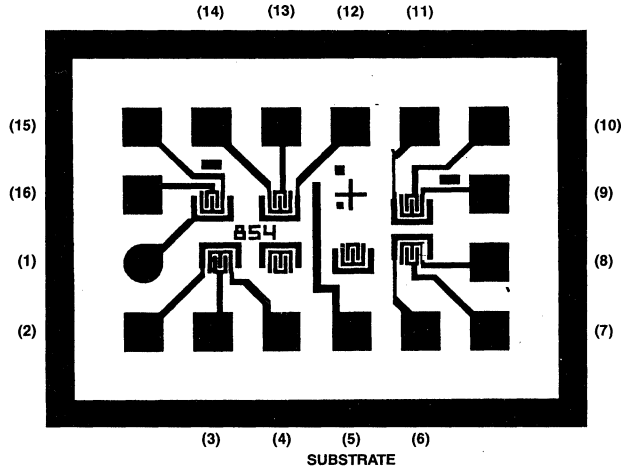
Die Characteristics

DIE DIMENSIONS:

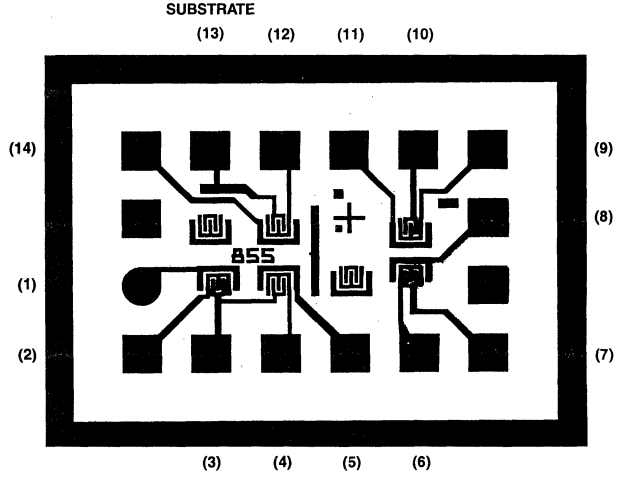
46 mils x 32 mils - CA3227
47 mils x 33 mils - CA3246

Metallization Mask Layout

CA3227



CA3246



HFA3046, HFA3096, HFA3127, HFA3128

August 1996

Ultra High Frequency Transistor Arrays

Features

- NPN Transistor (f_T) 8GHz
- NPN Current Gain (h_{FE})..... 70
- NPN Early Voltage (V_A) 50V
- PNP Transistor (f_T)..... 5.5GHz
- PNP Current Gain (h_{FE})..... 40
- PNP Early Voltage (V_A) 25V
- Noise Figure (50Ω) at 1.0GHz 3.5dB
- Collector-to-Collector Leakage..... <1pA
- Complete Isolation Between Transistors
- Pin Compatible with Industry Standard 3XXX Series Arrays

Applications

- VHF/UHF Amplifiers
- VHF/UHF Mixers
- IF Converters
- Synchronous Detectors

Description

The HFA3046, HFA3096, HFA3127 and the HFA3128 are Ultra High Frequency Transistor Arrays that are fabricated from Harris Semiconductor's complementary bipolar UHF-1 process. Each array consists of five dielectrically isolated transistors on a common monolithic substrate. The NPN transistors exhibit a f_T of 8GHz while the PNP transistors provide a f_T of 5.5GHz. Both types exhibit low noise (3.5dB), making them ideal for high frequency amplifier and mixer applications.

The HFA3046 and HFA3127 are all NPN arrays while the HFA3128 has all PNP transistors. The HFA3096 is an NPN-PNP combination. Access is provided to each of the terminals for the individual transistors for maximum application flexibility. Monolithic construction of these transistor arrays provides close electrical and thermal matching of the five transistors.

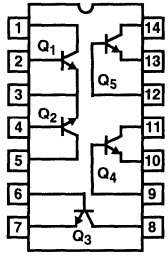
For PSPICE models, please request AnswerFAX document number 663046. Harris also provides an Application Note illustrating the use of these devices as RF amplifiers (request AnswerFAX document 99315).

Ordering Information

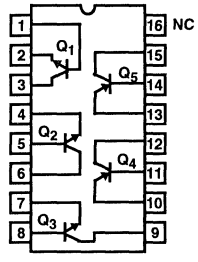
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3046B	-55 to 125	14 Ld SOIC	M14.15
HFA3096B	-55 to 125	16 Ld SOIC	M16.15
HFA3127B	-55 to 125	16 Ld SOIC	M16.15
HFA3128B	-55 to 125	16 Ld SOIC	M16.15

Pinouts

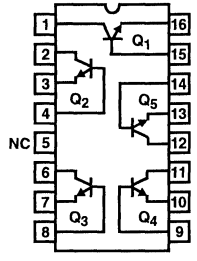
HFA3046
TOP VIEW



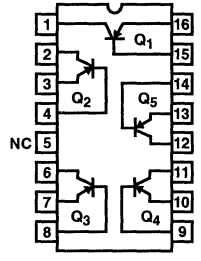
HFA3096
TOP VIEW



HFA3127
TOP VIEW



HFA3128
TOP VIEW



7 ARRAYS AND DIFF. AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **3076.8**

Absolute Maximum Ratings

Collector to Emitter Voltage (Open Base) 8V
Collector to Base Voltage (Shorted Base) 12V
Emitter to Base Voltage (Reverse Bias) 5.5V
Collector Current 15.5mA

Operating Conditions

Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
14 Ld SOIC Package	120
16 Ld SOIC Package	115

Maximum Power Dissipation (Any One Transistor) 0.15W
Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25°C$

PARAMETER	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC NPN CHARACTERISTICS								
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	$I_C = 100\mu A$, $I_E = 0$	12	18	-	12	18	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CEO}$	$I_C = 100\mu A$, $I_B = 0$	8	12	-	8	12	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	$I_C = 100\mu A$, Base Shorted to Emitter	10	20	-	10	20	-	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	5.5	6	-	5.5	6	-	V
Collector-Cutoff-Current, I_{CEO}	$V_{CE} = 6V$, $I_B = 0$	-	2	100	-	2	100	nA
Collector-Cutoff-Current, I_{CBO}	$V_{CB} = 8V$, $I_E = 0$	-	0.1	10	-	0.1	10	nA
Collector-to-Emitter Saturation Voltage, $V_{CE(SAT)}$	$I_C = 10mA$, $I_B = 1mA$	-	0.3	0.5	-	0.3	0.5	V
Base-to-Emitter Voltage, V_{BE}	$I_C = 10mA$	-	0.85	0.95	-	0.85	0.95	V
DC Forward-Current Transfer Ratio, h_{FE}	$I_C = 10mA$ $V_{CE} = 2V$	40	70	-	40	70	-	
Early Voltage, V_A	$I_C = 1mA$, $V_{CE} = 3.5V$	20	50	-	20	50	-	V
Base-to-Emitter Voltage Drift	$I_C = 10mA$	-	-1.5	-	-	-1.5	-	mV/°C
Collector-to-Collector Leakage		-	1	-	-	1	-	pA

Electrical Specifications $T_A = 25°C$

PARAMETER	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC NPN CHARACTERISTICS								
Noise Figure	$f = 1.0GHz$, $V_{CE} = 5V$, $I_C = 5mA$, $Z_S = 50\Omega$	-	3.5	-	-	3.5	-	dB
f_T Current Gain-Bandwidth Product	$I_C = 1mA$, $V_{CE} = 5V$	-	5.5	-	-	5.5	-	GHz
	$I_C = 10mA$, $V_{CE} = 5V$	-	8	-	-	8	-	GHz
Power Gain-Bandwidth Product, f_{MAX}	$I_C = 10mA$, $V_{CE} = 5V$	-	6	-	-	2.5	-	GHz
Base-to-Emitter Capacitance	$V_{BE} = -3V$	-	200	-	-	500	-	fF
Collector-to-Base Capacitance	$V_{CB} = 3V$	-	200	-	-	500	-	fF

Electrical Specifications $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC PNP CHARACTERISTICS								
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	I_C = -100µA, I_E = 0	10	15	-	10	15	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CEO}$	I_C = -100µA, I_B = 0	8	15	-	8	15	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C = -100µA, Base Shorted to Emitter	10	15	-	10	15	-	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	I_E = -10µA, I_C = 0	4.5	5	-	4.5	5	-	V
Collector-Cutoff-Current, I_{CEO}	V_{CE} = -6V, I_B = 0	-	2	100	-	2	100	nA
Collector-Cutoff-Current, I_{CBO}	V_{CB} = -8V, I_E = 0	-	0.1	10	-	0.1	10	nA
Collector-to-Emitter Saturation Voltage, $V_{CE(SAT)}$	I_C = -10mA, I_B = -1mA	-	0.3	0.5	-	0.3	0.5	V
Base-to-Emitter Voltage, V_{BE}	I_C = -10mA	-	0.85	0.95	-	0.85	0.95	V
DC Forward-Current Transfer Ratio, h_{FE}	I_C = -10mA, V_{CE} = -2V	20	35	-	20	35	-	
Early Voltage, V_A	I_C = -1mA, V_{CE} = -3.5V	10	25	-	10	25	-	V
Base-to-Emitter Voltage Drift	I_C = -10mA	-	-1.5	-	-	-1.5	-	mV/°C
Collector-to-Collector Leakage		-	1	-	-	1	-	pA

Electrical Specifications $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC PNP CHARACTERISTICS								
Noise Figure	f = 1.0GHz, V_{CE} = -5V, I_C = -5mA, Z_S = 50Ω	-	3.5	-	-	3.5	-	dB
f_T Current Gain-Bandwidth Product	I_C = -1mA, V_{CE} = -5V	-	2	-	-	2	-	GHz
	I_C = -10mA, V_{CE} = -5V	-	5.5	-	-	5.5	-	GHz
Power Gain-Bandwidth Product	I_C = -10mA, V_{CE} = -5V	-	3	-	-	2	-	GHz
Base-to-Emitter Capacitance	V_{BE} = 3V	-	200	-	-	500	-	fF
Collector-to-Base Capacitance	V_{CB} = -3V	-	300	-	-	600	-	fF

Electrical Specifications $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL PAIR MATCHING CHARACTERISTICS FOR THE HFA3046								
Input Offset Voltage	I_C = 10mA, V_{CE} = 5V	-	1.5	5.0	-	1.5	5.0	mV
Input Offset Current	I_C = 10mA, V_{CE} = 5V	-	5	25	-	5	25	µA
Input Offset Voltage TC	I_C = 10mA, V_{CE} = 5V	-	0.5	-	-	0.5	-	µV/°C

S-Parameter and PSPICE model data is available from Harris Sales Offices.

Common Emitter S-Parameters of NPN 3μm x 50μm Transistor

FREQ. (Hz)	$\|S_{11}\|$	PHASE(S_{11})	$\|S_{12}\|$	PHASE(S_{12})	$\|S_{21}\|$	PHASE(S_{21})	$\|S_{22}\|$	PHASE(S_{22})
V_{CE} = 5V and I_C = 5mA								
1.0E+08	0.83	-11.78	1.41E-02	78.88	11.07	168.57	0.97	-11.05
2.0E+08	0.79	-22.82	2.69E-02	68.63	10.51	157.89	0.93	-21.35
3.0E+08	0.73	-32.64	3.75E-02	59.58	9.75	148.44	0.86	-30.44
4.0E+08	0.67	-41.08	4.57E-02	51.90	8.91	140.36	0.79	-38.16
5.0E+08	0.61	-48.23	5.19E-02	45.50	8.10	133.56	0.73	-44.59
6.0E+08	0.55	-54.27	5.65E-02	40.21	7.35	127.88	0.67	-49.93
7.0E+08	0.50	-59.41	6.00E-02	35.82	6.69	123.10	0.62	-54.37
8.0E+08	0.46	-63.81	6.27E-02	32.15	6.11	119.04	0.57	-58.10
9.0E+08	0.42	-67.63	6.47E-02	29.07	5.61	115.57	0.53	-61.25
1.0E+09	0.39	-70.98	6.63E-02	26.45	5.17	112.55	0.50	-63.96
1.1E+09	0.36	-73.95	6.75E-02	24.19	4.79	109.91	0.47	-66.31
1.2E+09	0.34	-76.62	6.85E-02	22.24	4.45	107.57	0.45	-68.37
1.3E+09	0.32	-79.04	6.93E-02	20.53	4.15	105.47	0.43	-70.19
1.4E+09	0.30	-81.25	7.00E-02	19.02	3.89	103.57	0.41	-71.83
1.5E+09	0.28	-83.28	7.05E-02	17.69	3.66	101.84	0.40	-73.31
1.6E+09	0.27	-85.17	7.10E-02	16.49	3.45	100.26	0.39	-74.66
1.7E+09	0.25	-86.92	7.13E-02	15.41	3.27	98.79	0.38	-75.90
1.8E+09	0.24	-88.57	7.17E-02	14.43	3.10	97.43	0.37	-77.05
1.9E+09	0.23	-90.12	7.19E-02	13.54	2.94	96.15	0.36	-78.12
2.0E+09	0.22	-91.59	7.21E-02	12.73	2.80	94.95	0.35	-79.13
2.1E+09	0.21	-92.98	7.23E-02	11.98	2.68	93.81	0.35	-80.09
2.2E+09	0.20	-94.30	7.25E-02	11.29	2.56	92.73	0.34	-80.99
2.3E+09	0.20	-95.57	7.27E-02	10.64	2.45	91.70	0.34	-81.85
2.4E+09	0.19	-96.78	7.28E-02	10.05	2.35	90.72	0.33	-82.68
2.5E+09	0.18	-97.93	7.29E-02	9.49	2.26	89.78	0.33	-83.47
2.6E+09	0.18	-99.05	7.30E-02	8.96	2.18	88.87	0.33	-84.23
2.7E+09	0.17	-100.12	7.31E-02	8.47	2.10	88.00	0.33	-84.97
2.8E+09	0.17	-101.15	7.31E-02	8.01	2.02	87.15	0.33	-85.68
2.9E+09	0.16	-102.15	7.32E-02	7.57	1.96	86.33	0.33	-86.37
3.0E+09	0.16	-103.11	7.32E-02	7.16	1.89	85.54	0.33	-87.05
V_{CE} = 5V and I_C = 10mA								
1.0E+08	0.72	-16.43	1.27E-02	75.41	15.12	165.22	0.95	-14.26
2.0E+08	0.67	-31.26	2.34E-02	62.89	13.90	152.04	0.88	-26.95
3.0E+08	0.60	-43.76	3.13E-02	52.58	12.39	141.18	0.79	-37.31
4.0E+08	0.53	-54.00	3.68E-02	44.50	10.92	132.57	0.70	-45.45
5.0E+08	0.47	-62.38	4.05E-02	38.23	9.62	125.78	0.63	-51.77
6.0E+08	0.42	-69.35	4.31E-02	33.34	8.53	120.37	0.57	-56.72
7.0E+08	0.37	-75.26	4.49E-02	29.47	7.62	116.00	0.51	-60.65
8.0E+08	0.34	-80.36	4.63E-02	26.37	6.86	112.39	0.47	-63.85
9.0E+08	0.31	-84.84	4.72E-02	23.84	6.22	109.36	0.44	-66.49
1.0E+09	0.29	-88.83	4.80E-02	21.75	5.69	106.77	0.41	-68.71

Common Emitter S-Parameters of NPN 3μm x 50μm Transistor (Continued)

FREQ. (Hz)	$\|S_{11}\|$	PHASE(S_{11})	$\|S_{12}\|$	PHASE(S_{12})	$\|S_{21}\|$	PHASE(S_{21})	$\|S_{22}\|$	PHASE(S_{22})
1.1E+09	0.27	-92.44	4.86E-02	20.00	5.23	104.51	0.39	-70.62
1.2E+09	0.25	-95.73	4.90E-02	18.52	4.83	102.53	0.37	-72.28
1.3E+09	0.24	-98.75	4.94E-02	17.25	4.49	100.75	0.35	-73.76
1.4E+09	0.22	-101.55	4.97E-02	16.15	4.19	99.16	0.34	-75.08
1.5E+09	0.21	-104.15	4.99E-02	15.19	3.93	97.70	0.33	-76.28
1.6E+09	0.20	-106.57	5.01E-02	14.34	3.70	96.36	0.32	-77.38
1.7E+09	0.20	-108.85	5.03E-02	13.60	3.49	95.12	0.31	-78.41
1.8E+09	0.19	-110.98	5.05E-02	12.94	3.30	93.96	0.31	-79.37
1.9E+09	0.18	-113.00	5.06E-02	12.34	3.13	92.87	0.30	-80.27
2.0E+09	0.18	-114.90	5.07E-02	11.81	2.98	91.85	0.30	-81.13
2.1E+09	0.17	-116.69	5.08E-02	11.33	2.84	90.87	0.30	-81.95
2.2E+09	0.17	-118.39	5.09E-02	10.89	2.72	89.94	0.29	-82.74
2.3E+09	0.16	-120.01	5.10E-02	10.50	2.60	89.06	0.29	-83.50
2.4E+09	0.16	-121.54	5.11E-02	10.13	2.49	88.21	0.29	-84.24
2.5E+09	0.16	-122.99	5.12E-02	9.80	2.39	87.39	0.29	-84.95
2.6E+09	0.15	-124.37	5.12E-02	9.49	2.30	86.60	0.29	-85.64
2.7E+09	0.15	-125.69	5.13E-02	9.21	2.22	85.83	0.29	-86.32
2.8E+09	0.15	-126.94	5.13E-02	8.95	2.14	85.09	0.29	-86.98
2.9E+09	0.15	-128.14	5.14E-02	8.71	2.06	84.36	0.29	-87.62
3.0E+09	0.14	-129.27	5.15E-02	8.49	1.99	83.66	0.29	-88.25

Common Emitter S-Parameters of PNP 3μm² x 50μm² Transistor

FREQ. (Hz)	$\|S_{11}\|$	PHASE(S_{11})	$\|S_{21}\|$	PHASE(S_{21})	$\|S_{12}\|$	PHASE(S_{12})	$\|S_{22}\|$	PHASE(S_{22})
V_{CE} = -5V and I_C = -5mA								
1.0E+08	0.72	-16.65	10.11	166.77	1.66E-02	77.18	0.96	-10.76
2.0E+08	0.68	-32.12	9.44	154.69	3.10E-02	65.94	0.90	-20.38
3.0E+08	0.62	-45.73	8.57	144.40	4.23E-02	56.39	0.82	-28.25
4.0E+08	0.57	-57.39	7.68	135.95	5.05E-02	48.66	0.74	-34.31
5.0E+08	0.52	-67.32	6.86	129.11	5.64E-02	42.52	0.67	-38.81
6.0E+08	0.47	-75.83	6.14	123.55	6.07E-02	37.66	0.61	-42.10
7.0E+08	0.43	-83.18	5.53	118.98	6.37E-02	33.79	0.55	-44.47
8.0E+08	0.40	-89.60	5.01	115.17	6.60E-02	30.67	0.51	-46.15
9.0E+08	0.38	-95.26	4.56	111.94	6.77E-02	28.14	0.47	-47.33
1.0E+09	0.36	-100.29	4.18	109.17	6.91E-02	26.06	0.44	-48.15
1.1E+09	0.34	-104.80	3.86	106.76	7.01E-02	24.33	0.41	-48.69
1.2E+09	0.33	-108.86	3.58	104.63	7.09E-02	22.89	0.39	-49.05
1.3E+09	0.32	-112.53	3.33	102.72	7.16E-02	21.67	0.37	-49.26
1.4E+09	0.30	-115.86	3.12	101.01	7.22E-02	20.64	0.36	-49.38
1.5E+09	0.30	-118.90	2.92	99.44	7.27E-02	19.76	0.34	-49.43
1.6E+09	0.29	-121.69	2.75	98.01	7.32E-02	19.00	0.33	-49.44
1.7E+09	0.28	-124.24	2.60	96.68	7.35E-02	18.35	0.32	-49.43
1.8E+09	0.28	-126.59	2.47	95.44	7.39E-02	17.79	0.31	-49.40
1.9E+09	0.27	-128.76	2.34	94.29	7.42E-02	17.30	0.30	-49.38

Common Emitter S-Parameters of PNP 3μm^2 x 50μm^2 Transistor (Continued)

FREQ. (Hz)	$\|S_{11}\|$	PHASE(S_{11})	$\|S_{21}\|$	PHASE(S_{21})	$\|S_{12}\|$	PHASE(S_{12})	$\|S_{22}\|$	PHASE(S_{22})
2.0E+09	0.27	-130.77	2.23	93.19	7.45E-02	16.88	0.30	-49.36
2.1E+09	0.26	-132.63	2.13	92.16	7.47E-02	16.52	0.29	-49.35
2.2E+09	0.26	-134.35	2.04	91.18	7.50E-02	16.20	0.28	-49.35
2.3E+09	0.26	-135.96	1.95	90.24	7.52E-02	15.92	0.28	-49.38
2.4E+09	0.25	-137.46	1.87	89.34	7.55E-02	15.68	0.28	-49.42
2.5E+09	0.25	-138.86	1.80	88.48	7.57E-02	15.48	0.27	-49.49
2.6E+09	0.25	-140.17	1.73	87.65	7.59E-02	15.30	0.27	-49.56
2.7E+09	0.25	-141.39	1.67	86.85	7.61E-02	15.15	0.26	-49.67
2.8E+09	0.25	-142.54	1.61	86.07	7.63E-02	15.01	0.26	-49.81
2.9E+09	0.24	-143.62	1.56	85.31	7.65E-02	14.90	0.26	-49.96
3.0E+09	0.24	-144.64	1.51	84.58	7.67E-02	14.81	0.26	-50.13
V_{CE} = -5V, I_C = -10mA								
1.0E+08	0.58	-23.24	13.03	163.45	1.43E-02	73.38	0.93	-13.46
2.0E+08	0.53	-44.07	11.75	149.11	2.58E-02	60.43	0.85	-24.76
3.0E+08	0.48	-61.50	10.25	137.78	3.38E-02	50.16	0.74	-33.10
4.0E+08	0.43	-75.73	8.88	129.12	3.90E-02	42.49	0.65	-38.83
5.0E+08	0.40	-87.36	7.72	122.49	4.25E-02	36.81	0.58	-42.63
6.0E+08	0.37	-96.94	6.78	117.33	4.48E-02	32.59	0.51	-45.07
7.0E+08	0.35	-104.92	6.01	113.22	4.64E-02	29.39	0.47	-46.60
8.0E+08	0.33	-111.64	5.39	109.85	4.76E-02	26.94	0.43	-47.49
9.0E+08	0.32	-117.36	4.87	107.05	4.85E-02	25.04	0.40	-47.97
1.0E+09	0.31	-122.27	4.44	104.66	4.92E-02	23.55	0.37	-48.18
1.1E+09	0.30	-126.51	4.07	102.59	4.97E-02	22.37	0.35	-48.20
1.2E+09	0.30	-130.21	3.76	100.76	5.02E-02	21.44	0.33	-48.11
1.3E+09	0.29	-133.46	3.49	99.14	5.06E-02	20.70	0.32	-47.95
1.4E+09	0.29	-136.33	3.25	97.67	5.09E-02	20.11	0.31	-47.77
1.5E+09	0.28	-138.89	3.05	96.33	5.12E-02	19.65	0.30	-47.58
1.6E+09	0.28	-141.17	2.87	95.10	5.15E-02	19.29	0.29	-47.39
1.7E+09	0.28	-143.21	2.70	93.96	5.18E-02	19.01	0.28	-47.23
1.8E+09	0.28	-145.06	2.56	92.90	5.21E-02	18.80	0.27	-47.09
1.9E+09	0.27	-146.73	2.43	91.90	5.23E-02	18.65	0.27	-46.98
2.0E+09	0.27	-148.26	2.31	90.95	5.26E-02	18.55	0.26	-46.91
2.1E+09	0.27	-149.65	2.20	90.05	5.28E-02	18.49	0.26	-46.87
2.2E+09	0.27	-150.92	2.10	89.20	5.30E-02	18.46	0.25	-46.87
2.3E+09	0.27	-152.10	2.01	88.37	5.33E-02	18.47	0.25	-46.90
2.4E+09	0.27	-153.18	1.93	87.59	5.35E-02	18.50	0.25	-46.97
2.5E+09	0.27	-154.17	1.86	86.82	5.38E-02	18.55	0.24	-47.07
2.6E+09	0.26	-155.10	1.79	86.09	5.40E-02	18.62	0.24	-47.18
2.7E+09	0.26	-155.96	1.72	85.38	5.42E-02	18.71	0.24	-47.34
2.8E+09	0.26	-156.76	1.66	84.68	5.45E-02	18.80	0.24	-47.55
2.9E+09	0.26	-157.51	1.60	84.01	5.47E-02	18.91	0.24	-47.76
3.0E+09	0.26	-158.21	1.55	83.35	5.50E-02	19.03	0.23	-48.00

Typical Performance Curves

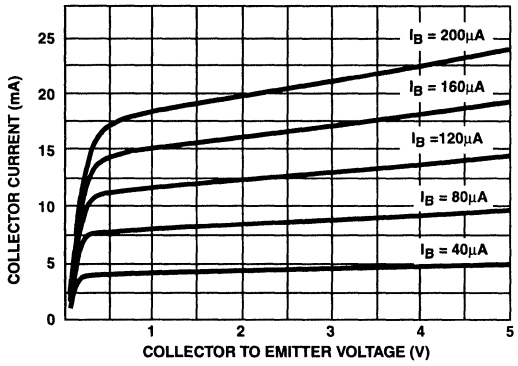


FIGURE 1. NPN COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

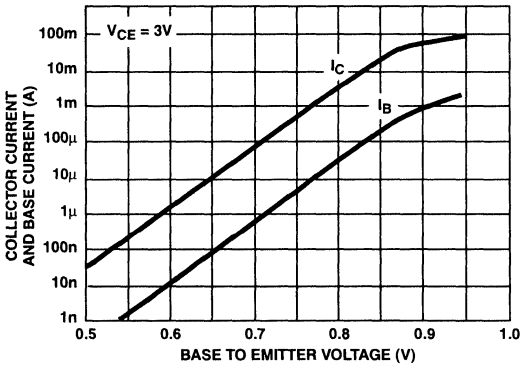


FIGURE 2. NPN COLLECTOR CURRENT AND BASE CURRENT TO EMITTER VOLTAGE

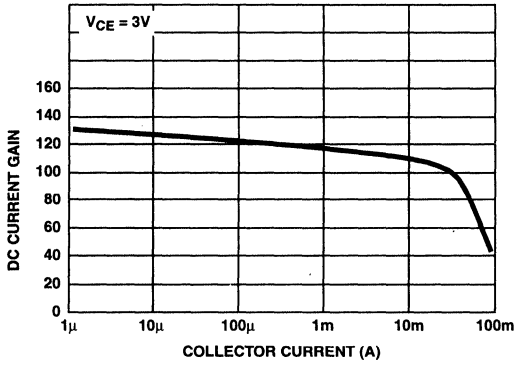


FIGURE 3. NPN DC CURRENT GAIN vs COLLECTOR CURRENT

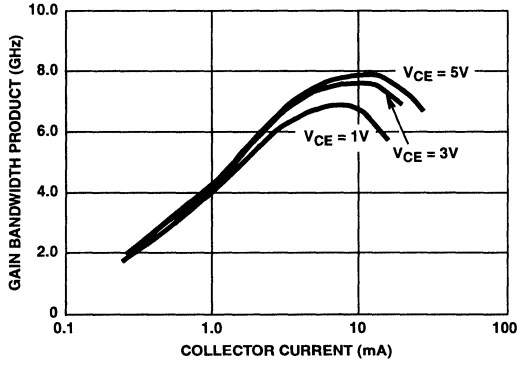


FIGURE 4. NPN GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT (UHF 3 x 50 WITH BOND PADS)

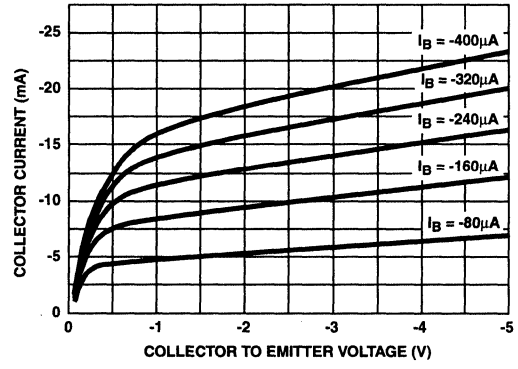


FIGURE 5. PNP COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

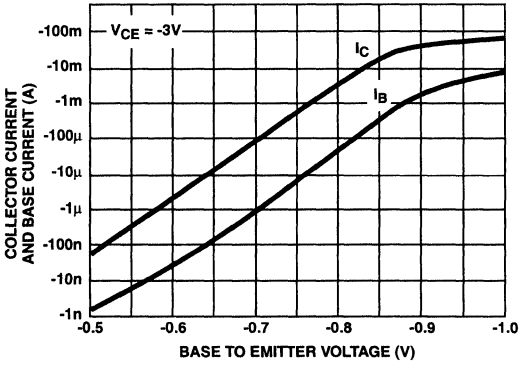


FIGURE 6. PNP COLLECTOR CURRENT AND BASE CURRENT TO EMITTER VOLTAGE

Typical Performance Curves (Continued)

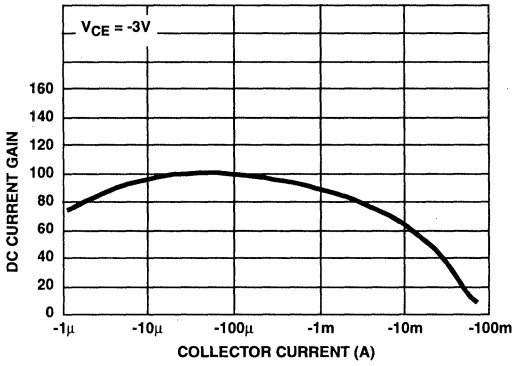


FIGURE 7. PNP DC CURRENT GAIN vs COLLECTOR CURRENT

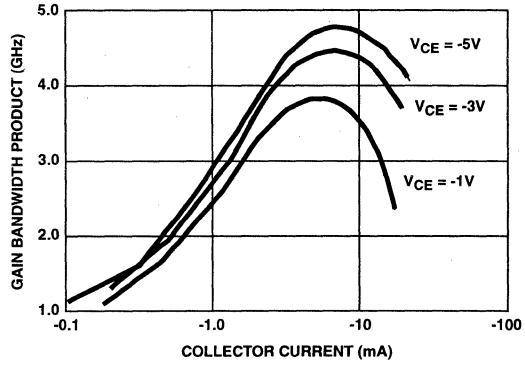


FIGURE 8. PNP GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT (UHF 3 x 50 WITH BOND PADS)

Die Characteristics

PROCESS:
UHF-1

DIE DIMENSIONS:
53 mils x 52 mils x 19 mils
1340µm x 1320µm x 483µm

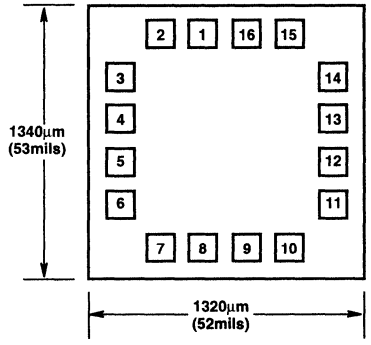
METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

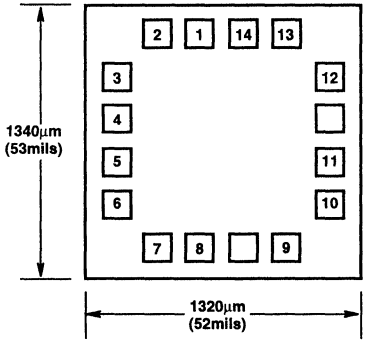
PASSIVATION:
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

Metallization Mask Layout

HFA3096, HFA3127, HFA3128



HFA3046



Pad numbers correspond to SOIC pinout.

HARRIS SEMICONDUCTOR

HFA3101

November 1996

Gilbert Cell UHF Transistor Array

Features

- High Gain Bandwidth Product (f_T) 10GHz
- High Power Gain Bandwidth Product 5GHz
- Current Gain (h_{FE}) 70
- Low Noise Figure (Transistor) 3.5dB
- Excellent h_{FE} and V_{BE} Matching
- Low Collector Leakage Current ..... <0.01nA
- Pin-to-Pin Compatible to UPA101

Applications

- Balanced Mixers
- Multipliers
- Demodulators/Modulators
- Automatic Gain Control Circuits
- Phase Detectors
- Fiber Optic Signal Processing
- Wireless Communication Systems
- Wide Band Amplification Stages
- Radio and Satellite Communications
- High Performance Instrumentation

Description

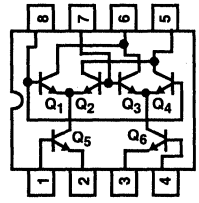
The HFA3101 is an all NPN transistor array configured as a Multiplier Cell. Based on Harris bonded wafer UHF-1 SOI process, this array achieves very high f_T (10GHz) while maintaining excellent h_{FE} and V_{BE} matching characteristics that have been maximized through careful attention to circuit design and layout, making this product ideal for communication circuits. For use in mixer applications, the cell provides high gain and good cancellation of 2nd order distortion terms.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3101B (H3101B)	-40 to 85	8 Ld SOIC	M8.15
HFA3101B96 (H3101B)	-40 to 85	8 Ld SOIC Tape and Reel	M8.15

Pinout

HFA3101
(SOIC)
TOP VIEW



NOTE: Q_5 and Q_6 - 2 Paralleled 3µm x 50µm Transistors
Q_1, Q_2, Q_3, Q_4 - Single 3µm x 50µm Transistors

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3663.3**

Absolute Maximum Ratings

V_{CEO}, Collector to Emitter Voltage 8.0V
V_{CBO}, Collector to Base Voltage 12.0V
V_{EBO}, Emitter to Base Voltage 5.5V
I_C, Collector Current 30mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	185

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25°C$

PARAMETER		TEST CONDITIONS	(NOTE 2) TEST LEVEL	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$, Q_1 thru Q_6		$I_C = 100\mu A$, $I_E = 0$	A	12	18	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CEO}$, Q_5 and Q_6		$I_C = 100\mu A$, $I_B = 0$	A	8	12	-	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$, Q_1 thru Q_6		$I_E = 10\mu A$, $I_C = 0$	A	5.5	6	-	V
Collector Cutoff Current, I_{CBO}, Q_1 thru Q_4		$V_{CB} = 8V$, $I_E = 0$	A	-	0.1	10	nA
Emitter Cutoff Current, I_{EBO}, Q_5 and Q_6		$V_{EB} = 1V$, $I_C = 0$	A	-	-	200	nA
DC Current Gain, h_{FE}, Q_1 thru Q_6		$I_C = 10mA$, $V_{CE} = 3V$	A	40	70	-	
Collector-to-Base Capacitance, C_{CB}	Q_1 thru Q_4	$V_{CB} = 5V$, f = 1MHz	C	-	0.300	-	pF
	Q_5 and Q_6			-	0.600	-	pF
Emitter-to-Base Capacitance, C_{EB}	Q_1 thru Q_4	$V_{EB} = 0$, f = 1MHz	B	-	0.200	-	pF
	Q_5 and Q_6			-	0.400	-	pF
Current Gain-Bandwidth Product, f_T	Q_1 thru Q_4	$I_C = 10mA$, $V_{CE} = 5V$	C	-	10	-	GHz
	Q_5 and Q_6	$I_C = 20mA$, $V_{CE} = 5V$	C	-	10	-	GHz
Power Gain-Bandwidth Product, f_{MAX}	Q_1 thru Q_4	$I_C = 10mA$, $V_{CE} = 5V$	C	-	5	-	GHz
	Q_5 and Q_6	$I_C = 20mA$, $V_{CE} = 5V$	C	-	5	-	GHz
Available Gain at Minimum Noise Figure, G_{NFMIN}, Q_5 and Q_6		$I_C = 5mA$, $V_{CE} = 3V$, f = 0.5GHz	C	-	17.5	-	dB
		$I_C = 5mA$, $V_{CE} = 3V$, f = 1.0GHz	C	-	11.9	-	dB
Minimum Noise Figure, NF_{MIN}, Q_5 and Q_6		$I_C = 5mA$, $V_{CE} = 3V$, f = 0.5GHz	C	-	1.7	-	dB
		$I_C = 5mA$, $V_{CE} = 3V$, f = 1.0GHz	C	-	2.0	-	dB
50Ω Noise Figure, $NF_{50\Omega}$, Q_5 and Q_6		$I_C = 5mA$, $V_{CE} = 3V$, f = 0.5GHz	C	-	2.25	-	dB
		$I_C = 5mA$, $V_{CE} = 3V$, f = 1.0GHz	C	-	2.5	-	dB
DC Current Gain Matching, h_{FE1}/h_{FE2}, Q_1 and Q_2, Q_3 and Q_4, and Q_5 and Q_6		$I_C = 10mA$, $V_{CE} = 3V$	A	0.9	1.0	1.1	
Input Offset Voltage, V_{OS}, (Q_1 and Q_2), (Q_3 and Q_4), (Q_5 and Q_6)		$I_C = 10mA$, $V_{CE} = 3V$	A	-	1.5	5	mV
Input Offset Current, I_C, (Q_1 and Q_2), (Q_3 and Q_4), (Q_5 and Q_6)		$I_C = 10mA$, $V_{CE} = 3V$	A	-	5	25	µA
Input Offset Voltage TC, dV_{OS}/dT, (Q1 and Q2, Q3 and Q_4, Q_5 and Q_6)		$I_C = 10mA$, $V_{CE} = 3V$	C	-	0.5	-	µV/°C
Collector-to-Collector Leakage, $I_{TRENCH-LEAKAGE}$		$\Delta V_{TEST} = 5V$	B	-	0.01	-	nA

NOTE:

2. Test Level: A. Production Tested, B. Typical or Guaranteed Limit Based on Characterization, C. Design Typical for Information Only.

PSPICE Model for a 3μm x 50μm Transistor

.Model NUHFARRY NPN

+ (IS = 1.840E-16	XTI = 3.000E+00	EG = 1.110E+00	VAF = 7.200E+01
+ VAR = 4.500E+00	BF = 1.036E+02	ISE = 1.686E-19	NE = 1.400E+00
+ IKF = 5.400E-02	XTB = 0.000E+00	BR = 1.000E+01	ISC = 1.605E-14
+ NC = 1.800E+00	IKR = 5.400E-02	RC = 1.140E+01	CJC = 3.980E-13
+ MJC = 2.400E-01	VJC = 9.700E-01	FC = 5.000E-01	CJE = 2.400E-13
+ MJE = 5.100E-01	VJE = 8.690E-01	TR = 4.000E-09	TF = 10.51E-12
+ ITF = 3.500E-02	XTF = 2.300E+00	VTF = 3.500E+00	PTF = 0.000E+00
+ XCJC = 9.000E-01	CJS = 1.689E-13	VJS = 9.982E-01	MJS = 0.000E+00
+ RE = 1.848E+00	RB = 5.007E+01	RBM = 1.974E+00	KF = 0.000E+00
+ AF = 1.000E+00)			

Common Emitter S-Parameters of 3μm x 50μm Transistor

FREQ. (Hz)	$\|S_{11}\|$	PHASE(S_{11})	$\|S_{12}\|$	PHASE(S_{12})	$\|S_{21}\|$	PHASE(S_{21})	$\|S_{22}\|$	PHASE(S_{22})
V_{CE} = 5V and I_C = 5mA								
1.0E+08	0.83	-11.78	1.41E-02	78.88	11.07	168.57	0.97	-11.05
2.0E+08	0.79	-22.82	2.69E-02	68.63	10.51	157.89	0.93	-21.35
3.0E+08	0.73	-32.64	3.75E-02	59.58	9.75	148.44	0.86	-30.44
4.0E+08	0.67	-41.08	4.57E-02	51.90	8.91	140.36	0.79	-38.16
5.0E+08	0.61	-48.23	5.19E-02	45.50	8.10	133.56	0.73	-44.59
6.0E+08	0.55	-54.27	5.65E-02	40.21	7.35	127.88	0.67	-49.93
7.0E+08	0.50	-59.41	6.00E-02	35.82	6.69	123.10	0.62	-54.37
8.0E+08	0.46	-63.81	6.27E-02	32.15	6.11	119.04	0.57	-58.10
9.0E+08	0.42	-67.63	6.47E-02	29.07	5.61	115.57	0.53	-61.25
1.0E+09	0.39	-70.98	6.63E-02	26.45	5.17	112.55	0.50	-63.96
1.1E+09	0.36	-73.95	6.75E-02	24.19	4.79	109.91	0.47	-66.31
1.2E+09	0.34	-76.62	6.85E-02	22.24	4.45	107.57	0.45	-68.37
1.3E+09	0.32	-79.04	6.93E-02	20.53	4.15	105.47	0.43	-70.19
1.4E+09	0.30	-81.25	7.00E-02	19.02	3.89	103.57	0.41	-71.83
1.5E+09	0.28	-83.28	7.05E-02	17.69	3.66	101.84	0.40	-73.31
1.6E+09	0.27	-85.17	7.10E-02	16.49	3.45	100.26	0.39	-74.66
1.7E+09	0.25	-86.92	7.13E-02	15.41	3.27	98.79	0.38	-75.90
1.8E+09	0.24	-88.57	7.17E-02	14.43	3.10	97.43	0.37	-77.05
1.9E+09	0.23	-90.12	7.19E-02	13.54	2.94	96.15	0.36	-78.12
2.0E+09	0.22	-91.59	7.21E-02	12.73	2.80	94.95	0.35	-79.13
2.1E+09	0.21	-92.98	7.23E-02	11.98	2.68	93.81	0.35	-80.09
2.2E+09	0.20	-94.30	7.25E-02	11.29	2.56	92.73	0.34	-80.99
2.3E+09	0.20	-95.57	7.27E-02	10.64	2.45	91.70	0.34	-81.85
2.4E+09	0.19	-96.78	7.28E-02	10.05	2.35	90.72	0.33	-82.68
2.5E+09	0.18	-97.93	7.29E-02	9.49	2.26	89.78	0.33	-83.47
2.6E+09	0.18	-99.05	7.30E-02	8.96	2.18	88.87	0.33	-84.23

Common Emitter S-Parameters of 3μm x 50μm Transistor (Continued)

FREQ. (Hz)	$\|S_{11}\|$	PHASE(S_{11})	$\|S_{12}\|$	PHASE(S_{12})	$\|S_{21}\|$	PHASE(S_{21})	$\|S_{22}\|$	PHASE(S_{22})
2.7E+09	0.17	-100.12	7.31E-02	8.47	2.10	88.00	0.33	-84.97
2.8E+09	0.17	-101.15	7.31E-02	8.01	2.02	87.15	0.33	-85.68
2.9E+09	0.16	-102.15	7.32E-02	7.57	1.96	86.33	0.33	-86.37
3.0E+09	0.16	-103.11	7.32E-02	7.16	1.89	85.54	0.33	-87.05
V_{CE} = 5V and I_C = 10mA								
1.0E+08	0.72	-16.43	1.27E-02	75.41	15.12	165.22	0.95	-14.26
2.0E+08	0.67	-31.26	2.34E-02	62.89	13.90	152.04	0.88	-26.95
3.0E+08	0.60	-43.76	3.13E-02	52.58	12.39	141.18	0.79	-37.31
4.0E+08	0.53	-54.00	3.68E-02	44.50	10.92	132.57	0.70	-45.45
5.0E+08	0.47	-62.38	4.05E-02	38.23	9.62	125.78	0.63	-51.77
6.0E+08	0.42	-69.35	4.31E-02	33.34	8.53	120.37	0.57	-56.72
7.0E+08	0.37	-75.26	4.49E-02	29.47	7.62	116.00	0.51	-60.65
8.0E+08	0.34	-80.36	4.63E-02	26.37	6.86	112.39	0.47	-63.85
9.0E+08	0.31	-84.84	4.72E-02	23.84	6.22	109.36	0.44	-66.49
1.0E+09	0.29	-88.83	4.80E-02	21.75	5.69	106.77	0.41	-68.71
1.1E+09	0.27	-92.44	4.86E-02	20.00	5.23	104.51	0.39	-70.62
1.2E+09	0.25	-95.73	4.90E-02	18.52	4.83	102.53	0.37	-72.28
1.3E+09	0.24	-98.75	4.94E-02	17.25	4.49	100.75	0.35	-73.76
1.4E+09	0.22	-101.55	4.97E-02	16.15	4.19	99.16	0.34	-75.08
1.5E+09	0.21	-104.15	4.99E-02	15.19	3.93	97.70	0.33	-76.28
1.6E+09	0.20	-106.57	5.01E-02	14.34	3.70	96.36	0.32	-77.38
1.7E+09	0.20	-108.85	5.03E-02	13.60	3.49	95.12	0.31	-78.41
1.8E+09	0.19	-110.98	5.05E-02	12.94	3.30	93.96	0.31	-79.37
1.9E+09	0.18	-113.00	5.06E-02	12.34	3.13	92.87	0.30	-80.27
2.0E+09	0.18	-114.90	5.07E-02	11.81	2.98	91.85	0.30	-81.13
2.1E+09	0.17	-116.69	5.08E-02	11.33	2.84	90.87	0.30	-81.95
2.2E+09	0.17	-118.39	5.09E-02	10.89	2.72	89.94	0.29	-82.74
2.3E+09	0.16	-120.01	5.10E-02	10.50	2.60	89.06	0.29	-83.50
2.4E+09	0.16	-121.54	5.11E-02	10.13	2.49	88.21	0.29	-84.24
2.5E+09	0.16	-122.99	5.12E-02	9.80	2.39	87.39	0.29	-84.95
2.6E+09	0.15	-124.37	5.12E-02	9.49	2.30	86.60	0.29	-85.64
2.7E+09	0.15	-125.69	5.13E-02	9.21	2.22	85.83	0.29	-86.32
2.8E+09	0.15	-126.94	5.13E-02	8.95	2.14	85.09	0.29	-86.98
2.9E+09	0.15	-128.14	5.14E-02	8.71	2.06	84.36	0.29	-87.62
3.0E+09	0.14	-129.27	5.15E-02	8.49	1.99	83.66	0.29	-88.25

Application Information

The HFA3101 array is a very versatile RF Building block. It has been carefully laid out to improve its matching properties, bringing the distortion due to area mismatches, thermal distribution, betas and ohmic resistances to a minimum.

The cell is equivalent to two differential stages built as two "variable transconductance multipliers" in parallel, with their outputs cross coupled. This configuration is well known in the industry as a Gilbert Cell which enables a four quadrant multiplication operation.

Due to the input dynamic range restrictions for the input levels at the upper quad transistors and lower tail transistors, the HFA3101 cell has restricted use as a linear four quadrant multiplier. However, its configuration is well suited for uses where its linear response is limited to one of the inputs only, as in modulators or mixer circuit applications. Examples of these circuits are up converters, down converters, frequency doublers and frequency/phase detectors.

Although linearization is still an issue for the lower pair input, emitter degeneration can be used to improve the dynamic range and consequent linearity. The HFA3101 has the lower pair emitters brought to external pins for this purpose.

In modulators applications, the upper quad transistors are used in a switching mode where the pairs Q_1/Q_2 and Q_3/Q_4 act as non saturating high speed switches. These switches are controlled by the signal often referred as the carrier input. The signal driving the lower pair Q_5/Q_6 is commonly used as the modulating input. This signal can be linearly transferred to the output by either the use of low signal levels (Well below the thermal voltage of 26mV) or by the use of emitter degeneration. The chopped waveform appearing at the output of the upper pair (Q_1 to Q_4) resembles a signal that is multiplied by +1 or -1 at every half cycle of the switching waveform.

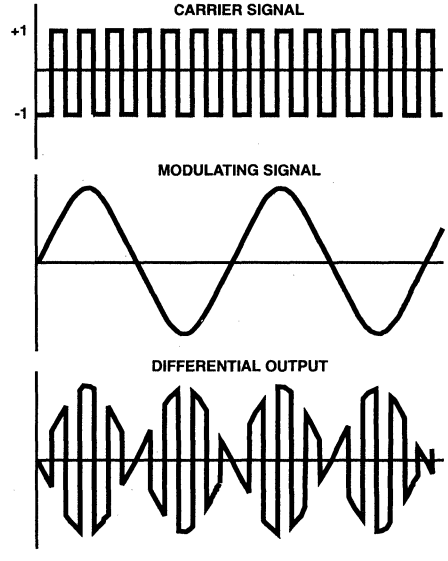


FIGURE 1. TYPICAL MODULATOR SIGNALS

Figure 1 shows the typical input waveforms where the frequency of the carrier is higher than the modulating signal. The output waveform shows a typical suppressed carrier output of an up converter or an AM signal generator.

Carrier suppression capability is a property of the well known Balanced modulator in which the output must be zero when one or the other input (carrier or modulating signal) is equal to zero. however, at very high frequencies, high frequency mismatches and AC offsets are always present and the suppression capability is often degraded causing carrier and modulating feedthrough to be present.

Being a frequency translation circuit, the balanced modulator has the properties of translating the modulating frequency (ω_M) to the carrier frequency (ω_C), generating the two side bands $\omega_U = \omega_C + \omega_M$ and $\omega_L = \omega_C - \omega_M$. Figure 2 shows some translating schemes being used by balanced mixers.

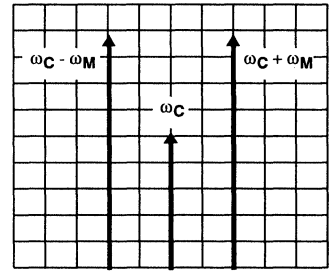


FIGURE 2A. UP CONVERSION OR SUPPRESSED CARRIER AM

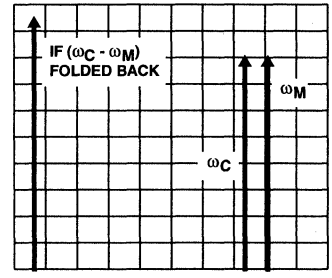


FIGURE 2B. DOWN CONVERSION

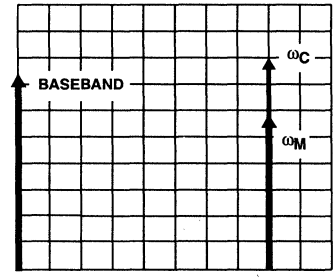


FIGURE 2C. ZERO IF OR DIRECT DOWN CONVERSION

FIGURE 2. MODULATOR FREQUENCY SPECTRUM

The use of the HFA3101 as modulators has several advantages when compared to its counterpart, the diode double-balanced mixer, in which it is required to receive enough energy to drive the diodes into a switching mode and has also some requirements depending on the frequency range desired, of different transformers to suit specific frequency responses. The HFA3101 requires very low driving capabilities for its carrier input and its frequency response is limited by the F_T of the devices, the design and the layout techniques being utilized.

Up conversion uses, for UHF transmitters for example, can be performed by injecting a modulating input in the range of 45MHz to 130MHz that carries the information often called IF (Intermediate frequency) for up conversion (The IF signal has been previously modulated by some modulation scheme from a baseband signal of audio or digital information) and by injecting the signal of a local oscillator of a much higher frequency range from 600MHz to 1.2GHz into the carrier input. Using the example of a 850MHz carrier input and a 70MHz IF, the output spectrum will contain a upper side band of 920MHz, a lower side band of 780MHz and some of the carrier (850MHz) and IF (70MHz) feedthrough. A Band pass filter at the output can attenuate the undesirable signals and the 920MHz signal can be routed to a transmitter RF power amplifier.

Down conversion, as the name implies, is the process used to translate a higher frequency signal to a lower frequency range conserving the modulation information contained in the higher frequency signal. One very common typical down conversion use for example, is for superheterodyne radio receivers where a translated lower frequency often referred as intermediate frequency (IF) is used for detection or demodulation of the baseband signal. Other application uses include down conversion for special filtering using frequency translation methods.

An oscillator referred as the local oscillator (LO) drives the upper quad transistors of the cell with a frequency called ω_C. The lower pair is driven by the RF signal of frequency ω_M to be translated to a lower frequency IF. The spectrum of the IF output will contain the sum and difference of the frequencies ω_C and ω_M. Notice that the difference can become negative when the frequency of the local oscillator is lower than the incoming frequency and the signal is folded back as in Figure 2.

NOTE: The acronyms RF, IF and LO are often interchanged in the industry depending on the application of the cell as mixers or modulators. The output of the cell also contains multiples of the frequency of the signal being fed to the upper quad pair of transistors because of the switching action equivalent to a square wave multiplication. In practice, however, not only the odd multiples in the case of a symmetrical square wave but some of the even multiples will also appear at the output spectrum due to the nature of the actual switching waveform and high frequency performance. By-products of the form $M^*\omega_C + N^*\omega_M$ with M and N being positive or negative integers are also expected to be present at the output and their levels are carefully examined and minimized by the design. This distortion is considered one of the figures of merit for a mixer application.

The process of frequency doubling is also understood by having the same signal being fed to both modulating and carrier ports. The output frequency will be the sum of ω_C and ω_M which is equivalent to the product of the input frequency by 2 and a zero Hz or DC frequency equivalent to the difference of ω_C and ω_M. Figure 2 also shows one technique in use today where a process of down conversion named zero IF is made by using a local oscillator with a very pure signal frequency equal to the incoming RF frequency signal that contains a baseband (audio or digital signal) modulation. Although complex, the extraction or detection of the signal is straightforward.

Another useful application of the HFA3101 is its use as a high frequency phase detector where the two signals are fed to the carrier and modulation ports and the DC information is extracted from its output. In this case, both ports are utilized in a switching mode or overdrive, such that the process of multiplication takes place in a quasi digital form (2 square waves). One application of a phase detector is frequency or phase demodulation where the FM signal is split before the modulating and carrier ports. The lower input port is always 90 degrees apart from the carrier input signal through a high Q tuned phase shift network. The network, being tuned for a precise 90 degrees shift at a nominal frequency, will set the two signals 90 degrees apart and a quiescent output DC level will be present at the output. When the input signal is frequency modulated, the phase shift of the signal coming from the network will deviate from 90 degrees proportional to the frequency deviation of the FM signal and a DC variation at the output will take place, resembling the demodulated FM signal.

The HFA3101 could also be used for quadrature detection, (I/Q demodulation), AGC control with limited range, low level multiplication to name a few other applications.

Biasing

Various biasing schemes can be employed for use with the HFA3101. Figure 3 shows the most common schemes. The biasing method is a choice of the designer when cost, thermal dependence, voltage overheads and DC balancing properties are taken into consideration.

Figure 3A shows the simplest form of biasing the HFA3101. The current source required for the lower pair is set by the voltage across the resistor R_{BIAS} less a V_{BE} drop of the lower transistor. To increase the overhead, collector resistors are substituted by an RF choke as the upper pair functions as a current source for AC signals. The bases of the upper and lower transistors are biased by R_{B1} and R_{B2} respectively. The voltage drop across the resistor R_2 must be higher than a V_{BE} with an increase sufficient to assure that the collector to base junctions of the lower pair are always reverse biased. Notice that this same voltage also sets the V_{CE} of operation of the lower pair which is important for the optimization of gain. Resistors R_{EE} are nominally zero for applications where the input signals are well below 25mV peak. Resistors R_{EE} are used to increase the linearity of the circuit upon higher level signals. The drop across R_{EE} must be taken into consideration when setting the current source value.

Figure 3B depicts the use of a common resistor sharing the current through the cell which is used for temperature compensation as the lower pair V_{BE} drop at the rate of -2mV/°C.

Figure 3C uses a split supply.

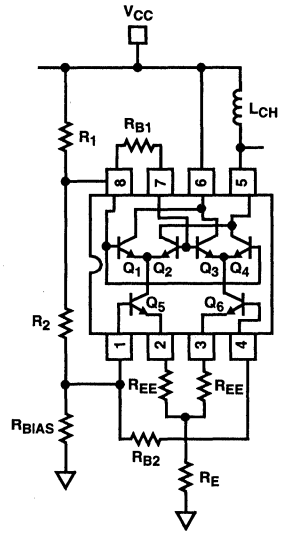


FIGURE 3A.

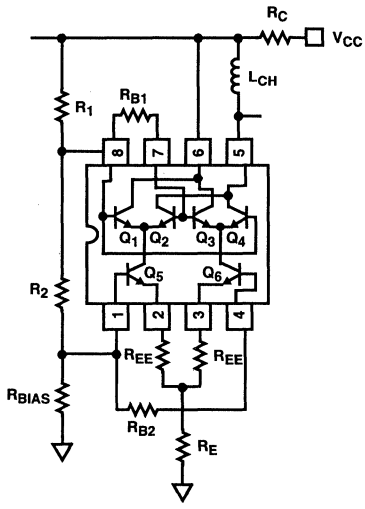


FIGURE 3B.

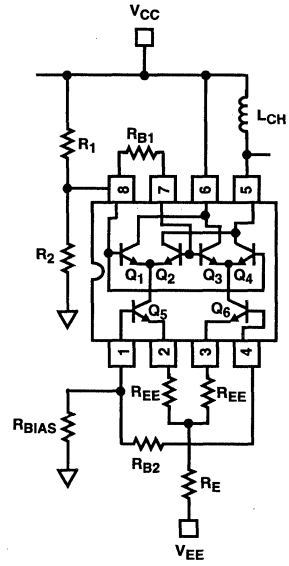


FIGURE 3C.

FIGURE 3.

Design Example: Down Converter Mixer

Figure 4 shows an example of a low cost mixer for cellular applications.

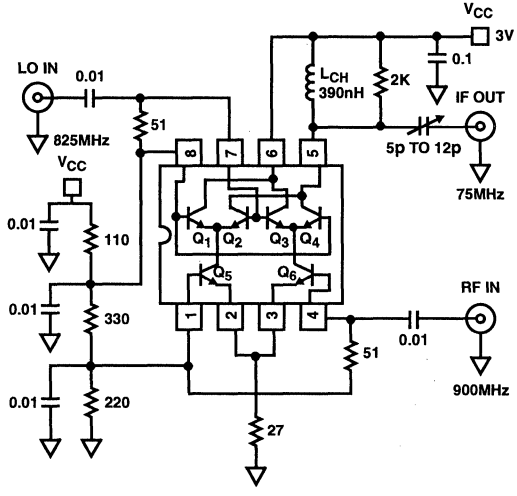


FIGURE 4. 3V DOWN CONVERTER APPLICATION

The design flexibility of the HFA3101 is demonstrated by a low cost, and low voltage mixer application at the 900MHz range. The choice of good quality chip components with their self resonance outside the boundaries of the application are important. The design has been optimized to accommodate the evaluation of the same layout for various quiescent current values and lower supply voltages. The choice of R_E became important for the available overhead and also for maintaining an AC true impedance for high frequency signals. The value of 27Ω has been found to be the optimum minimum for the application. The input impedances of the HFA3101 base input ports are high enough to permit their termination with 50Ω resistors. Notice the AC termination by decoupling the bias circuit through good quality capacitors.

The choice of the bias has been related to the available power supply voltage with the values of R_1, R_2 and R_{BIAS} splitting the voltages for optimum V_{CE} values. For evaluation of the cell quiescent currents, the voltage at the emitter resistor R_E has been recorded.

The gain of the circuit, being a function of the load and the combined emitter resistances at high frequencies have been kept to a maximum by the use of an output match network. The high output impedance of the HFA3101 permits broadband match if so desired at 50Ω (R_L = 50Ω to 2kΩ) as well as with tuned medium Q matching networks (L, T etc.).

Stability

The cell, by its nature, has very high gain and precautions must be taken to account for the combination of signal reflections, gain, layout and package parasitics. The rule of thumb of avoiding reflected waves must be observed. It is important to assure good matching between the mixer stage and its front end. Laboratory measurements have shown some susceptibility for oscillation at the upper quad transistors input. Any LO prefiltering has to be designed such the return loss is maintained within acceptable limits specially at high frequencies. Typical off the shelf filters exhibits very

poor return loss for signals outside the passband. It is suggested that a "pad" or a broadband resistive network be used to interface the LO port with a filter. The inclusion of a parallel 2K resistor in the load decreases the gain slightly which improves the stability factor and also improves the distortion products (output intermodulation or 3rd order intercept). The employment of good RF techniques shall suffice the stability requirements.

Evaluation

The evaluation of the HFA3101 in a mixer configuration is presented in Figures 6 to 11, Table 1 and Table 2. The layout is depicted in Figure 5.

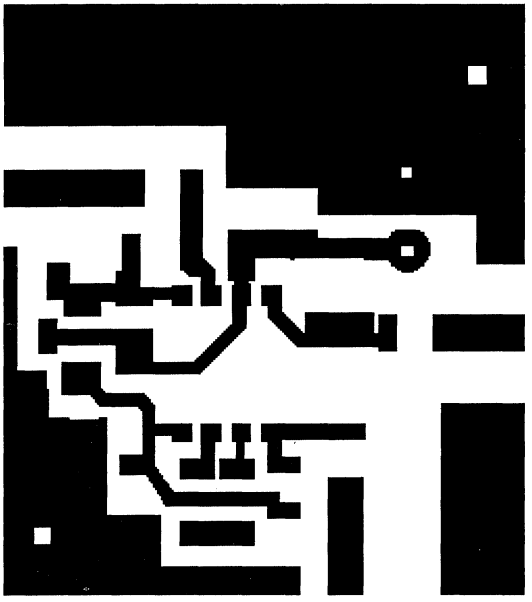


FIGURE 5. UP/DOWN CONVERTER LAYOUT, 400%; MATERIAL G10, 0.031

The output matching network has been designed from data taken at the output port at various test frequencies with the setup as in Table 1. S_{22} characterization is enough to assure the calculation of L, T or transmission line matching networks.

TABLE 1. S_{22} PARAMETERS FOR DOWN CONVERSION, L_{CH} = 10µH

FREQUENCY	RESISTANCE	REACTANCE
10MHz	265Ω	615Ω
45MHz	420Ω	- 735Ω
75MHz	122Ω	- 432Ω
100MHz	67Ω	- 320Ω

TABLE 2. TYPICAL PARAMETERS FOR DOWN CONVERSION, L_{CH} = 10µH

PARAMETER	LO LEVEL	V_{CC} = 3V I_{BIAS} = 8mA
Power Gain	-6dBm	8.5dB
TOI Output	-6dBm	11.5dBm
NF SSB	-6dBm	14.5dB
Power Gain	0dBm	8.6dB
TOI Output	0dBm	11dBm
NF SSB	0dBm	15dB

PARAMETER	LO LEVEL	V_{CC} = 4V I_{BIAS} = 19mA
Power Gain	-6dBm	10dB
TOI Output	-6dBm	13dBm
NF SSB	-6dBm	20dB
Power Gain	0dBm	11dB
TOI Output	0dBm	12.5dBm
NF SSB	0dBm	24dB

TABLE 3. TYPICAL VALUES OF S_{22} FOR THE OUTPUT PORT. L_{CH} = 390nH I_{BIAS} = 8mA (SET UP OF FIGURE 11)

FREQUENCY	RESISTANCE	REACTANCE
300MHz	22Ω	-115Ω
600MHz	7.5Ω	-43Ω
900MHz	5.2Ω	-14Ω
1.1GHz	3.9Ω	0Ω

TABLE 4. TYPICAL VALUES OF S22. L_{CH} = 390nH, I_{BIAS} = 18mA

FREQUENCY	RESISTANCE	REACTANCE
300MHz	23.5Ω	-110Ω
600MHz	10.3Ω	-39Ω
900MHz	8.7Ω	-14Ω
1.1GHz	8Ω	0Ω

Up Converter Example

An application for a up converter as well as a frequency multiplier can be demonstrated using the same layout, with an addition of matching components. The output port S_{22} must be characterized for proper matching procedures and depending on the frequency desired for the output, transmission line transformations can be designed. The return loss of the input ports maintain acceptable values in excess of 1.2GHz which can permit the evaluation of a frequency doubler to 2.4GHz if so desired.

The addition of the resistors R_{EE} can increase considerably the dynamic range of the up converter as demonstrated at Figure 13. The evaluation results depicted in Table 5 have been obtained by a triple stub tuner as a matching network for the output due to the layout constraints. Based on the evaluation results it is clear that the cell requires a higher Bias current for overall performance.

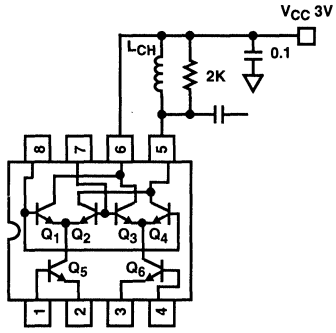


FIGURE 6. OUTPUT PORT S_{22} TEST SET UP

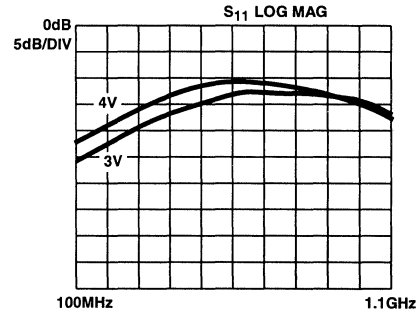


FIGURE 7. LO PORT RETURN LOSS

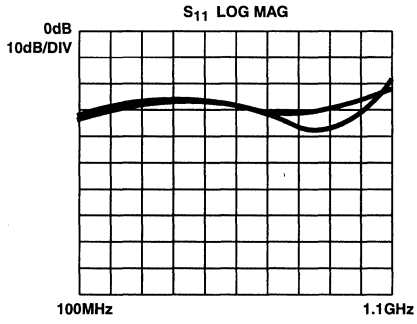


FIGURE 8. RF PORT RETURN LOSS

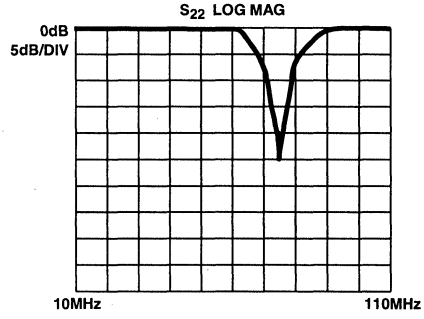


FIGURE 9. IF PORT RETURN LOSS, WITH MATCHING NETWORK

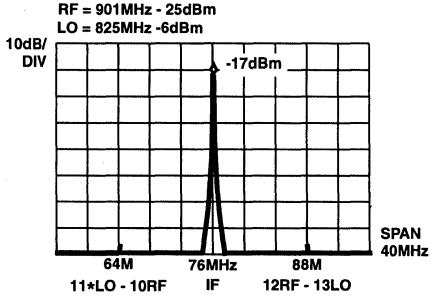


FIGURE 10. TYPICAL IN BAND OUTPUT SPECTRUM, V_{CC} = 3V

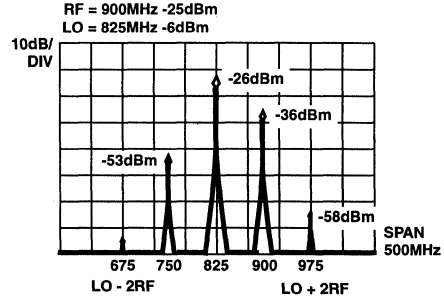


FIGURE 11. TYPICAL OUT OF BAND OUTPUT SPECTRUM

Design Example: Up Converter Mixer

Figure 12 shows an example of an up converter for cellular applications.

Conclusion

The HFA3101 offers the designer a number of choices and different applications as a powerful RF building block. Although isolation is degraded from the theoretical results for the cell due to the unbalanced, nondifferential input schemes being used, a number of advantages can be taken into consideration like cost, flexibility, low power and small outline when deciding for a design.

TABLE 5. TYPICAL PARAMETERS FOR AN UP CONVERTER EXAMPLE

PARAMETER	V_{CC} = 3V I_{BIAS} = 8mA	V_{CC} = 4V I_{BIAS} = 18mA
Power Gain, LO = -6dBm	3dB	5.5dBm
Power Gain, LO = 0dBm	4dB	7.2dB
RF Isolation, LO = 0dBm	15dBc	22dBc
LO Isolation, LO = 0dBm	28dBc	28dBc

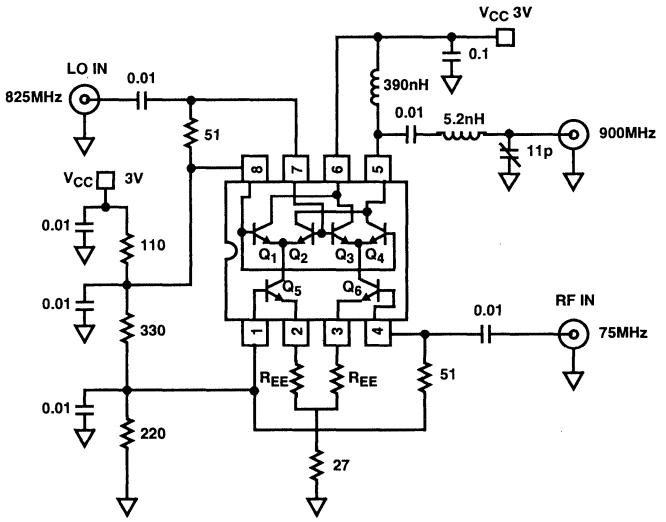


FIGURE 12.

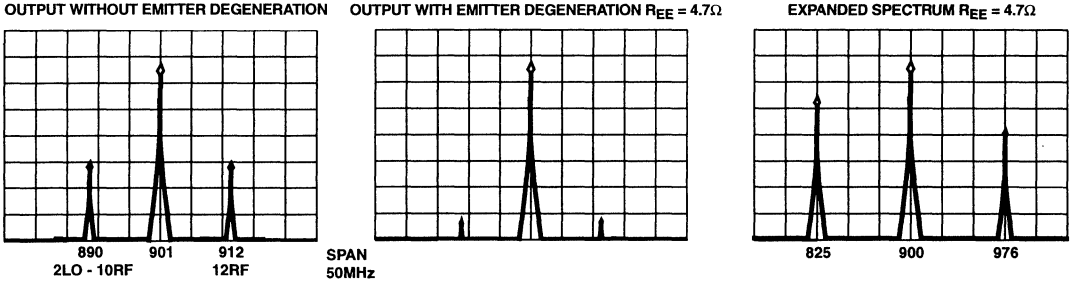


FIGURE 13. TYPICAL SPECTRUM PERFORMANCE

Typical Performance Curves for Transistors

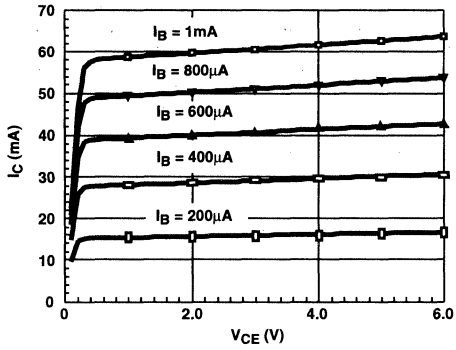


FIGURE 14. I_C vs V_{CE}

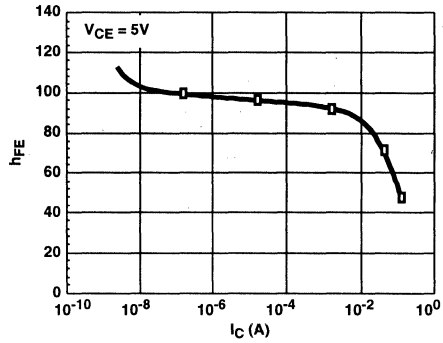


FIGURE 15. H_{FE} vs I_C

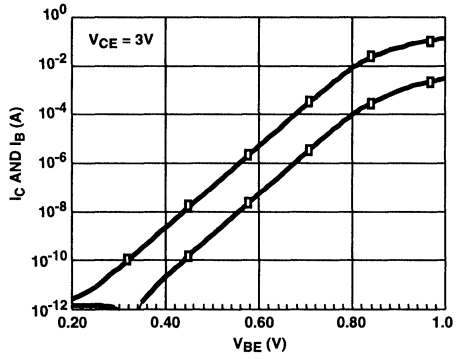


FIGURE 16. GUMMEL PLOT

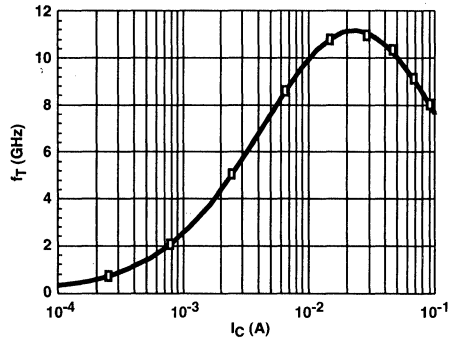


FIGURE 17. f_T vs I_C

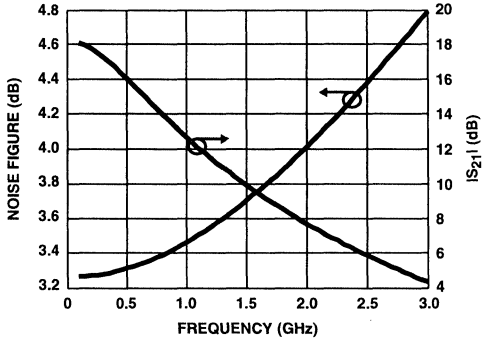


FIGURE 18. GAIN AND NOISE FIGURE vs FREQUENCY

NOTE: Figures 14 through 18 are only for Q_5 and Q_6.

Die Characteristics

PROCESS

UHF-1

DIE DIMENSIONS:

53 mils x 52 mils x 14 mils
1340µm x 1320µm x 355.6µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.5kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

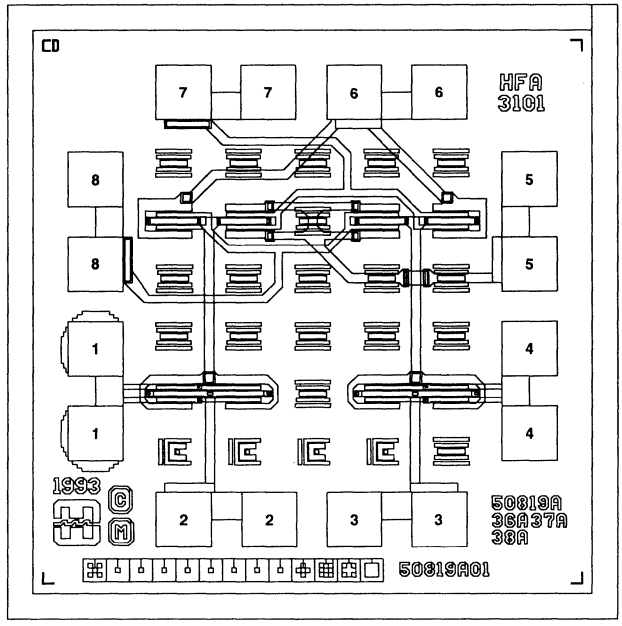
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating

Metallization Mask Layout

HFA3101



HARRIS SEMICONDUCTOR

HFA3102

August 1996

Dual Long-Tailed Pair Transistor Array

Features

- High Gain-Bandwidth Product (f_T) 10GHz
- High Power Gain-Bandwidth Product 5GHz
- High Current Gain (h_{FE}) 70
- Noise Figure (Transistor) 3.5dB
- Low Collector Leakage Current . . . . . <0.01nA
- Excellent h_{FE} and V_{BE} Matching
- Pin-to-Pin to UPA102G

Applications

- Single Balanced Mixers
- Wide Band Amplification Stages
- Differential Amplifiers
- Multipliers
- Automatic Gain Control Circuits
- Frequency Doublers, Tripplers
- Oscillators
- Constant Current Sources
- Wireless Communication Systems
- Radio and Satellite Communications
- Fiber Optic Signal Processing
- High Performance Instrumentation

Description

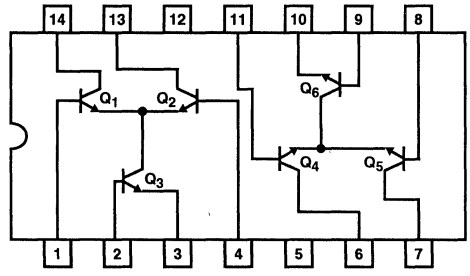
The HFA3102 is an all NPN transistor array configured as dual differential amplifiers with tail transistors. Based on Harris bonded wafer UHF-1 SOI process, this array achieves very high f_T (10GHz) while maintaining excellent h_{FE} and V_{BE} matching characteristics over temperature. Collector leakage currents are maintained to under 0.01nA.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3102B	-40 to 85	14 Ld SOIC	M14.15
HFA3102B96	-40 to 85	14 Ld SOIC Tape and Reel	M14.15

Pinout/Functional Diagram

HFA3102
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1996

File Number **3635.2**

Absolute Maximum Ratings $T_A = 25^oC$

V_{CEO} Collector to Emitter Voltage 8.0V
V_{CBO} Collector to Base Voltage 12.0V
V_{EBO} Emitterr to Base Voltage 12.0V
I_C, Collector Current 30mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOIC Package 125
Maximum Power Dissipation at 75^oC
Any One Transistor 0.25W
Maximum Junction Temperature (Die) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$

SYMBOLS	PARAMETER	TEST CONDITIONS		(NOTE 2) TEST LEVEL	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage (Q_1, Q_2, Q_4, and Q_5)	$I_C = 100\mu A$, $I_E = 0$		A	12	18	-	V
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage (Q_1 thru Q_6)	$I_C = 100\mu A$, $I_B = 0$		A	8	12	-	V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage (Q_3 and Q_6)	$I_E = 50\mu A$, $I_C = 0$		A	5.5	6	-	V
I_{CBO}	Collector Cutoff Current (Q_1, Q_2, Q_4, and Q_5)	$V_{CB} = 5V$, $I_E = 0$		A	-	0.1	10	nA
I_{EBO}	Emitter Cutoff Current (Q_3 and Q_6)	$V_{EB} = 1V$, $I_C = 0$		A	-	-	100	nA
h_{FE}	DC Current Gain (Q_1 thru Q_6)	$I_C = 10mA$, $V_{CE} = 3V$		A	40	70	-	-
C_{CB}	Collector-to-Base Capacitance	$V_{CB} = 5V$, f = 1MHz		B	-	300	-	fF
C_{EB}	Emitter-to-Base Capacitance	$V_{EB} = 0$, f = 1MHz		B	-	200	-	fF
f_T	Current Gain-Bandwidth Product	$I_C = 10mA$, $V_{CE} = 5V$		C	-	10	-	GHz
f_{MAX}	Power Gain-Bandwidth Product	$I_C = 10mA$, $V_{CE} = 5V$		C	-	5	-	GHz
G_{NFMIN}	Available Gain at Minimum Noise Figure	$I_C = 3mA$, $V_{CE} = 3V$	f = 0.5GHz	C	-	17.5	-	dB
			f = 1.0GHz	C	-	12.4	-	dB
NF_{MIN}	Minimum Noise Figure	$I_C = 3mA$, $V_{CE} = 3V$	f = 0.5GHz	C	-	1.8	-	dB
			f = 1.0GHz	C	-	2.1	-	dB
$NF_{50\Omega}$	50Ω Noise Figure	$I_C = 3mA$, $V_{CE} = 3V$	f = 0.5GHz	C	-	3.3	-	dB
			f = 1.0GHz	C	-	3.5	-	dB
h_{FE1}/h_{FE2}	DC Current Gain Matching (Q_1 and Q_2, Q_4 and Q_5)	$I_C = 10mA$, $V_{CE} = 3V$		A	0.9	1.0	1.1	-
V_{OS}	Input Offset Voltage (Q_1 and Q_2), (Q_4 and Q_5)	$I_C = 10mA$, $V_{CE} = 3V$		A	-	1.5	5	mV
I_{OS}	Input Offset Current (Q_1 and Q_2), (Q_4 and Q_5)	$I_C = 10mA$, $V_{CE} = 3V$		A	-	5	25	μA
dV_{OS}/dT	Input Offset Voltage TC (Q_1 and Q_2, Q_4 and Q_5)	$I_C = 10mA$, $V_{CE} = 3V$		C	-	0.5	-	$\mu V/^oC$

Electrical Specifications $T_A = 25^oC$ **(Continued)**

SYMBOLS	PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	ALL GRADES			UNITS
				MIN	TYP	MAX	
$I_{TRENCH-LEAKAGE}$	Collector-to-Collector Leakage (Pin 6, 7, 13, and 14)	$\Delta V_{TEST} = 5V$	B	-	0.01	-	nA

NOTE:

2. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only

PSPICE Model for a Single Transistor

.Model NUHFARRY NPN

+ (IS= 1.840E-16 XTI= 3.000E+00 EG= 1.110E+00 VAF= 7.200E+01

+ VAR= 4.500E+00 BF= 1.036E+02 ISE= 1.686E-19 NE= 1.400E+00

+ IKF= 5.400E-02 XTB= 0.000E+00 BR= 1.000E+01 ISC= 1.605E-14

+ NC= 1.800E+00 IKR= 5.400E-02 RC= 1.140E+01 CJC= 3.980E-13

+ MJC= 2.400E-01 VJC= 9.700E-01 FC= 5.000E-01 CJE= 2.400E-13

+ MJE= 5.100E-01 VJE= 8.690E-01 TR= 4.000E-09 TF= 10.51E-12

+ ITF= 3.500E-02 XTF= 2.300E+00 VTF= 3.500E+00 PTF= 0.000E+00

+ XCJC= 9.000E-01 CJS= 1.689E-13 VJS= 9.982E-01 MJS= 0.000E+00

+ RE= 1.848E+00 RB= 5.007E+01 RBM= 1.974E+00 KF= 0.000E+00

+ AF= 1.000E+00)

Common Emitter S-Parameters

V_{CE} = 5V and I_C = 5mA

FREQ. (Hz)	$\|S_{11}\|$	PHASE(S_{11})	$\|S_{12}\|$	PHASE(S_{12})	$\|S_{21}\|$	PHASE(S_{21})	$\|S_{22}\|$	PHASE(S_{22})
1.0E+08	0.833079	-11.7873	1.418901E-02	78.8805	11.0722	168.576	0.976833	-11.0509
2.0E+08	0.791776	-22.8290	2.695740E-02	68.6355	10.5177	157.897	0.930993	-21.3586
3.0E+08	0.734911	-32.6450	3.750029E-02	59.5861	9.75379	148.443	0.868128	-30.4451
4.0E+08	0.672811	-41.0871	4.572138E-02	51.9018	8.91866	140.361	0.799886	-38.1641
5.0E+08	0.612401	-48.2370	5.194147E-02	45.5043	8.10511	133.569	0.734033	-44.5998
6.0E+08	0.557126	-54.2780	5.659943E-02	40.2112	7.35944	127.882	0.674392	-49.9370
7.0E+08	0.508133	-59.4102	6.009507E-02	35.8226	6.69712	123.102	0.622181	-54.3777
8.0E+08	0.465361	-63.8123	6.274213E-02	32.1594	6.11750	119.047	0.577269	-58.1022
9.0E+08	0.428238	-67.6313	6.477134E-02	29.0743	5.61303	115.571	0.538952	-61.2587
1.0E+09	0.396034	-70.9834	6.634791E-02	26.4506	5.17405	112.556	0.506365	-63.9647
1.1E+09	0.368032	-73.9591	6.758932E-02	24.1974	4.79104	109.913	0.478663	-66.3116
1.2E+09	0.343589	-76.6285	6.857937E-02	22.2441	4.45546	107.570	0.455091	-68.3702
1.3E+09	0.322155	-79.0462	6.937837E-02	20.5358	4.15997	105.472	0.435008	-70.1958
1.4E+09	0.303268	-81.2548	7.003020E-02	19.0293	3.89845	103.576	0.417872	-71.8314
1.5E+09	0.286542	-83.2880	7.056718E-02	17.6908	3.66577	101.849	0.403238	-73.3108
1.6E+09	0.271660	-85.1723	7.101343E-02	16.4930	3.45770	100.262	0.390735	-74.6609
1.7E+09	0.258359	-86.9292	7.138717E-02	15.4143	3.27074	98.7956	0.380056	-75.9030
1.8E+09	0.246420	-88.5759	7.170231E-02	14.4370	3.10197	97.4307	0.370947	-77.0544
1.9E+09	0.235659	-90.1265	7.196964E-02	13.5469	2.94897	96.1533	0.363195	-78.1288
2.0E+09	0.225923	-91.5925	7.219757E-02	12.7319	2.80969	94.9515	0.356623	-79.1377
2.1E+09	0.217085	-92.9836	7.239274E-02	11.9824	2.68243	93.8156	0.351081	-80.0903
2.2E+09	0.209034	-94.3076	7.256046E-02	11.2901	2.56573	92.7373	0.346442	-80.9942
2.3E+09	0.201678	-95.5713	7.270498E-02	10.6480	2.45837	91.7097	0.342599	-81.8557
2.4E+09	0.194939	-96.7803	7.282977E-02	10.0503	2.35928	90.7271	0.339458	-82.6802
2.5E+09	0.188747	-97.9395	7.293764E-02	9.49212	2.26756	89.7844	0.336942	-83.4719
2.6E+09	0.183044	-99.0530	7.303093E-02	8.96908	2.18243	88.8775	0.334982	-84.2347
2.7E+09	0.177780	-100.124	7.311157E-02	8.47753	2.10322	88.0026	0.333518	-84.9716
2.8E+09	0.172909	-101.156	7.318117E-02	8.01430	2.02934	87.1565	0.332499	-85.6853
2.9E+09	0.168394	-102.152	7.324107E-02	7.57661	1.96027	86.3366	0.331879	-86.3781
3.0E+09	0.164200	-103.114	7.329243E-02	7.16204	1.89556	85.5404	0.331620	-87.0518

V_{CE} = 5V and I_C = 10mA

FREQ. (Hz)	$\|S_{11}\|$	PHASE(S_{11})	$\|S_{12}\|$	PHASE(S_{12})	$\|S_{21}\|$	PHASE(S_{21})	$\|S_{22}\|$	PHASE(S_{22})
1.0E+08	0.728106	-16.4319	1.273920E-02	75.4177	15.1273	165.227	0.959692	-14.2688
2.0E+08	0.670836	-31.2669	2.342300E-02	62.8941	13.9061	152.045	0.886232	-26.9507
3.0E+08	0.600268	-43.7663	3.132521E-02	52.5891	12.3970	141.185	0.796016	-37.3172
4.0E+08	0.531768	-54.0028	3.681579E-02	44.5019	10.9257	132.570	0.708892	-45.4503
5.0E+08	0.471795	-62.3880	4.057046E-02	38.2308	9.62995	125.781	0.633146	-51.7704
6.0E+08	0.421506	-69.3569	4.316292E-02	33.3405	8.53559	120.378	0.570209	-56.7206
7.0E+08	0.379961	-75.2612	4.499071E-02	29.4764	7.62375	116.005	0.518803	-60.6598
8.0E+08	0.345693	-80.3608	4.631140E-02	26.3755	6.86423	112.398	0.476987	-63.8540
9.0E+08	0.317301	-84.8420	4.728948E-02	23.8481	6.22797	109.365	0.442915	-66.4948
1.0E+09	0.293608	-88.8381	4.803091E-02	21.7581	5.69057	106.771	0.415044	-68.7193
1.1E+09	0.273680	-92.4452	4.860515E-02	20.0070	5.23257	104.518	0.392146	-70.6269
1.2E+09	0.256782	-95.7336	4.905871E-02	18.5224	4.83873	102.532	0.373261	-72.2899
1.3E+09	0.242344	-98.7555	4.942344E-02	17.2505	4.49716	100.759	0.357640	-73.7620
1.4E+09	0.229918	-101.551	4.972158E-02	16.1506	4.19854	99.1602	0.344698	-75.0832
1.5E+09	0.219152	-104.150	4.996903E-02	15.1915	3.93554	97.7028	0.333974	-76.2840
1.6E+09	0.209767	-106.577	5.017730E-02	14.3490	3.70234	96.3629	0.325102	-77.3877
1.7E+09	0.201539	-108.851	5.035491E-02	13.6040	3.49428	95.1215	0.317789	-78.4122
1.8E+09	0.194288	-110.988	5.050825E-02	12.9411	3.30758	93.9633	0.311800	-79.3715
1.9E+09	0.187867	-113.001	5.064218E-02	12.3482	3.13919	92.8761	0.306940	-80.2768
2.0E+09	0.182157	-114.902	5.076045E-02	11.8151	2.98658	91.8500	0.303051	-81.1365
2.1E+09	0.177056	-116.698	5.086598E-02	11.3338	2.84766	90.8766	0.300003	-81.9578
2.2E+09	0.172484	-118.399	5.096107E-02	10.8974	2.72068	89.9494	0.297686	-82.7460
2.3E+09	0.168370	-120.012	5.104755E-02	10.5001	2.60420	89.0626	0.296007	-83.5057
2.4E+09	0.164656	-121.542	5.112690E-02	10.1373	2.49697	88.2115	0.294889	-84.2405
2.5E+09	0.161293	-122.996	5.120031E-02	9.80479	2.39793	87.3920	0.294266	-84.9533
2.6E+09	0.158239	-124.378	5.126876E-02	9.49919	2.30619	86.6007	0.294081	-85.6466
2.7E+09	0.155458	-125.694	5.133304E-02	9.21750	2.22098	85.8348	0.294285	-86.3223
2.8E+09	0.152919	-126.947	5.139381E-02	8.95716	2.14162	85.0916	0.294836	-86.9822
2.9E+09	0.150595	-128.140	5.145164E-02	8.71595	2.06753	84.3690	0.295696	-87.6275
3.0E+09	0.148463	-129.279	5.150697E-02	8.49194	1.99820	83.6651	0.296834	-88.2595

Typical Performance Curves

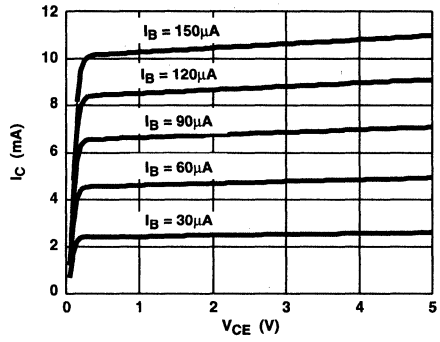


FIGURE 1. I_C vs V_{CE}

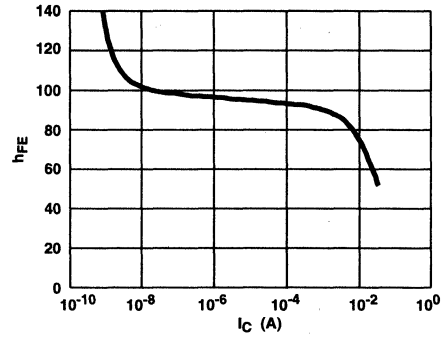


FIGURE 2. h_{FE} vs I_C

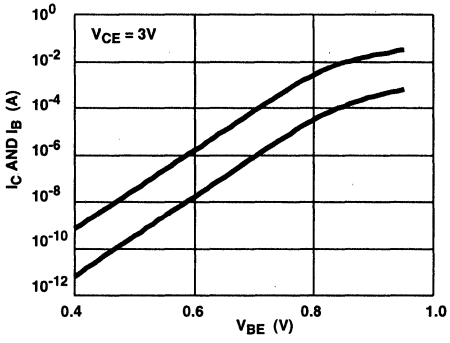


FIGURE 3. GUMMEL PLOT

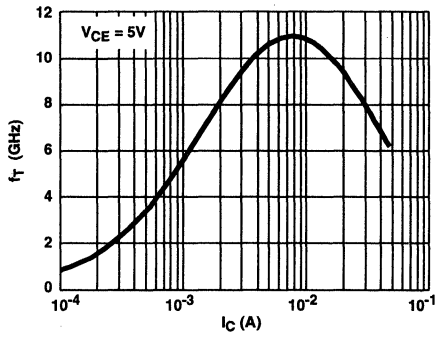


FIGURE 4. f_T vs I_C

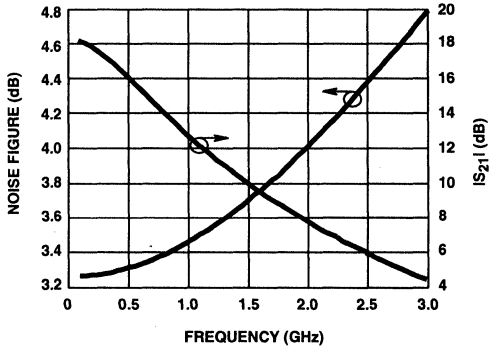


FIGURE 5. GAIN AND NOISE FIGURE vs FREQUENCY

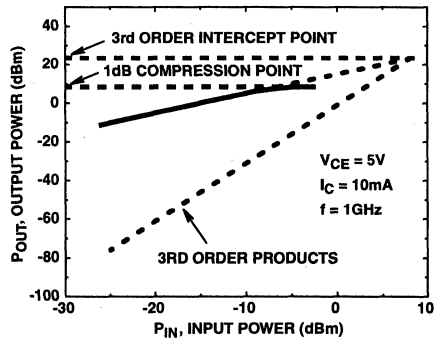


FIGURE 6. P_{1dB} AND 3RD ORDER INTERCEPT

Die Characteristics

PROCESS:

UHF-1

DIE DIMENSIONS:

53 mils x 52 mils x 14 mils
1340µm x 1320µm x 355.6µm

METALIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.5kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

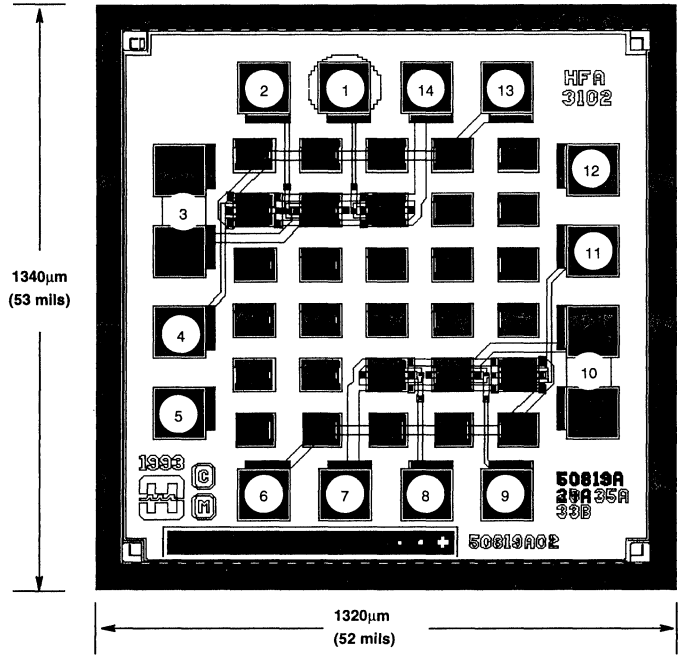
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating

Metallization Mask Layout

HFA3102
TOP VIEW



Pad numbers correspond to the 14 pin SOIC pinout.

LINEAR 8

SPECIAL ANALOG CIRCUITS

HARRIS SEMICONDUCTOR

CA555, CA555C, LM555, LM555C

Timers for Timing Delays and Oscillator Application in Commercial, Industrial and Military Equipment

November 1996

Features

- Accurate Timing From Microseconds Through Hours
- Astable and Monostable Operation
- Adjustable Duty Cycle
- Output Capable of Sourcing or Sinking up to 200mA
- Output Capable of Driving TTL Devices
- Normally ON and OFF Outputs
- High Temperature Stability . . . . . 0.005%/°C
- Directly Interchangeable with SE555, NE555, MC1555, and MC1455

Applications

- Precision Timing
- Sequential Timing
- Time Delay Generation
- Pulse Generation
- Pulse Detector
- Pulse Width and Position Modulation

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA0555E	-55 to 125	8 Ld PDIP	E8.3
CA0555M (555)	-55 to 125	8 Ld SOIC	M8.15
CA0555M96 (555)	-55 to 125	8 Ld SOIC †	M8.15
CA0555T	-55 to 125	8 Pin Metal Can	T8.C
CA0555CE	0 to 70	8 Ld PDIP	E8.3
CA0555CM (555C)	0 to 70	8 Ld SOIC	M8.15
CA0555CM96 (555C)	0 to 70	8 Ld SOIC †	M8.15
CA0555CT	0 to 70	8 Pin Metal Can	T8.C
LM555N	0 to 70	8 Ld PDIP	E8.3
LM555CN	0 to 70	8 Ld PDIP	E8.3

NOTE: † Denotes Tape and Reel

Description

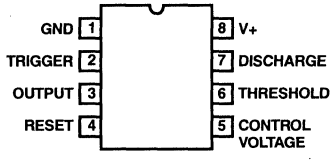
The CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the waveform signal, and the output of these circuits can source or sink up to a 200mA current or drive TTL circuits.

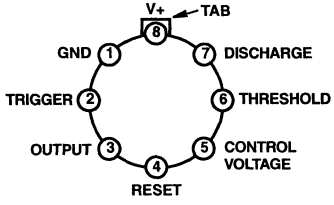
These types are direct replacements for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

Pinouts

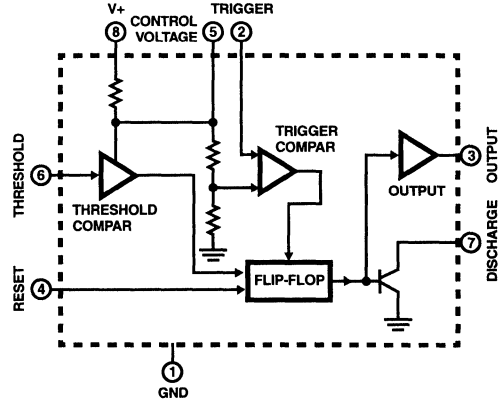
CA555, CA555C (PDIP, SOIC)
LM555, LM555C (PDIP)
TOP VIEW



CA555, CA555C (METAL CAN)
TOP VIEW



Functional Block Diagram



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **834.3**

Absolute Maximum Ratings

DC Supply Voltage 18V

Operating Conditions

Temperature Range
- CA555 . . . . . -55°C to 125°C
- CA555C, LM555, LM555C . . . . . .0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	170	85
PDIP Package	100	N/A
SOIC Package	160	N/A

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = 25°C, V+ = 5V to 15V Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA555, LM555			CA555C, LM555C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC Supply Voltage	V+		4.5	-	18	4.5	-	16	V
DC Supply Current (Low State), (Note 2)	I+	V+ = 5V, $R_L = \infty$	-	3	5	-	3	6	mA
		V+ = 15V, $R_L = \infty$	-	10	12	-	10	15	mA
Threshold Voltage	V_{TH}		-	(2/3)V+	-	-	(2/3)V+	-	V
Trigger Voltage		V+ = 5V	1.45	1.67	1.9	-	1.67	-	V
		V+ = 15V	4.8	5	5.2	-	5	-	V
Trigger Current			-	0.5	-	-	0.5	-	µA
Threshold Current (Note 3)	I_{TH}		-	0.1	0.25	-	0.1	0.25	µA
Reset Voltage			0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			-	0.1	-	-	0.1	-	mA
Control Voltage Level		V+ = 5V	2.9	3.33	3.8	2.6	3.33	4	V
		V+ = 15V	9.6	10	10.4	9	10	11	V
Output Voltage	V_{OL}	V+ = 5V, I_{SINK} = 5mA	-	-	-	-	0.25	0.35	V
Low State		I_{SINK} = 8mA	-	0.1	0.25	-	-	-	V
		V+ = 15V, I_{SINK} = 10mA	-	0.1	0.15	-	0.1	0.25	V
		I_{SINK} = 50mA	-	0.4	0.5	-	0.4	0.75	V
		I_{SINK} = 100mA	-	2.0	2.2	-	2.0	2.5	V
		I_{SINK} = 200mA	-	2.5	-	-	2.5	-	V
Output Voltage	V_{OH}	V+ = 5V, I_{SOURCE} = 100mA	3.0	3.3	-	2.75	3.3	-	V
High State		V+ = 15V, I_{SOURCE} = 100mA	13.0	13.3	-	12.75	13.3	-	V
		I_{SOURCE} = 200mA	-	12.5	-	-	12.5	-	V
Timing Error (Monostable)		R_1, R_2 = 1kΩ to 100kΩ, C = 0.1µF Tested at V+ = 5V, V+ = 15V	-	0.5	2	-	1	-	%
Frequency Drift with Temperature			-	30	100	-	50	-	ppm/°C
Drift with Supply Voltage			-	0.05	0.2	-	0.1	-	%/V

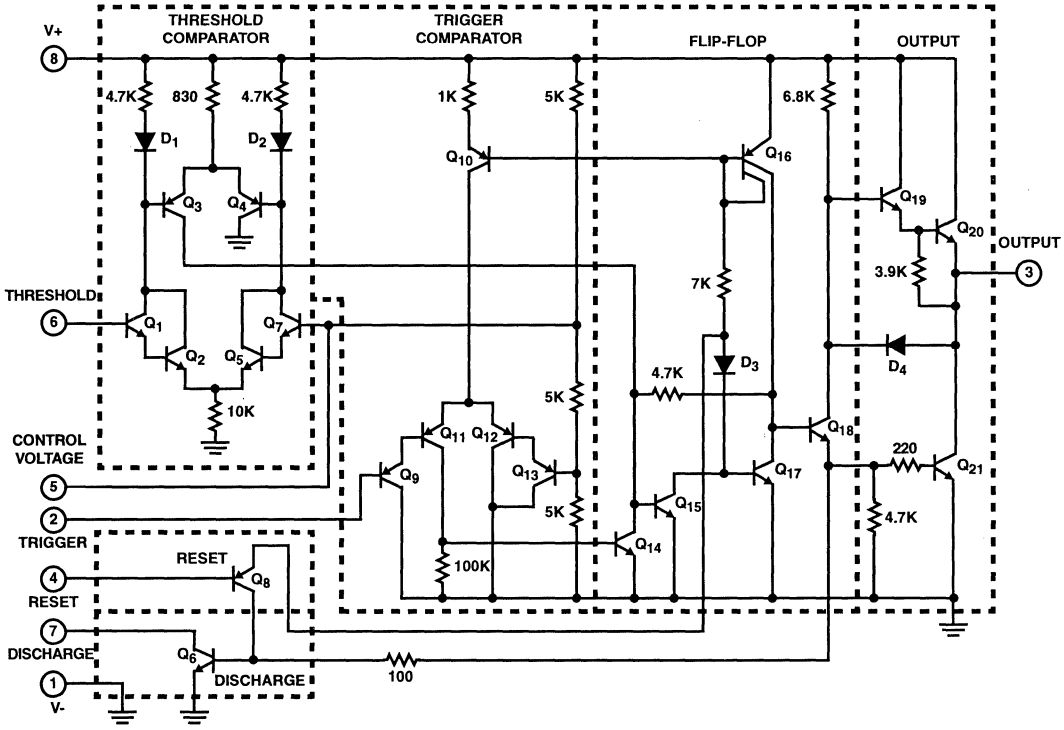
Electrical Specifications $T_A = 25^oC$, V+ = 5V to 15V Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA555, LM555			CA555C, LM555C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Rise Time	t_R		-	100	-	-	100	-	ns
Output Fall Time	t_F		-	100	-	-	100	-	ns

NOTES:

2. When the output is in a high state, the DC supply current is typically 1mA less than the low state value.
3. The threshold current will determine the sum of the values of R_1 and R_2 to be used in Figure 4 (astable operation); the maximum total $R_1 + R_2 = 20M\Omega$.

Schematic Diagram

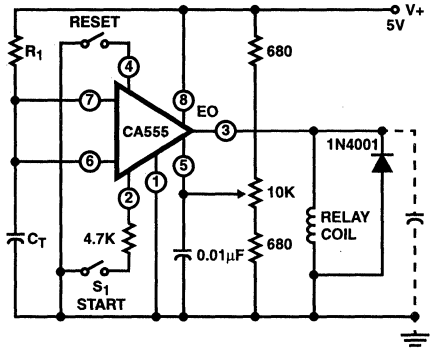


NOTE: Resistance values are in ohms.

Typical Applications

Reset Timer (Monostable Operation)

Figure 1 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.



NOTE: All resistance values are in ohms.

FIGURE 1. RESET TIMER (MONOSTABLE OPERATION)

Since the charge rate and threshold level of the comparator are both directly proportional to V+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1V change in V+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Figure 2 shows the typical waveforms generated during this mode of operation, and Figure 3 gives the family of time delay curves with variations in R_1 and C_T.

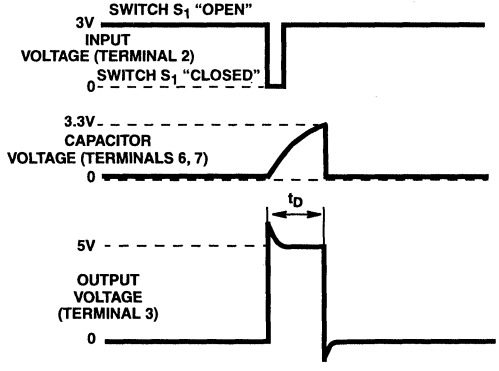


FIGURE 2. TYPICAL WAVEFORMS FOR RESET TIMER

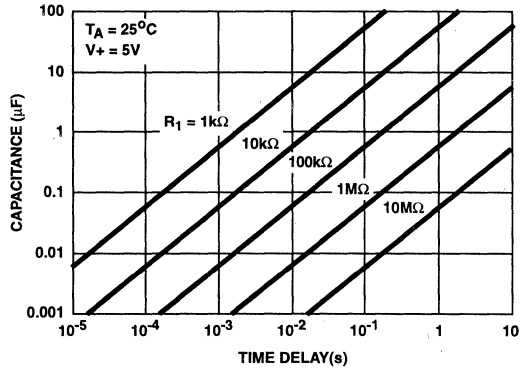


FIGURE 3. TIME DELAY vs RESISTANCE AND CAPACITANCE

Repeat Cycle Timer (Astable Operation)

Figure 4 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R_1 and R_2.

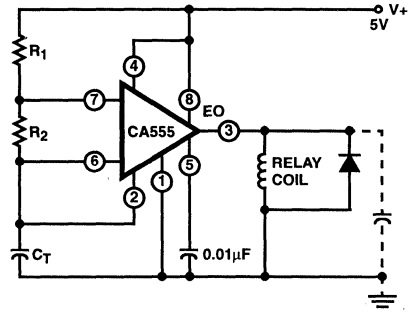


FIGURE 4. REPEAT CYCLE TIMER (ASTABLE OPERATION)

$$T = 0.693\,(R_1 + 2R_2)\,C_T = t_1 + t_2$$

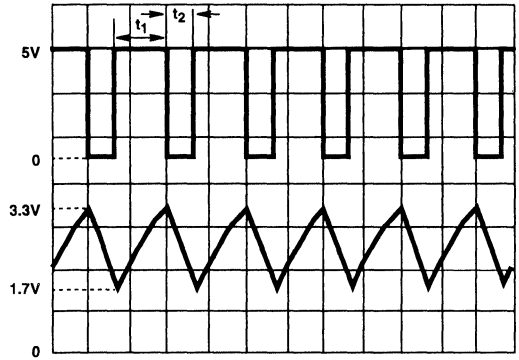
where $t_1 = 0.693\,(R_1 + R_2)\,C_T$

and $t_2 = 0.693\,(R_2)\,C_T$

the duty cycle is:

$$\frac{t_1}{t_1 + t_2} = \frac{R_1 + R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Figure 5. Figure 6 gives the family of curves of free running frequency with variations in the value of $(R_1 + 2R_2)$ and C_T.



Top Trace: Output voltage (2V/Div. and 0.5ms/Div.)
Bottom Trace: Capacitor voltage (1V/Div. and 0.5ms/Div.)

FIGURE 5. TYPICAL WAVEFORMS FOR REPEAT CYCLE TIMER

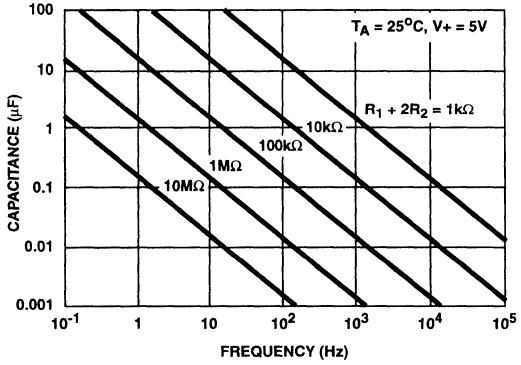
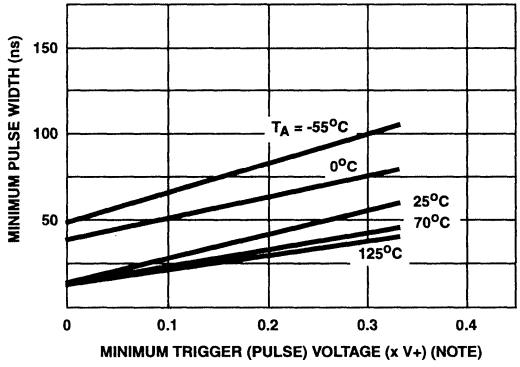


FIGURE 6. FREE RUNNING FREQUENCY OF REPEAT CYCLE TIMER WITH VARIATION IN CAPACITANCE AND RESISTANCE

Typical Performance Curves



NOTE: Where x is the decimal multiplier of the supply voltage.

FIGURE 7. MINIMUM PULSE WIDTH vs MINIMUM TRIGGER VOLTAGE

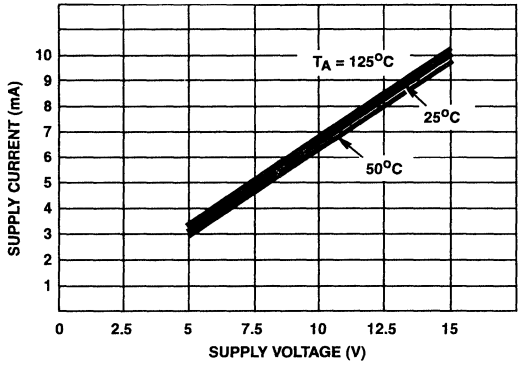


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE

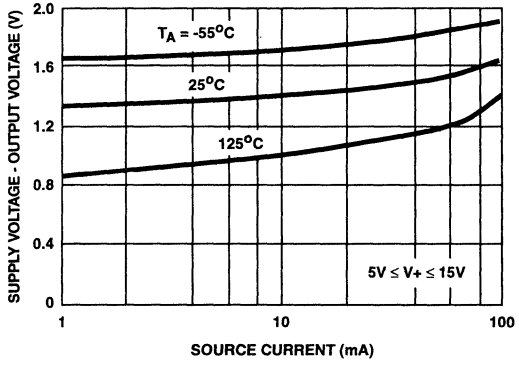


FIGURE 9. OUTPUT VOLTAGE DROP (HIGH STATE) vs SOURCE CURRENT

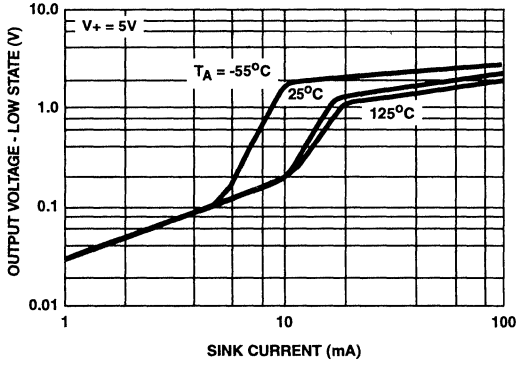


FIGURE 10. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT

Typical Performance Curves (Continued)

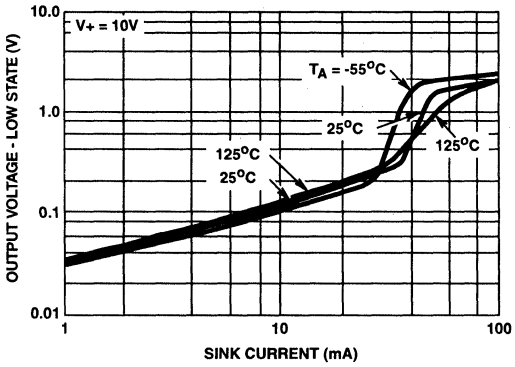


FIGURE 11. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT

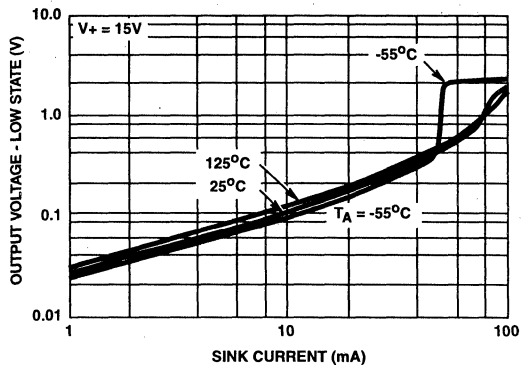


FIGURE 12. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT

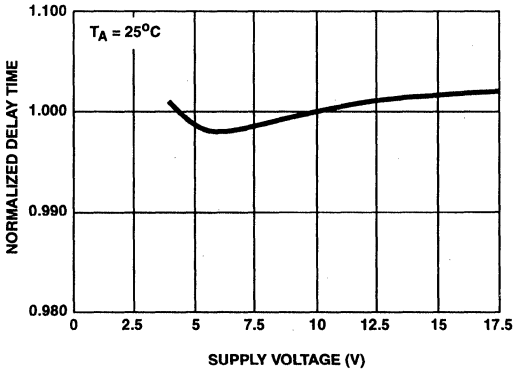


FIGURE 13. DELAY TIME vs SUPPLY VOLTAGE

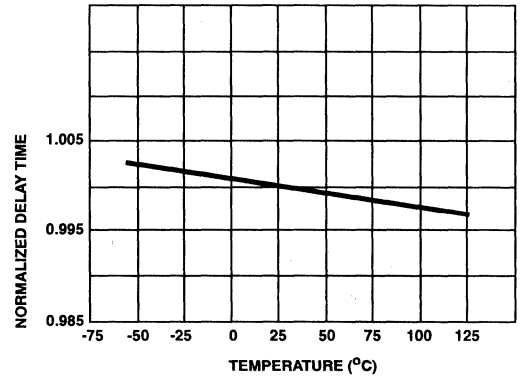
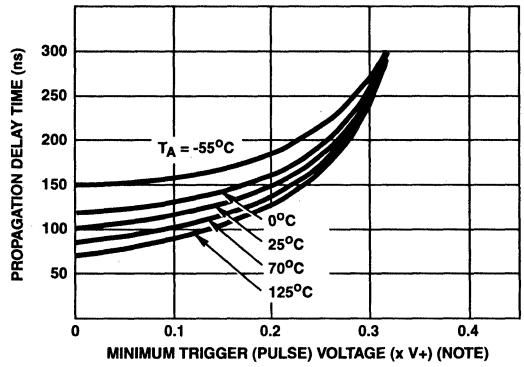


FIGURE 14. DELAY TIME vs TEMPERATURE



NOTE: Where x is the decimal multiplier of the supply voltage.

FIGURE 15. PROPAGATION DELAY TIME vs TRIGGER VOLTAGE

CA1391, CA1394

November 1996

TV Horizontal Processors

Features

- CA1391E - Positive Horizontal Sawtooth Input
- CA1394E - Negative Horizontal Sawtooth Input
- Internal Shunt Regulator
- Linear Balanced Phase Detector
- Preset Hold Control Capability
- Pull-In ..... ±300Hz (Typ)
- Low Thermal Frequency Drift
- Small Static Phase Error
- Variable Output Duty Cycle
- Adjustable DC Loop Gain

Description

The Harris CA1391E and CA1394E are monolithic integrated circuits designed for use in the low-level horizontal section of monochrome or color television receivers. Functions include a phase detector, an oscillator, a regulator, and a pre-driver.

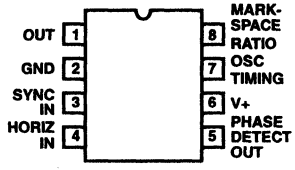
The CA1391E and CA1394E are electrically equivalent and pin compatible with industry types 1391 and 1394 in similar packages.

Ordering Information

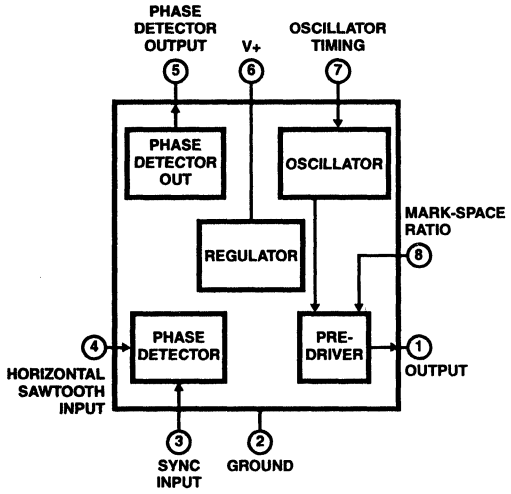
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA1391E	0 to 85	8 Ld PDIP	E8.3
CA1394E	0 to 85	8 Ld PDIP	E8.3

Pinout

CA1391, CA1394
(PDIP)
TOP VIEW



Functional Diagram



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 981.3

Absolute Maximum Ratings

DC Supply Current 40mA
DC Output Voltage 40V
DC Output Current 30mA
Sync Input Voltage ..... $5V_{P-P}$
Sawtooth Input Voltage ..... $5V_{P-P}$

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PDIP Package 120
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C

Operating Conditions

Temperature Range ..... 0°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications (See Figure 1)

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Supply Voltage	$S_1, S_5, S_6 = 2$; $S_2, S_3, S_4, S_7, S_8 = 1$ Measure Terminal 6 to GND	25	8	-	9	V
Free Running Frequency -1%	$S_1, S_5, S_6 = 2$; $S_2, S_3, S_4, S_7, S_8 = 1$ Counter to Terminal 1	25	14734	-	16734	Hz
Output Leakage	$S_2, S_3, S_6, S_8 = 1$; $S_1, S_4, S_5, S_7 = 2$ Measure Terminal 1 to 25V	25	-	10	-	mV
Output Saturation	$S_2, S_3, S_5, S_6, S_8 = 1$; $S_1, S_4, S_7 = 2$ Measure Terminal 1 to GND	25	-	60	-	mV
Phase Detector Bias	$S_2, S_5, S_6, S_8 = 1$; $S_1, S_3, S_4, S_7 = 2$ Measure Terminal 3 to GND	25	-	1.9	-	V
Phase Detector Leak	$S_5, S_8 = 1$; $S_1, S_2, S_3, S_4, S_6, S_7 = 2$ Measure Terminal 5 to +4V	25	-2	-	2	mV
Phase Detector Low	$S_1, S_5, S_8 = 1$; $S_2, S_3, S_4, S_6, S_7 = 2$ Measure Terminal 5 to +4V	25	-0.55 (Note 2)	-	-	V
Phase Detector High	$S_1, S_5, S_6, S_8 = 1$; $S_2, S_3, S_4, S_7 = 2$ Measure Terminal 5 to +4V	25	+0.55 (Note 2)	-	-	V
Phase Detector Balance	$V_{DET2} + V_{DET3}$	25	-100	-	100	mV
Sync Diode	$S_1, S_2, S_3, S_4, S_6, S_7 = 1$; $S_5, S_8 = 2$	25	0.3	-	1.2	V
Static Phase Error	See Figure 3	25	-	0.5	-	µs
Oscillator Pull In Range			-	±300	-	Hz
Oscillator Hold In Range			-	±900	-	Hz

NOTE:

2. Polarity reversed in the CA1391.

Test Circuit

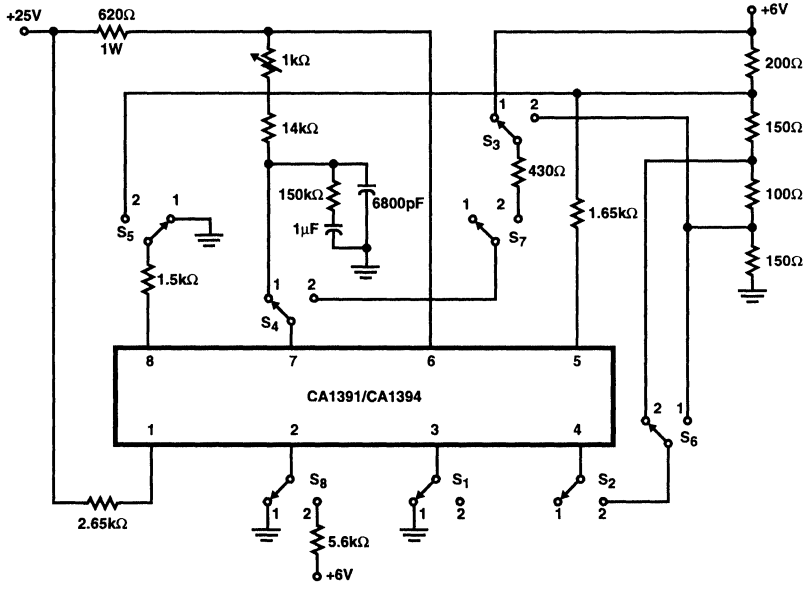
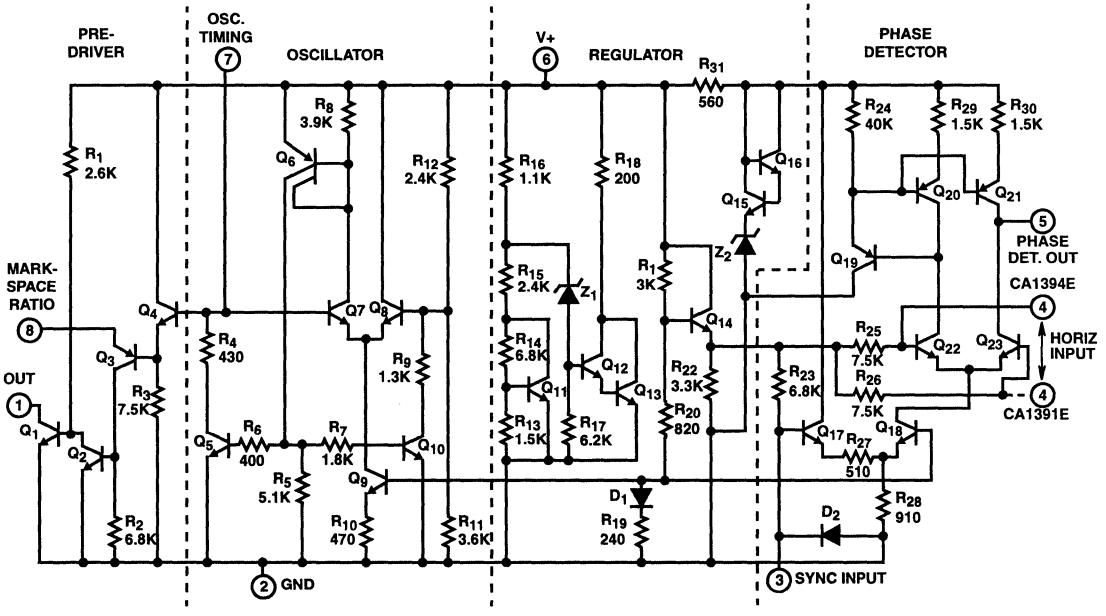


FIGURE 1. DC TEST CIRCUIT

Schematic Diagram



NOTE: All resistances are in ohms.

Application Information

Circuit Operation (See Schematic Diagram)

The CA1391 and CA1394 contain the oscillator, phase detector, and predriver sections necessary for the television horizontal oscillator and AFC loop.

The oscillator is an RC type with Terminal 7 used to control the timing. If it is assumed that Q_7 is initially off, then an external capacitor connected from Terminal 7 to ground charges through an external resistance connected between Terminals 6 and 7. As soon as the voltage at Terminal 7 exceeds the potential set at the base of Q_8 by resistors R_{11} and R_{12}, Q_7 turns on, and Q_6 supplies base current to Q_5 and Q_{10}. Transistor Q_5 discharges the capacitor through R_4 until the base bias of Q_7 falls below that of Q_8 at which time, Q_7 turns off, and the cycle repeats.

The sawtooth generated at the base of Q_4 appears across R_3 and turns off Q_3 whenever the sawtooth voltage rises to a value that exceeds the bias set at Terminal 8. By adjusting the potential at Terminal 8, the duty cycle at the pre-drive output (Terminal 1) may be changed. The phase detector is isolated from the remainder of the circuit by R_{31}, Z_2, Q_{15} and Q_{16}. The phase detector consists of the comparator Q_{22} and Q_{23}, and the gated current source Q_{18}. Negative going sync pulses at Terminal 3 turn off Q_{17}, and the current division between Q_{22} and Q_{23} is then determined by the phase relationship of the sync and the sawtooth waveform at Terminal 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents flow in the collectors of Q_{22} and Q_{23} during each half of the sync pulse period. The current in Q_{22} is turned around by current mirror Q_{20} and Q_{21} so that there is no net output current at Terminal 5 for balanced conditions. When a phase offset occurs, current flows either in or out of Terminal 5. In circuit applications, this terminal is connected to Terminal 7 through an external low pass filter, thereby controlling the oscillator.

Shunt regulation for the circuit is obtained by using a V_{BE} and zener multiplier. Resistors R_{13} and R_{14} multiply the V_{BE} of Q_{11}, and the ratio of R_{15} and R_{16} multiplies the voltage of the zener diode Z_1.

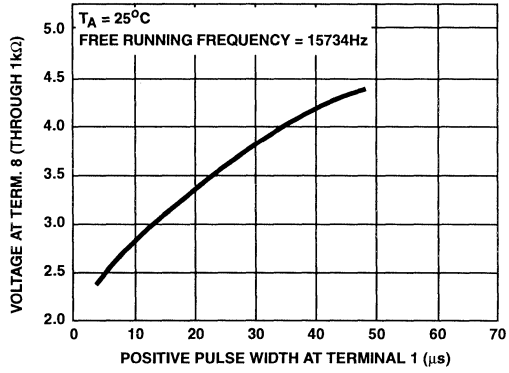


FIGURE 2. DUTY CYCLE AT THE PRE-DRIVE OUTPUT (TERMINAL 1) AS IT IS AFFECTED BY THE INPUT AT TERMINAL 8

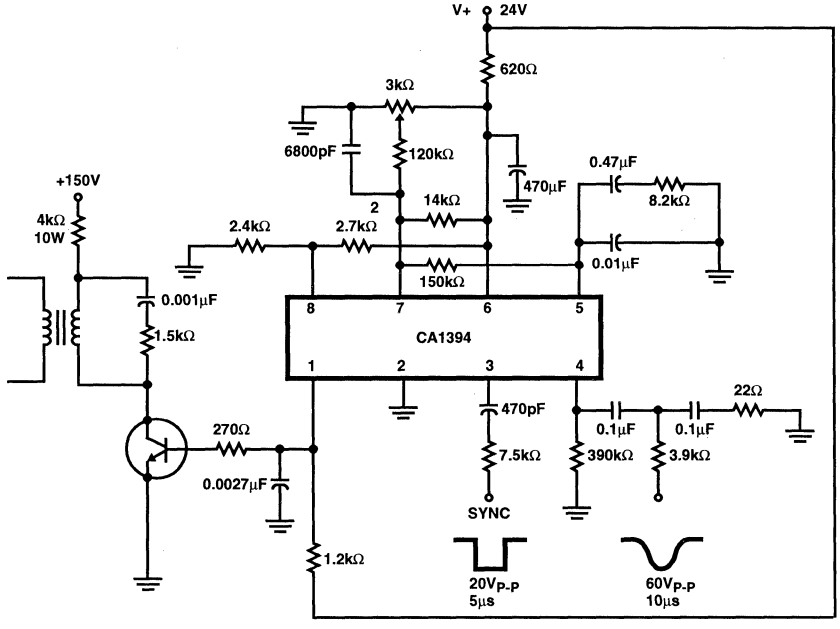


FIGURE 3. TYPICAL CIRCUIT APPLICATION

HARRIS SEMICONDUCTOR

CA2111A

FM IF Amplifier-Limiter and Quadrature Detector

November 1996

Features

- Input Limiting Voltage At 10.7MHz 400μV
- Input Limiting Voltage At 4.5, 5.5MHz 250μV
- Typical AM Rejection At 10.7MHz. 45dB
- Provision for Output from 3-Stage IF Amplifier Section
- Low Harmonic Distortion
- Quadrature Detection Permits Simplified Single-Coil Tuning
- Extremely Low AFC Voltage Drift Over Full Operating Temperature Range
- Minimum Number of External Components Required

Applications

- FM IF Sound
- TV Sound IF

Description

The CA2111A provides a multistage wideband amplifier-limiter, a quadrature detector, and an emitter-follower output stage. This device is designed for use in FM receivers and in the sound IF sections of TV receivers. In addition, an output terminal is provided which allows the use of the amplifier-limiter as a straight 60dB wideband amplifier.

The amplifier-limiter features the excellent limiting characteristic of 3 cascaded differential amplifiers. The quadrature detector requires only one coil in the associated outboard circuit and therefore, tuning is a simple procedure.

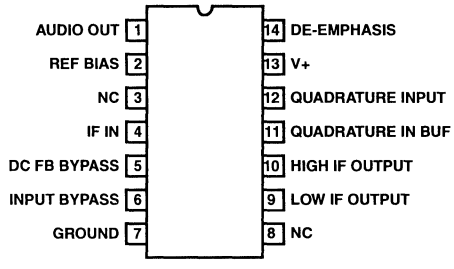
A unique feature of the CA2111A is its exceptionally low AFC voltage drift over the full operating-temperature range.

Ordering Information

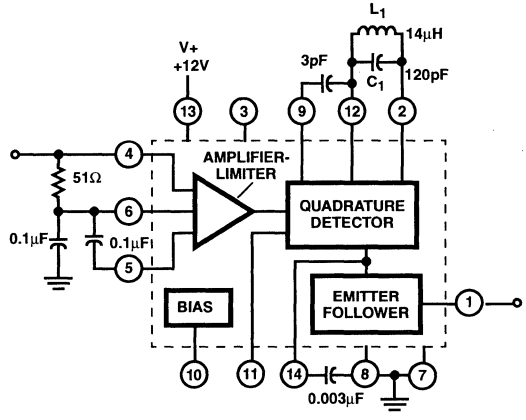
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA2111AE	-40 to 85	14 Ld PDIP	E14.3

Pinout

CA2111A
(PDIP)
TOP VIEW



Block Diagram



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 612.1

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V+ to V-) 16V

Operating Conditions

Temperature Range . . . . . -40°C to 85°C
Supply Voltage Range (Typical) . . . . . 8V to 12V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	150

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

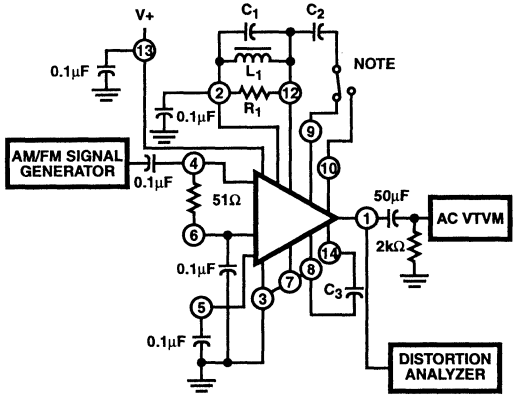
Electrical Specifications $T_A = 25^oC$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Terminal 1 DC Voltage	V_1	V+ = 12V	-	5.4	-	V
		V+ = 8V	-	3.7	-	V
Terminals 4, 5, 6, 10 DC Voltage	$V_{4, 5, 6, 10}$	V+ = 8V	-	1.35	-	V
Terminals 2, 12 DC Voltage	$V_{2, 12}$	V+ = 8V	-	3.5	-	V
Supply Current, Pin 13	I_{13}	V+ = 8V	-	14	-	mA
		V+ = 12V	-	16	-	mA
Amplifier Input Resistance	R_4	f_O = 10.7MHz	-	7	-	kΩ
Amplifier Input Capacitance	C_4		-	11	-	pF
Detector Input Resistance	R_{12}		-	70	-	kΩ
Detector Input Capacitance	C_{12}		-	2.7	-	pF
Amplifier Output Resistance	R_{10}		-	60	-	Ω
Detector Output Resistance	R_1		-	200	-	Ω
De-emphasis Resistance	R_{14}		-	8.8	-	kΩ
DYNAMIC CHARACTERISTICS f_O = 10.7MHz, Δf = ±75kHz, V+ = 8V, FM Modulation Frequency = 400Hz, Source Resistance = 50Ω						
Input Limiting Threshold Voltage	$V_{I(LIM)}$		-	400	600	μV_{RMS}
AM Rejection	AMR	$V_I = 10mV_{RMS}$, 100% FM, 30% AM	-	37	-	dB
Amplifier Voltage Gain	A_V	$V_I = 50\mu V_{RMS}$	-	55	-	dB
Detector Recovered Audio Output	$V_{O(AF)}$	$V_I = 10mV_{RMS}$	-	0.3	-	V_{RMS}
Total Harmonic Distortion	THD	$V_I = 10mV_{RMS}$	-	1	-	%
DYNAMIC CHARACTERISTICS f_O = 10.7MHz, Δf = ±75kHz, V+ = 12V, FM Modulation Frequency = 400Hz, Source Resistance = 50Ω						
Input Limiting Threshold Voltage	$V_{I(LIM)}$		-	400	600	μV_{RMS}
AM Rejection	AMR	$V_I = 10mV_{RMS}$, 100% FM, 30% AM	-	45	-	dB
Amplifier Voltage Gain	A_V	$V_I = 50\mu V_{RMS}$	-	55	-	dB
Detector Recovered Audio Output	$V_{O(AF)}$	$V_I = 10mV_{RMS}$	-	0.48	-	V_{RMS}
Total Harmonic Distortion	THD	$V_I = 10mV_{RMS}$	-	1	-	%
DYNAMIC CHARACTERISTICS f_O = 4.5MHz, Δf = ±25kHz, V+ = 12V, FM Modulation Frequency = 400Hz, Source Resistance = 50Ω						
Input Limiting Threshold Voltage	$V_{I(LIM)}$		-	250	400	μV_{RMS}
AM Rejection	AMR	$V_I = 10mV_{RMS}$, 100% FM, 30% AM	-	36	-	dB

Electrical Specifications $T_A = 25^oC$ Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier Voltage Gain	A_V	$V_I = 50\mu V_{RMS}$	-	60	-	dB
Detector Recovered Audio Output	$V_{O(AF)}$	$V_I = 10mV_{RMS}$	-	0.72	-	V_{RMS}
Total Harmonic Distortion	THD	$V_I = 10mV_{RMS}$	-	1.5	-	%
DYNAMIC CHARACTERISTICS $f_O = 5.5MHz$, $\Delta f = \pm 50kHz$, V+ = 12V, FM Modulation Frequency = 400Hz, Source Resistance = 50Ω						
Input Limiting Threshold Voltage	$V_{I(LIM)}$		-	250	400	μV_{RMS}
AM Rejection	AMR	$V_I = 10mV_{RMS}$, 100% FM, 30% AM	-	40	-	dB
Amplifier Voltage Gain	A_V	$V_I = 50\mu V_{RMS}$	-	60	-	dB
Detector Recovered Audio Output	$V_{O(AF)}$	$V_I = 10mV_{RMS}$	-	1.2	-	V_{RMS}
Total Harmonic Distortion	THD	$V_I = 10mV_{RMS}$	-	3	-	%

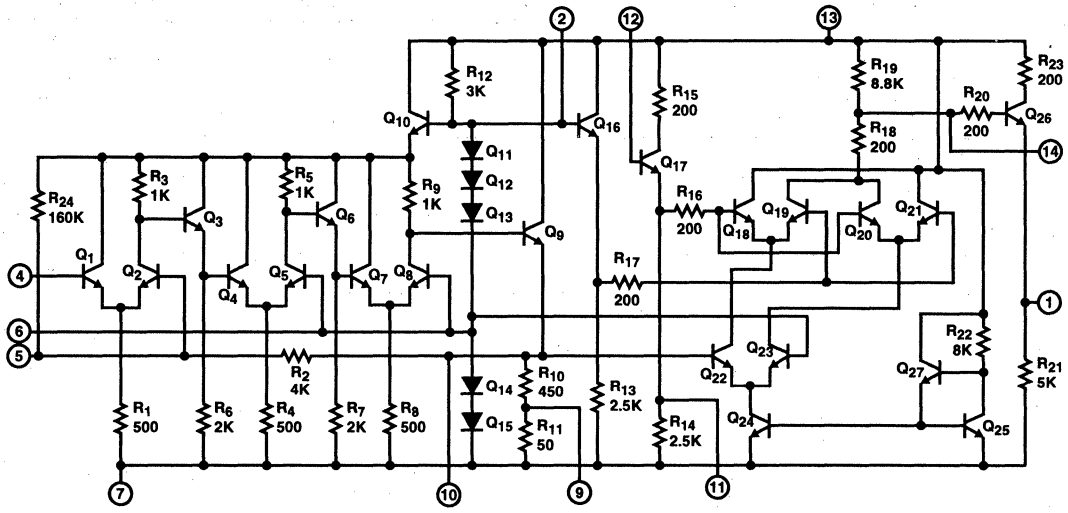
Test Circuit



NOTE: Input to the quadrature coil can be from either terminal 9 or terminal 10. Terminal 9 is normally used because it lessens the possibility of overloads during tuning. The use of terminal 10 increases the limiting sensitivity significantly and has been used successfully in these tests.

COMPONENT VALUES							DETECTOR TRANSFER CHARACTERISTICS	
f	L_1	C_1	R_1	Q	C_2	C_3	UPPER PEAK	LOWER PEAK
MHz	µH	pF	kΩ	-	pF	µF	MHz	MHz
4.5	14	120	20	30	3	0.003	4.58	4.42
5.5	8	100	20	30	3	0.003	5.63	5.37
10.7	2	120	3.9	20	4.7	0.01	10.9	10.5

Schematic Diagram



Typical Performance Curves

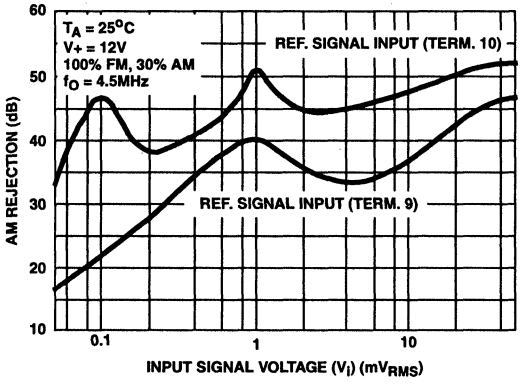


FIGURE 2. AM REJECTION vs INPUT VOLTAGE (AT 4.5MHz)

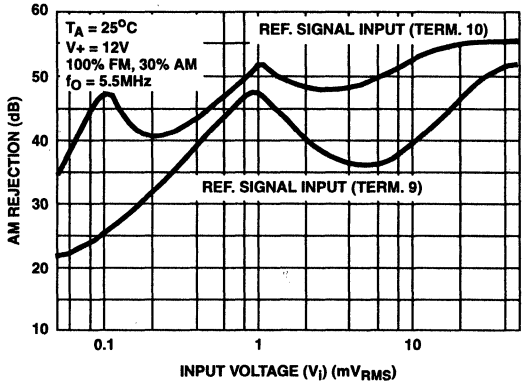


FIGURE 3. AM REJECTION vs INPUT VOLTAGE (AT 5.5MHz)

Typical Performance Curves (Continued)

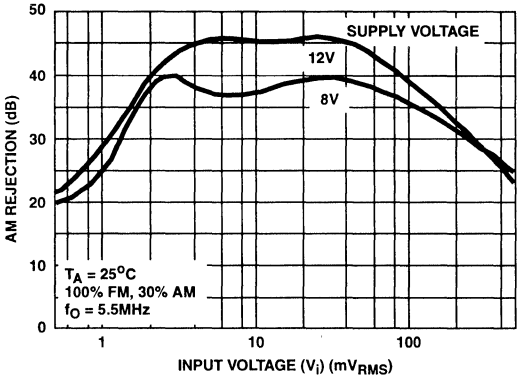


FIGURE 4. AM REJECTION vs INPUT VOLTAGE (AT 10.7MHz)

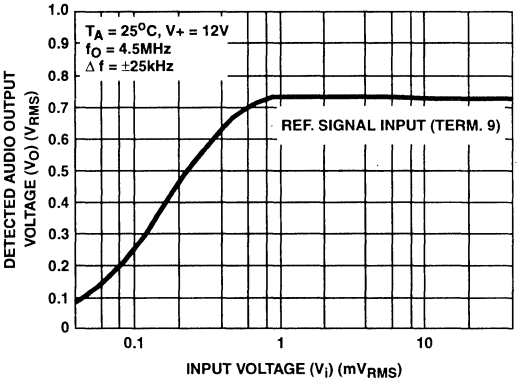


FIGURE 5. DETECTED AUDIO OUTPUT vs INPUT VOLTAGE (4.5MHz)

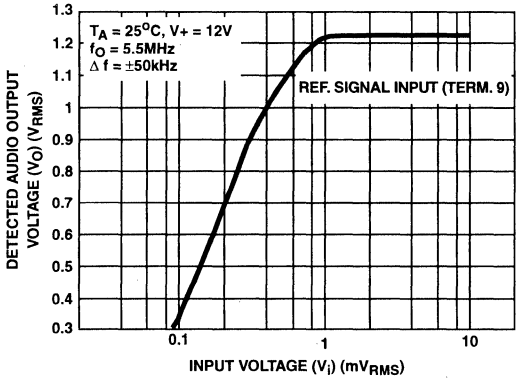


FIGURE 6. DETECTED AUDIO OUTPUT vs INPUT VOLTAGE (AT 5.5MHz)

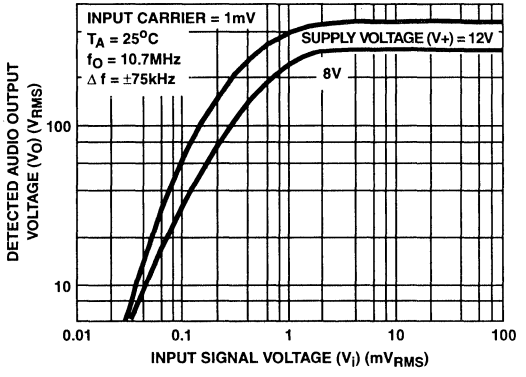


FIGURE 7. DETECTED AUDIO OUTPUT VOLTAGE vs INPUT VOLTAGE (AT 10.7MHz)

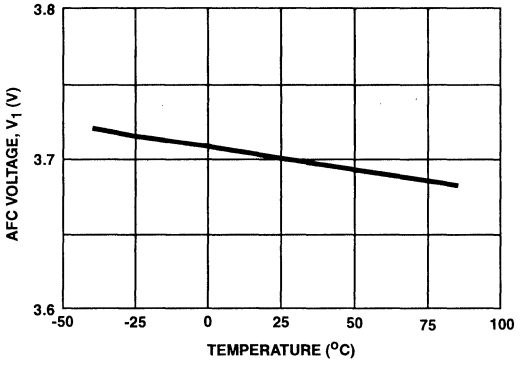


FIGURE 8. AFC VOLTAGE vs AMBIENT TEMPERATURE

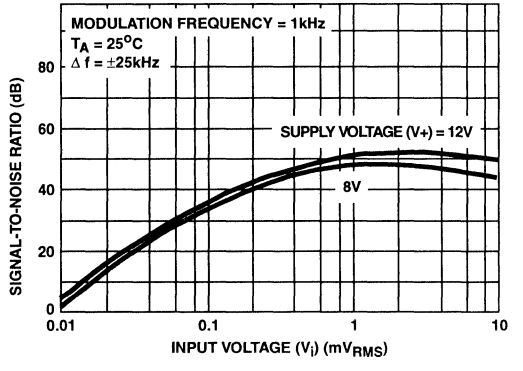


FIGURE 9. SIGNAL-TO-NOISE RATIO vs INPUT VOLTAGE

HARRIS SEMICONDUCTOR

CA3012

November 1996

FM IF Wideband Amplifier

Features

- **Exceptionally High Amplifier Gain**
  - **Power Gain at 4.5MHz 75dB**
- **Excellent Input Limiting Characteristics**
  - **Limiting Voltage (Knee) at 10.7MHz .... 600μV (Typ)**
- **Wide Frequency Capability:**
  - **Bandwidth..... 100kHz to 20MHz**

Applications

- **FM IF Amplifiers**
- **FM Communication Receivers**
- **TV IF Amplifiers**

Description

The CA3012 is an FM IF wideband amplifier with 3 limiter gain stages in a bipolar monolithic technology. The pin 1 input is an open base and has a separate feedback bias. The feedback bias pin, DC FB BYPASS, is externally bypassed and provides the means for a tuned coil input to the IF IN pin. The output is a high impedance open collector which may be matched to a tuned transformer, driving an FM detector. Internal regulation circuits provide DC bias to the gain stages and DC feedback circuit.

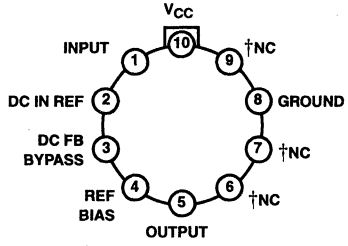
The CA3012 is intended for FM limiting applications requiring high gain.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3012	-55 to 125	10 Ld Metal Can	T10.C

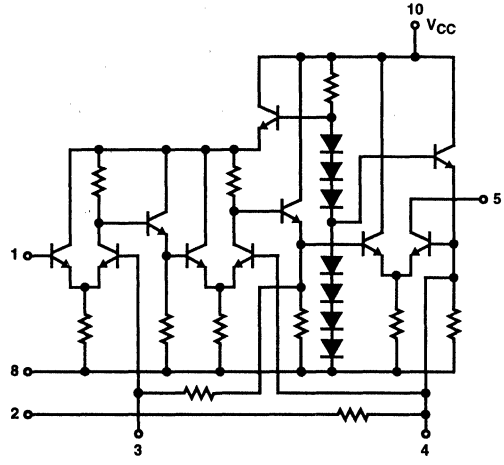
Pinout

CA3012
(METAL CAN)
TOP VIEW



†Internal connection, do not use.

Schematic Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **128.1**

Absolute Maximum Ratings $T_A = 25^oC$

Maximum Supply Voltage V_{CC}, Pin 10 . . . . . 10V
Maximum Output Voltage, Pin 5 . . . . . 13V
Maximum Input Signal Voltage between Pin 1 and Pin 2 . . . . . ±3VV

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC
Supply Voltage Range (Typical) . . . . . 5.5V to 10V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
Metal Can Package	175	100

Maximum Junction Temperature . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS: SETUP AND PROCEDURE (FIGURE)	TEST CONDITIONS: FREQUENCY f (MHz)	TEST CONDITIONS: DC SUPPLY VOLTAGE V_{CC} (V)	TEST CONDITIONS: TEMP (^oC)	MIN	TYP	MAX	UNITS
Total Device Dissipation (Note 2)	P_T	1	-	6	-55	66	80	135	mW
					25	66	90	121	mW
					125	65	70	121	mW
			-	7.5	-55	97	130	190	mW
					25	97	120	167	mW
					125	95	100	167	mW
			-	10	-55	150	210	275	mW
					25	150	190	255	mW
					125	150	160	255	mW
Voltage Gain (Note 3)	A	3	1	6	-55	50	55	-	dB
					25	60	66	-	dB
					125	50	61	-	dB
		3	1	7.5	-55	55	59	-	dB
					25	65	70	-	dB
					125	55	65	-	dB
		3	1	10	-55	55	61	-	dB
					25	65	71	-	dB
					125	55	66	-	dB
		3	4.5	7.5	25	60	67	-	dB
			10.7	7.5	25	55	61	-	dB
Input Impedance Components									
Parallel Input Resistance	R_{IN}	6	4.5	7.5	25	-	3	-	kΩ
Parallel Input Capacitance	C_{IN}	6	4.5	7.5	25	-	7	-	pF
Output Impedance Components									
Parallel Output Resistance	R_{OUT}	8	4.5	7.5	25	-	31.5	-	kΩ
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	25	-	4.2	-	pF
Noise Figure	NF	10	4.5	7.5	25	-	8.7	-	dB
Input Limiting Voltage (Knee)	$V_{I(LIM)}$	3	4.5	7.5	25	-	300	400	µV

NOTES:

2. The total current drain may be determined by dividing P_T by V_{CC}.
3. Recommended minimum DC supply voltage (V_{CC}) is 5.5V. Nominal load current flowing into terminal 5 is 1.5mA at 7.5V.

Typical Performance Curves and Test Setups

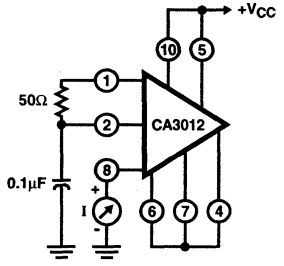


FIGURE 1. DISSIPATION TEST SETUP

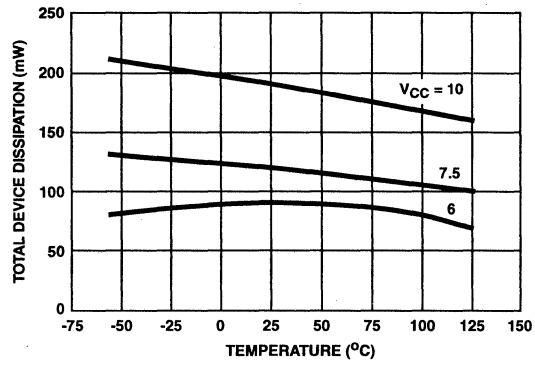
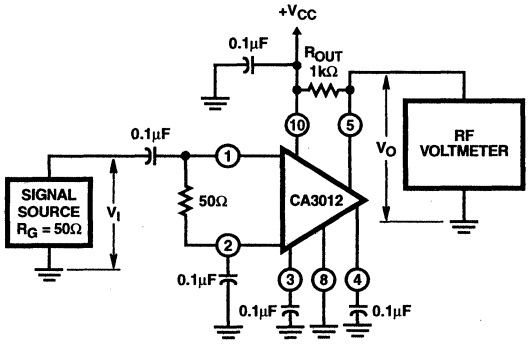


FIGURE 2. DISSIPATION vs TEMPERATURE



Procedures

A. Voltage Gain

1. Set input frequency at desired value, $V_I = 100\mu V_{RMS}$
2. Record V_O
3. Calculate Voltage Gain A from $A = 20 \log_{10} V_O/V_I$
4. Repeat steps 1, 2 and 3 for each frequency and/or for temperature desired

B. Input Limiting Voltage (Knee)

1. Repeat steps A1 and A2, using $V_I = 100mV$
2. Decrease V_I to the level at which V_O is 3dB below its value for $V_I = 100mV$
3. Record V_I as Input Limiting Voltage (Knee)

FIGURE 3. VOLTAGE GAIN TEST SETUP

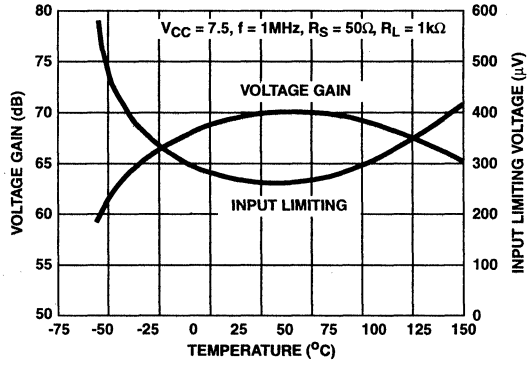


FIGURE 4. VOLTAGE GAIN AND INPUT LIMITING VOLTAGE vs TEMPERATURE

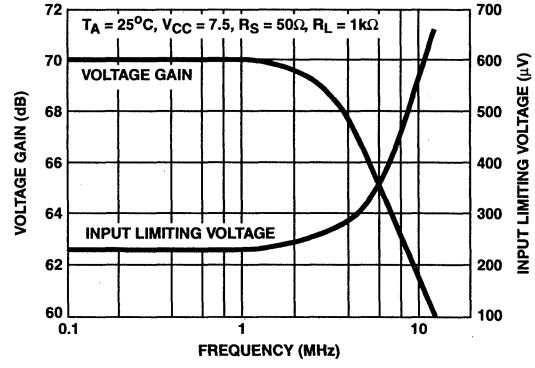


FIGURE 5. VOLTAGE GAIN AND INPUT LIMITING VOLTAGE vs FREQUENCY

Typical Performance Curves and Test Setups (Continued)

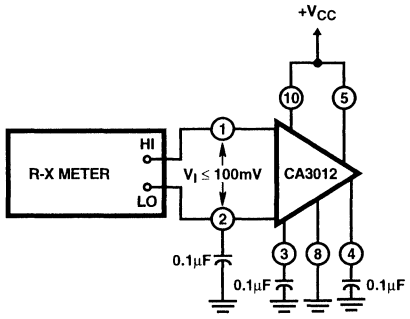


FIGURE 6. INPUT IMPEDANCE TEST SETUP

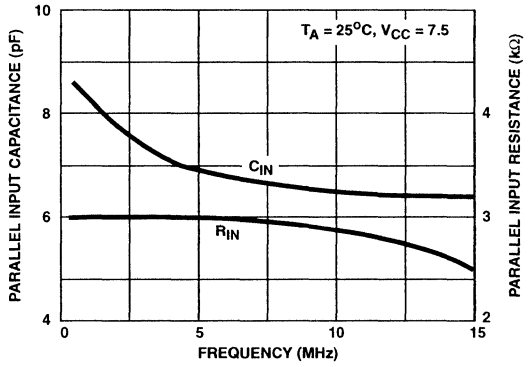


FIGURE 7. INPUT IMPEDANCE vs FREQUENCY

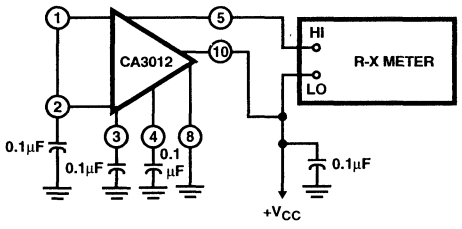


FIGURE 8. OUTPUT IMPEDANCE TEST SETUP

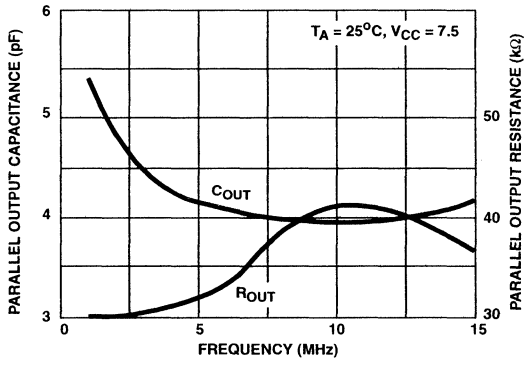


FIGURE 9. OUTPUT IMPEDANCE vs FREQUENCY

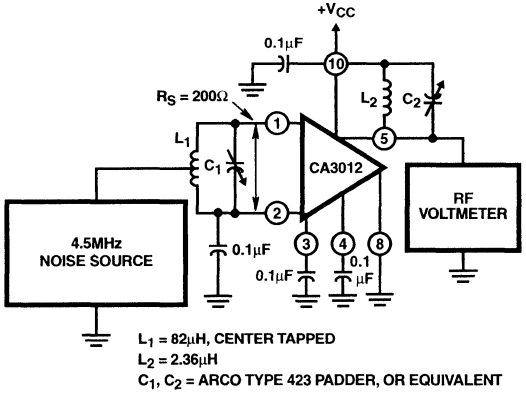


FIGURE 10.

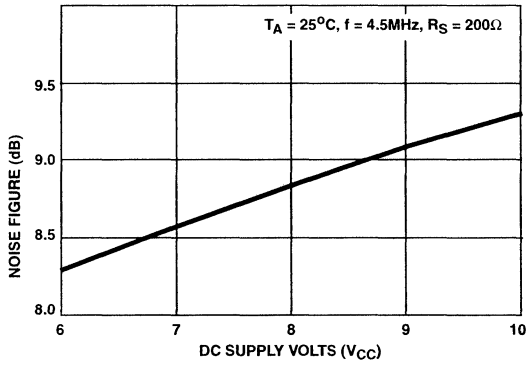


FIGURE 11. NOISE FIGURE vs DC SUPPLY VOLTAGE

Typical Application

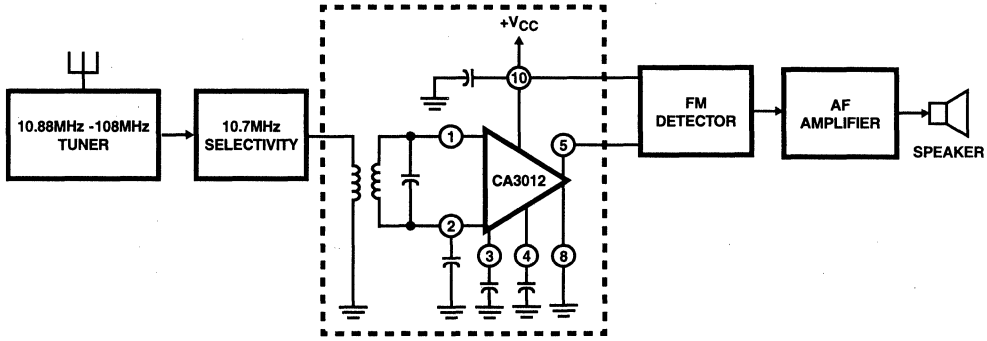


FIGURE 12. BLOCK DIAGRAM OF TYPICAL FM RECEIVER USING THE CA3012 INTEGRATED CIRCUIT WIDEBAND AMPLIFIER

HARRIS SEMICONDUCTOR

CA3088E

AM Receiver Subsystem and General-Purpose Amplifier Array

November 1996

Features

- Excellent Overload Characteristics
- AGC for IF Amplifier
- Buffered Output Signal for Tuning Meter
- Internal Zener Diode Provides Voltage Regulation
- Two IF Amplifier Stages
- Low-Noise Converter and First IF Amplifier
- Low Harmonic Distortion (THD)
- Delayed AGC for RF Amplifier
- Terminals for Optional Inclusion of Tone Control
- Operates from Wide Range of Power Supplies: V+ = 6V to 16V
- Optional AC and/or DC Feedback on Wide-Band Amplifier
- Array of Amplifiers for General-Purpose Applications
- Suitable for Use With Optional External RF Stage, Either MOS or Bipolar
- Related at:
  - Refer to AN6022 for Application Note Information

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3088E	-40 to 85	16 Ld PDIP	E16.3

Description

The CA3088E, a monolithic integrated circuit, is an AM subsystem that provides the converter, IF amplifier, detector, and audio preamplifier stages for an AM receiver.

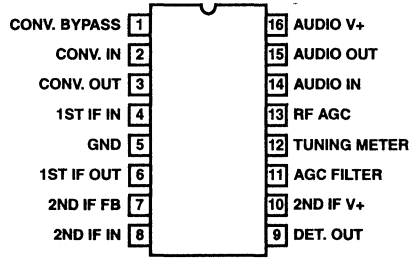
The CA3088E also provides internal AGC for the first IF amplifier stage, delayed AGC for an optional external RF amplifier, a buffer stage to drive a tuning meter, and terminals facilitating the optional use of a tone control.

Figure 2 is a functional diagram of the CA3088E. The signal from the low-noise converter is applied to the first IF amplifier and is then coupled to the second IF amplifier. This IF signal is then detected and externally filtered. The resultant audio signal is applied to an audio preamplifier. Optionally, a tone control circuit may be connected at the junction of the detector circuit and the audio preamplifier. The gain of the first IF amplifier stage is controlled by an internal AGC circuit. The CA3088E supplies a delayed AGC signal output for use with an external RF amplifier. A buffered output signal is also available for driving a tuning meter. A DC voltage, internally regulated by a Zener diode, supplies the second IF amplifier, the AGC and tuning meter circuits and may also be used with any other stage.

The CA3088E features four independent transistor amplifiers, each incorporating internal biasing for temperature tracking. These amplifiers are particularly useful in general-purpose amplifier, oscillator, and detector applications in a wide variety of equipment designs.

Pinout

CA3088E
(PDIP)
TOP VIEW



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 560.1

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage
(Across Term. 5 and Terms. 3, 6, 13, 16, Respectively) 16V
Output Current
Terminals 3, 6, 13, 16, (Respectively) 10mA
Terminal 10 ..... 30mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
PDIP Package 110
Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC

Operating Conditions

Temperature Range ..... -40^oC to 85^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, V+ = 12V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Voltage (Figure 1)	V_1, V_4, V_9, V_{11}	Terminals 1, 4, 9, 11	-	0.7	-	V
	V_2, V_7, V_8	Terminals 2, 7, 8	-	1.4	-	V
	V_{10}	Terminal 10	-	5.6	-	V
	V_{12}	Terminal 12	-	0	-	V
	V_{15}	Terminal 15	-	3.5	-	V
Current (Figure 1)	I_3	Terminal 3	-	0.35	-	mA
	I_6	Terminal 6	-	1.0	-	mA
	I_{10}	Terminal 10	-	20	-	mA
	I_{13}	Terminal 13	-	0	-	mA
	I_{16}	Terminal 16	-	1.2	-	mA
DYNAMIC CHARACTERISTICS						
Detector Output (Figure 2)		30% Modulation	-	75	-	mV_{RMS}
Audio Amplifier Gain (Figure 2)	A_{AF}	f = 1kHz	-	30	-	dB
Audio Distortion (Figure 2)		V_{OUT} = 100mV	-	0.2	-	%
Sensitivity (f_{IN} = 1MHz, Signal-to-Noise Ratio (S/N) = 20dB))		At Converter Stage Input (Figure 2)	-	200	-	µV/m
		At RF Stage Input (Figure 2)	-	100	-	µV/m
Total Harmonic Distortion (Figure 2)	THD	30% Modulation	-	1.0	-	%
Input Resistance (No AGC, f_{IN} = 1MHz)	R_{IN}	At Transistor Q_1	-	3500	-	Ω
		At Transistor Q_5	-	2000	-	Ω
Input Capacitance (No AGC, f_{IN} = 1MHz)	C_{IN}	At Transistor Q_1	-	17	-	pF
		At Transistor Q_5	-	12	-	pF
Feedback Capacitance (No AGC, f_{IN} = 1MHz)	C_{FB}	At Transistor Q_1	-	1.5	-	pF
		At Transistor Q_5	-	1.5	-	pF

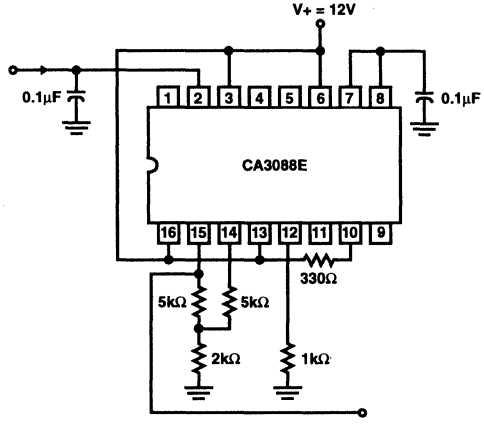
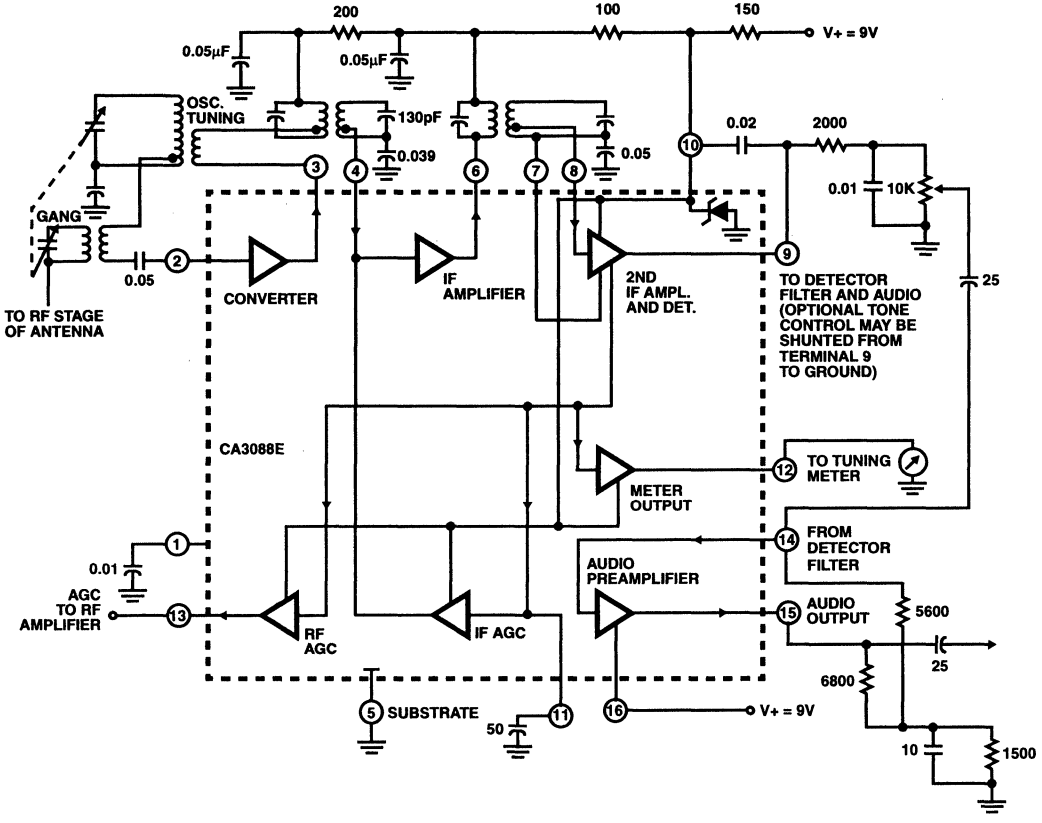


FIGURE 1. TEST CIRCUIT FOR DC CHARACTERISTICS



NOTE: Resistance values are in Ω. Capacitance values in μF, except as noted.

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM OF THE CA3088E

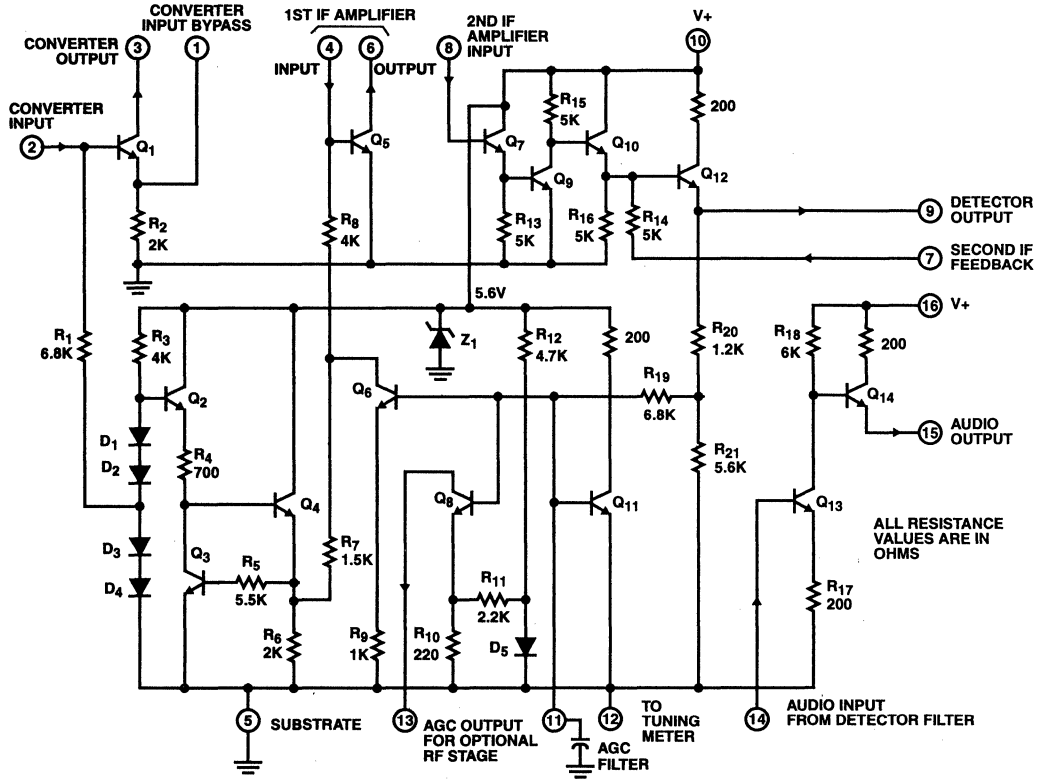


FIGURE 3. SCHEMATIC DIAGRAM OF THE CA3088E

CA3089

November 1996

FM IF System

Features

- For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers
- Includes: IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter
- Exceptional Limiting Sensitivity at -3dB Point . . . . . 12μV (Typ)
- Low Distortion: (with Double-Tuned Coil) . . . . . 0.1% (Typ)
- Single-Coil Tuning Capability
- High Recovered Audio . . . . . 400mV (Typ)
- Provides Specific Signal for Control of Interchannel Muting (Squelch)
- Provides Specific Signal for Direct Drive of a Tuning Meter
- Provides Delayed AGC Voltage for RF Amplifier
- Provides a Specific Circuit for Flexible AFC
- Internal Supply-Voltage Regulators

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3089E	-40 to 85	16 Ld PDIP	E16.3
CA3089M1 (3089M)	-40 to 85	20 Ld SOIC	M20.3

Description

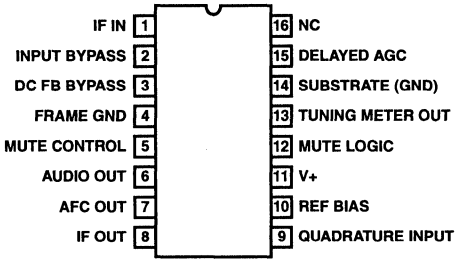
Harris CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. The block diagram shows the CA3089 features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, and AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16V.

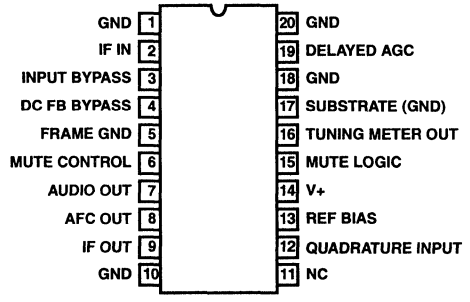
The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

Pinout

CA3089
(PDIP)
TOP VIEW



CA3089
(SOIC)
TOP VIEW



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 561.3

Absolute Maximum Ratings

Supply Voltage
- Between V+ and Frame GND 16V
- Between V+ and Substrate GND 16V

DC Current (Out of Delayed AGC) 2mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	80

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V+ = 12V (See Figures 3 and 4)

(NOTE 3) PARAMETER		TEST CONDITIONS		TEMP. (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS								
Quiescent Circuit Current		No signal input, Non muted		25	16	23	30	mA
DC Voltages	Terminal 1 (IF Input)			25	1.2	1.9	2.4	V
	Terminal 2 (AC Return to Input)			25	1.2	1.9	2.4	V
	Terminal 3 (DC Bias to Input)			25	1.2	1.9	2.4	V
	Terminal 6 (Audio Output)			25	5.0	5.6	6.0	V
	Terminal 10 (DC Reference)			25	5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS								
Input Limiting Voltage (-3dB point), V_1 (lim)		-	f_O = 10.7MHz, f_{MOD} = 400Hz, Deviation = ±75kHz	25	-	12	25	µV
AM Rejection (Terminal 6), AMR		V_{IN} = 0.1V, AM Mod. = 30%		25	45	55	-	dB
Recovered AF Voltage (Terminal 6) V_O (AF)		V_{IN} = 0.1V		25	300	400	500	mV
Total Harmonic Distortion, THD (Note 2)	Single Tuned (Terminal 6)			25	-	0.5	1.0	%
	Double Tuned (Terminal 6)			25	-	0.1	-	%
Signal Plus Noise to Noise Ratio (Terminal 6)				25	60	67	-	dB

NOTES:

2. THD characteristics are essentially a function of the phase characteristics of the network connected between Terminals 8, 9, and 10.
3. Terminal numbers refer to 16 Lead PDIP.

Application Information

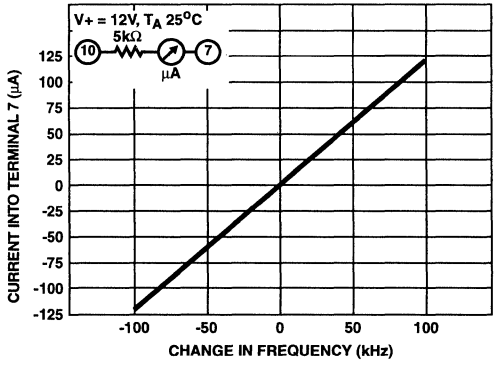


FIGURE 1. AFC CHARACTERISTICS (CURRENT AT TERMINAL 7) vs CHANGE IN FREQUENCY. (SEE TEST CIRCUIT FIGURE 3.)

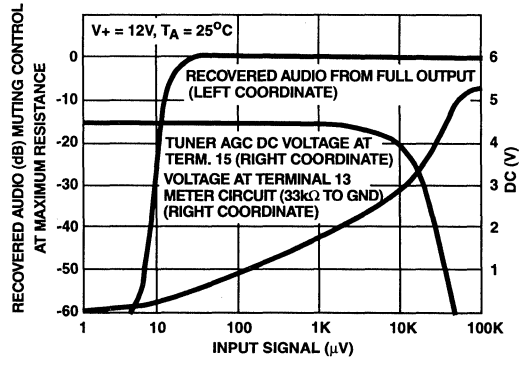
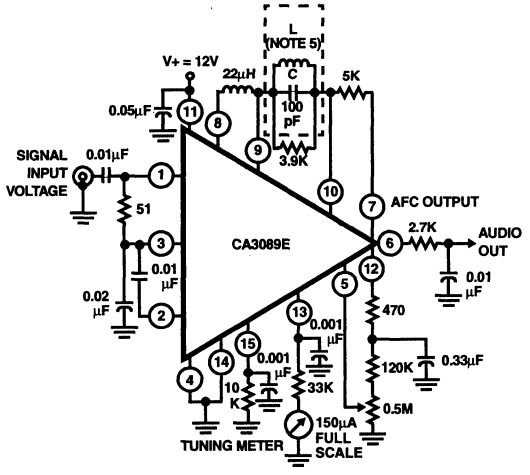


FIGURE 2. MUTING ACTION, TUNER AGC, AND TUNING METER OUTPUT vs INPUT SIGNAL VOLTAGE. (SEE TEST CIRCUIT FIGURE 3.)

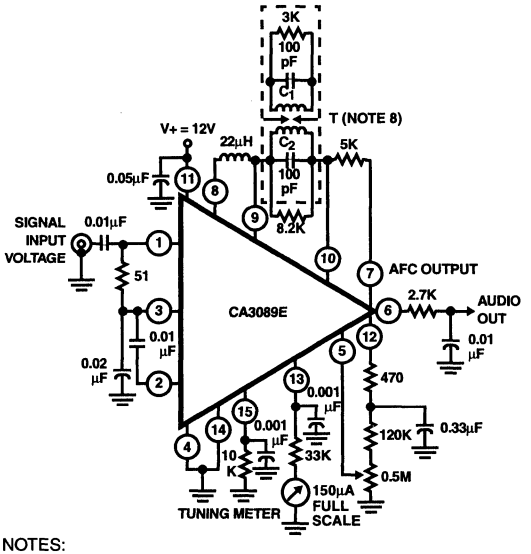
Test Circuits



NOTES:

4. All resistance values are in ohms.
5. L tunes with 100pF (C) at 10.7MHz.
6. Q_0 (unloaded) ≅ 75 (G.I. Automatic Mfg. Div. EX22741 or equivalent).

FIGURE 3. TEST CIRCUIT FOR CA3089E USING A SINGLE-TUNED DETECTOR COIL



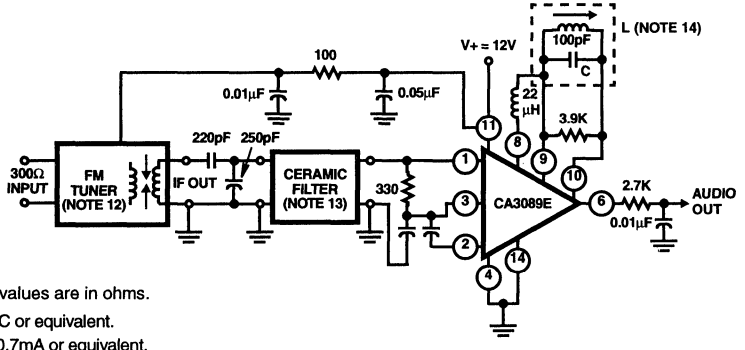
NOTES:

7. All resistance values are in ohms.
8. T PRI. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_1) 20↑ of 34e on $^7/_{32}$" dia. form).
9. SEC. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_2) 20↑ of 34e on $^7/_{32}$" dia. form).
10. kQ (percent of critical coupling) ≅ 70%.
    (Adjusted for coil voltage V_C) = 150mV.

Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm.

FIGURE 4. TEST CIRCUIT FOR CA3089E USING A DOUBLE-TUNED DETECTOR COIL

Typical Applications



NOTES:

11. All resistance values are in ohms.
12. Waller 4SN3FIC or equivalent.
13. Murata SFG 10.7mA or equivalent.
14. L tunes with 100pF (C) at 10.7MHz Q_0 unloaded ≅ 75 (G.I. EX22741 or equivalent).

Performance Data at f_O = 98MHz, f_{MOD} = 400Hz, Deviation = ±75kHz:

-3dB Limiting Sensitivity . . . . . 2µV (Antenna Level)
20dB Quieting Sensitivity . . . . . 1µV (Antenna Level)
30dB Quieting Sensitivity . . . . . 1.5µV (Antenna Level)

FIGURE 5. TYPICAL FM TUNER USING THE CA3089E WITH A SINGLE TUNED DETECTOR COIL

Typical Applications (Continued)

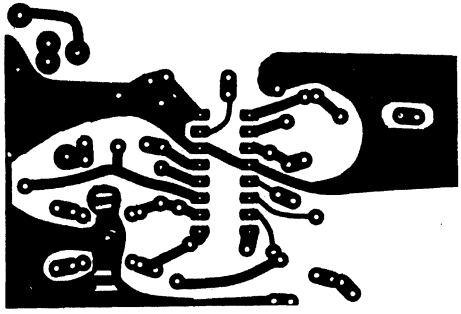
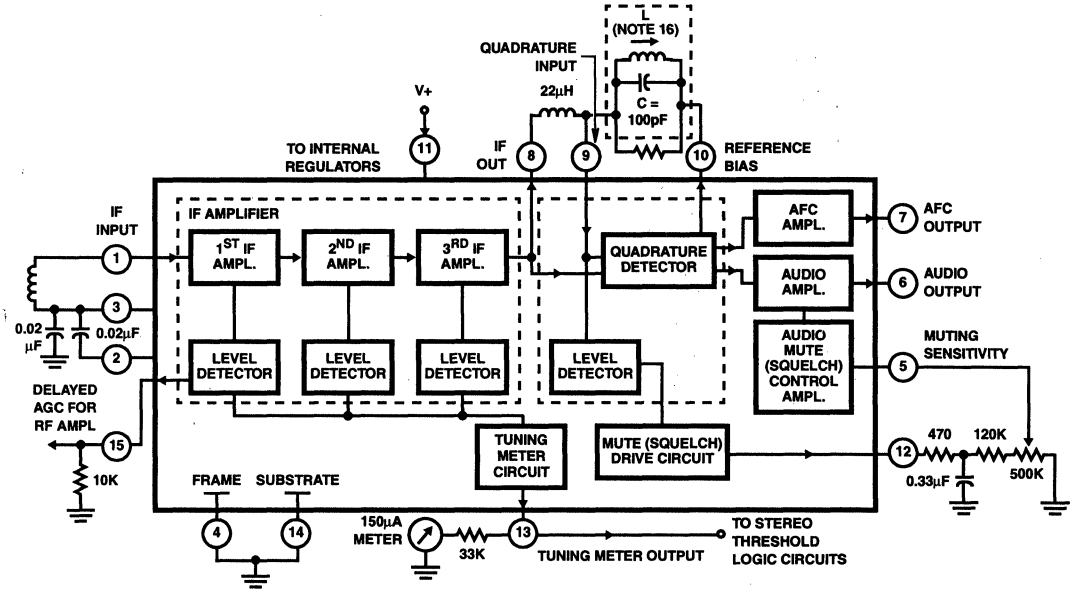


FIGURE 6A. BOTTOM VIEW OF PRINTED CIRCUIT BOARD

FIGURE 6B. COMPONENT SIDE - TOP VIEW

FIGURE 6. ACTUAL SIZE PHOTOGRAPHS OF THE CA3089E AND OUTBOARD COMPONENTS MOUNTED ON A PRINTED-CIRCUIT BOARD

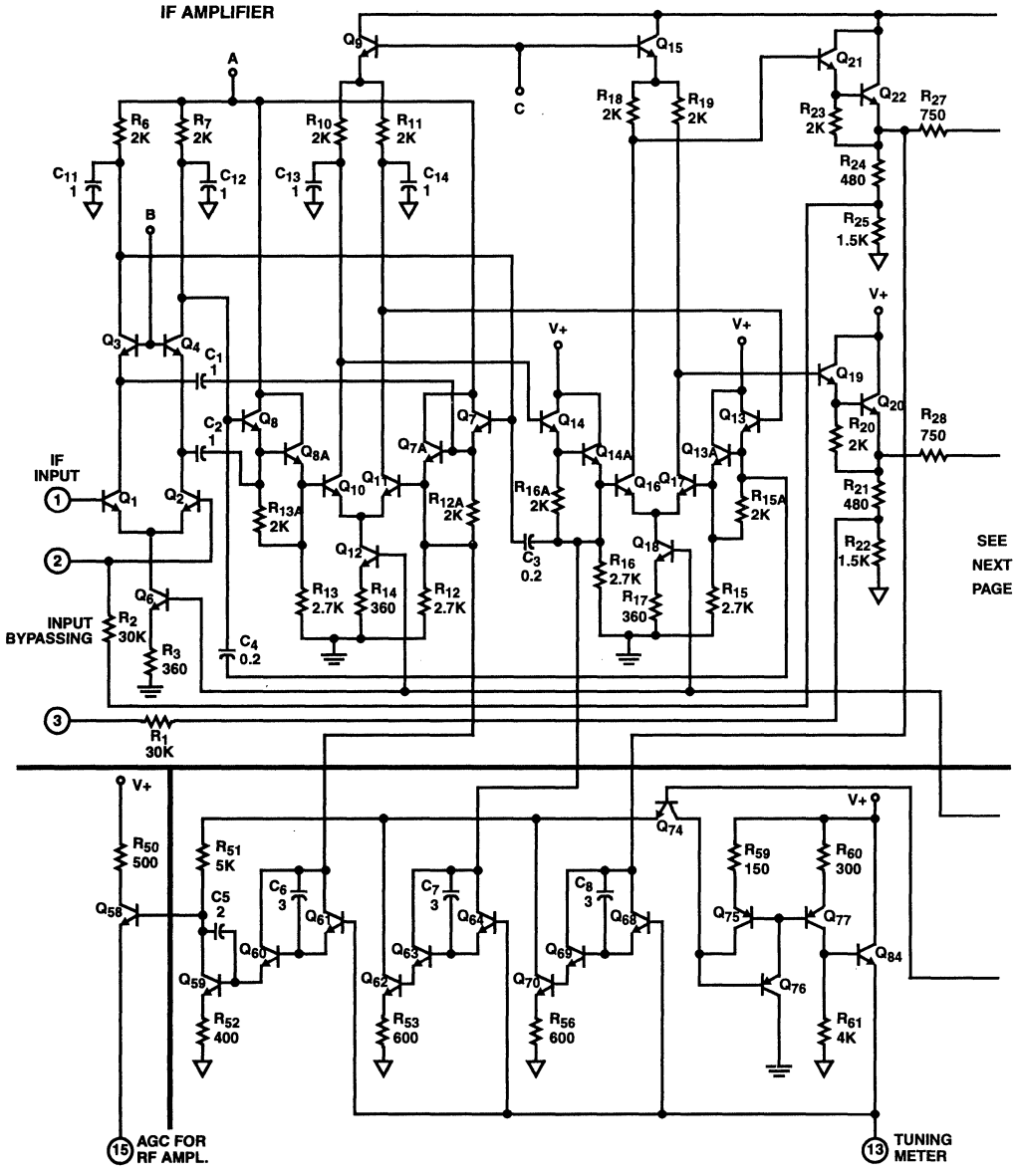
Block Diagram



NOTES:

15. All resistance values are in ohms.
16. L Tunes with 100pF (C) at 10.7MHz.
17. $Q_O \cong 75$ (G.I. EX22741 or equivalent).
18. Pin numbers refer to 16 lead DIP.

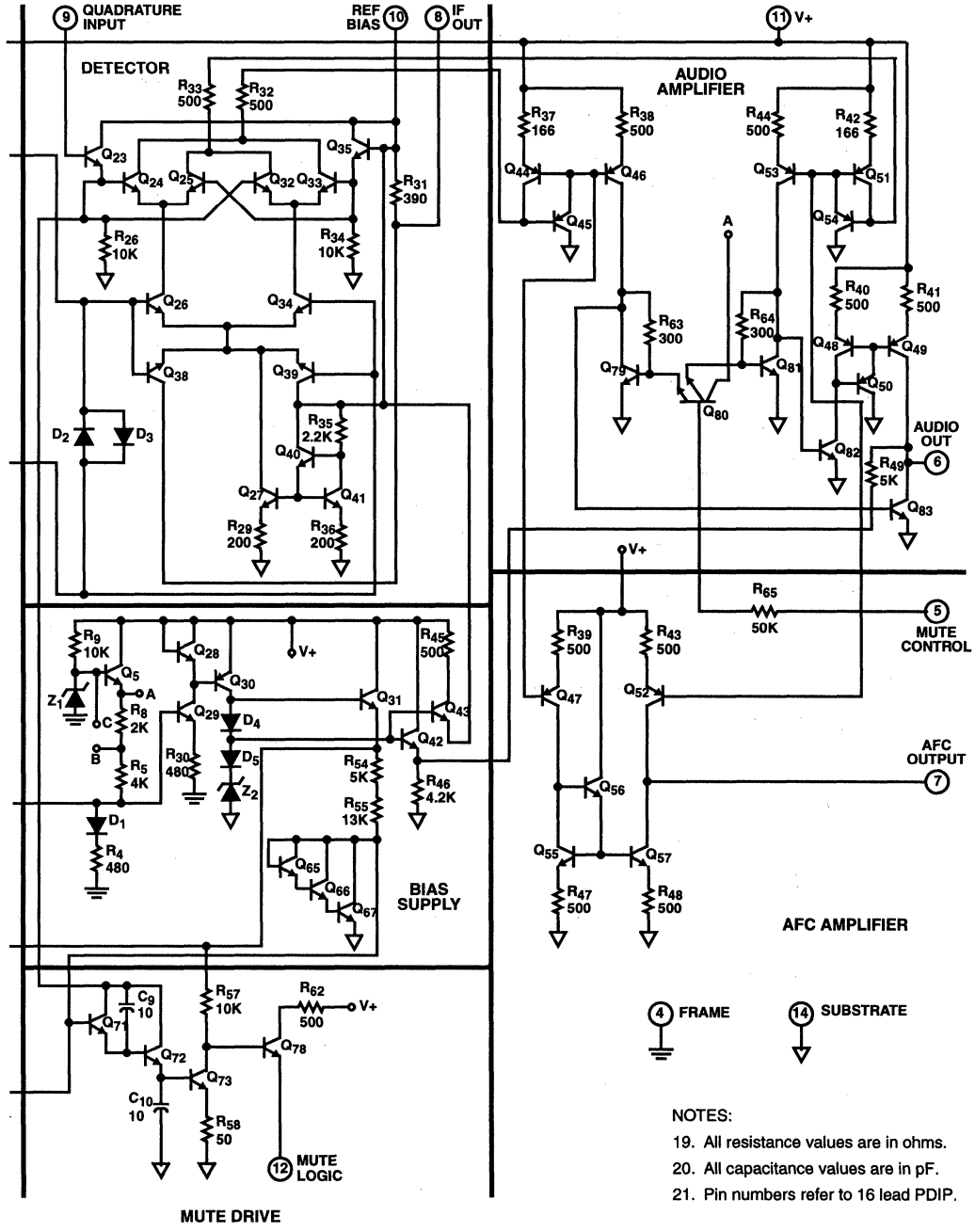
Schematic Diagram



NOTE: Pin numbers refer to 16 lead PDIP.

LEVEL DETECTOR AND METER CIRCUIT

Schematic Diagram (Continued)



NOTES:

19. All resistance values are in ohms.
20. All capacitance values are in pF.
21. Pin numbers refer to 16 lead PDIP.

HARRIS SEMICONDUCTOR

CA3126

November 1996

TV Chroma Processor

Features

- Phase Locked Subcarrier Regeneration Utilizes Sample-and-Hold Techniques
- Automatic Chrominance Control (ACC)/Killer Detector Employs Sample-and-Hold Techniques
- Supplementary ACC with an Overload Detector to Prevent Oversaturation of this Picture Tube
- Sinusoidal Subcarrier Output
- Keyed Chroma Output
- Emitter Follower Buffered Outputs for Low Output Impedance
- Linear DC Saturation Control

Applications

- TV/CATV Receiver Circuits
- NTSC Color Decoder/Processor
- Computer Graphics Subcarrier Regenerator
- Timing Reference for Frame Grabbers
- DSP Clock Timing Reference Source

Description

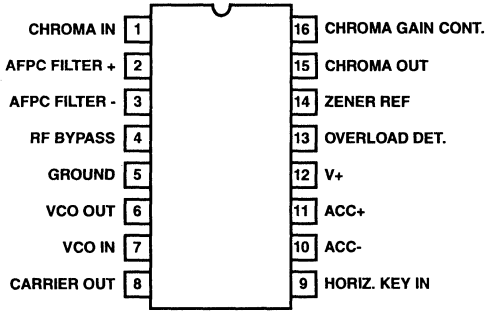
The Harris CA3126 is a monolithic silicon integrated circuit designed for TV chroma processing and is ideally suited for NTSC color graphic applications that require subcarrier regeneration of the color burst signal.

Ordering Information

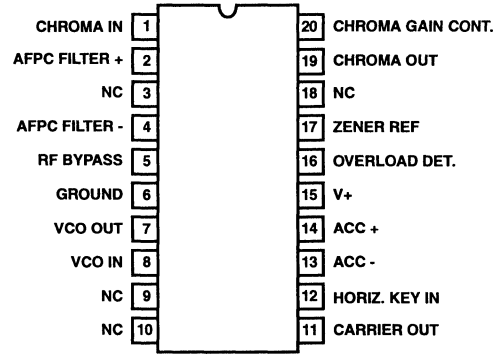
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3126E	-40 to 85	16 Ld PDIP	E16.3
CA3126M1	-40 to 85	20 Ld SOIC	M20.3

Pinouts

CA3126
(PDIP)
TOP VIEW



CA3126
(SOIC)
TOP VIEW



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 860.4

Absolute Maximum Ratings

DC Supply Voltage (V+ to GND) (Note 1) 13.2V
DC Current:
Into V+ Pin 38mA
Into Zener Reference Pin 20mA
DC Voltage (Horizontal Key In)
Negative Rating . . . . . -5V
Positive Rating 3V

Operating Conditions

Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{o}C/W$)
PDIP Package	100
SOIC Package	85

Maximum Junction Temperature (Plastic Packages) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. This rating does not apply when using the internal zener reference in conjunction with an external pass transistor.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

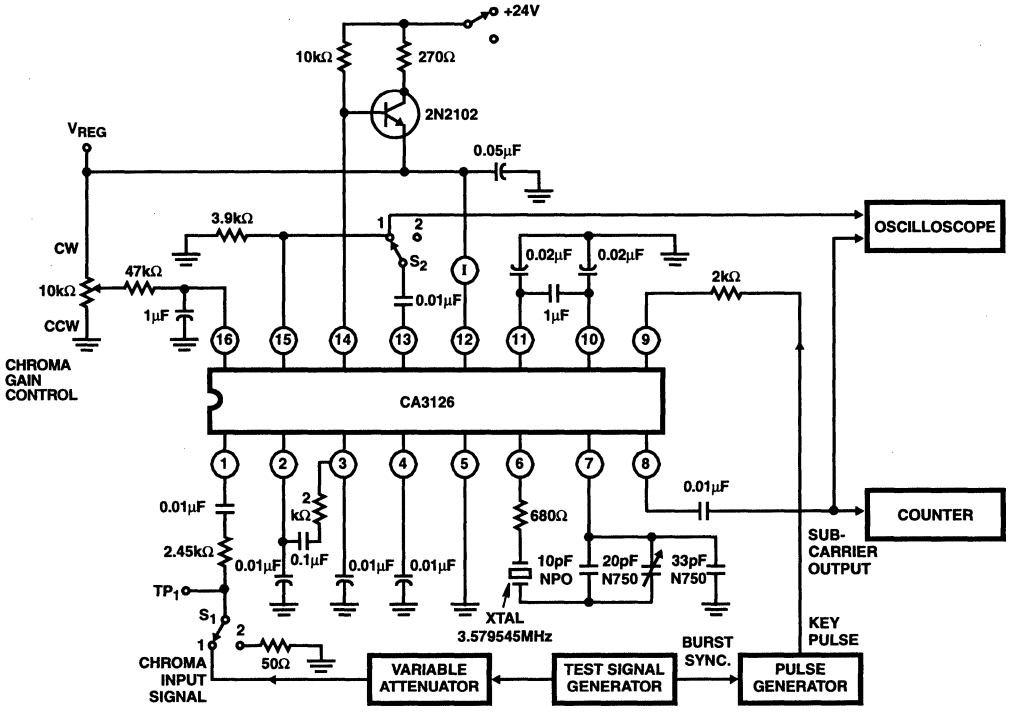
$T_A = 25^{o}C$, Chroma Gain Control at maximum position for all tests except as noted. Electrical specifications referenced to test circuit.

PARAMETER	TERMINAL, MEASUREMENT AND SYMBOL	SWITCH POS. S_1	SWITCH POS. S_2	V_{CHROMA} INPUT TP_1	MIN	TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS								
Voltage Regulator	V_{12}	2	2	0	10.1	11.2	12.1	V
Supply Current	I_{12}	2	2	0	16	25	38	mA
SWITCHING ELECTRICAL SPECIFICATIONS (Note 3)								
Pull-In Range (Note 4)	V_8	(Note 6)	2	$0.5V_{P-P}$	±250	-	-	Hz
Oscillator Output	V_8	2	2	0	0.6	1.0	-	V_{P-P}
100% Chroma Output	V_{15}	1	2	$0.5V_{P-P}$	1.4	2.7	-	V_{P-P}
Overload Detector	V_{15}	1	1	$0.5V_{P-P}$	0.4	-	0.7	V_{P-P}
Minimum Chroma Output (Note 5)	V_{15}	1	2	$0.5V_{P-P}$	-	-	20	mV_{P-P}
200% Chroma Output	V_{15}	1	2	$1V_{P-P}$	70	100	140	% of 100% Reading
20% Chroma Output	V_{15}	1	2	$0.1V_{P-P}$	40	-	105	
Kill Level	V_{TP1}	1	2	Vary	5	-	60	mV_{P-P}

NOTES:

3. Except for pull-in range testing, tune oscillator trimmer capacitor for free running frequency of 3.579545MHz ±10Hz.
4. Set Switch 1 to Position 2, detune oscillator ±250Hz, set Switch 1 to Position 1, and check for oscillator pull-in.
5. Set Chroma Gain Control to minimum position (CCW).

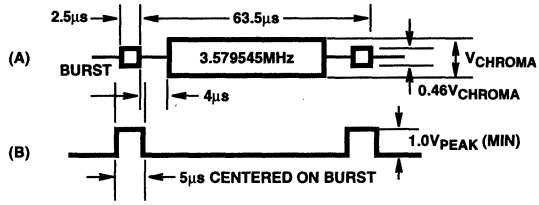
Test Circuit



Pin numbers refer to the PDIP package.

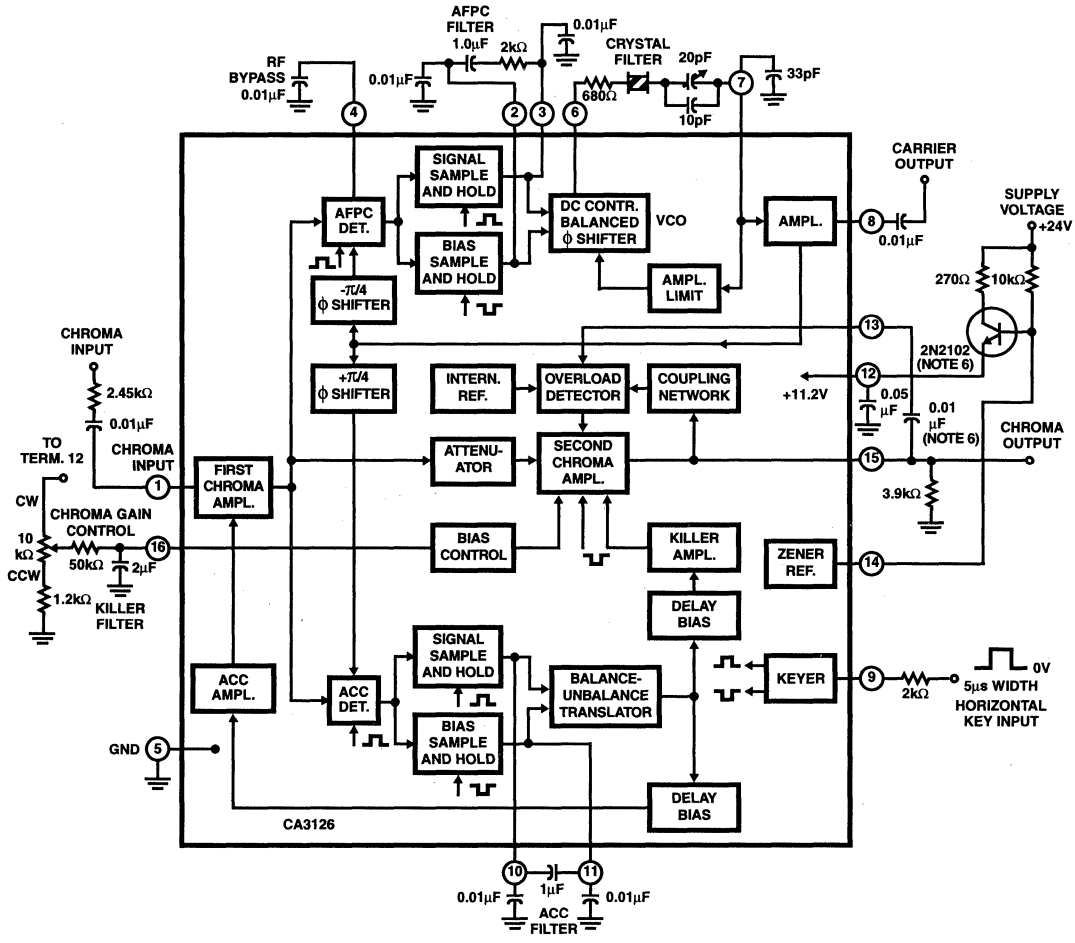
(A) Chroma input signal

(B) Key pulse input signal



Block Diagram

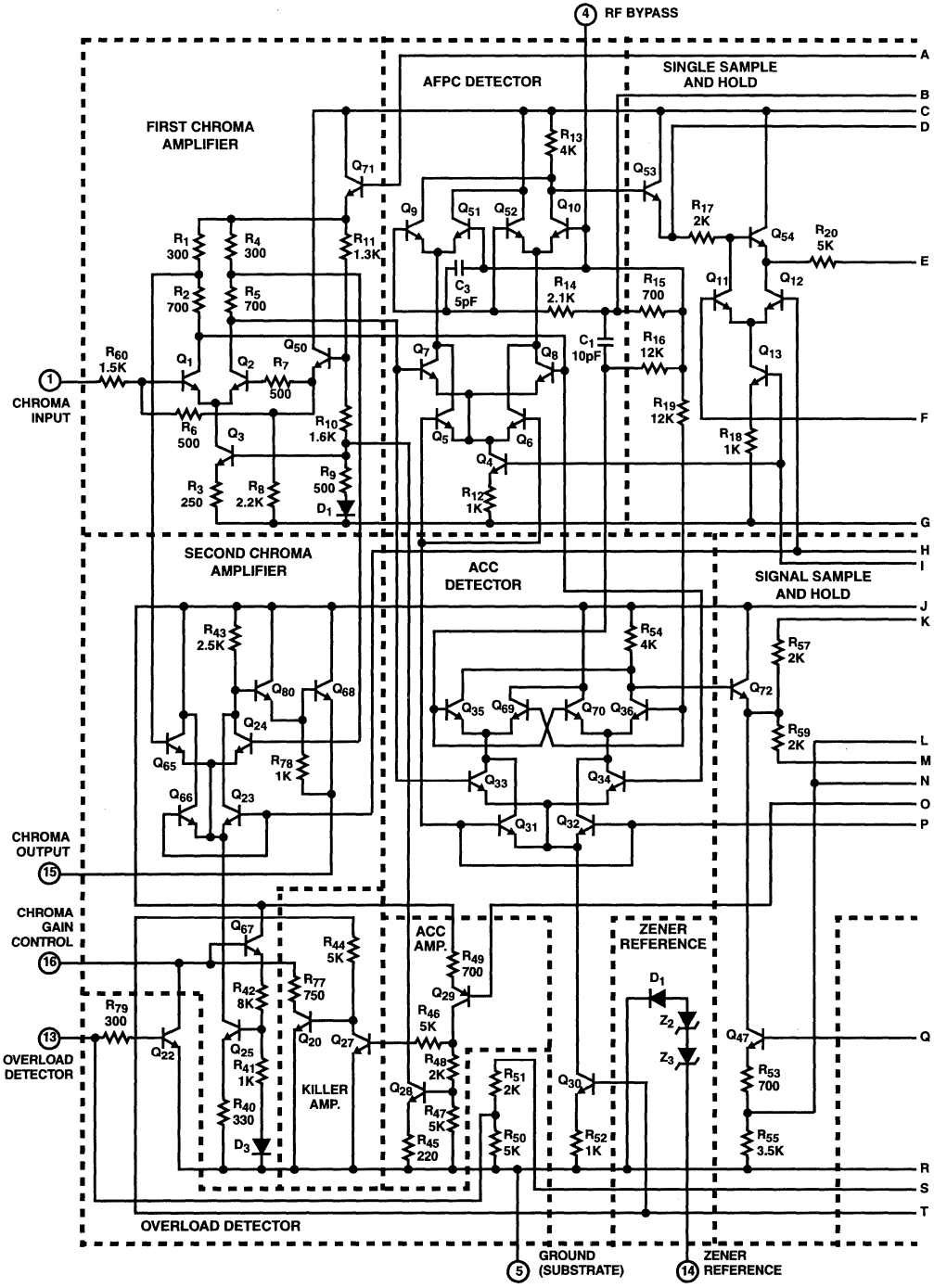
TV CHROMA PROCESSOR



NOTES:

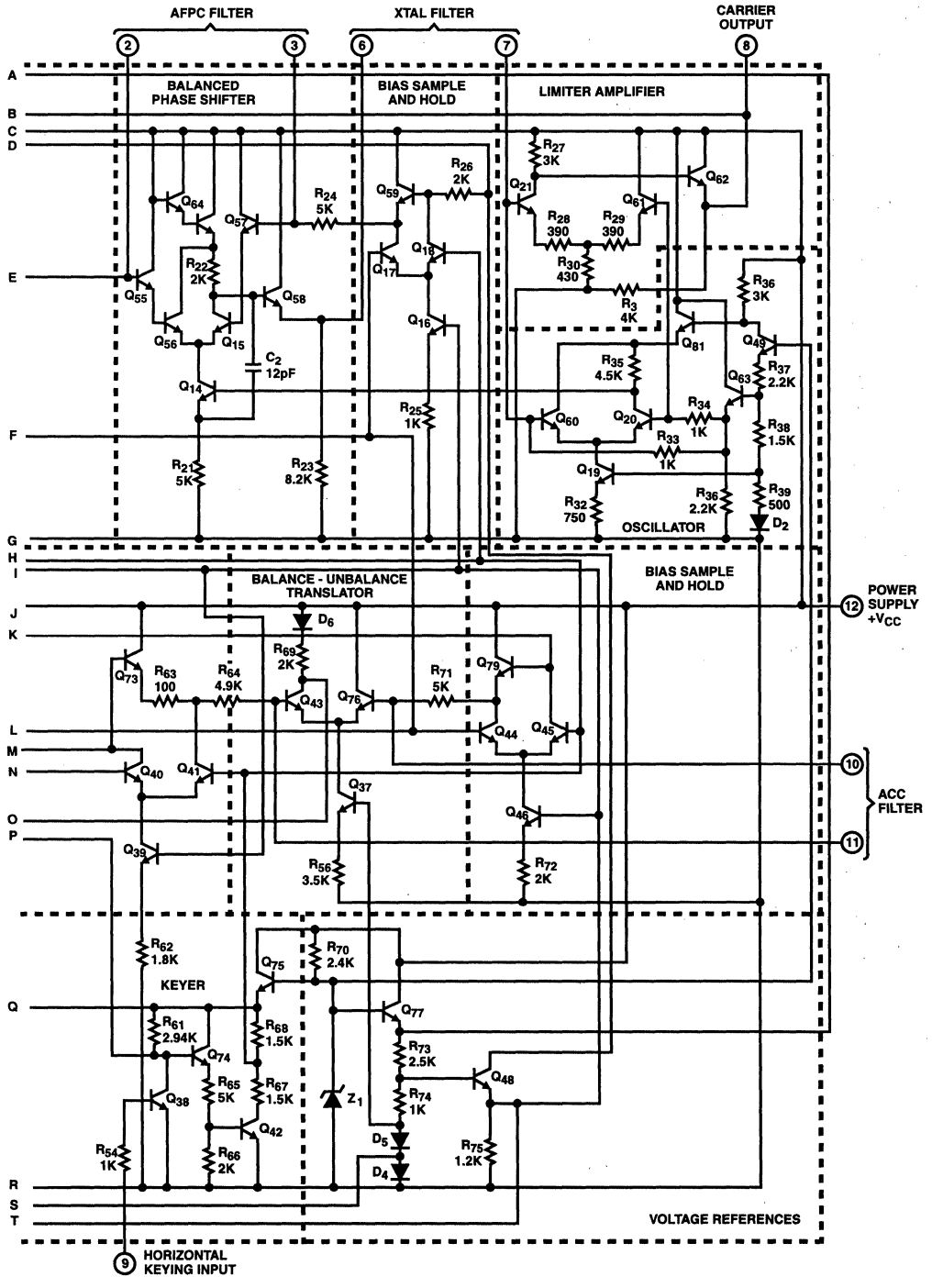
6. Optional design features.
7. Pinout numbers refer to the PDIP package.

Schematic Diagram



NOTE: Pin numbers refer to the PDIP Package. Resistance values are in ohms.

Schematic Diagram (Continued)



Application Information

Circuit Description (Pin numbers refer to the DIP package.)

The following paragraphs briefly describe the circuit operation of the CA3126 (shown in the Block Diagram and Schematic Diagram). A detailed description of the operation of various portions of the CA3126 is given in AN6247, "Application of the CA3126 Chroma-Processing IC Using Sample-and-Hold Techniques".

The chroma input is applied to Terminal 1 through the desired band-shaping network. A 2,450Ω resistor should be placed in series with Terminal 1 to minimize oscillator pickup in the first chroma amplifier. This amplifier supplies signals to the second chroma amplifier and to the ACC and AFPC detectors. The first chroma amplifier is gain-controlled by the ACC amplifier.

A horizontal keying pulse is applied to Terminal 9. This pulse must be present to ensure proper operation of the oscillator circuit. The subcarrier burst is sampled during the keying interval in the AFPC detector. The error voltage, produced at Terminal 2 and proportional to the burst phase, is compared to the quiescent bias voltage at Terminal 3 by the sample-and-hold circuitry. This "compared" voltage controls the phase- shifting network in the phase-locked loop. The operation of the AFPC loop is independent of any external adjustments or voltages except for an initial capacitor adjustment to set the free-running frequency.

The regenerated oscillator signal at Terminal 8 is applied internally to the AFPC and ACC detectors through +45 and -45-degree phase-shifter networks to establish the proper phase relationship for these detectors. The ACC detector, which also samples the burst during the keying interval, produces a correction voltage proportional to the burst amplitude. The correction voltage is compared to the quiescent bias level using sample-and-hold circuitry similar to that used in the AFPC portion of the circuit. The "compared" voltage is applied internally to the ACC amplifier and killer amplifier. Because the amplifier gains and killer threshold are determined by the ratios of the internal resistors, these functions are independent of external voltages or controls.

The attenuated chroma signal is fed to the second chroma amplifier, where the burst is removed by keyer action. The killer amplifier, the chroma gain control, and the overload detector control the action of the second chroma amplifier, whose gain is proportional to the dc voltage at Terminal 16. The overload detector (Terminal 13) receives a sample of the chroma output (Terminal 15) and detects the peak of the signal. The detected voltage is stored in an external capacitor connected to Terminal 16. This stored voltage on Terminal 16 affects the gain of the second chroma in the same manner as the chroma gain control.

General Considerations

The block diagram shown is typical of the type of circuit used in the practical application of the CA3126. Several items are critical for proper operation of the circuit.

1. A series resistor of approximately 2,450Ω (or high source impedance) must be used at the chroma input, Terminal 1. This high impedance minimizes pickup of unbalanced currents, particularly of the subcarrier oscillator signal.
2. When the overload detector is used, a large resistor (nominally 47,000Ω) must be placed in series with Terminal 16 to set the required RC time constant. The same RC network series serves to set the killer time constant.
3. The setting of the free-running oscillator frequency requires the presence of the keying pulse. The free-running frequency will be erroneous if Terminal 1 is DC shorted during the setting operation because of the DC offset voltage introduced to the AFPC detector.
4. Care must be taken in PC board designs to provide reasonable isolation between the oscillator portion of the circuit (Terminals 6, 7, and 8) and the chroma input (Terminal 1).

Overload Detector

The overload detector accomplishes two purposes:

1. It prevents oversaturation due to low burst-to-chroma ratios.
2. It prevents overload conditions due to noise.

Both of these conditions are discussed in more detail in AN6247. The extent to which the overload detector is used depends upon the individual receiver design goals. If greater than $0.5V_{P-P}$ output is desired, the chroma output at Terminal 15 can be tapped to yield any desired degree of overload detector action.

Chroma Gain Control

The chroma gain control operates by varying the base bias on current source transistor Q_{25}. To ensure proper temperature tracking of the chroma gain control, it is essential that the control be operated from a supply source derived from the reference voltage at Terminal 12. Because the control operates from a current source, chroma gain is much more predictable and far less temperature sensitive than controls that steer current by means of a differential amplifier. The typical chroma gain characteristic for the CA3126 is shown in Figure 1.

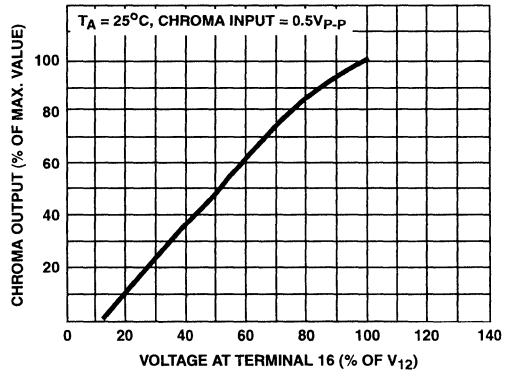


FIGURE 1. CHROMA GAIN CONTROL

Subcarrier Regenerator Oscillator

The oscillator filter consists of a 3.579545MHz crystal, a 680Ω resistor, and a 10pF capacitor connected in series across Terminals 6 and 7. A 33pF capacitor, shunt connected from Terminal 7 to ground, rolls off higher order harmonics, thereby preventing oscillation at the crystal third-harmonic frequency. A

curve of the typical static phase error as a function of the free-running oscillator frequency is shown in Figure 2. It should be noted that the slope of the curve determines the DC gain of the phase-locked loop, i.e., 40Hz per degree.

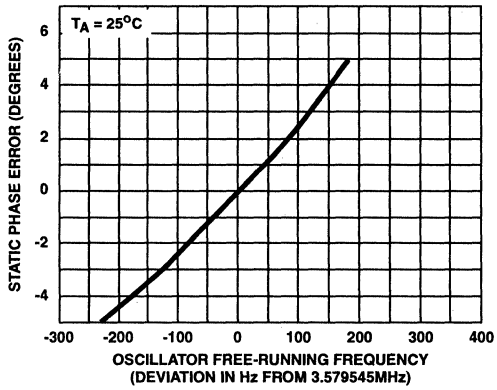


FIGURE 2. STATIC PHASE ERROR

Thermal Considerations

The circuit of the CA3126 is thermally compensated to achieve the optimal operating characteristics over the normal operating temperature range of TV receivers. Figures 3 and 4 show the oscillator and chroma-output amplitudes and phases as a function of temperature (Terminals 8 and 15), respectively.

Both the oscillator and chroma-output amplitudes and phases are measured relative to the chroma-input phase. The performance of the oscillator free-running frequency as a function of temperature is shown in Figure 5. All the temperature plots are characteristic of the test circuit with the indicated component types and values given.

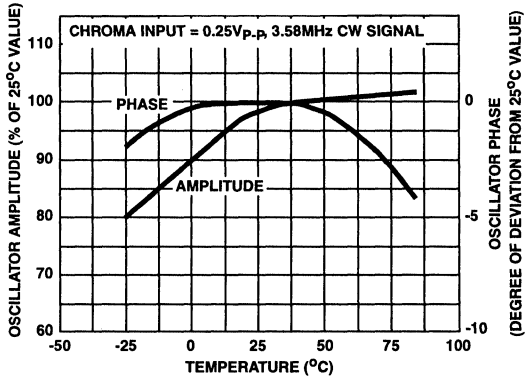


FIGURE 3. AMPLITUDE AND PHASE VARIATIONS OF OSCILLATOR OUTPUT vs TEMPERATURE

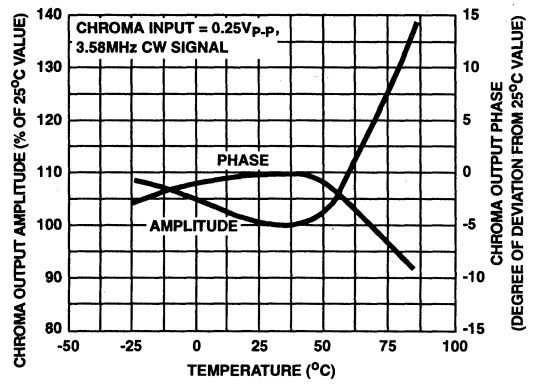


FIGURE 4. AMPLITUDE AND PHASE VARIATIONS OF CHROMA OUTPUT vs TEMPERATURE

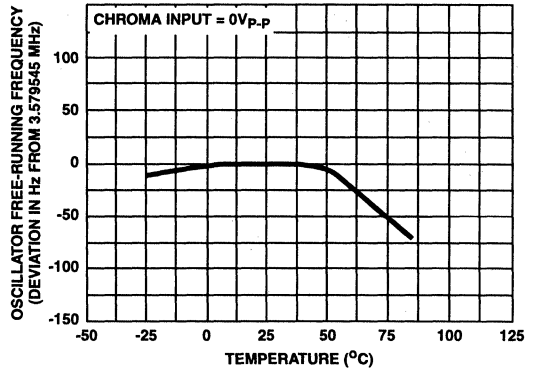
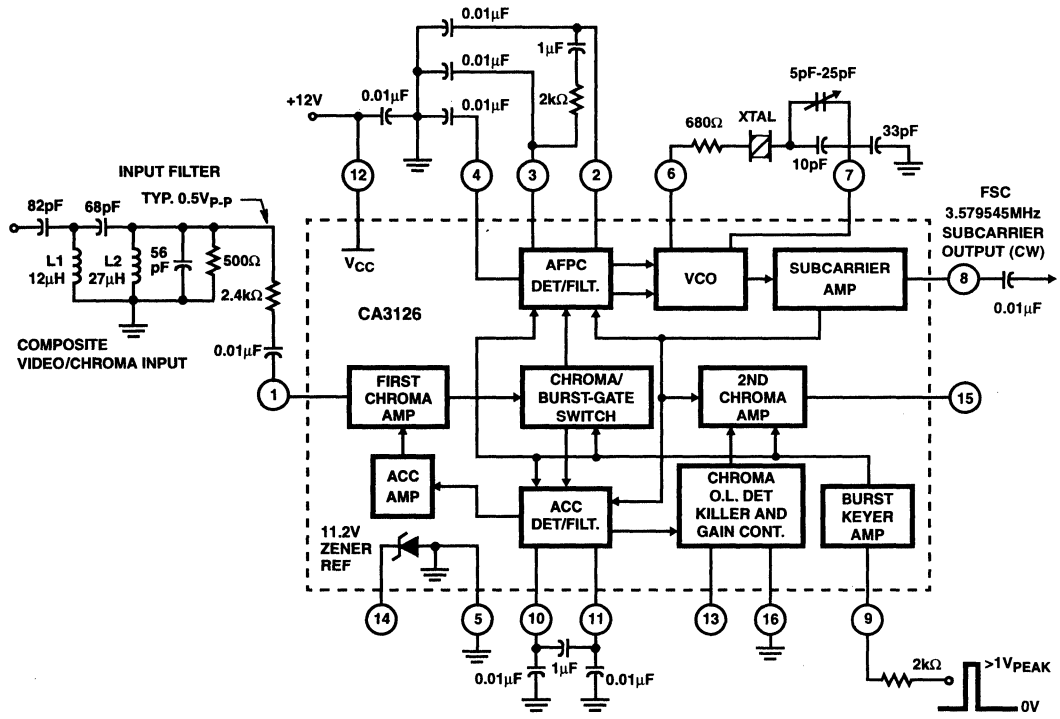


FIGURE 5. VARIATION OF OSCILLATOR FREE RUNNING FREQUENCY vs TEMPERATURE



NOTE: For Subcarrier Regenerator, the second chroma amp is not used; Pins 13,14, and 15 are not connected and pin 16 is grounded.

FIGURE 6. TYPICAL APPLICATION OF THE CA3126 AS A SUBCARRIER REGENERATOR

HARRIS SEMICONDUCTOR

CA3154

November 1996

TV Sync/AGC/Horizontal Signal Processor

Features

- Horizontal Oscillator with AFC
- Sync Separator with Noise Immunity
- Strobed AGC System
- IF AGC Output
- Delayed Outputs for Forward or Reverse AGC Tuners
- Internal Noise Threshold
- High-Impedance Video Input
- Choice of Dual External Time Constants for Sync Separator Noise Immunity
- RF AGC Delay Externally Controlled
- Output Short-Circuit Protection

Description

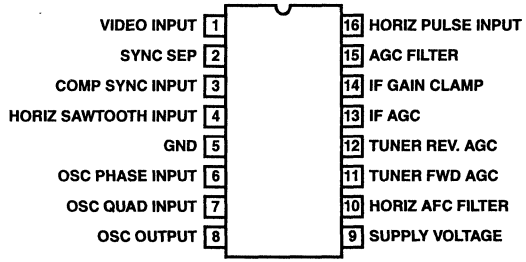
The CA3154 is a monolithic integrated circuit TV signal processor designed for use in color or monochrome receivers. Circuit functions include a horizontal oscillator with AFC, a sync separator, and a keyed AGC system. The AGC system provides output signals for IF (reverse) and tuner (forward and/or reverse). The wide frequency-range horizontal oscillator has high stability at 503.5kHz. When the CA3154 is used in conjunction with horizontal/vertical countdown circuits, the need for horizontal and vertical hold controls is eliminated.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3154E	-40 to 85	16 Ld PDIP	E16.3

Pinout

CA3154
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1183.1**

Absolute Maximum Ratings

DC Supply Voltage (V+ to V-) 15V

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)

PDIP Package 80

Maximum Junction Temperature (Plastic Package) . . . . . 150°C

Maximum Storage Temperature Range . . . . . -65°C to 150°C

Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Terminal 5 to GND, and Terminal 9 to +12V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS (TERMINALS CONNECTED AS SHOWN BELOW)	TEMP (°C)	MIN	TYP	MAX	UNITS
Power Supply Current	I_9	Measure (9)	25	10	-	22	mA
Video Inverter Voltage	V_2	(1) to +4V, (2) 12kΩ to GND, (3) 27kΩ to GND, Measure (2)	25	5.2	-	6.4	V
Sync Separator High Output Voltage	V_{3H}	(1) to +4V, (2) 12kΩ to GND, (3) 27kΩ to GND, Measure (2)	25	10.7	-	-	V
Sync Separator Low Output Voltage	V_{3L}	(1) to +4V, (3) 27kΩ to GND, Measure (3)	25	-	-	1.3	V
Video Noise Clamp Voltage	V_3 Clamp	(1) to +3.1V, (3) 27kΩ to GND, Measure (3)	25	10.7	-	-	V
AGC Discharge Current	I_{15} Discharge	(1) to +4.4V, (2) 10kΩ to GND, (15) 470Ω to +6V, (16) 27kΩ to 12V, Measure (15)	25	0.6	-	1.4	mA
AGC Charge Current	I_{15} Charge	(1) to +3.45V, Otherwise, Same as Above	25	-2.1	-	-4.8	mA
AGC Comparator Leakage	I_{15} Leakage	(1) to +3.45V, (2) 10kΩ to GND, (15) 4.7kΩ to +6V, Measure (15)	25	-20	-	20	µA
AGC Threshold Voltage	V_{1TH}	Adj. (1) for $I_{15} = 0 \pm 0.1$mA, (2) 10kΩ to GND, (15) 4.7kΩ to +6V, (16) 27kΩ to +12V, Measure (1)	25	3.8	4	4.3	V
Minimum IF AGC	V_{13L}	(11) 10kΩ to GND, (12) 10kΩ to +12V, (13) 22kΩ to +5V, (14) 1kΩ to +2.95V, (16) 1kΩ to +2.2V, Measure (13)	25	0.75	-	1.25	V
Forward Tuner AGC Leakage Current	I_{11} Leakage	(11) 10kΩ to GND, (12) 10kΩ to 12V, (13) 2.2kΩ to +5V, (14) 1kΩ to +2.95V, (15) 1kΩ to +5.3V, Measure (11)	25	-20	-	20	µA
Reverse Tuner AGC Leakage	I_{12} Leakage	Same as Above, but Measure (12)	25	-10	-	10	µA
IF AGC High Voltage	V_{13H}	Same as Above, but Measure (13)	25	3.65	-	4.15	V
Forward Tuner AGC Low Voltage	V_{11L}	(11) 3.6kΩ to GND, (12) 3.16kΩ to +12V, (13) 2.2kΩ to +5V, (14) 1kΩ to +2.95V, (15) 1kΩ to +7.9V, Measure (11)	25	0.8	-	3.2	V
Reverse Tuner AGC Low Voltage	V_{12L}	Same as Above, but Measure (12)	25	1.65	-	3.25	V
Maximum IF AGC Voltage	V_{13H}	(11) 10kΩ to GND, (12) 10kΩ to +12V, (13) 2.2kΩ to +5V, (14) 1kΩ to +2.95V, (15) 1kΩ to +7.9V, Measure (13)	25	4.85	-	5.2	V
Phase Detector Leakage Current	I_{10L}	(2) 10kΩ to GND, (3) to GND, (4) 5kΩ to +3.8V, (10) 10kΩ to +6V, Limit GND at (3) to 10s, Measure 10	25	-5	-	5	µA

Electrical Specifications Terminal 5 to GND, and Terminal 9 to +12V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS (TERMINALS CONNECTED AS SHOWN BELOW)	TEMP (°C)	MIN	TYP	MAX	UNITS
Phase Detector Bias Voltage	V_4		25	2.65	-	3.1	V
Oscillator Output Voltage	V_6	Connect Oscillator Loop Shown in Test Circuit to (6), (7), (8); (3) to GND for 10s Max, Measure (6)	25	0.6	-	1.6	V_{P-P}
Oscillator Free-Running Frequency	f_{6FR}	Same as Above	25	475	-	535	kHz
Oscillator Frequency High	f_{6H}	Connect Oscillator Circuit Shown in Test Circuit to (10), (7), (8); (2) 10kΩ to GND, (4) 5kΩ to +18V, Measure (6)	25	520	-	-	kHz
Oscillator Frequency Low	f_{6L}	Same as Above, Except (4) 5kΩ to +3.8V	25	-	-	485	kHz
Sync Separator Short Circuit	I_3 Max	(3) 10Ω to GND for 10s Max	25	-	-	40	mA
Oscillator Output Short Circuit	I_8 Max	(8) 10Ω to GND for 10s Max (3) 10Ω to GND for 10s Max	25	-	-	130	mA

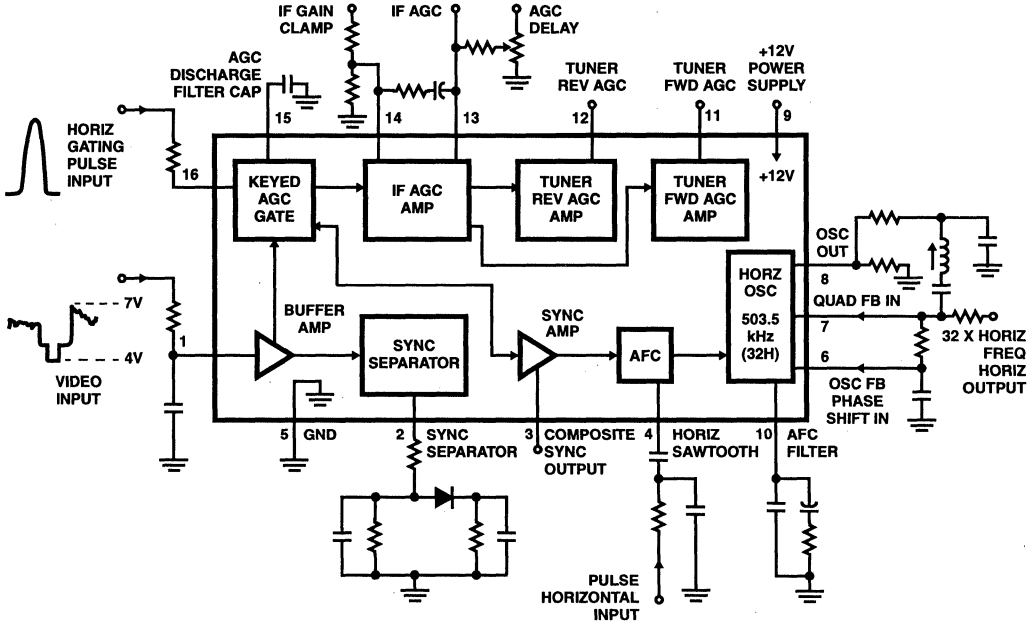
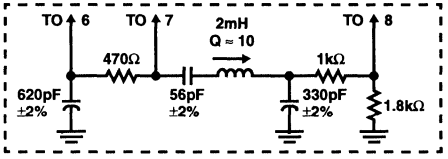


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF CA3154



NOTE: Oscillator loop to be used as indicated in the electrical characteristics chart, with coil adjusted for typical unit to 503.5kHz for f_{6FR}.

FIGURE 2. ELECTRICAL CHARACTERISTICS TEST CIRCUIT

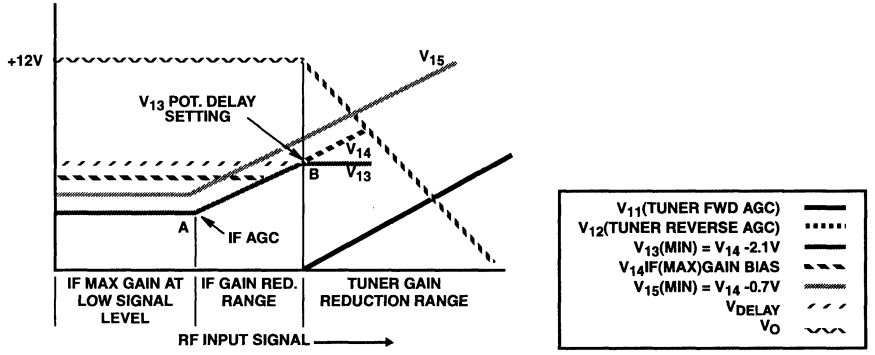


FIGURE 3. TYPICAL OPERATION OF AGC CIRCUITS USING THE CA3154

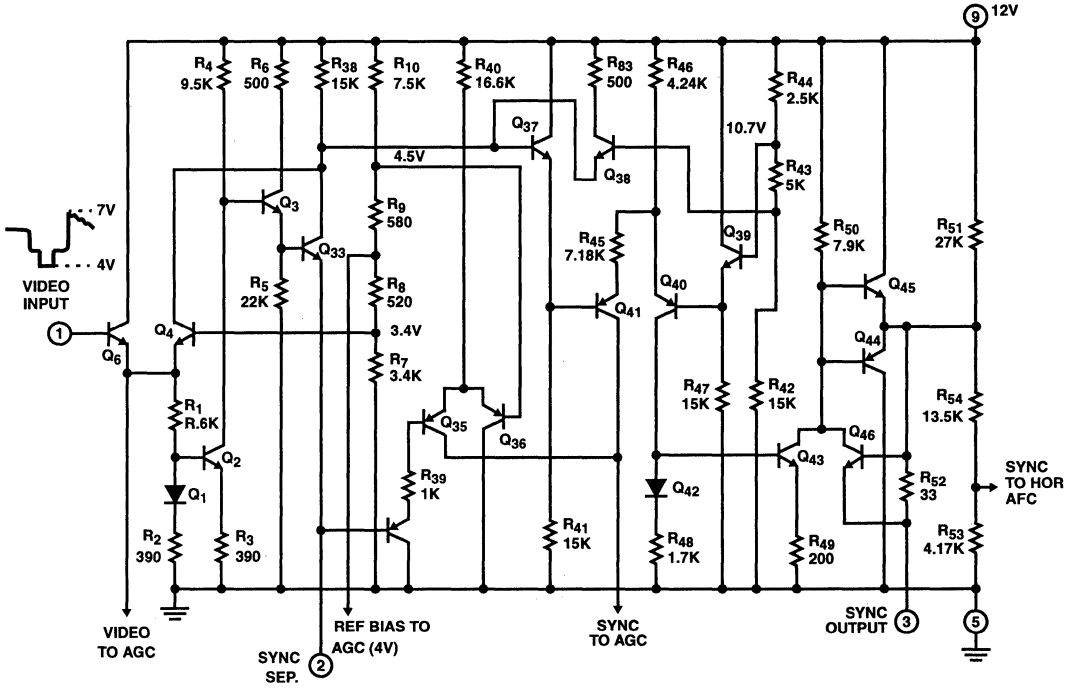


FIGURE 4. SCHEMATIC OF SYNC SEPARATOR SECTION OF THE CA3154

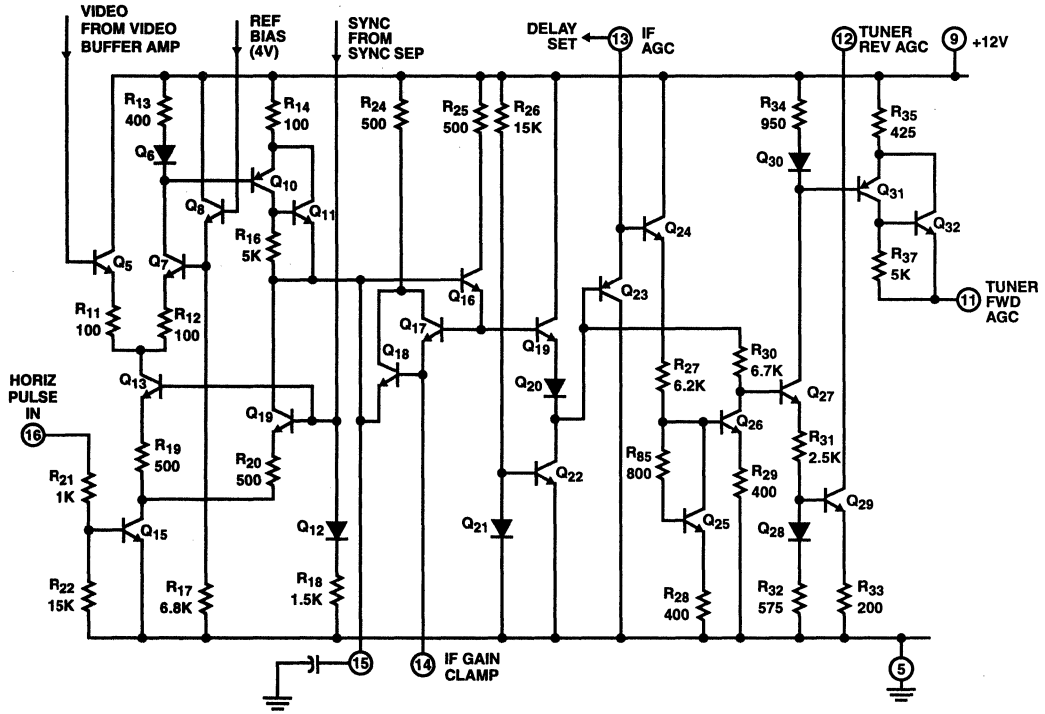


FIGURE 5. SCHEMATIC OF AGC SECTION OF THE CAA3154

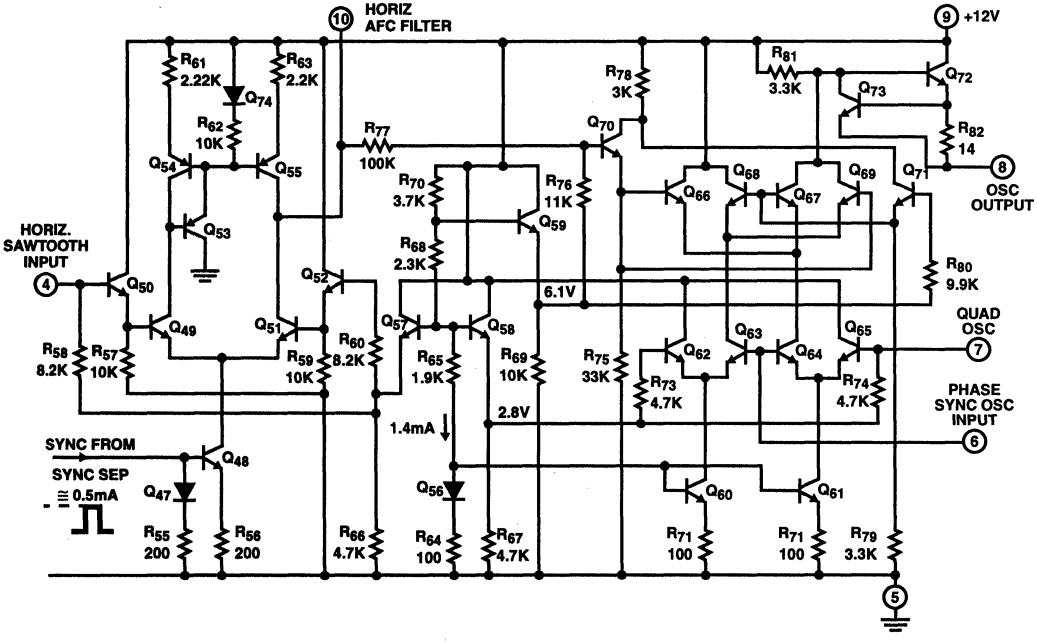


FIGURE 6. SCHEMATIC OF AFC-OSCILLATOR SECTION OF THE CA3154

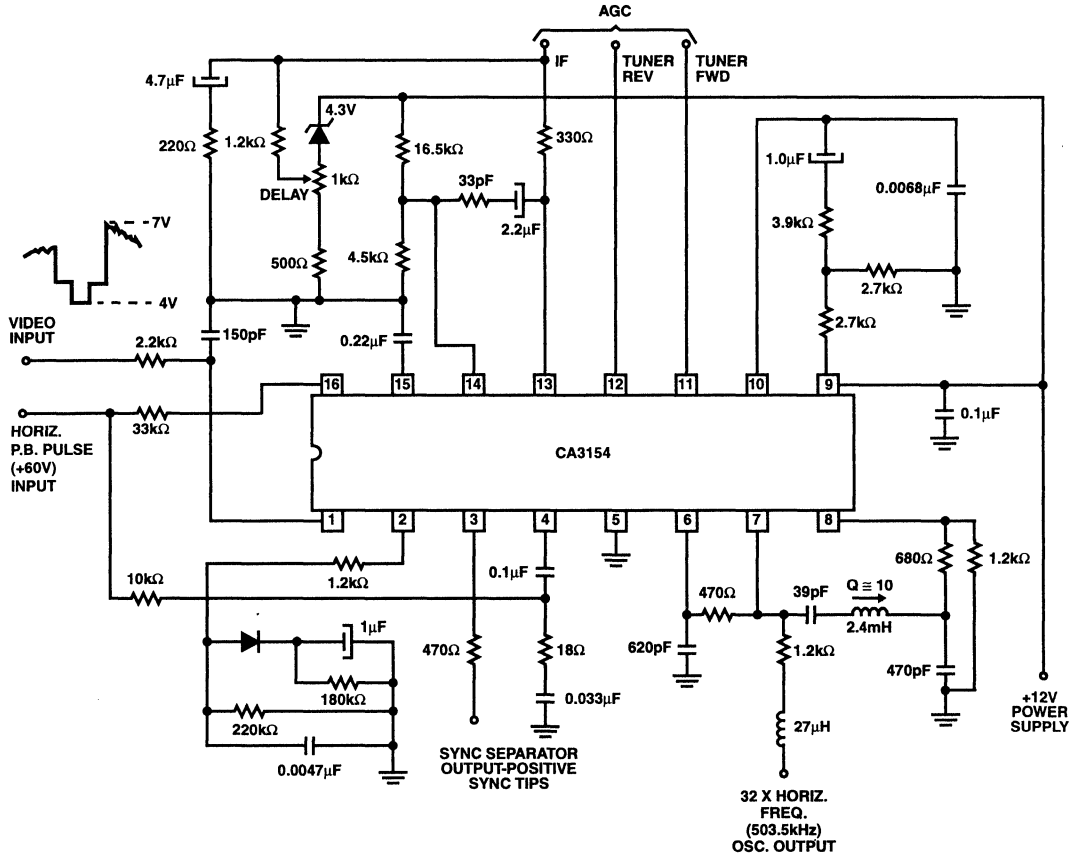


FIGURE 7. TYPICAL APPLICATION OF THE CA3154

HARRIS SEMICONDUCTOR

CA3189

November 1996

FM IF System

Features

- Includes IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Tuning Meter, Deviation-Noise Muting, and ON Channel Detector
- FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers
- Exceptional Limiting Sensitivity -12μV (Typ) at -3dB Point
- Low Distortion -0.1% (Typ) (with Double-Tuned Coil)
- Single-Coil Tuning Capability
- Improved S + N/N Ratio
- Externally Programmable Recovered Audio Level
- Provides Specific Signal for Control of Interchannel Muting (Squelch)
- Provides Specific Signal for Direct Drive of a Tuning Meter
- On Channel Step for Search Control
- Provides Programmable AGC Voltage for RF Amplifier
- Provides a Specific Circuit for Flexible Audio Output
- Internal Supply Voltage Regulators
- Externally Programmable "On" Channel Step Width, and Deviation at Which Muting Occurs

Description

The Harris CA3189E is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. The block diagram of the CA3189E includes a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power-supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16V.

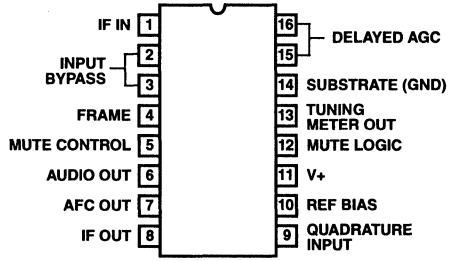
The CA3189E is ideal for high-fidelity operation. Distortion in a CA3189E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil. The CA3189E has all the features of the CA3089E plus additions. See CA3189E features compared to the CA3089E in Table 1.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3189E	-40 to 85	16 Ld PDIP	E16.3

Pinout

CA3189
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 1046.3

Absolute Maximum Ratings

DC Supply Voltage
(Between Terminals 11 and 4) 16V
(Between Terminals 11 and 14) 16V
DC Current (Out of Terminal 15) 2mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	90

Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s)..... 300°C

Operating Conditions

Temperature Range ..... -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25°C$, V+ = 12V

PARAMETER	SYMBOL	TEST CONDITIONS		CIRCUIT OR FIG. NO.	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS								
Quiescent Circuit Current	I_{11}	No Signal Input, Non Muted		1, 2	20	31	40	mA
DC Voltages		No Signal Input, Non Muted						
Terminal 1 (IF Input)	V_1			1, 2	1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2			1, 2	1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3			1, 2	1.2	1.9	2.4	V
Terminal 15 (RF AGC)	V_{15}			1, 2	7.5	9.5	11	V
Terminal 10 (DC Reference)	V_{10}			1, 2	5	5.6	6	V
DYNAMIC SPECIFICATIONS								
Input Limiting Voltage (-3dB Point)	V_I(lim)		f_O = 10.7MHz, $f_{MOD.}$ = 400Hz, Deviation ±75kHz	1, 2	-	12	25	µV
AM Rejection (Terminal 6)	AMR	V_{IN} = 0.1V, AM Mod. = 30%		1, 2	45	55	-	dB
Recovered AF Voltage (Terminal 6)	V_O(AF)			1, 2	325	500	650	mV
Total Harmonic Distortion (Note 2)								
Single Tuned (Terminal 6)	THD	V_{IN} = 0.1V		1	-	0.5	1	%
Double Tuned (Terminal 6)	THD			2	-	0.1	-	%
Signal Plus Noise to Noise Ratio (Terminal 6)	S + N/N	V_{IN} = 0.1V		1, 2	65	72	-	dB
Deviation Mute Frequency	f_{DEV}		f_{MOD} = 0	1, 5, 6	-	±40	-	kHz
RF AGC Threshold	V_{16}			1, 2	-	1.25	-	V
On Channel Step	V_{12}	V_{IN} = 0.1V	f_{DEV} < ±40kHz	1	-	0	-	V
			f_{DEV} > ±40kHz	1	-	5.6	-	V

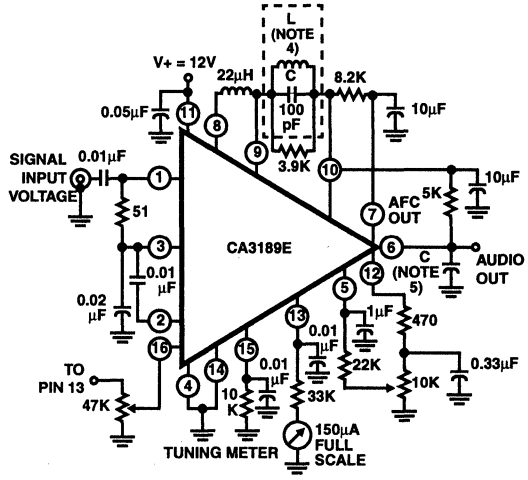
NOTE:

2. THD characteristics are essentially a function of the phase characteristics of the network connected between Terminals 8, 9, and 10.

TABLE 1. CA3189E FEATURES COMPARED TO CA3089E

FEATURES	CA3189E	CA3089E
Low Limiting Sensitivity (12μV Typ)	Yes	Yes
Low Distortion	Yes	Yes
Single-Coil Tuning Capability	Yes	Yes
Programmable Audio Level	Yes	No
S/N Mute	Yes	Yes
Deviation Mute	Yes	No
Flexible AFC	Yes	Yes
Programmable AGC Threshold and Voltage	Yes	No
Typical S + N/N > 70 dB	Yes	No
Meter Drive Voltage Depressed at Very Low Signal Levels	Yes	No
On-Channel Step Control Voltage	Yes	No

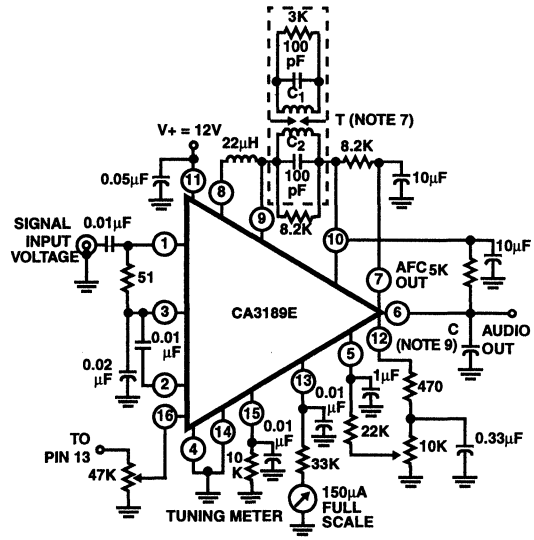
Test Circuits



NOTES:

3. All resistance values are in ohms.
4. L tunes with 100pF (C) at 10.7MHz. Q_0 (unloaded) ≅ 75 (TOKO No. KACS K586HM or equivalent).
5. C = 0.01μF for 50μs deemphasis (Europe). C = 0.015μF for 75μs deemphasis (USA).

FIGURE 1. TEST CIRCUIT FOR CA3189E USING A SINGLE-TUNED DETECTOR COIL

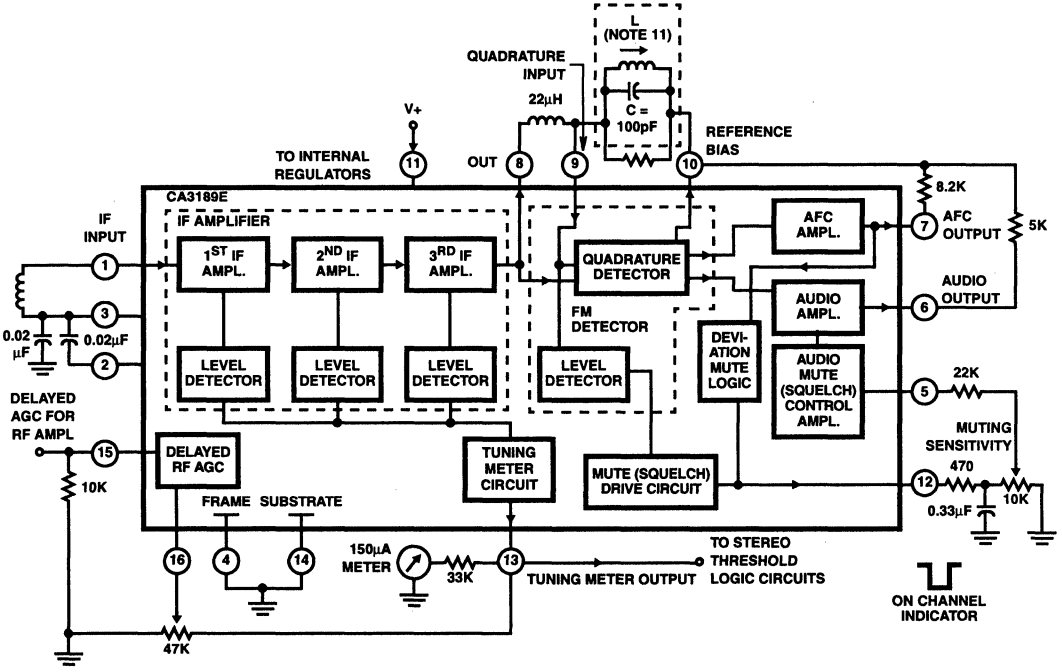


NOTES:

6. All resistance values are in ohms.
7. T: PRI. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_1) 20↑ of 34e on $^7/_{32}$" dia. form. SEC. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_2) 20↑ of 34e on $^7/_{32}$" dia. form. kQ (percent of critical coupling) ≅ 70% (Adjusted for coil voltage (V_C) = 150mV).
8. Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm.
9. C = 0.01μF for 50μs deemphasis (Europe) C = 0.015μF for 75μs deemphasis (USA).

FIGURE 2. TEST CIRCUIT FOR CA3189E USING A DOUBLE-TUNED DETECTOR COIL

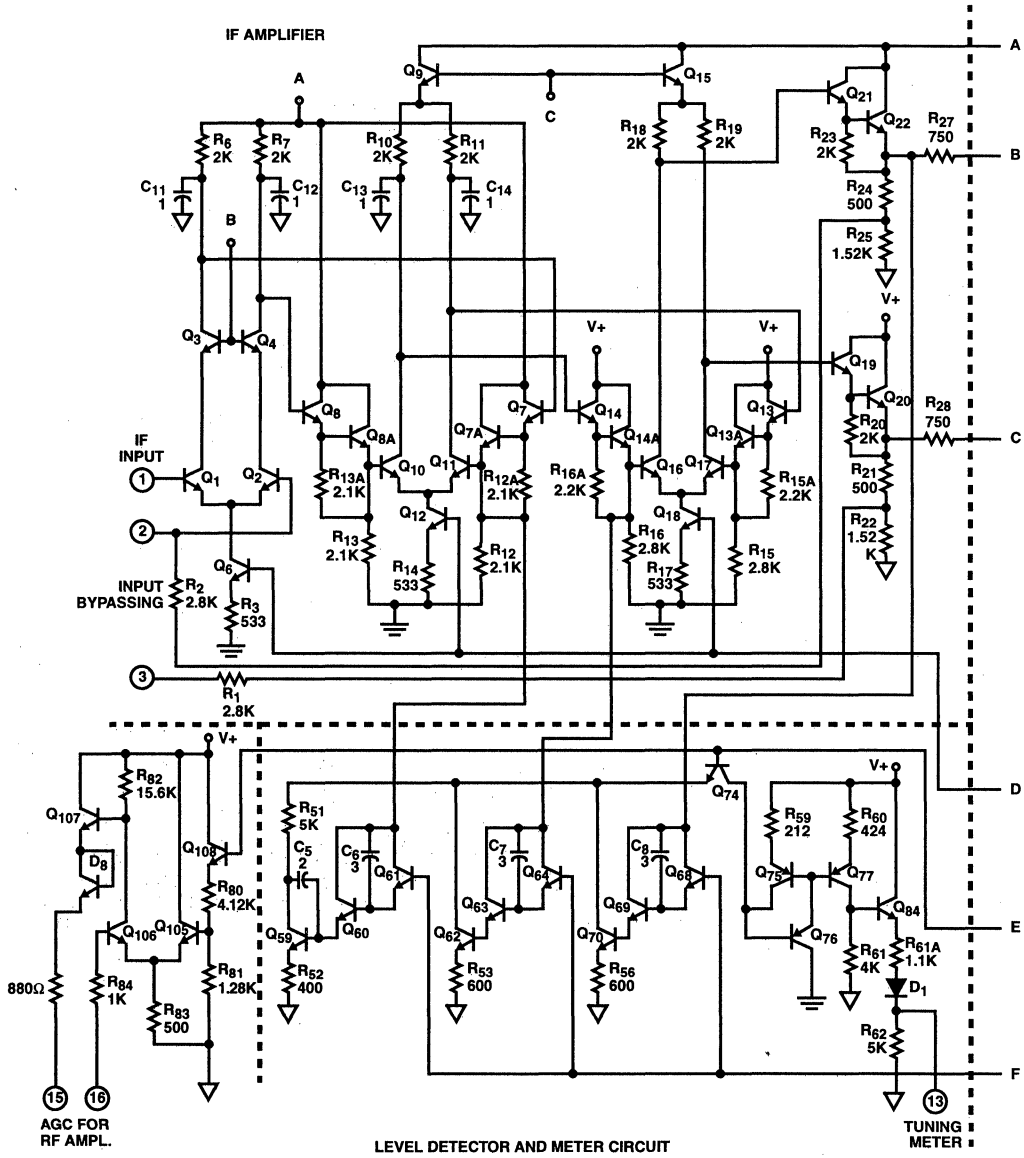
Block Diagram



NOTES:

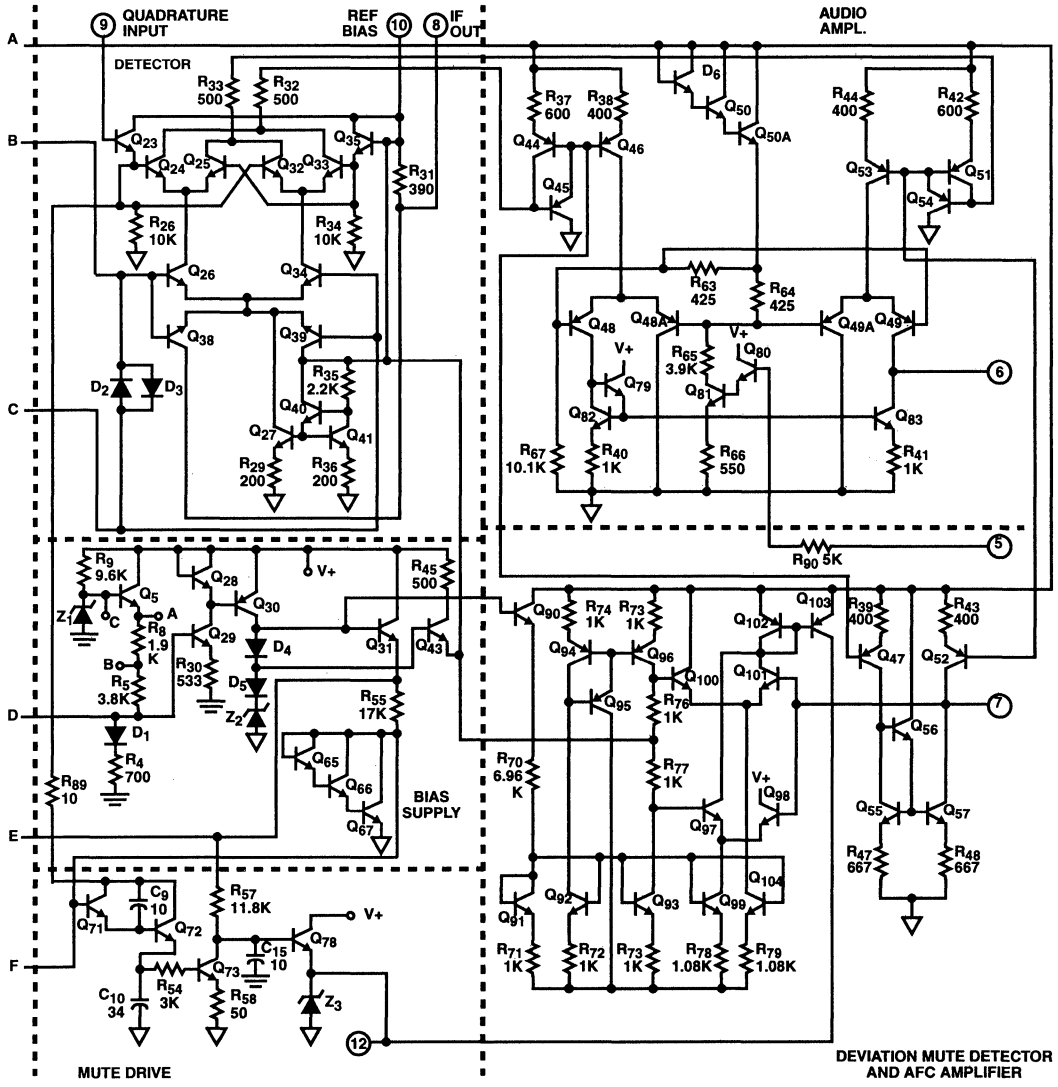
10. All resistance values are in Ω.
11. L Tunes with 100pF (C) at 10.7MHz. $Q_O \cong 75$ (TOKO No. KACS K586HM or equivalent).

Schematic Diagrams

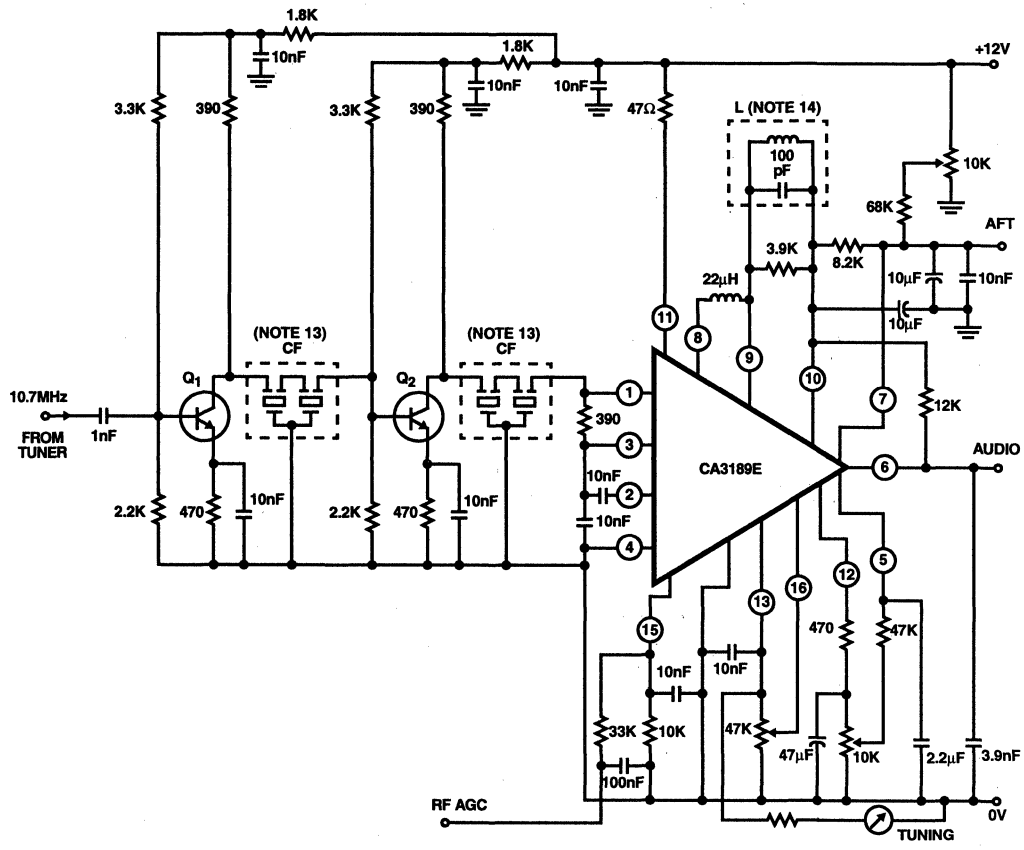


Schematic Diagrams (Continued)

CA3189E



Typical Application



NOTES:

12. All resistance values are in ohms.
13. CF: Ceramic filters, TOKO CSFE or equivalent.
14. L tunes with 100pF (C) at 10.7MHz. Q_0 (unloaded) ≅ 75 (TOKO No. KACS K586HM or equivalent).

FIGURE 3. COMPLETE FM IF SYSTEM FOR HIGH QUALITY RECEIVERS

Typical Performance Curves

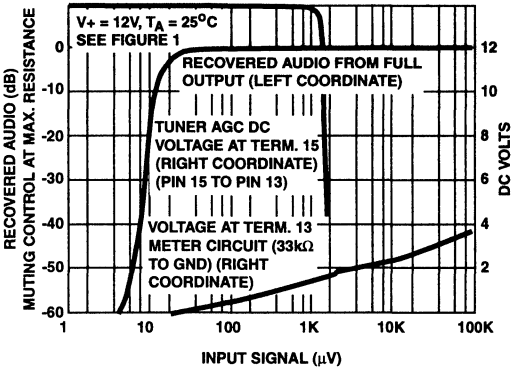


FIGURE 4. MUTING ACTION, TUNER AGC, AND TUNING METER OUTPUT vs INPUT SIGNAL VOLTAGE

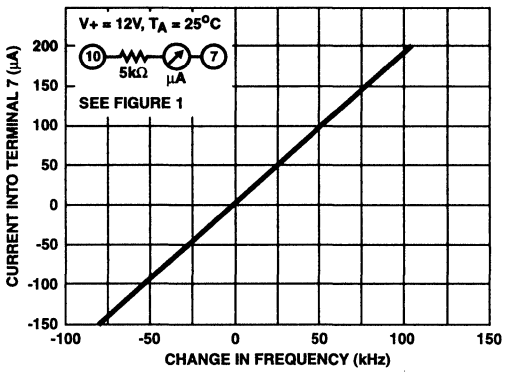


FIGURE 5. AFC CHARACTERISTICS (CURRENT AT TERMINAL 7 vs CHANGE IN FREQUENCY)

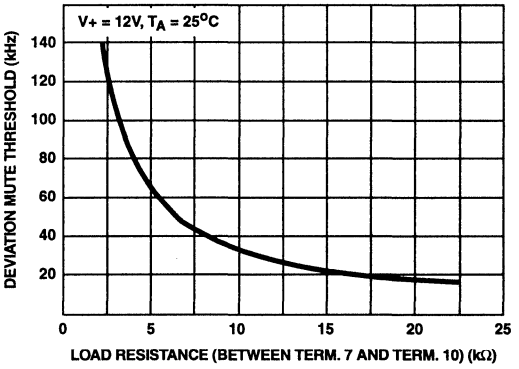


FIGURE 6. DEVIATION MUTE THRESHOLD vs LOAD RESISTANCE (BETWEEN TERMINAL 7 AND TERMINAL 10)

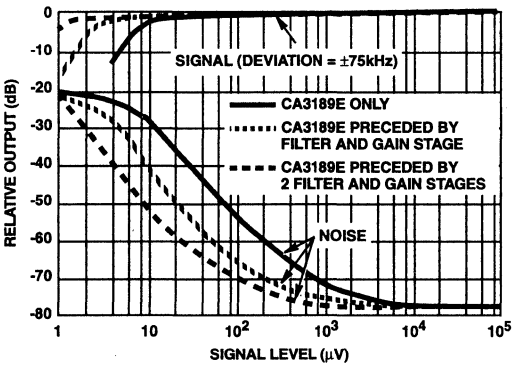


FIGURE 7. TYPICAL LIMITING AND NOISE CHARACTERISTICS

HARRIS SEMICONDUCTOR

CA3224E

November 1996

Automatic Picture Tube Bias Control Circuit

Features

- Automatic Picture Tube Bias Cutoff Control
- Automatic Background Color Balance
- Eliminates Grey Scale Adjustments
- Compensates for Cathode-to-Heater Leakage
- Electrostatic Protection on All Pins
- Servo Loop Design
- Wide Dynamic Range
- Three-Gun Control
- Minimal External Components

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3224E	-40 to 85	22 Ld PDIP	E22.4

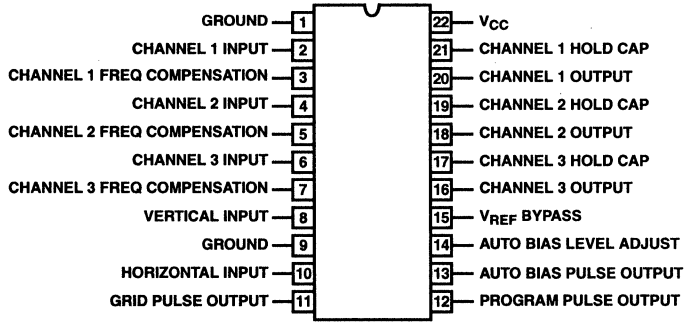
Description

The CA3224E is an automatic picture tube bias control circuit used in color TV receiver CRT drive circuits. It is used to provide dynamic bias control of the grey scale both initially and over the CRT operating life, compensating for CRT cutoff changes.

The CA3224E provides automatic continuous control of the cutoff current in each gun of a three-gun color CRT. From an input pulse amplitude proportional to the difference between the desired and the actual CRT cutoff, a gated sample/hold circuit generates a DC correction voltage which correctly biases the CRT driver circuit. The sample/hold bias correction takes place each frame following the vertical blanking. Figure 1 shows a block diagram of the CA3224E. The functions include three identical servo loop transconductance amplifiers with a sample/hold switch and buffer amplifier plus control logic, internal bias and a mode switch.

Pinout

CA3224E
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 1553.1

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{CC}) 11V
DC Input Voltage . . . . . -1 to V_{CC}
Output Current . . . . . Short Circuit Protected

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage Range (Typical) . . . . . 10V ±10%

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
PDIP Package 77
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

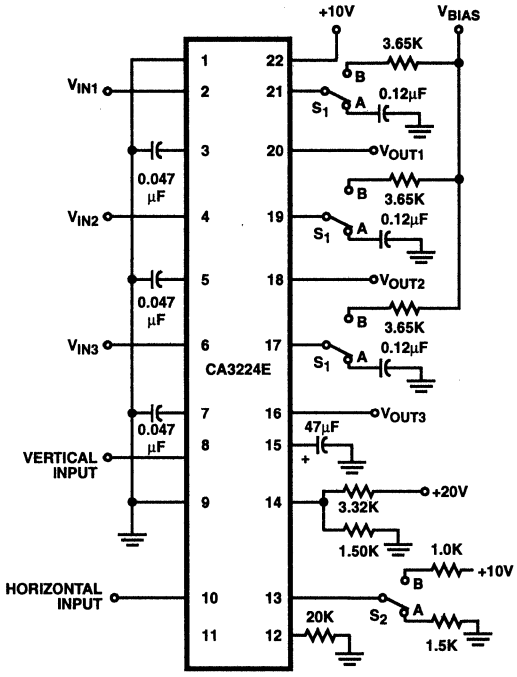
At $T_A = 25^oC$, $V_{CC} = 10V$, $V_{BIAS} = 3.75V$, V_V (Pin 8) = V_H (Pin 10) = 6.0V, S_1 = A, S_2 = A, See Test Circuit and Timing Diagrams

PARAMETER		TEST PIN NO.	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		22	I_{CC}		-	-	65	mA
Reference Voltage		2, 4, 6	V_{REF}	Measure at t_4	5.6	6.0	6.4	V
Input Current		2, 4, 6	I_I	$V_{IN} = 7.2V$, S_1 = B	-	-	250	nA
Output Current	Source	17,19, 21	I_{OM+}	$V_{BIAS} = 0.5V$, Measure at t_6, S_1 = B	-	-	-0.8	mA
	Sink		I_{OM-}	$V_{BIAS} = 7.0V$, Measure at t_6, S_1 = B	0.8	-	-	mA
Output Buffer	Input Current	17,19, 21	I_I	$V_{OUT} = 6.5V$, V_{IN} At pins 16, 18, 20, Measure at t_4, S_1 = B	-	-	150	nA
	Voltage Gain		A_V		0.97	-	1.07	-
Transconductance		17,19, 21	g_M	Measure at t_6, $V_{IN} = 8mV_{P-P}$ at 40kHz, S_1 = B	50	-	100	mS
Auto Bias Pulse	Output Low	13	V_{OL}	Measure at t_1	-	-	0.3	V
	High		V_{OH}	Measure at t_4	6.05	-	-	V
	Current Sink		I_{OM-}	Measure at t_4, S_2 = B	2.5	-	-	mA
Grid Pulse Output	Low	11	V_{OL}	Measure at t_4	-	-	0.4	V
	High		V_{OH}	Measure at t_1	4.2	-	-	V
Program Pulse Output	Low	12	V_{OL}	Measure at t_6	-	-	0.4	V
	High		V_{OH}	Measure at t_1	8.2	-	-	V
Vertical Input		8	V_V	See Figure 3	-	6.0	-	V
Horizontal Input		10	V_H	See Figure 3	-	6.0	-	V
Auto Bias Pulse Timing	Start	13		t_0 to t_2, Note 2	835	-	842	µs
	Finish			t_0 to t_7, Note 2	1270	-	1275	µs
Grid Pulse Timing	Start	11		t_0 to t_3, Note 2	899	-	905	µs
	Finish			t_0 to t_5, Note 2	1080	-	1084	µs
Program Pulse Timing	Start	12		t_0 to t_5, Note 2	1080	-	1084	µs
	Finish			t_0 to t_7, Note 2	1270	-	1275	µs

NOTE:

2. All time measurements are made from 50% point to 50% point.

Test Circuit



Device Description and Operation

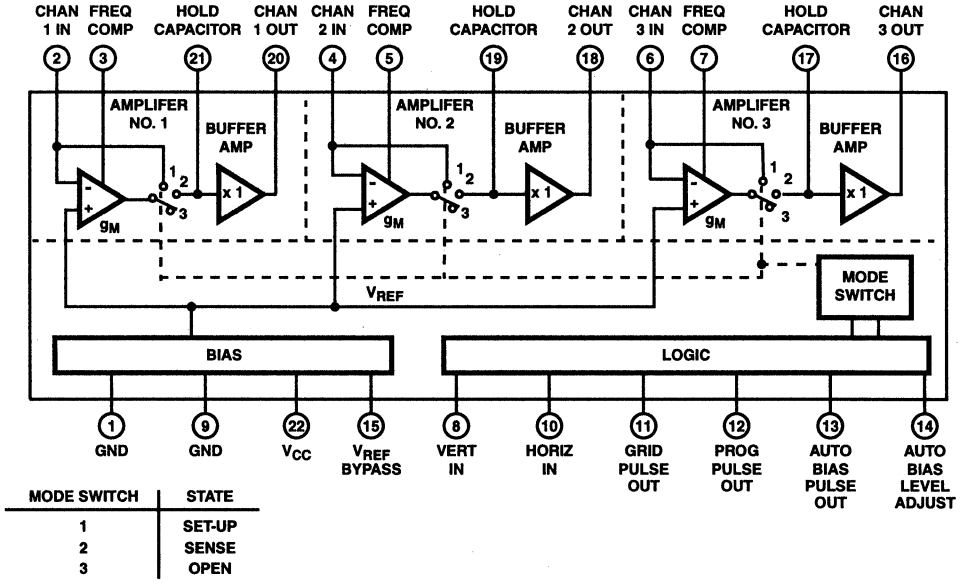
(See Figures 1, 2, 4 and 5)

During the vertical retrace interval, 13 horizontal sync pulses are counted. On the 14th sync pulse the auto-bias pulse output goes high. This is used to set the RGB drive of the companion chroma/luma circuit to black level. The auto-bias pulse stays high for 7 horizontal periods during the auto-bias cycle.

On the 15th horizontal sync pulse, the internal logic initiates the setup interval. During the setup interval, the cathode current is increased to a reference value (A in Figure 5) through the action of the grid pulse. The cathode current causes a voltage drop across R_S. This voltage drop, together with the program pulse output results in a reference voltage at V_S (summing point) which causes capacitor C_1 to charge to a voltage proportional to the reference cathode current. The setup interval lasts for 3 horizontal periods.

On the 18th horizontal sync pulse the grid pulse output goes high, which through the grid pulse amplifier/inverter, causes the cathode current to decrease. The decrease in cathode current results in a positive recovered voltage pulse with respect to the setup reference level at the V_S summing point. The positive recovered voltage pulse is summed with a negative voltage pulse caused by the program pulse output going low (cutting off Diode D_1 and switching in resistors R_1 and R_2). Any difference between the positive and negative pulses is fed through capacitor C_1 to the transconductance amplifier. The difference signal is amplified in the transconductance amplifier and charges the hold capacitor C_2, which, through the buffer amplifier, adjusts the bias on the driver circuit.

Components R_S, R_1, and R_2 must be chosen such that the program pulse and the recovered pulse just cancel at the desired cathode cutoff level.



MODE SWITCH	STATE
1	SET-UP
2	SENSE
3	OPEN

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

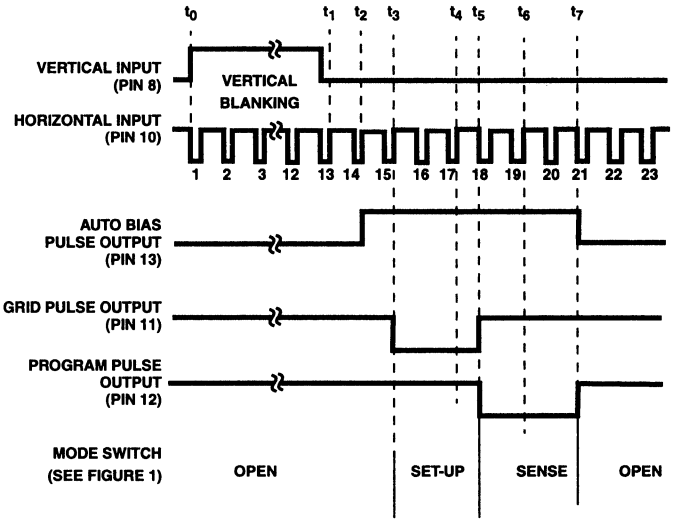


FIGURE 2. FUNCTIONAL TIMING DIAGRAMS

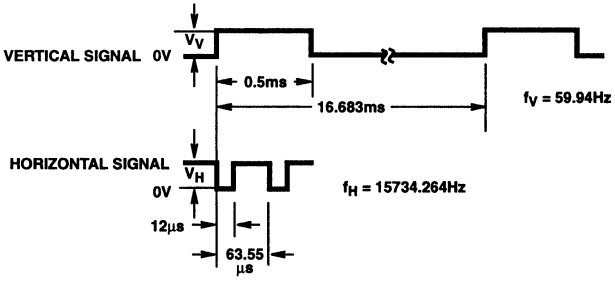
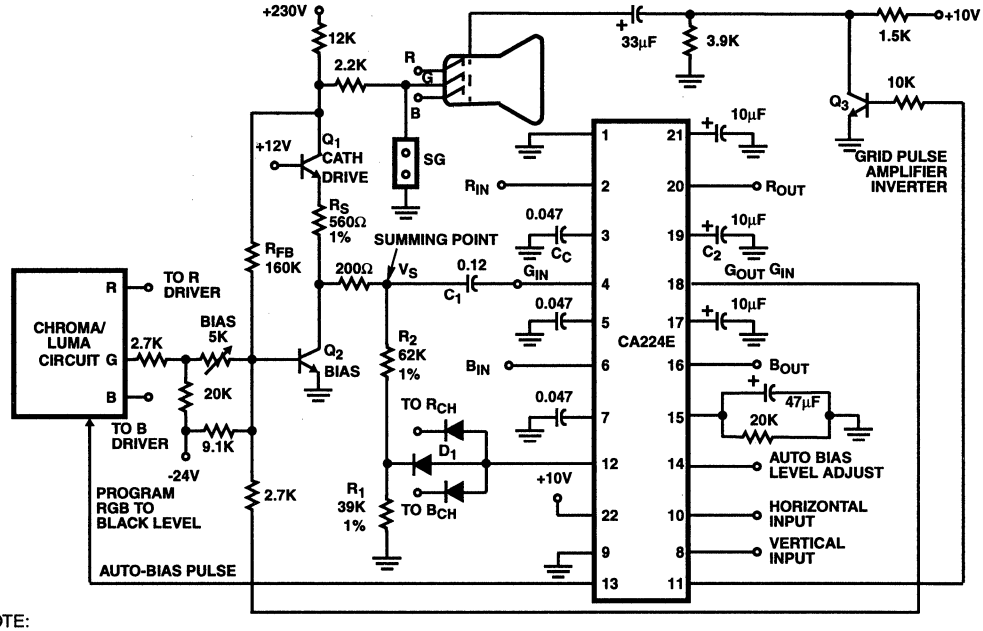


FIGURE 3. VERTICAL AND HORIZONTAL INPUT SIGNALS



NOTE:

3. One of three identical driver circuits shown.

FIGURE 4. TYPICAL APPLICATION CIRCUIT

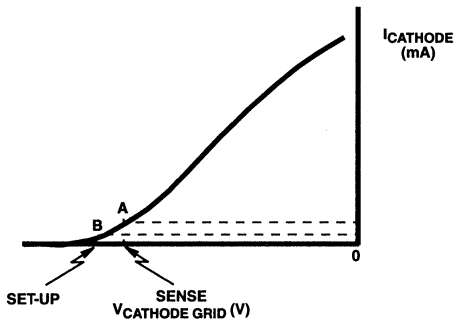


FIGURE 5. PICTURE TUBE V-I CURVE

Electrostatic Protection (Note)

When correctly designed for ESD protection, SCRs can be highly effective, enabling circuits to be protected to well in excess of 4kV. The SCR ESD-EOS protection structures used on each terminal of the CA3224E are shown schematically in either Figures 6A or 6B. Although ESD-EOS protection is included in the CA3224E, proper circuit board layout and grounding techniques should be observed.

NOTE: For further information on CA3224E protection structures refer to: AN7304, "Using SCRs as Transient Protection Structures in Integrated Circuits", by L.R. Avery. Harris AnswerFAX (407-724-7800) document #97304.

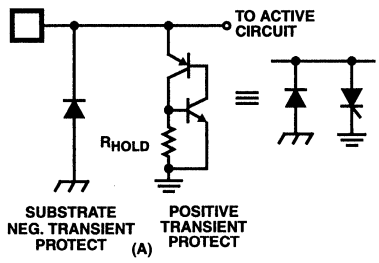


FIGURE 6A.

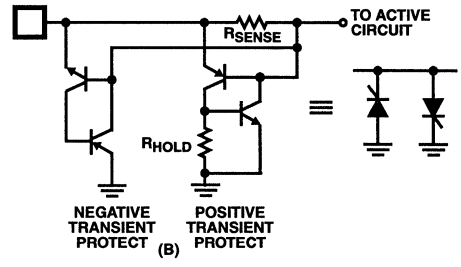


FIGURE 6B.

FIGURE 6. TRANSIENT PROTECTION

Complete data sheet available via web, Harris' home page: http://www.semi.harris.com/ or via Harris AnswerFAX, see Section 12

CA3256

25MHz, BiMOS Analog Video Switch and Amplifier

November 1996

Features

- 5 Multiplex Video Channels
  - 1 Independent Channel
  - 4 Channels with Enable
- 4 LED Channel Indicator Outputs
- Wideband Video Amplifier .....25MHz Unity Gain
- Adjustable Video Amplifier Gain
- High Signal-Drive Capability

Applications

- Video Multiplex Switch
- 75Ω Video Amplifier/Line Driver
- Video Signal-Level Control
- Monitor Switching Control
- TV/CATV Audio/Video Switch
- Video Signal Adder/Fader Control

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3256E	-40 to 85	18 Ld PDIP	E18.3
CA3256M	-40 to 85	20 Ld SOIC	M20.3

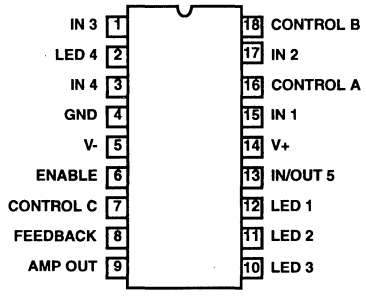
Description

The CA3256 BiMOS analog video switch has five channels of CMOS multiplex switching for general-purpose video-signal control. One of four CMOS channels may be selected in parallel with channel 5. The CMOS switches are inputs to the video amplifier but may be used in bilateral switching between channels 1 to 4 and channel 5. The analog switches of channels 1 to 4 are digitally controlled with logic level conversion and binary decoding to select 1 of 4 channels. The enable function controls channels 1 to 4 but does not affect channel 5. LED output drivers are selected with the channel 1-to-4 switch selection to indicate the ON-channel. Channel 5 may be used as a monitor output for data or signal information on channels 1 to 4. The transmission gate switches shown in the block diagram of the CA3256 are configured in a "T" design to minimize feedthrough. When the switch is off, the shunt or center of the "T" is grounded.

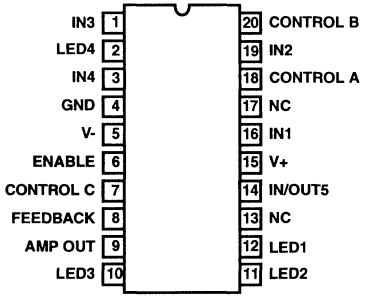
The amplifier has high input impedance to minimize the R_{ON} transmission gate insertion loss. The amplifier output impedance is typically 5Ω in a complementary symmetry output. The amplifier can directly drive a nominal 75Ω coaxial cable to provide line-to-line video switching. The gain of the amplifier is programmable by different feedback resistor values between pins 8 and 9. Compensation may also be used between these pins for an optimally flat frequency response. An internal regulated 5V bias reference with temperature compensation permits stable direct-coupled output drive and minimizes DC offset during signal switching.

Pinouts

CA3256
(PDIP)
TOP VIEW



CA3256
(SOIC)
TOP VIEW



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 1769.4

HARRIS SEMICONDUCTOR

CD22402

Sync Generator for TV Applications and Video Processing Systems

November 1996

Features

- Interlaced Composite Sync Output
- Automatic Genlock Capability
- Crystal Oscillator Operation
- 525 or 625 Line Operation
- Vertical Reset Option
- Wide Power Supply Operating Voltage . . . . . 4V to 15V

Applications

- Cameras
- Monitors and Displays
- CATV
- Teletext
- Video Games
- Sync Restorer
- Video Service Instruments

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22402D	-55 to 125	24 Ld SBDIP	D24.6
CD22402E	-40 to 85	24 Ld PDIP	E24.6

Description

The Harris CD22402 (Note) is a CMOS LSI sync generator that produces all the timing signals required to drive a fully 2-to-1 interlaced 525-line 30-frame/second, or 625-line 25-frame/second TV camera or video processing system. A complete sync waveform is produced which begins each field with six serrated vertical sync pulses, preceded and followed by six half-width double frequency equalizing pulses. The sync output is gated by the master clock to preserve horizontal phase continuity during the vertical interval.

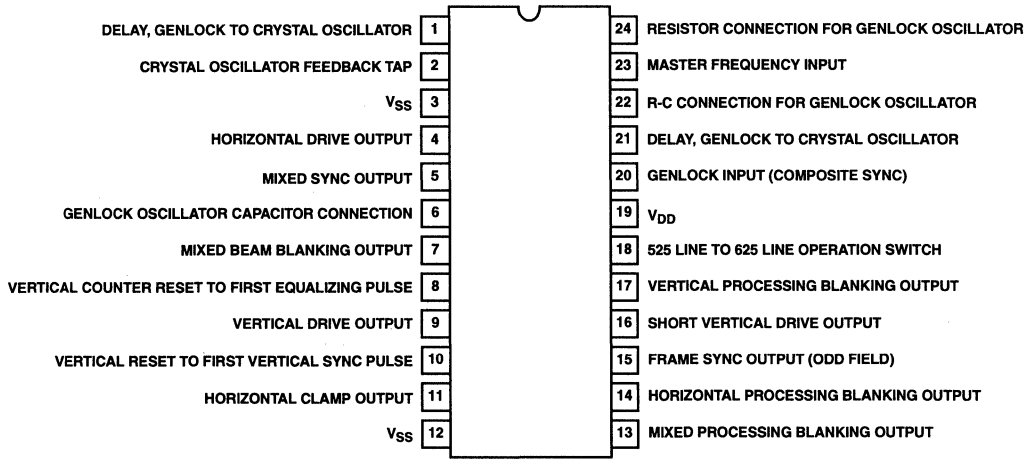
The CD22402 can be operated either in "genlock" mode, in which it is synchronized with a reference sync pulse train from another TV camera, or in "stand-alone" mode, in which it is synchronized with a local on-chip crystal oscillator (the crystal and two passive components are off chip). Also, the circuit can sense the presence or absence of a reference sync pulse train and automatically select the "genlock" or "stand-alone" mode.

A frame sync pulse is produced at the beginning of every odd field. The vertical counter can be reset to either the first equalizing pulse or the first vertical sync pulse of the vertical interval. The interlaced sync provided by the CD22402 differs from RS-170 by having slightly narrower sync and equalizing pulses. The clock frequency of 32 times horizontal rate allows for approximately 4µs horizontal pulse widths and 2µs equalizing pulses. Otherwise operation can be phase locked to a color sub-carrier for a full interlaced operating system.

The CD22402 is operable with a single supply over a voltage range of 4V to 15V.

Pinout

CD22402 (PDIP, SBDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1686.3**

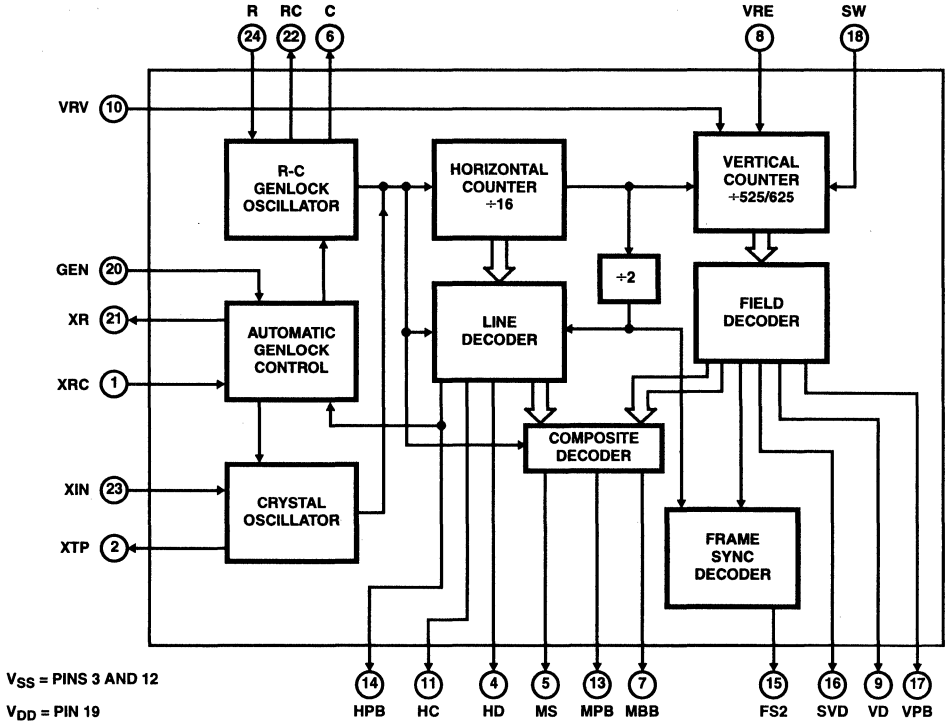
Pin Descriptions

PIN NO.	SYMBOL	DESCRIPTION
1	XRC	**Delay, Genlock to Crystal Oscillator.** Resistor, diode and capacitor connection for delay that automatically turns on the crystal oscillator when the genlock input is removed. When the signal on Terminal 1 is high the crystal oscillator is inhibited. Typical values for R and C are 1MΩ and 0.001µF. For operation as a crystal controlled stand alone sync generator without genlock, Terminal 1 should be hardwired to V_{SS}.
2	XTP	**Crystal Oscillator Feedback Tap.** Feedback connection (tap) for crystal oscillator. When a crystal (shunted by a 1MΩ resistor) is connected between this terminal and Terminal 23, and a 100pF capacitor is connected from this terminal to V_{SS}, the sync generator creates its own master frequency. For a 525-line, 30-frame/second raster, the crystal frequency is 504.000kHz (Note 1); and for a 625-line, 25-frame/second raster, the crystal frequency is 500.000kHz (Note 1).
3	V_{SS}	**Negative Power Supply Voltage.** This terminal must be hardwired to Terminal 12 (V_{SS}).
4	HD	**Horizontal Drive Output**
5	MS	**Mixed Sync Output**
6	C	**Capacitor Connection for R-C Genlock Oscillator**
7	MBB	**Mixed Beam Blanking Output**
8	VRE	**Vertical Counter Reset to First Equalizing Pulse.** A low level signal on this terminal resets the vertical counter to the first equalizing pulse of a field. When not in use this terminal should be connected to V_{DD}.
9	VD	**Vertical Drive Output**
10	VRV	**Vertical Counter Reset to First Vertical Sync Pulse.** A low level signal on this terminal resets the sync generator to the first vertical sync pulse of a field. For genlock operation, Terminal 10 is used as a resistor and capacitor connection for an integrator network that detects vertical sync pulses in a master sync waveform to which the sync generator is to be genlocked. R is 22kΩ, and C is 0.001pF. When not in use this terminal should be connected to V_{DD}.
11	HC	**Horizontal Clamp Output**
12	V_{SS}	**Negative Power Supply Voltage**
13	MPB	**Mixed Processing Blanking Output**
14	HPB	**Horizontal Processing Blanking Output**
15	FS2	**Frame Sync Output (Odd Field).** A pulse coinciding with the first equalizing pulse is produced at the beginning of every odd field.
16	SVD	**Short Vertical Drive Output**
17	VPB	**Vertical Processing Blanking Output**
18	SW	**Operation Switch for 525-Line or 625-Line Raster.** A high level signal on Terminal 18 causes the sync generator to generate a 625-line raster. An internal pulldown resistor is connected to Terminal 18, so in the absence of an applied input to this terminal, a 525-line raster is produced.
19	V_{DD}	**Positive Power Supply Voltage.** V_{DD} can be any voltage between +4 and +15 relative to V_{SS}.
20	GEN	**Genlock Input Composite Sync.** A negative going reference mixed sync waveform applied to Terminal 20 disables the crystal oscillator and locks the R-C genlock oscillator to the horizontal pulses of the reference sync waveform. Vertical sync detection is achieved by an R-C integrator connected from Terminal 20 to Terminal 10 (vertical reset to first vertical sync pulse). An internal pull-up resistor is connected to Terminal 20 so that in the absence of an applied input the crystal oscillator is enabled and the R-C genlock oscillator is disabled.
21	XR	**Delay, Genlock to Crystal Oscillator, Resistor and Diode Connection for Delay, Genlock to Crystal Oscillator.** Automatically turns on the crystal oscillator when the input to Terminal 20 is removed.
22	RC	**Resistor and Capacitor Connection for Genlock Oscillator.** If the genlock oscillator is not used this terminal should be connected to V_{SS}. C should be 100pF, and R should be a 10kΩ potentiometer.
23	XIN	**Master Frequency Input.**
24	R	**Resistor Connection for Genlock Oscillator.**

NOTE: 32 times horizontal frequency.

Block Diagram

CD22402 MONOCHROME TV SYNC GENERATOR WITH AUTOMATIC GENLOCK



Absolute Maximum Ratings

DC Supply Voltage (Referenced to V_{SS} Terminal) 15V
Input Voltage Range, All Inputs (Notes 2, 3) . . . . . $V_{SS} \le V_I \le V_{DD}$
DC Input Current, Any One Input (Note 2) . . . . . ±10mA

Operating Conditions

Temperature Range
CD22402D . . . . . -55°C to 125°C
CD22402E . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	50	10
PDIP Package	50	N/A

Maximum Junction Temperature (SBDIP Package) . . . . . 175°C
Maximum Junction Temperature (PDIP Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10mA even when the power is off.
3. A connection must be provided at every input terminal. All unused inputs must be connected to V_{DD} or V_{SS}, whichever is appropriate.

Electrical Specifications

Values at -55°C, 25°C, 125°C Apply to D Package
Values at -40°C, 25°C, 85°C Apply to E Package

PARAMETER	SYMBOL	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	-55°C	-40°C	85°C	125°C	25°C MIN	25°C TYP	25°C MAX	UNITS
DC ELECTRICAL SPECIFICATIONS											
Quiescent Device Current	I_{DD} (Max)	-	5	-	-	-	-	0.5	0.75	1	mA
		-	10	-	-	-	-	1.5	2	2.5	mA
		-	15	-	-	-	-	3	4	5	mA
Output Low (Sink) Current	I_{OL} (Min)	0.5	5	100	96	66	56	80	160	-	µA
		5	5	1200	1155	787	672	960	1920	-	µA
		0.5	10	248	239	164	140	200	400	-	µA
		10	10	3000	2868	1968	1680	2400	4800	-	µA
Output High (Source) Current	I_{OH} (Min)	4.5	5	-100	-96	-66	-56	-80	-160	-	µA
		0	5	-1200	-1155	-787	-672	-960	-1920	-	µA
		9.5	10	-248	-239	-164	-140	-200	-400	-	µA
		0	10	-3000	-2868	-1968	-1680	-2400	-4800	-	µA
Output Voltage Low Level	V_{OL} (Max)	-	5	0.15	0.15	0.15	0.15	-	-	0.15	V
		-	10	0.15	0.15	0.15	0.15	-	-	0.15	V
Output Voltage High Level	V_{OH} (Min)	-	5	4.85	4.85	4.85	4.85	4.85	-	-	V
		-	10	9.85	9.85	9.85	9.85	9.85	-	-	V
Input Low Voltage	V_{IL} (Max)	0.5, 4.5	5	1.5	1.5	1.4	1.4	-	2.25	1.5	V
		1, 9	10	3	3	2.9	2.9	-	4.5	3	V
Input High Voltage	V_{IH} (Min)	0.5, 4.5	5	3.6	3.6	3.5	3.5	3.5	2.25	-	V
		1, 9	10	7.1	7.1	7	7	7	4.5	-	V
Input Current	I_{IN} (Max)	-	-	-	-	-	-	-	10	-	pA

Refer to the CD4000B Series data book 250.5 for general operating and application considerations.

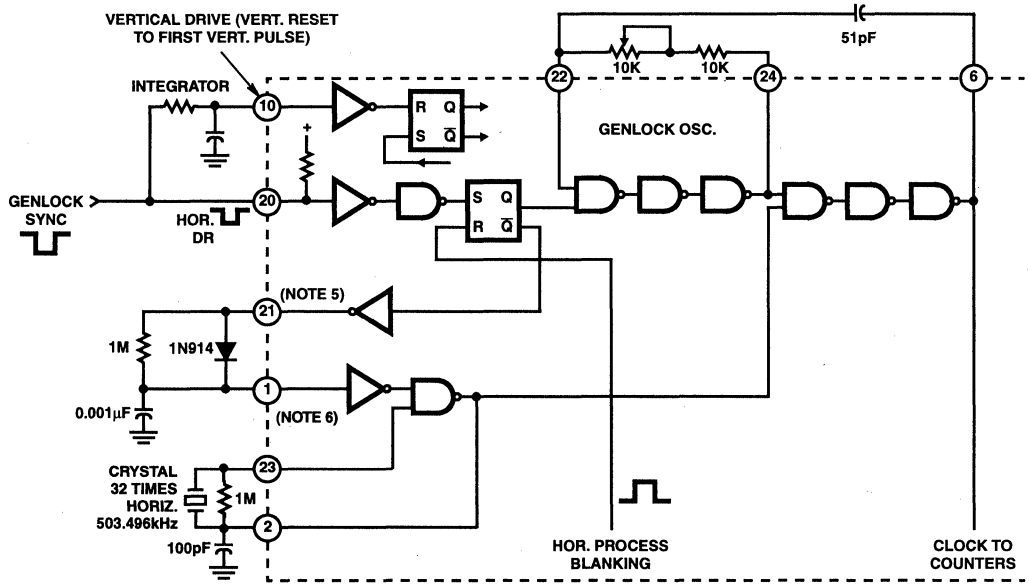
Switching Electrical Specifications $T_A = 25^oC$ and $C_L = 15pF$. Typical Temperature Coefficient for All Values of $V_{DD} = 0.3\%/^oC$

PARAMETER (NOTE 4)	SYMBOL	TEST CONDITIONS V_{DD} (V)	MIN	TYP	MAX	UNITS
Output State Propagation Delay Time (50% to 50%)						
Low-to-High Level	t_{PLH}	5	-	40	80	ns
High-to-Low Level	t_{PHL}	10	-	20	40	ns
Output State Transition Time (10% to 90%)						
Low-to-High	t_{TLH}	5	-	45	90	ns
High-to-Low	t_{THL}	10	-	30	60	ns
Input Capacitance (Per Input)	C_I	-	-	5	-	pF

NOTE:

4. The characteristics given are defined for unbuffered gate in the CMOS process of the CD22402.

Logic Diagram



NOTES:

5. Pin 21 high when pin 20 is high (or open).
6. Pin 1 high inhibits clock.

FIGURE 1. DETAIL OF THE OSCILLATOR/GENLOCK PORTION OF THE CD22402

Timing Waveforms

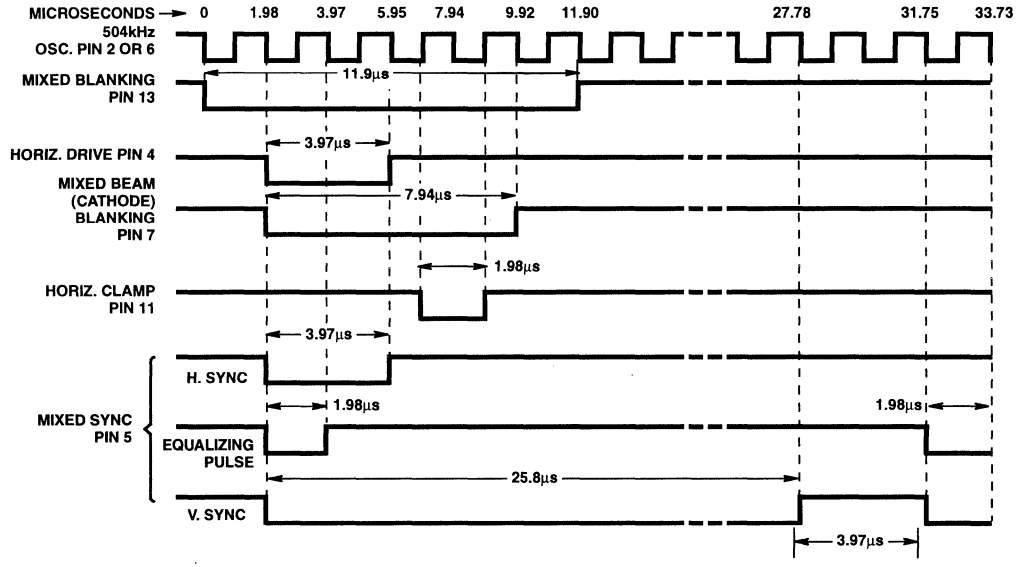


FIGURE 2. SYNC GENERATOR TIMING - 525/60Hz, HORIZONTAL TIMING WAVEFORMS

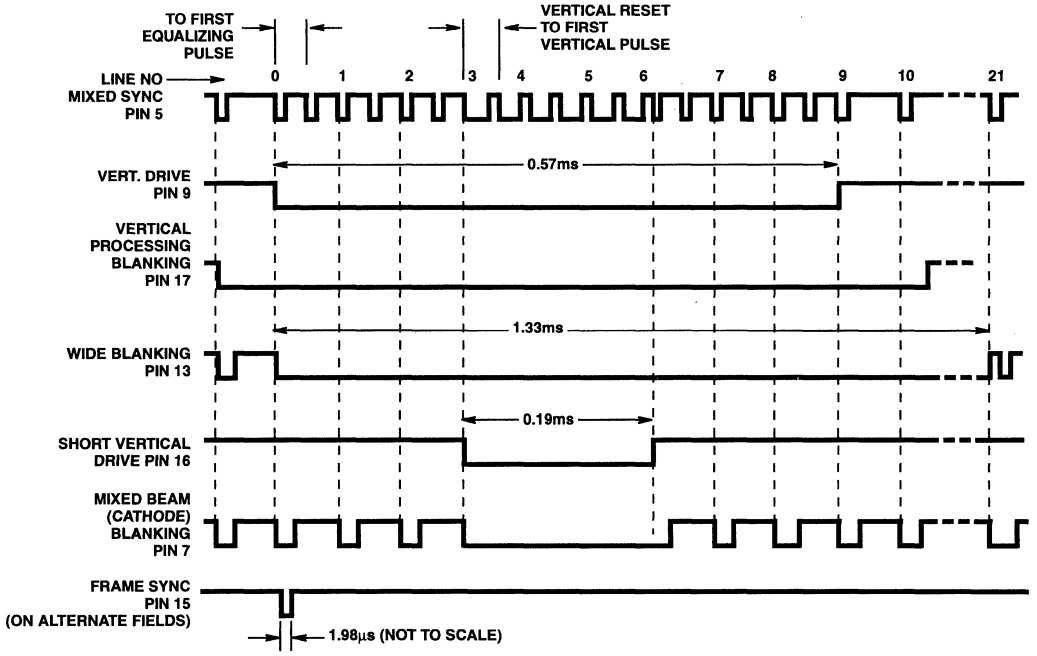


FIGURE 3. SYNC GENERATOR TIMING - 525/60Hz, VERTICAL TIMING WAVEFORMS

Timing Waveforms (Continued)

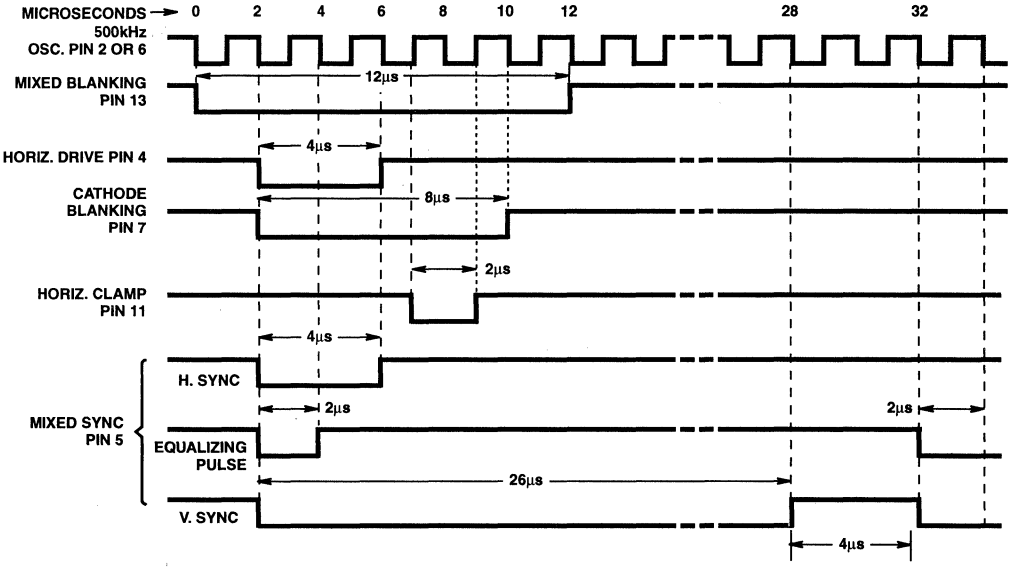


FIGURE 4. SYNC GENERATOR TIMING - 625/50Hz, HORIZONTAL TIMING WAVEFORMS

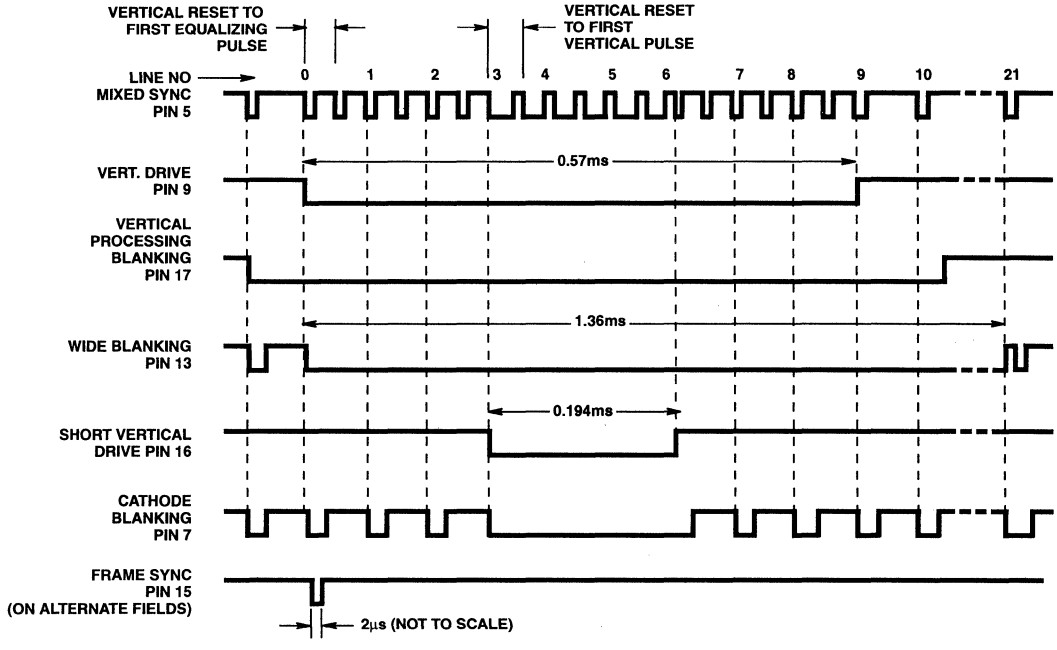


FIGURE 5. SYNC GENERATOR TIMING - 625/50Hz, VERTICAL TIMING WAVEFORMS

Timing Waveforms (Continued)

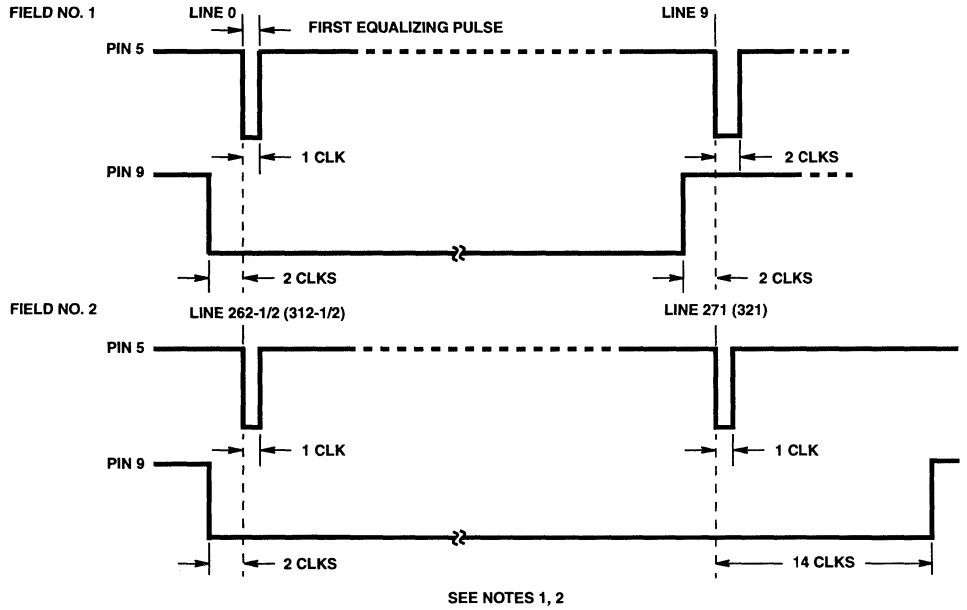


FIGURE 6. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (VERTICAL DRIVE - PIN 9)

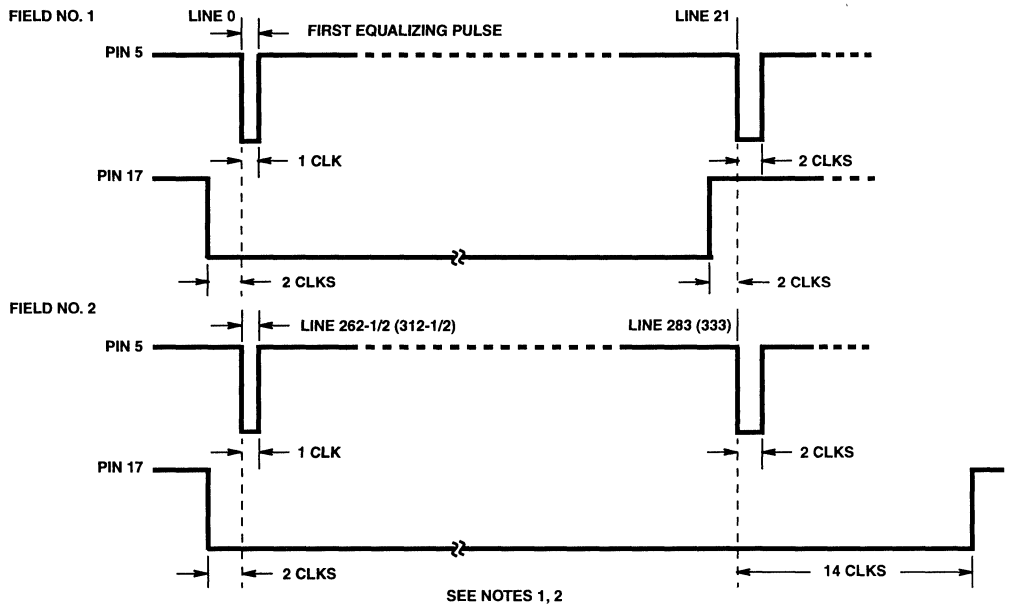


FIGURE 7. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (VERTICAL PROCESSING BLANKING - PIN 17)

Timing Waveforms (Continued)

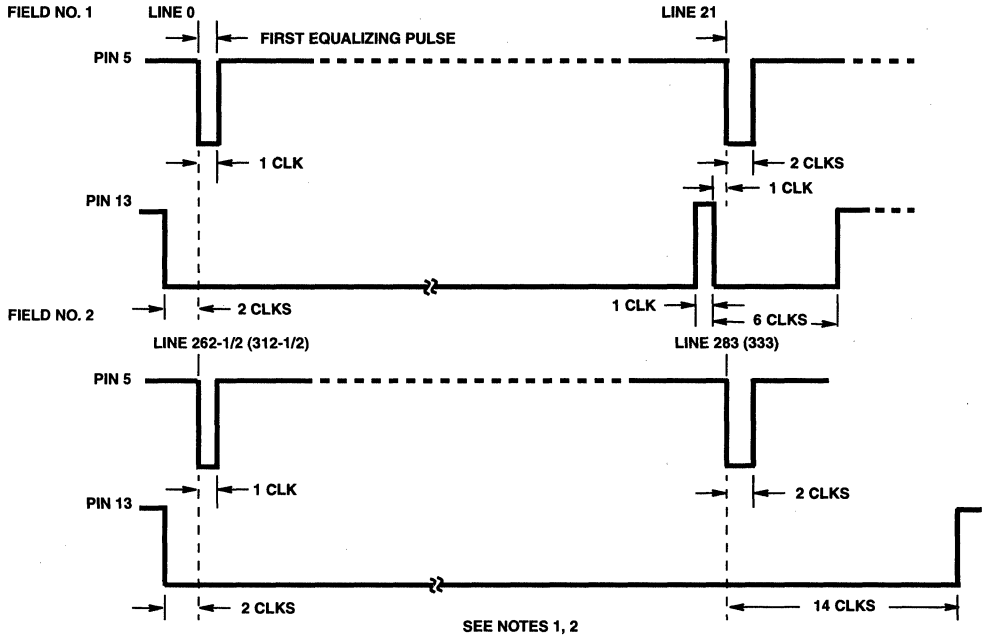


FIGURE 8. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (MIXED PROCESSING BLANKING - PIN 13)

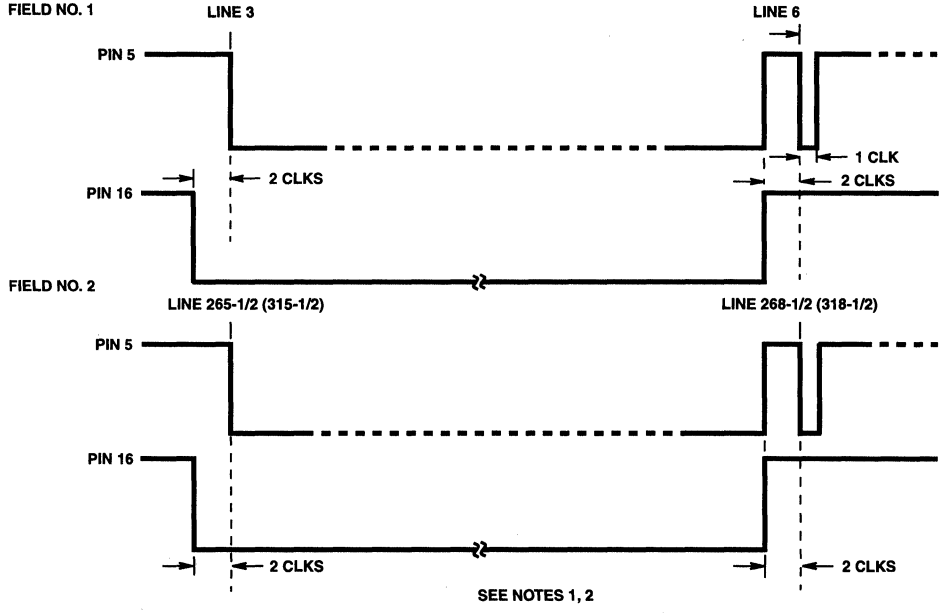
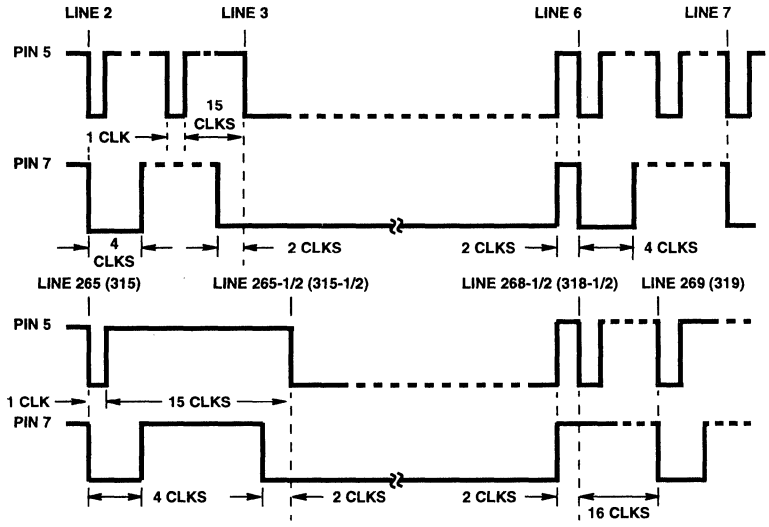


FIGURE 9. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (SHORT VERTICAL DRIVE - PIN 16)

Timing Waveforms (Continued)



NOTES:

7. Waveforms shown are for 525 line/60Hz, line number in parenthesis are for (625 line/50Hz).
8. Timing widths by clock count; for 525 line, 1 CLK = 1.98µs; for 625 line, 1 CLK = 2µs; 1 horizontal period = 32 CLKS.

FIGURE 10. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (MIXED BEAM BLANKING - PIN 7)

Typical Applications (Refer to Application Note AN8742, for more information)

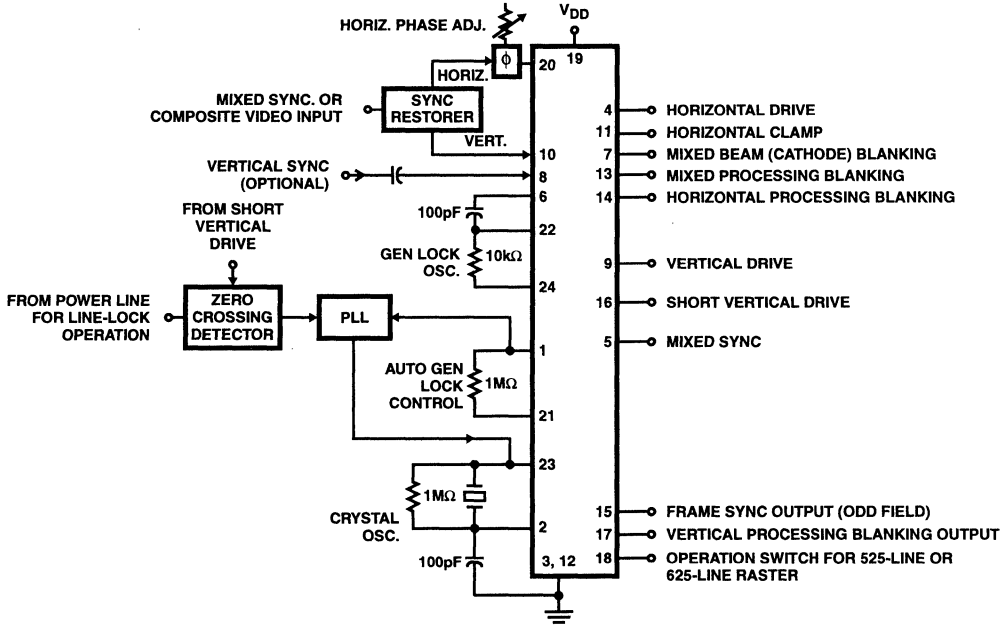
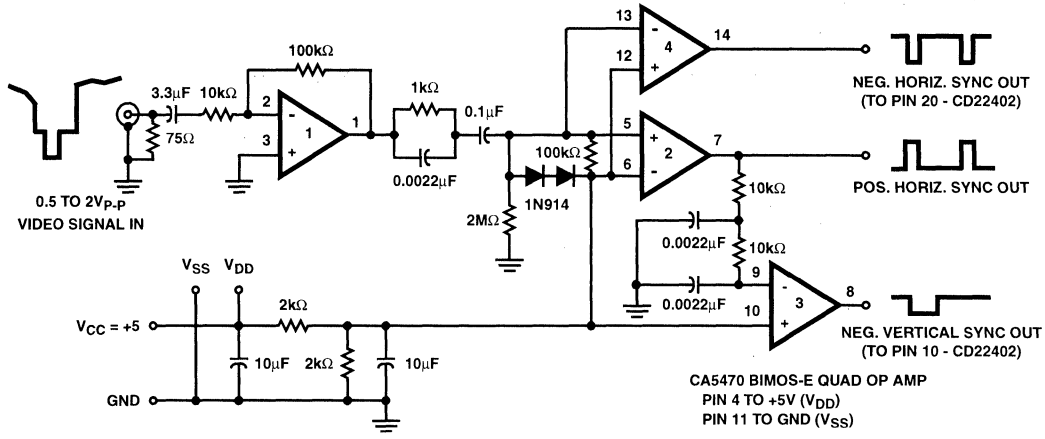


FIGURE 11. TYPICAL APPLICATION IN A TV CAMERA



NOTE: The genlock input to pins 10 and 20 of the CD22402 are direct coupled to the output from Pins 8 and 14 of the CA5470. Refer to Application Note AN-8742 for additional information.

FIGURE 12. SUGGESTED SYNC-SEPARATOR CIRCUIT USING THE CA5470 BIMOS-E QUAD OP AMP IN THE V_{DD} RANGE OF 4V TO 12V

HARRIS SEMICONDUCTOR

HA-2546

30MHz, Voltage Output, Two Quadrant Analog Multiplier

November 1996

Features

- High Speed Voltage Output 300V/μs
- Low Multiplication error 1.6%
- Input Bias Currents 1.2μA
- Signal Input Feedthrough . . . . . -52dB
- Wide Signal Bandwidth 30MHz
- Wide Control Bandwidth 17MHz
- Gain Flatness to 5MHz 0.10dB

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Description

The HA-2546 is a monolithic, high speed, two quadrant, analog multiplier constructed in the Harris Dielectrically Isolated High Frequency Process. The HA-2546 has a voltage output with a 30MHz signal bandwidth, 300V/μs slew rate and a 17MHz control bandwidth. High bandwidth and slew rate make this part an ideal component for use in video systems. The suitability for precision video applications is demonstrated further by the 0.1dB gain flatness to 5MHz, 1.6% multiplication error, -52dB feedthrough and differential inputs with 1.2μA bias currents. The HA-2546 also has low differential gain (0.1%) and phase (0.1 degree) errors.

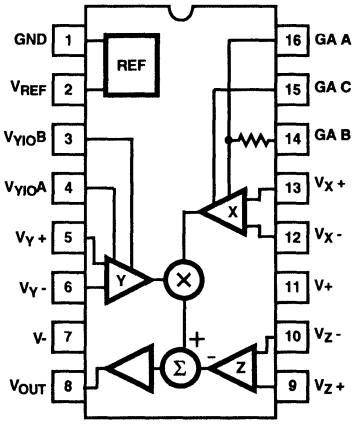
The HA-2546 is well suited for AGC circuits as well as mixer applications for sonar, radar, and medical imaging equipment. The voltage output simplifies many designs by eliminating the current to voltage conversion stage required for current output multipliers. For MIL-STD-883 compliant product, consult the HA-2546/883 datasheet.

Ordering Information

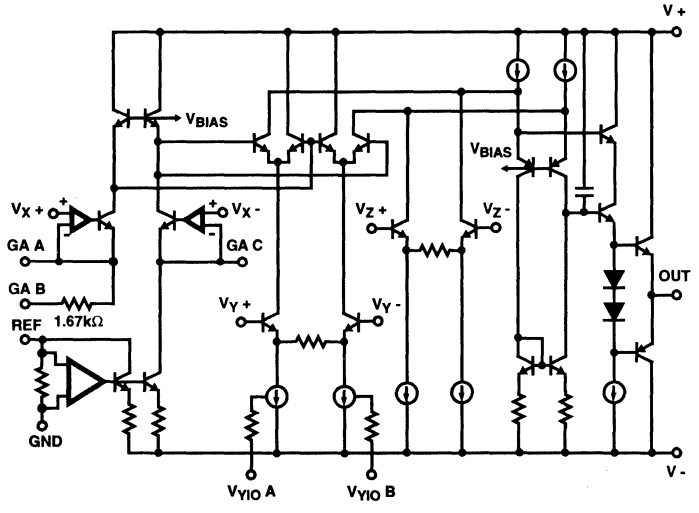
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-2546-5	0 to 75	16 Ld CERDIP	F16.3
HA1-2546-9	-40 to 85	16 Ld CERDIP	F16.3
HA3-2546-5	0 to 75	16 Ld PDIP	E16.3
HA9P2546-5	0 to 65	16 Ld SOIC	M16.3

Pinout

HA-2546
(PDIP, CERDIP, SOIC)
TOP VIEW



Simplified Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 2861.2

Absolute Maximum Ratings

Voltage Between V+ and V- 35V
Differential Input Voltage 6V
Output Current ..... ±60mA

Operating Conditions

Temperature Range
HA1-2546-9 ..... -40°C to 85°C
HA3-2546-5 ..... 0°C to 75°C
HA9P2546-5 ..... 0°C to 65°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
PDIP Package	86	N/A
SOIC Package	96	N/A

Maximum Junction Temperature (CERDIP Package) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L = 50pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE						
Multiplication Error (Note 2)		25	-	1.6	3	%
		Full	-	3.0	7	%
Multiplication Error Drift		Full	-	0.003	-	%/°C
Differential Gain (Notes 3, 9)		25	-	0.1	0.2	%
Differential Phase (Notes 3, 9)		25	-	0.1	0.3	Degrees
Gain Flatness (Note 9)	DC to 5MHz, $V_X = 2V$	25	-	0.1	0.2	dB
	5MHz to 8MHz, $V_X = 2V$	25	-	0.18	0.3	dB
Scale Factor Error		Full	-	0.7	5.0	%
1% Amplitude Bandwidth Error		25	-	6	-	MHz
1% Vector Bandwidth Error		25	-	260	-	kHz
THD + N (Note 4)		25	-	0.03	-	%
Voltage Noise	$f_O = 10Hz$, $V_X = V_Y = 0V$	25	-	400	-	$nV/\sqrt{Hz}$
	$f_O = 100Hz$, $V_X = V_Y = 0V$	25	-	150	-	$nV/\sqrt{Hz}$
	$f_O = 1kHz$, $V_X = V_Y = 0V$	25	-	75	-	$nV/\sqrt{Hz}$
Common Mode Range		25	-	±9	-	V
SIGNAL INPUT, V_Y						
Input Offset Voltage		25	-	3	10	mV
		Full	-	8	20	mV
Average Offset Voltage Drift		Full	-	45	-	µV/°C
Input Bias Current		25	-	7	15	µA
		Full	-	10	15	µA
Input Offset Current		25	-	0.7	2	µA
		Full	-	1.0	3	µA
Input Capacitance		25	-	2.5	-	pF
Differential Input Resistance		25	-	720	-	kΩ
Small Signal Bandwidth (-3dB)	$V_X = 2V$	25	-	30	-	MHz

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L = 50pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
Full Power Bandwidth (Note 5)	$V_X = 2V$	25	-	9.5	-	MHz
Feedthrough	Note 11	25	-	-52	-	dB
CMRR	Note 6	Full	60	78	-	dB
V_Y TRANSIENT RESPONSE (Note 10)						
Slew Rate	$V_{OUT} = \pm5V$, $V_X = 2V$	25	-	300	-	V/µs
Rise Time	Note 7	25	-	11	-	ns
Overshoot	Note 7	25	-	17	-	%
Propagation Delay		25	-	25	-	ns
Settling Time (To 0.1%)	$V_{OUT} = \pm5V$, $V_X = 2V$	25	-	200	-	ns
CONTROL INPUT, V_X						
Input Offset Voltage		25	-	0.3	2	mV
		Full	-	3	20	mV
Average Offset Voltage Drift		Full	-	10	-	µV/°C
Input Bias Current		25	-	1.2	2	µA
		Full	-	1.8	5	µA
Input Offset Current		25	-	0.3	2	µA
		Full	-	0.4	3	µA
Input Capacitance		25	-	2.5	-	pF
Differential Input Resistance		25	-	360	-	kΩ
Small Signal Bandwidth (-3dB)	$V_Y = 5V$, $V_X = -1V$	25	-	17	-	MHz
Feedthrough	Note 12	25	-	-40	-	dB
Common Mode Rejection Ratio	Note 13	25	-	80	-	dB
V_X TRANSIENT RESPONSE (Note 10)						
Slew Rate	Note 13	25	-	95	-	V/µs
Rise Time	Note 14	25	-	20	-	ns
Overshoot	Note 14	25	-	17	-	%
Propagation Delay		25	-	50	-	ns
Settling Time (To 0.1%)	Note 13	25	-	200	-	ns
V_Z CHARACTERISTICS						
Input Offset Voltage	$V_X = V_Y = 0V$	25	-	4	15	mV
		Full	-	8	20	mV
Open Loop Gain		25	-	70	-	dB
Differential Input Resistance		25	-	900	-	kΩ
OUTPUT CHARACTERISTICS						
Output Voltage Swing	$V_X = 2.5V$, $V_Y = \pm5V$	Full	-	±6.25	-	V
Output Current		Full	±20	±45	-	mA
Output Resistance		25	-	1	-	Ω

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L = 50pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
POWER SUPPLY						
PSRR	Note 8	Full	58	63	-	dB
Supply Current		Full	-	23	29	mA

NOTES:

2. Error is percent of full scale, 1% = 50mV.
3. $f_O = 3.58MHz/4.43MHz$, $V_Y = 300mV_{P-P}$, 0 to $1V_{DC}$ offset, $V_X = 2V$.
4. $f_O = 10kHz$, $V_Y = 1V_{RMS}$, $V_X = 2V$.
5. Full Power Bandwidth calculated by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, $V_{PEAK} = 5V$.
6. $V_Y = 0$ to $\pm5V$, $V_X = 2V$.
7. $V_{OUT} = 0$ to $\pm100mV$, $V_X = 2V$.
8. $V_S = \pm12V$ to $\pm15V$, $V_Y = 5V$, $V_X = 2V$.
9. Guaranteed by characterization and not 100% tested.
10. See Test Circuit.
11. $f_O = 5MHz$, $V_X = 0$, $V_Y = 200mV_{RMS}$.
12. $f_O = 100kHz$, $V_Y = 0$, $V_{X+} = 200mV_{RMS}$, $V_{X-} = -0.5V$.
13. $V_X = 0$ to $2V$, $V_Y = 5V$.
14. $V_X = 0$ to $200mV$, $V_Y = 5V$.

Test Circuits and Waveforms

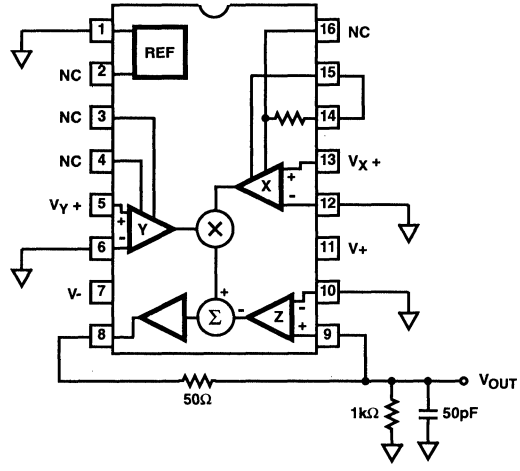
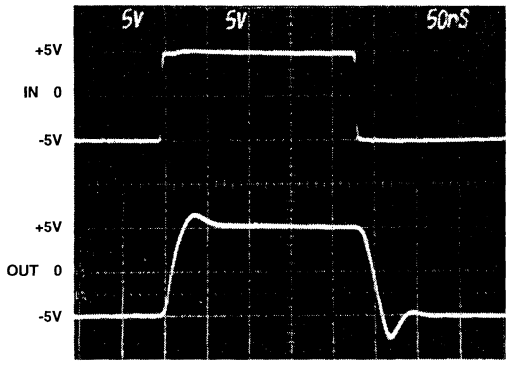
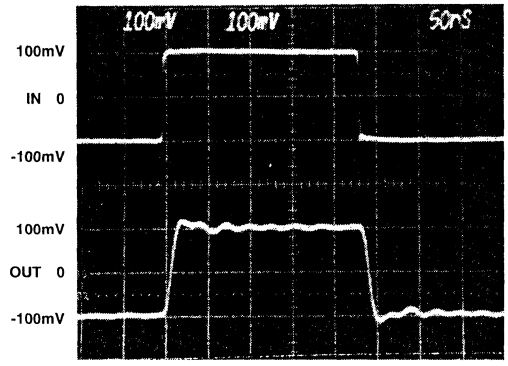


FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

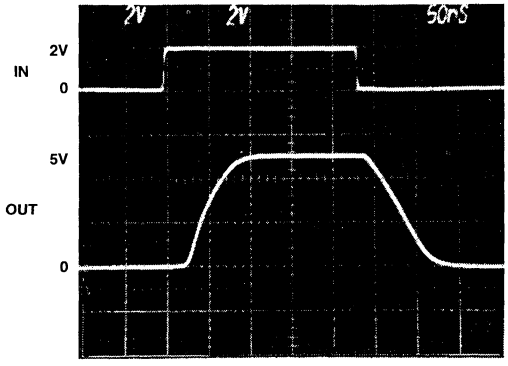
Test Circuits and Waveforms (Continued)



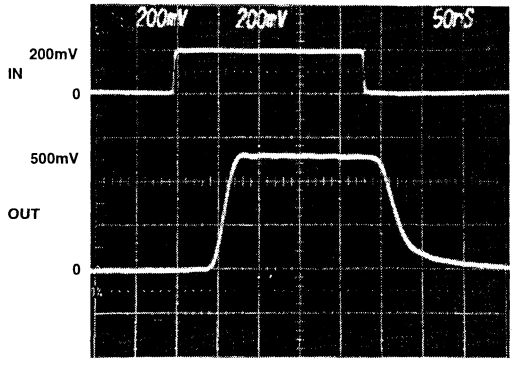
Vertical Scale: 5V/Div.; Horizontal Scale: 50ns/Div.
V_Y LARGE SIGNAL RESPONSE



Vertical Scale: 100mV/Div.; Horizontal Scale: 50ns/Div.
V_Y SMALL SIGNAL RESPONSE



Vertical Scale: 2V/Div.; Horizontal Scale: 50ns/Div.
V_X LARGE SIGNAL RESPONSE



Vertical Scale: 200mV/Div.; Horizontal Scale: 50ns//Div.
V_X SMALL SIGNAL RESPONSE

Application Information

Theory of Operation

The HA-2546 is a two quadrant multiplier with the following three differential inputs; the signal channel, V_{Y+} and V_{Y-}, the control channel, V_{X+} and V_{X-}, and the summed channel, V_{Z+} and V_{Z-}, to complete the feedback of the output amplifier. The differential voltages of channel X and Y are converted to differential currents. These currents are then multiplied in a circuit similar to a Gilbert Cell multiplier, producing a differential current product. The differential voltage of the Z channel is converted into a differential current which then sums with the products currents. The differential "product/sum" currents are converted to a single-ended current and then converted to a voltage output by a transimpedance amplifier.

The open loop transfer equation for the HA-2546 is:

$$V_{OUT} = A\left[\frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{SF} - (V_{Z+} - V_{Z-})\right]$$

where;

A = Output Amplifier Open Loop Gain
SF = Scale Factor
V_X, V_Y, V_Z = Differential Inputs

The scale factor is used to maintain the output of the multiplier within the normal operating range of ±5V. The scale factor can be defined by the user by way of an optional external resistor, R_{EXT}, and the Gain Adjust pins, Gain Adjust A (GA

A), Gain Adjust B (GA B), and Gain Adjust C (GA C). The scale factor is determined as follows:

SF = 2, when GA B is shorted to GA C

SF ≅ 1.2 R_{EXT}, when R_{EXT} is connected between GA A and GA C (R_{EXT} is in kΩ)

SF ≅ 1.2 (R_{EXT} + 1.667kΩ), when R_{EXT} is connected to GA B and GA C (R_{EXT} is in kΩ)

The scale factor can be adjusted from 2 to 5. It should be noted that any adjustments to the scale factor will affect the AC performance of the control channel, V_X. The normal input operating range of V_X is equal to the scale factor voltage.

The typical multiplier configuration is shown in Figure 2. The ideal transfer function for this configuration is:

$$V_{OUT} = \begin{cases} \dfrac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{2} + V_{Z-}, & \text{when } V_X \geq 0V \\ 0, & \text{when } V_X < 0V \end{cases}$$

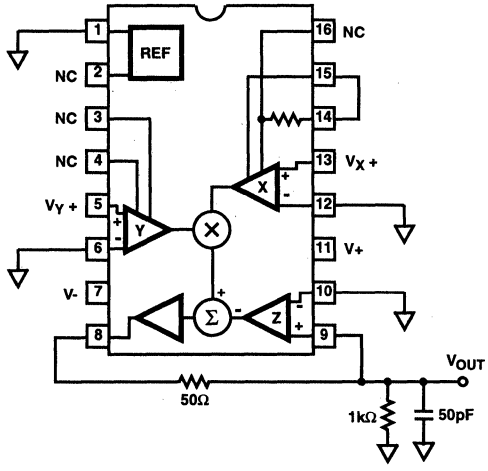


FIGURE 2.

The V_{X-} pin is usually connected to ground so that when V_{X+} is negative there is no signal at the output, i.e. two quadrant operation. If the V_X input is a negative going signal the V_{X+} pin maybe grounded and the V_{X-} pin used as the control input.

The V_{Y-} terminal is usually grounded allowing the V_{Y+} to swing ±5V. The V_{Z+} terminal is usually connected directly to V_{OUT} to complete the feedback loop of the output amplifier while V_{Z-} is grounded. The scale factor is normally set to 2 by connecting GA B to GA C. Therefore the transfer equation simplifies to $V_{OUT} = (V_X V_Y) / 2$.

Offset Adjustment

The signal channel offset voltage may be nulled by using a 20kΩ potentiometer between V_{YIO} Adjust pins A and B and connecting the wiper to V-. Reducing the signal channel offset will reduce V_X AC feedthrough. Output offset voltage can also be nulled by connecting V_{Z-} to the wiper of a 20kΩ potentiometer which is tied between V+ and V-.

Capacitive Drive Capability

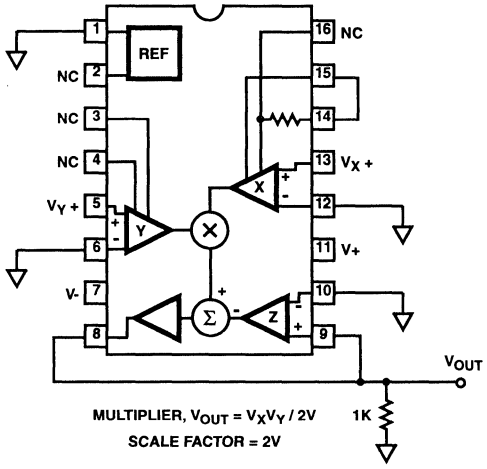
When driving capacitive loads >20pF, a 50Ω resistor is recommended between V_{OUT} and V_{Z+}, using V_{Z+} as the output (see Figure 2). This will prevent the multiplier from going unstable.

Power Supply Decoupling

Power supply decoupling is essential for high frequency circuits. A 0.01µF high quality ceramic capacitor at each supply pin in parallel with a 1µF tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to the close spacing with which they may be placed to the supply pins minimizing lead inductance.

Adjusting Scale Factor

Adjusting the scale factor will tailor the control signal, V_X, input voltage range to match your needs. Referring to the simplified schematic on the front page and looking for the V_X input stage, you will notice the unusual design. The internal reference sets up a 1.2mA current sink for the V_X differential pair. The control signal applied to this input will be forced across the scale factor setting resistor and set the current flowing in the V_{X+} side of the differential pair. When the current through this resistor reaches 1.2mA, all the current available is flowing in the one side and full scale has been reached. Normally the 1.67kΩ internal resistor sets the scale factor to 2V when the Gain Adjust pins B and C are connected together, but you may set this resistor to any convenient value using pins 16 (GA A) and 15 (GA C) (See Figure 3).



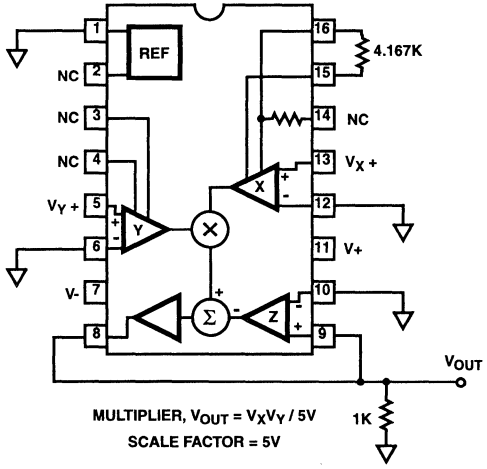


FIGURE 3. SETTING THE SCALE FACTOR

Typical Applications

Automatic Gain Control

In Figure 4 the HA-2546 is configured in a true Automatic Gain Control or AGC application. The HA-5127, low noise op amp, provides the gain control level to the X input. This level will set the peak output voltage of the multiplier to match the reference level. The feedback network around the HA-5127 provides stability and a response time adjustment for the gain control circuit.

This multiplier has the advantage over other AGC circuits, in that the signal bandwidth is not affected by the control signal gain adjustment.

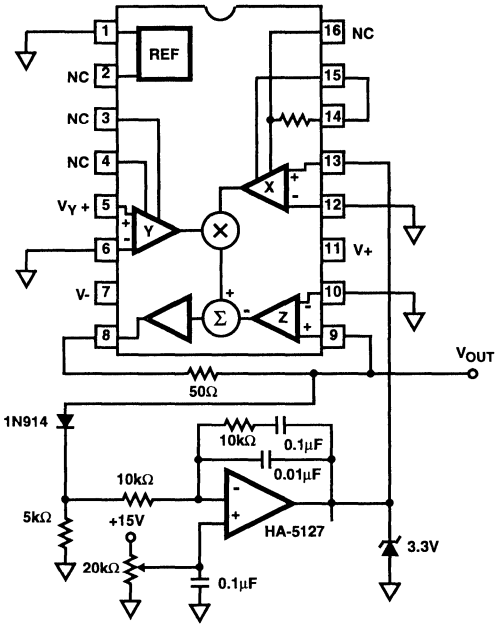


FIGURE 4. AUTOMATIC GAIN CONTROL

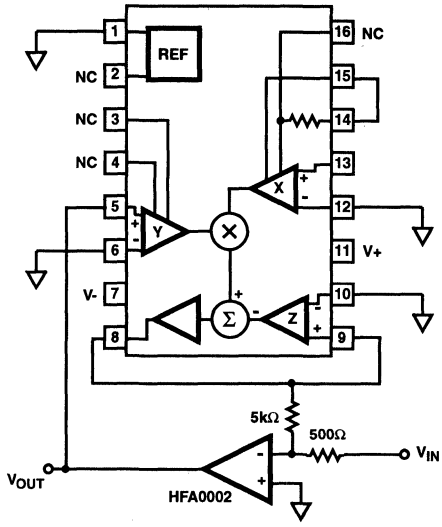
Voltage Controlled Amplifier

A wide range of gain adjustment is available with the Voltage Controlled Amplifier configuration shown in Figure 5. Here the gain of the HFA0002 is swept from 20V/V at a control voltage of 0.902V to a gain of almost 1000V/V with a control voltage of 0.03V.

Video Fader

The Video Fader circuit provides a unique function. Here Ch B is applied to the minus Z input in addition to the minus Y input. In this way, the function in Figure 6 is generated. V_{MIX} will control the percentage of Ch A and Ch B that are mixed together to produce a resulting video image or other signal.

Many other applications are possible including division, squaring, square-root, percentage calculations, etc. Please refer to the HA-2556 four quadrant multiplier data sheet for additional applications.



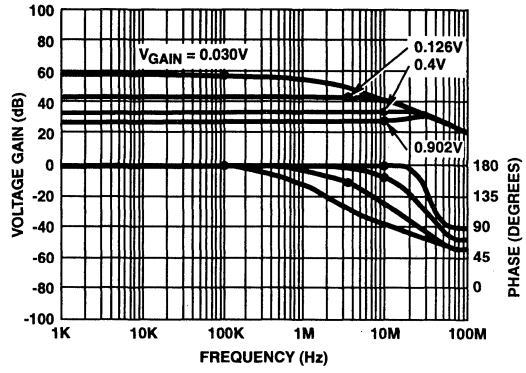
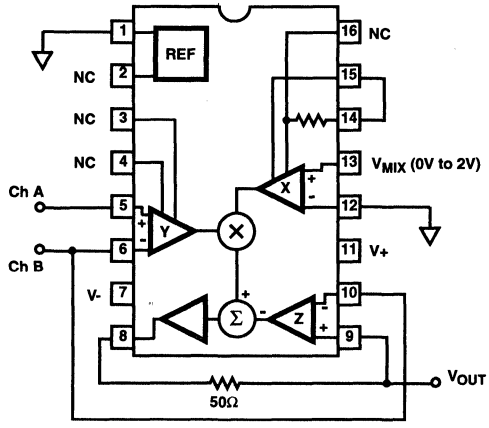


FIGURE 5. VOLTAGE CONTROLLED AMPLIFIER



V_{OUT} = Ch B + (Ch A - Ch B) V_{MIX} / Scale Factor

Scale Factor = 2

V_{OUT} = All Ch B; if V_{MIX} = 0V

V_{OUT} = All Ch A; if V_{MIX} = 2V (Full Scale)

V_{OUT} = Mix of Ch A and Ch B; if 0V < V_{MIX} < 2V

FIGURE 6. VIDEO FADER

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$, See Test Circuit For Multiplier Configuration

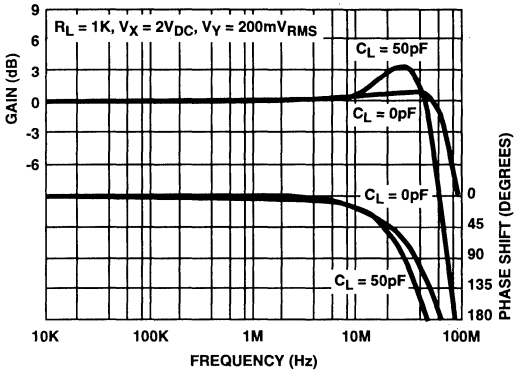


FIGURE 7. V_Y GAIN AND PHASE vs FREQUENCY

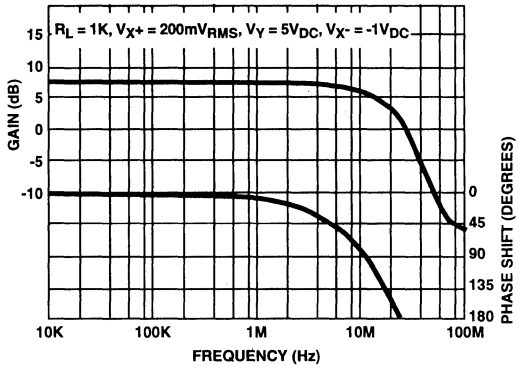


FIGURE 8. V_X GAIN AND PHASE vs FREQUENCY

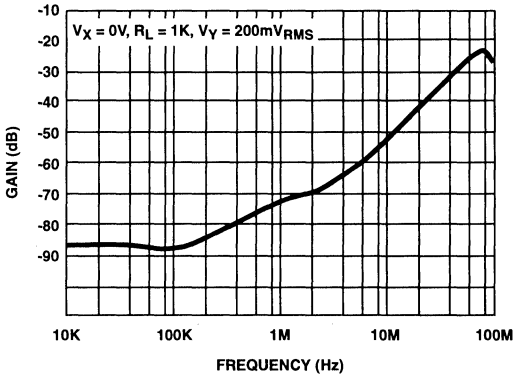


FIGURE 9. V_Y FEEDTHROUGH vs FREQUENCY

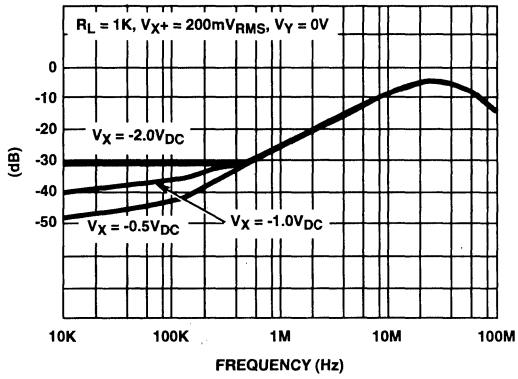


FIGURE 10. V_X FEEDTHROUGH vs FREQUENCY

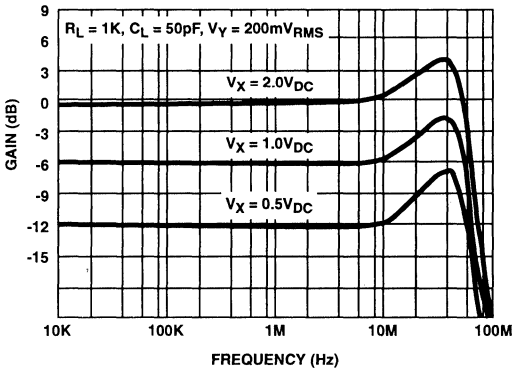


FIGURE 11. VARIOUS V_Y FREQUENCY RESPONSES

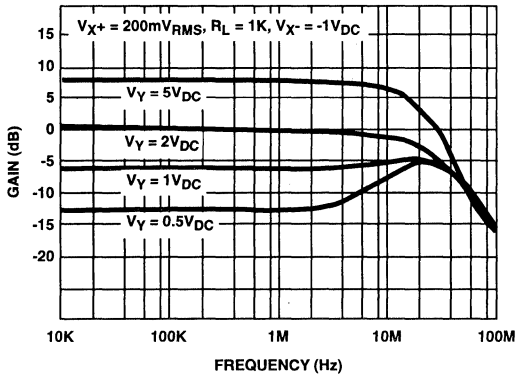


FIGURE 12. VARIOUS V_X FREQUENCY RESPONSES

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, See Test Circuit For Multiplier Configuration (Continued)

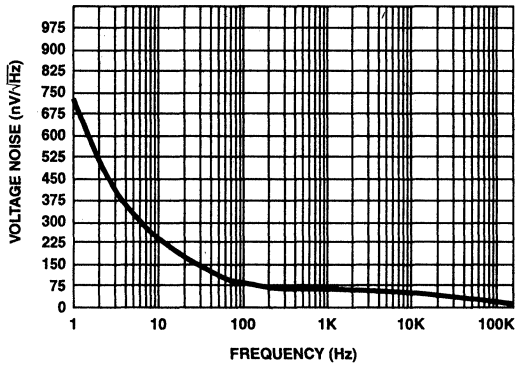


FIGURE 13. VOLTAGE NOISE DENSITY

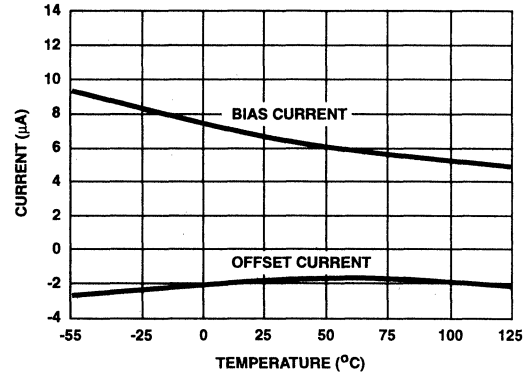


FIGURE 14. V_Y OFFSET AND BIAS CURRENT vs TEMPERATURE

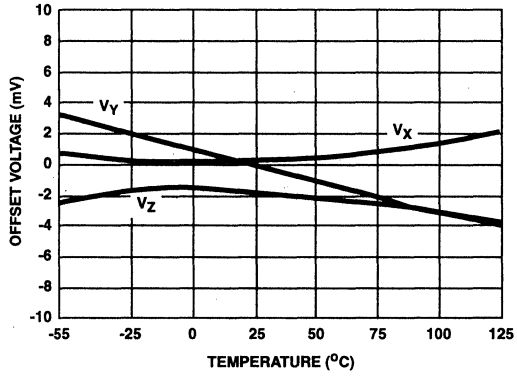


FIGURE 15. OFFSET VOLTAGE vs TEMPERATURE

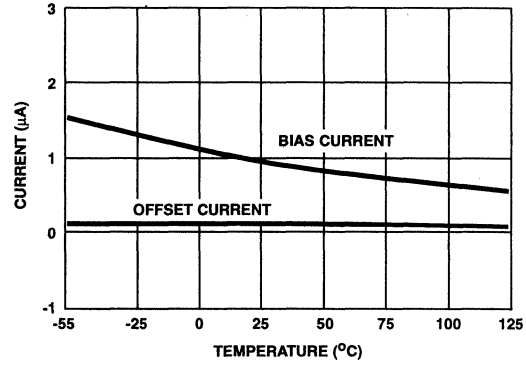


FIGURE 16. V_X OFFSET AND BIAS CURRENT vs TEMPERATURE

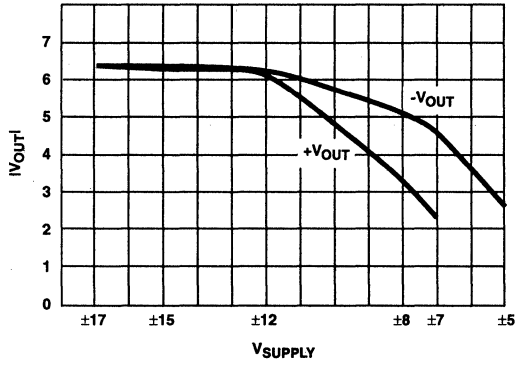


FIGURE 17. V_{OUT} vs V_{SUPPLY}

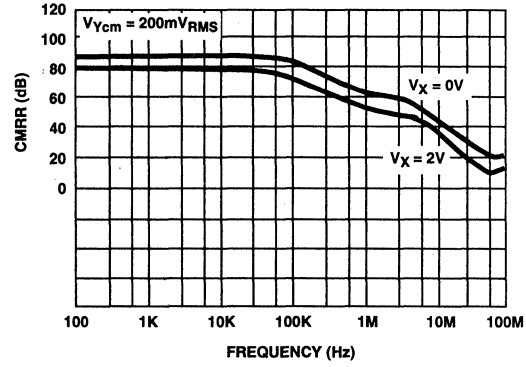


FIGURE 18. V_Y CMRR vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, See Test Circuit For Multiplier Configuration (Continued)

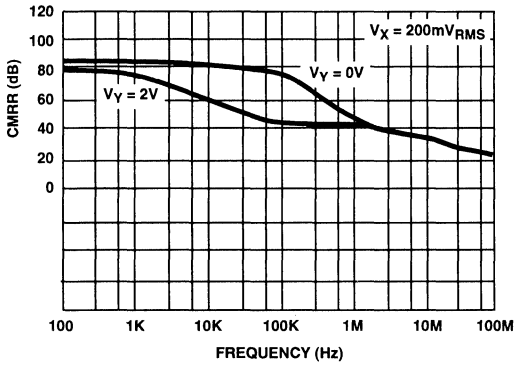


FIGURE 19. V_X COMMON MODE REJECTION RATIO vs FREQUENCY

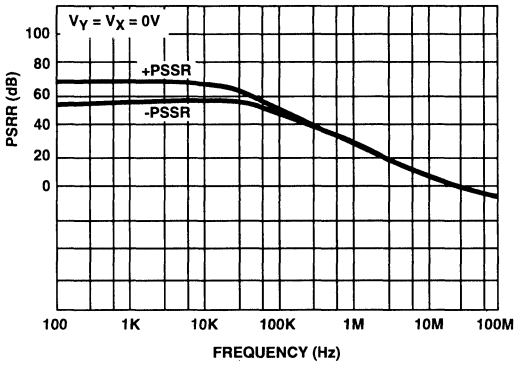


FIGURE 20. PSRR vs FREQUENCY

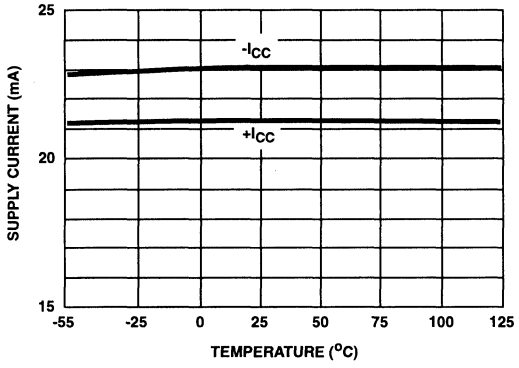


FIGURE 21. SUPPLY CURRENT vs TEMPERATURE

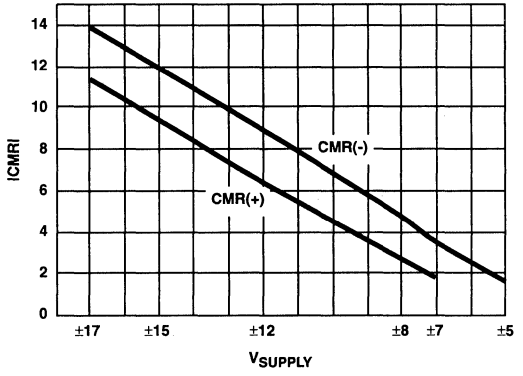


FIGURE 22. CMR vs V_{SUPPLY}

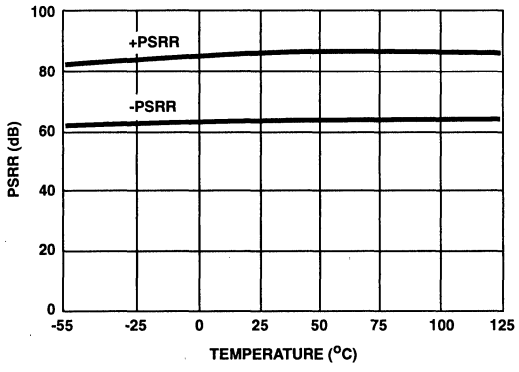


FIGURE 23. PSRR vs TEMPERATURE

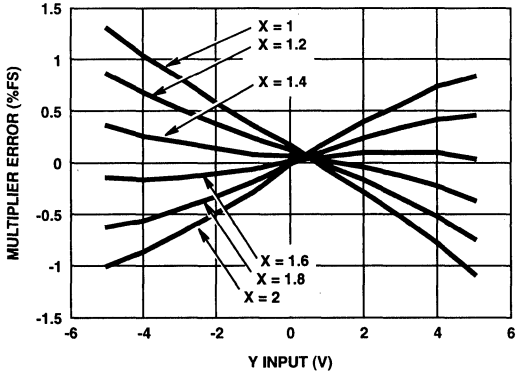


FIGURE 24. MULTIPLICATION ERROR vs V_Y

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$, See Test Circuit For Multiplier Configuration (Continued)

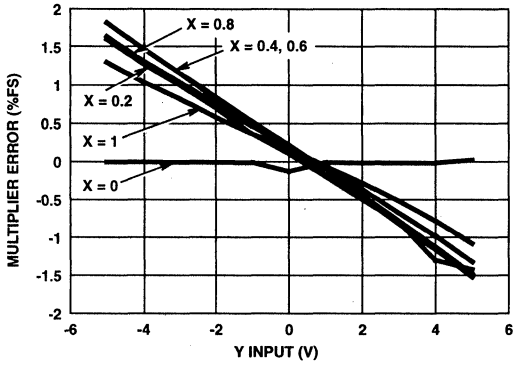


FIGURE 25.

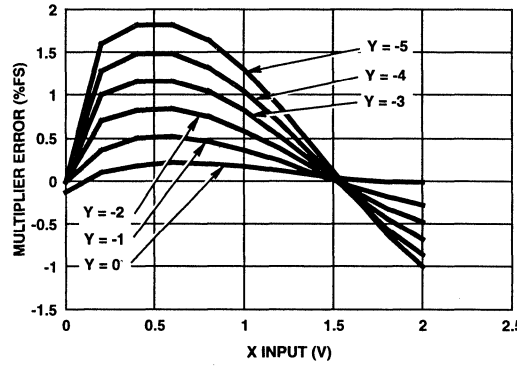


FIGURE 26.

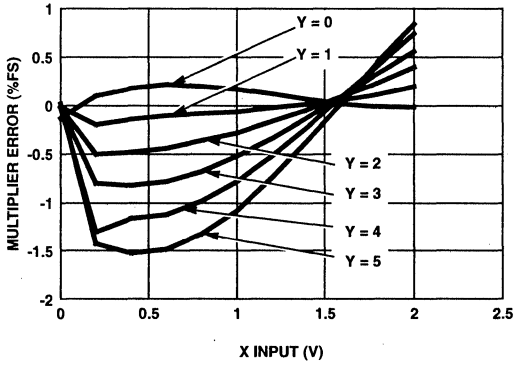


FIGURE 27.

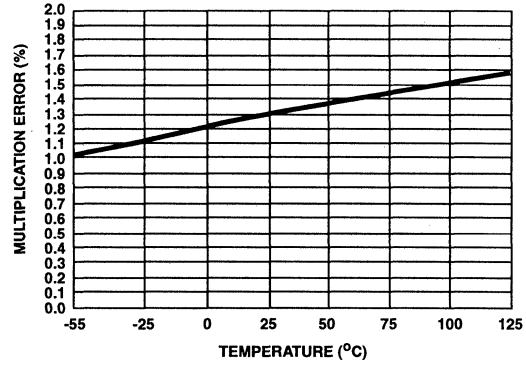


FIGURE 28. WORST CASE MULTIPLICATION ERROR vs TEMPERATURE

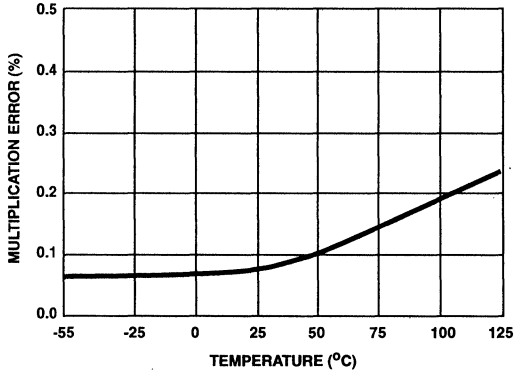


FIGURE 29. MULTIPLICATION ERROR vs TEMPERATURE

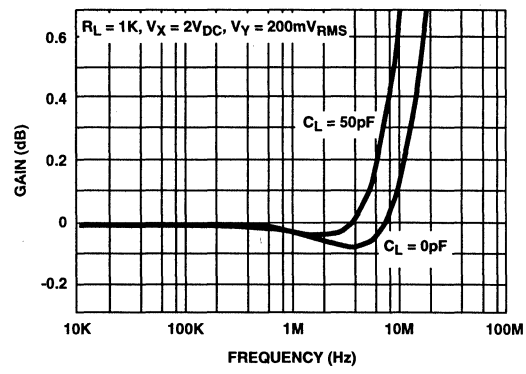


FIGURE 30. GAIN VARIATION vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, See Test Circuit For Multiplier Configuration (Continued)

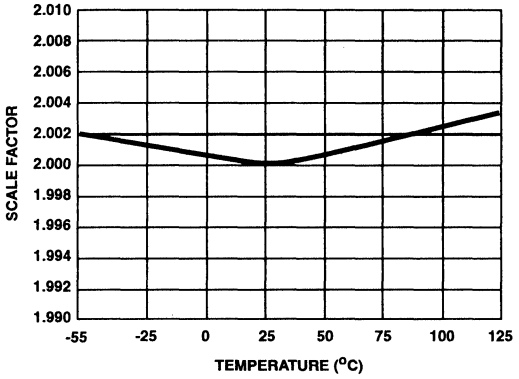


FIGURE 31. SCALE FACTOR vs TEMPERATURE

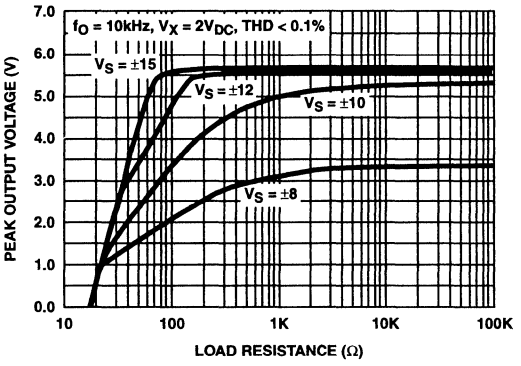


FIGURE 32. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

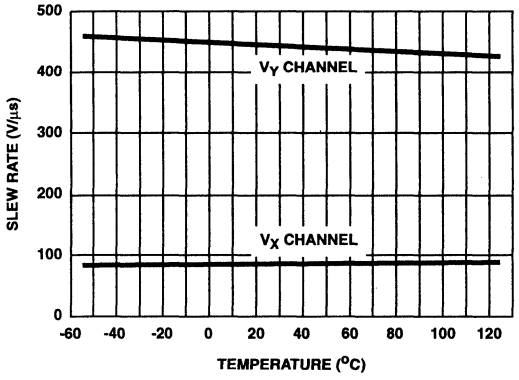


FIGURE 33. SLEW RATE vs TEMPERATURE

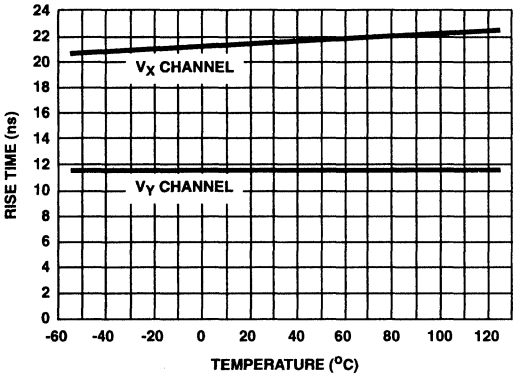


FIGURE 34. RISE TIME vs TEMPERATURE

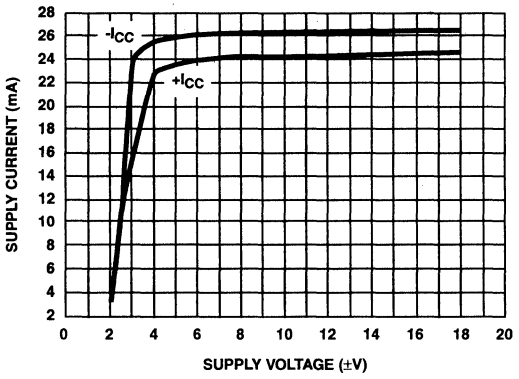


FIGURE 35. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

79.9 mils x 119.7 mils x 19 mils

METALLIZATION:

Type: Al, 1% Cul
Thickness: 16kÅ ±2kÅ

PASSIVATION:

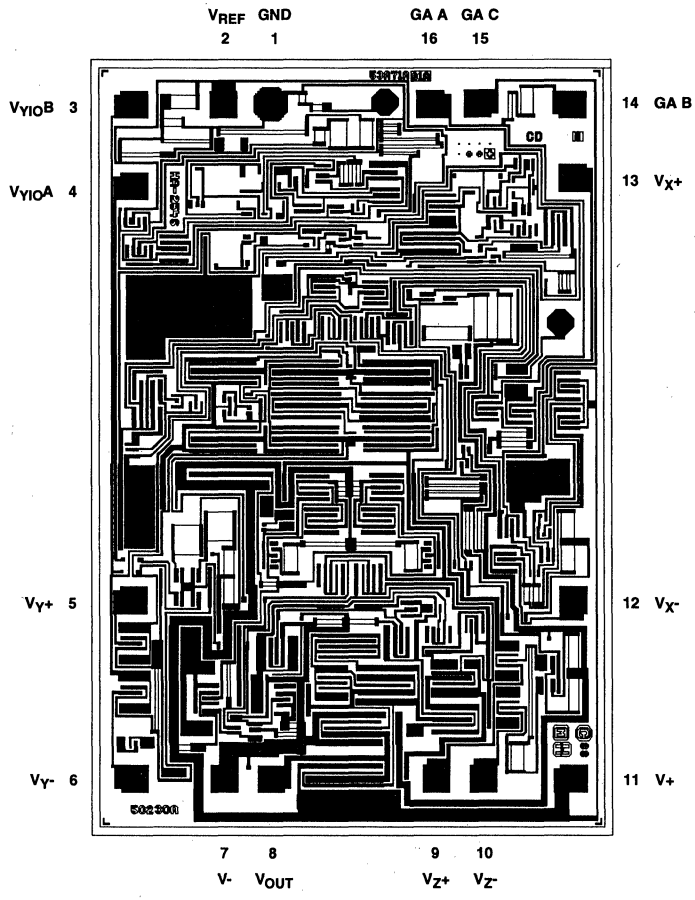
Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±2kÅ

TRANSISTOR COUNT:

87

Metallization Mask Layout

HA-2546



NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HA-2547

100MHz, Two Quadrant, Current Output, Analog Multiplier

November 1996

Features

- Low Multiplication Error 1.6%
- Input Bias Currents 1.2µA
- Signal Input Feedthrough at 5MHz. . . . . -50dB
- Wide Signal Bandwidth 100MHz
- Wide Control Bandwidth 22MHz

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-2547-5	0 to 75	16 Ld CERDIP	F16.3
HA1-2547-9	-40 to 85	16 Ld CERDIP	F16.3

Description

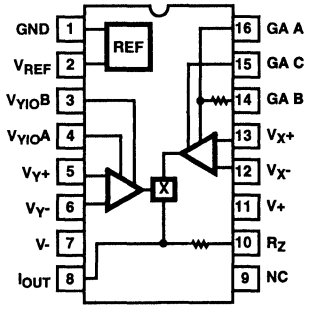
The HA-2547 is a monolithic, high speed, two quadrant, analog multiplier constructed in Harris' Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2547 rivals the best analog multipliers currently available including hybrids.

The single-ended current output of the HA-2547 has a 100MHz signal bandwidth (R_L = 50Ω) and a 22MHz control input bandwidth. High bandwidth and low distortion make this part an ideal component in video systems. The suitability for precision video applications is demonstrated further by low multiplication error (1.6%), low feedthrough (-50dB), and differential inputs with low bias currents (1.2µA). The HA-2547 is also well suited for mixer circuits as well as AGC applications for sonar, radar, and medical imaging equipment.

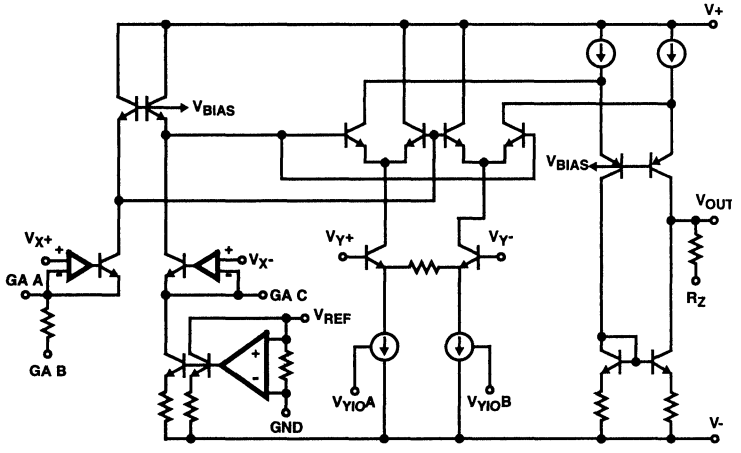
The current output of the HA-2547 allows it to achieve higher bandwidths than voltage output multipliers. An internal feedback resistor is provided to give an accurate current-to-voltage conversion and is trimmed to give a full scale output voltage of ±5V. The HA-2547 is not limited to multiplication applications only; frequency doubling and power detection are also possible.

Pinout

HA-2547
(CERDIP)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 2862.2

HARRIS SEMICONDUCTOR

HA-2556

57MHz, Wideband, Four Quadrant, Voltage Output Analog Multiplier

November 1996

Features

- High Speed Voltage Output 450V/µs
- Low Multiplication Error 1.5%
- Input Bias Currents 8µA
- 5MHz Feedthrough . . . . . -50dB
- Wide Y Channel Bandwidth 57MHz
- Wide X Channel Bandwidth 52MHz
- V_Y 0.1dB Gain Flatness 5.0MHz

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generators

Description

The HA-2556 is a monolithic, high speed, four quadrant, analog multiplier constructed in the Harris Dielectrically Isolated High Frequency Process. The voltage output simplifies many designs by eliminating the current-to-voltage conversion stage required for current output multipliers. The HA-2556 provides a 450V/µs slew rate and maintains 52MHz and 57MHz bandwidths for the X and Y channels respectively, making it an ideal part for use in video systems.

The suitability for precision video applications is demonstrated further by the Y Channel 0.1dB gain flatness to 5.0MHz, 1.5% multiplication error, -50dB feedthrough and differential inputs with 8µA bias current. The HA-2556 also has low differential gain (0.1%) and phase (0.1°) errors.

The HA-2556 is well suited for AGC circuits as well as mixer applications for sonar, radar, and medical imaging equipment. The HA-2556 is not limited to multiplication applications only; frequency doubling, power detection, as well as many other configurations are possible.

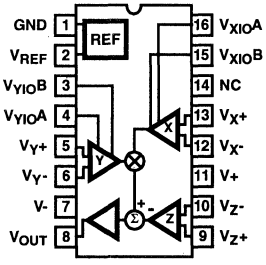
For MIL-STD-883 compliant product consult the HA-2556/883 datasheet.

Ordering Information

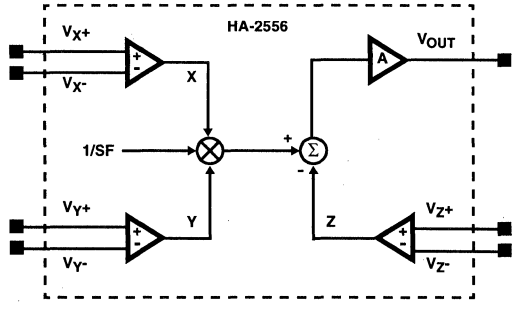
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3-2556-9	-40 to 85	16 Ld PDIP	E16.3
HA9P2556-9	-40 to 85	16 Ld SOIC	M16.3
HA1-2556-9	-40 to 85	16 Ld CERDIP	F16.3

Pinout

HA-2556
(PDIP, CERDIP, SOIC)
TOP VIEW



Functional Block Diagram



NOTE: The transfer equation for the HA-2556 is:
$(V_{X+} - V_{X-})(V_{Y+} - V_{Y-}) = S_F (V_{Z+} - V_{Z-})$,
where SF = Scale Factor = 5V; V_X, V_Y, V_Z = Differential Inputs.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **2477.4**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage. 6V
Output Current . . . . . ±60mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	77	N/A
SOIC Package	90	N/A
CERDIP Package	75	20

Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Packages) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15V, R_F = 50Ω, R_L = 1kΩ, C_L = 20pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE						
Transfer Function		$V_{OUT} = A\left[\frac{(V_{X+} - V_{X-}) \times (V_{Y+} - V_{Y-})}{5} - (V_{Z+} - V_{Z-})\right]$				
Multiplication Error	Note 2	25	-	1.5	3	%
		Full	-	3.0	6	%
Multiplication Error Drift		Full	-	0.003	-	%/°C
Scale Factor		25	-	5	-	V
Linearity Error	V_X, V_Y = ±3V, Full Scale = 3V	25	-	0.02	-	%
	V_X, V_Y = ±4V, Full Scale = 4V	25	-	0.05	0.25	%
	V_X, V_Y = ±5V, Full Scale = 5V	25	-	0.2	0.5	%
AC CHARACTERISTICS						
Small Signal Bandwidth (-3dB)	V_Y = 200mV_{P-P}, V_X = 5V	25	-	57	-	MHz
	V_X = 200mV_{P-P}, V_Y = 5V	25	-	52	-	MHz
Full Power Bandwidth (-3dB)	10V_{P-P}	25	-	32	-	MHz
Slew Rate	Note 5	25	420	450	-	V/µs
Rise Time	Note 6	25	-	8	-	ns
Overshoot	Note 6	25	-	20	-	%
Settling Time	To 0.1%, Note 5	25	-	100	-	ns
Differential Gain	Notes 3, 8	25	-	0.1	0.2	%
Differential Phase	Notes 3, 8	25	-	0.1	0.3	Degrees
V_Y 0.1dB Gain Flatness	200mV_{P-P}, V_X = 5V, Note 8	25	4.0	5.0	-	MHz
V_X 0.1dB Gain Flatness	200mV_{P-P}, V_Y = 5V, Note 8	25	2.0	4.0	-	MHz
THD + N	Note 4	25	-	0.03	-	%
1MHz Feedthrough	200mV_{P-P}, Other Ch Nulled	25	-	-65	-	dB
5MHz Feedthrough	200mV_{P-P}, Other Ch Nulled	25	-	-50	-	dB
SIGNAL INPUT (V_X, V_Y, V_Z)						
Input Offset Voltage		25	-	3	15	mV
		Full	-	8	25	mV
Average Offset Voltage Drift		Full	-	45	-	µV/°C

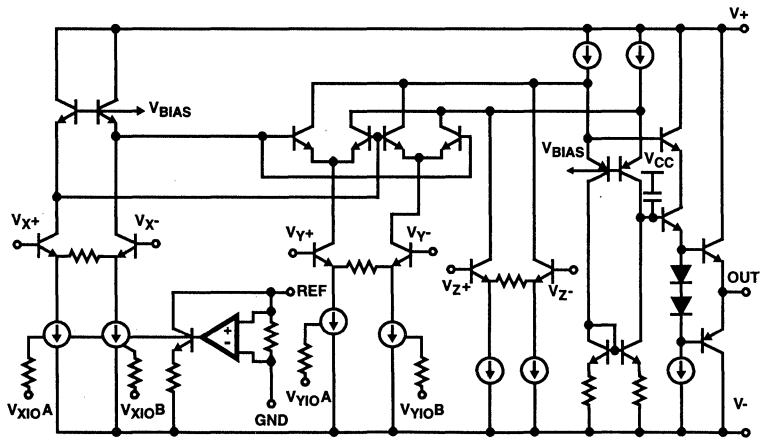
Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_F = 50\Omega$, $R_L = 1k\Omega$, $C_L = 20pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Input Bias Current		25	-	8	15	µA
		Full	-	12	20	µA
Input Offset Current		25	-	0.5	2	µA
		Full	-	1.0	3	µA
Differential Input Resistance		25	-	1	-	MΩ
Full Scale Differential Input (V_X, V_Y, V_Z)		25	±5	-	-	V
V_X Common Mode Range		25	-	±10	-	V
V_Y Common Mode Range		25	-	+9, -10	-	V
CMRR Within Common Mode Range		Full	65	78	-	dB
Voltage Noise (Note 9)	f = 1kHz	25	-	150	-	nV/√Hz
	f = 100kHz	25	-	40	-	nV/√Hz
OUTPUT CHARACTERISTICS						
Output Voltage Swing	Note 10	Full	±5.0	±6.05	-	V
Output Current		Full	±20	±45	-	mA
Output Resistance		25	-	0.7	1.0	Ω
POWER SUPPLY						
+PSRR	Note 7	Full	65	80	-	dB
-PSRR	Note 7	Full	45	55	-	dB
Supply Current		Full	-	18	22	mA

NOTES:

2. Error is percent of full scale, 1% = 50mV.
3. f = 4.43MHz, $V_Y = 300mV_{P-P}$, 0 to $1V_{DC}$ offset, $V_X = 5V$.
4. f = 10kHz, $V_Y = 1V_{RMS}$, $V_X = 5V$.
5. $V_{OUT} = 0$ to ±4V.
6. $V_{OUT} = 0$ to ±100mV.
7. $V_S = \pm12V$ to ±15V.
8. Guaranteed by characterization and not 100% tested.
9. $V_X = V_Y = 0V$.
10. $V_X = 5.5V$, $V_Y = \pm5.5V$.

Simplified Schematic



Application Information

Operation at Reduced Supply Voltages

The HA-2556 will operate over a range of supply voltages, ±5V to ±15V. Use of supply voltages below ±12V will reduce input and output voltage ranges. See "Typical Performance Curves" for more information.

Offset Adjustment

X and Y channel offset voltages may be nulled by using a 20K potentiometer between the V_{YIO} or V_{XIO} adjust pin A and B and connecting the wiper to V-. Reducing the channel offset voltage will reduce AC feedthrough and improve the multiplication error. Output offset voltage can also be nulled by connecting V_Z- to the wiper of a potentiometer which is tied between V+ and V-.

Capacitive Drive Capability

When driving capacitive loads >20pF a 50Ω resistor should be connected between V_{OUT} and V_Z+, using V_Z+ as the output (see Figure 1). This will prevent the multiplier from going unstable and reduce gain peaking at high frequencies. The 50Ω resistor will dampen the resonance formed with the capacitive load and the inductance of the output at pin 8. Gain accuracy will be maintained because the resistor is inside the feedback loop.

Theory of Operation

The HA-2556 creates an output voltage that is the product of the X and Y input voltages divided by a constant scale factor of 5V. The resulting output has the correct polarity in each of the four quadrants defined by the combinations of positive and negative X and Y inputs. The Z stage provides the means for negative feedback (in the multiplier configuration) and an input for summation into the output. This results in the following equation, where X, Y and Z are high impedance differential inputs.

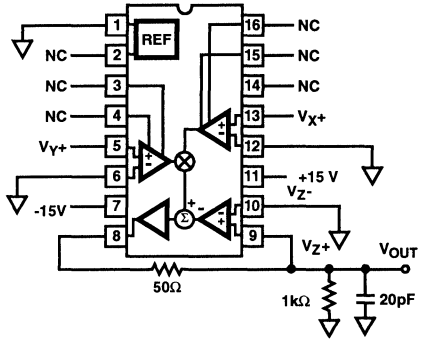


FIGURE 1. DRIVING CAPACITIVE LOAD

$$V_{OUT} = \frac{X \times Y}{5} - Z$$

To accomplish this the differential input voltages are first converted into differential currents by the X and Y input transconductance stages. The currents are then scaled by a constant reference and combined in the multiplier core. The multiplier core is a basic Gilbert Cell that produces a differential output current proportional to the product of X and Y input signal currents. This current becomes the output for the HA-2557.

The HA-2556 takes the output current of the core and feeds it to a transimpedance amplifier, that converts the current to a voltage. In the multiplier configuration, negative feedback is provided with the Z transconductance amplifier by connecting V_{OUT} to the Z input. The Z stage converts V_{OUT} to a current which is subtracted from the multiplier core before being applied to the high gain transimpedance amp. The Z stage, by virtue of it's similarity to the X and Y stages, also cancels second order errors introduced by the dependence of V_{BE} on collector current in the X and Y stages.

The purpose of the reference circuit is to provide a stable current, used in setting the scale factor to 5V. This is achieved with a bandgap reference circuit to produce a temperature stable voltage of 1.2V which is forced across a NiCr resistor. Slight adjustments to scale factor may be possible by overriding the internal reference with the V_{REF} pin. The scale factor is used to maintain the output of the multiplier within the normal operating range of ±5V when full scale inputs are applied.

The Balance Concept

The open loop transfer equation for the HA-2556 is:

$$V_{OUT} = A\left[\frac{(V_{X+} - V_{X-}) \times (V_{Y+} - V_{Y-})}{5V} - (V_{Z+} V_Z)\right]$$

where;

A	=	Output Amplifier Open Loop Gain
V_X, V_Y, V_Z	=	Differential Input Voltages
5V	=	Fixed Scaled Factor

An understanding of the transfer function can be gained by assuming that the open loop gain, A, of the output amplifier is infinite. With this assumption, any value of V_{OUT} can be generated with an infinitesimally small value for the terms within the brackets. Therefore we can write the equation:

$$0 = \frac{(V_{X+} - V_{X-}) \times (V_{Y+} - V_{Y-})}{5V} - (V_{Z+} - V_{Z-})$$

which simplifies to:

$$(V_{X+} - V_{X-}) \times (V_{Y+} - V_{Y-}) = 5V\,(V_{Z+} - V_{Z-})$$

This form of the transfer equation provides a useful tool to analyze multiplier application circuits and will be called the Balance Concept.

Typical Applications

Let's first examine the Balance Concept as it applies to the standard multiplier configuration (Figure 2).

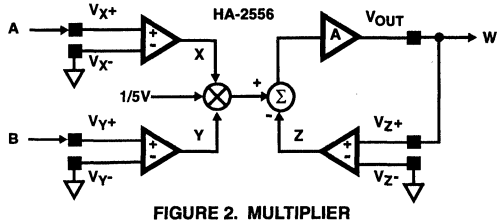


FIGURE 2. MULTIPLIER

Signals A and B are input to the multiplier and the signal W is the result. By substituting the signal values into the Balance equation you get:

$$(A) \times (B) = 5(W)$$

And solving for W:

$$W = \frac{A \times B}{5}$$

Notice that the output (W) enters the equation in the feedback to the Z stage. The Balance Equation does not test for stability, so remember that you must provide negative feedback. In the multiplier configuration, the feedback path is connected to V_{Z+} input, not V_{Z-}. This is due to the inversion that takes place at the summing node just prior to the output amplifier. Feedback is not restricted to the Z stage, other feedback paths are possible as in the Divider Configuration shown in Figure 3.

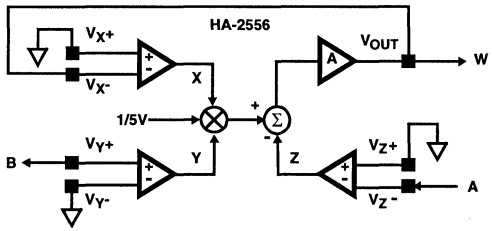


FIGURE 3. DIVIDER

Inserting the signal values A, B and W into the Balance Equation for the divider configuration yields:

$$(-W)\ (B)\ = 5V \times (-A)$$

Solving for W yields:

$$W = \frac{5A}{B}$$

Notice that, in the divider configuration, signal B must remain ≥0 (positive) for the feedback to be negative. If signal B is negative, then it will be multiplied by the V_{X-} input to produce positive feedback and the output will swing into the rail.

Signals may be applied to more than one input at a time as in the Squaring configuration in Figure 4:

Here the Balance equation will appear as:

$$(A) \times (A)\ = 5(W)$$

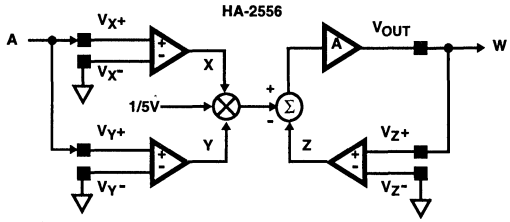


FIGURE 4. SQUARE

Which simplifies to:

$$W = \frac{A^2}{5}$$

The last basic configuration is the Square Root as shown in Figure 5. Here feedback is provided to both X and Y inputs.

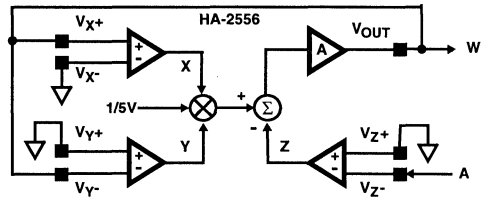


FIGURE 5. SQUARE ROOT (FOR A > 0)

The Balance equation takes the form:

$$(W) \times (-W)\ = 5(-A)$$

Which equates to:

$$W = \sqrt{5A}$$

The four basic configurations (Multiply, Divide, Square and Square Root) as well as variations of these basic circuits have many uses.

Frequency Doubler

For example, if $ACos(\omega\tau)$ is substituted for signal A in the Square function, then it becomes a Frequency Doubler and the equation takes the form:

$$(ACos(\omega\tau)) \times (ACos(\omega\tau))\ = 5(W)$$

And using some trigonometric identities gives the result:

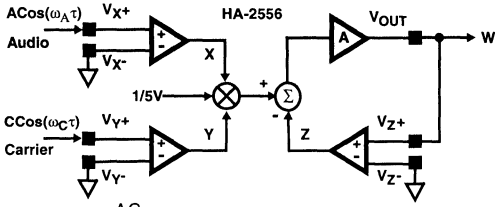
$$W = \frac{A^2}{10}(1 + Cos(2\omega\tau))$$

Square Root

The Square Root function can serve as a precision/wide bandwidth compander for audio or video applications. A compander improves the Signal to Noise Ratio for your system by amplifying low level signals while attenuating or compressing large signals (refer to Figure 17; $X^{0.5}$ curve). This provides for better low level signal immunity to noise during transmission. On the receiving end the original signal may be reconstructed with the standard Square function.

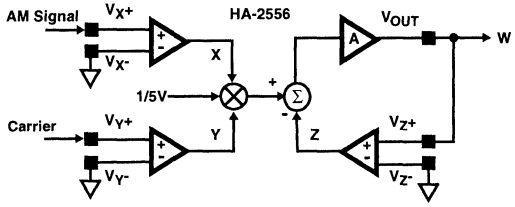
Communications

The Multiplier configuration has applications in AM Signal Generation, Synchronous AM Detection and Phase Detection to mention a few. These circuit configurations are shown in Figures 6, 7 and 8. The HA-2556 is particularly useful in applications that require high speed signals on all inputs.



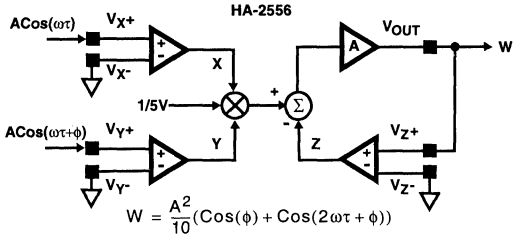
$$W = \frac{AC}{10}(\cos(\omega_C - \omega_A)\tau + \cos(\omega_C + \omega_A)\tau)$$

FIGURE 6. AM SIGNAL GENERATION



LIKE THE FREQUENCY DOUBLER YOU GET AUDIO CENTERED AT DC AND $2F_C$.

FIGURE 7. SYNCHRONOUS AM DETECTION



$$W = \frac{A^2}{10}(\cos(\phi) + \cos(2\omega\tau + \phi))$$

DC COMPONENT IS PROPORTIONAL TO COS(f)

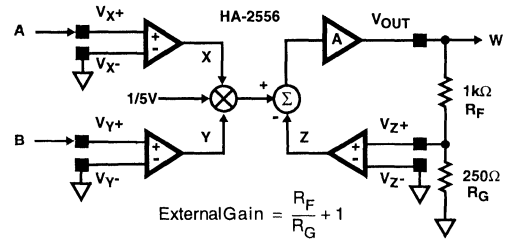
FIGURE 8. PHASE DETECTION

Each input X, Y and Z has similar wide bandwidth and input characteristics. This is unlike earlier products where one input was dedicated to a slow moving control function as is required for Automatic Gain Control. The HA-2556 is versatile enough for both.

Although the X and Y inputs have similar AC characteristics, they are not the same. The designer should consider input parameters such as small signal bandwidth, AC feedthrough and 0.1dB gain flatness to get the most performance from the HA-2556. The Y channel is the faster of the two inputs with a small signal bandwidth of typically 57MHz verses 52MHz for the X channel. Therefore in AM Signal Generation, the best performance will be obtained with the Carrier applied to the Y channel and the modulation signal (lower frequency) applied to the X channel.

Scale Factor Control

The HA-2556 is able to operate over a wide supply voltage range ±5V to ±17.5V. The ±5V range is particularly useful in video applications. At ±5V the input voltage range is reduced to ±1.4V. The output cannot reach its full scale value with this restricted input, so it may become necessary to modify the scale factor. Adjusting the scale factor may also be useful when the input signal itself is restricted to a small portion of the full scale level. Here we can make use of the high gain output amplifier by adding external gain resistors. Generating the maximum output possible for a given input signal will improve the Signal to Noise Ratio and Dynamic Range of the system. For example, let's assume that the input signals are $1V_{PEAK}$ each. Then the maximum output for the HA-2556 will be 200mV. (1V x 1V)/(5V) = 200mV. It would be nice to have the output at the same full scale as our input, so let's add a gain of 5 as shown in Figure 9.



$$\text{External Gain} = \frac{R_F}{R_G} + 1$$

FIGURE 9. EXTERNAL GAIN OF 5

One caveat is that the output bandwidth will also drop by this factor of 5. The multiplier equation then becomes:

$$W = \frac{5AB}{5} = A \times B$$

Current Output

Another useful circuit for low voltage applications allows the user to convert the voltage output of the HA2556 to an output current. The HA-2557 is a current output version offering 100MHz of bandwidth, but its scale factor is fixed and does not have an output amplifier for additional scaling. Fortunately the circuit in Figure 10 provides an output current that can be scaled with the value of $R_{CONVERT}$ and provides an output impedance of typically 1MΩ. The equation for I_{OUT} becomes:

$$I_{OUT} = \frac{A \times B}{5} \times \frac{1}{R_{CONVERT}}$$

Video Fader

The Video Fader circuit provides a unique function. Here Ch B is applied to the minus Z input in addition to the minus Y input. In this way, the function in Figure 11 is generated. V_{MIX} will control the percentage of Ch A and Ch B that are mixed together to produce a resulting video image or other signal.

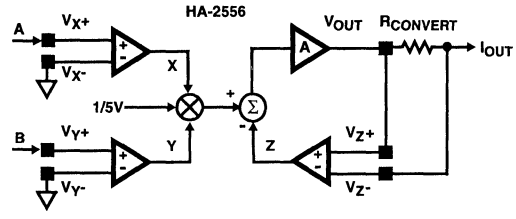


FIGURE 10. CURRENT OUTPUT

The Balance equation looks like:

$$(V_{MIX}) \times (ChA - ChB) = 5(V_{OUT} - ChB)$$

Which simplifies to:

$$V_{OUT} = ChB + \frac{V_{MIX}}{5}(ChA - ChB)$$

When V_{MIX} is 0V the equation becomes V_{OUT} = Ch B and Ch A is removed, conversely when V_{MIX} is 5V the equation becomes V_{OUT} = Ch A eliminating Ch B. For V_{MIX} values $0V \leq V_{MIX} \leq 5V$ the output is a blend of Ch A and Ch B.

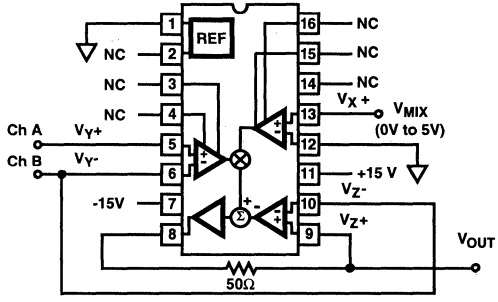


FIGURE 11. VIDEO FADER

Other Applications

As shown above, a function may contain several different operators at the same time and use only one HA-2556. Some other possible multi-operator functions are shown in Figures 12, 13 and 14.

Of course the HA-2556 is also well suited to standard multiplier applications such as Automatic Gain Control and Voltage Controlled Amplifier.

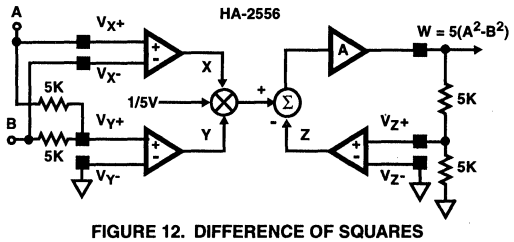
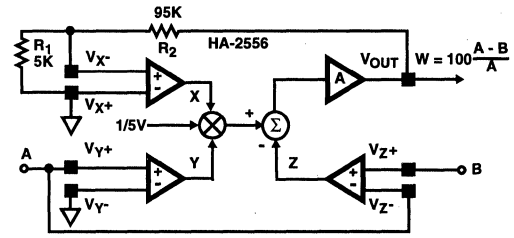


FIGURE 12. DIFFERENCE OF SQUARES



R_1 and R_2 set scale to 1V/%, other scale factors possible.
For A 0V

FIGURE 13. PERCENTAGE DEVIATION

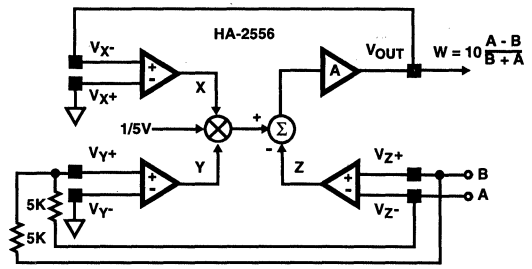


FIGURE 14. DIFFERENCE DIVIDED BY SUM (For A + B ≥ 0V)S

Automatic Gain Control

Figure 15 shows the HA-2556 configured in an Automatic Gain Control or AGC application. The HA-5127 low noise amplifier provides the gain control signal to the X input. This control signal sets the peak output voltage of the multiplier to match the preset reference level. The feedback network around the HA-5127 provides a response time adjustment. High frequency changes in the peak are rejected as noise or the desired signal to be transmitted. These signals do not indicate a change in the average peak value and therefore no gain adjustment is needed. Lower frequency changes in the peak value are given a gain of -1 for feedback to the control input. At DC the circuit is an integrator automatically compensating for Offset and other constant error terms.

This multiplier has the advantage over other AGC circuits, in that the signal bandwidth is not affected by the control signal gain adjustment.

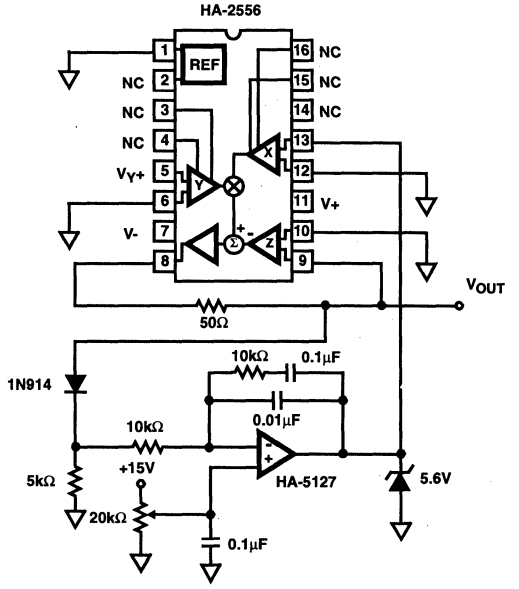


FIGURE 15. AUTOMATIC GAIN CONTROL

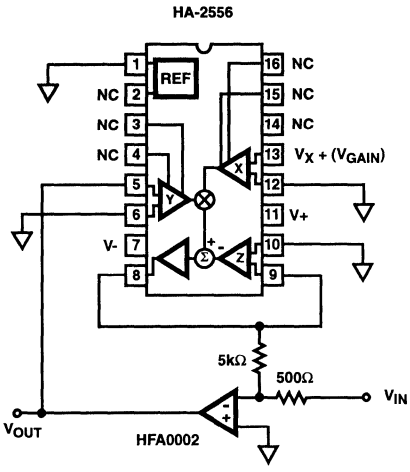


FIGURE 16. VOLTAGE CONTROLLED AMPLIFIER

Voltage Controlled Amplifier

A wide range of gain adjustment is available with the Voltage Controlled Amplifier configuration shown in Figure 16. Here the gain of the HFA0002 can be swept from 20V/V to a gain of almost 1000V/V with a DC voltage from 0V to 5V.

Wave Shaping Circuits

Wave shaping or curve fitting is another class of application for the analog multiplier. For example, where a nonlinear sensor requires corrective curve fitting to improve linearity the HA-2556 can provide nonintegral powers in the range 1 to 2 or nonintegral roots in the range 0.5 to 1.0 (refer to References). This effect is displayed in Figure 17.

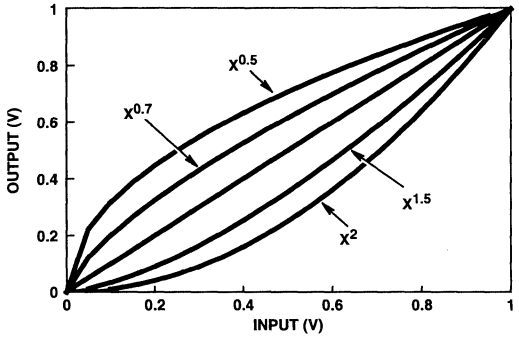


FIGURE 17. EFFECT OF NONINTEGRAL POWERS / ROOTS

A multiplier can't do nonintegral roots "exactly", but it can yield a close approximation. We can approximate nonintegral roots with equations of the form:

$$V_O = (1-\alpha)V_{IN}^2 + \alpha V_{IN}$$

$$V_O = (1-\alpha)V_{IN}^{1/2} + \alpha V_{IN}$$

Figure 18 compares the function $V_{OUT} = V_{IN}^{0.7}$ to the approximation $V_{OUT} = 0.5V_{IN}^{0.5} + 0.5V_{IN}$.

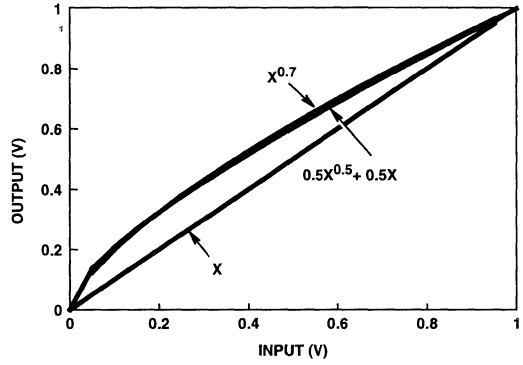


FIGURE 18. COMPARE APPROXIMATION TO NONINTEGRAL ROOT

This function can be easily built using an HA-2556 and a potentiometer for easy adjustment as shown in Figures 19 and 20. If a fixed nonintegral power is desired, the circuit shown in Figure 21 eliminates the need for the output buffer amp. These circuits approximate the function V_{IN}^M where M is the desired nonintegral power or root.

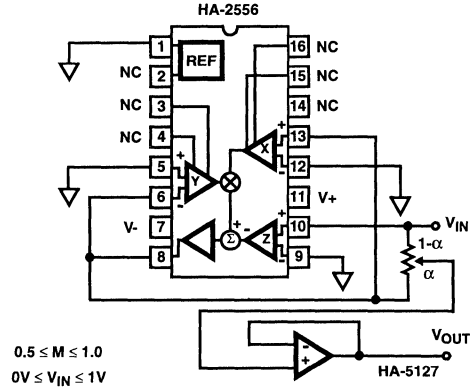


FIGURE 19. NONINTEGRAL ROOTS - ADJUSTABLE

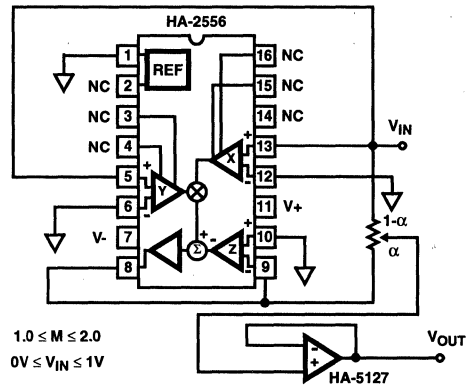


FIGURE 20. NONINTEGRAL POWERS - ADJUSTABLE

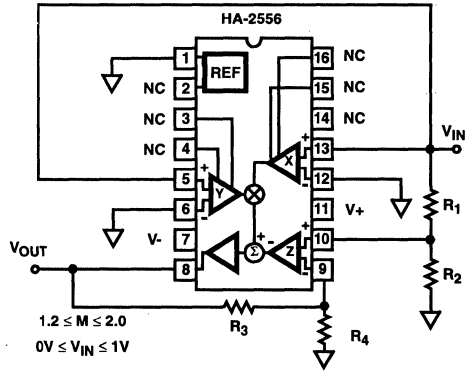


FIGURE 21. NONINTEGRAL POWERS - FIXED

$$V_{OUT} = \frac{1}{5}\left(\frac{R_3}{R_4}+1\right)V_{IN}^2 + \left(\frac{R_3}{R_4}+1\right)\left(\frac{R_2}{R_1+R_2}\right)V_{IN}$$

Setting:

$$1-\alpha = \frac{1}{5}\left(\frac{R_3}{R_4}+1\right) \qquad \alpha = \left(\frac{R_3}{R_4}+1\right)\left(\frac{R_2}{R_1+R_2}\right)$$

Values for α to give a desired M root or power are as follows:

ROOTS - FIGURE 19		POWERS - FIGURE 20	
M	α	M	α
0.5	0	1.0	1
0.6	≈0.25	1.2	≈0.75
0.7	≈0.50	1.4	≈0.5
0.8	≈0.70	1.6	≈0.3
0.9	≈0.85	1.8	≈0.15
1.0	1	2.0	0

Sine Function Generators

Similar functions can be formulated to approximate a SINE function converter as shown in Figure 22. With a linearly changing (0V to 5V) input the output will follow 0 degrees to 90 degrees of a sine function (0V to 5V) output. This configuration is theoretically capable of ±2.1% maximum error to full scale.

By adding a second HA-2556 to the circuit an improved fit may be achieved with a theoretical maximum error of 0.5% as shown in Figure 23. Figure 23 has the added benefit that it will work for positive and negative input signals. This makes a convenient triangle (±5V input) to sine wave (±5V output) converter.

References

[1] Pacifico Cofrancesco, "RF Mixers and Modulators made with a Monolithic Four-Quadrant Multiplier" Microwave Journal, December 1991 pg. 58 - 70.

[2] Richard Goller, "IC Generates Nonintegral Roots" Electronic Design, December 3, 1992.

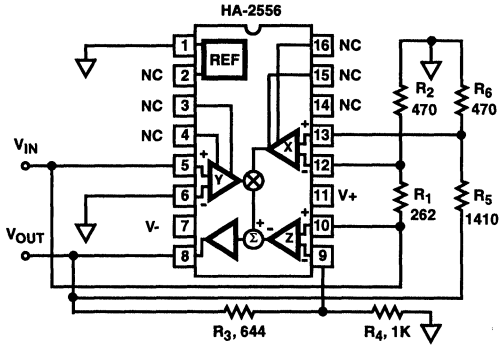


FIGURE 22. SINE-FUNCTION GENERATOR

$$V_{OUT} = V_{IN}\frac{(1-0.1284V_{IN})}{(0.6082-0.05V_{IN})} \approx 5\sin\left(\frac{\pi}{2}\cdot\frac{V_{IN}}{5}\right)$$

for; $0V \le V_{IN} \le 5V$ Max Theoretical Error = 2.1%FS

where:

$$0.6082 = \frac{R_4}{R_3+R_4}; \qquad 5(0.1284) = \frac{R_2}{R_1+R_2}$$

$$5(0.05) = \frac{R_6}{R_5+R_6}$$

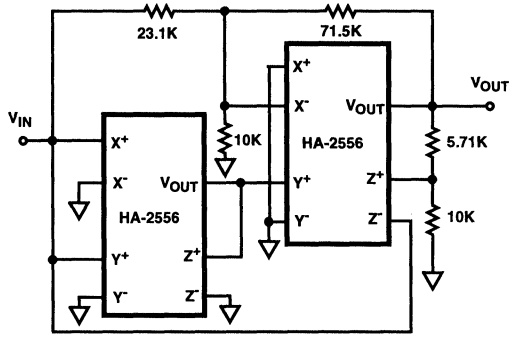


FIGURE 23. BIPOLAR SINE-FUNCTION GENERATOR

$$V_{OUT} = \frac{5V_{IN} - 0.05494V_{IN}^3}{3.18167 + 0.0177919V_{IN}^2} \approx 5\sin\left(\frac{\pi}{2}\cdot\frac{V_{IN}}{5}\right)$$

for; $-5V \le V_{IN} \le 5V$ Max Theoretical Error = 0.5%FS

Typical Performance Curves

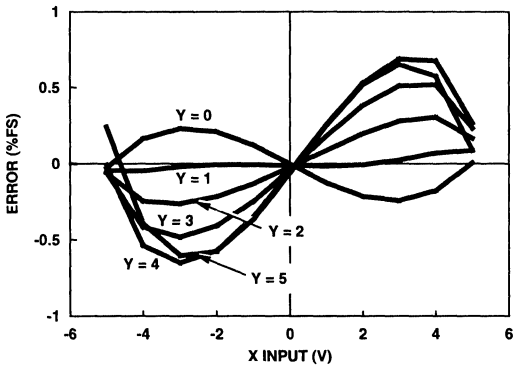


FIGURE 24. X CHANNEL MULTIPLIER ERROR

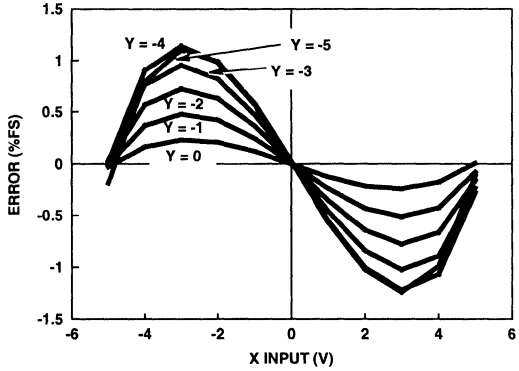


FIGURE 25. X CHANNEL MULTIPLIER ERROR

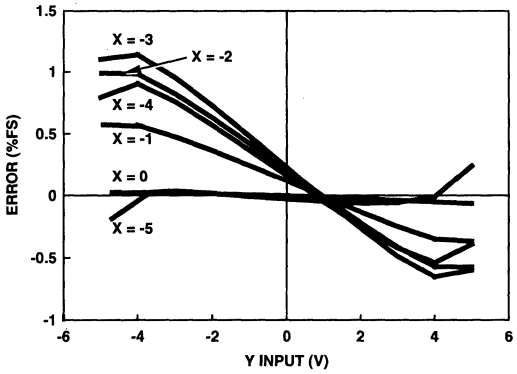


FIGURE 26. Y CHANNEL MULTIPLIER ERROR

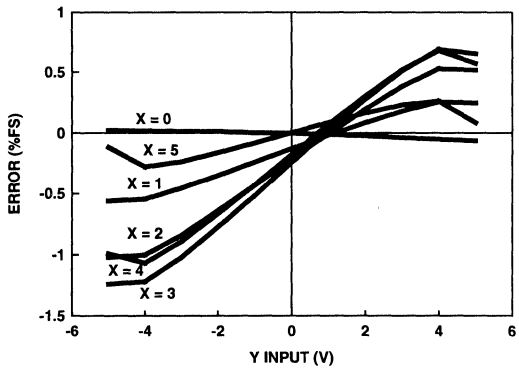


FIGURE 27. Y CHANNEL MULTIPLIER ERROR

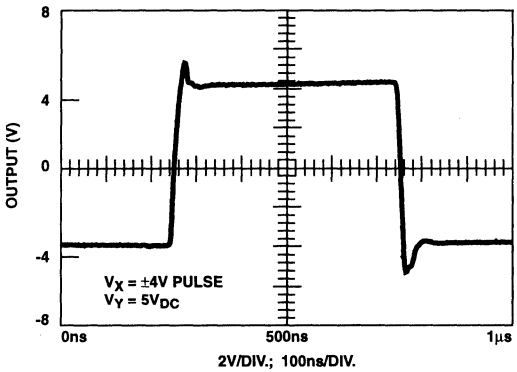


FIGURE 28. LARGE SIGNAL RESPONSE

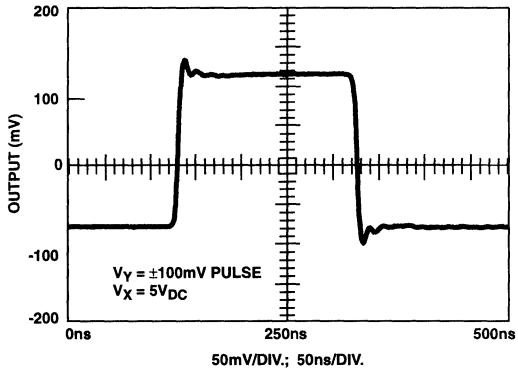


FIGURE 29. SMALL SIGNAL RESPONSE

Typical Performance Curves (Continued)

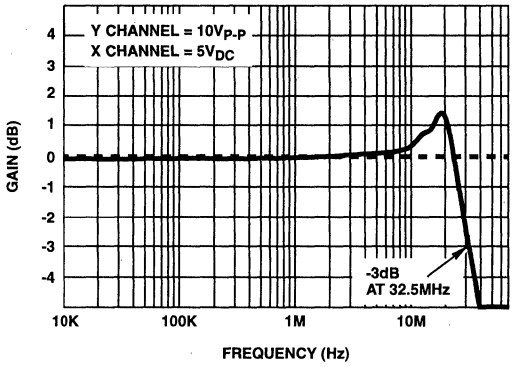


FIGURE 30. Y CHANNEL FULL POWER BANDWIDTH

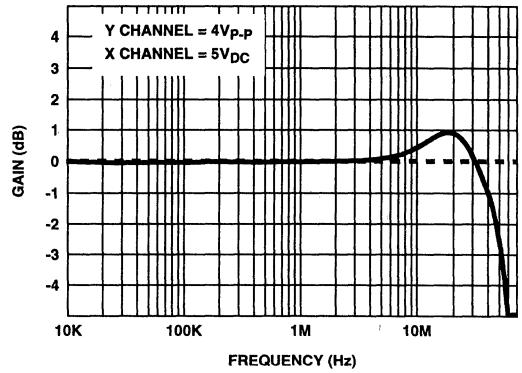


FIGURE 31. Y CHANNEL FULL POWER BANDWIDTH

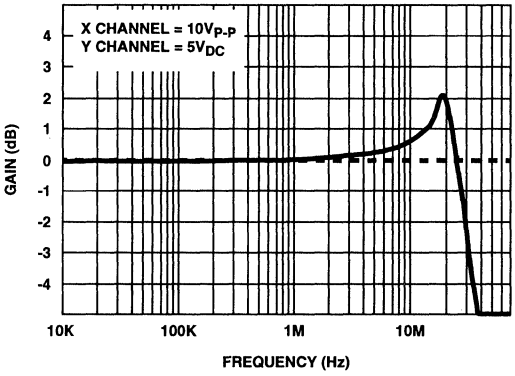


FIGURE 32. X CHANNEL FULL POWER BANDWIDTH

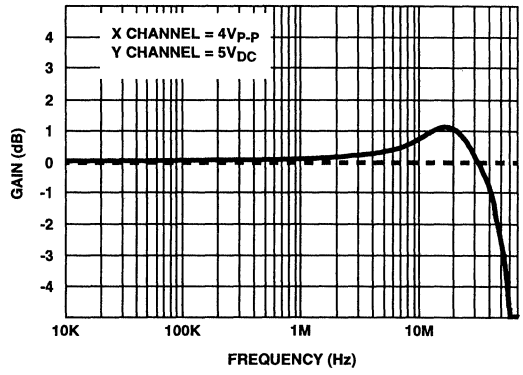


FIGURE 33. X CHANNEL FULL POWER BANDWIDTH

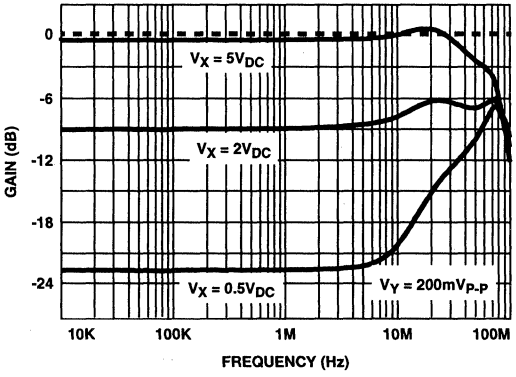


FIGURE 34. Y CHANNEL BANDWIDTH vs X CHANNEL

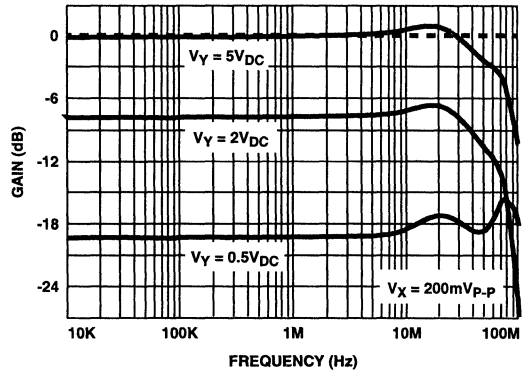


FIGURE 35. X CHANNEL BANDWIDTH vs Y CHANNEL

Typical Performance Curves (Continued)

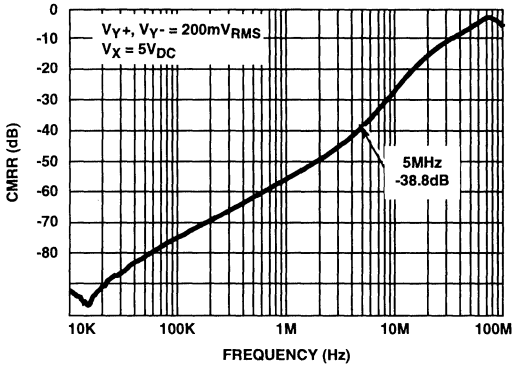


FIGURE 36. Y CHANNEL CMRR vs FREQUENCY

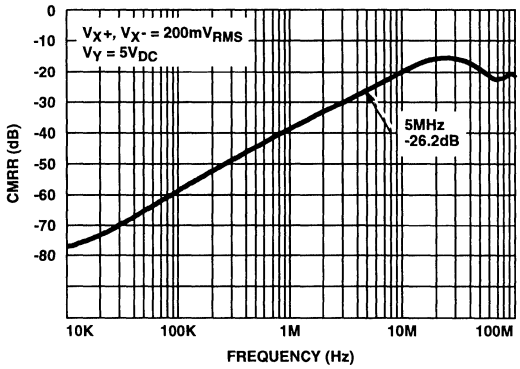


FIGURE 37. X CHANNEL CMRR vs FREQUENCY

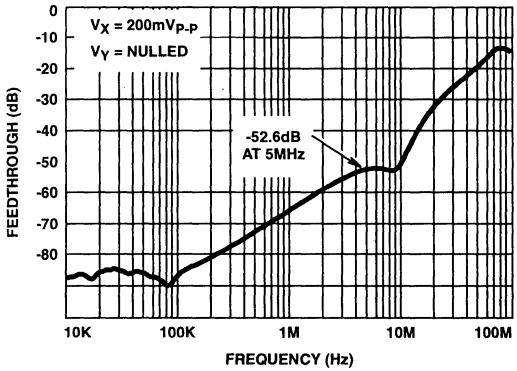


FIGURE 38. FEEDTHROUGH vs FREQUENCY

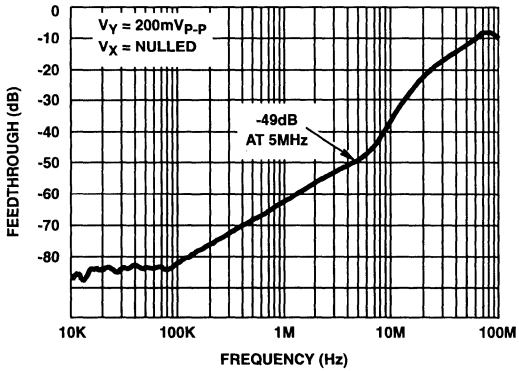


FIGURE 39. FEEDTHROUGH vs FREQUENCY

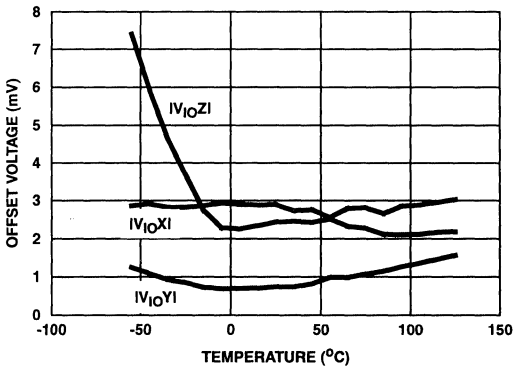


FIGURE 40. OFFSET VOLTAGE vs TEMPERATURE

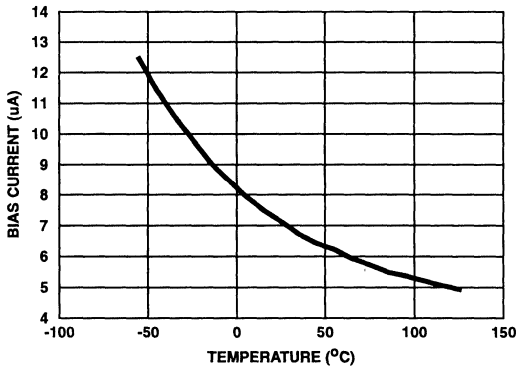


FIGURE 41. INPUT BIAS CURRENT (V_X, V_Y, V_Z) vs TEMPERATURE

Typical Performance Curves (Continued)

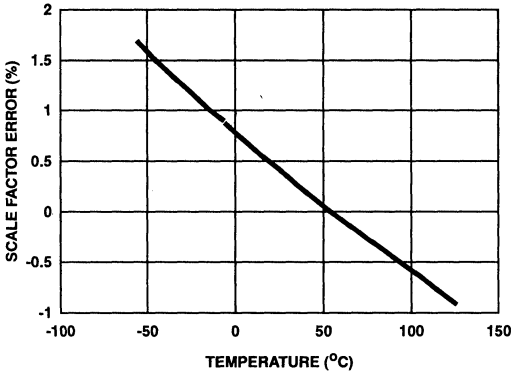


FIGURE 42. SCALE FACTOR ERROR vs TEMPERATURE

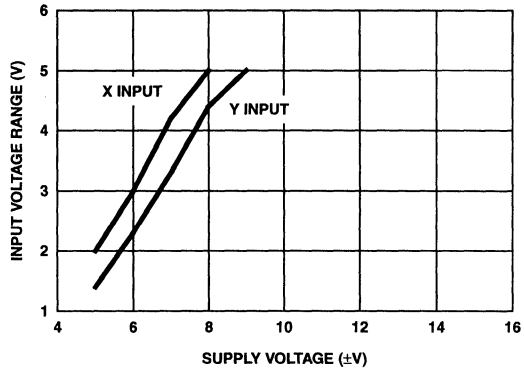


FIGURE 43. INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

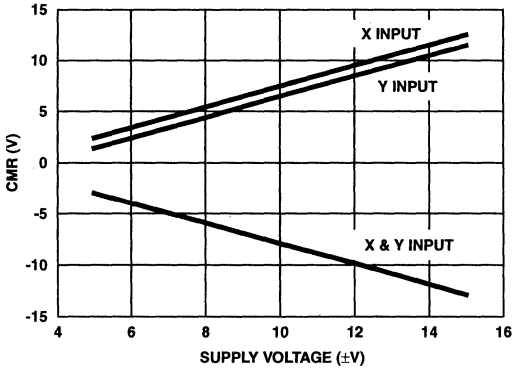


FIGURE 44. INPUT COMMON MODE RANGE vs SUPPLY VOLTAGE

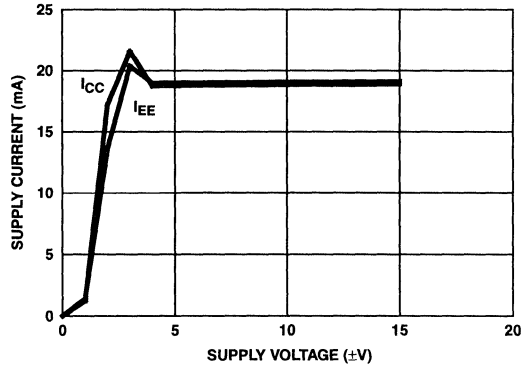


FIGURE 45. SUPPLY CURRENT vs SUPPLY VOLTAGE

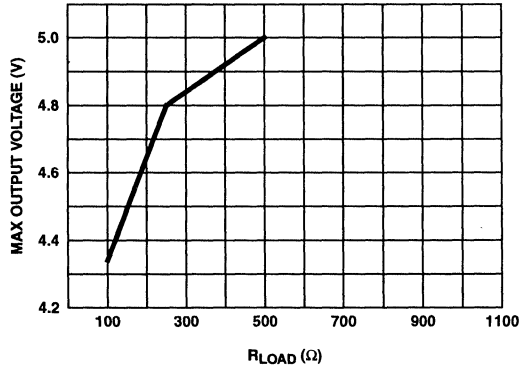


FIGURE 46. OUTPUT VOLTAGE vs R_{LOAD}

Die Characteristics

DIE DIMENSIONS:

71 mils x 100 mils x 19 mils

TRANSISTOR COUNT:

84

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL:

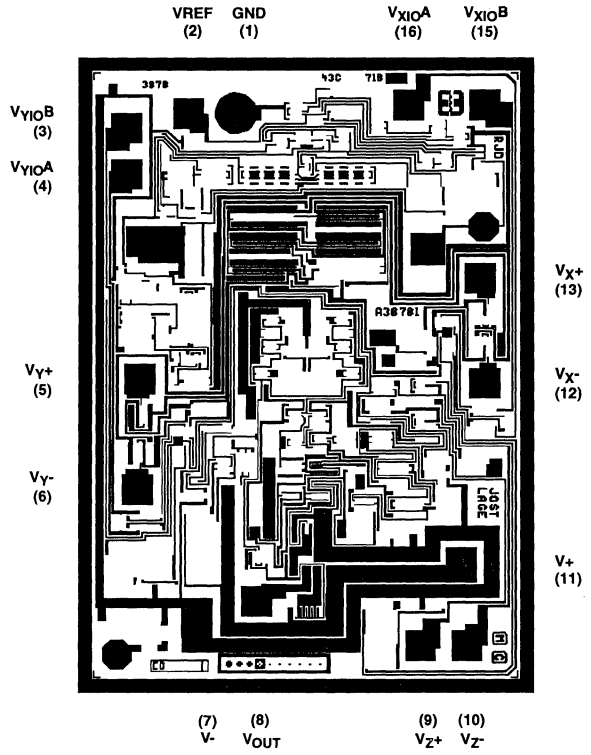
V-

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±2kÅ

Metallization Mask Layout

HA-2556



HARRIS SEMICONDUCTOR

Complete data sheet available via web, Harris' home page: http://www.semi.harris.com/ or via Harris AnswerFAX, see Section 12

HA-2557

130MHz, Four Quadrant, Current Output Analog Multiplier

November 1996

Features

- Low Multiplication Error 1.5%
- Input Bias Currents 8μA
- Y Input Feedthrough at 5MHz . . . . . -50dB
- Wide Y Channel Bandwidth 130MHz
- Wide X Channel Bandwidth 75MHz

Applications

- Military Avionics
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3-2557-9	-40 to 85	16 Ld PDIP	E16.3
HA9P2557-9	-40 to 85	16 Ld SOIC	M16.3

Description

The HA-2557 is a monolithic, high speed, four quadrant, analog multiplier constructed in Harris' Dielectrically Isolated High Frequency Process. The single-ended current output of the HA-2557 has a 130MHz signal bandwidth (R_L = 50Ω). High bandwidth and low distortion make this part an ideal component in video systems.

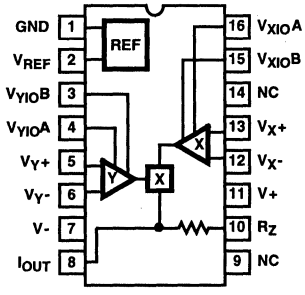
The suitability for precision video applications is demonstrated further by low multiplication error (1.5%), low feedthrough (-50dB), and differential inputs with low bias currents (8μA). The HA-2557 is also well suited for mixer circuits as well as AGC applications for sonar, radar, and medical imaging equipment.

The current output of the HA-2557 allows it to achieve higher bandwidths than voltage output multipliers. Full scale output current is trimmed to 1.6mA. An internal 2500Ω feedback resistor is also provided to accurately convert the current, if desired, to a full scale output voltage of ±4V. The HA-2557 is not limited to multiplication applications only; frequency doubling and power detection are also possible.

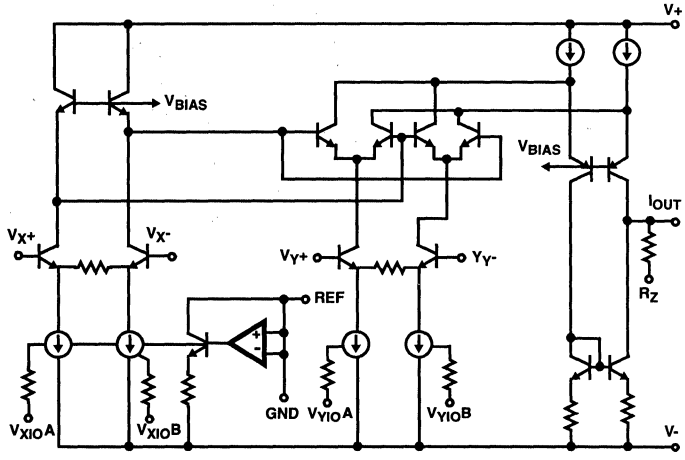
For MIL-STD-883 compliant product consult the HA-2557/883 datasheet.

Pinout

HA-2557
(PDIP, SOIC)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number **2478.5**

HA7210, HA7211

November 1996

10kHz to 10MHz, Low Power Crystal Oscillator

Features

- Single Supply Operation at 32kHz . . . . . 2V to 7V
- Operating Frequency Range. . . . . 10kHz to 10MHz
- Supply Current at 32kHz 5µA
- Supply Current at 1MHz 130µA
- Drives 2 CMOS Loads
- Only Requires an External Crystal for Operation
- Two Pinouts Available

Applications

- Battery Powered Circuits
- Remote Metering
- Embedded Microprocessors
- Palm Top/Notebook PC
- Related Literature
  - AN9334, Improving HA7210 Start-Up Time

Description

The HA7210 and HA7211 are very low power crystal-controlled oscillators that can be externally programmed to operate between 10kHz and 10MHz. For normal operation it requires only the addition of a crystal. The part exhibits very high stability over a wide operating voltage and temperature range.

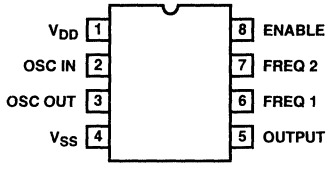
The HA7210 and HA7211 also feature a disable mode that switches the output to a high impedance state. This feature is useful for minimizing power dissipation during standby and when multiple oscillator circuits are employed.

Ordering Information

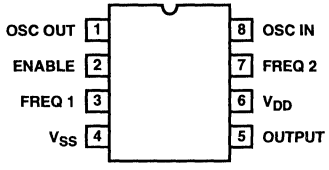
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA7210IP	-40 to 85	8 Ld PDIP	E8.3
HA7210IB (H7210I)	-40 to 85	8 Ld SOIC	M8.15
HA7210Y	-40 to 85	DIE	
HA7211IB (H7211I)	-40 to 85	8 Ld SOIC	M8.15

Pinouts

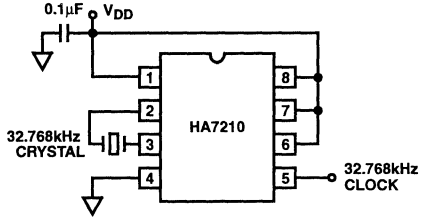
HA7210
(PDIP, SOIC)
TOP VIEW



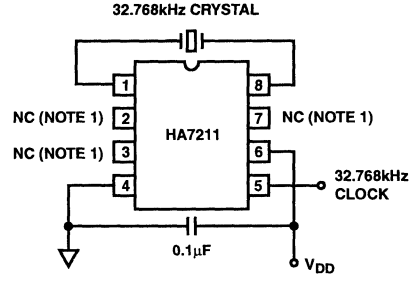
HA7211
(SOIC)
TOP VIEW



Typical Application Circuits



32.768kHz MICROPOWER CLOCK OSCILLATOR



NOTE:

1. Internal pull-up resistors provided for both HA7210 and HA7211.

8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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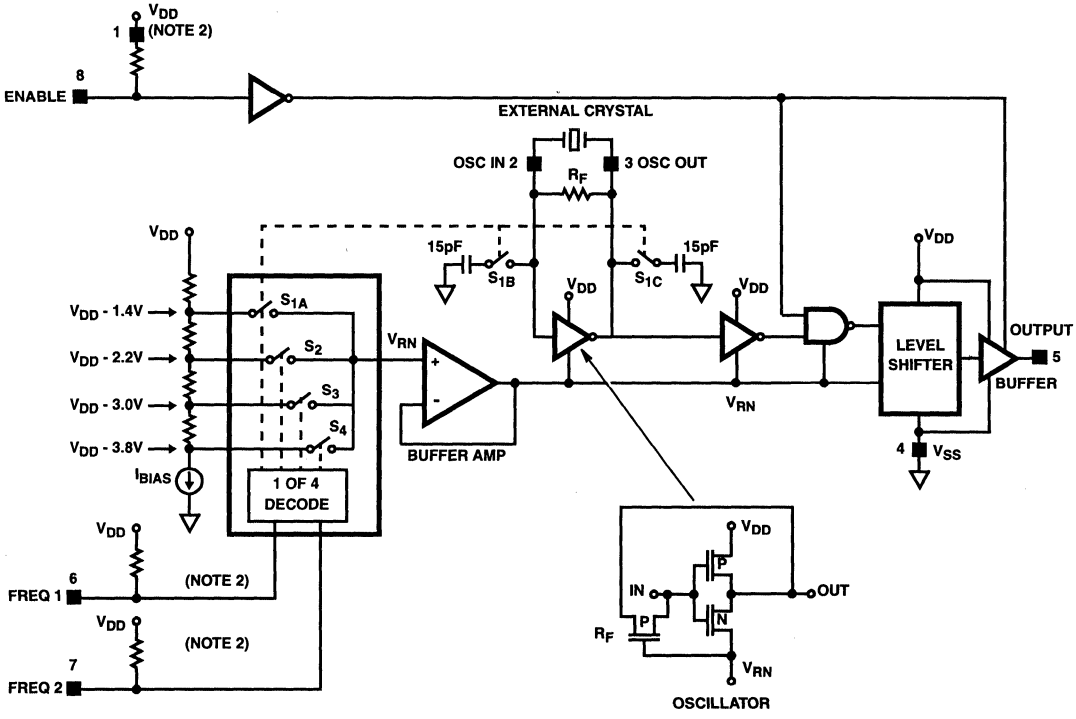
Simplified Block Diagram (HA7210)



FREQUENCY SELECTION TRUTH TABLE

ENABLE	FREQ 1	FREQ 2	SWITCH	OUTPUT RANGE
1	1	1	S_{1A}, S_{1B}, S_{1C}	10kHz - 100kHz
1	1	0	S_2	100kHz - 1MHz
1	0	1	S_3	1MHz - 5MHz
1	0	0	S_4	5MHz - 10MHz+
0	X	X	X	High Impedance

NOTE:

2. Logic input pull-up resistors are constant current source of 0.4µA.

Absolute Maximum Ratings

Supply Voltage 10V
Voltage (any pin) . . . . . V_{SS}-0.3V to V_{DD}+0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . 4000V

Operating Conditions

Temperature Range (Note 3) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
PDIP Package	125
SOIC Package	170

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. This product is production tested at 25°C only.
4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SS} = GND, T_A = 25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	V_{DD} = 5V			V_{DD} = 3V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{DD} Supply Range	f_{OSC} = 32kHz	2	5	7	-	-	-	V
I_{DD} Supply Current	f_{OSC} = 32kHz, EN = 0 (Standby)	-	5.0	9.0	-	-	-	µA
	f_{OSC} = 32kHz, C_L = 10pF (Note 5), EN = 1, Freq1 = 1, Freq2 = 1	-	5.2	10.2	-	3.6	6.1	µA
	f_{OSC} = 32kHz, C_L = 40pF, EN = 1, Freq1 = 1, Freq2 = 1	-	10	15	-	6.5	9	µA
	f_{OSC} = 1MHz, C_L = 10pF (Note 5), EN = 1, Freq1 = 0, Freq2 = 1	-	130	200	-	90	180	µA
	f_{OSC} = 1MHz, C_L = 40pF, EN = 1, Freq1 = 0, Freq2 = 1	-	270	350	-	180	270	µA
V_{OH} Output High Voltage	I_{OUT} = -1mA	4.0	4.9	-	-	2.8	-	V
V_{OL} Output Low Voltage	I_{OUT} = 1mA	-	0.07	0.4	-	0.1	-	V
I_{OH} Output High Current	$V_{OUT} \geq$ 4V	-	-10	-5	-	-	-	mA
I_{OL} Output Low Current	$V_{OUT} \leq$ 0.4V	5.0	10.0	-	-	-	-	mA
Three-State Leakage Current	V_{OUT} = 0V, 5V, T_A = 25°C, -40°C	-	0.1	-	-	-	-	nA
	V_{OUT} = 0V, 5V, T_A = 85°C	-	10	-	-	-	-	nA
I_{IN} Enable, Freq1, Freq2 Input Current	V_{IN} = V_{SS} to V_{DD}	-	0.4	1.0	-	-	-	µA
V_{IH} Input High Voltage Enable, Freq1, Freq2		2.0	-	-	-	-	-	V
V_{IL} Input Low Voltage Enable, Freq1, Freq2		-	-	0.8	-	-	-	V
Enable Time	C_L = 18pF, R_L = 1kΩ	-	800	-	-	-	-	ns
Disable Time	C_L = 18pF, R_L = 1kΩ	-	90	-	-	-	-	ns
t_R Output Rise Time	10% - 90%, f_{OSC} = 32kHz, C_L = 40pF	-	12	25	-	12	-	ns
t_F Output Fall Time	10% - 90%, f_{OSC} = 32kHz, C_L = 40pF	-	12	25	-	14	-	ns
Duty Cycle, Packaged Part Only (Note 6)	C_L = 40pF, f_{OSC} = 1MHz	40	54	60	-	-	-	%
Duty Cycle, (See Typical Curves)	C_L = 40pF, f_{OSC} = 32kHz	-	41	-	-	44	-	%
Frequency Stability vs Supply Voltage	f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF	-	1	-	-	-	-	ppm/V
Frequency Stability vs Temperature	f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF	-	0.1	-	-	-	-	ppm/°C
Frequency Stability vs Load	f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF	-	0.01	-	-	-	-	ppm/pF

NOTES:

5. Calculated using the equation $I_{DD} = I_{DD}$ (No Load) + (V_{DD}) (f_{OSC})(C_L)
6. Duty cycle will vary with supply voltage, oscillation frequency, and parasitic capacitance on the crystal pins.

Test Circuit

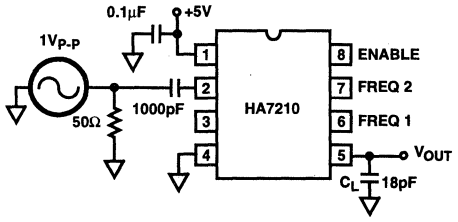


FIGURE 1.

In production the HA7210 is tested with a 32kHz and a 1MHz crystal. However for characterization purposes data was taken using a sinewave generator as the frequency determining element, as shown in Figure 1. The $1V_{P-P}$ input is a smaller amplitude than what a typical crystal would generate so the transitions are slower. In general the Generator data will show a "worst case" number for I_{DD}, duty cycle, and rise/fall time. The Generator test method is useful for testing a variety of frequencies quickly and provides curves which can be used for understanding performance trends. Data for the HA7210 using crystals has also been taken. This data has been overlaid onto the generator data to provide a reference for comparison.

Application Information

Theory Of Operation

The HA7210 and HA7211 are Pierce Oscillators optimized for low power consumption, requiring no external components except for a bypass capacitor and a Parallel Mode Crystal. The Simplified Block Diagram shows the Crystal attached to pins 2 and 3, (HA7210) the Oscillator input and output. The crystal drive circuitry is detailed showing the simple CMOS inverter stage and the P-channel device being used as biasing resistor R_F. The inverter will operate mostly in its linear region increasing the amplitude of the oscillation until limited by its transconductance and voltage rails, V_{DD} and V_{RN}. The inverter is self biasing using R_F to center the oscillating waveform at the input threshold. Do not interfere with this bias function with external loads or excessive leakage on pin 2 for HA7210, pin 8 for HA7211. Nominal value for R_F is 17MΩ in the lowest frequency range to 7MΩ in the highest frequency range.

The HA7210 and HA7211 optimizes its power for 4 frequency ranges selected by digital inputs Freq1 and Freq2 as shown in the Block Diagram. Internal pull up resistors (constant current 0.4µA) on Enable, Freq1 and Freq2 allow the user simply to leave one or all digital inputs not connected for a corresponding "1" state. All digital inputs may be left open for 10kHz to 100kHz operation.

A current source develops 4 selectable reference voltages through series resistors. The selected voltage, V_{RN}, is buffered and used as the negative supply rail for the oscillator section of the circuit. The use of a current source in the reference string allows for wide supply variation with minimal effect on performance. The reduced operating voltage of the oscillator section reduces power consumption and limits transconductance and bandwidth to the frequency range selected. For frequencies at the edge of a range, the higher range may provide better performance.

The OSC OUT waveform on pin 3 for HA7210 (pin 1 for HA7211) is squared up through a series of inverters to the output drive stage. The Enable function is implemented with a NAND gate in the inverter string, gating the signal to the level shifter and output stage. Also during Disable the output is set to a high impedance state useful for minimizing power during standby and when multiple oscillators are OR'ed to a single node.

Design Considerations

The low power CMOS transistors are designed to consume power mostly during transitions. Keeping these transitions short requires a good decoupling capacitor as close as possible to the supply pins 1 and 4 for HA7210, pins 4 and 6 for HA7211. A ceramic 0.1µF is recommended. Additional supply decoupling on the circuit board with 1µF to 10µF will further reduce overshoot, ringing and power consumption. The HA7210, when compared to a crystal and inverter alone, will speed clock transition times, reducing power consumption of all CMOS circuitry run from that clock.

Power consumption may be further reduced by minimizing the capacitance on moving nodes. The majority of the power will be used in the output stage driving the load. Minimizing the load and parasitic capacitance on the output, pin 5, will play the major role in minimizing supply current. A secondary source of wasted supply current is parasitic or crystal load capacitance on pins 2 and 3 for HA7210, pins 1 and 8 for HA7211. The HA7210 is designed to work with most available crystals in its frequency range with no external components required. Two 15pF capacitors are internally switched onto crystal pins 2 and 3 on the HA7210 to compensate the oscillator in the 10kHz to 100kHz frequency range.

The supply current of the HA7210 and HA7211 may be approximately calculated from the equation:

$$I_{DD} = I_{DD}(\text{Disabled}) + V_{DD} \times f_{OSC} \times C_L$$

where: I_{DD} = Total supply current
V_{DD} = Total voltage from V_{DD} (pin1) to V_{SS} (pin4)
f_{OSC} = Frequency of Oscillation
C_L = Output (pin5) load capacitance

Example #1:

V_{DD} = 5V, f_{OSC} = 100kHz, C_L = 30pF
I_{DD}(Disabled) = 4.5µA (Figure 10)
I_{DD} = 4.5µA + (5V)(100kHz)(30pF) = 19.5µA
Measured I_{DD} = 20.3µA

Example #2:

V_{DD} = 5V, f_{OSC} = 5MHz, C_L = 30pF
I_{DD}(Disabled) = 75µA (Figure 9)
I_{DD} = 75µA + (5V)(5MHz)(30pF) = 825µA
Measured I_{DD} = 809µA

Crystal Selection

For general purpose applications, a Parallel Mode Crystal is a good choice for use with the HA7210 or HA7211. However for applications where a precision frequency is required, the designer needs to consider other factors.

Crystals are available in two types or modes of oscillation, Series and Parallel. Series Mode crystals are manufactured to operate at a specified frequency with zero load capacitance and appear as a near resistive impedance when oscillating. Parallel Mode crystals are manufactured to operate with a specific capacitive load in series, causing the crystal to operate at a more inductive impedance to cancel the load capacitor. Loading a crystal with a different capacitance will "pull" the frequency off its value.

The HA7210 and HA7211 has 4 operating frequency ranges. The higher three ranges do not add any loading capacitance to the oscillator circuit. The lowest range, 10kHz to 100kHz, automatically switches in two 15pF capacitors onto OSC IN and OSC OUT to eliminate potential start-up problems. These capacitors create an effective crystal loading capacitor equal to the series combination of these two capacitors. For the HA7210 and HA7211, in the lowest range, the effective loading capacitance is 7.5pF. Therefore the choice for a crystal, in this range, should be a Parallel Mode crystal that requires a 7.5pF load.

In the higher 3 frequency ranges, the capacitance on OSC IN and OSC OUT will be determined by package and layout parasitics, typically 4 to 5pF. Ideally the choice for crystal should be a Parallel Mode set for 2.5pF load. A crystal manufactured for a different load will be "pulled" from its nominal frequency (see Crystal Pullability).

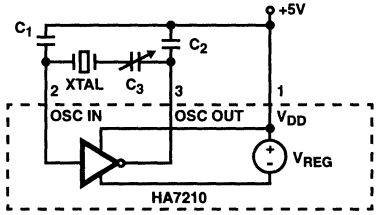


FIGURE 2.

Frequency Fine Tuning

Two Methods will be discussed for fine adjustment of the crystal frequency. The first and preferred method (Figure 2), provides better frequency accuracy and oscillator stability than method two (Figure 3). Method one also eliminates start-up problems sometimes encountered with 32kHz tuning fork crystals.

For best oscillator performance, two conditions must be met: the capacitive load must be matched to both the inverter and crystal to provide ideal conditions for oscillation, and the frequency of the oscillator must be adjustable to the desired frequency. In Method two these two goals can be at odds with each other; either the oscillator is trimmed to frequency by de-tuning the load circuit, or stability is increased at the expense of absolute frequency accuracy.

Method one allows these two conditions to be met independently. The two fixed capacitors, C_1 and C_2, provide the optimum load to the oscillator and crystal. C_3 adjusts the frequency at which the circuit oscillates without appreciably changing the load (and thus the stability) of the system. Once a value for C_3 has been determined for the particular type of crystal being used, it could be replaced with a fixed capacitor. For the most precise control over oscillator frequency, C_3 should remain adjustable.

This three capacitor tuning method will be more accurate and stable than method two and is recommended for 32kHz tuning fork crystals; without it they may leap into an overtone mode when power is initially applied.

Method two has been used for many years and may be preferred in applications where cost or space is critical. Note that in both cases the crystal loading capacitors are connected between the oscillator and V_{DD}; do not use V_{SS} as an AC ground. The Simplified Block Diagram shows that the oscillating inverter does not directly connect to V_{SS} but is referenced to V_{DD} and V_{RN}. Therefore V_{DD} is the best AC ground available.

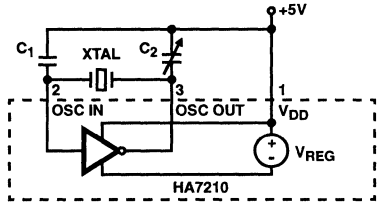


FIGURE 3.

Typical values of the capacitors in Figure 2 are shown below. Some trial and error may be required before the best combination is determined. The values listed are total capacitance including parasitic or other sources. Remember that in the 10kHz to 100kHz frequency range setting the HA7210 switches in two internal 15pF capacitors.

CRYSTAL FREQUENCY	LOAD CAPS C_1, C_2	TRIMMER CAP C_3
32kHz	33pF	5pF to 50pF
1MHz	33pF	5pF to 50pF
2MHz	25pF	5pF to 50pF
4MHz	22pF	5pF to 100pF

CRYSTAL PULLABILITY

Figure 4 shows the basic equivalent circuit for a crystal and its loading circuit.

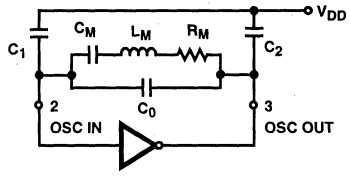


FIGURE 4.

Where: C_M = Motional Capacitance
L_M = Motional Inductance
R_M = Motional Resistance
C_0 = Shunt Capacitance

$$C_{CL} = \frac{1}{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)} = \text{Equivalent Crystal Load}$$

If loading capacitance is connected to a Series Mode Crystal, the new Parallel Mode frequency of resonance may be calculated with the following equation:

$$f_P = f_S\left[1 + \frac{C_M}{2(C_0 + C_{CL})}\right]$$

Where: f_P = Parallel Mode Resonant Frequency
f_S = Series Mode Resonant Frequency

In a similar way, the Series Mode resonant frequency may be calculated from a Parallel Mode crystal and then you may calculate how much the frequency will "pull" with a new load.

Layout Considerations

Due to the extremely low current (and therefore high impedance) the circuit board layout of the HA7210 or HA7211 must be given special attention. Stray capacitance should be minimized. Keep the oscillator traces on a single layer of the PCB. Avoid putting a ground plane above or below this layer. The traces between the crystal, the capacitors, and the OSC pins should be as short as possible. Completely surround the oscillator components with a thick trace of V_{DD} to minimize coupling with any digital signals. The final assembly must be free from contaminants such as solder flux, moisture, or any other potential source of leakage. A good solder mask will help keep the traces free of moisture and contamination over time.

Further Reading

Al Little "HA7210 Low Power Oscillator: Micropower Clock Oscillator and Op Amps Provide System Shutdown for Battery Circuits". Harris Semiconductor Application Note AN9317.

Robert Rood "Improving Start-Up Time at 32KHz for the HA7210 Low Power Crystal Oscillator". Harris Semiconductor Application Note AN9334.

S. S. Eaton "Timekeeping Advances Through COS/MOS Technology". Harris Semiconductor Application Note ICAN-6086.

E. A. Vittoz, et. al. "High-Performance Crystal Oscillator circuits: Theory and Application". IEEE Journal of Solid-State Circuits, Vol. 23, No3, June 1988, pp774-783.

M. A. Unkrich, et. al. "Conditions for Start-Up in Crystal Oscillators". IEEE Journal of Solid-State Circuits, Vol. 17, No1, Feb. 1982, pp87-90.

Marvin E. Frerking "Crystal Oscillator Design and Temperature Compensation". New York: Van Nostrand-Reinhold, 1978. Pierce Oscillators Discussed pp56-75.

Typical Performance Curves

C_L = 40pF, f_{OSC} = 5MHz, V_{DD} = 5V, V_{SS} = GND

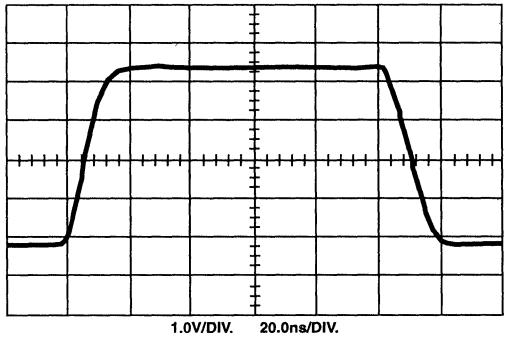


FIGURE 5. OUTPUT WAVEFORM (C_L = 40pF)

C_L = 18pF, f_{OSC} = 5MHz, V_{DD} = 5V, V_{SS} = GND

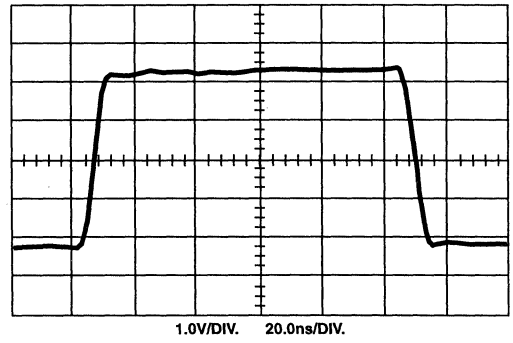


FIGURE 6. OUTPUT WAVEFORM (C_L = 18pF)

NOTE: Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

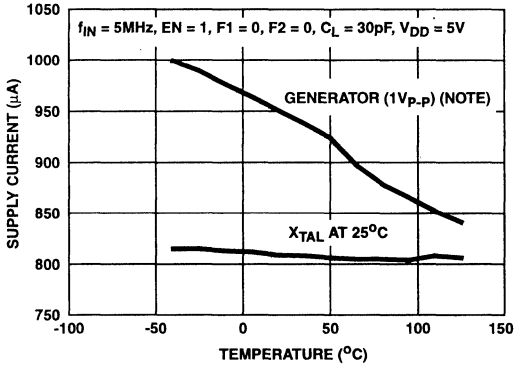


FIGURE 7. SUPPLY CURRENT vs TEMPERATURE

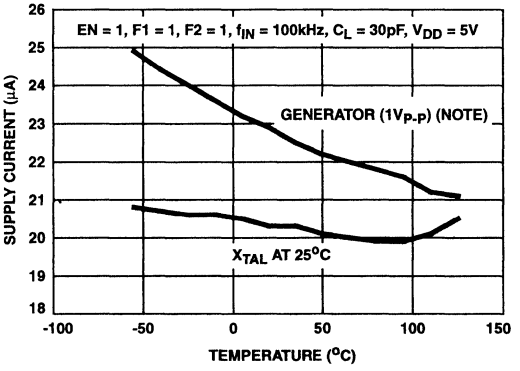


FIGURE 8. SUPPLY CURRENT vs TEMPERATURE

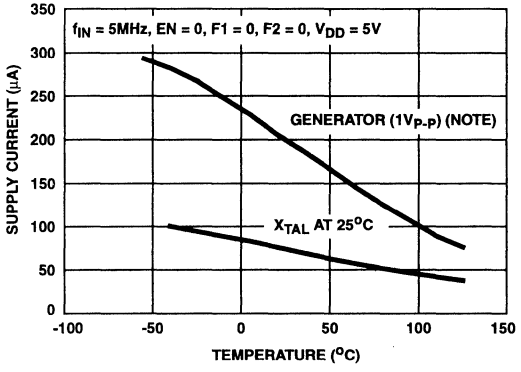


FIGURE 9. DISABLE SUPPLY CURRENT vs TEMPERATURE

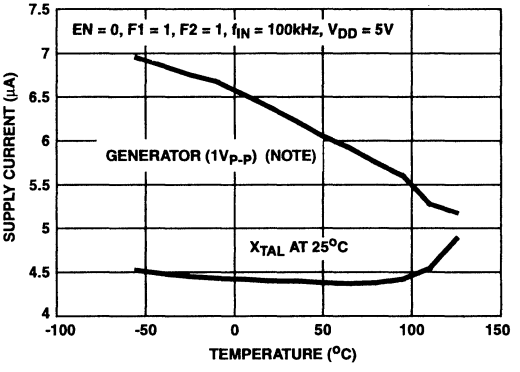


FIGURE 10. DISABLE SUPPLY CURRENT vs TEMPERATURE

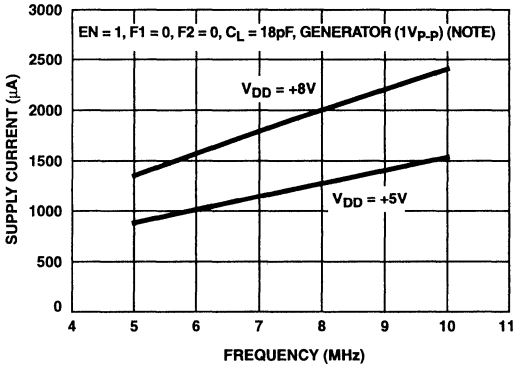


FIGURE 11. SUPPLY CURRENT vs FREQUENCY

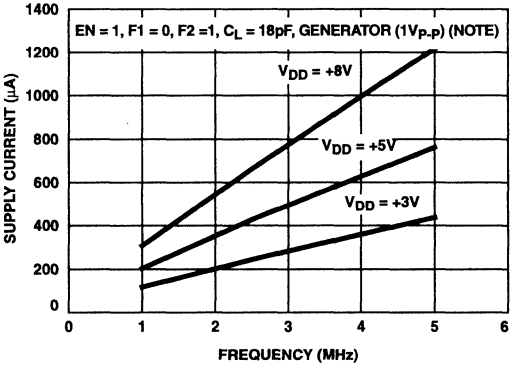


FIGURE 12. SUPPLY CURRENT vs FREQUENCY

NOTE: Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

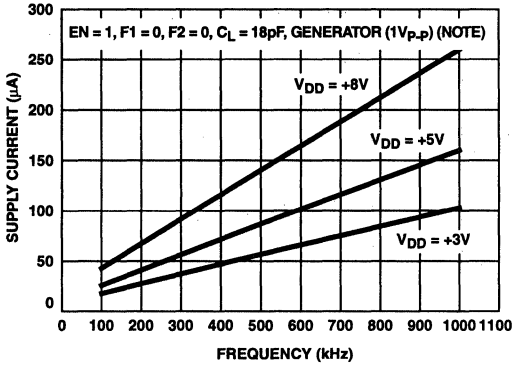


FIGURE 13. SUPPLY CURRENT vs FREQUENCY

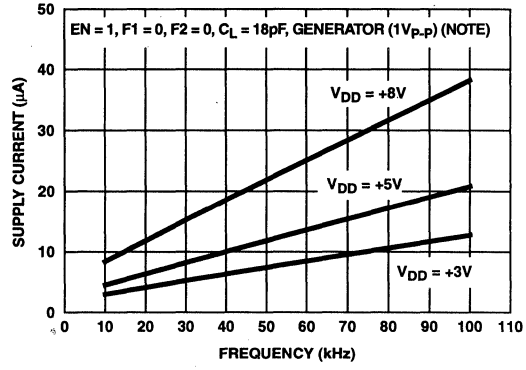


FIGURE 14. SUPPLY CURRENT vs FREQUENCY

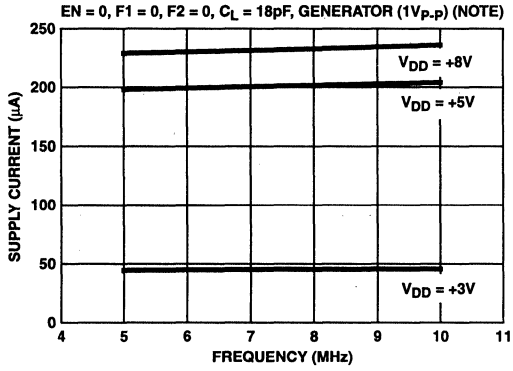


FIGURE 15. DISABLED SUPPLY CURRENT vs FREQUENCY

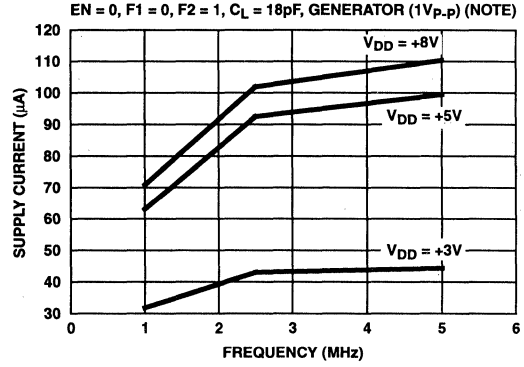


FIGURE 16. DISABLE SUPPLY CURRENT vs FREQUENCY

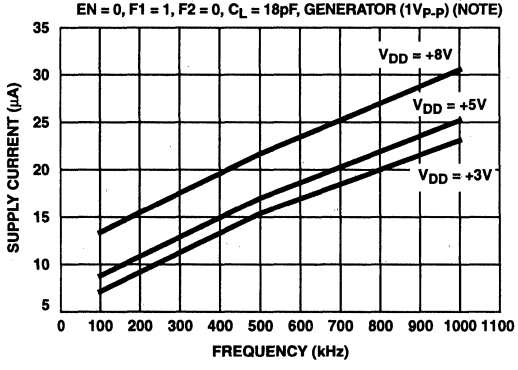


FIGURE 17. DISABLE SUPPLY CURRENT vs FREQUENCY

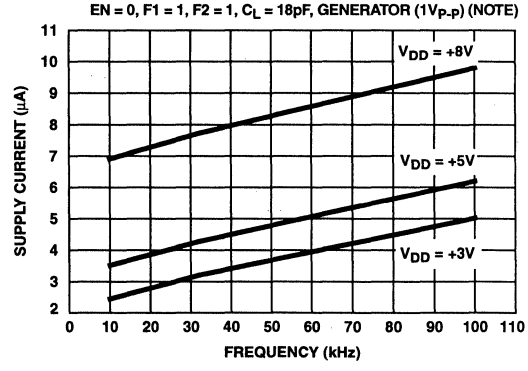


FIGURE 18. DISABLE SUPPLY CURRENT vs FREQUENCY

NOTE: Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

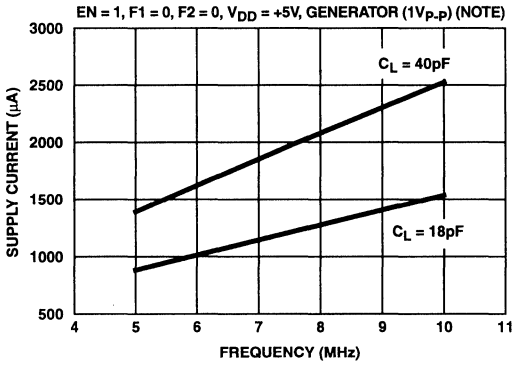


FIGURE 19. SUPPLY CURRENT vs FREQUENCY

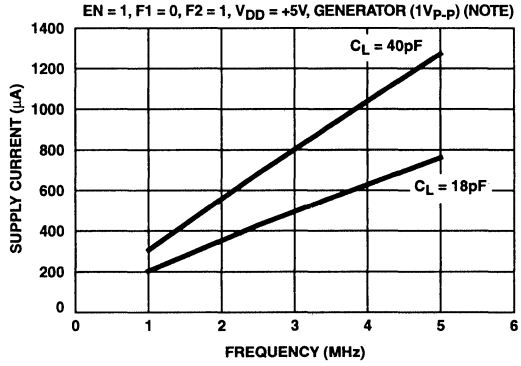


FIGURE 20. SUPPLY CURRENT vs FREQUENCY

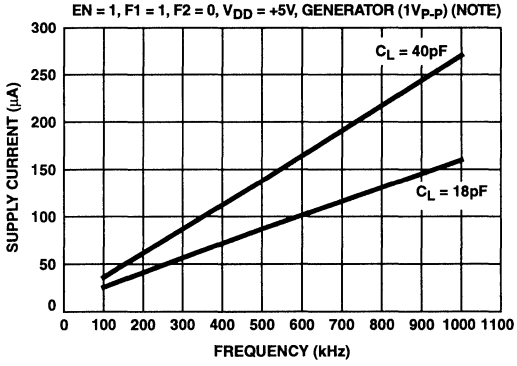


FIGURE 21. SUPPLY CURRENT vs FREQUENCY

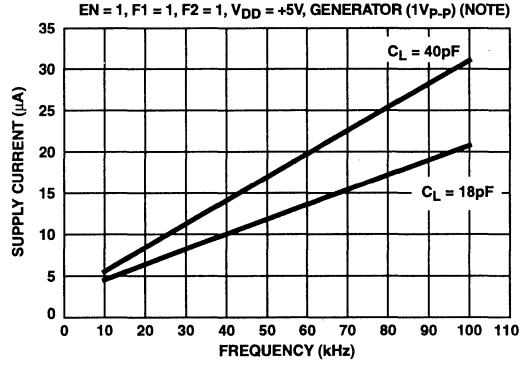


FIGURE 22. SUPPLY CURRENT vs FREQUENCY

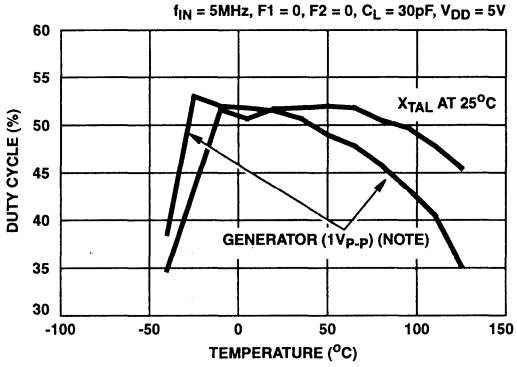


FIGURE 23. DUTY CYCLE vs TEMPERATURE

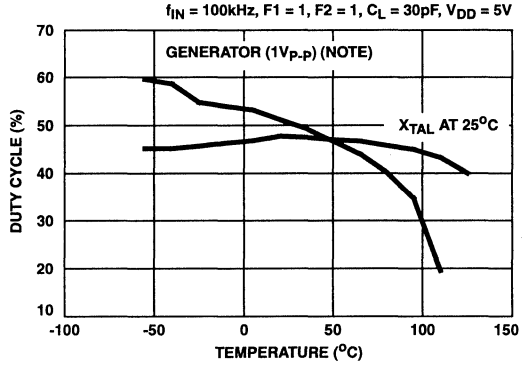


FIGURE 24. DUTY CYCLE vs TEMPERATURE

NOTE: Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

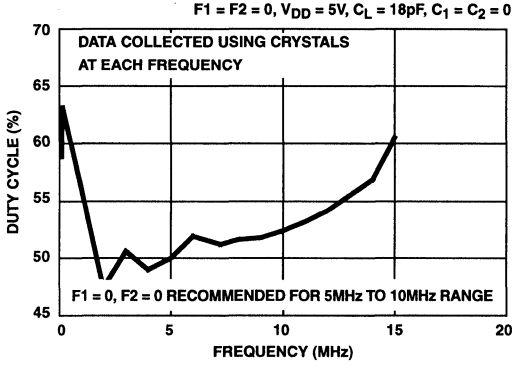


FIGURE 25. DUTY CYCLE vs FREQUENCY

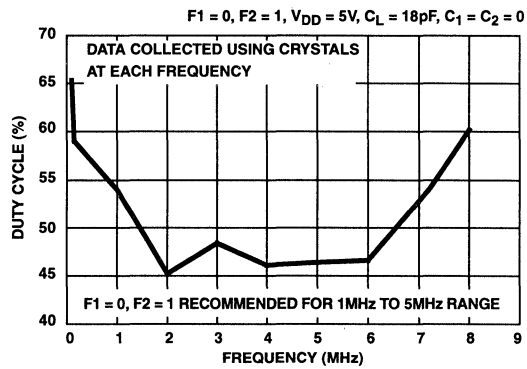


FIGURE 26. DUTY CYCLE vs FREQUENCY

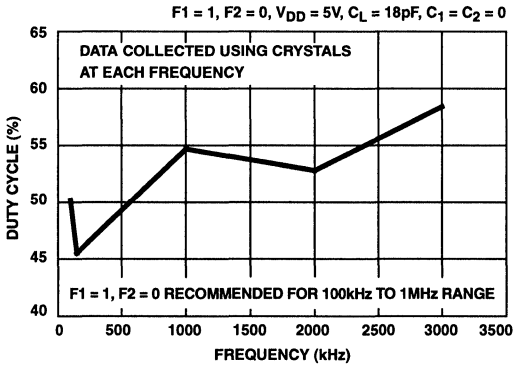


FIGURE 27. DUTY CYCLE vs FREQUENCY

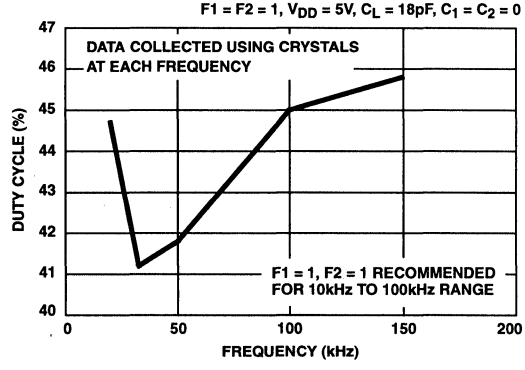


FIGURE 28. DUTY CYCLE vs FREQUENCY

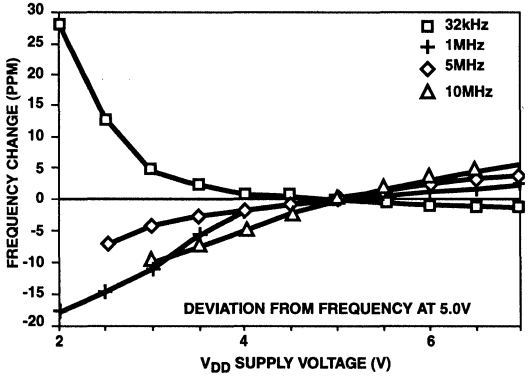


FIGURE 29. FREQUENCY CHANGE vs V_{DD}

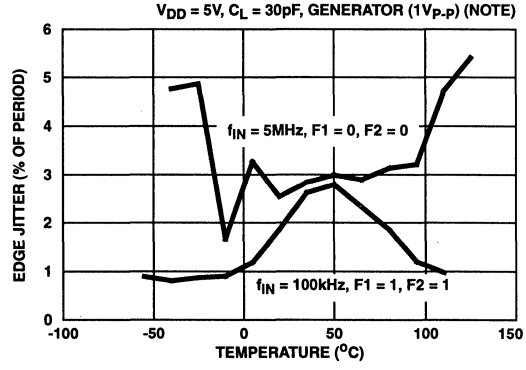


FIGURE 30. EDGE JITTER vs TEMPERATURE

NOTE: Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

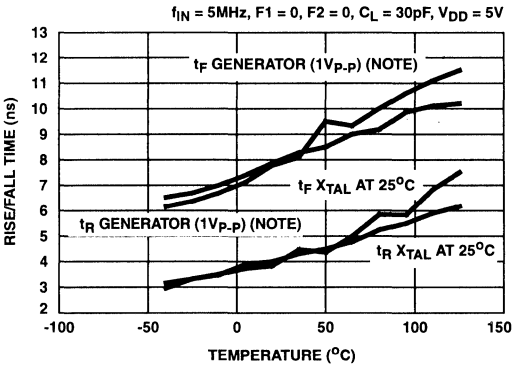


FIGURE 31. RISE/FALL TIME vs TEMPERATURE

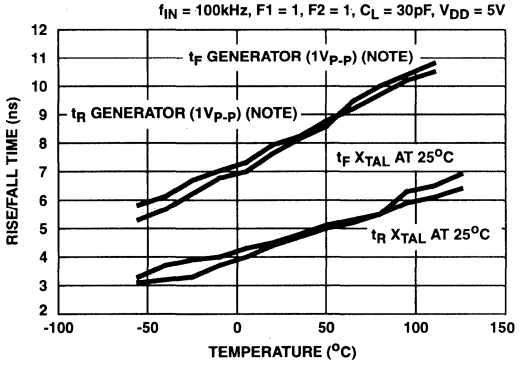


FIGURE 32. RISE/FALL TIME vs TEMPERATURE

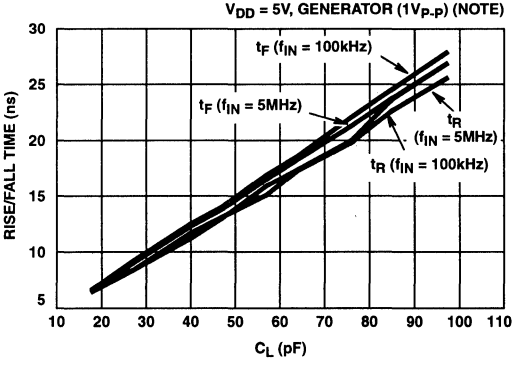


FIGURE 33. RISE/FALL TIME vs C_L

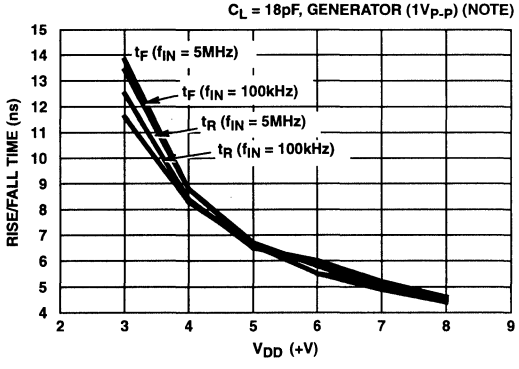


FIGURE 34. RISE/FALL TIME vs V_{DD}

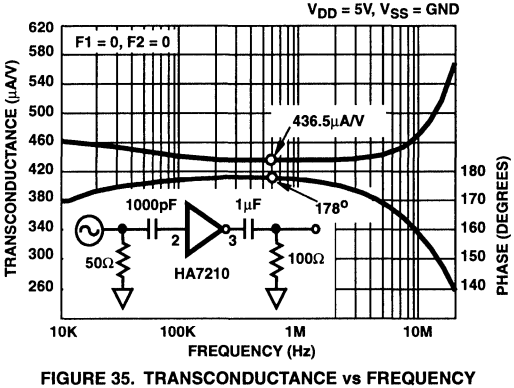


FIGURE 35. TRANSCONDUCTANCE vs FREQUENCY

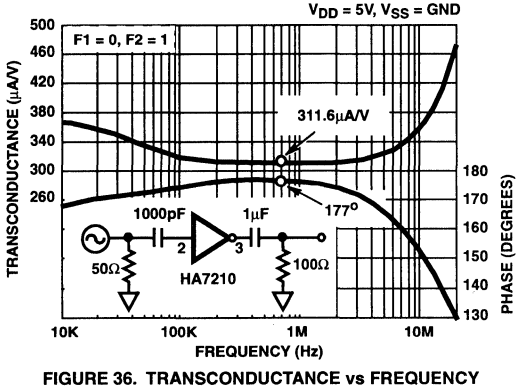


FIGURE 36. TRANSCONDUCTANCE vs FREQUENCY

NOTE: Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

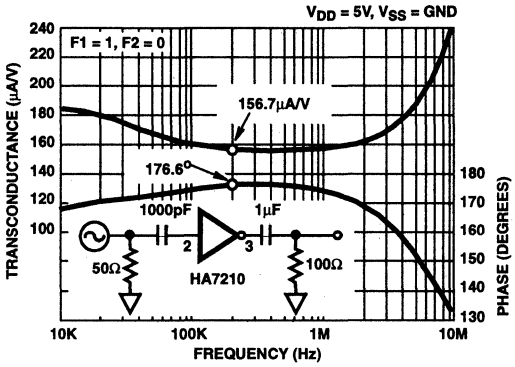


FIGURE 37. TRANSCONDUCTANCE vs FREQUENCY

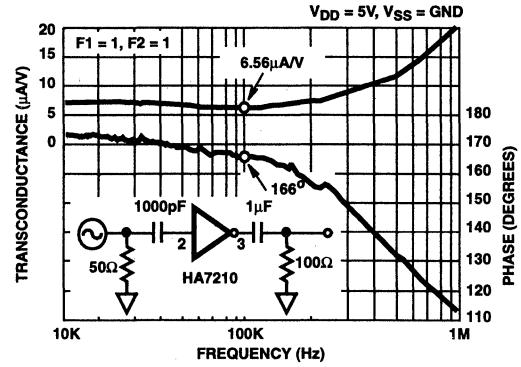
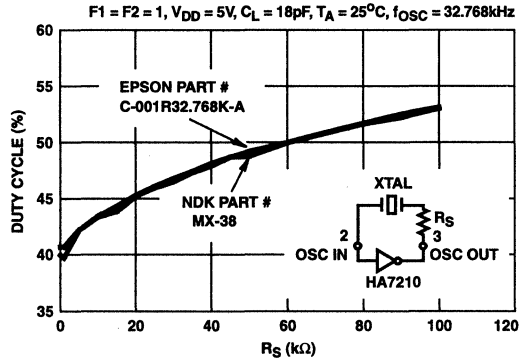


FIGURE 38. TRANSCONDUCTANCE vs FREQUENCY



NOTE: Figure 39 (Duty Cycle vs R_S at 32kHz) should only be used for 32kHz crystals. R_S may be used at other frequencies to adjust Duty Cycle but experimentation will be required to find an appropriate value. The R_S value will be proportional to the effective series resistance of the crystal being used.

FIGURE 39. DUTY CYCLE vs R_S at 32kHz

NOTE: Refer to Test Circuit (Figure 1).

Die Characteristics

DIE DIMENSIONS:

68 mils x 64 mils x 14 mils

SUBSTRATE POTENTIAL

V_{SS}

METALLIZATION:

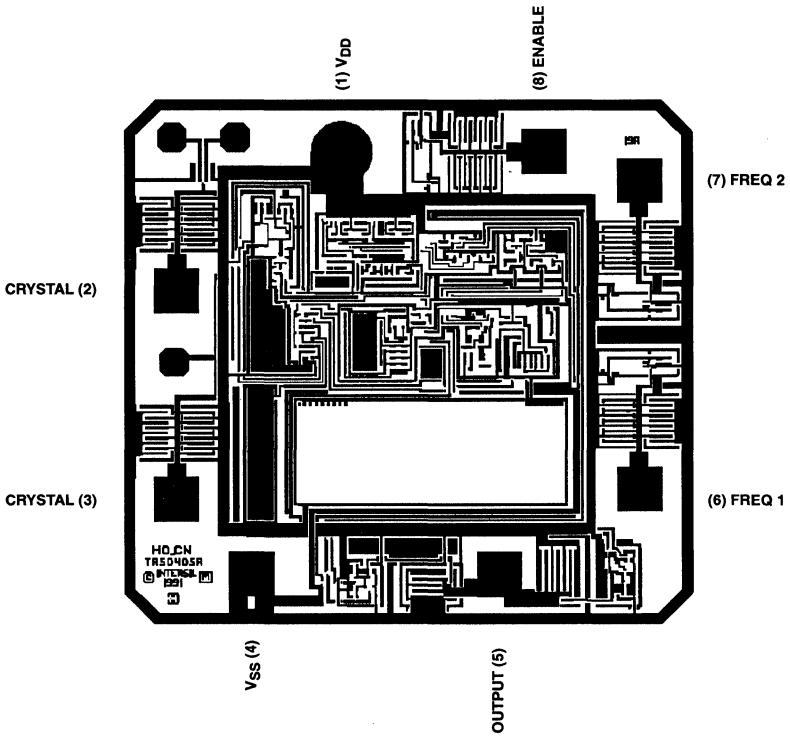
Type: Si - Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) Over Silox (SiO_2, 3% Phos)
Silox Thickness: 7kÅ ±1kÅ
Nitride Thickness: 8kÅ ±1kÅ

Metallization Mask Layout

HA7210



HARRIS SEMICONDUCTOR

NOT RECOMMENDED FOR NEW DESIGNS
A complete data sheet is available via web,
Harris' home page: http://www.semi.harris.com/
or via Harris AnswerFAX, see Section 12

HFA5250

500MHz, Ultra High Speed Monolithic Pin Driver

November 1996

Features

- High Digital Data Rate 500MHz
- Very Fast Slew Rate 2500V/µs
- Very Fast Rise/Fall Times 600ps
- Wide Output Range . . . . . +7V to -2V
- Precise 50Ω Output Impedance
- High Impedance, Three-State Output Control

Applications

- IC Tester Pin Electronics
- Pattern Generators
- Pulse Generators
- Built-In Test Equipment (BITE)
- Level Comparator/Translator

Description

The HFA5250 is the ideal monolithic pin driver solution for high performance test systems. The device will switch at high data rates between two input voltage levels providing variable amplitude pulses. The output impedance is trimmed to achieve a precision 50Ω source for impedance matching. Two differential ECL/TTL compatible inputs control the operation of the HFA5250, one controlling the V_{HIGH}/V_{LOW} switching and the other controlling the output's high-impedance state. The HFA5250's 500MHz data rate makes it compatible with today's high speed VLSI test systems and the +7V to -2V output swing allows testing of all common logic families.

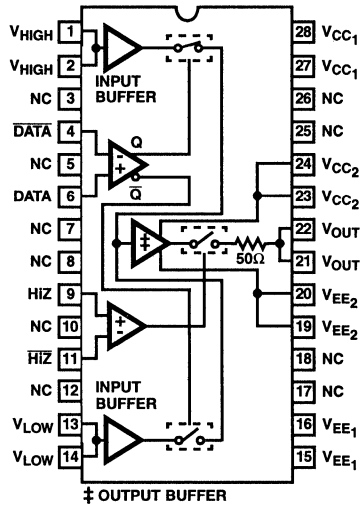
The HFA5250 is manufactured in the Harris proprietary complementary bipolar process.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA5250CB	0 to 50 Without Air Flow	28 Ld SOIC	M28.3
	0 to 70 With 400lfpm Air Flow		

Pinout

HFA5250
(SOIC)
TOP VIEW



NOTE: Switches Shown in the "1" State.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2943.4**

HARRIS SEMICONDUCTOR

HFA5251

November 1996

800MHz Monolithic Pin Driver

Features

- High Digital Data Rate 800MHz
- Very Fast Rise/Fall Times 500ps
- Wide Output Range . . . . . +7V to -2V
- Precise 50Ω Output Impedance
- High Impedance, Three-State Output Control

Applications

- IC Tester Pin Electronics
- Pattern Generators
- Pulse Generators
- Level Comparator/Translator

Description

The HFA5251 is a very high speed monolithic pin driver solution for high performance test systems. The device will switch at high data rates between two input voltage levels providing variable amplitude pulses. The output impedance is trimmed to achieve a precision 50Ω source for impedance matching. Two differential ECL/TTL compatible inputs control the operation of the HFA5251, one controlling the V_{HIGH}/V_{LOW} switching and the other controlling the output's high-impedance state. The HFA5251's 800MHz data rate makes it compatible with today's high-speed VLSI test systems and the +7V to -2V output swing allows testing of all common logic families.

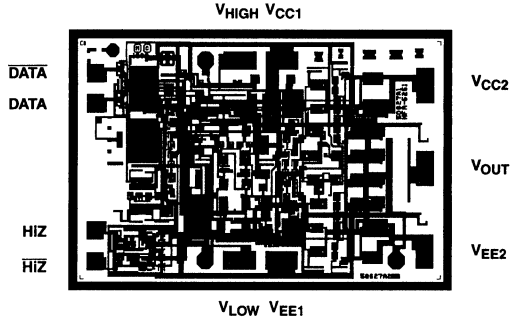
The HFA5251 is manufactured in Harris' proprietary complementary bipolar UHF-1 process. The HFA5251 is offered in die form. Contact your local sales representative for packaging options.

Ordering Information

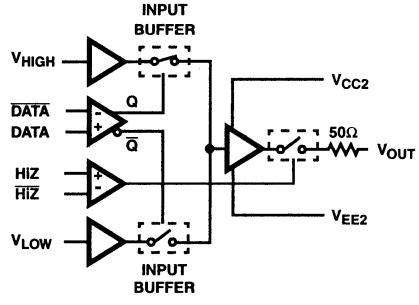
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
HFA5251Y	$T_{JUNCTION}$ < 175	Die Form

Pinout

HFA5251
(DIE FORM)
TOP VIEW



Functional Diagram



TRUTH TABLE FOR V_{OUT}

		DATA	
		0	1
HiZ	0	V_{LOW}	V_{HIGH}
	1	HiZ	HiZ

8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 3689.3

Pin Descriptions

NAME	FUNCTION
V_{CC1}	Positive Supply. Nominal value is 10V ±0.2V. Reducing supply voltage below 9.8V will reduce positive output voltage swing. The total supply voltage from V_{CC1} to V_{EE1} should not exceed 15.6V for normal operation or exceed 17.0V to prevent damage. Harris recommends two wire bonds to this pad to provide the lowest possible impedance. In addition, power supply decoupling chip capacitors of 470pF, 0.1µF and a 10µF tantalum are recommended.
V_{EE1}	Negative Supply. Nominal value is -5.2V ±0.2V. A supply voltage more positive than -5.0V will reduce negative output voltage swing. The total supply voltage from V_{CC1} to V_{EE1} should not exceed 15.6V for normal operation or exceed 17.0V to prevent damage. Harris recommends two wire bonds to this pad to provide the lowest possible impedance. In addition, power supply decoupling chip capacitors of 470pF, 0.1µF and a 10µF tantalum are recommended.
V_{CC2}	Output Stage Positive Supply. Nominal voltage and cautions are the same as for V_{CC1}. Having decoupling chip capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through this pad to the output during transients. Normally V_{CC1} and V_{CC2} are connected together close to the die and share decoupling capacitors. Harris recommends two wire bonds for this pad.
V_{EE2}	Output Stage Negative Supply. Nominal voltage and cautions are the same as for V_{EE1}. Having decoupling chip capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through this pad to the output during transients. Normally V_{EE1} and V_{EE2} are connected together close to the die and share decoupling capacitors. Harris recommends two wire bonds for this pad.
V_{HIGH}	Input Voltage High is used to set the output high level V_{OH}. V_{HIGH} is sensitive to capacitively coupled AC noise. Protection from high frequency noise can be achieved with a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this precaution the pin driver may oscillate due to feedback from the output through the PC board ground.
V_{LOW}	Input Voltage Low is used to set the output low level V_{OL}. V_{LOW} is sensitive to capacitively coupled AC noise. Protection from high frequency noise can be achieved with a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this precaution the pin driver may oscillate due to feedback from the output through the PC board ground.
V_{OUT}	Driver Output. The output impedance has been laser trimmed to match a 50Ω transmission line ±2Ω. Custom output impedance trimming is available (contact sales office for details) to provide the best match possible to your 50Ω system.
$\overline{DATA}$, DATA	Differential Digital Inputs used to switch V_{OUT} to the V_{HIGH} or V_{LOW} level. Harris recommends this input pair be driven by complementary ECL signals to provide optimal switching speeds and timing accuracy. However a large Common Mode and Differential Voltage Range is provided to accommodate a variety of signals including single ended TTL and CMOS. When using single ended signals the other input must be tied to an appropriate threshold.
$\overline{HiZ}$, HiZ	Differential Digital Inputs used to switch V_{OUT} from an Active to a High Impedance State. Harris recommends that this input pair be driven by complementary ECL signals to provide optimal switching speeds and timing accuracy. However a large Common Mode and Differential Voltage Range is provided to accommodate a variety of signals including single ended TTL and CMOS. When using single ended signals the other input must be tied to an appropriate threshold.

Absolute Maximum Ratings

Supply Voltage 17V
Differential Input Voltage (DATA and HiZ) 5V
Output Current Continuous (Note 1) 160mA
Input Voltage (Any pin except as specified) . . . . . V_{CC} to V_{EE}
V_{OUT} Voltage . . . . . 8V to -5.5V
V_{HIGH} Voltage . . . . . V_{CC} to -3V
V_{LOW} Voltage . . . . . 8V to V_{EE}
V_{HIGH} to V_{LOW} Voltage . . . . . $V_{HIGH} > V_{LOW}$

Thermal Information

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{CC} = +10V, V_{EE} = -5.2V, V_{IH} = -0.9V, V_{IL} = -1.75V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS (V_{HIGH}, V_{LOW})						
V_{HIGH} Input Offset Voltage	V_{OUT} = 0V	25	-150	-50	+50	mV
V_{LOW} Input Offset Voltage	V_{OUT} = 0V	25	-150	-50	+50	mV
V_{HIGH} Input Bias Current	V_{HIGH} = -2.25V to +7.5V	25	-50	110	300	µA
V_{LOW} Input Bias Current	V_{LOW} = -2.5V to +7.25V	25	-300	-110	50	µA
V_{HIGH} Voltage Range		25	-2.25	-	7.5	V
V_{LOW} Voltage Range		25	-2.5	-	7.25	V
V_{HIGH} to V_{LOW} Differential Voltage Range		25	0.25	-	10	V
V_{HIGH}/V_{LOW} Interaction at 500mV (Note 11)		25	-	2	4	mV
V_{HIGH}/V_{LOW} Interaction at 250mV (Note 11)		25	-	20	40	mV
LOGIC INPUT CHARACTERISTICS (DATA, $\overline{DATA}$, HiZ, $\overline{HiZ}$)						
Logic Input Voltage Range		25	-2	-	7	V
Logic Differential Input Voltage		25	0.4	-	5	V
DATA/$\overline{DATA}$ Logic Input High Current	V_{IH} = 0V, V_{IL} = -2V	25	-50	110	300	µA
DATA/$\overline{DATA}$ Logic Input Low Current	V_{IH} = 0V, V_{IL} = -2V	25	-700	-300	50	µA
HiZ/$\overline{HiZ}$ Logic Input High Current	V_{IH} = 0V, V_{IL} = -2V	25	-50	70	200	µA
HiZ/$\overline{HiZ}$ Logic Input Low Current	V_{IH} = 0V, V_{IL} = -2V	25	-300	-80	50	µA
TRANSFER CHARACTERISTICS						
V_{HIGH} Voltage Gain	V_{HIGH} = -1V to 6.5V	25	0.95	-	1	V/V
V_{LOW} Voltage Gain	V_{LOW} = -1.5V to 6V	25	0.95	-	1	V/V
V_{HIGH}/V_{LOW} Linearity Error (Note 7)	Fullscale = 5V	25	-0.5	-	0.5	%
V_{HIGH}/V_{LOW} Linearity Error (Note 8)	Fullscale = 8.5V	25	-0.75	-	0.75	%
V_{HIGH}/V_{LOW} End Point Gain Deviation (Notes 10, 13)	0.5V Steps	25	-2.0	-	2.0	%
V_{HIGH} End Point Gain Error (Notes 10 and 14)	V_{OUT} = 6.7V to 7.0V	25	-20	-	20	mV
V_{HIGH}/V_{LOW} -3dB Bandwidth	200mV_{P-P}	25	-	100	-	MHz

Electrical Specifications V_{CC} = +10V, V_{EE} = -5.2V, V_{IH} = -0.9V, V_{IL} = -1.75V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Z_{LOAD} = 16 inches of RG-58 Terminated with 50Ω)						
Propagation Delay (Notes 2, 17)		25	0.8	-	1.5	ns
Propagation Delay Match (Notes 2, 17)	Rising to Falling Edge	25	-100	-	100	ps
Rising Edge Propagation Delay vs Duty Cycle (Notes 12, 17)		25	-120	-20	80	ps
Falling Edge Propagation Delay vs Duty Cycle (Notes 12, 17)		25	-80	20	120	ps
Active to HiZ Delay (Note 17)		25	1.2	1.7	2.2	ns
HiZ to Active Delay (Note 17)		25	2.1	2.6	3.1	ns
TRANSIENT RESPONSE (Z_{LOAD} = 16 inches of RG-58 Terminated with 5pF)						
Rise/Fall Time (20%-80%)	$1V_{P-P}$	25	-	450	500	ps
Rise/Fall Time (10%-90%)	$3V_{P-P}$	25	-	890	1000	ps
Rise/Fall Time (10%-90%) (Note 6)	$5V_{P-P}$	25	-	1.5	1.7	ns
Rise/Fall Time Match (Note 6)		25	-	50	150	ps
Minimum Pulse Width (Note 16)	$1V_{P-P}$	25	-	1.0	-	ns
Minimum Pulse Width (Note 16)	$3V_{P-P}$	25	-	1.2	-	ns
Minimum Pulse Width (Note 16)	$5V_{P-P}$	25	-	2.0	-	ns
Overshoot/Undershoot/Preshoot	$3V_{P-P}$	25	-	5	-	%
Data Settling Time to 1% (Note 3)		25	-	10	-	ns
OUTPUT CHARACTERISTICS						
Output Voltage Swing (No Load)	V_{CC} = 10V, V_{EE} = -5.2V	25	-2	-	7	V
	At Other Supplies	25	V_{EE} +3.2	-	V_{CC} -3.0	V
DC Output Resistance - Active (Note 18)	-2V to 7V	25	45	47	49	Ω
Output Leakage - HiZ	-2V to 7V	25	-100	±10	100	nA
Output Capacitance - HiZ		25	-	5	-	pF
Output Current - Active		25	70	100	-	mA
POWER SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio (Note 4)	V_{HIGH}	25	-	14	40	mV/V
	V_{LOW}	25	-	14	40	mV/V
Total Supply Current		25	90	94	96	mA
Supply Current (I_{CC1}, I_{EE1})		25	-	74	-	mA
Supply Current (I_{CC2}, I_{EE2})		25	-	20	-	mA
Supply Voltage Range (Note 5)	V_{CC}	25	9.8	10	10.2	V
Supply Voltage Range (Note 5)	V_{EE}	25	-5.4	-5.2	-5.0	V
Supply Voltage Differential	V_{CC} - V_{EE}	25	12	-	15.6	V

Electrical Specifications V_{CC} = +10V, V_{EE} = -5.2V, V_{IH} = -0.9V, V_{IL} = -1.75V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Power Dissipation	No Load At V_{CC} = 10V, V_{EE} = -5.2V	25	-	-	1.46	W

NOTES:

1. Internal Power Dissipation may limit Output Current below 160mA.
2. 3V Step, 50% duty cycle, 200ns period.
3. 3V Step, measured from 50% of input to ±1% of reference value at 50ns.
4. V_{HIGH} = 2.6V, V_{LOW} = 2.3V, V_{CC} = 9V to 10V, V_{EE} = -4.2V to -5.2V
5. Minimum/maximum output swing will vary with supply voltage.
6. 5V Step, 50% duty cycle, 100ns period.
7. For V_{HIGH} = 0V to 5V, For V_{LOW} = 0V to 5V, Fullscale = 5V, 0.1% = 5mV.
8. For V_{HIGH} = -1.5V to 7V, For V_{LOW} = -2.0V to 6.5V, Fullscale = 8.5V, 0.1% = 8.5mV
9. Shorting the output to a voltage outside the specified range may damage the output.
10. V_{CC} = 9.9V, V_{EE} = -5.1V.
11. V_{HIGH} to V_{LOW} Interaction is measured as the change in V_{OUT} (the active channel) due to a change in the inactive channel. V_{HIGH} Interaction at 250mV is measured as the deviation from 1V as V_{LOW} is changed from 0V to 750mV (Referred to V_{OUT}). V_{Low} Interaction at 250mV is measured as the deviation from 0V as V_{HIGH} is changed from 1V to 250mV (Referred to V_{OUT}).
12. 0V to 3V Step, 200ns period, Pulse Width is varied from 5ns to 195ns.
13. End Point Gain Deviation is the percent deviation of Gain calculated in 0.5V steps at the extremes of output voltage range. For example in the V_{HIGH} range 5.7V to 6.7V, Gain is calculated for V_{HIGH} = 5.7V to 6.2V (Note 15) and V_{HIGH} = 6.2V to 6.7V (Note 15) the difference in gain is calculated and converted to a percentage. The voltage ranges tested are: V_{HIGH} = -1.5V to -0.5V (Note 15) and 5.7V to 6.7V (Note 15), V_{LOW} = -2.0V to -1.0V (Note 15) and 5.5V to 6.5V (Note 15).
14. V_{HIGH} End Point Gain Error is the V_{OUT} absolute error from ideal for a V_{HIGH} change from 6.7V to 7.0V (Note 15).
15. Input voltages V_{HIGH} and V_{LOW} are corrected for Offset Voltage and 7.5V Full Scale Gain Error.
16. Minimum Pulse Width is measured 50% to 50% of specified amplitude with pulse peak at 90% of amplitude.
17. Test is performed into a 50Ω load with a 3V step. Measurement is made from the 50% of input to 50% of output.
18. Dynamic Output Resistance will be higher (typical 48.5Ω) than DC Output Resistance.

Application Information

The HFA5251 is a pin driver designed for use in automatic test equipment (ATE) and high speed pulse generators. Pin drivers, especially those with very high-speed performance, have generally been implemented with discrete transistors (sometimes GaAs) on a circuit board or in a hybrid. Recent IC process improvements, specifically Harris' UHF1 process [1], have enabled the manufacturing of this 800MHz silicon monolithic pin driver.

The ultra high speed performance of the HFA5251 is a result of UHF1 process leverages: low parasitic collector-to-substrate capacitance of the bonded wafer, low collector-to-base parasitic capacitance of the self-aligned base/emitter technology and ultra high f_T NPN (8GHz) and PNP (5.5GHz) poly-silicon transistors.

Functional Block Diagram

The HFA5251 functional block diagram is shown in Figure 1.

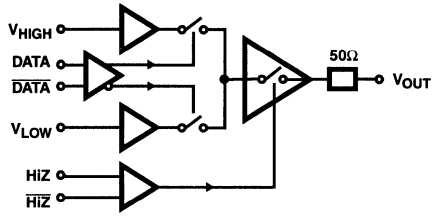


FIGURE 1. BLOCK DIAGRAM

The control inputs, DATA and $\overline{DATA}$, determine the output level. If DATA is at logic "1" and $\overline{DATA}$ is at logic "0", the output level will be the same as V_{HIGH}. If DATA is at logic "0" and $\overline{DATA}$ is at logic "1", the output will be the same as V_{LOW}. The control inputs, HiZ and $\overline{HiZ}$, make the output either active or high-impedance. If HiZ is at logic "1" and $\overline{HiZ}$ is at logic "0", the output will be in high impedance mode. If HiZ is at logic "0" and $\overline{HiZ}$ is at logic "1", the output will be enabled. The output impedance in the enabled mode is trimmed to 50Ω.

Circuit Schematic

The Pin Driver circuit consists of a switch, an output buffer, and two differential control elements as shown in Figure 8.

A two stage approach, separating the switch from the output buffer, allows the speed and accuracy requirements of the switch to be de-coupled from the load driving capability of the buffer.

The patent pending switch circuitry[2] uses cascaded emitter followers as input buffers and also to switch the input V_{HIGH} and V_{LOW} to node VSO. Dual differential pairs controlled by the data timing (DATA and $\overline{DATA}$) direct current to select either the V_{HIGH} or V_{LOW} switch. Matching transistor types and transdiodes improve linearity and lowers the voltage offset and offset drift. Stacking two emitter-base junctions allows the V_{HIGH} to V_{LOW} range to be extended to two BVebo's of the process. The speed of the pin driver is largely determined by the current flowing through the switch stage and the collector-base capacitance of the output stage transistors connected to the node VSO.

The output stage consists of cascaded emitter followers constructed in a typical push-pull manner as shown in Figure 2. However, transdiodes are added to increase the voltage breakdown characteristics of the output during high impedance mode. HiZ and $\overline{HiZ}$ control the mode of the output stage. A trimmed, NiCr resistor is added to provide the 50Ω output impedance.

Overall, a symmetry of device types and paths is constructed to improve slew and delay symmetry. Both the V_{HIGH} to V_{OUT} path and the V_{LOW} to V_{OUT} path contain three NPN and three PNP transistors operating at similar collector currents. Thus the transient response of V_{HIGH} to V_{LOW} and V_{LOW} to V_{HIGH} are kept symmetrical. Also, a trimmable current reference (not shown) allows the AC parameters to be adjusted to maintain unit to unit consistency.

Speed Advantage

Harris Pin Drivers on bonded-wafer technology definitely have a speed advantage, coming from the low collector-to-substrate capacitance and the high f_T of the transistors. In addition, the patent-pending switching stage which fits uniquely to Harris' UHF1 process is another big contributor for the high speed. This switching circuitry requires low series-resistance NPN and PNP transdiodes available in UHF1. The rise and fall times of the pin driver are largely determined by the slew rate at the node VSO in Figure 2. The dominant mechanism for the slew rate is the charging/discharging of the collector-base capacitors of the transistors connected to the node VSO. The charging/discharging currents are coming from the switching stage current sources. The fast rise and fall times are achieved because of the negligible collector-to-substrate capacitance and the small base-collector capacitance due to the self-aligned recessed oxide [1].

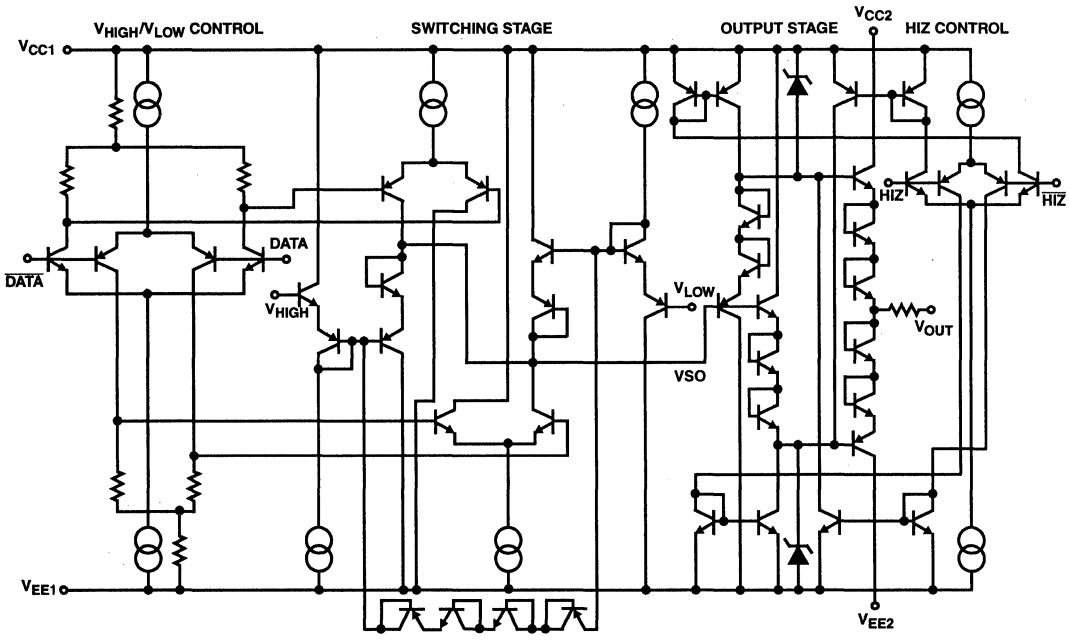


FIGURE 2. CIRCUIT SCHEMATIC

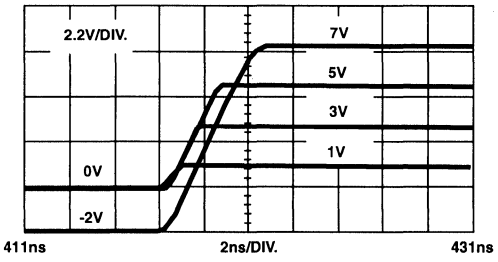


FIGURE 3. OUTPUT RESPONSE WITH VARIOUS V_{LOW} AND V_{HIGH} CONDITIONS

The DATA/$\overline{DATA}$ differential stage is not a factor for the speed if its current sources have enough current not to bottleneck the transient. However it should be noted that the propagation delay mismatch is determined by this stage. Sufficient current is allocated to the differential stage current sources to best match the low-to-high and high-to-low transient propagation delays.

Figure 3 shows various output responses, 0V to 1V, 0V to 3V, 0V to 5V, and -2V to 7V (full swing). The load condition is a 16 inch 50Ω SMA cable with a 5pF capacitor at the end of the cable. The rise/fall time with $5V_{P-P}$ is typically 1.45ns for the HFA5251. Pin drivers, built out of the same circuit structure as shown in Figure 2, can be made faster by trimming for a higher power supply current. Currently the pin driver has rise/fall times of less than 1ns (10% to 90% of $5V_{P-P}$) when I_{CC} is trimmed to 125mA. Further speed enhancement will be made if there is a market demand.

Basic ATE System Application

Figure 3 shows a pin driver in a typical per-pin ATE system. The pin driver works closely with the dual-level comparator and the active load. When the DUT pin acts as an input waiting for a series of digital signals, the pin driver becomes active with a logic "0" applied on the HiZ pin and provides the DUT pin with digital signals. When the DUT pin acts as an output, the pin driver output will be in high impedance mode (HiZ) with a logic "1" applied to the "HiZ" pin of the pin driver. During this high impedance mode the pin driver presents a capacitance of less than 5pF to the DUT. Special care has to be taken to match the impedance (to 50Ω) at the pin driver output to minimize reflections.

The dual level comparator detects the logic levels of the DUT pin when it acts as an output. The comparator has two threshold level inputs, VCH and VCL. The logic level information of DUT pin output is sent to the edge/window comparator through the dual level comparator. The edge/window comparator interprets this information in terms of corresponding transient performance in conjunction with the timing information. Thus it detects any possible failure transients.

The formatter sends a sequence of digital information to the pin driver which contains logic information over time. The active load is enabled when the DUT pin acts as an output. It simulates the load of the DUT pin by sinking or sourcing programmed current. Finally the sequencer controls the overall activities of the automatic testing.

Decoupling Circuit for Oscillation-Free Operation

To insure the oscillation-free operation in ATE or pulse generator applications, the pin driver needs an appropriate decoupling circuit on a printed circuit board which consists of chip capacitors and chip resistors. Figures 5 and 6 refer to a proven decoupling circuit currently working in the lab and a 1X scale film of its associated PC board (metal level).

The control pins, DATA, $\overline{DATA}$, HiZ, and $\overline{HiZ}$ are fed ECL signals through 50Ω micro-strip lines terminated with 50Ω for impedance matching since the input impedance at these pins is much higher than 50Ω. At the end of the micro-strip lines there is usually a high-speed pulse generator with an output impedance of 50Ω. A 50Ω micro-strip line is connected to each of the pins, $\overline{DATA}$ and $\overline{HiZ}$ through a 50Ω chip resistor to monitor the pulse signals.

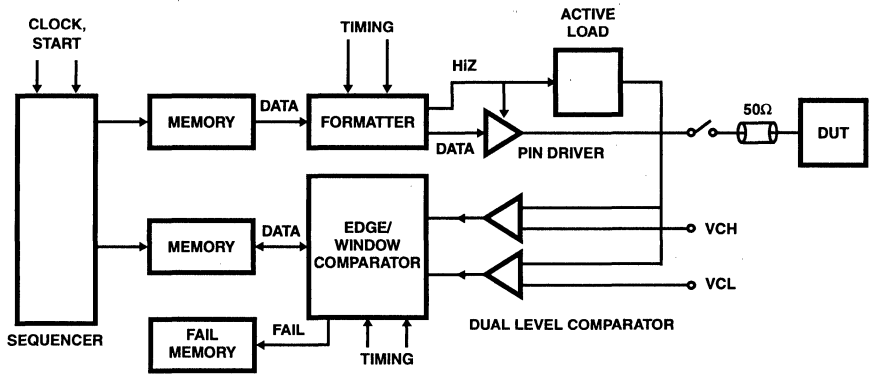


FIGURE 4. TYPICAL ATE SYSTEM

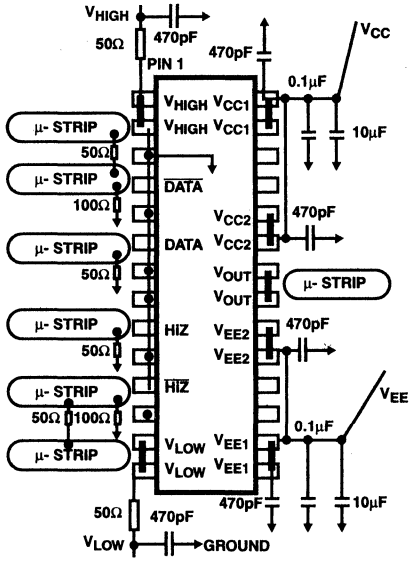


FIGURE 5. DECOUPLING CIRCUIT OF 28 PIN SOIC HFA5251 FOR OSCILLATION-FREE OPERATION

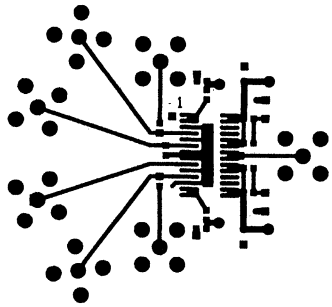


FIGURE 6. 1X FILM OF THE EVALUATION BOARD METAL

The two input voltage pins, V_{HIGH} and V_{LOW}, need to be protected from any capacitively coupled AC noise. Normally this protection can be achieved by having a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this protection circuit the pin driver may oscillate due to signals fed back from the output through the PC board ground.

The power supply pins, V_{CC1}, V_{CC2}, V_{EE1}, and V_{EE2}, require decoupling chip capacitors of 470pF, 0.1µF, 10µF. Having decoupling capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through either V_{CC2} or V_{EE2} during transients.

The output of the pin driver is usually connected to the device-under-test (DUT) through 50Ω micro-strip line and coaxial cable which carries the signal to a high input impedance DUT pin.

References

1. Chris K. Davis et. al., "UHF1: A High Speed Complementary Bipolar Analog Process on SOI," Bipolar Circuits and Technology Meeting Proceedings, pp260-263, October 1992.

2. Donald K. Whitney Jr., "Symmetrical, High Speed, Voltage Switching Circuit," United States Patent Pending, Filed November 1991.

Definition of Terms

V_{OH} and V_{OL}

Output High Voltage and Output Low Voltage. V_{OH} is the voltage at V_{OUT} when the HiZ input is Low and the DATA input is High. V_{OL} is the voltage at V_{OUT} when HiZ is Low and DATA is Low. The V_{OH} and V_{OL} levels are set with the V_{HIGH} and V_{LOW} inputs respectively.

Offset Voltage

Offset Voltage is the DC error between the voltage placed on V_{HIGH} or V_{LOW} and the resulting V_{OH} and V_{OL}. V_{HIGH} Offset Voltage Error is obtained by measuring V_{OH} with V_{HIGH} set to 0V and V_{LOW} set to -2.5V to minimize interaction effects. V_{LOW} Offset Voltage Error is the measurement of V_{OL} with V_{LOW} set to 0V and V_{HIGH} set to +7.5V.

Gain

Gain is defined as the ratio of output voltage change to input voltage change for a defined range. V_{HIGH} Gain is calculated with the following equation with V_{LOW} fixed at -2.5V

$$V_{HIGH}GAIN = \frac{V_{OH}(V_{HIGH}\text{ at }6.5V) - V_{OH}(V_{HIGH}\text{ at }-1V)}{7.5}$$

V_{LOW} Gain is calculated in a similar manner.

$$V_{LOW}GAIN = \frac{V_{OL}(V_{LOW}\text{ at }6V) - V_{OL}(V_{LOW}\text{ at }-1.5V)}{7.5}$$

V_{HIGH} is held fixed at 7.5V. These Gain calculations minimize the effects of Interaction and End Point Nonlinearities.

Linearity Error

Linearity Error is a measure of output voltage worst case deviation from a straight line that has been corrected for offset and 7.5V Gain. Linearity Error is given as a percentage of fullscale and is done in two ranges 5V and 8.5V. Data is measured at 0.5V steps from -1.5V to 7V for V_{HIGH} and -2V to 6.5V for V_{LOW}. The Linearity Error equation is as follows for 8.5V fullscale:

$$V_{OUT}(IDEAL) = \frac{V_{OUT}}{GAIN} - OFFSET$$

$$LINEARITYERROR = \frac{V_{OUT} - V_{OUT}(IDEAL)}{8.5}$$

The Linearity Error equation is as follows for 5V fullscale:

$$\text{LINEARITY ERROR} = \frac{V_{OUT} - V_{OUT(IDEAL)}}{5}$$

Linearity Error is calculated for every data point in the range and the worst case value is recorded.

End Point Deviation

End Point Deviation is the percent change of gain in the 1V range at the extremes of output voltage. Gain is calculated for each 0.5V step and then compared to the adjacent step for a percentage change. This specification is designed to quantify the amount of curvature present at the end points of output swing. V_{HIGH} and V_{LOW} inputs are corrected for gain and offset to provide more accurate V_{OH} and V_{OL} levels. For example V_{OH} End Point Deviation is tested in the range 5.7V to 6.7V as shown below:

$$GAIN_{6.7-6.2} = \frac{V_{OH}(V_{HIGH} \text{ at } 6.7V) - V_{OH}(V_{HIGH} \text{ at } 6.2V)}{0.5}$$

$$GAIN_{6.2-5.7} = \frac{V_{OH}(V_{HIGH} \text{ at } 6.2V) - V_{OH}(V_{HIGH} \text{ at } 5.7V)}{0.5}$$

$$\text{END POINT DEVIATION} = |GAIN_{6.7-6.2} - GAIN_{6.2-5.7}| \times 100$$

End Point Gain Error

End Point Gain Error (EPGE) is the V_{OUT} absolute error in millivolts for a V_{HIGH} change from 6.7V to 7V. The V_{HIGH} input is corrected for gain and offset to provide a more accurate V_{OH} level.

EPGE = V_{OH} (V_{HIGH} at 7V) - V_{OH} (V_{HIGH} at 6.7V) - 0.3

V_{HIGH} to V_{LOW} Interaction

V_{HIGH} to V_{LOW} Interaction is the change in V_{OUT} (the active channel) due to the inactive channel. V_{HIGH} Interaction is measured as the change in V_{OH} from 1V as V_{LOW} is moved from 0V to 750mV (V_{LOW} is corrected for gain and offset errors). V_{LOW} Interaction is measured as the change in V_{OL} from 0V as V_{HIGH} is moved from 1V to 250mV (with V_{HIGH} corrected for gain and offset errors). The minimum recommended difference between V_{HIGH} and V_{LOW} for the HFA5251 is 250mV.

Typical Performance Curves

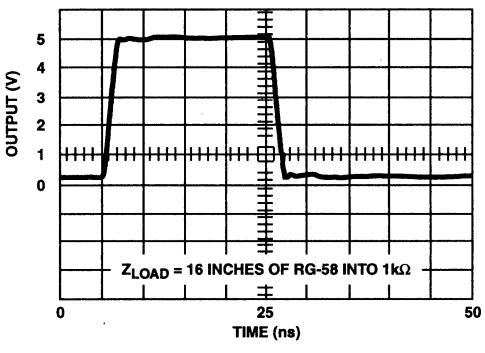


FIGURE 7. LARGE SIGNAL RESPONSE

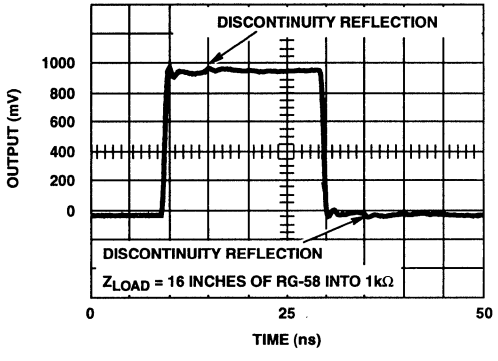


FIGURE 8. SMALL SIGNAL RESPONSE

Typical Performance Curves (Continued)

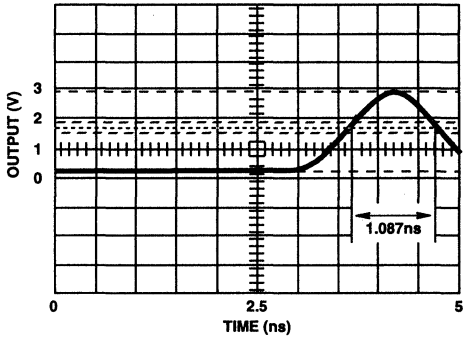


FIGURE 9. MINIMUM PULSE WIDTH

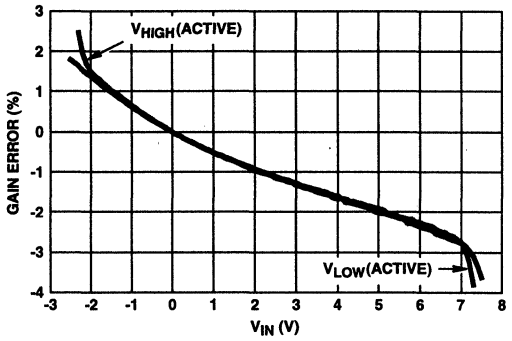


FIGURE 10. GAIN ERROR (FULLSCALE = 8.5V)

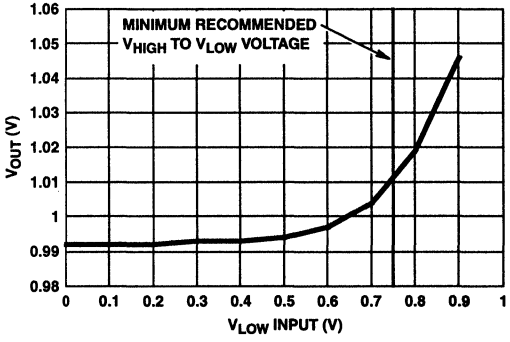


FIGURE 11. V_{HIGH}/V_{LOW} INTERACTION, V_{HIGH} ACTIVE (NOMINAL 1.0V)

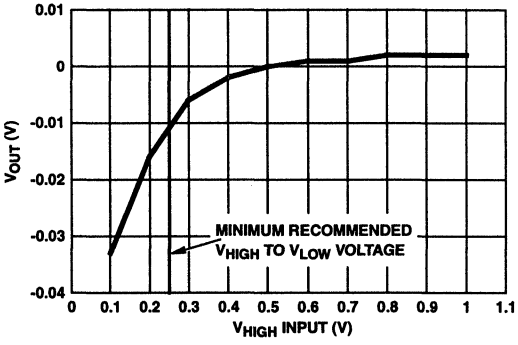


FIGURE 12. V_{HIGH}/V_{LOW} INTERACTION, V_{LOW} ACTIVE (NOMINAL 0.0V)

Die Characteristics

DIE DIMENSIONS:
2670µm x 1730µm x 525µm

METALLIZATION:
Type: Metal 1: Cu (2%) SiAl/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Backside: Gold

Type: Metal 2: Cu (2%) Al
Thickness: Metal 2: 16kÅ ±0.8kÅ

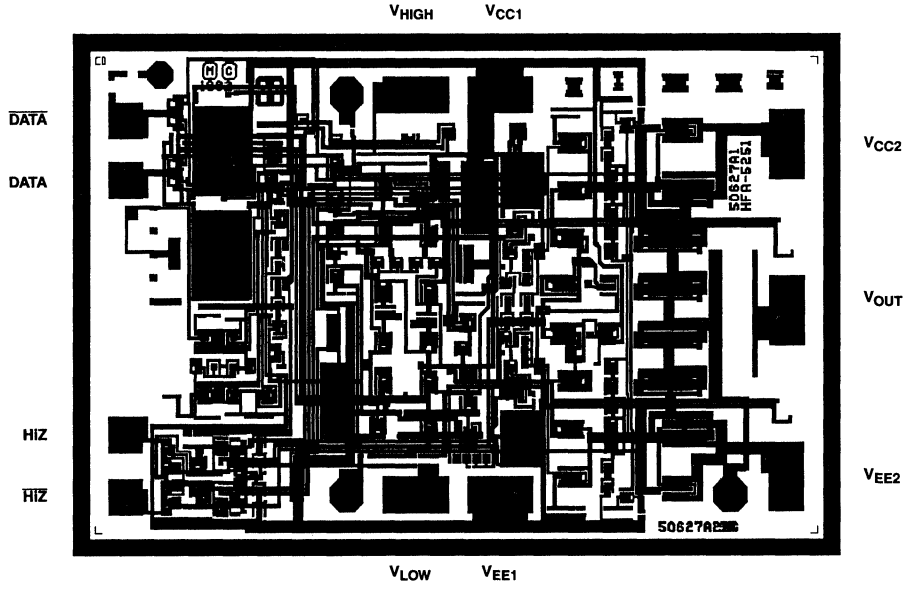
PASSIVATION:
Nitride, 4kÅ ±0.5kÅ

TRANSISTOR COUNT:
115

SUBSTRATE POTENTIAL:
Floating

Metallization Mask Layout

HFA5251



HARRIS SEMICONDUCTOR

HFA5253

November 1996

800MHz, Ultra High-Speed Monolithic Pin Driver

Features

- High Digital Data Rate 800MHz
- Very Fast Rise/Fall Times 500ps
- Wide Output Range . . . . . +8V to -3V
- Precise 50Ω Output Impedance
- High Impedance, Three-State Output Control
- Slew Rate Control

Applications

- IC Tester Pin Electronics
- Pattern Generators
- Pulse Generators
- Level Comparator/Translator

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA5253CB	0 to 50	20 Ld PSOP	M20.3A
HFA5253Y	$T_{JUNCTION}$ < 175	Die Form	N/A

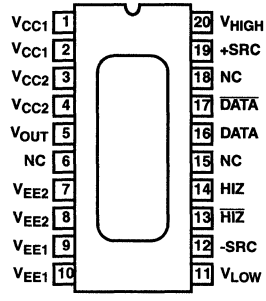
Description

The HFA5253 is a very high speed monolithic pin driver solution for high performance test systems. The device will switch at high data rates between two input voltage levels providing variable amplitude pulses. Slew Rate Control pins provide independent control over positive and negative slew rate allowing the customer to optimize the pin driver speed for their application. The output impedance is trimmed to achieve a precision 50Ω source for impedance matching. Two differential ECL/TTL compatible inputs control the operation of the HFA5253, one controlling the V_{HIGH}/V_{LOW} switching and the other controlling the output's high-impedance state. The HFA5253's 800MHz data rate makes it compatible with today's high-speed VLSI test systems and the +8V to -3V output swing satisfies the most stringent testing requirements of all common logic families.

The HFA5253 is manufactured in Harris' proprietary complementary bipolar UHF-1 process.

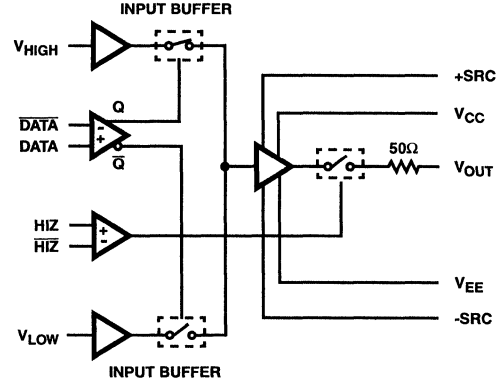
Pinout

HFA5253 (PSOP)
TOP VIEW



POWER PSOP PACKAGE
(HEAT SLUG SURFACE IS ELECTRICALLY FLOATING)

Block Diagram



TRUTH TABLE FOR V_{OUT}

		DATA	
		0	1
HIZ	0	V_{LOW}	V_{HIGH}
	1	HIZ	HIZ

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **4003.2**

Pin Descriptions

NAME	FUNCTION
V_{CC1}	Positive Supply. Nominal value is 11.2V ±0.2V. Reducing supply voltage below 11.0V will reduce positive output voltage swing. The total supply voltage from V_{CC1} to V_{EE1} should not exceed 18.0V for normal operation or exceed 19.0V to prevent damage. Harris recommends two wire bonds to this pad to provide the lowest possible impedance. In addition, power supply decoupling chip capacitors of 470pF, 0.1µF and a 10µF tantalum are recommended. Do not connect the V_{CC1} and V_{CC2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1µF || 10.0µF).
V_{EE1}	Negative Supply. Nominal value is -6.4V ±0.2V. A supply voltage more positive than -6.2V will reduce negative output voltage swing. The total supply voltage from V_{CC1} to V_{EE1} should not exceed 18.0V for normal operation or exceed 19.0V to prevent damage. Harris recommends two wire bonds to this pad to provide the lowest possible impedance. In addition, power supply decoupling chip capacitors of 470pF, 0.1µF and a 10µF tantalum are recommended. Do not connect the V_{EE1} and V_{EE2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1µF || 10.0µF).
V_{CC2}	Output Stage Positive Supply. Nominal voltage and cautions are the same as for V_{CC1}. Having decoupling chip capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through this pad to the output during transients. Harris recommends two wire bonds for this pad. Do not connect the V_{CC1} and V_{CC2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1µF || 10.0µF).
V_{EE2}	Output Stage Negative Supply. Nominal voltage and cautions are the same as for V_{EE1}. Having decoupling chip capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through this pad to the output during transients. Harris recommends two wire bonds for this pad. Do not connect the V_{EE1} and V_{EE2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1µF || 10.0µF).
V_{HIGH}	Input Voltage High is used to set the output high level V_{OH}. V_{HIGH} is sensitive to capacitively coupled AC noise. Protection from high frequency noise can be achieved with a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this precaution the pin driver may oscillate due to feedback from the output through the PC board ground.
V_{LOW}	Input Voltage Low is used to set the output low level V_{OL}. V_{LOW} is sensitive to capacitively coupled AC noise. Protection from high frequency noise can be achieved with a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this precaution the pin driver may oscillate due to feedback from the output through the PC board ground.
V_{OUT}	Driver Output. The output impedance has been laser trimmed to match a 50Ω transmission line ±2Ω. Custom output impedance trimming is available (contact sales office for details) to provide the best match possible to your 50Ω system.
$\overline{DATA}$, DATA	Differential Digital Inputs used to switch V_{OUT} to the V_{HIGH} or V_{LOW} level. Harris recommends this input pair be driven by complementary ECL signals to provide optimal switching speeds and timing accuracy. However a large Common Mode and Differential Voltage Range is provided to accommodate a variety of signals including single ended TTL and CMOS. When using single ended signals the other input must be tied to an appropriate threshold voltage.
$\overline{HIZ}$, HIZ	Differential Digital Inputs used to switch V_{OUT} from an Active to a High Impedance State. Harris recommends that this input pair be driven by complementary ECL signals to provide optimal switching speeds and timing accuracy. However a large Common Mode and Differential Voltage Range is provided to accommodate a variety of signals including single ended TTL and CMOS. When using single ended signals the other input must be tied to an appropriate threshold voltage.
+SRC	The Positive Slew Rate Control Pin adjusts the rising edge slew rate with an external current I_{STEAL}. I_{STEAL} draws current (0mA to 10mA) from an internal current source limiting the rate of change of the high impedance node. Typically an external resistor to GND is sufficient to set the slew rate at a desired level. Leaving the +SRC Pin open will give the highest speed performance. The external current I_{STEAL} for a resistor R_{STEAL} connected from +SRC to GND may be calculated by: $I_{STEAL} = (V_{CC} - 0.35)/R_{STEAL}$.
-SRC	The Negative Slew Rate Control Pin adjusts the falling edge slew rate with an external current I_{STEAL}. I_{STEAL} supplies current (0mA to 10mA) to an internal current source limiting the amount of current being drawn from the circuit and thus limiting the rate of change of the high impedance node. Typically an external resistor to GND is sufficient to set the slew rate at a desired level. Leaving the -SRC Pin open will give the highest speed performance. The external current I_{STEAL} for a resistor R_{STEAL} connected from -SRC to GND may be calculated by: $I_{STEAL} = (V_{EE} + 0.35)/R_{STEAL}$.

Absolute Maximum Ratings

Supply Voltage 19V
Differential Input Voltage (DATA and HIZ) 5V
Output Current Continuous (Note 1) 160mA
Input Voltage (Any pin except as specified) ..... V_{CC} to V_{EE}
V_{OUT} Voltage (Note 3) ..... 9V to -4V
V_{HIGH} Voltage ..... V_{CC} to -4V

Operating Conditions

V_{LOW} Voltage ..... 9V to V_{EE}
V_{HIGH} to V_{LOW} Voltage ..... 11V to 0V ($V_{HIGH} > V_{LOW}$)
Slew Rate Control Current (+SRC, -SRC) 12mA
Temperature Range ..... 0°C to 50°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld PSOP Package	49	2

(θ_{JC} Measured At Copper Slug Top Center with Infinite Heat Sink)
Maximum Junction Temperature (Die) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(PSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:
1. Internal Power Dissipation may limit Output Current below 160mA.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. Shorting the output to a voltage outside the specified range may damage the output.

Electrical Specifications

V_{CC} = +11.2V; V_{EE} = -6.4V; V_{IH} = -0.9V; V_{IL} = -1.75V; +SRC and -SRC are Not Connected Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS (V_{HIGH}, V_{LOW})							
V_{HIGH} Input Offset Voltage		A	25	-150	-50	+50	mV
V_{LOW} Input Offset Voltage		A	25	-150	-50	+50	mV
V_{HIGH} Input Bias Current	V_{HIGH} = -3.25V to +8.5V	A	25	-50	110	400	µA
V_{LOW} Input Bias Current	V_{LOW} = -3.5V to +8.25V	A	25	-400	-110	50	µA
V_{HIGH} Voltage Range		A	25	-3.5	-	8.5	V
V_{LOW} Voltage Range		A	25	-3.5	-	8.5	V
V_{HIGH} to V_{LOW} Differential Voltage Range	$V_{HIGH} \geq V_{LOW}$	A	25	0	-	9.5	V
V_{HIGH}/V_{LOW} Interaction (Notes 5, 17)	At 500mV	A	25	-	2	4	mV
	At 250mV	A	25	-	20	40	mV
LOGIC INPUT CHARACTERISTICS (DATA, $\overline{DATA}$, HIZ, $\overline{HIZ}$)							
Logic Input Voltage Range		B	25	-3	-	8	V
Logic Differential Input Voltage		B	25	0.4	-	5	V
DATA/$\overline{DATA}$ Logic Input High Current	V_{IH} = 0V, V_{IL} = -2V	A	25	-50	110	700	µA
DATA/$\overline{DATA}$ Logic Input Low Current	V_{IH} = 0V, V_{IL} = -2V	A	25	-700	-300	50	µA
HIZ/$\overline{HIZ}$ Logic Input High Current	V_{IH} = 0V, V_{IL} = -2V	A	25	-50	70	400	µA
HIZ/$\overline{HIZ}$ Logic Input Low Current	V_{IH} = 0V, V_{IL} = -2V	A	25	-400	-80	50	µA
TRANSFER CHARACTERISTICS							
V_{HIGH} Voltage Gain	V_{HIGH} = -1V to 6.5V	A	25	0.95	0.97	1	V/V
V_{LOW} Voltage Gain	V_{LOW} = -1.5V to 6V	A	25	0.95	0.97	1	V/V
V_{HIGH}/V_{LOW} Linearity Error	Fullscale = 5V, Note 6	A	25	-0.2	-	0.2	%
	Fullscale = 10.5V, Note 7	A	25	-0.4	-	0.4	%
V_{HIGH}/V_{LOW} -3dB Bandwidth	$200mV_{P-P}$	B	25	-	100	-	MHz
Typical Slew Rate Control Range	I_{STEAL} = 0mA to 10mA, 5V Step	B	25	1.0	-	2.8	V/ns
+SRC Pin Voltage		C	25	-	V_{CC} - 0.35	-	V
-SRC Pin Voltage		C	25	-	V_{EE} + 0.35	-	V
SWITCHING CHARACTERISTICS (Z_{LOAD} = 16 inches of RG-58 Terminated with 50Ω)							
Propagation Delay (Notes 8, 10)		B	25	1	-	2	ns
Propagation Delay Match (Rising to Falling Edge, Notes 8, 10)		B	25	-100	-	100	ps
Rising Edge Propagation Delay vs Duty Cycle (Notes 9, 10)		B	25	-120	-20	80	ps

Electrical Specifications V_{CC} = +11.2V; V_{EE} = -6.4V; V_{IH} = -0.9V; V_{IL} = -1.75V; +SRC and -SRC are Not Connected Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Falling Edge Propagation Delay vs Duty Cycle (Notes 9, 10)		B	25	-80	20	120	ps
Active to HIZ Delay (Note 10)		B	25	1.5	2.0	2.5	ns
HIZ to Active Delay (Note 10)		B	25	2.8	3.3	3.8	ns
TRANSIENT RESPONSE (Z_{LOAD} = 16 inches of RG-58 Terminated with 5pF)							
Rise/Fall Time	$1V_{P-P}$, 20% - 80% (Note 11)	B	25	350	450	500	ps
	$3V_{P-P}$, 10% - 90% (Note 11)	B	25	700	890	1000	ps
	$5V_{P-P}$, 10% - 90% (Note 12)	B	25	1.1	1.3	1.7	ns
Rise/Fall Time Match (Note 12)		B	25	-	100	-	ps
Minimum Pulse Width (Note 13)	$1V_{P-P}$	B	25	-	1.0	-	ns
	$3V_{P-P}$	B	25	-	1.2	-	ns
	$5V_{P-P}$	B	25	-	2.0	-	ns
Overshoot/Undershoot/Preshoot	$3V_{P-P}$	B	25	-	5	-	%
Data Settling Time (Note 14)	To 1%	B	25	-	10	-	ns
OUTPUT CHARACTERISTICS							
Output Voltage Swing	No Load at V_{CC} = 11V, V_{EE} = -6.2V	A	25	-3	-	8	V
Output Amplitude Voltage	V_{OH} - V_{OL}	A	25	0.25	-	9.0	V
DC Output Resistance (Note 15)	-3V to 8V	A	25	45	47	49	Ω
Output Leakage - HIZ	-3V to 8V	A	25	-100	-	100	nA
Output Capacitance - HIZ		C	25	-	5	-	pF
Output Current - Active		A	25	80	100	-	mA
Output Short Circuit Range (Note 3)		A	25	-4.0	-	9.0	V
POWER SUPPLY CHARACTERISTICS (V_{HIGH} = 5V Active, No Load)							
V_{HIGH} Power Supply Rejection Ratio (Note 16)		A	25	-	14	40	mV/V
V_{LOW} Power Supply Rejection Ratio (Note 16)		A	25	-	14	40	mV/V
Total Supply Current		A	25	90	96	98	mA
I_{CC1}/I_{EE1} Supply Current		B	25	-	74	-	mA
I_{CC2}/I_{EE2} Supply Current		B	25	-	22	-	mA
Supply Voltage Range	V_{CC}	A	25	11.0	11.2	11.4	V
	V_{EE}	A	25	-6.6	-6.4	-6.2	V
	V_{CC} - V_{EE}	A	25	17.2	-	18.0	V
Power Dissipation	V_{CC} = 11.2V, V_{EE} = -6.4V, No Load	A	25	-	-	1.72	W

NOTES:

4. Test Level: A = 100% production tested, B = Typical or limit based on lab characterization of a limited number of lots, C = Design Information, goal or condition.
5. V_{HIGH} to V_{LOW} Interaction is measured as the change in V_{OUT} (the active channel) due to a change in the inactive channel. V_{HIGH} Interaction at 250mV is measured as the deviation from 1V as V_{LOW} is changed from 0V to 750mV (Referred to V_{OUT}). V_{LOW} Interaction at 250mV is measured as the deviation from 0V as V_{HIGH} is changed from 1V to 250mV (Referred to V_{OUT}).
6. For V_{HIGH} = 0V to 5V, for V_{LOW} = 0V to 5V, Fullscale = 5V, 0.1% = 5mV. Output Amplitude (V_{HIGH} - V_{LOW}) = $1V_{P-P}$.
7. For V_{HIGH} = -2.5V to 8V, for V_{LOW} = -3.0V to 7.5V, Fullscale = 10.5V, 0.1% = 10.5mV. Output Amplitude (V_{HIGH} - V_{LOW}) = $1V_{P-P}$.
8. 3V Step, 50% duty cycle, 200ns period.
9. 0V to 3V Step, 200ns period, Pulse Width is varied from 5ns to 195ns.
10. Test is performed into a 50Ω load with a 3V step. Measurement is made from the 50% of the input to 50% of output.
11. Limit based on calculation. Not 100% tested.
12. 5V Step, 50% duty cycle, 100ns period. 100% Tested.
13. Minimum Pulse Width is measured 50% to 50% of specified amplitude with pulse peak at 100% of amplitude.
14. 3V Step, measured from 50% of input to ±1% of reference value at 50ns.
15. Dynamic Output Resistance will be higher (typ 48.5Ω) than DC Output Resistance. DC Output Resistance is measured at 0V with I_{OUT} set from 0mA to 40mA.
16. V_{HIGH} = 2.6V, V_{LOW} = 2.3V, V_{CC} = 10.2V to 11.2V, V_{EE} = -5.4V to -6.4V.
17. Input voltages V_{HIGH} and V_{LOW} are corrected for Offset Voltage and Gain Error.

Functional Block Diagram

The HFA5253 functional block diagram is shown in on the first page of this data sheet.

The control inputs, DATA and DATA, determines the output level. If DATA is at logic "1" and DATA is at logic "0", the output level will be the same as V_{HIGH}. If DATA is at logic "0" and DATA is at logic "1", the output will be the same as V_{LOW}. The control inputs, HIZ and HIZ, cause the output to become either active or high-impedance. If HIZ is at logic "1" and HIZ is at logic "0", the output will be in high impedance mode. If HIZ is at logic "0" and HIZ is at logic "1", the output will be enabled. The output impedance in the enabled mode is trimmed to 50Ω.

Circuit Schematic

The Pin Driver circuit consists of a switch, an output buffer, and two differential control elements as shown in the circuit Schematic Diagram.

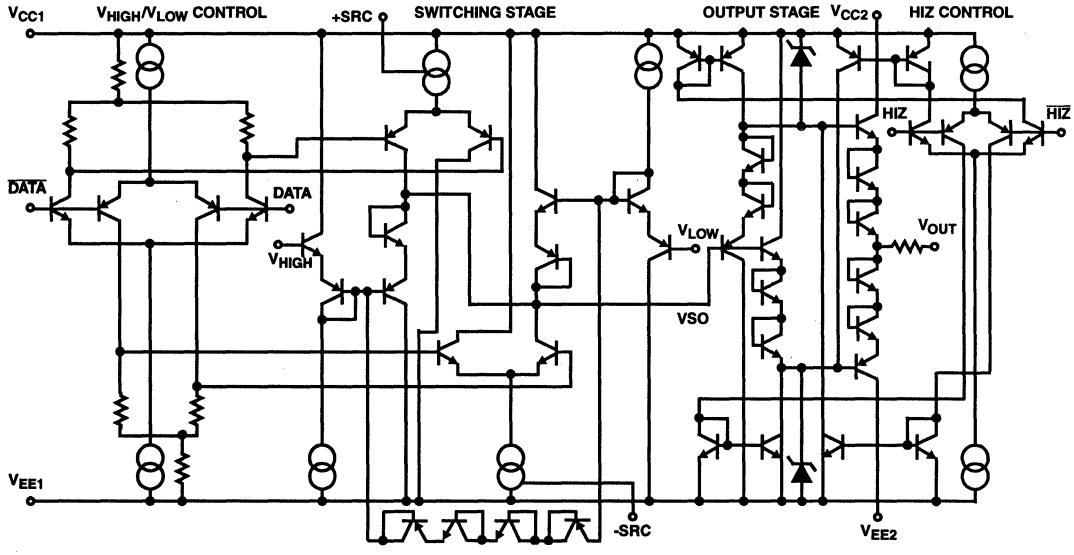
A two stage approach, separating the switch from the output buffer, allows the speed and accuracy requirements of the switch to be de-coupled from the load driving capability of the buffer.

The patented switch circuitry [3] uses cascaded emitter followers as input buffers and also to switch the input V_{HIGH} and V_{LOW} to node VSO. Dual differential pairs controlled by the data timing (DATA and DATA) direct current to select either the V_{HIGH} or V_{LOW} switch. Matching transistor types and transdiodes improve linearity and lowers the voltage offset and offset drift. Stacking two emitter-base junctions allows the V_{HIGH} to V_{LOW} range to be extended to two Emitter - Base breakdown voltages of the process. The speed of the pin driver is largely determined by the current flowing through the switch stage and the collector-base capacitance of the output stage transistors connected to the node VSO. The Slew Rate Control Pins, +SRC and -SRC, allow the user to control the amount of current available in the V_{HIGH} and V_{LOW} switch, respectively and thus the slew rate of node VSO.

The output stage consists of cascaded emitter followers constructed in a typical push-pull manner as shown in the Schmatic Diagram. However, transdiodes are added to increase the voltage breakdown characteristics of the output during high impedance mode. HIZ and $\overline{HIZ}$ control the mode of the output stage. A trimmed, NiCr resistor is added to provide the 50Ω output impedance.

Overall, a symmetry of device types and paths is constructed to improve slew and delay symmetry. Both the V_{HIGH} to V_{OUT} path and the V_{LOW} to V_{OUT} path contain three NPN and three PNP transistors operating at similar collector currents. Thus the transient response of V_{HIGH} to V_{LOW} and V_{LOW} to V_{HIGH} are kept symmetrical. Also, a trimmable current reference (not shown) allows the AC parameters to be adjusted to maintain unit to unit consistency.

Schematic Diagram



Application Information

The HFA5253 is a pin driver designed for use in automatic test equipment (ATE) and high speed pulse generators. Pin drivers, especially those with very high-speed performance, have generally been implemented with discrete transistors (sometimes GaAs) on a circuit board or in a hybrid. Recent IC process improvements, specifically Harris' UHF1 process [2], have enabled the manufacturing of the 500MHz and 800MHz silicon monolithic pin drivers, HFA5250, HFA5251 and now the HFA5253.

The ultra high speed performance of the HFA5253 is a result of UHF1 process leverages: low parasitic collector-to-substrate capacitance of the bonded wafer, low collector-to-base parasitic capacitance of the self-aligned base/emitter technology and ultra high f_T NPN (8GHz) and PNP (5.5GHz) poly-silicon transistors.

Definition of Terms

V_{OH} and V_{OL}

Output High Voltage and Output Low Voltage. V_{OH} is the voltage at V_{OUT} when the HIZ input is low and the DATA input is high. V_{OL} is the voltage at V_{OUT} when HIZ is low and DATA is low. The V_{OH} and V_{OL} levels are set with the V_{HIGH} and V_{LOW} inputs respectively.

Offset Voltage

Offset Voltage is the DC error between the voltage placed on V_{HIGH} or V_{LOW} and the resulting V_{OH} and V_{OL}. V_{HIGH} Offset Voltage Error is obtained by measuring V_{OH} with V_{HIGH} set to 0V and V_{LOW} set to -2.5V to minimize interaction effects. V_{LOW} Offset Voltage Error is the measurement of V_{OL} with V_{LOW} set to 0V and V_{HIGH} set to +7.5V.

Gain

Gain is defined as the ratio of output voltage change to input voltage change for a defined range. V_{HIGH} Gain is calculated with the following equation with V_{LOW} fixed at -2.5V:

$$V_{HIGH}GAIN = \frac{V_{OH}(V_{HIGH}\text{at } 6.5V) - V_{OH}(V_{HIGH}\text{at } -1V)}{7.5}$$

V_{LOW} Gain is calculated in a similar manner.

$$V_{LOW}GAIN = \frac{V_{OL}(V_{LOW}\text{at } 6V) - V_{OL}(V_{LOW}\text{at } -1.5V)}{7.5}$$

V_{HIGH} is held fixed at 7.5V. These Gain calculations minimize the effects of Interaction and End Point Nonlinearities.

Linearity Error

Linearity Error is a measure of output voltage worst case deviation from a straight line that has been corrected for offset and 7.5V Gain. Linearity Error is given as a percentage of fullscale and is done in two ranges, 5V and 10.5V. DATA is measure at 0.5V steps from -2.5V to 8V for V_{HIGH} and -3V to 7.5V for V_{LOW}. The Linearity Error equation is as follows for 10.5V fullscale:

$$V_{OUT}(IDEAL) = V_{IN} \times Gain + Offset$$

$$\text{Linearity Error} = \frac{V_{OUT} - V_{OUT}(IDEAL)}{10.5}$$

The Linearity Error equation is as follows for 5V fullscale:

$$\text{Linearity Error} = \frac{V_{OUT} - V_{OUT}(IDEAL)}{5}$$

Linearity Error is calculated for every data point in the range and the worst case value is recorded.

V_{HIGH} to V_{LOW} Interaction

V_{HIGH} to V_{LOW} Interaction is the change in V_{OUT} (the active channel) due to the inactive channel. V_{HIGH} Interaction is measured as the change in V_{OH} from 1V as V_{LOW} is moved from 0V to 750mV (V_{LOW} is corrected for gain and offset errors). V_{LOW} Interaction is measured as the change in V_{OL} from 0V as V_{HIGH} is moved from 1V to 250mV (with V_{HIGH} corrected for gain and offset errors). The minimum recommended difference between V_{HIGH} and V_{LOW} for the HFA5253 is 250mV.

Speed Advantage

Harris Pin Drivers on bonded-wafer technology definitely have a speed advantage, coming from the low collector-to-substrate capacitance and the high f_T of the transistors. In addition, the patented switching stage which fits uniquely to Harris' UHF1 process is another big contributor for the high speed. This switching circuitry requires low series-resistance NPN and PNP transdiodes available in UHF1. The rise and fall times of the pin driver are largely determined by the slew rate at the node VSO in the Schematic. The dominant mechanism for the slew rate is the charging/discharging of the collector-base capacitors of the transistors connected to the node VSO. The charging/discharging currents are coming from the switching stage current sources. The fast rise and fall times are achieved because of the negligible collector-to-substrate capacitance and the small base-collector capacitance due to the self-aligned recessed oxide [2].

The DATA/DATA differential stage is not a factor for the speed if its current sources have enough current not to bottleneck the transient. However it should be noted that the propagation delay mismatch is determined by this stage. Sufficient current is allocated to the differential stage current sources to best match the low-to-high and high-to-low transient propagation delays.

The specified load condition is a 16 inch 50Ω SMA cable with a 5pF capacitor at the end of the cable. This load simulates a typical ATE environment for a DUT (Device Under Test) with high impedance (>1kΩ) digital inputs. The rise/fall time for HFA5253 with $5V_{P-P}$ is typically 1.3ns. Pin drivers, built out of the same circuit structure as shown in the Schematic, can be made faster by trimming for a higher power supply current. Currently the pin driver has rise/fall times of less than 1ns (10% to 90% of $5V_{P-P}$) when I_{CC} is trimmed to 125mA. Further speed enhancement will be made if there is a market demand.

Basic ATE System Application

Figure 1 shows a pin driver in a typical per-pin ATE system. The pin driver works closely with the Dual-Level Comparator and the Active Load. When the DUT pin acts as an input waiting for

a series of digital signals, the pin driver becomes active with a logic "0" applied on the HIZ pin and provides the DUT pin with digital signals. When the DUT pin acts as an output, the pin driver output will be in high impedance mode (HIZ) with a logic "1" applied to the "HIZ" pin. During this high impedance mode the pin driver presents a capacitance of less than 5pF to the DUT. Special care has to be taken to match the impedance (to 50Ω) at the pin driver output to minimize reflections.

The Dual-Level Comparator detects the logic levels of the DUT pin when it acts as an output. The comparator has two threshold level inputs, V_{CH} and V_{CL}. The logic level information of the DUT pin output is sent to the edge/window comparator through the Dual-Level Comparator. The edge/window comparator interprets this information in terms of corresponding transient performance in conjunction with the timing information. Thus it detects any possible failure transients.

The formatter sends a sequence of digital information to the pin driver which contains logic information over time. The Active Load is enabled when the DUT pin acts as an output. It simulates the load of the DUT pin by sinking or sourcing programmed current. Finally the sequencer controls the overall activities of the automatic testing.

Decoupling Circuit for Oscillation-Free Operation

To ensure oscillation-free operation in ATE or pulse generator applications, the pin driver needs an appropriate decoupling circuit on a printed circuit board which consists of chip capacitors and chip resistors. Figures 2, 3, and 4 refer to a proven decoupling circuit currently working in the lab and a 1X scale film of its associated PC board (metal level). Do not connect the V_{CC1} and V_{CC2} pins or the V_{EE1} and V_{EE2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1µF || 10.0µF).

The control pins, DATA, $\overline{DATA}$, HIZ, and $\overline{HIZ}$ are fed ECL signals through 50Ω micro-strip lines terminated with 50Ω for impedance matching since the input impedance at these pins is much higher than 50Ω. At the end of the micro-strip lines there is usually a high-speed pulse generator with an output impedance of 50Ω. A 50Ω micro-strip line is connected to each of the pins, $\overline{DATA}$ and $\overline{HIZ}$ through a 50Ω chip resistor to monitor the pulse signals.

PARTS LIST

QTY	VALUE	COMPONENT
6	470pF	Chip Cap: 0805
4	0.1µF	Chip Cap: 0805
2	10µF	Tant.
8	50Ω	Chip Res: 0805
2	100Ω	Chip Res: 0805
7	SMA Jacks	Wide Body
1	20 Lead PSOP	HFA5253
4	4-40	1" Standoff
4	4-40	1/4" Screws
2	Twisted Wire Assemblies with 4 Wires Each: One for V_{CC}, V_{HIGH}, +SRC, GND; and 1 for V_{EE}, V_{LOW}, -SRC, GND.	

The input pins, V_{HIGH}, V_{LOW}, +SRC, and -SRC need to be protected from any capacitively coupled AC noise. Normally this protection can be achieved by having a low pass filter consisting of a 50Ω chip resistor and a chip capacitor, 470pF for V_{HIGH}/V_{LOW} and 0.1µF for +SRC/-SRC. Without this protection circuit the pin driver may oscillate due to signals fed back from the output through the PC board ground.

The power supply pins, V_{CC1}, V_{CC2}, V_{EE1}, and V_{EE2}, require decoupling chip capacitors of 470pF, 0.1µF, 10µF. Having decoupling capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through either V_{CC2} or V_{EE2} during transients.

The output of the pin driver is usually connected to the device-under-test (DUT) through 50Ω micro-strip line and coaxial cable which carries the signal to a high input impedance DUT pin.

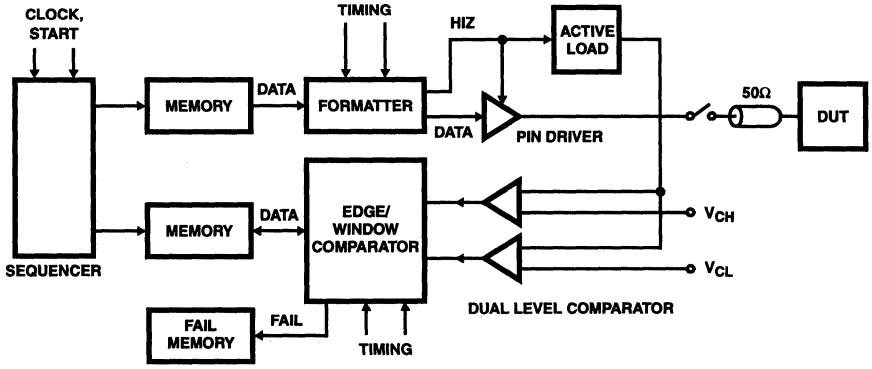


FIGURE 1. TYPICAL ATE SYSTEM

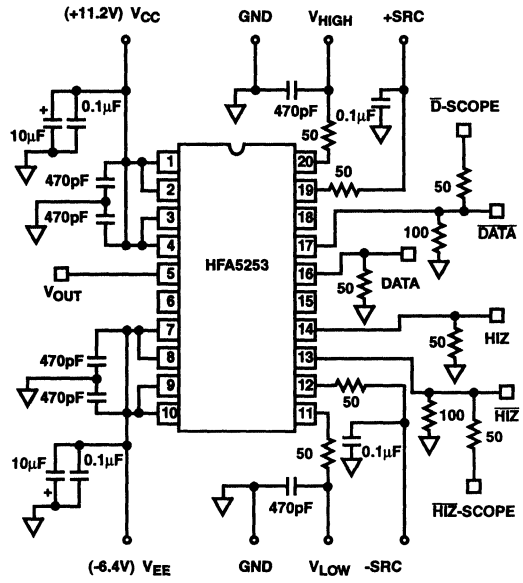


FIGURE 2. DECOUPLING CIRCUIT SCHEMATIC

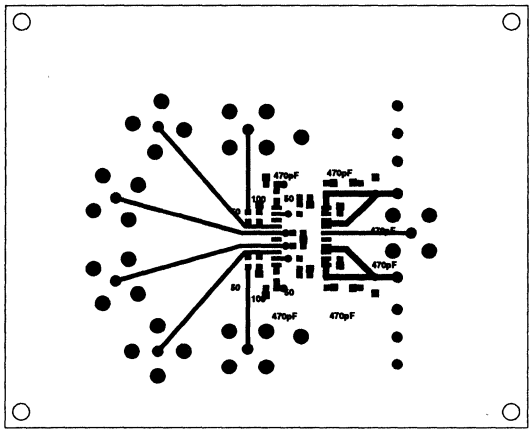


FIGURE 3. 1X PC BOARD LAYOUT (BOTTOM VIEW)

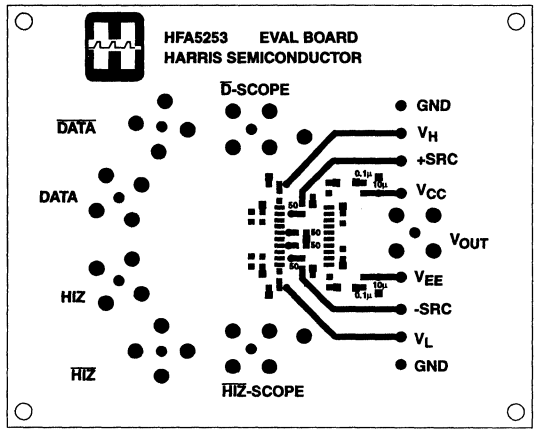


FIGURE 4. 1X PC BOARD LAYOUT (TOP VIEW)

References

[1] Taewon Jung and Donald K. Whitney Jr., "A 500MHz ATE Pin Driver," Bipolar Circuits and Technology Meeting Proceedings, pp238-241, October 1992.

[2] Chris K. Davis et. al., "UHF1: A High Speed Complementary Bipolar Analog Process on SOI," Bipolar Circuits and Technology Meeting Proceedings, pp260-263, October 1992.

[3] Donald K. Whitney Jr., "Symmetrical, High Speed, Voltage Switching Circuit," United States Patent Pending, Filed November 1991.

Typical Performance Curves

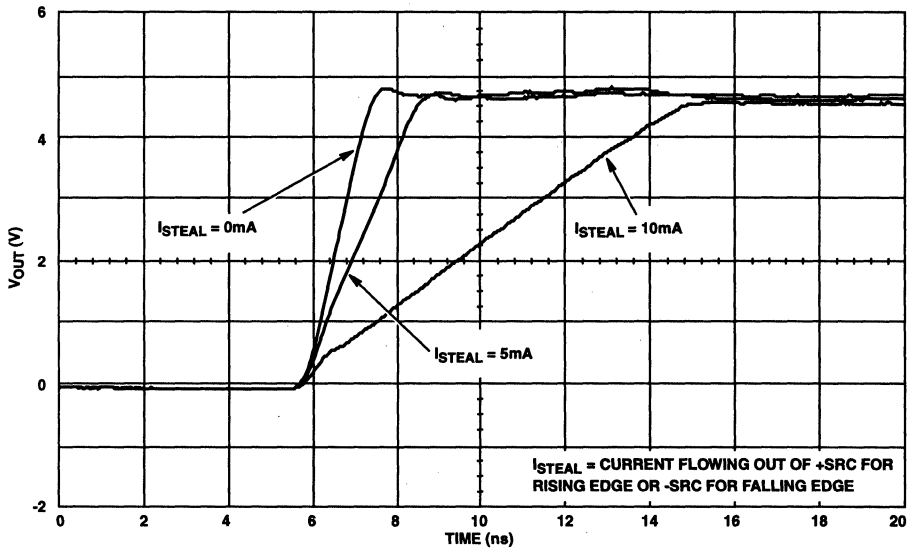


FIGURE 5. 5V STEP RESPONSE vs SLEW RATE CONTROL

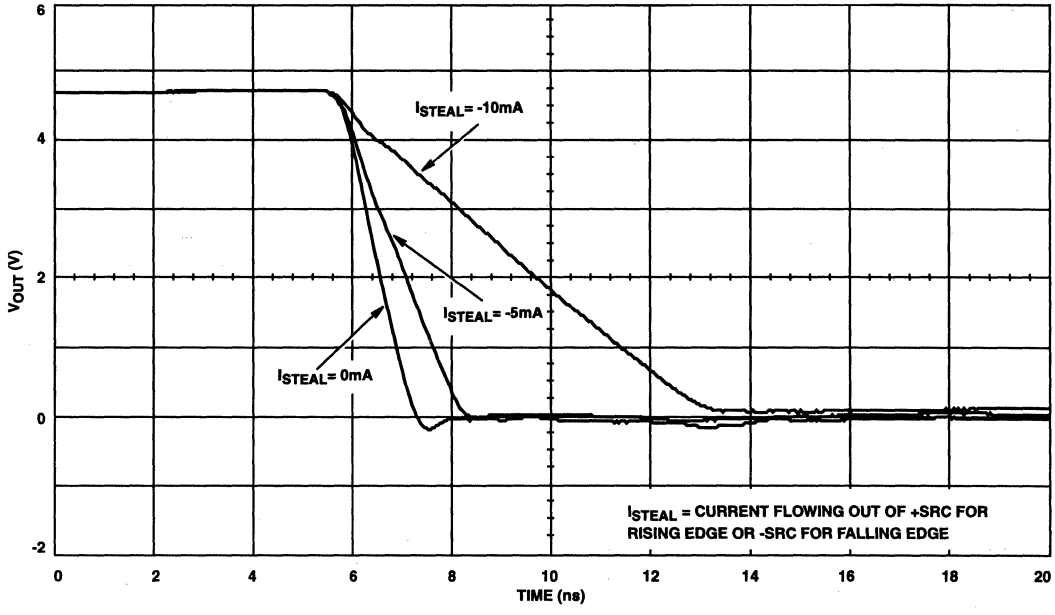


FIGURE 6. 5V STEP RESPONSE vs SLEW RATE CONTROL

Typical Performance Curves (Continued)

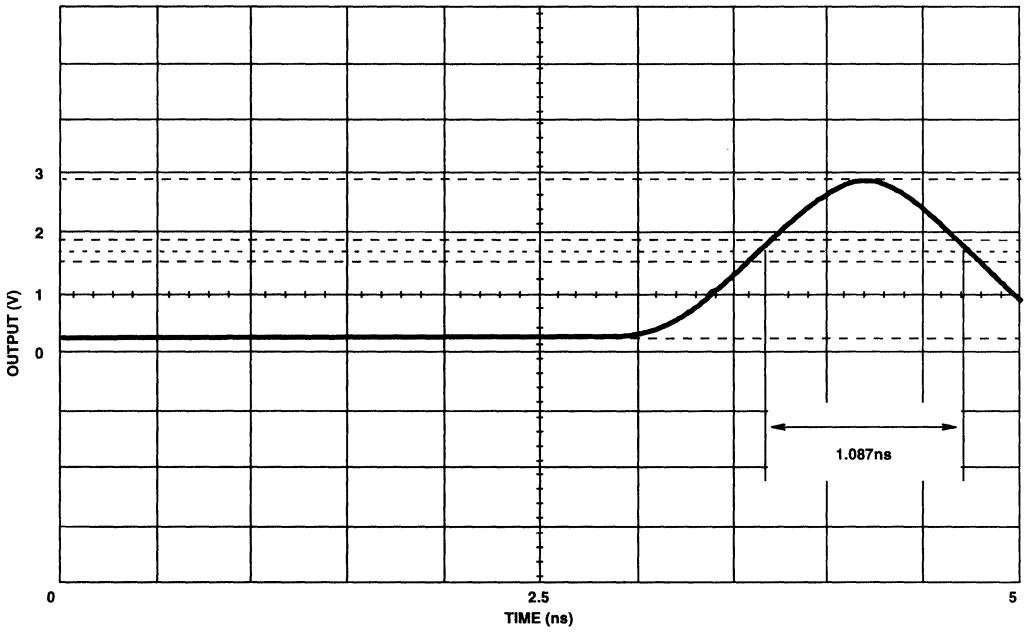


FIGURE 7. MINIMUM PULSE WIDTH, 1V/DIV.; 500ps/DIV.

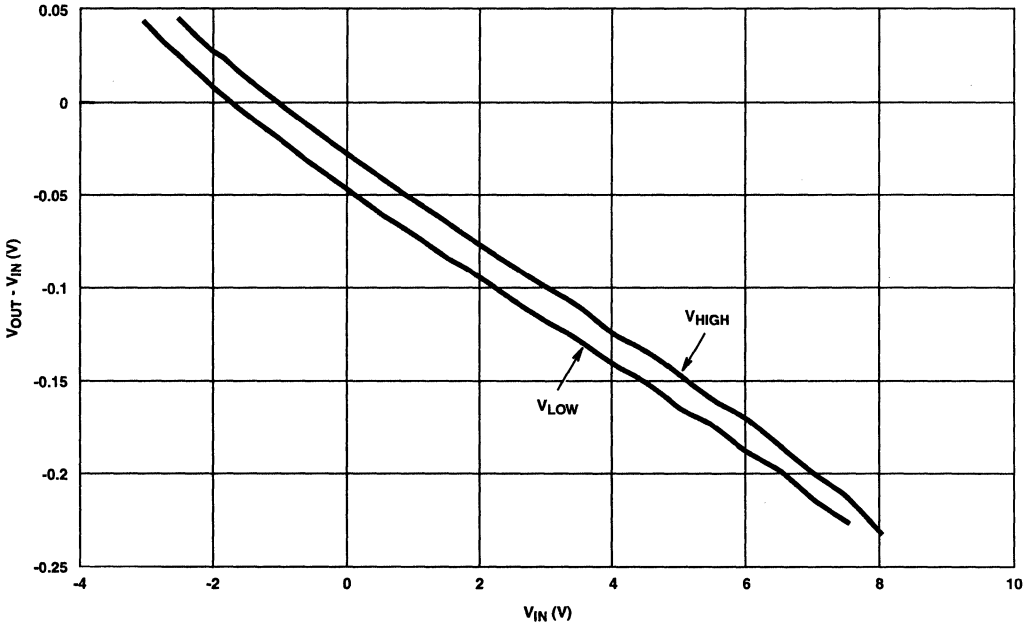


FIGURE 8. V_{OUT} ERROR vs V_{IN}

Typical Performance Curves (Continued)

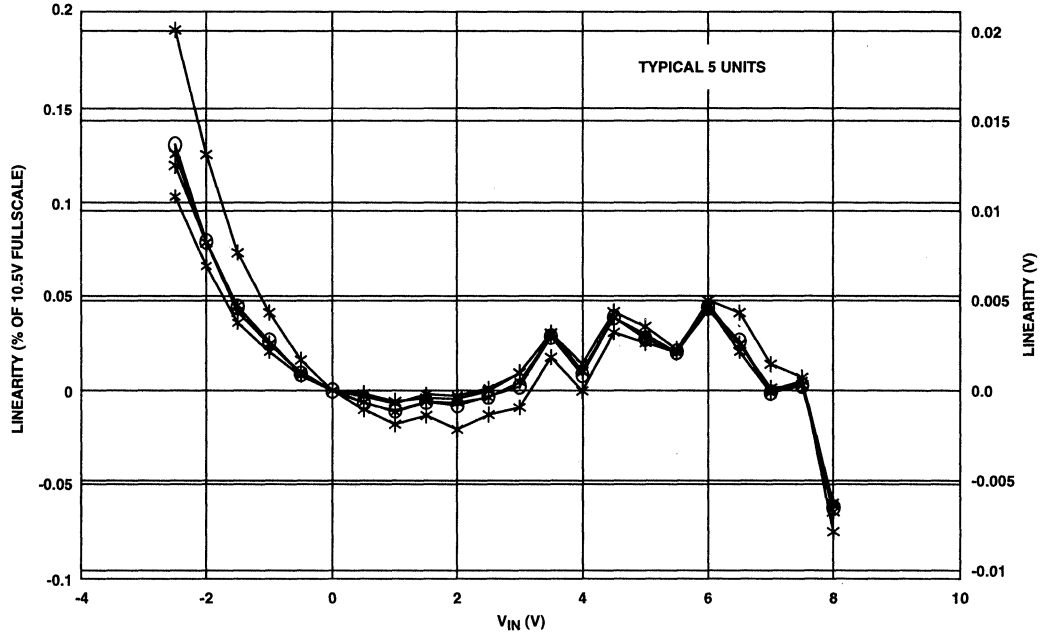


FIGURE 9. V_{HIGH} LINEARITY ERROR 10.5V FULLSCALE

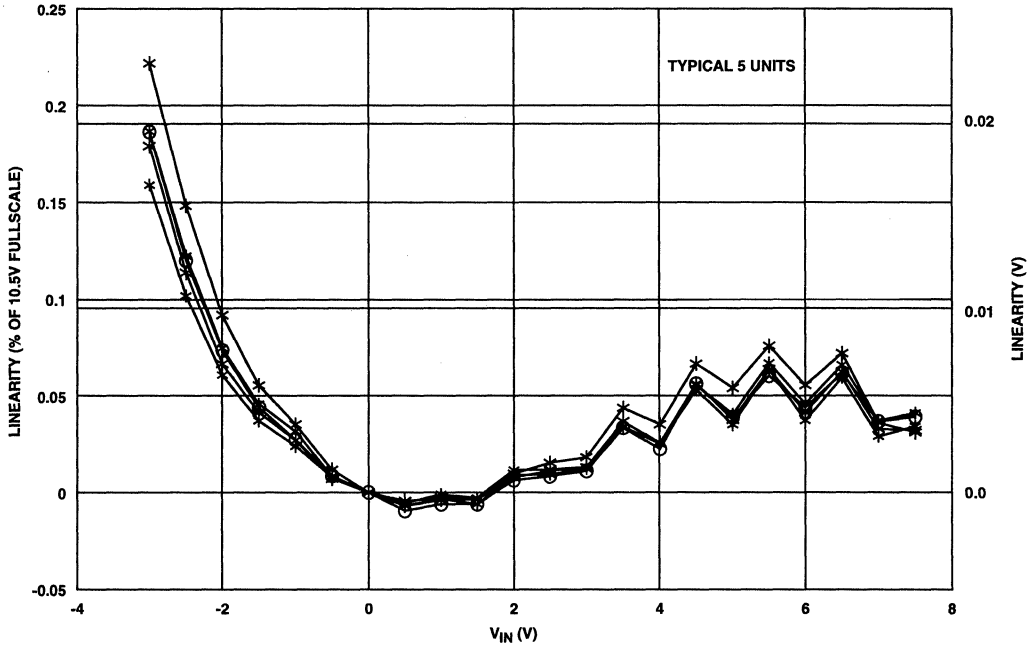


FIGURE 10. V_{LOW} LINEARITY ERROR 10.5V FULLSCALE

Typical Performance Curves (Continued)

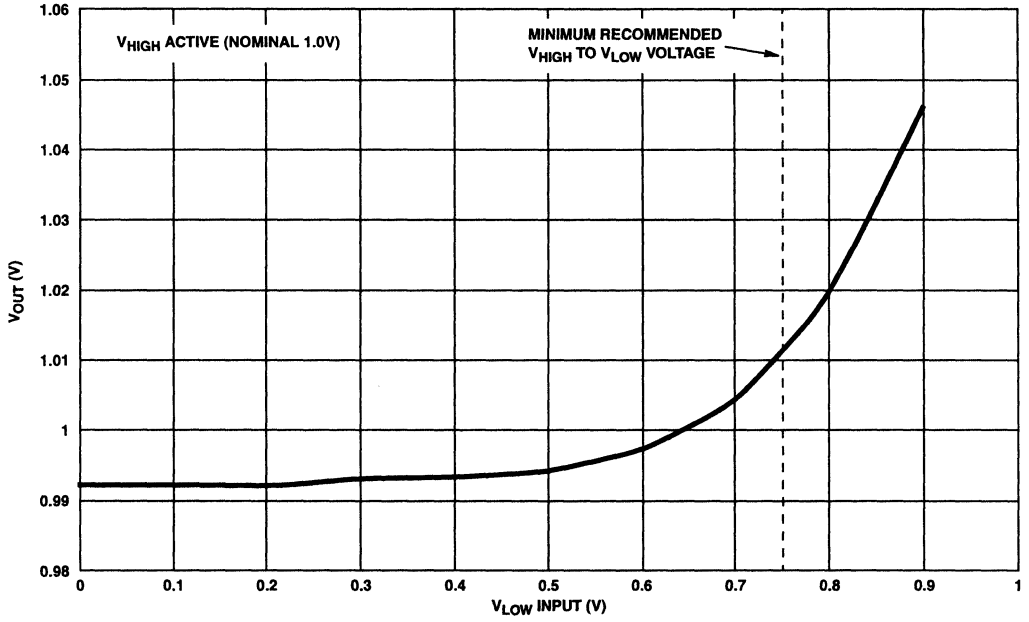


FIGURE 11. V_{HIGH}/V_{LOW} INTERACTION

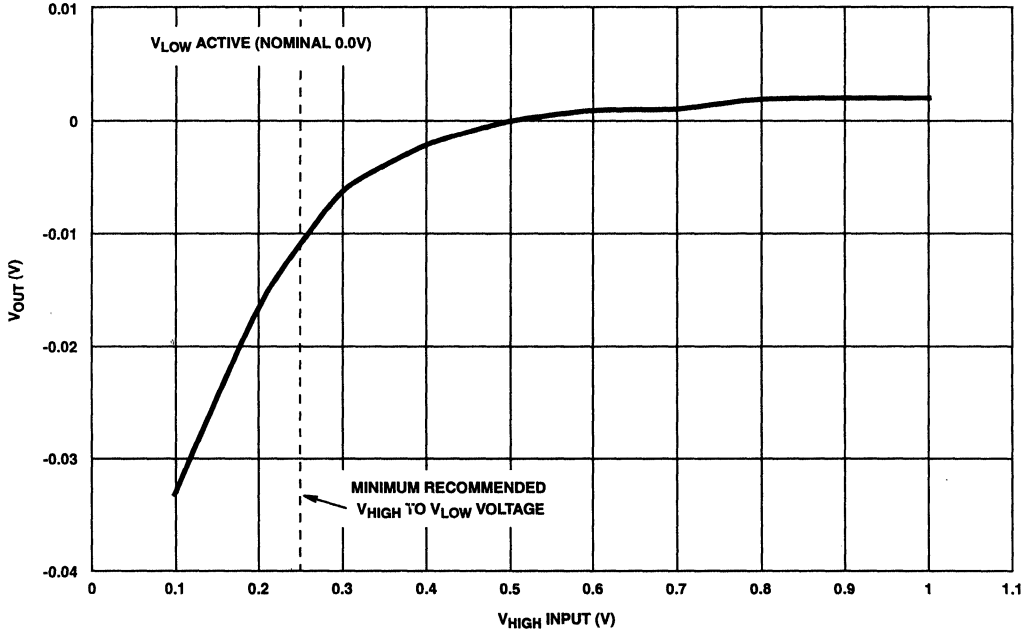


FIGURE 12. V_{HIGH}/V_{LOW} INTERACTION

Typical Performance Curves (Continued)

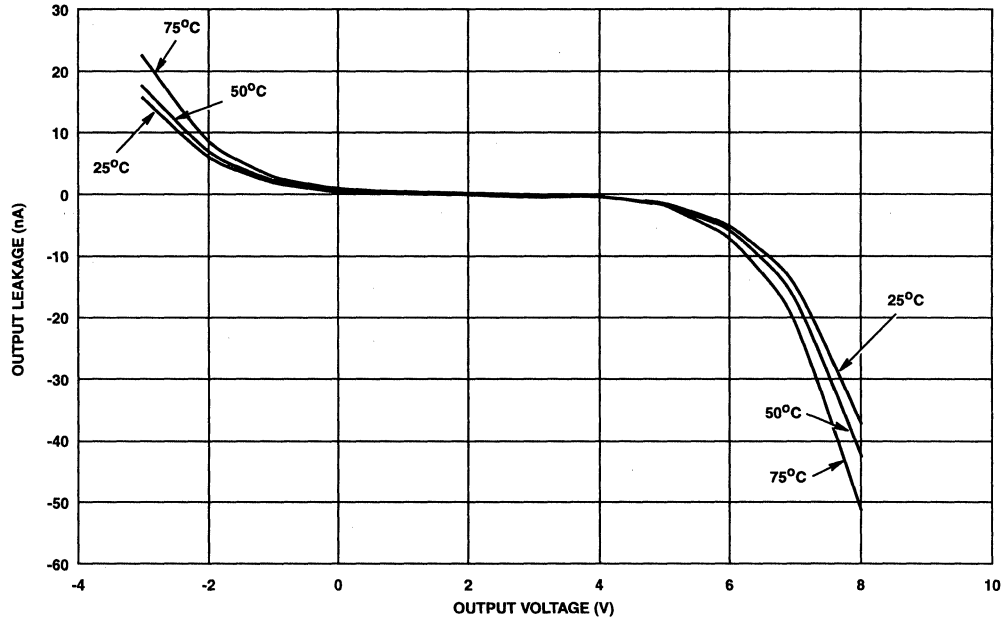


FIGURE 13. HIZ OUTPUT LEAKAGE

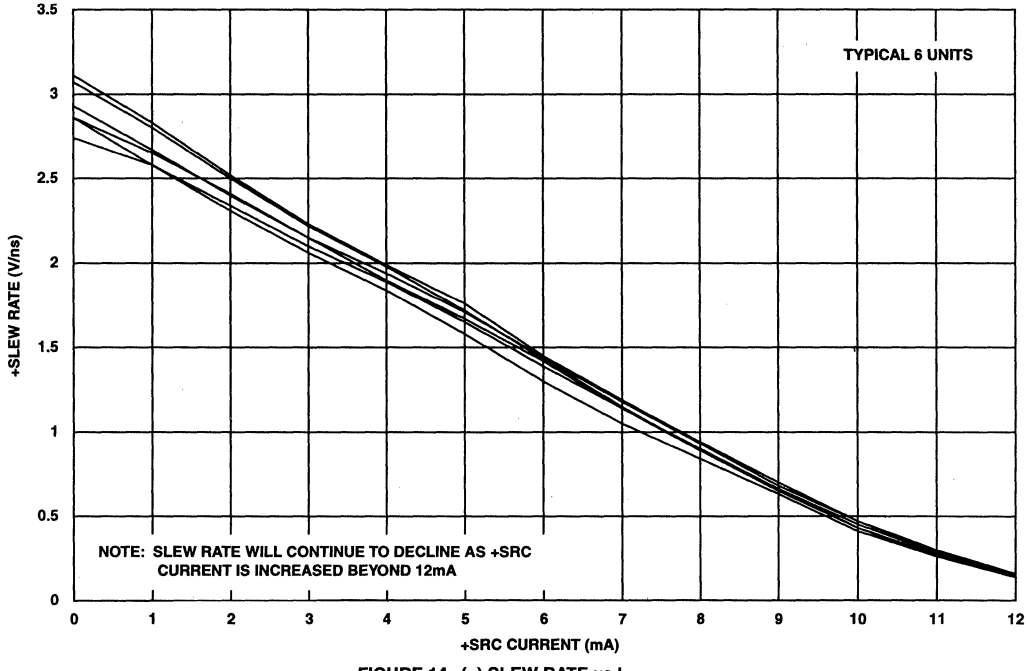


FIGURE 14. (+) SLEW RATE vs I_{STEAL}

Typical Performance Curves (Continued)

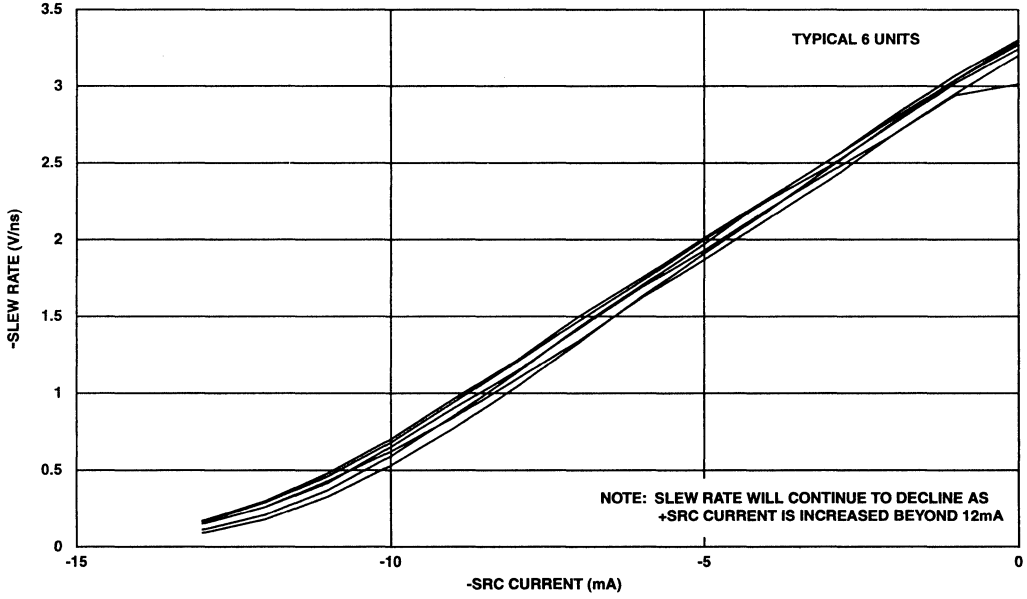
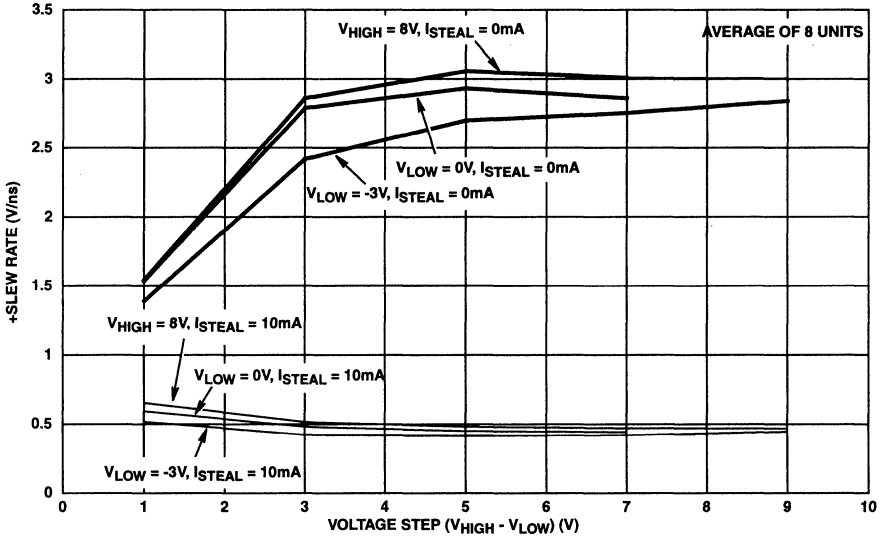


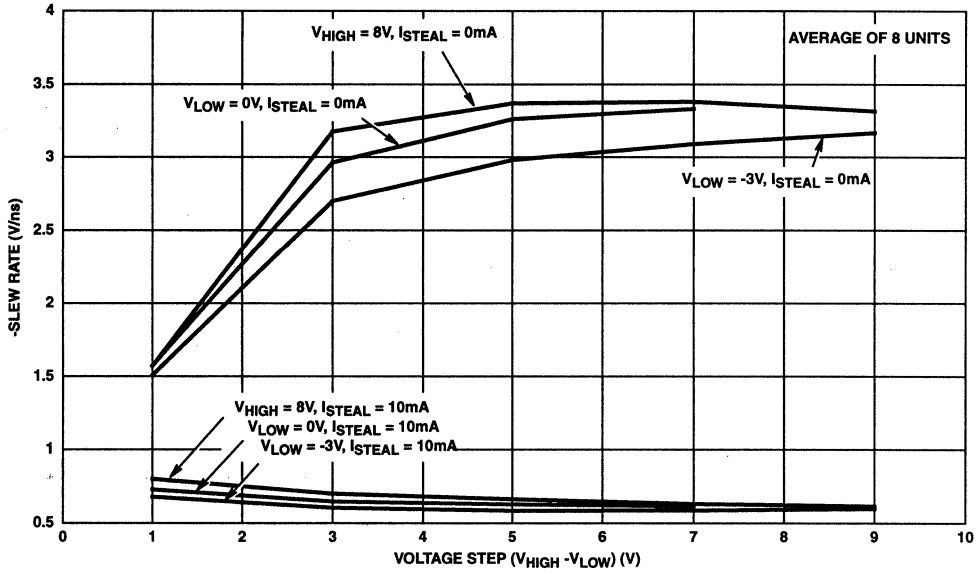
FIGURE 15. (-) SLEW RATE vs I_{STEAL}



NOTE: The family of curves shows slew rate as a function of common mode voltage. A voltage is provided for each trace specifying one level of the voltage step for which slew rate is measured. Example 1: Top Trace (V_{HIGH} = 8V, I_{STEAL} = 0mA). A voltage step of 1V goes from V_{LOW} = 7V to V_{HIGH} = 8V and a voltage step of 9V goes from V_{LOW} = -1V to V_{HIGH} = 8V. Example 2: Trace (V_{LOW} = -3V, I_{STEAL} = 0mA). A voltage step of 1V goes from V_{LOW} = -3V to V_{HIGH} = -2V and a voltage step of 9V goes from V_{LOW} = -3V to V_{HIGH} = 6V.

FIGURE 16. (+) SLEW RATE vs AMPLITUDE

Typical Performance Curves (Continued)



NOTE: The family of curves shows slew rate as a function of common mode voltage. A voltage is provided for each trace specifying one level of the voltage step for which slew rate is measured. Example 1: Top Trace (V_{HIGH} = 8V, I_{STEAL} = 0mA). A voltage step of 1V goes from V_{HIGH} = 8V to V_{LOW} = 7V and a voltage step of 9V goes from V_{HIGH} = 8V to V_{LOW} = -1V. Example 2: Trace (V_{LOW} = -3V, I_{STEAL} = 0mA). A voltage step of 1V goes from V_{HIGH} = -2V to V_{LOW} = -3V and a voltage step of 9V goes from V_{HIGH} = 6V to V_{LOW} = -3V.

FIGURE 17. (-) SLEW RATE vs AMPLITUDE

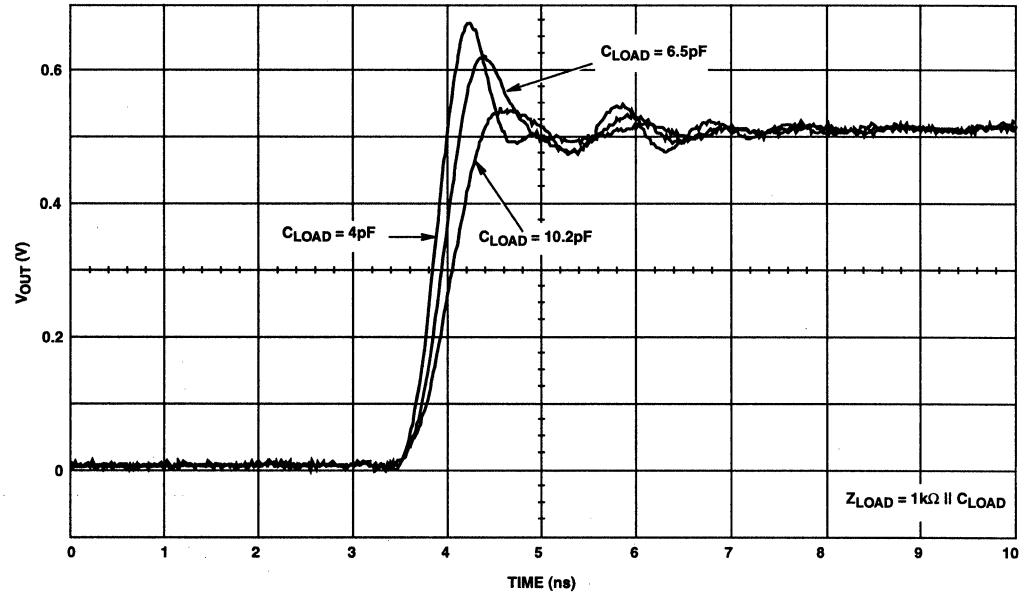


FIGURE 18. 0.5V STEP RESPONSE vs C_{LOAD}

Typical Performance Curves (Continued)

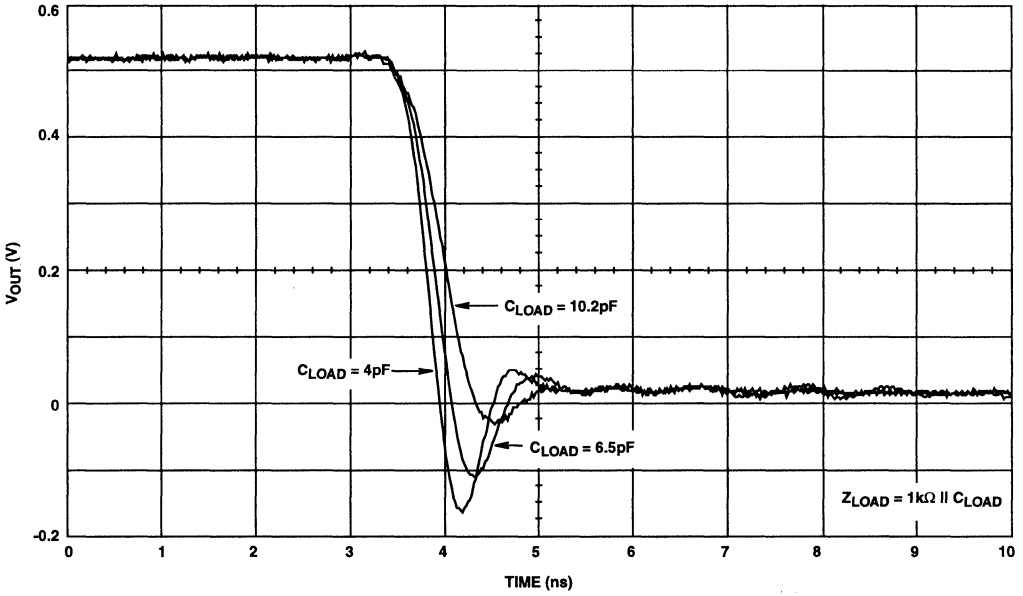


FIGURE 19. 0.5V STEP RESPONSE vs C_{LOAD}

Die Characteristics

DIE DIMENSIONS:

2670µm x 1730µm x 525µm

METALLIZATION:

Type: Metal 1: Cu (2%) SiAl/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Backside: Gold

Type: Metal 2: Cu (2%) Al
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Nitride, 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

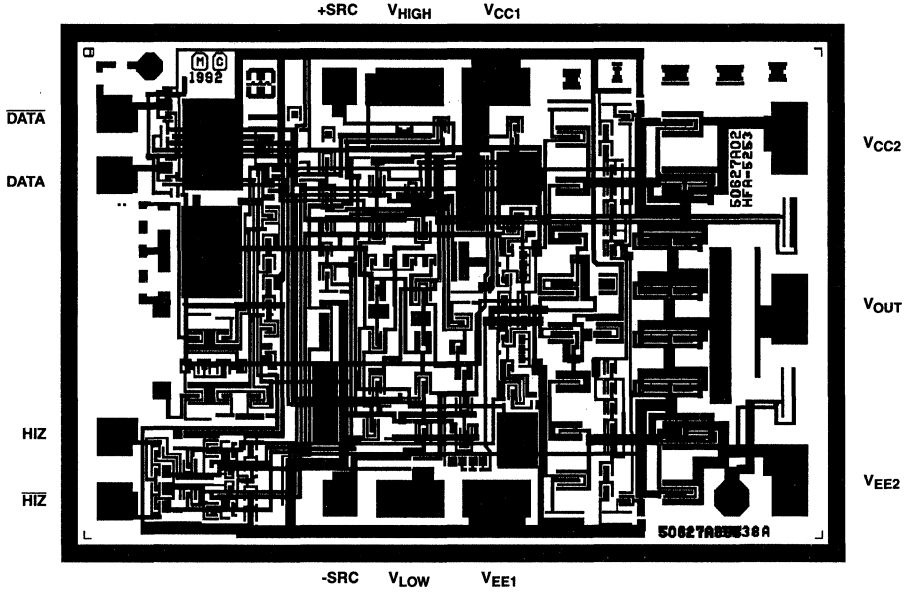
113

SUBSTRATE POTENTIAL:

Floating

Metallization Mask Layout

HFA5253



HARRIS SEMICONDUCTOR

ICL8013

November 1996

1MHz, Four Quadrant Analog Multiplier

Features

- **Accuracy** . . . . . **±0.5% ("A" Version)**
- **Input Voltage Range** . . . . . **±10V**
- **Bandwidth** **1MHz**
- **Uses Standard ±15V Supplies**
- **Built-In Op Amp Provides Level Shifting, Division and Square Root Functions**

Description

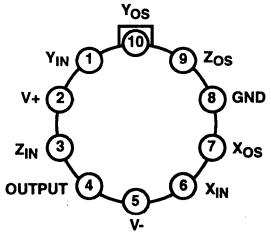
The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 make it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and voltage controlled amplifiers.

Ordering Information

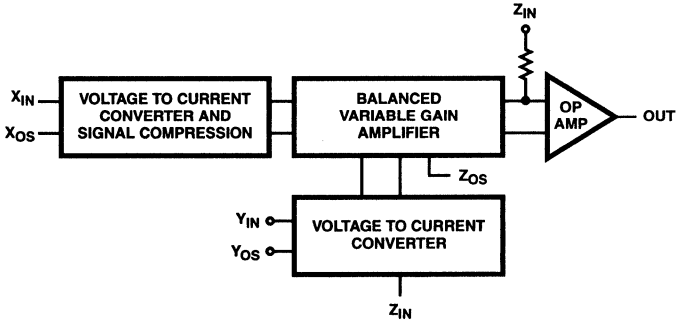
PART NUMBER	MULTIPLICATION ERROR	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL8013AMTX	±0.5% } Max	-55 to 125	10 Pin Metal Can	T10.B
ICL8013BMTX	±1% } Max	-55 to 125	10 Pin Metal Can	T10.B
ICL8013ACTX	±0.5% } Max	0 to 70	10 Pin Metal Can	T10.B
ICL8013BCTX	±1% } Max	0 to 70	10 Pin Metal Can	T10.B
ICL8013CCTX	±2% } Max	0 to 70	10 Pin Metal Can	T10.B

Pinout

ICL8013
(METAL CAN)
TOP VIEW



Functional Diagram



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2863.2**

Absolute Maximum Ratings

Supply Voltage ..... ±18
Input Voltages (X_{IN}, Y_{IN}, Z_{IN}, X_{OS}, Y_{OS}, Z_{OS}) ..... V_{SUPPLY}

Operating Conditions

Temperature Range
ICL8013XC ..... 0°C to 70°C
ICL8013XM ..... -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	160	75

Maximum Junction Temperature (Metal Can Package) ..... 175°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

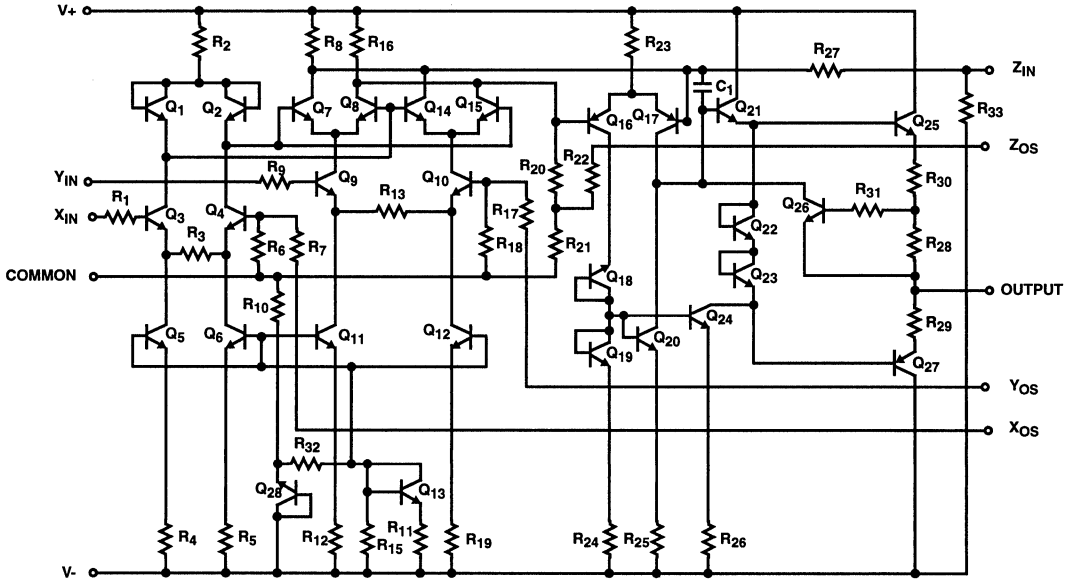
$T_A = 25°C$, $V_{SUPPLY} = \pm 15V$, Gain and Offset Potentiometers Externally Trimmed, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Multiplier Function		-	$\frac{XY}{10}$	-	-	$\frac{XY}{10}$	-	-	$\frac{XY}{10}$	-	
Multiplication Error	-10 < X < 10 -10 < Y < 10	-	-	0.5	-	-	1.0	-	-	2.0	% Full Scale
Divider Function		-	$\frac{10Z}{X}$	-	-	$\frac{10Z}{X}$	-	-	$\frac{10Z}{X}$	-	
Division Error	X = -10	-	0.3	-	-	0.3	-	-	0.3	-	% Full Scale
	X = -1	-	1.5	-	-	1.5	-	-	1.5	-	% Full Scale
Feedthrough	X = 0, Y = ±10V	-	-	50	-	-	100	-	-	200	mV
	Y = 0, X = ±10V	-	-	50	-	-	100	-	-	150	mV
Non-Linearity		-	-	-	-		-	-		-	
X Input	$X = 20V_{P-P}$ $Y = \pm 10V_{DC}$		±0.5			±0.5			±0.8		%
Y Input	$Y = 20V_{P-P}$ $X = \pm 10V_{DC}$	-	±0.2	-	-	±0.2	-	-	±0.3	-	%
Frequency Response Small Signal Bandwidth (-3dB)		-	1.0	-	-	1.0	-	-	1.0	-	MHz
Full Power Bandwidth		-	750	-	-	750	-	-	750	-	kHz
Slew Rate		-	45	-	-	45	-	-	45	-	V/µs
1% Amplitude Error		-	75	-	-	75	-	-	75	-	kHz
1% Vector Error (0.5° Phase Shift)		-	5	-	-	5	-	-	5	-	kHz
Settling Time (to ±2% of Final Value)	$V_{IN} = \pm 10V$	-	1	-	-	1	-	-	1	-	µs
Overload Recovery (to ±2% of Final Value)	$V_{IN} = \pm 10V$	-	1	-	-	1	-	-	1	-	µs
Output Noise	5Hz to 10kHz	-	0.6	-	-	0.6	-	-	0.6	-	mV_{RMS}
	5Hz to 5MHz	-	3	-	-	3	-	-	3	-	mV_{RMS}
Input Resistance		-		-	-		-	-		-	
X Input	$V_{IN} = 0V$	-	10			10			10		MΩ
Y Input		-	6	-	-	6	-	-	6	-	MΩ
Z Input		-	36	-	-	36	-	-	36	-	kΩ
Input Bias Current		-	-	-	-	-		-	-		
X or Y Input	$V_{IN} = 0V$	-	2	5			7.5			10	µA
Z Input		-	25	-	-	25	-	-	25	-	µA

Electrical Specifications $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, Gain and Offset Potentiometers Externally Trimmed, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Variation		-		-	-		-	-	-	-	
Multiplication Error		-	0.2			0.2			0.2		%/%
Output Offset		-	-	50	-	-	75	-	-	100	mV/V
Scale Factor		-	0.1	-	-	0.1	-	-	0.1	-	%/%
Quiescent Current		-	3.5	6.0	-	3.5	6.0	-	3.5	6.0	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES											
Multiplication Error	$-10V < X_{IN} < 10V$, $-10V < Y_{IN} < 10V$	-	1.5	-	-	2	-	-	3	-	% Full Scale
Average Temp. Coefficients		-		-	-		-	-		-	
Accuracy			0.06			0.06			0.06		%/°C
Output Offset		-	0.2	-	-	0.2	-	-	0.2	-	mV/°C
Scale Factor		-	0.04	-	-	0.04	-	-	0.04	-	%/°C
Input Bias Current		-	-		-	-		-	-		
X or Y Input	$V_{IN} = 0V$			5			5			10	µA
Z Input		-	-	25	-	-	25	-	-	35	µA
Input Voltage (X, Y, or Z)		-	-	±10	-	-	±10	-	-	±10	V
Output Voltage Swing	$R_L \geq 2k\Omega$ $C_L < 1000pF$	-	±10	-	-	±10	-	-	±10	-	V

Schematic Diagram



8 SPECIAL ANALOG CIRCUITS

Application Information

Detailed Circuit Description

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 1.

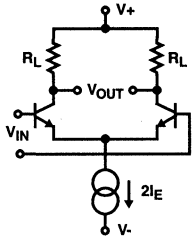


FIGURE 1. DIFFERENTIAL AMPLIFIER

The small signal differential voltage gain of this circuit is given by:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_E}$$

Substituting $r_E = \frac{1}{g_M} = \frac{kT}{qI_E}$

$$V_{OUT} = V_{IN}\left(\frac{R_L}{r_E}\right) = V_{IN} \times \frac{qI_E R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E. In the simple transconductance multiplier of Figure 2, a current source comprising Q_3, D_1, and R_Y is used. If V_Y is large compared with the drop across D_1, then

$$I_D \approx \frac{V_Y}{R_Y} = 2I_E \text{ and}$$

$$V_{OUT} = \frac{qR_L}{kTR_Y}(V_X \times V_Y)$$

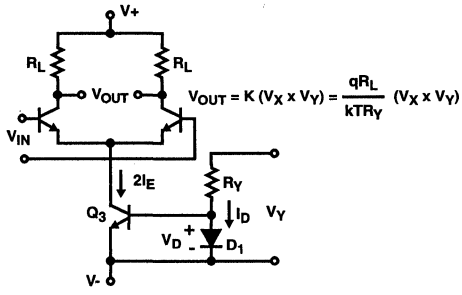


FIGURE 2. TRANSCONDUCTANCE MULTIPLIER

There are several difficulties with this simple modulator:

1. V_Y must be positive and greater than V_D.
2. Some portion of the signal at V_X will appear at the output unless $I_E = 0$.
3. V_X must be a small signal for the differential pair to be linear.
4. The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 3, uses another differential pair but with considerable emitter degeneration. In this circuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0V to ±10V with excellent linearity.

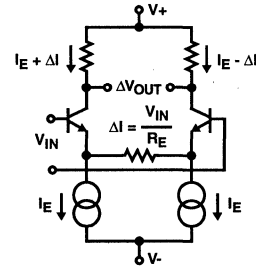


FIGURE 3. VOLTAGE TO CURRENT CONVERTER

The second problem is called feedthrough; i.e., the product of zero and some finite Input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 4A, 4B, and 4C overcomes this problem and forms the heart of many multiplier circuits in use today.

This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in Figure 4A of exactly equal current sources basing the two pairs. With a small positive signal at V_{IN}, the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.

In Figure 4B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 4C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2} the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4. Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 3 we have a balanced multiplier circuit capable of four quadrant operation (Figure 5).

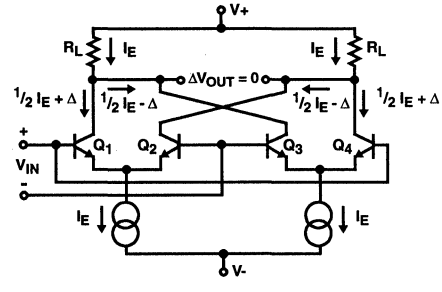


FIGURE 4A. INPUT SIGNAL WITH BALANCED CURRENT SOURCES $\Delta V_{OUT} = 0V$

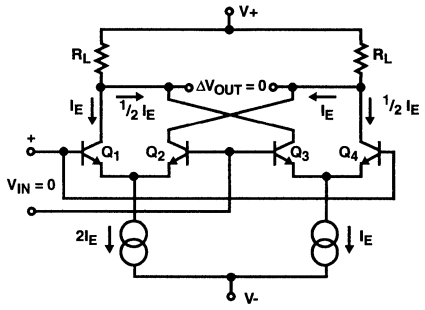


FIGURE 4B. NO INPUT SIGNAL WITH UNBALANCED CURRENT SOURCES $\Delta V_{OUT} = 0V$

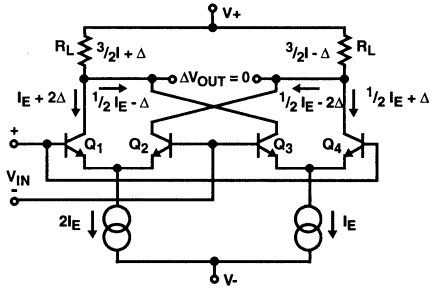


FIGURE 4C. INPUT SIGNAL WITH UNBALANCED CURRENT SOURCES, DIFFERENTIAL OUTPUT VOLTAGE

This circuit of Figure 5 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.

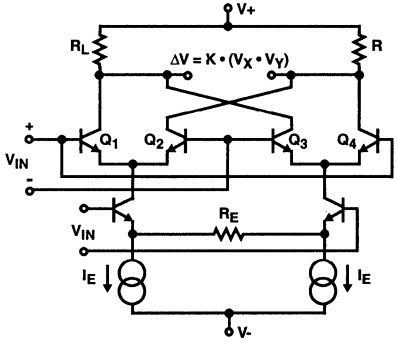


FIGURE 5. TYPICAL FOUR QUADRANT MULTIPLIER-MODULATOR

Figure 2 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Figure 6A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 6A is the difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Figure 3, we have Figure 6B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown after the Electrical Specifications Table. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2. These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15}. The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10}. Transistors Q_5, Q_6, Q_{11}, and Q_{12} are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors Q_{16} through Q_{27}.

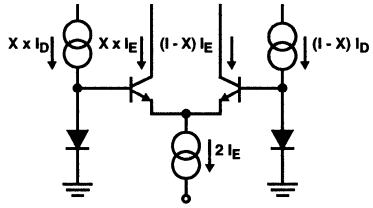


FIGURE 6A. CURRENT GAIN CELL

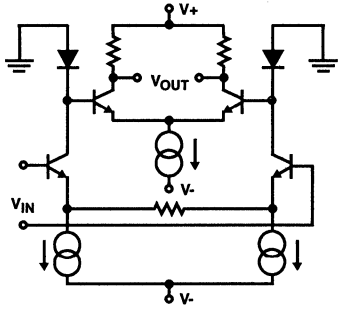


FIGURE 6B. VOLTAGE GAIN WITH SIGNAL COMPRESSION

Definition of Terms

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and

the other swept through it nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

Typical Applications

Multiplication

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R_{27} and produces a proportional output voltage.

Multiplier Trimming Procedure

1. Set $X_{IN} = Y_{IN} = 0V$ and adjust Z_{OS} for zero Output.
2. Apply a ±10V low frequency (≤100Hz) sweep (sine or triangle) to Y_{IN} with $X_{IN} = 0V$, and adjust X_{OS} for minimum output.
3. Apply the sweep signal of Step 2 to X_{IN} with $Y_{IN} = 0V$ and adjust Y_{OS} for minimum Output.
4. Readjust Z_{OS} as in Step 1, if necessary.
5. With $X_{IN} = 10.0V_{DC}$ and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A+B) by inverting one signal and adjusting Gain control for (Output - Y_{IN}) = Zero.

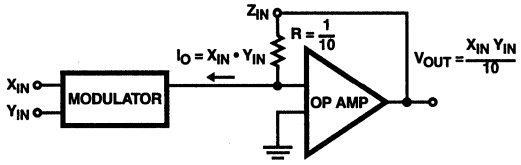


FIGURE 7A. MULTIPLIER BLOCK DIAGRAM

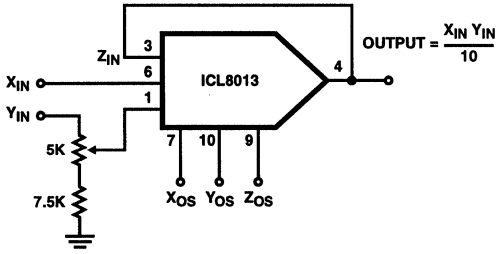


FIGURE 7B. MULTIPLIER CIRCUIT CONNECTION

Division

If the Z terminal is used as an input, and the output of the op amp connected to the Y input, the device functions as a divider. Since the input to the op amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

Therefore $I_O = X_{IN} \bullet Y_{IN} = \frac{Z_{IN}}{R} = 10Z_{IN}$

Since $Y_{IN} = V_{OUT}$, $V_{OUT} = \frac{10Z_{IN}}{X_{IN}}$

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.

Divider Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for 0V.
2. With $Z_{IN} = 0V$, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from -10V through -1V.
3. With $Z_{IN} = 0V$ and $X_{IN} = -10.0V$ adjust Y_{OS} for zero Output voltage.
4. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust X_{OS} for minimum worst case variation of Output, as X_{IN} is varied from -10V to -1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust the gain control until the output is the closest average around +10.0V (-10V for $Z_{IN} = -X_{IN}$) as X_{IN} is varied from -10V to -3V.

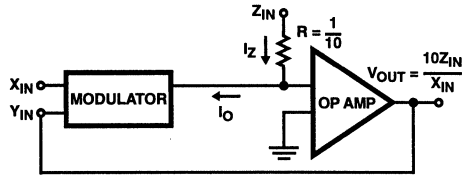


FIGURE 8A. DIVISION BLOCK DIAGRAM

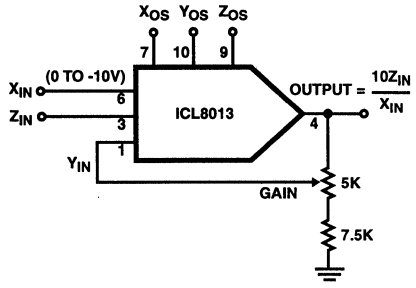


FIGURE 8B. DIVISION CIRCUIT CONNECTION

Squaring

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2\omega t = {}^1/_2 (\cos 2\omega t + 1)$.

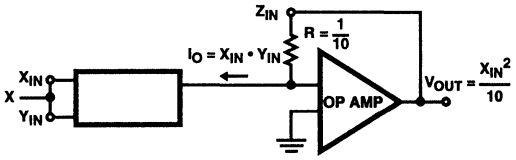


FIGURE 9A. SQUARER BLOCK DIAGRAM

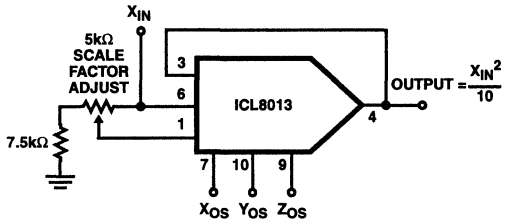


FIGURE 9B. SQUARER CIRCUIT CONNECTION

Square Root

Tying the X and Y inputs together and using overall feedback from the op amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X_{IN} \times Y_{IN} = (-V_{OUT})^2 = 10Z_{IN}$$

$$V_{OUT} = -\sqrt{10Z_{IN}}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the op amp output prevents the latchup that would otherwise occur for negative input voltages.

Square Root Trimming Procedure

1. Connect the ICL8013 in the Divider configuration.
2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the output and inserting a diode between Pin 4 and the output node.
4. With Z_{IN} = 0V adjust Z_{OS} for zero output voltage.

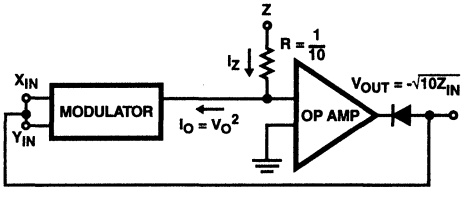


FIGURE 10A. SQUARE ROOT BLOCK DIAGRAM

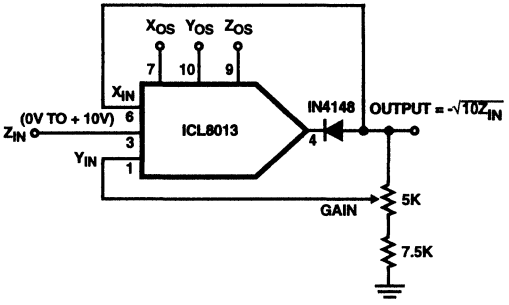


FIGURE 10B. ACTUAL CIRCUIT CONNECTION

Variable Gain Amplifier

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.

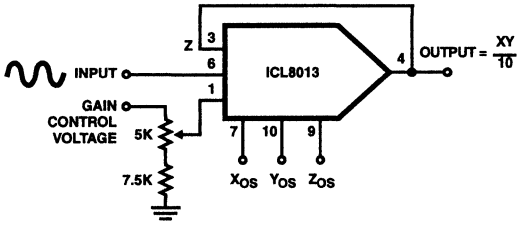


FIGURE 11. VARIABLE GAIN AMPLIFIER

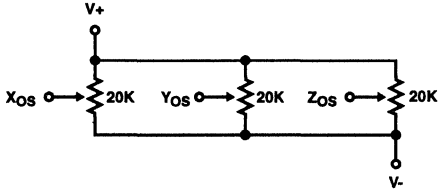


FIGURE 12. POTENTIOMETERS FOR TRIMMING OFFSET AND FEEDTHROUGH

Typical Performance Curves

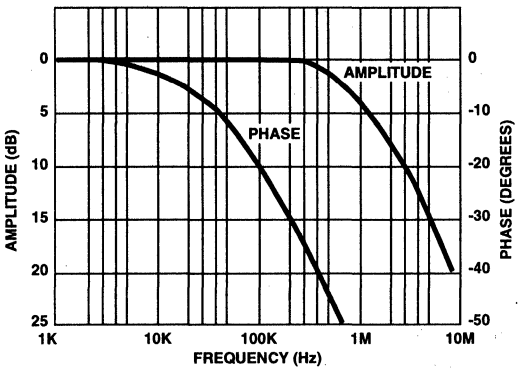


FIGURE 13. FREQUENCY RESPONSE

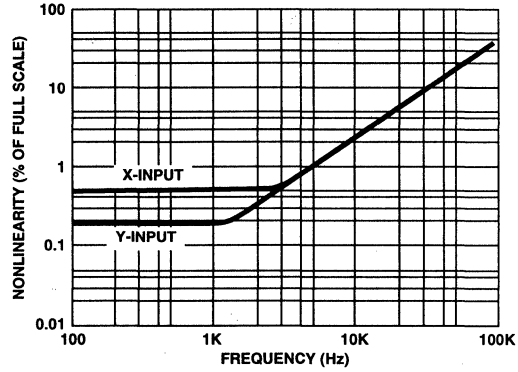


FIGURE 14. NONLINEARITY vs FREQUENCY

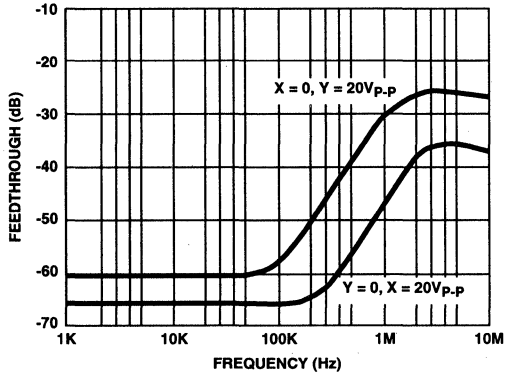


FIGURE 15. FEEDTHROUGH vs FREQUENCY

HARRIS SEMICONDUCTOR

ICL8038

Precision Waveform Generator/ Voltage Controlled Oscillator

November 1996

Features

- Low Frequency Drift with Temperature . . . 250ppm/°C
- Low Distortion . . . . . 1% (Sine Wave Output)
- High Linearity . . . . . 0.1% (Triangle Wave Output)
- Wide Frequency Range . . . . . 0.001Hz to 300kHz
- Variable Duty Cycle . . . . . 2% to 98%
- High Level Outputs . . . . . TTL to 28V
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Easy to Use - Just a Handful of External Components Required

Description

The ICL8038 waveform generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from 0.001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

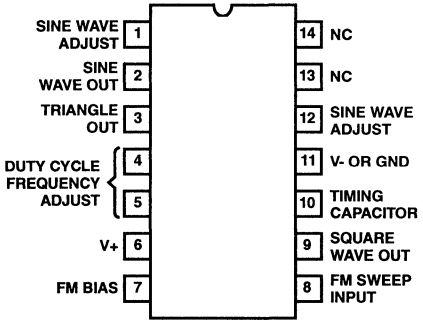
Ordering Information

PART NUMBER	STABILITY	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL8038CCPD	250ppm/°C (Typ)	0 to 70	14 Ld PDIP	E14.3
ICL8038CCJD	250ppm/°C (Typ)	0 to 70	14 Ld CERDIP	F14.3
ICL8038BCJD	180ppm/°C (Typ)	0 to 70	14 Ld CERDIP	F14.3
ICL8038ACJD	120ppm/°C (Typ)	0 to 70	14 Ld CERDIP	F14.3
ICL8038BMJD (Note)	350ppm/°C (Max)	-55 to 125	14 Ld CERDIP	F14.3
ICL8038AMJD (Note)	250ppm/°C (Max)	-55 to 125	14 Ld CERDIP	F14.3

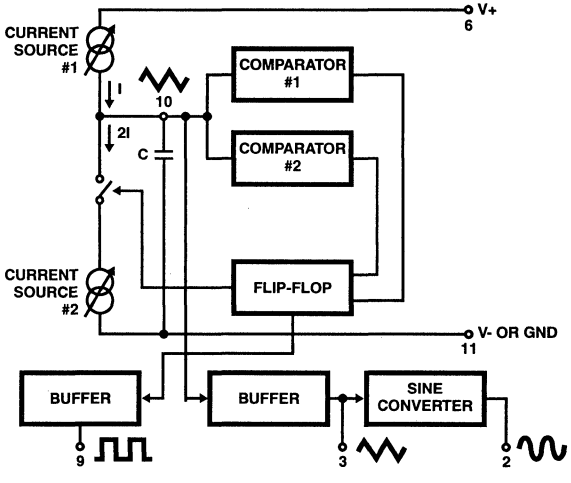
NOTE: Add /883B to part number if 883 processing is required.

Pinout

ICL8038
(PDIP, CERDIP)
TOP VIEW



Functional Diagram



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number 2864.2

Absolute Maximum Ratings

Supply Voltage (V- to V+) 36V
Input Voltage (Any Pin) . . . . . V- to V+
Input Current (Pins 4 and 5) 25mA
Output Sink Current (Pins 3 and 9) 25mA

Operating Conditions

Temperature Range
ICL8038AM, ICL8038BM . . . . . -55°C to 125°C
ICL8038AC, ICL8038BC, ICL8038CC . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
PDIP Package	115	N/A

Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8038CC			ICL8038BC(BM)			ICL8038AC(AM)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Operating Range	V_{SUPPLY}											
	V+	Single Supply	+10	-	+30	+10	-	+30	+10	-	+30	V
	V+, V-	Dual Supplies	±5	-	±15	±5	-	±15	±5	-	±5	V
Supply Current	I_{SUPPLY}	V_{SUPPLY} = ±10V (Note 2)										
8038AM 8038BM			-	-		-	12	15	-	12	15	mA
8038AC, 8038BC, 8038CC				12	20	-	12	20	-	12	20	mA
FREQUENCY CHARACTERISTICS (All Waveforms)												
Max. Frequency of Oscillation	f_{MAX}		100	-	-	100	-	-	100	-	-	kHz
Sweep Frequency of FM Input	f_{SWEEP}		-	10	-	-	10	-	-	10	-	kHz
Sweep FM Range		(Note 3)	-	35:1	-	-	35:1	-	-	35:1	-	
FM Linearity		10:1 Ratio	-	0.5	-	-	0.2	-	-	0.2	-	%
Frequency Drift with Temperature (Note 5)	$\Delta f/\Delta T$											
8038AC, 8038BC, 8038CC		0°C to 70°C	-	250	-	-	180	-	-	120		ppm/°C
8038AM, 8038BM		-55°C to 125°C	-		-	-	-	350	-	-	250	ppm/°C
Frequency Drift with Supply Voltage	$\Delta f/\Delta V$	Over Supply Voltage Range	-	0.05	-	-	0.05		-	0.05	-	%/V
OUTPUT CHARACTERISTICS												
Square Wave Leakage Current	I_{OLK}	V_9 = 30V	-	-	1	-	-	1	-	-	1	µA
Saturation Voltage	V_{SAT}	I_{SINK} = 2mA	-	0.2	0.5	-	0.2	0.4	-	0.2	0.4	V
Rise Time	t_R	R_L = 4.7kΩ	-	180	-	-	180	-	-	180	-	ns
Fall Time	t_F	R_L = 4.7kΩ	-	40	-	-	40	-	-	40	-	ns
Typical Duty Cycle Adjust (Note 6)	ΔD		2		98	2	-	98	2	-	98	%
Triangle/Sawtooth/Ramp Amplitude	$V_{TRIANGLE}$	R_{TRI} = 100kΩ	0.30	0.33	-	0.30	0.33	-	0.30	0.33	-	xV$_{SUPPLY}$
Linearity			-	0.1	-	-	0.05	-	-	0.05	-	%
Output Impedance	Z_{OUT}	I_{OUT} = 5mA	-	200	-	-	200	-	-	200	-	Ω

Electrical Specifications V_{SUPPLY} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8038CC			ICL8038BC(BM)			ICL8038AC(AM)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Impedance	Z_{OUT}	I_{OUT} = 5mA	-	200	-	-	200	-	-	200	-	Ω
Sine Wave Amplitude	V_{SINE}	R_{SINE} = 100kΩ	0.2	0.22	-	0.2	0.22	-	0.2	0.22	-	xV_{SUPPLY}
THD	THD	R_S = 1MΩ (Note 4)	-	2.0	5	-	1.5	3	-	1.0	1.5	%
THD Adjusted	THD	Use Figure 4	-	1.5	-	-	1.0	-	-	0.8	-	%

NOTES:

2. R_A and R_B currents not included.
3. V_{SUPPLY} = 20V; R_A and R_B = 10kΩ, f ≅ 10kHz nominal; can be extended 1000 to 1. See Figures 5A and 5B.
4. 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B.)
5. Figure 1, pins 7 and 8 connected, V_{SUPPLY} = ±10V. See Typical Curves for T.C. vs V_{SUPPLY}.
6. Not tested, typical value for design purposes only.

Test Conditions

PARAMETER	R_A	R_B	R_L	C	SW_1	MEASURE
Supply Current	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current Into Pin 6
Sweep FM Range (Note 7)	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 3
Frequency Drift with Supply Voltage (Note 8)	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude (Note 10) Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk Output at Pin 2
Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk Output at Pin 3
Leakage Current (Off) (Note 9)	10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (On) (Note 9)	10kΩ	10kΩ		3.3nF	Closed	Output (Low) at Pin 9
Rise and Fall Times (Note 11)	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust (Note 11) Max	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Min	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTES:

7. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{HI}) and then connecting pin 8 to pin 6 (f_{LO}). Otherwise apply Sweep Voltage at pin 8 ($^2/_3$ V_{SUPPLY} +2V) ≤ V_{SWEEP} ≤ V_{SUPPLY} where V_{SUPPLY} is the total supply voltage. In Figure 5B, pin 8 should vary between 5.3V and 10V with respect to ground.
8. 10V ≤ V+ ≤ 30V, or ±5V ≤ V_{SUPPLY} ≤ ±15V.
9. Oscillation can be halted by forcing pin 10 to +5V or -5V.
10. Output Amplitude is tested under static conditions by forcing pin 10 to 5V then to -5V.
11. Not tested; for design purposes only.

Test Circuit

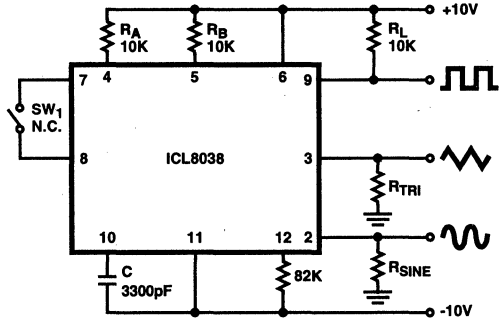
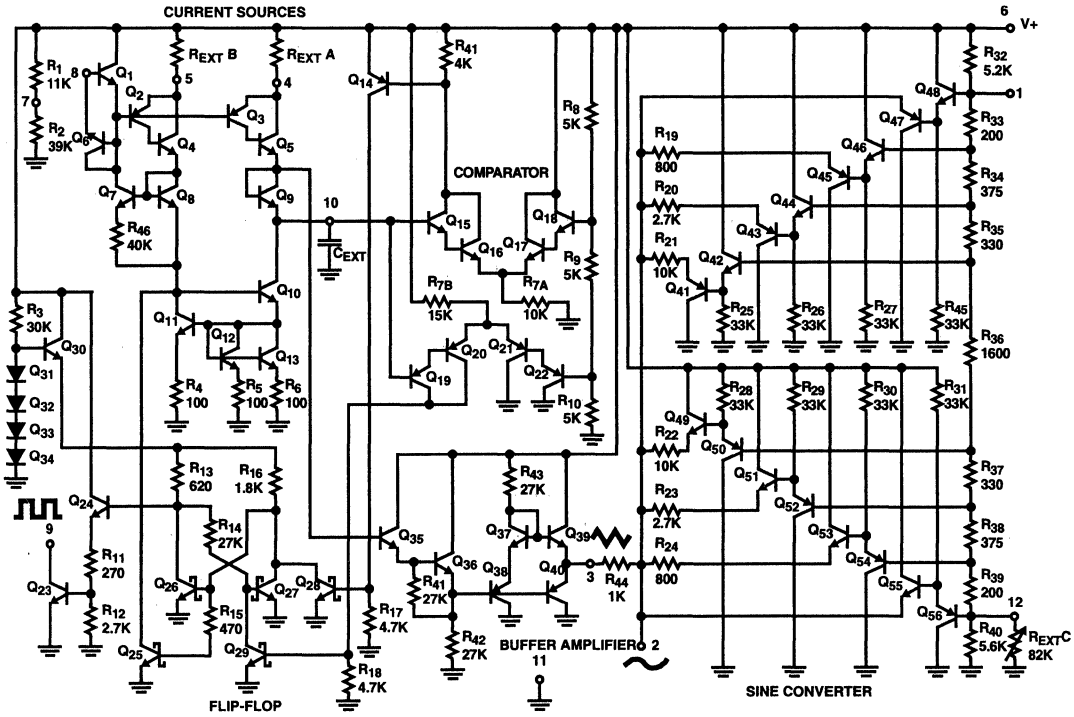


FIGURE 1. TEST CIRCUIT

Detailed Schematic



Application Information (See Functional Diagram)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearly with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at Terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at Terminal 9.

The sine wave is created by feeding the triangle wave into a nonlinear network (sine converter). This network provides a decreasing shunt impedance as the potential of the triangle moves toward the two extremes.

Waveform Timing

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 3. Best results are obtained by keeping the timing resistors R_A and R_B separate (A). R_A controls the rising portion of the triangle and sine wave and the 1 state of the square wave.

The magnitude of the triangle waveform is set at $^1/_3$ V_{SUPPLY}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V_{SUPPLY} \times R_A}{0.22 \times V_{SUPPLY}} = \frac{R_A \times C}{0.66}$$

The falling portion of the triangle and sine wave and the 0 state of the square wave is:

$$t_2 = \frac{C \times V}{1} = \frac{C \times 1/3 V_{SUPPLY}}{2(0.22)\frac{V_{SUPPLY}}{R_B} - 0.22\frac{V_{SUPPLY}}{R_A}} = \frac{R_A R_B C}{0.66(2R_A - R_B)}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty cycle is to be varied over a small range about 50% only, the connection shown in Figure 3B is slightly more convenient. A 1kΩ potentiometer may not allow the duty cycle to be adjusted through 50% on all devices. If a 50% duty cycle is required, a 2kΩ or 5kΩ potentiometer should be used.

With two separate timing resistors, the frequency is given by:

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{R_A C}{0.66}\left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.33}{RC} \text{ (for Figure 3A)}$$

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents and thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

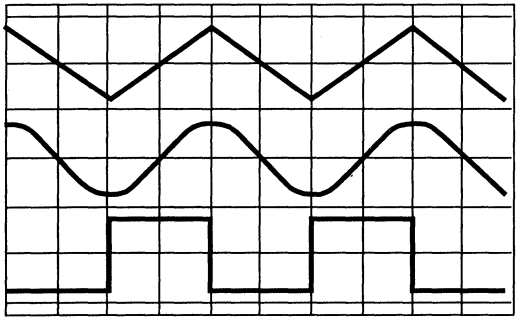


FIGURE 2A. SQUARE WAVE DUTY CYCLE - 50%

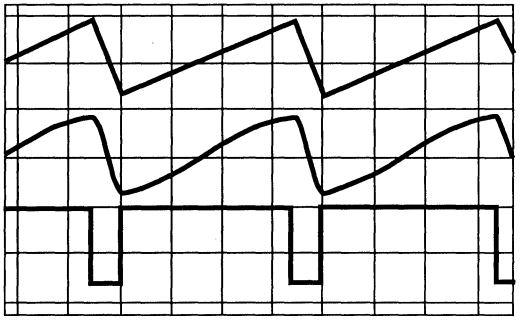


FIGURE 2B. SQUARE WAVE DUTY CYCLE - 80%

FIGURE 2. PHASE RELATIONSHIP OF WAVEFORMS

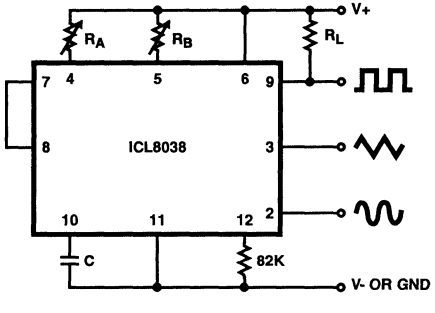


FIGURE 3A.

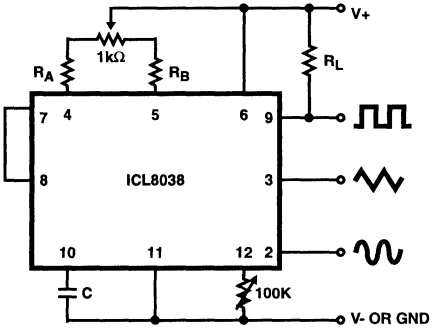


FIGURE 3B.

FIGURE 3. POSSIBLE CONNECTIONS FOR THE EXTERNAL TIMING RESISTORS

Reducing Distortion

To minimize sine wave distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 4; this configuration allows a typical reduction of sine wave distortion close to 0.5%.

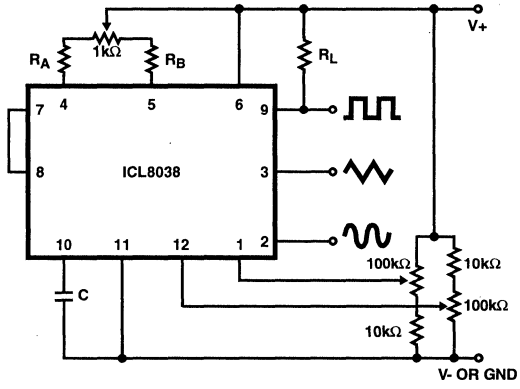


FIGURE 4. CONNECTION TO ACHIEVE MINIMUM SINE WAVE DISTORTION

Selecting R_A, R_B and C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times (V+ - V-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{0.22(V+ - V-)}{R_A}$$

R_1 and R_2 are shown in the Detailed Schematic.

A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.

Waveform Out Level Control and Power Supplies

The waveform generator can be operated either from a single power supply (10V to 30V) or a dual power supply (±5V to ±15V). With a single power supply the average levels of the triangle and sine wave are at exactly one-half of the supply voltage, while the square wave alternates between V+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square wave output is not committed. A load resistor can be connected to a different power supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square wave output can be made TTL compatible (load resistor connected to +5V) while the waveform generator itself is powered from a much higher voltage.

Frequency Modulation and Sweeping

The frequency of the waveform generator is a direct function of the DC voltage at Terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 5A. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 5B). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f = 0 at V_{SWEEP} = 0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V+ by ($^1/_3$ V_{SUPPLY} - 2V).

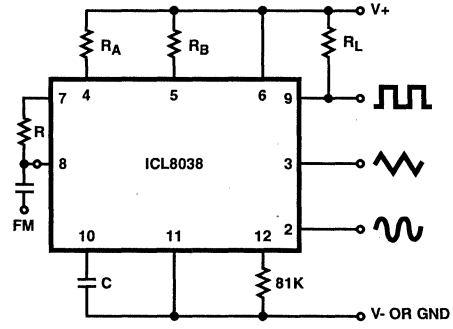


FIGURE 5A. CONNECTIONS FOR FREQUENCY MODULATION

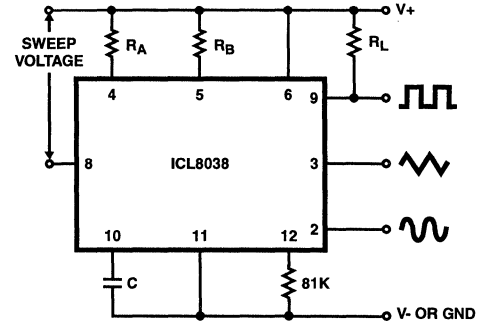


FIGURE 5B. CONNECTIONS FOR FREQUENCY SWEEP

FIGURE 5.

Typical Applications

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 6 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

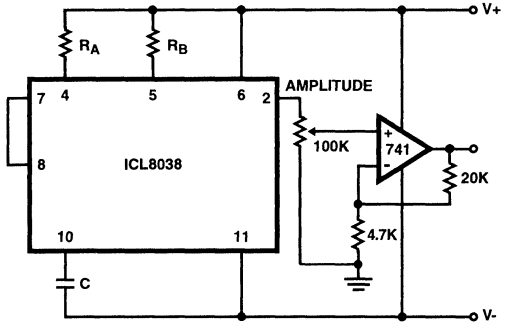


FIGURE 6. SINE WAVE OUTPUT BUFFER AMPLIFIERS

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 7 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

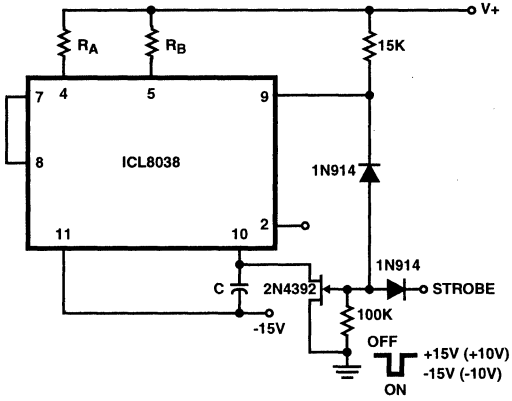
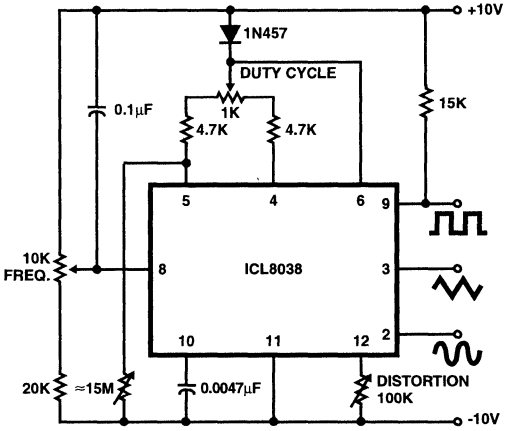


FIGURE 7. STROBE TONE BURST GENERATOR

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors R_A and R_B must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of R_A and R_B by a few hundred mV. The Circuit of Figure 8 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 9.



GURE 8. VARIABLE AUDIO OSCILLATOR, 20Hz TO 20kHzY

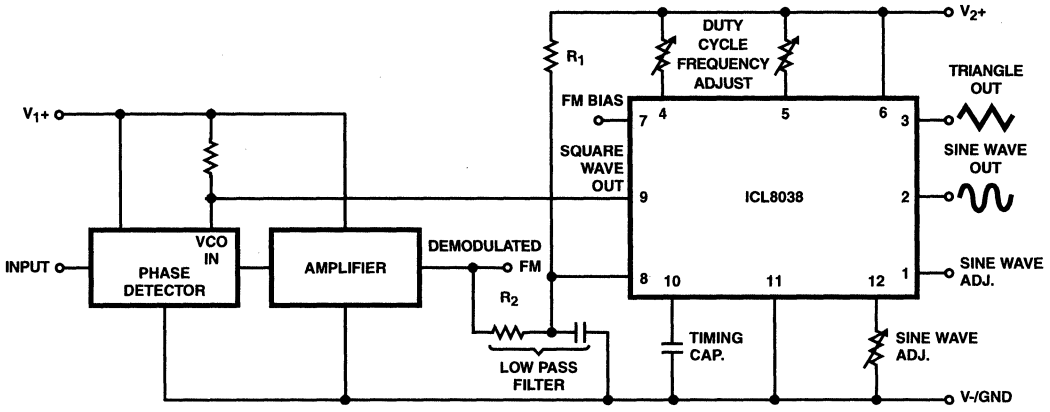


FIGURE 9. WAVEFORM GENERATOR USED AS STABLE VCO IN A PHASE-LOCKED LOOP

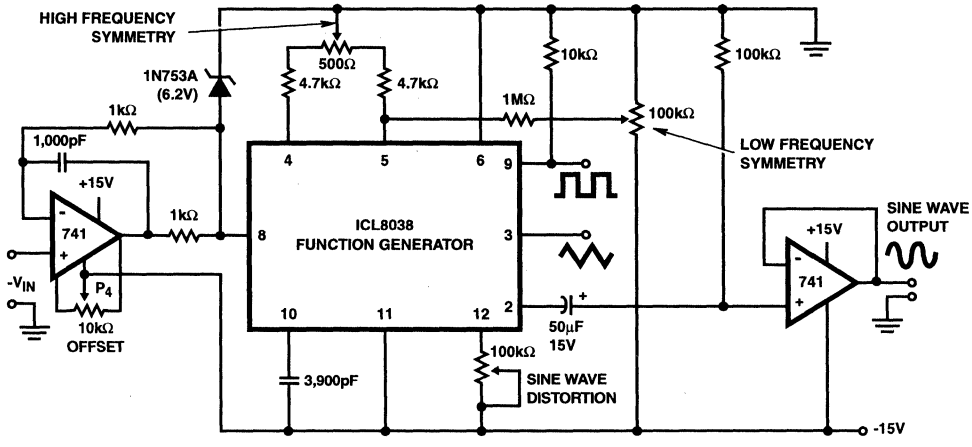


FIGURE 10. LINEAR VOLTAGE CONTROLLED OSCILLATOR

Use in Phase Locked Loops

Its high frequency stability makes the ICL8038 an ideal building block for a phase locked loop as shown in Figure 10. In this application the remaining functional blocks, the phase detector and the amplifier, can be formed by a number of available ICs (e.g., MC4344, NE562, HA2800, HA2820).

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8V+). The simplest solution here is to provide a voltage divider to V+ (R_1, R_2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but is also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Harris Application Note AN013, "Everything You Always Wanted to Know About the ICL8038".

Definition of Terms

Supply Voltage (V_{SUPPLY}). The total supply voltage from V+ to V-.

Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.

Frequency Range. The frequency range at the square wave output through which circuit operation is guaranteed.

Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range:

$(^2/_3\ V_{SUPPLY} + 2V) < V_{SWEEP} < V_{SUPPLY}$

FM Linearity. The percentage deviation from the best fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

Saturation Voltage. The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.

Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

Triangle Waveform Linearity. The percentage deviation from the best fit straight line on the rising and falling triangle waveform.

Total Harmonic Distortion. The total harmonic distortion at the sine wave output.

Typical Performance Curves

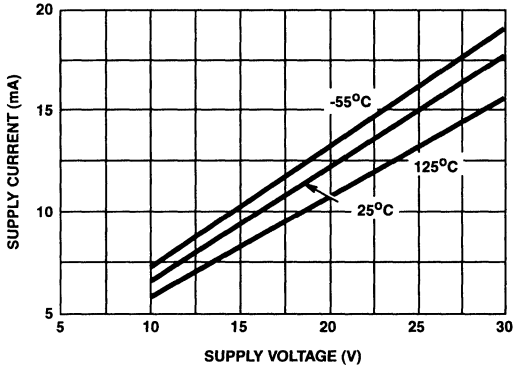


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE

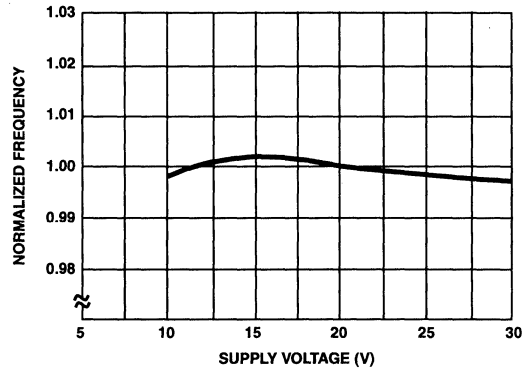


FIGURE 12. FREQUENCY vs SUPPLY VOLTAGE

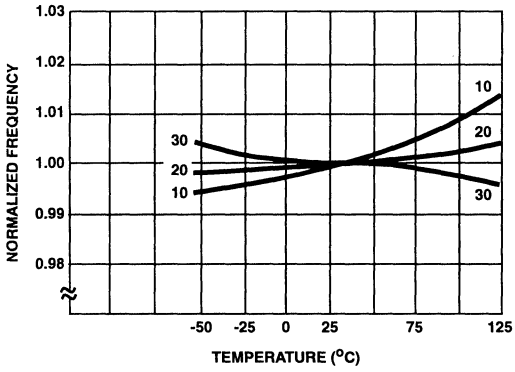


FIGURE 13. FREQUENCY vs TEMPERATURE

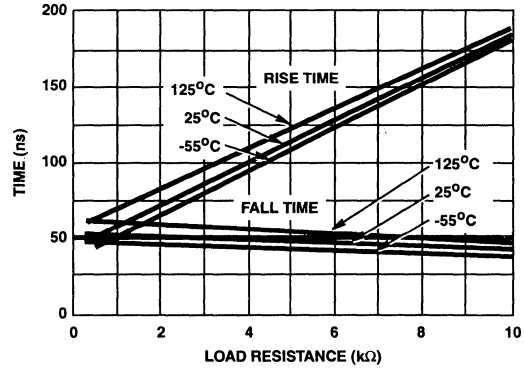


FIGURE 14. SQUARE WAVE OUTPUT RISE/FALL TIME vs LOAD RESISTANCE

Typical Performance Curves (Continued)

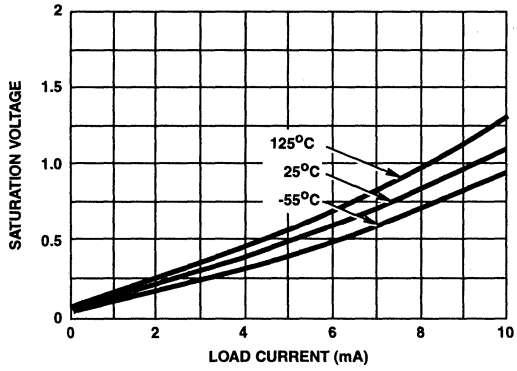


FIGURE 15. SQUARE WAVE SATURATION VOLTAGE vs LOAD CURRENT

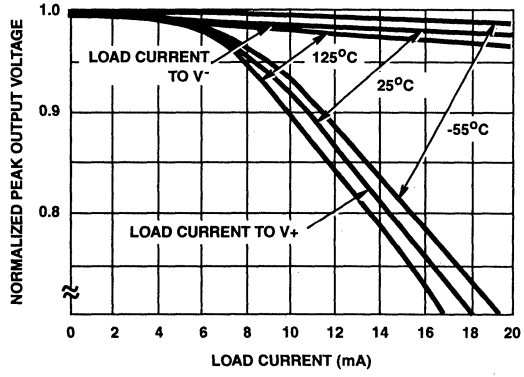


FIGURE 16. TRIANGLE WAVE OUTPUT VOLTAGE vs LOAD CURRENT

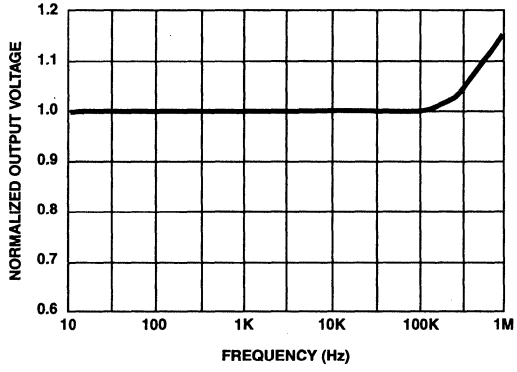


FIGURE 17. TRIANGLE WAVE OUTPUT VOLTAGE vs FREQUENCY

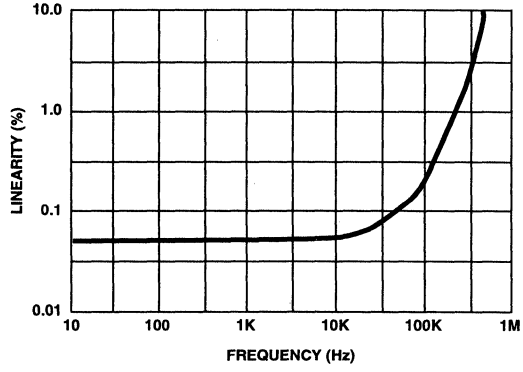


FIGURE 18. TRIANGLE WAVE LINEARITY vs FREQUENCY

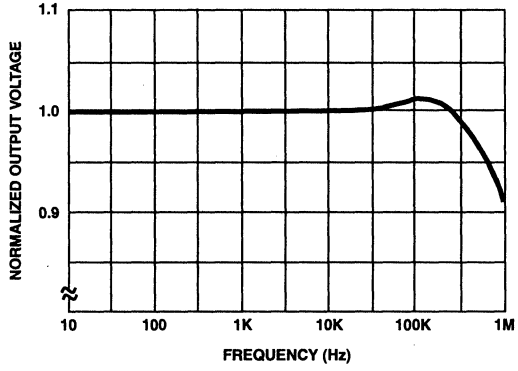


FIGURE 19. SINE WAVE OUTPUT VOLTAGE vs FREQUENCY

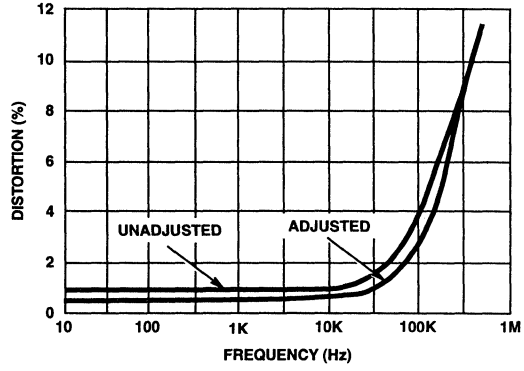


FIGURE 20. SINE WAVE DISTORTION vs FREQUENCY

HARRIS SEMICONDUCTOR

ICM7242

November 1996

Long Range Fixed Timer

Features

- **Replaces the 2242 in Most Applications**
- **Timing From Microseconds to Days**
- **Cascadable**
- **Monostable or Astable Operation**
- **Wide Supply Voltage Range . . . . . 2V to 16V**
- **Low Supply Current . . . . . 115µA at 5V**

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICM7242IPA	-25 to 85	8 Ld PDIP	E8.3
ICM7242CBA (7242CBA)	0 to 70	8 Ld SOIC	M8.15

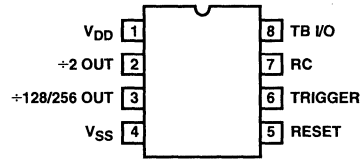
Description

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in most applications, with a significant reduction in the number of external components.

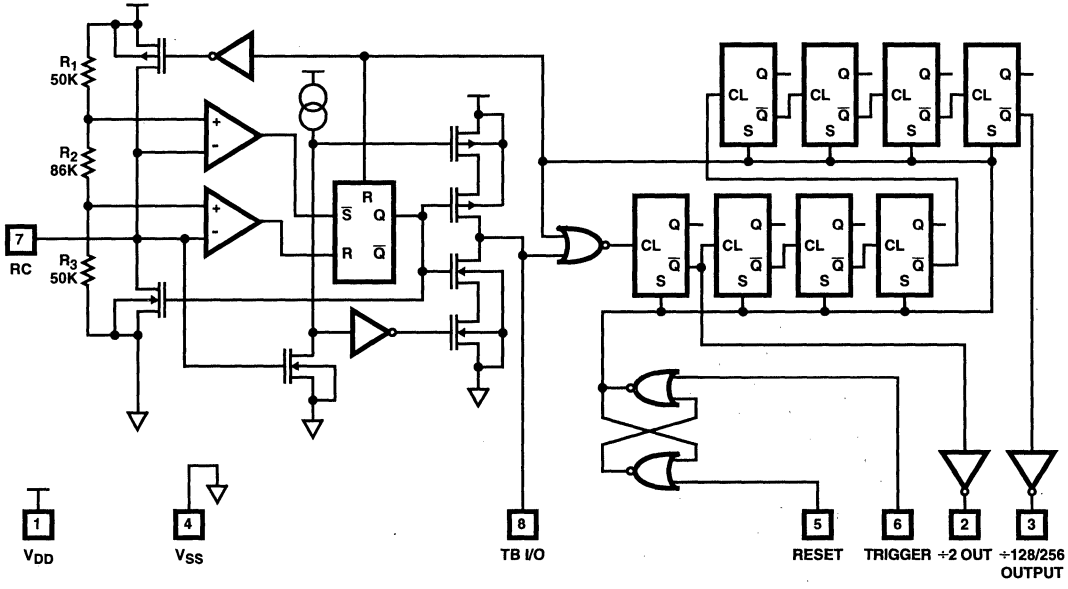
Three outputs are provided. They are the oscillator output, and buffered outputs from the first and eighth counters.

Pinout

ICM7242
(PDIP, SOIC)
TOP VIEW



Functional Diagram



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1996

File Number **2866.2**

Absolute Maximum Ratings

Supply Voltage (V_{DD} to V_{SS}) 18V
Input Voltage (Note 1)
Terminals (Pins 5, 6, 7, 8) . . . . . (V_{SS} -0.3V) to (V_{DD} +0.3V)
Continuous Output Current (Each Output) 50mA

Operating Conditions

Temperature Range
ICM7242I . . . . . -25°C to 85°C
ICM7242C . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	100
SOIC Package	160

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

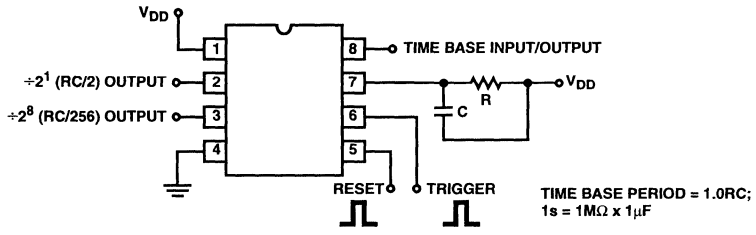
V_{DD} = 5V, T_A = 25°C, R = 10kΩ, C = 0.1µF, V_{SS} = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V_{DD}		2	-	16	V
Supply Current	I_{DD}	Reset	-	125	-	µA
		Operating, R = 10kΩ, C = 0.1µF	-	340	800	µA
		Operating, R = 1MΩ, C = 0.1µF	-	220	600	µA
		TB Inhibited, RC Connected to V_{SS}	-	225	-	µA
Timing Accuracy			-	5	-	%
RC Oscillator Frequency Temperature Drift	$\Delta f/\Delta t$	Independent of RC Components	-	250	-	ppm/°C
Time Base Output Voltage	V_{OTB}	I_{SOURCE} = 100µA	-	3.5	-	V
		I_{SINK} = 1.0mA	-	0.40	-	V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground	-	-	25	µA
Trigger Input Voltage	V_{TRIG}	V_{DD} = 5V	-	1.6	2.0	V
		V_{DD} = 15V	-	3.5	4.5	V
Reset Input Voltage	V_{RST}	V_{DD} = 5V	-	1.3	2.0	V
		V_{DD} = 15V	-	2.7	4.0	V
Trigger/Reset Input Current	I_{TRIG}, I_{RST}		-	10	-	µA
Max Count Toggle Rate	f_T	V_{DD} = 2V (Counter/Divider Mode)	-	1	-	MHz
		V_{DD} = 5V (Counter/Divider Mode)	2	6	-	MHz
		V_{DD} = 15V (Counter/Divider Mode)	-	13	-	MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V_{DD} and V_{SS}				
Output Saturation Voltage	V_{SAT}	All Outputs Except TB Output V_{DD} = 5V, I_{OUT} = 3.2mA	-	0.22	0.4	V
Output Sourcing Current	I_{SOURCE}	V_{DD} = 5V Terminals 2 and 3, V_{OUT} = 1V	-	300	-	µA
MIN Timing Capacitor (Note 3)	C_T		10	-	-	pF
Timing Resistor Range (Note 3)	R_T	V_{DD} = 2 - 16V	1K	-	22M	Ω

NOTE:

3. For design only, not tested.

Test Circuit



NOTE:

4. $\div 2^1$ and $\div 2^8$ outputs are inverters and have active pullups.

Application Information

Operating Considerations

Shorting the RC terminal or output terminals to V_{DD} may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in Figure 8. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200kHz.

The timing capacitor should be connected between the RC pin and the positive supply rail, V_{DD}, as shown in Figure 1. When system power is turned off, any charge remaining on the capacitor will be discharged to ground through a large internal diode between the RC node and V_{SS}. Do NOT reference the timing capacitor to ground, since there is no high current path in this direction to safely discharge the capacitor when power is turned off. The discharge current from such a configuration could potentially damage the device.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to the supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be ANDed, output inverters are used instead of open drain N-Channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

The timing diagram for the ICM7242 is shown in Figure 1. Assuming that the device is in the RESET mode, which occurs on power up or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the $\div 2^8$ output returns to the high state.

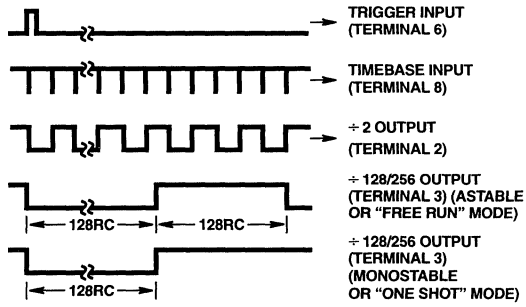


FIGURE 1. TIMING DIAGRAMS OF OUTPUT WAVEFORMS FOR THE ICM7242 (COMPARE WITH FIGURE 5)

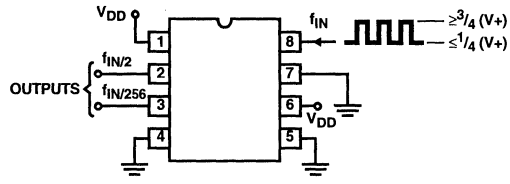


FIGURE 2. USING THE ICM7242 AS A RIPPLE COUNTER (DIVIDER)

To use the 8-bit counter without the timebase, Terminal 7 (RC) should be connected to ground and the outputs taken from Terminals 2 and 3.

The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 3).

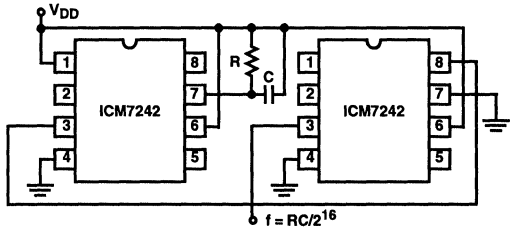


FIGURE 3. LOW FREQUENCY REFERENCE (OSCILLATOR)

For monostable operation the $\div 2^8$ output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

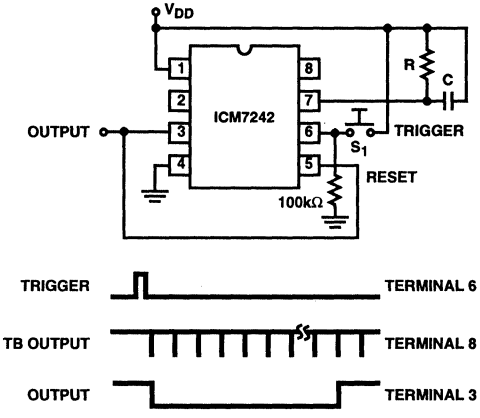


FIGURE 4. MONOSTABLE OPERATION

The ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p- resistors have been used on the ICM7242 to provide the comparator timing points.

Comparing the ICM7242 With the 2242

	ICM7242	2242
Operating Voltage	2V - 16V	4V - 15V
Operating Temperature Range	-25°C to 85°C	0°C to 70°C
Supply Current, V_{DD} = 5V	0.7mA (Max)	7mA (Max)
Pullup Resistors		
TB Output	No	Yes
÷2 Output	No	Yes
÷256 Output	No	Yes
Toggle Rate	3.0MHz	0.5MHz
Resistor to Inhibit Oscillator	No	Yes
Resistor in Series with Reset for Monostable Operation	No	Yes
Capacitor TB Terminal for HF Operation	No	Sometimes

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as shown in Figure 5.

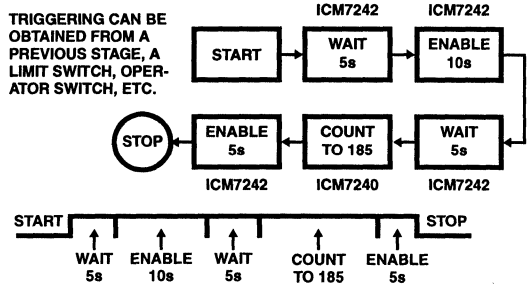
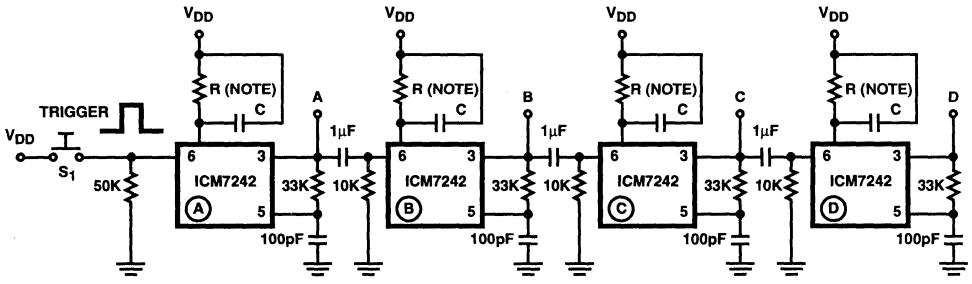


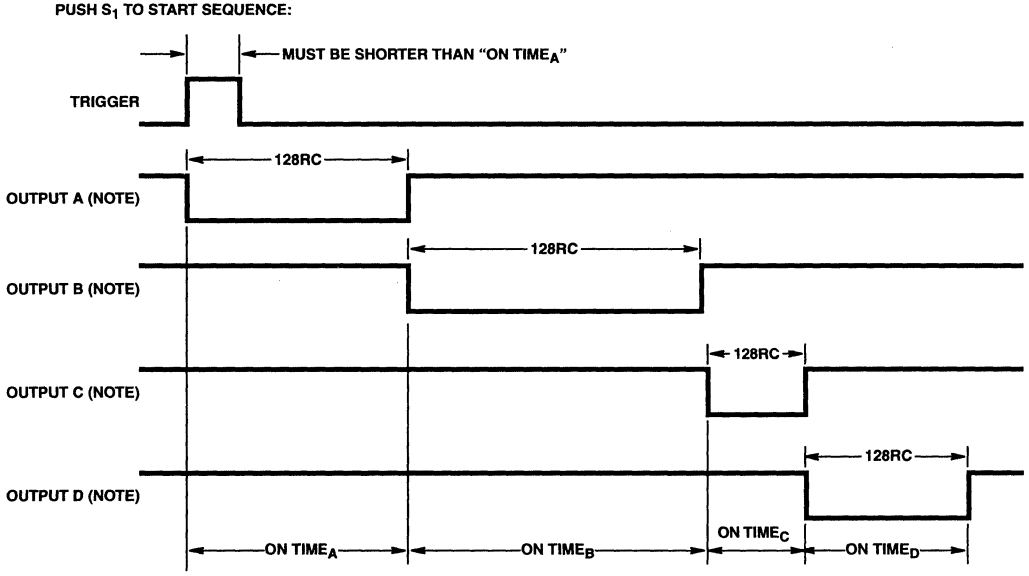
FIGURE 5. FLOW CHART FOR MACHINE TOOL CONTROLLER

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

Sequence Timing

- Process Control
- Machine Automation
- Electro-Pneumatic Drivers
- Multi Operation (Serial or Parallel Controlling)





NOTE: Select RC values for desired "ON TIME" for each ICM7242.

FIGURE 6. SEQUENCE TIMER

Typical Performance Curves

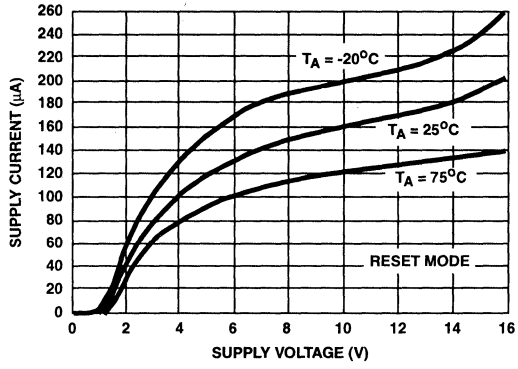


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

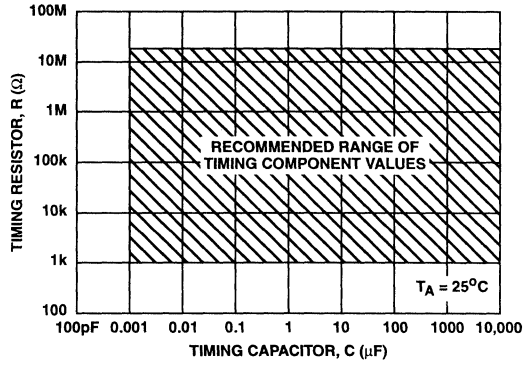


FIGURE 8. RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING

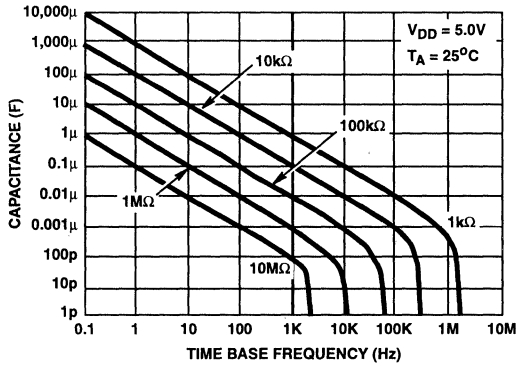


FIGURE 9. TIMEBASE FREE RUNNING FREQUENCY vs R AND C

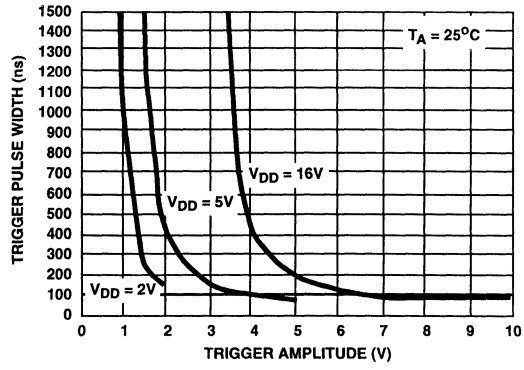


FIGURE 10. MINIMUM TRIGGER PULSE WIDTH vs TRIGGER AMPLITUDE

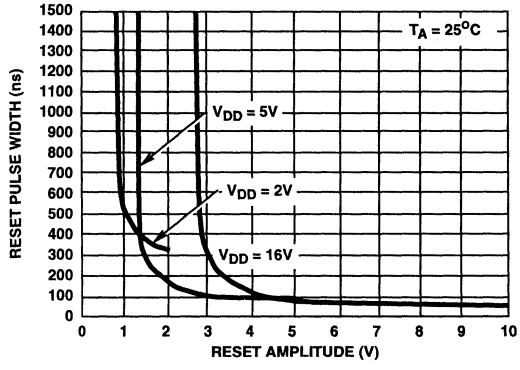


FIGURE 11. MINIMUM RESET PULSE WIDTH vs RESET AMPLITUDE

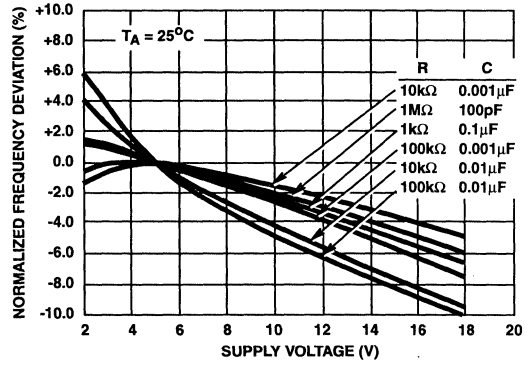


FIGURE 12. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

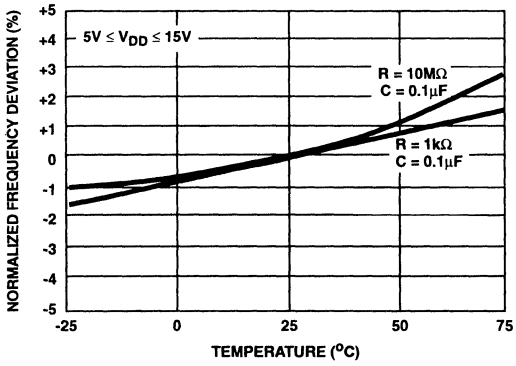


FIGURE 13. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs TEMPERATURE

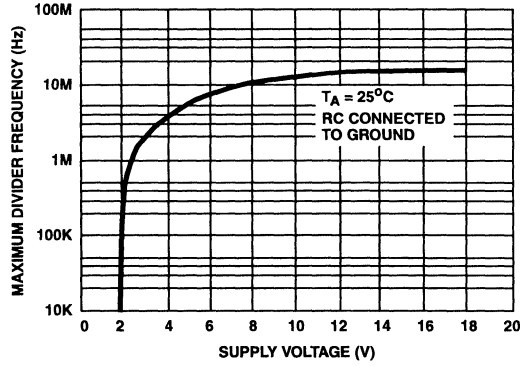


FIGURE 14. MAXIMUM DIVIDER FREQUENCY vs SUPPLY VOLTAGE

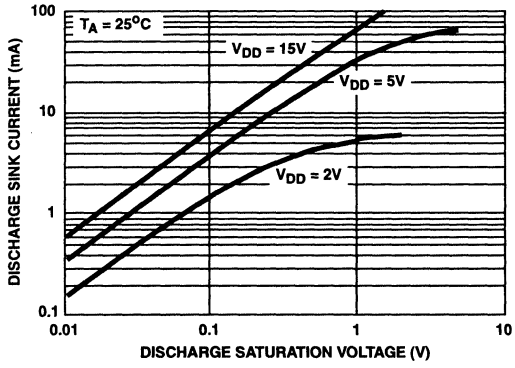


FIGURE 15. DISCHARGE OUTPUT CURRENT vs DISCHARGE OUTPUT VOLTAGE

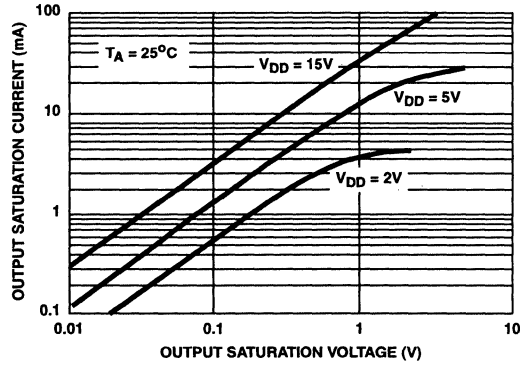


FIGURE 16. OUTPUT SATURATION CURRENT vs OUTPUT SATURATION VOLTAGE

HARRIS SEMICONDUCTOR

ICM7555, ICM7556

November 1996

General Purpose Timers

Features

- Exact Equivalent in Most Cases for SE/NE555/556 or TLC555/556
- Low Supply Current
  - ICM7555 ..... 60μA
  - ICM7556 ..... 120μA
- Extremely Low Input Currents 20pA
- High Speed Operation 1MHz
- Guaranteed Supply Voltage Range ..... 2V to 18V
- Temperature Stability ..... 0.005%/°C at 25°C
- Normal Reset Function - No Crowbarring of Supply During Output Transition
- Can be Used with Higher Impedance Timing Elements than Regular 555/6 for Longer RC Time Constants
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Output Source/Sink Driver can Drive TTL/CMOS
- Outputs have Very Low Offsets, HI and LO

Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

Description

The ICM7555 and ICM7556 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555 and ICM7556 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

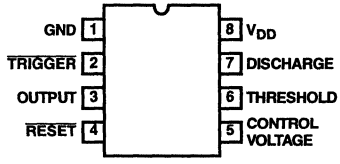
Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICM7555CBA (7555CBA)	0 to 70	8 Ld SOIC	M18.5
ICM7555IBA (7555IBA)	-25 to 85	8 Ld SOIC	M18.5
ICM7555IPA	-25 to 85	8 Ld PDIP	E8.3
ICM7555ITV	-25 to 85	8 Pin Metal Can	T8.C
ICM7555MTV (Note)	-55 to 125	8 Pin Metal Can	T8.C
ICM7556IPD	-25 to 85	14 Ld PDIP	E14.3
ICM7556MJD (Note)	-55 to 125	14 Ld CERDIP	F14.3

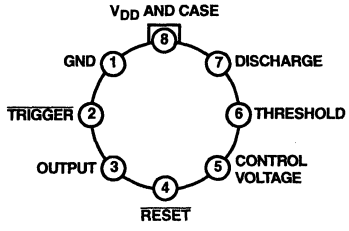
NOTE: Add /883B to part number if 883B processing is desired.

Pinouts

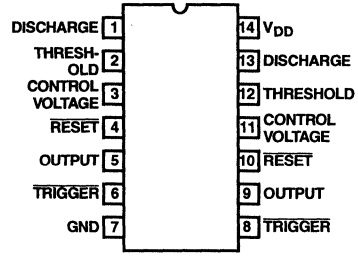
ICM7555 (PDIP, SOIC)
TOP VIEW



ICM7555 (METAL CAN)
TOP VIEW



ICM7556 (PDIP, CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2867.2**

Absolute Maximum Ratings

Supply Voltage . . . . . +18V
Input Voltage
$\overline{\text{Trigger}}$, Control Voltage, Threshold,
$\overline{\text{Reset}}$ (Note 1). . . . . V+ +0.3V to GND -0.3V
Output Current 100mA

Operating Conditions

Temperature Range
ICM7555C. . . . . 0°C to 70°C
ICM7555I, ICM7556I. . . . . -25°C to 85°C
ICM7555M, ICM7556M. . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	80	24
Metal Can Package	165	80
14 Lead PDIP Package	115	N/A
8 Lead PDIP Package	110	N/A
SOIC Package	170	N/A

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ +0.3V or less than V- -0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple supply systems, the supply of the ICM7555/6 must be turned on first.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Applies to ICM7555 and ICM7556, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		$T_A = 25°C$			(NOTE 4) -55°C TO 125°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Static Supply Current	I_{DD}	ICM7555	V_{DD} = 5V	-	40	200	-	-	300	µA
			V_{DD} = 15V	-	60	300	-	-	300	µA
		ICM7556	V_{DD} = 5V	-	80	400	-	-	600	µA
			V_{DD} = 15V	-	120	600	-	-	600	µA
Monostable Timing Accuracy		R_A = 10K, C = 0.1µF, V_{DD} = 5V		-	2	-	-	-	-	%
				-	-	-	858	-	1161	µs
Drift with Temperature (Note 3)		V_{DD} = 5V		-	-	-	-	150	-	ppm/°C
		V_{DD} = 10V		-	-	-	-	200	-	ppm/°C
		V_{DD} = 15V		-	-	-	-	250	-	ppm/°C
Drift with Supply (Note 3)		V_{DD} = 5V to 15V		-	0.5	-	-	0.5	-	%/V
Astable Timing Accuracy		$R_A = R_B$ = 10K, C = 0.1µF, V_{DD} = 5V		-	2	-	-	-	-	%
				-	-	-	1717	-	2323	µs
Drift with Temperature (Note 3)		V_{DD} = 5V		-	-	-	-	150	-	ppm/°C
		V_{DD} = 10V		-	-	-	-	200	-	ppm/°C
		V_{DD} = 15V		-	-	-	-	250	-	ppm/°C
Drift with Supply (Note 3)		V_{DD} = 5V to 15V		-	0.5	-	-	0.5	-	%/V
Threshold Voltage	V_{TH}	V_{DD} = 15V		62	67	71	61	-	72	% V_{DD}
Trigger Voltage	V_{TRIG}	V_{DD} = 15V		28	32	36	27	-	37	% V_{DD}
Trigger Current	I_{TRIG}	V_{DD} = 15V		-	-	10	-	-	50	nA
Threshold Current	I_{TH}	V_{DD} = 15V		-	-	10	-	-	50	nA
Control Voltage	V_{CV}	V_{DD} = 15V		62	67	71	61	-	72	% V_{DD}
Reset Voltage	V_{RST}	V_{DD} = 2V to 15V		0.4	-	1.0	0.2	-	1.2	V
Reset Current	I_{RST}	V_{DD} = 15V		-	-	10	-	-	50	nA

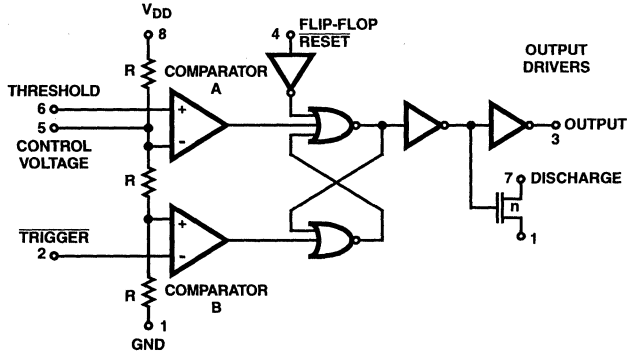
Electrical Specifications Applies to ICM7555 and ICM7556, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A = 25^oC$			(NOTE 4) -55^oC TO 125^oC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Discharge Leakage	I_{DIS}	V_{DD} = 15V	-	-	10	-	-	50	nA
Output Voltage	V_{OL}	V_{DD} = 15V, I_{SINK} = 20mA	-	0.4	1.0	-	-	1.25	V
		V_{DD} = 5V, I_{SINK} = 3.2mA	-	0.2	0.4	-	-	0.5	V
	V_{OH}	V_{DD} = 15V, I_{SOURCE} = 0.8mA	14.3	14.6	-	14.2	-	-	V
		V_{DD} = 5V, I_{SOURCE} = 0.8mA	4.0	4.3	-	3.8	-	-	V
Discharge Output Voltage	V_{DIS}	V_{DD} = 5V, I_{SINK} = 15mA	-	0.2	0.4	-	-	0.6	V
		V_{DD} = 15V, I_{SINK} = 15mA	-	-	-	-	-	0.4	V
Supply Voltage (Note 3)	V_{DD}	Functional Operation	2.0	-	18.0	3.0	-	16.0	V
Output Rise Time (Note 3)	t_R	R_L = 10M, C_L = 10pF, V_{DD} = 5V	-	75	-	-	-	-	ns
Output Fall Time (Note 3)	t_F	R_L = 10M, C_L = 10pF, V_{DD} = 5V	-	75	-	-	-	-	ns
Oscillator Frequency (Note 3)	f_{MAX}	V_{DD} = 5V, R_A = 470Ω, R_B = 270Ω, C = 200pF	-	1	-	-	-	-	MHz

NOTES:

3. These parameters are based upon characterization data and are not tested.
4. Applies only to military temperature range product (M suffix).

Functional Diagram



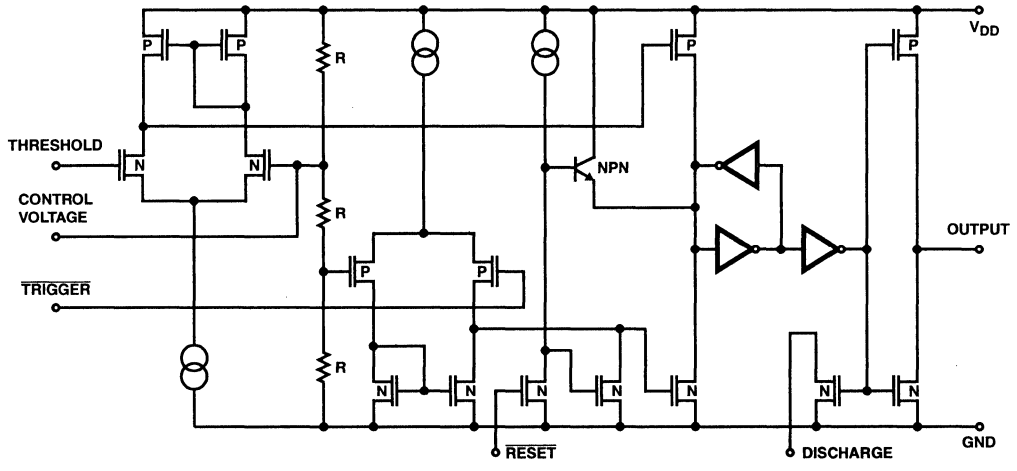
NOTE: This functional diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs. R = 100kΩ, ±20% (Typ)

TRUTH TABLE

THRESHOLD VOLTAGE	$\overline{\text{TRIGGER}}$ VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
Don't Care	Don't Care	Low	Low	On
$>^2/_3(V+)$	$>^1/_3(V+)$	High	Low	On
$<^2/_3(V+)$	$>^1/_3(V+)$	High	Stable	Stable
Don't Care	$<^1/_3(V+)$	High	High	Off

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

Schematic Diagram



R = 100kΩ ±20% (TYP)

Application Information

General

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 1.

The ICM7555/6 produces supply current spikes of only 2mA - 3mA instead of 300mA - 400mA and supply decoupling is normally not necessary. Also, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

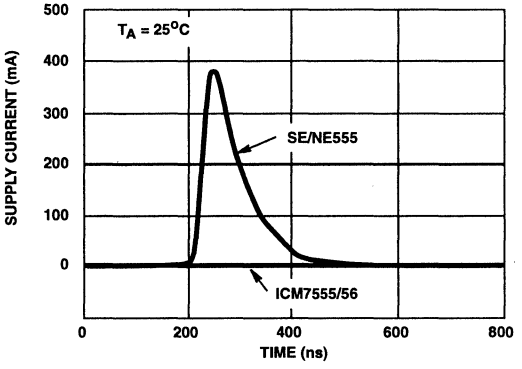


FIGURE 1. SUPPLY CURRENT TRANSIENT COMPARED WITH A STANDARD BIPOLAR 555 DURING AN OUTPUT TRANSITION

Power Supply Considerations

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply current can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 2 and 3.

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more the ICM7555/6 will drive at least 2 standard TTL loads.

Astable Operation

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 2A. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5V to +15V.

$$f = \frac{1}{1.4\,RC}$$

The timer can also be connected as shown in Figure 2B. In this circuit, the frequency is:

$$f = 1.44/(R_A + 2R_B)C$$

The duty cycle is controlled by the values of R_A and R_B, by the equation:

$$D = (R_A + R_B)/(R_A + 2R_B)$$

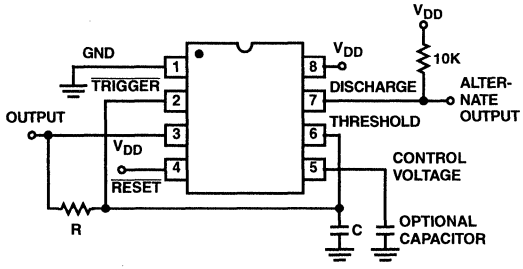


FIGURE 2A. ASTABLE OPERATION

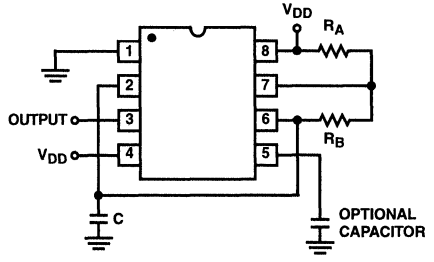


FIGURE 2B. ALTERNATE ASTABLE CONFIGURATION

Monostable Operation

In this mode of operation, the timer functions as a one-shot, see Figure 3. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip-flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals $^2/_3$ V+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

$$t_{OUTPUT} = -\ln(^1/_3)\,R_AC = 1.1R_AC$$

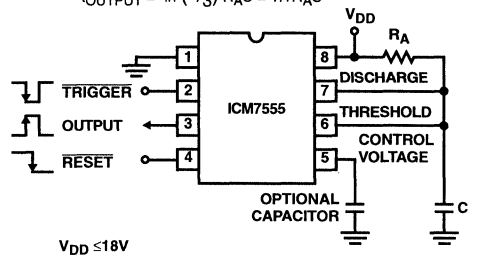


FIGURE 3. MONOSTABLE OPERATION

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e., 0.6V to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

Typical Performance Curves

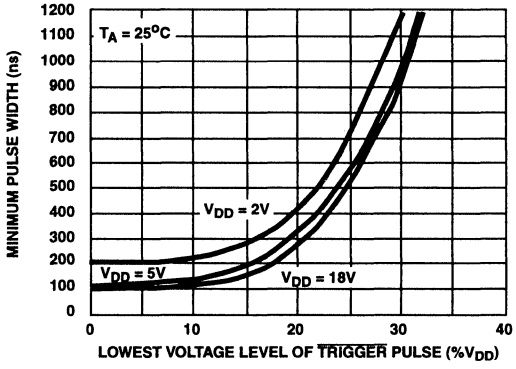


FIGURE 4. MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING

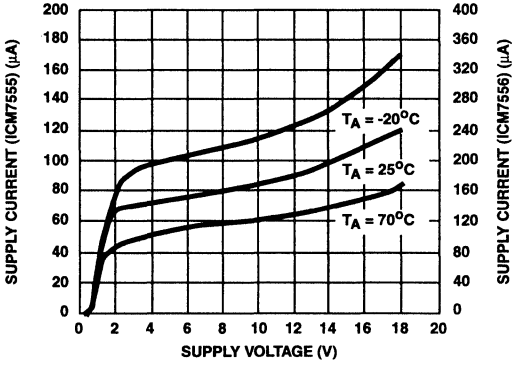


FIGURE 5. SUPPLY CURRENT vs SUPPLY VOLTAGE

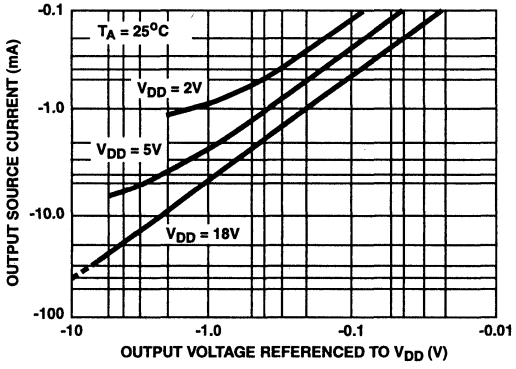


FIGURE 6. OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

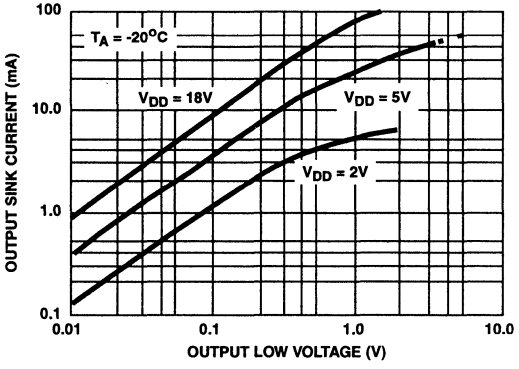


FIGURE 7. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

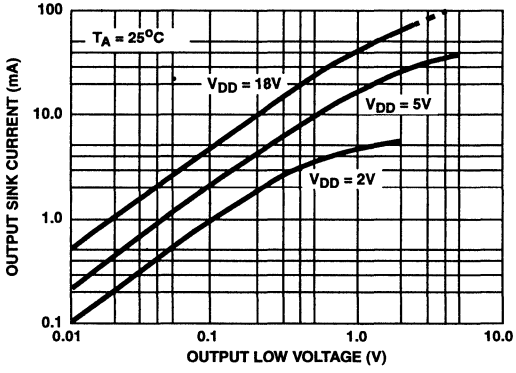


FIGURE 8. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

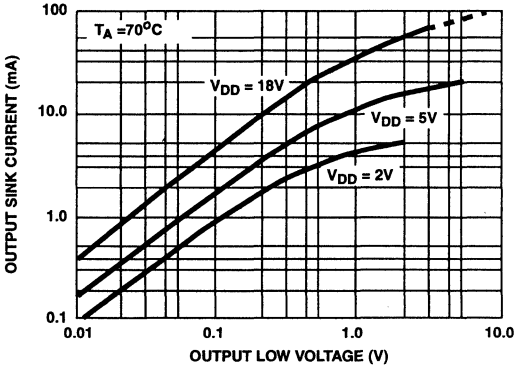


FIGURE 9. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

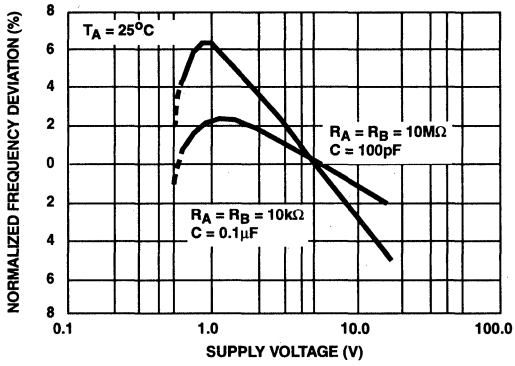


FIGURE 10. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs SUPPLY VOLTAGE

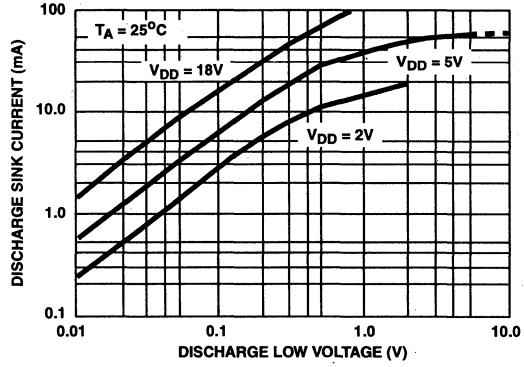


FIGURE 11. DISCHARGE OUTPUT CURRENT vs DISCHARGE OUTPUT VOLTAGE

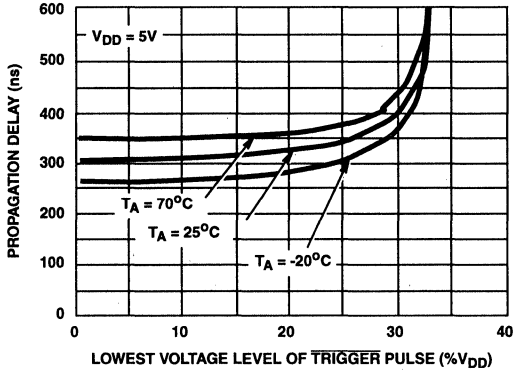


FIGURE 12. PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE

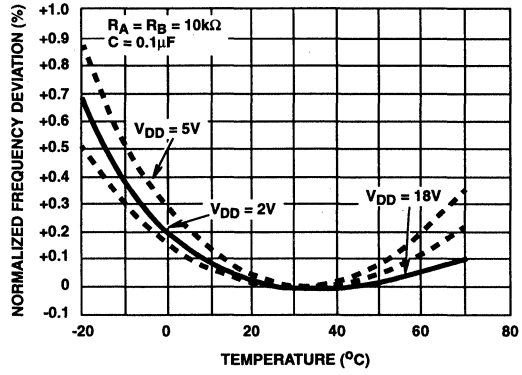


FIGURE 13. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs TEMPERATURE

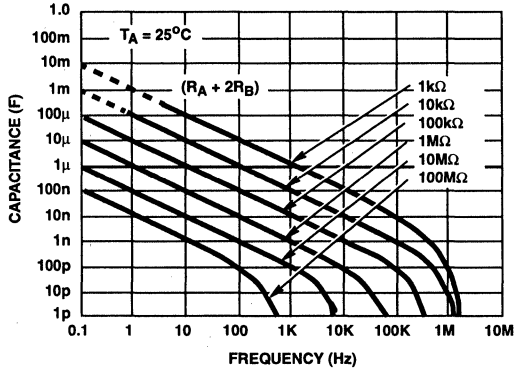


FIGURE 14. FREE RUNNING FREQUENCY vs R_A, R_B AND C

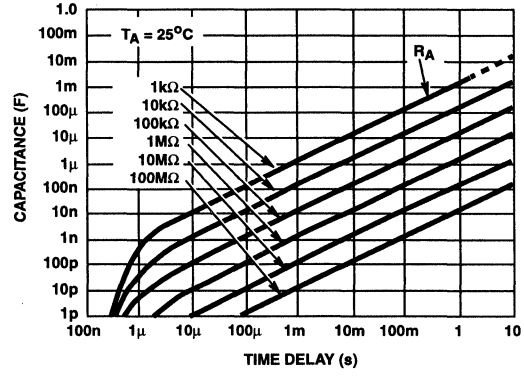


FIGURE 15. TIME DELAY IN THE MONOSTABLE MODE vs R_A AND C

LINEAR 9

HARRIS QUALITY AND RELIABILITY

Harris Quality

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

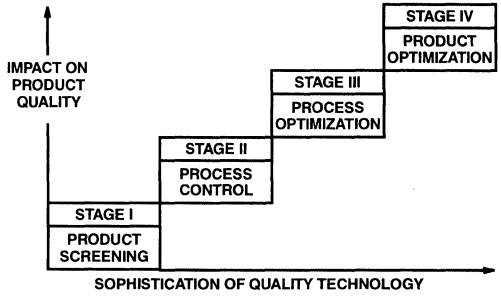


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

ISO 9000 Certification

The manufacturing operations of Harris Semiconductor have all received ISO certification. The ISO 9000 series of standards were very consistent with our goals to build an even stronger quality system foundation.

Qualified Manufacturing List (QML)

Harris Semiconductor has supplied military grade integrated circuits for over 20 years. The government's certifying body had audited and granted approval to ship JAN, 883 compliant, and Source Military Drawing parts used in ground and space applications. The discipline required to manufacture high reliability components has been beneficial to the commercial product lines. Harris has now taken the next evolutionary step by transitioning into QML as defined in MIL-PRF-38535. These guidelines incorporate the best commercial practices for semiconductor manufacturing.

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• Internal Audits		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance	X	X
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X
Assembly	• Internal Audits		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Ball Bond Shear/Controls		X
	- Die Shear Controls		X
	- Post-Bond/Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND Test	X	X
	- Lead Finish Visuals, Thickness	X	X
	- Solderability	X	X
	• Process		
	- Operator Quality Performance	X	X
	- Saw Controls	X	X
	- Die Attach Temperatures	X	X
	- Seal Parameters	X	X
	- Seal Temperature Profile	X	X
	- Sta-Bake Profile	X	X
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	X
	- Mold Parameters	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Test	• Internal Audits		X
	• Temperature/Humidity	X	X
	• ESD Controls	X	X
	• Temperature Test Calibration	X	X
	• Test System Calibration	X	X
	• Test Procedures		X
	• Control Unit Compliance	X	X
	• Lot Acceptance Conformance	X	X
	• Group A Lot Acceptance		X
Probe	• Internal Audits		X
	• Wafer Repeat Correlation	X	X
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X
Burn-In	• Internal Audits		X
	• Functionality Board Check	X	X
	• Oven Temperature Controls	X	X
	• Procedural Conformance		X
Brand	• Internal Audits		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	X
	• Procedural Conformance		X
QCI Inspection	• Internal Audits		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

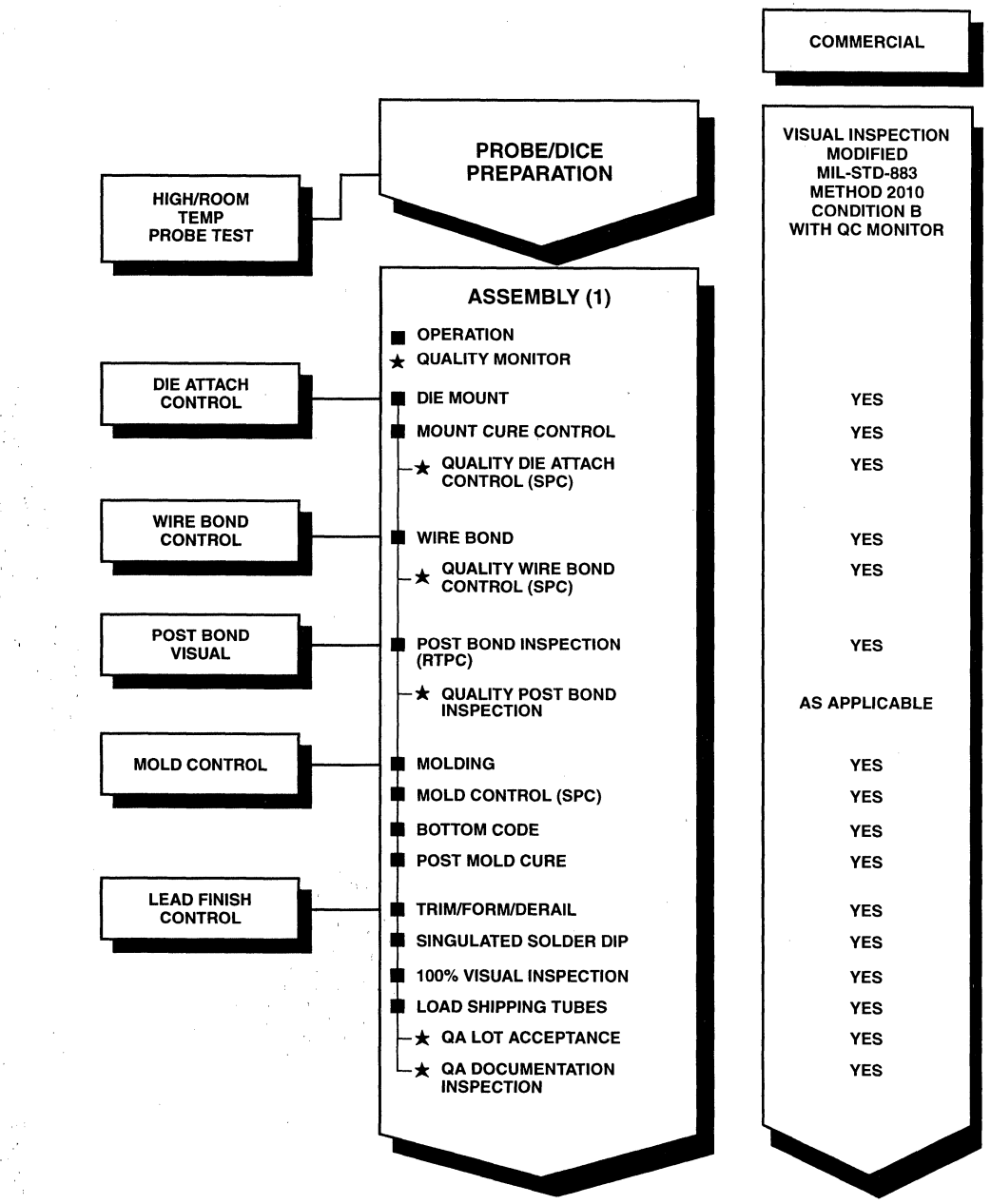
Special Testing

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than 25°C. The flow shown in Figures 2 and 3 indicates the Harris standard processing flow for a commercial linear part in a PDIP package. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for nonstandard environmental stress screening. Consult your field sales representative for details

TABLE 2. HARRIS IC DESIGN TOOLS

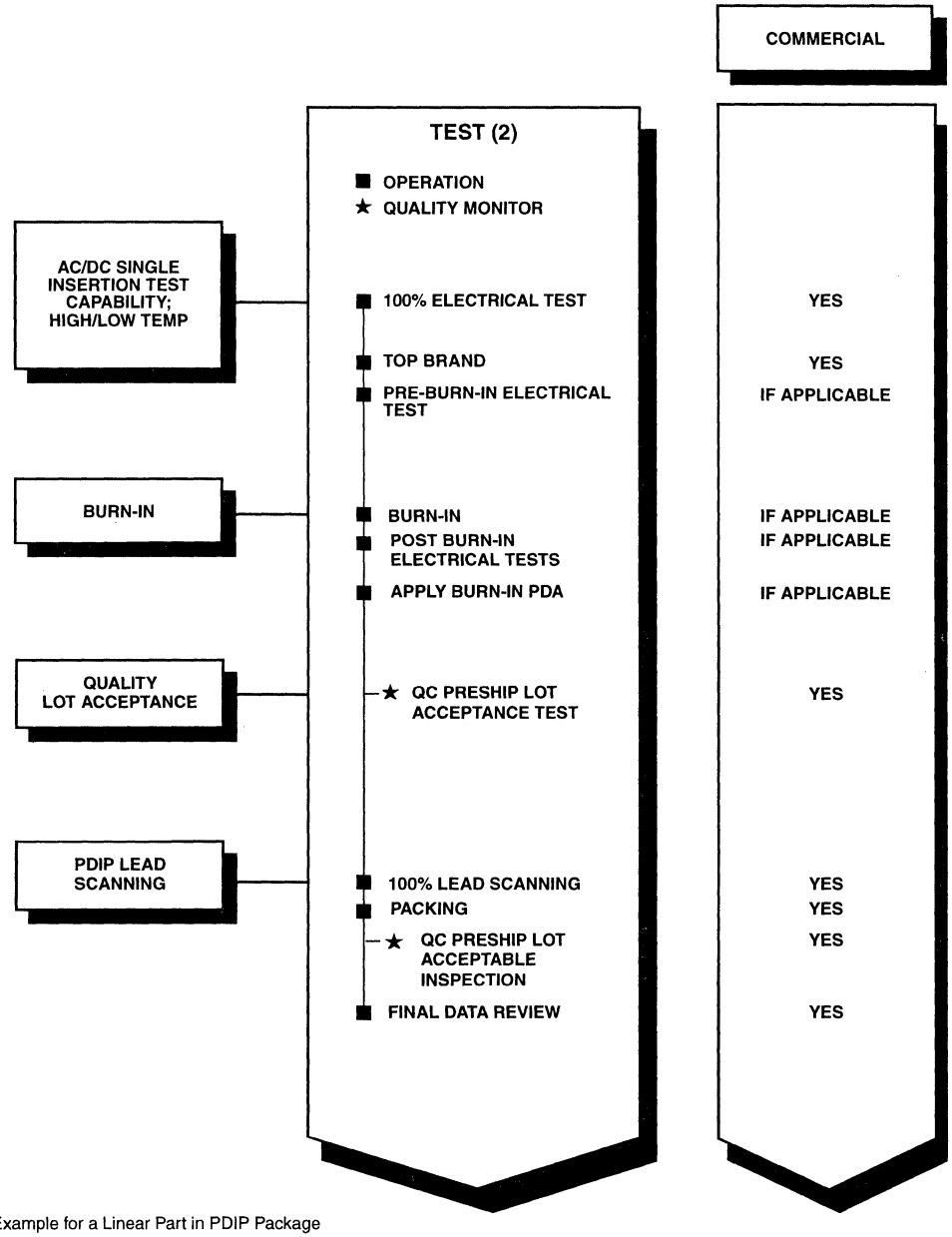
DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Cds Spice	Cds Spice Verilog
Parametric Simulation	Cds Spice Monte Carlo	Cds Spice
Schematic Capture	Cadence	Cadence
Functional Checking	Cadence	Cadence
Rules Checking	Cadence	Cadence
Parasitic Extraction	Cadence	Cadence

Harris Semiconductor Standard Processing Flow



(1) Example for a PDIP Package Part

FIGURE 2.



(2) Example for a Linear Part in PDIP Package

FIGURE 3.

TABLE 3. PROCESS CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition - Particles Added	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates - Energy Monitor (E_O)	• Measurement Equipment - Critical Dimension - Film Thickness - Resistivity
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Ball Bond Shear - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control - Temperature - Humidity	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost (see Table 4).

TABLE 4. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at upgrading process performance by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in ANSI/ASQC Z1.4, MIL-STD-883 and MIL-PRF-38535 are used by our quality inspectors.

The focus on this quality parameter has resulted in a continuous improvement to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, facilitators, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and facilitators in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris's manufacturing needs and vendor capabilities, and continual improvement programs are all

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs
Capability Studies	Techs, Faciitators, Engineers	Capability Indices (C_P and C_{PK}), Variance Components, Nested Models, Fixed and Random Effects

part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials. Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificate of Analysis for all Critical Parameters • Control Charts from On-Line Processing • Certificate of Conformance
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Certificate of Conformance • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters • Certificate of Conformance
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Certificate of Conformance • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of ANSI/NCSL Z540-1.

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

Introduction

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing processes. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life.

Reliability Engineering

The Reliability Engineering department is responsible for all aspects of reliability assurance at Harris Semiconductor:

- Charter
  - To ensure that Harris is recognized by our customers and competitors as a company that consistently delivers products with high reliability.

- Mission
  - To develop systems for assessing, enhancing, and assuring that quality and reliability are integrated into all aspects of our business.

- Vision
  - To establish excellence and integrity through all design and manufacturing processes as it relates to quality and reliability.

Values

- To be considered responsive and service oriented by our customers.
- To be acknowledged by Harris as a highly qualified resource for reliability assurance, product analysis, and electronic materials characterization.
- To successfully utilize the organization's talents through trained, empowered employees/employee team participation.
- To maintain an attitude of integrity, dignity and respect for all.

Strategy

- To provide quantitative assessments of product reliability focusing on the identification and timely elimination of design and processing deficiencies that degrade product performance and operating life expectancy.
- To provide systems for continuous improvement of reliability and quality through the assessment of existing processes, products, and packages.
- To perform product analysis as a means of problem solving and feedback to our customers, both internal and external.
- To exercise full authority over the internal qualifications of new products, processes, and packages.

The reliability organization is comprised of a team that possesses a broad cross section of expertise in these areas:

- Custom Military (Radiation Hardened)
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities
- Failure Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics, and service systems. These major systems are summarized below:

- A process and product development system known as ACT PTM (Applying Concurrent Teams to Product-To-Market) has been established. The ACT PTM philosophy is one of new product development through a team that pursues customer involvement. The team has the authority, responsibility, and training necessary to successfully bring the product to market. This not only includes product definition and design, but also all manufacturing capabilities as well.
- Standard test vehicles (over 100) have been developed for process characterization of wear-out failure mechanisms. These vehicles are used for conventional stresses (for modeling failure rates) and for wafer level reliability characterization during development.
- Common qualification standards have been established for all sites.
- A reliability monitoring system (also known as the Matrix monitoring system) is utilized for products in production to ensure ongoing reliability and verification of continuous improvement.
- The field return system is designed to handle a variety of customer issues in a timely manner. Product issues are often handled by routing the product into the PFAST (Product Failure Analysis Solution Team) system. Return authorizations (RAs) are issued where an entire lot of product needs to be returned to Harris. The Customer Return Services (CRS) group is responsible for the administration of this system (see Customer Return Services.)
- The PFAST system has been established to expedite failure analysis, failure root cause determination, and corrective actions for field returns. PFAST is a team effort involving many functional areas at all Harris sites. The purpose of this system is to enable Harris's Field Sales and Quality operations to properly route, track, and respond to our customer's needs as they relate to product analysis.

Design for Reliability (Wear-Out Characterization)

The concept of "Design for Reliability" focuses on moving reliability assessment away from tests on sample product to a point much earlier in the design cycle. Effort is directed at building in and verifying the reliability of a new process well before manufacture of the first shippable product that uses that technology. This gives these first new products a higher probability of success and achieves reduced product-to-market cycle times.

In practice, a set of standardized test vehicles containing special test structures are transferred to the new process using the layout ground rules specified for that process. Each test structure is designed for a specific wear-out failure mechanism. Highly accelerated stress tests are performed on these structures and the results can be extrapolated to customer use conditions. Generally, log-normal statistics are used to define wear-out distributions for the life prediction models. The results are used to establish reliability design ground rules and critical node lists for each process. These ground rules and critical nodes ensure that wear-out failures do not occur during the customer's projected use of the product.

Process/Product/Package Qualifications

Once the new process has successfully completed wear-out characterization, the final qualification consists of more conventional testing (e.g. biased life, storage life, temp cycle etc.). These tests are performed on the first new product designs (sampled across multiple wafer production lots). Successful completion of the final qualification tests concurrently qualifies the new process and the new products that were used in the qualification. Subsequent products designed within the now-established ground rules are qualified individually prior to introduction. New package configurations are also qualified individually prior to being available for use with new products.

Harris's qualification procedures are specified via controlled documentation and the same standard is used at Harris's sites worldwide. Figure 4 gives more information on the new process/product development and life cycle.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard product. Harris's continuing reliability monitoring program consists of three groups of stress tests, labeled Matrix I, II and III. Table 7 outlines the Matrix tests used to monitor plastic packaged ICs in Harris's off-shore assembly plants, where each wafer fab technology is sampled. Matrix I consists of highly accelerated, short duration (typically 48 hours) tests, sampled biweekly, which provide real-time feedback on product reliability. Matrix II consists of the more conventional, longer term stress-tests, sampled monthly, which are similar to those used for product qualification. Finally, Matrix III, performed monthly on each package style, monitors the mechanical reliability aspects of the package. Any failures occurring on the Matrix monitors are fully analyzed and the failure mechanisms identified, with containment and corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, to ensure that failure rates are continuously being reduced over time.

Reliability data, including the Matrix Monitor results, can be obtained by accessing our Reliability Engineering WWW Home Page at URL: http://rel.semi.harris.com or by contacting your local Harris sales office.

TABLE 7. PLASTIC PACKAGED IC MONITORING TESTS

MATRIX I

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	121°C, 100%RH, 15PSIG	96 Hours	45/5
Biased Life	175°C	48 Hours	45/5
Biased Life	125°C	48 Hours	45/5
HAST	135°C, 85% RH	48 Hours	45/5
Thermal Shock	-65°C to 150°C	200 Cycles	45/5

MATRIX II

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	121°C, 100%RH, 15PSIG	192 Hours	45/5
Biased Humidity	85°C, 85% RH	1000 Hours	45/5
Biased Life	125°C	1000 Hours	45/5
Dynamic Life	125°C	1000 Hours	45/5
Storage Life	150°C	1000 Hours	45/5
Temp. Cycle	-65°C to 150°C	1000 Cycles	45/5

MATRIX III

TEST	CONDITIONS	SAMPLE/LTPD
Brand Adhesion	MIL-STD-883/2015	15/15
Flammability	(UL-94 Vertical Burn)	11/20
Lead Fatigue	MIL-STD-883/2004	15/15
Physical Dimensions	MIL-STD-883/2016	11/20
Solderability	MIL-STD-883/2003	45/15

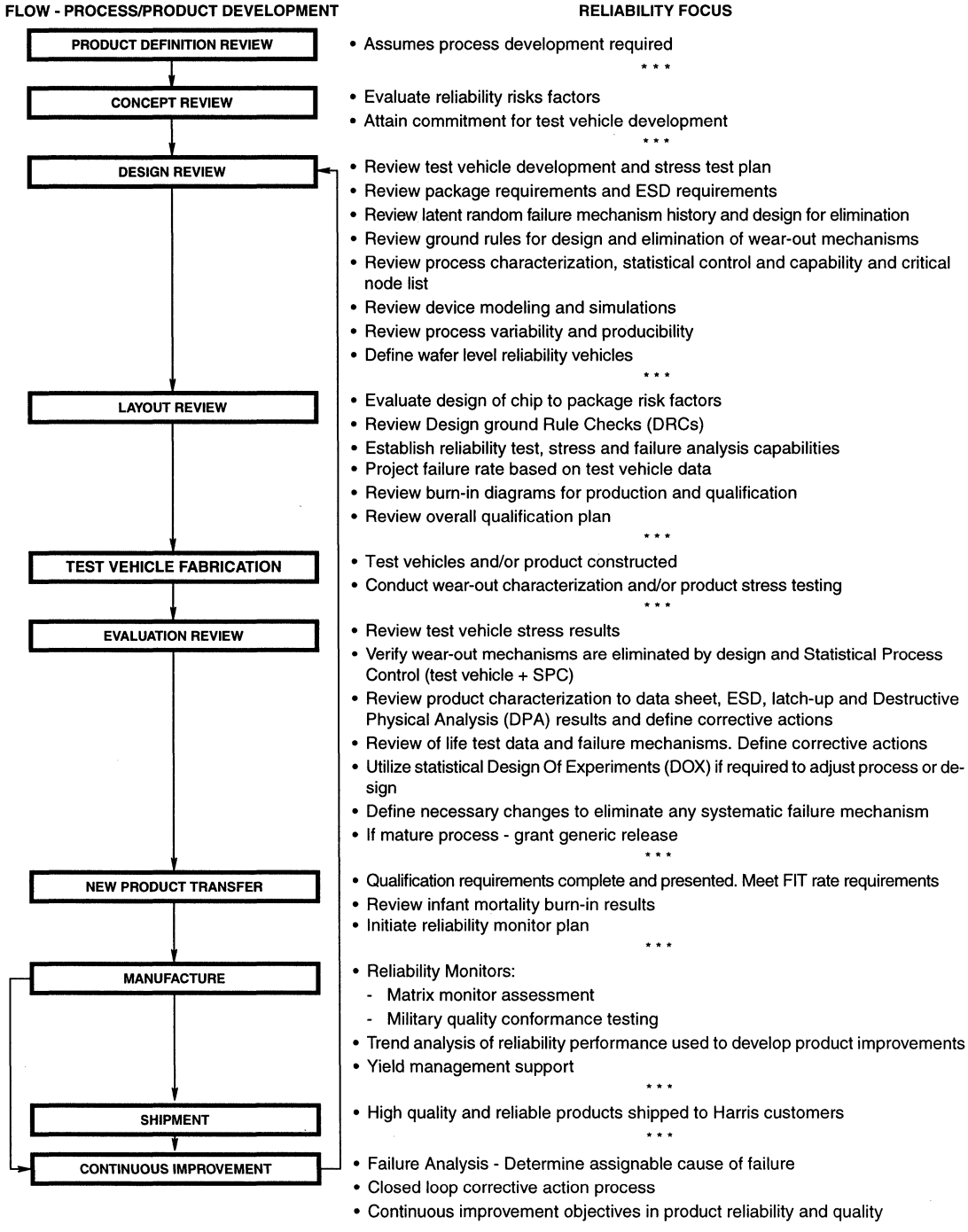


FIGURE 4. NEW PROCESS/PRODUCT DEVELOPMENT AND LIFE CYCLE

Customer Return Services

Harris places a high priority on resolving customer return issues. The Customer Return Services (CRS) department is responsible for determining the best manner to handle a return issue as illustrated in Figure 5.

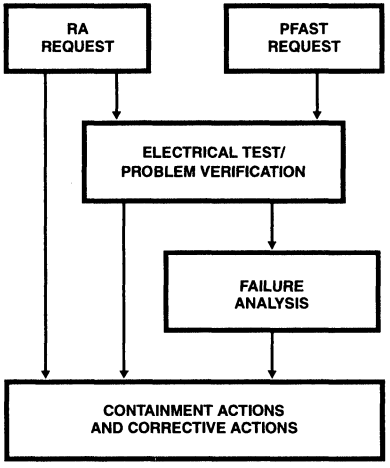


FIGURE 5. GENERAL RETURN FLOW

The diversity of return reasons requires that many different organizations be involved to test, analyze, and correct field return issues. The CRS group coordinates the responses from the supporting organizations to drive closure of issues within the customer response time requirements, see Table 7. The results from the work performed on customer returns are used to initiate corrective actions and continuous improvements within the factories. When the work on a return is completed, the customer is contacted to be certain all issues have been satisfactorily resolved.

The two methods used to return devices are by a RA (Return Authorization) request or by a PFAST (Product Failure Analysis Solution Team) request. The main difference between RA and PFAST is that the PFAST requests often require extensive analysis and a more formal response to the customer. All returns follow the same general procedure from the customer's perspective as seen in steps one to five of the customer return procedure.

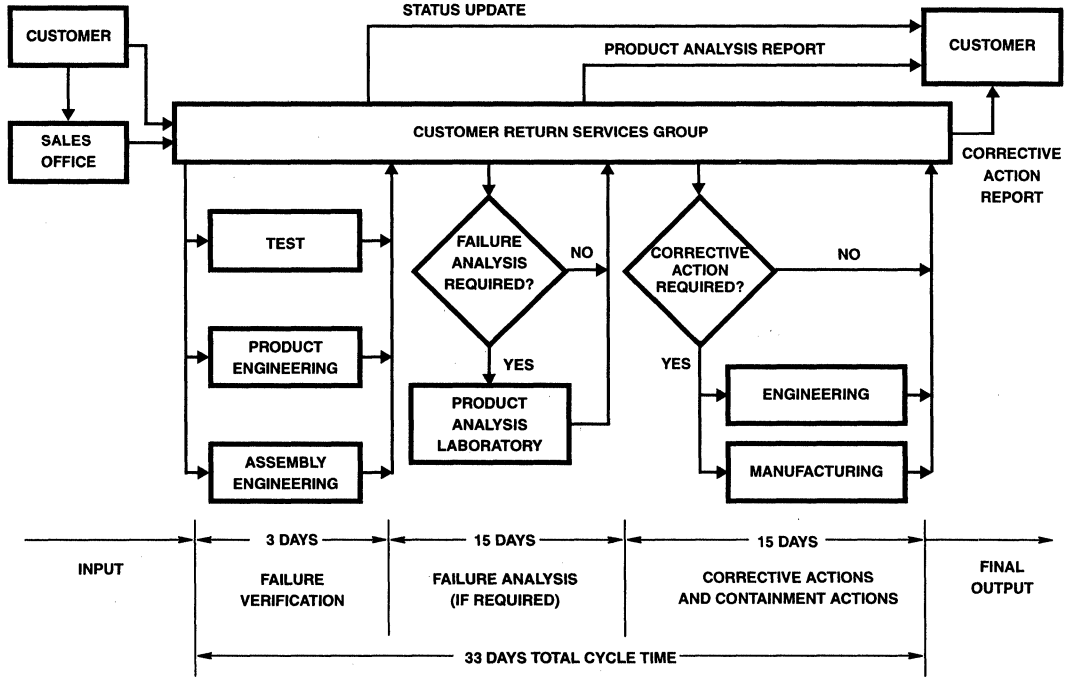
- **Step 1** - Customer or Sales office contacts the Customer Return Services department. If a return is to be routed into the PFAST system, then a PFAST Action Request (see the PFAST form in this section) needs to be completed to understand the customer's issue and direct the analysis efforts.
  - **Phone Number: (407)-724-7400**
  - **FAX Number: (407)-724-7658**
  - **Internet: creturn@huey.mis.semi.harris.com**
  - **PROFS: CRETURN**
- **Step 2** - The Customer Return Services department notifies all affected sales, factory, and engineering organizations of the issue.
- **Step 3** - When product is received, the issue is verified and any required analysis is performed. Where applicable, a preliminary analysis report is sent to the customer.
- **Step 4** - A determination of the root cause of failure initiates the corrective actions to address the source of the problem. A final corrective action report is sent to the customer if requested.
- **Step 5** - The Customer Return Services department contacts the customer to confirm that all issues have been handled properly and the customer is satisfied that the return is completed.

The RA request is used to return and replace an entire lot of product. The lot is returned to Harris for replacement or credit. Once the product is received various tests and evaluations will be performed to determine the appropriate actions that should be taken to resolve any problems or issues.

A PFAST request is used to return a small sample for analysis of a problem. The ultimate outcome of both types of requests is to determine corrective actions that would preclude the same problem occurring in the future. Where appropriate, a containment plan is also implemented to prevent a re-occurrence of the problem in the field. The customer return flow diagram (Figure 6) provides the typical activities and cycle times for processing a PFAST request..

TABLE 8. CUSTOMER RETURN SERVICES

CHARTER	MISSION	RESPONSIBILITIES
To resolve product quality issues while providing feedback to both external and internal customers to facilitate corrective actions and continuous improvement of the product.	To provide a single point interface between the customer and the factory for resolving technical problems, issues, and field returns.	1. Maintain customer return history. 2. Track returns through the factory. 3. Establish a history library of problems and corrective actions. 4. Ensure closure with customers.



NOTE: The days indicated are the typical number of 'working days' not calendar days. Analysis difficulty and the nature of the corrective actions may either improve or degrade the total cycle time.

FIGURE 6. CUSTOMER RETURN FLOW DIAGRAM

HARRIS SEMICONDUCTOR

PFAST ACTION REQUEST

(Product Failure Analysis Solution Team)

Request # _____

Date: _____

Originator _____	Customer _____
Company/Phone No. _____	Location _____
Device Type/Part No. _____	Customer's Reference No. _____
No. Samples Returned _____	Quantity Received _____

Instructions and requirements are on the back of this form.

Has Field Applications been contacted for assistance? ☐ No ☐ Yes - Who was contacted _____

SOURCE OF PROBLEM

(Enter the sequence of events in the boxes provided)

1. Visual/Mechanical
   - ☐ Describe _____
2. Incoming Test
   - ☐ Not Performed
   - ☐ 100% Tested
   - ☐ Sample Tested
   - No. Tested _____ No. of Rejects _____
   - Are results representative of previous lots?
   - ☐ YES ☐ NO
3. In Process/Manufacturing Failure
   - ☐ Board Test ☐ System Test
   - How many units failed? _____
   - Failed after _____hours of testing
   - Was unit retested at incoming inspection?
   - ☐ YES ☐ NO
   - Are results representative of previous lots?
   - ☐ YES ☐ NO
4. Field Failure
   - Failed after _____hours operation
   - Estimated failure rate_____ % per _____
   - End User_____ Location _____
   - Min. _____°C Ave. _____°C Max. _____°C
5. Other

ACTION REQUESTED BY CUSTOMER

Specific Action Requested (Contact PFAST Coordinator for other options)

- ☐ Test Sample for Correlation Only
- ☐ Test Sample for Product Return >$5k
- ☐ Failure Analysis
- ☐ Other

Impact of Failed Units on Customer's Situation: _____

Customer Contact with Specific Knowledge of Rejects

Name _____

Position _____ Phone_____

REASON FOR ELECTRICAL REJECT

(Where appropriate serialize units and specify for each)

Test Conditions Relating to Failure

Tester Used (Mfgr/Model) _____

Test Temperature _____

Test Time ☐ Continuous (T = _____sec) ☐ One Shot (T = _____sec)

Describe any observed condition to which failure appears sensitive _____

1. ☐ DC Failure
   - ☐ Open ☐ Short ☐ Leakage
   - ☐ Power Drain ☐ Input Level ☐ Output Level
   - Pin Number_____
2. ☐ AC Failure
   - Power Supply Voltages = _____V
   - Input Voltages V_{IH} = _____V V_{IL} = _____V
   - Pin Number_____
   - Failing characteristics _____
3. ☐ RAM and ROM Failures (ROM failures must be returned with a good master unit if failure analysis is requested).
   - Address of Failing Location _____
   - Describe Pattern Used (If not standard patterns, give very complete description including address sequence). _____
   - Include timing diagrams and circuit schematic if available.
   - ROM Programmer Used (If purchased unprogrammed) _____

Conformal Coating (Mfgr/Model) _____

Additional Comments:

FIGURE 7. PFAST ACTION REQUEST

INSTRUCTIONS FOR COMPLETING PFAST ACTION REQUEST FORM

The purpose of this form is to help us provide you with a more accurate, complete, and timely response to failures which may occur. Accurate and complete information is essential to ensure that the appropriate corrective action can be implemented. Due to this need for accurate and complete information, requests without a completed PFAST Action Request form will be returned.

Source of Problem:

This section requests the product flow leading to the failure. Mark an 'X' in the appropriate boxes up to and including the step which detected the failure. Also mark an 'X' in the appropriate box under "ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?" to indicate whether this is a rare failure or a repeated problem.

Example 1. No incoming electrical test was performed; the units were installed onto boards; the boards functioned correctly for two hours and then 1 unit failed. The customer rarely has a failure due to the Harris device.

Example 2. 100 out of the 500 units shipped were tested at incoming and all passed. The units were installed into boards and the boards passed. The boards were installed into the system and the system failed immediately when turned on. There were 3 system failures due to this part. The customer frequently has failures of this Harris device. The 3 units were not retested at incoming.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☒ NOT PERFORMED
   ☐ 100% TESTED ☐ SAMPLE TESTED
   NO. TESTED _____ NO. OF REJECTS _____
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☐ SYSTEM TEST
   HOW MANY UNITS FAILED? 1
   FAILED AFTER 2 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☒ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____°C AVE. _____°C MAX._____°C
5. OTHER _____

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☐ NOT PERFORMED
   ☐ 100% TESTED ☒ SAMPLE TESTED
   NO. TESTED 100 NO. OF REJECTS 0
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☒ SYSTEM TEST
   HOW MANY UNITS FAILED? 3
   FAILED AFTER 0 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____°C AVE. _____°C MAX._____°C
5. OTHER _____

Action Requested by Customer:

This section should be completed with the customer's expectations. This information is essential for an appropriate response.

Reason for Electrical Reject:

This section should be completed if the type of failure could be identified. If this information is contained in attached customer correspondence there is no need to transpose onto the PFAST Action Request form.

PFAST REQUIREMENTS

The value of returning failing products is in the corrective actions that are generated. Failure to meet the following requirements can cause erroneous conclusion and corrective action; therefore, failure to meet these requirements will result in the request being returned. Contact the local PFAST Coordinator if you have any questions.

Units with conformal coating should include the coating manufacturer and model. This is requested since the coating must be removed in order to perform electrical and hermeticity testing.

1. Units must be returned with proper ESD protection (ESD-safe shipping tubes within shielding box/bag or inserted into conductive foam within shielding box/bag). No tape, paper bags, or plastic bags should be used. This requirement ensures that the devices are not damaged during shipment back to Harris.
2. Units must be intact (lid not removed and at least part of each package lead present). This is a requirement since the parts must be intact in order to perform electrical test. Also, opening the package can remove evidence of the cause of failure and lead to an incorrect conclusion.
3. Programmable parts (ROMs, PROMs, UVEPROMs, and EEPROMs) must include a master unit with the same pattern. This requirement is to provide the pattern so all failing locations can be identified. A master unit is required if a failure analysis is requested.

FIGURE 7. PFAST ACTION REQUEST (Continued)

Product Analysis Lab

The Product Analysis Laboratory capabilities and charter encompass the isolation and identification of failure modes and mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. The primary activities of the Product Analysis Lab are electrical verification/characterization of the failure, package inspection/analysis, die inspection/analysis, and circuit isolation/probing. A variety of tools and techniques have been developed to ensure the accuracy and integrity of the product analysis. This section lists some of the tools and techniques that are employed during a typical analysis.

The electrical verification/characterization of devices failing electrical parameters is essential prior to performing an analysis. The information obtained from the electrical verification provides a direction for the analysis efforts. The following electrical verification/characterization equipment may be used to obtain electrical data on a device:

- ASIC Verification System
- Analog Test System
- Curve Tracer
- Mixed Signal/Telecom Test System
- Parametric Analyzer

Prior to die level analysis, package inspection and analysis are performed. These steps are performed routinely since valuable data may not be obtainable once the package is opened. The package inspection and analysis may require the use of some of the following lab equipment:

- X-ray
- C-mode Scanning Acoustic Microscope (C-SAM)
- Optical inspection microscopes
- Package opening tools and techniques

Once the device has been opened, die inspection and analysis can be performed. Depending on the type of failure, several tools and techniques may be used to identify the failure mechanism. Usually the faster and easier to use operations are performed first in an attempt to expedite the analysis. The list of equipment and techniques for performing die inspection and analysis is as follows:

- Optical microscopes
- Liquid crystal
- Emission microscope
- Scanning electron microscopes - SEM

The final step of circuit isolation is ready to be performed when an area of the circuit has been identified as the source of the problem through one of the previous analysis efforts. Circuit analysis is performed using the following probing and isolation tools:

- Mechanical probing
- Laser cutter and isolation
- E-beam probing
- Cross sectioning and chemical deprocessing

A typical analysis flow is shown in the Figure 8 below. The exact analysis steps and sequence are determined as the situation dictates. For the analysis to be conclusive, it is essential that the failure mechanism correlates to the initial product failure conditions. Some failure mechanisms require elemental and chemical analysis to identify the root cause within the manufacturing process. Elemental and chemical analysis tasks are sent to the Analytical Services Lab for further evaluation.

The results of each analysis are entered into a computer data base. This data base is used to search for specific types of problems, to identify trends, and to verify that the corrective actions were effective.

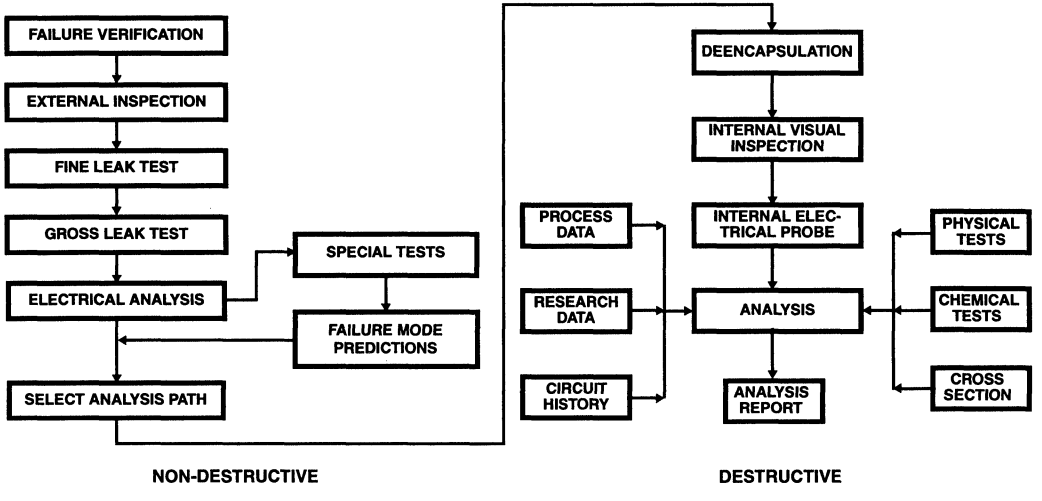


FIGURE 8. ANALYSIS SEQUENCE

Analytical Services Laboratory

Chemical and physical analysis of materials and processes is an integral part of Harris' Total Quality/Continuous Improvement efforts to build reliability into processes and products. Manufacturing operations are supported with real-time analyses to help maintain robust processes. Analyses are run in cooperation with raw material suppliers to help them provide controlled materials in dock-to-stock procurement programs.

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies.

The department also maintains ongoing working arrangements with commercial laboratories, universities, and equipment manufacturers to obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

Figures 9 and 10 show the capabilities of each area.

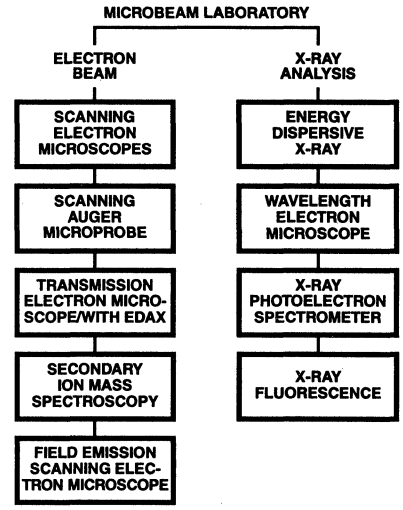


FIGURE 9. MICROBEAM LABORATORY

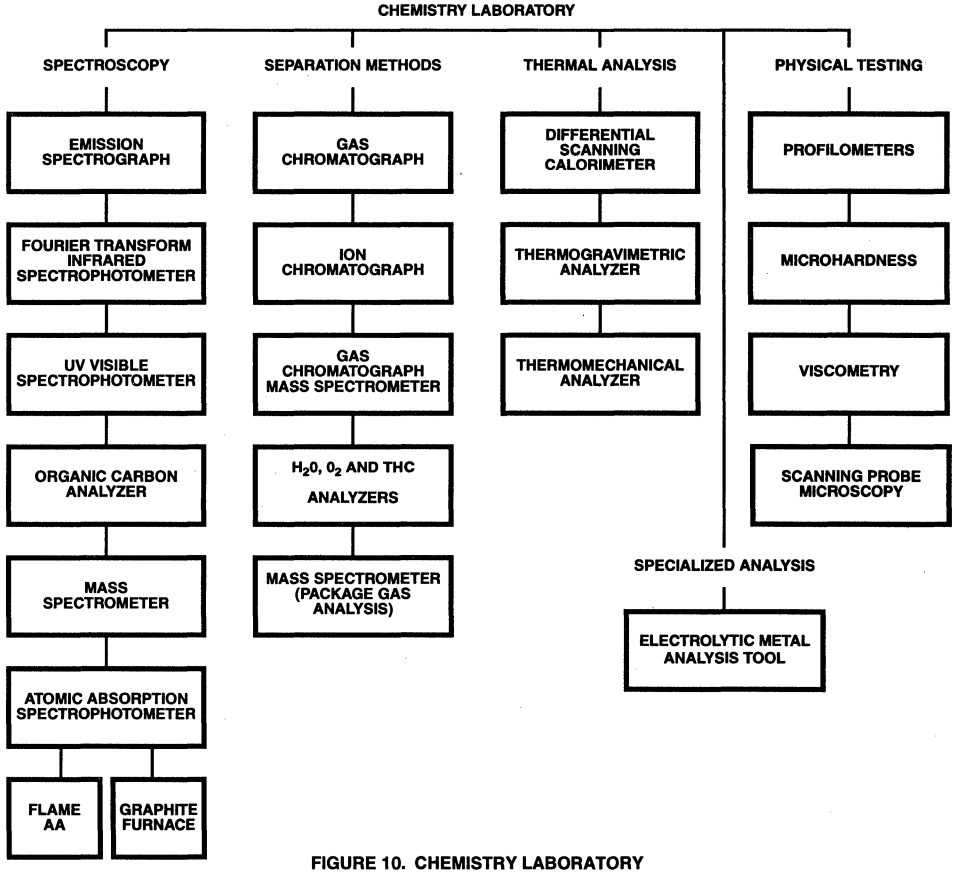


FIGURE 10. CHEMISTRY LABORATORY

Reliability Fundamentals and Calculation of Failure Rate

Table 9 defines some of the more important terminology used in describing the lifetime of integrated circuits. Of prime importance is the concept of "failure rate" and its calculation.

Failure Rate Calculations

Since reliability data can be accumulated from a number of different life tests with several different failure mechanisms, a comprehensive failure rate is desired. The failure rate calculation can be complicated if there are more than one failure mechanism in a life test, since the failure mechanisms are thermally activated at different rates The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum_{j=1}^{k} TDH_j \, AF_{ij}} \right] \times \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = number of distinct possible failure mechanisms

k = number of life tests being combined

x_i = number of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test $j, j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

$M = X^2_{(\alpha, 2r+2)}/2$
where,
X^2 = chi square factor for $2r + 2$ degrees of freedom
r = total number of failures (Σx_i)
α = risk associated with UCL;
i.e. $\alpha = (100\text{-UCL}(\%))/100$

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of 55°C has been popular. Harris Semiconductor Reliability Reports will derate to 55°C and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 9. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The early life failure rate is typically higher, decreases slightly, and then becomes relatively constant over time. The onset of wear-out will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution.
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Example: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more that 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{USE}} - \frac{1}{T_{STRESS}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln (t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln (t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 10. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3eV - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3eV - 0.5eV	HTOL and voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5eV - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation.
Mask Defects/Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL and oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

Harris Semiconductor

TechBrief

No. TB52 January 1994

Harris Digital

Electrostatic Discharge Control: A Guide To Handling Integrated Circuits

This paper discusses methods and materials recommended for protection of ICs against ESD damage or degradation during manufacturing operations vulnerable to ESD exposure. Areas of concern include dice prep and handling, dice and package inspection, packing, shipping, receiving, testing, assembly and all operations where ICs are involved.

All integrated circuits are sensitive to electrostatic discharge (ESD) to some degree. Since the introduction of integrated circuits with MOS structures and high quality junctions, safe and effective means of handling these devices have been of primary importance.

If static discharge occurs at a sufficient magnitude, 2kV or greater, some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. Avoiding any damage or degradation by ESD when handling devices during the manufacturing flow is therefore essential.

ESD Protection and Prevention Measures

One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry.

In areas where ICs are being handled, certain equipment should be utilized to reduce the damaging effects of ESD. Typically, equipment such as grounded work stations, conductive wrist straps, conductive floor mats, ionized air blowers and conductive packaging materials are included in the IC handling environment. Any time an individual intends to handle an IC, in any way, they must insure they have been grounded to eliminate circuit damage.

Grounding personnel can, practically, be performed by two methods. First, grounded wrist straps which are usually made of a conductive material, such as Velostat or metal. A resistor value of 1 megohm (1/2 watt) in series with the strap to ground completes a discharge path for ESD when the operator wears the strap in contact with the skin. Another method is to insure direct physical contact with a grounded, conductive work surface.

This consists of a conductive surface like Velostat, covering the work area. The surface is connected to a 1 megohm (1/2 watt) resistor in series with ground.

In addition to personnel grounding, areas where work is being performed with ICs, should be equipped with an ionized air blower. Ionized air blowers force positive and negative ions simultaneously over the work area so that any nonconductors that are near the work surface would have their static charge neutralized before it would cause device damage or degradation.

Relative humidity in the work area should be maintained as high as practical. When the work environment is less than 40% RH, a static build-up condition can exist on nonconductors allowing stored charges to remain near the ICs causing possible static electricity discharge to ICs.

Integrated circuits that are being shipped or transported require special handling and packaging materials to eliminate ESD damage. Dice or packaged devices should be in conductive carriers during all phases of transport and handling. Leads of packaged devices can be shorted by tubular metallic carriers, conductive foam or foil.

Do's and Don'ts for Integrated Circuit Handling

Do's

Do keep paper, nonconductive plastic, plastic foams and films or cardboard off the static controlled conductive bench top. Placing devices, loaded sticks or loaded burn-in boards on top of any of these materials effectively insulates them from ground and defeats the purpose of the static controlled conductive surface.

Do keep hand creams and food away from static controlled conductive work surfaces. If spilled on the bench top, these materials will contaminate and increase the resistivity of the work area.

Do be especially careful when using soldering guns around conductive work surfaces. Solder spills and heat from the gun may melt and damage the conductive mat.

Do check the grounded wrist strap connections daily. Make certain they are snugly fitted before starting work with the product.

Do put on grounded wrist strap before touching any devices. This drains off any static buildup from the operator.

Do know the ESD caution symbols.

Do remove devices or loaded sticks from shielding bags only when grounded via wrist strap at grounded work station. This also applies when loading or removing devices from the antistatic sticks or the loading on or removing from the burn-in boards.

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Do wear grounded wrist straps in direct contact with the bare skin never over clothing.

Do use the same ESD control with empty burn-in boards as with loaded boards if boards contain permanently mounted ICs as part of driver circuits.

Do insure electrical test equipment and solder irons at an ESD control station are grounded and only uninsulated metal hand tools be used. Ordinary plastic solder suckers and other plastic assembly aids shall not be used.

Do use ionizing air blowers in static controlled areas when the use of plastic (nonconductive) materials cannot be avoided.

Don'ts

Don't allow anyone not grounded to touch devices, loaded sticks or loaded burn-in boards. To be grounded they must be standing on a conductive floor mat with conductive heel straps attached to footwear or must wear a grounded wrist strap.

Don't touch the devices by the pins or leads unless grounded since most ESD damage is done at these points.

Don't handle devices or loaded sticks during transport from work station to work station unless protected by shielding bags. These items must never be directly handled by anyone not grounded.

Don't use freon or chlorinated cleaners at a grounded work area.

Don't wax grounded static controlled conductive floor and bench top mats. This would allow buildup of an insulating layer and thus defeating the purpose of a conductive work surface.

Don't touch devices or loaded sticks or loaded burn-in boards with clothing or textiles even though grounded wrist strap is worn. This does not apply if conductive coats are worn.

Don't allow personnel to be attached to hard ground. There must always be 1 megohm series resistance (1/2 watt between the person and the ground).

Don't touch edge connectors of loaded burn-in boards or empty burn-in boards containing permanently mounted driver circuits when not grounded. This also applies to burn-in programming cards containing ICs.

Don't unload stick on a metal bench top allowing rapid discharge of charged devices.

Don't touch leads. Handle devices by their package even though grounded.

Don't allow plastic "snow or peanut" polystyrene foam or other high dielectric materials to come in contact with devices or loaded sticks or loaded burn-in boards.

Don't allow rubber/plastic floor mats in front of static controlled work benches.

Don't solvent-clean devices when loaded in antistatic sticks since this will remove antistatic inner coating from sticks.

Don't use antistatic sticks for more than one throughput process. Used sticks should not be reused unless recoated.

Recommended Maintenance Procedures

Daily

Perform visual inspection of ground wires and terminals on floor mats, bench tops, and grounding receptacles to ensure that proper electrical connections via 1 megohm resistor (1/2 watt) exist.

Clean bench top mats with a soft cloth or paper towel dampened with a mild solution of detergent and water.

Weekly

Damp mop conductive floor mats to remove any accumulated dirt layer which causes high resistivity.

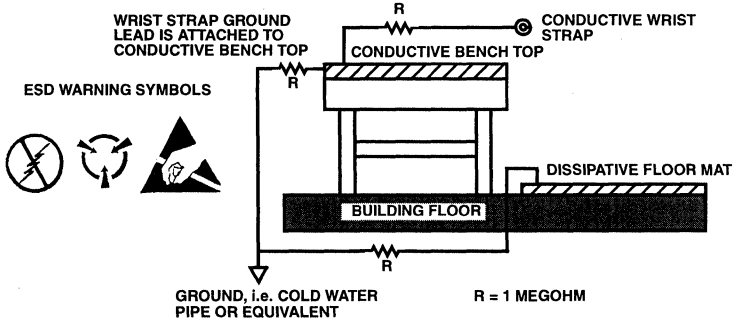
Annually

Replace nuclear elements for ionized air blowers.

Review ESD protection procedures and equipment for updating and adequacy.

Static Controlled Work Station

The figure below shows an example of a work bench properly equipped to control electrostatic discharge. Note that the wrist strap is connected to a 1 megohm resistor. This resistor can be omitted in the setup if the wrist strap has a 1 megohm assembled on the cable attached.



LINEAR 10

APPLICATION NOTES, ABSTRACTS AND SPICE MODEL LISTING

Application Notes, Abstracts and Spice Model Listing (Continued)

Application Note Abstracts

AN #	TITLE	ABSTRACT
007	Using the 8048/8049 Monolithic Log-Anti-Log Amplifiers	Describes in detail the operation of the ICL8048 logarithmic amplifier, and its counterpart, the ICL8049 anti-log amp.
013	**Everything You Always Wanted to Know About the 8038**	This note includes 17 of the most asked questions regarding the use of the ICL8038.
040	A Precision Four Quadrant Multiplier - The 8013	Describes, in detail, the operation of the ICL8013 analog multiplier. Included are multiplication, division, and square root applications.
053	**The ICL7650 - A New Era in Glitch-Free Chopper Stabilizer Amplifiers**	A brief discussion of the internal operation of the ICL7650, followed by an extensive application section including amplifiers, comparators, log-amps, pre-amps, etc.
509	A Simple Comparator Using The HA-2620	Performance characteristics, application schematics, output parameter control methods.
514	**The HA-2400 PRAM Four Channel Operational Amplifier**	HA-2400 Programmable Analog Microcircuit description, frequency compensation, applications (analog multiplexer, non-inverting programmable gain amplifier, inverting programmable gain amplifier, programmable attenuator, programmable adder-subtractor, phase selector, phase detector, synchronous rectifier, balanced modulator, integrator, ramp generator, track and hold, sample and hold, sine wave oscillator, multivibrator, active filter, programmable power supply, comparator, multiplying D/A converter).
515	Operational Amplifier Stability: Input Capacitance Considerations	Input capacitance and stability, capacitive feedback compensation, guidelines for compensation requirements.
517	Applications of a Monolithic Sample and Hold Amplifier	General Sample and Hold information and fourteen specific applications, including filtered Sample and Hold DAC de-glitcher, Integrate-Hold-Reset, gated op amp, etc.
519	**Operational Amplifier Noise Prediction**	Noise model and equations, procedure for computing total output noise, example, broadband noise measurement, spot noise prediction techniques, typical spot noise curves, popcorn noise discussion.
525	HA-5190/5195 Fast Settling Operational Amplifier	Internal schematic, prototyping considerations, frequency compensation, performance enhancement methods, applications.
526	Video Applications for the HA-5190/5195	Video applications, video response tests, S/N ratio measurements, power supply requirements temperature considerations, design hints, prototyping tips, RF AGO amplifier, DC gain controlled video amplifier.
538	Monolithic Sample/Hold Combines Speed and Precision	Description and electrical specifications for the HA-5320 Sample/Hold Amplifier, explanation of errors sources, and HA-5320 applications.
540	HA-5170 Precision Low Noise JFET Input Operation Amplifier	Internal design and technology, JFET noise discussion, trimming of offset voltage, single op amp Instrumentation Amplifier, sine wave oscillator, high impedance transducer interface, current source/sink and current sense circuits.
541	Using HA-2539 or HA-2540 Very High Slew Rate, Wideband Operational Amplifier	Prototyping considerations, output short circuit protection, offset voltage adjustment, frequency compensation, composite amplifier scheme, DC error reduction, boosting output current, increasing output signal swing, cascade amplifier, video gain block, high frequency oscillator, wideband signal splitter.
544	Micropower Op Amp Family, HA-514X	Operation, noise performance, applications (remote sensor loop transmitter, charge pool power supply, low power microphone preamplifier, AGO with squelch control, Wein bridge oscillator, bar code scanner, monostable multivibrator).
546	A Method of Calculating HA-2625 Gain Bandwidth Product vs Temperature	A method of calculating Gain Bandwidth product performance versus temperature for the HA-2625 Op Amp.
548	**A Designer's Guide for the HA-5033 Video Buffer**	Operation, video performance, video parameter specifications, Y parameters, applications (flash converter pre-driver, coaxial line driver, video gain block, high speed sample and hold, audio drivers, crystal oscillator).

NOTE: Bold type indicates Appnote is included in this data book.

See pages i, ii for information on Ordering Literature

Application Note Abstracts

AN #	TITLE	ABSTRACT
550	Using the HA-2541	Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (Wein bridge oscillator, high power gain stage, video stage with clamp, multiplexer/demultiplexer, disk drive write amplifier, gain programmable amp, composite amp).
551	**Recommended Test Procedures for Operational Amplifiers**	Operational amplifier test procedures for offset voltage, bias current, offset current, power supply rejection ratio, common mode rejection ratio, output voltage swing, output current, open loop gain, slew rate, full power bandwidth, transient response, settling time, GBP, phase margin, noise voltage and current, and channel separation.
552	Using the HA-2542	Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (multi-channel security system, unbalanced coaxial driver, flash converter driver, programmable power supply, bridge load driver, high current stage, differential line driver, DC motor speed control).
553	Using the HA-5147/5137/ 5127	Construction and operation, low noise design applications (instrumentation amplifier bridge sensor, multiplexer, precision threshold detector, audio driver, NAB amplifier, multivibrator, programmable gain stage, log amp, professional mixer).
554	Low Noise Family HA-5101/5102/5104/5112/ 5114	Low noise design, operation, applications (Electronic scales, programmable attentuator, Baxandal circuit, RIAA amplifier, NAB preamplifier, microphone amplifier, standard and simple biquads, professional mixer.
556	Thermal Safe-Operating-Areas for High Current Op Amps	Thermal management equations and curves indicating areas of V_{OUT} and I_{OUT} for safe operation. Also, the effects of packaging and heat sinking are examined.
5290	General Purpose Op Amps	Discusses various uses of op amps.
5296	CA3018	Transistor Array
5337	CA3028	RF amplifiers in the HF and VHF ranges.
5766	CA3020	Multipurpose wideband power amplifiers
6048	CA3094	Programmable power switch/amplifier.
6077	CA3094	OTA with power capability.
6247	CA3126	Chroma processing IC using sample and hold circuit techniques.
6257	CA3089	FM IF Subsystem
6386	CA3130	Understanding BiMOS op amps.
6459	CA3130	Why and how to use the BiMOS op amp.
6472	CA3126	A chrominance demodulator IC with dynamic flesh correction.
6668	**CA3080 OTA**	What is an Operational Transconductance Amplifier (OTA)? Circuit description plus numerous application examples.
6669	CA3240	BiMOS op amp mates directly to system sensors.
6732	Noise Measurement	Measurement of burst noise and "popcorn" noise in ICs.
6818	CA3280 Dual OTA	OTA simplifies complex analog designs.
7127	CA3420	BiMOS amplifier circumvents low voltage limitations.
8636	Video Devices	Discusses advanced video speed switches, multiplexers, cross points and buffer amplifiers.
8707	CA3450	Single chip video line driver-high speed op amp.
8742	CD22402	Sync Generator
8811	CA5470	BiMOS-E process enhances quad op amp.
9202	**Using the HFA1100, HFA1130 Evaluation Fixture**	Uses for the HFA11XX Evaluation Board, and performance examples.
9305	**HA5020 Operational Amplifier Feedback Resistor Selection**	Discusses a method for calculating the optimum feedback resistor value when using a current feedback amplifier at closed loop gains grater than 1.
9313	**Circuit Considerations In Imaging Applications**	Discusses the analog input section of an image processing system. Presents video formats, analog circuit design considerations, etc.
9314	**Harris UHF Pin Drivers**	Description, use of, and applications for the HFA5250 and HFA5251.

NOTE: Bold type indicates Appnote is included in this data book.

See pages i, ii for information on Ordering Literature

AN #	TITLE	ABSTRACT
9315	**RF Amplifier Design Using HFA3046/3096/3127/3128 Transistor Arrays**	Sample RF amplifier designs including layout techniques and performance results.
9317	**Micropower Clock Oscillator and OP Amps Provide System Control for Battery Operated Circuits**	Using HA7210 in a control circuit to switch a battery powered digital system from sleep mode (ultra low power) to active when an external event (sound, pressure, etc.) is detected.
9334	**Improving Start-up Time at 32kHz for the HA7210 Low Power Crystal Oscillator**	Techniques to speed up the oscillator start-up time when operating the HA7210 at low power settings.
9415	**Feedback, Op Amps, and Compensation**	Basic feedback theory and op amp fundamentals.
9420	**Current Feedback Amplifier Theory**	In depth analysis of Current feedback amplifiers.
9502	**Oscillator Produces Quadrature Waves**	Using a quad op amp to implement an RC oscillator producing quadrature outputs.
9503	**Low Output Impedance MUX**	Amplifiers with output disable functions implement muxes to drive low impedance loads.
9507	**Video Cable Drivers Save Board Space, Increase Bandwidth**	Limitations of long cables on video circuit performance, and use of novel video buffers to counteract cable limitations and save board space.
9508	**Video Multiplexer Delivers Lower Signal Degradation**	Implementation of a 4:1, cable driving, video mux using quad op amps featuring an output disable function.
9510	**Basic Analog for Digital Designers**	Analog refresher for engineers who haven't worked with analog circuits since college.
9513	**Component Video Sync Formats**	Discussion of video sync signals and sync formats.
9514	**Video Amp with Sync Stripper and DC Restore**	Use of the HFA1103 as a component video, sync stripping, amplifier.
9515	**Multiplier Improves the Dynamic Range of Echo Systems (HA-2556, HA-5177)**	Implementation of a time-gain amplifier using an analog multiplier.
9516	**Adjustable Bandpass or Bandreject Filter (HA-2841)**	Describes an active filter with easily adjusted center frequency, symmetrical skirts, and 40dB of attenuation (band reject) or gain (band pass).
9523	**Evaluation Programs for SPICE Op Amp Models**	Discussion of standard PSPICE programs for evaluating op amp models. Programs are given to simulate AC and transient responses as well as DC performance.
9524	**HFA1212 Dual Video Buffer Forms Differential Line Driver/Receiver**	Using a novel dual buffer to implement differential functions minimizes the number of external components required.
9528	**900MHz Down Converter Consumes Little Power (HFA3101)**	Using the HFA3101 transistor array to implement a battery powered 900MHz down converter.
9536	**PSPICE Performs Op Amp Open Loop Stability Analysis**	Using a simulator to perform a stability analysis makes a difficult task easier.
9621	**Comparison of Current Feedback Op Amp Spice Models**	All op amp macro models aren't equal. This Application Note compares models from several vendors.
9641	**High-Frequency VGA Has Digital Control**	Utilizing the HFA3102 to implement a Variable Gain amplifier with the HI5731 providing digital gain control.
9653	**Use and Application of Output Limiting Amplifiers (HFA1115, HFA1130, HFA1135)**	Discussion of Input Limiting vs Output Limiting amplifiers. Description of output limiting circuitry and resultant inaccuracies. Application examples: A/D input protection, 2ns T_R Comparators, AM Modulator, Soft Clipping Circuit.
TB334	**Guidelines for Soldering Surface Mount Components to PC Boards**	Discussion of the most common techniques for mounting SMDs to PC boards.

NOTE: Bold type indicates Appnote is included in this data book.

See pages i, ii for information on Ordering Literature

SPICE Model Listing

PART NUMBER	DESCRIPTION
CA3227	3.0GHz NPN Arrays (See Data Sheet for Model)
CA3246	3.0GHz NPN Arrays (See Data Sheet for Model)
HA-2500	Precision, High Slew Rate
HA-2502	Precision, High Slew Rate
HA-2510	High Slew Rate
HA-2512	High Slew Rate
HA-2520	+3 Stable, High Slew Rate
HA-2522	+3 Stable, High Slew Rate
HA-2539	Very High Slew Rate, Wideband, +10 Stable
HA-2540	Wideband, Fast Settling, +10 Stable
HA-2541	Wideband, Fast Settling, Unity Gain Stable
HA-2542	Wideband, High Slew Rate, High Output Current, +2 Stable
HA-2544	Precision, High Slew Rate, Unity Gain Stable
HA-2548	Precision, High Slew Rate, Wideband, +5 Stable
HA-2600	Wideband, High Input Impedance
HA-2602	Wideband, High Input Impedance
HA-2620	Very Wideband, Uncompensated, +5 Stable
HA-2622	Very Wideband, Uncompensated, +5 Stable
HA-2839	Very High Slew Rate, Wideband, +10 Stable
HA-2840	Very High Slew Rate, Wideband, +10 Stable
HA-2841	Wideband, Fast Settling, Unity Gain Stable, Video
HA-2842	Wideband, High Slew Rate, High Drive, Video, +2 Stable
HA-2850	Low Power, High Slew Rate, Wideband, +10 Stable
HA-5002	Wideband, High Slew Rate Buffer

PART NUMBER	DESCRIPTION
HA-5004	100MHz Current Feedback Video Amplifier
HA-5013	Triple, 125MHz Current Feedback Video Amplifier
HA-5020	100MHz Current Feedback Video Amplifier with Output Disable Function
HA-5022	Dual, 125MHz Current Feedback Video Amplifier, with Output Disable Function
HA-5023	Dual, 125MHz Current Feedback Video Amplifier
HA-5024	Quad, 125MHz Current Feedback Video Amplifier, with Output Disable Function
HA-5025	Quad, 125MHz Current Feedback Video Amplifier
HA-5033	Video Buffer
HA-5101	Low Noise, High Performance
HA-5102	Dual, Low Noise, High Performance
HA-5104	Quad, Low Noise, High Performance
HA-5112	Dual, Low Noise, High Performance, +10 Stable
HA-5114	Quad, Low Noise, High Performance, +10 Stable
HA-5127	Low Noise, Precision, Unity Gain Stable
HA-5137	Low Noise, Precision, +5 Stable
HA-5147	Low Noise, Precision, +10 Stable
HA-5190	Wideband, Fast-settling, +5 Stable
HA-5221	Low Noise, Wideband, Precision
HA-5222	Dual, Low Noise, Wideband, Precision
HFA1100*	850MHz Current Feedback Amplifier
HFA3046, HFA3096, HFA3127, HFA3128	8GHz NPN, 5.5GHz PNP Arrays

* Macromodel is on disk but App Note does not exist.

Harris Semiconductor

APPNOTE

No. AN013.1 November 1996

Harris Linear

Everything You Always Wanted To Know About The ICL8038

Author: Bill O'Neil

Introduction

The 8038 is a function generator capable of producing sine, square, triangular, sawtooth and pulse waveforms (some at the same time). Since its introduction, marketing and application engineers have been manning the phones explaining the care and feeding of the 8038 to customers worldwide. This experience has enabled us to form articulate responses to the most frequently asked questions. So, with data sheet and breadboard in hand, read on and be enlightened.

Question 1

I want to sweep the frequency externally but can only get a range of 100:1 (or 50:1, or 10:1). Your data sheet says 1000:1. How much sweep range can I expect?

Answer

Let's look at what determines the output frequency. Start by examining the circuit schematic at pin 8 in the upper left hand corner. From pin 8 to pin 5 we have the emitter-base of NPN Q_1 and the emitter-base of PNP Q_2. Since these two diode drops cancel each other (approximately), the potential at pins 8, 5, and 4 are the same. This means that the voltage from V+ to pin 8 is the same as the voltage across external resistors R_A and R_B. This is a textbook example of a voltage across two resistors which produce two currents to charge and discharge a capacitor between two fixed voltages. This is also a linear system. If the voltage across the resistors is dropped from 10V to 1V, the frequency will drop by 10:1. Changing from 1V to 0.1V will also change the frequency by 10:1. Therefore, by causing the voltage across the external resistors to change from say 10V to 10mV, the frequency can be made to vary at least 1000:1. There are, however, several factors which make this large sweep range less than ideal.

Question 2

You say I can vary the voltage on pin 8 (FM sweep input) to get this large range, yet when I short pin 8 to V+ (pin 6), the ratio is only around 100:1.

Answer

This is often true. With pin 8 shorted to V+, a check on the potentials across the external R_A and R_B will show 100mV or more. This is due to the V_{BE} mismatch between Q_1 and Q_2 (also Q_1 and Q_3) because of the geometries and current levels involved. Therefore, to get smaller voltages across these resistors, pin 8 must be raised above V+.

Question 3

How can I raise pin 8 above V+ without a separate power supply?

Answer

First of all, the voltage difference need only be a few hundred millivolts so there is no danger of damaging the 8038. One way to get this higher potential is to lower the supply voltage on the 8038 and external resistors. The simplest way to do this is to include a diode in series with pin 6 and resistors R_A and R_B. See Figure 1. This technique should increase the sweep range to 1000:1.

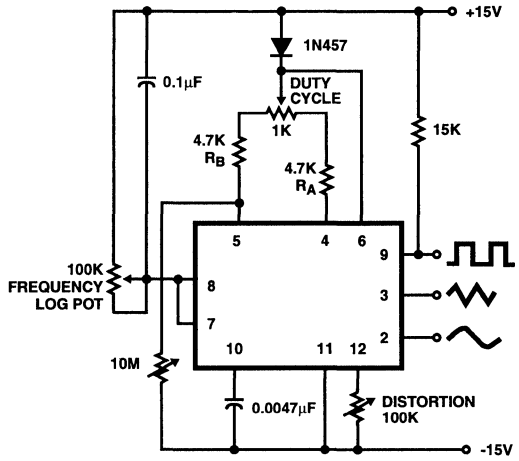


FIGURE 1. VARIABLE AUDIO OSCILLATOR, 20Hz TO 20kHz

Question 4

O.K., now I can get a large frequency range, but I notice that the duty cycle and hence my distortion changes at the lowest frequencies.

Answer

This is caused partly by a slight difference in the V_{BE}s of Q_2 and Q_3. In trying to manufacture two identical transistors, it is not uncommon to get V_{BE} differences of several millivolts or more. In the standard 8038 connection with pins 7 and 8 connected together, there are several volts across R_A and R_B and this small mismatch is negligible. However, in a swept mode

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with the voltage at pin 8 near V+ and only tens of millivolts across R_A and R_B, the V_{BE} mismatch causes a larger mismatch in charging currents, hence the duty cycle changes. For lowest distortion then, it is advisable to keep the minimum voltage across R_A and R_B around 100mV. This would of course, limit the frequency sweep range to around 100:1.

Question 5

I have a similar duty cycle problem when I use high values of R_A and R_B. What causes this?

Answer

There is another error term which becomes important at very low charge and discharge currents. This error current is the emitter current of Q_7. The application note on the 8038 gives a complete circuit description, but it is sufficient to know that the current charging the capacitor is the current in R_A which flows down through diode Q_9 and into the external C. The discharge current is the current in R_B which flows down through diode Q_8. Adding to the Q_8 current is the current of Q_7 which is only a few microamperes. Normally, this Q_7 current is negligible, but with a small current in R_B, this current will cause a faster discharge than would be expected. This problem will also appear in sweep circuits when the voltage across the external resistors is small.

Question 6

How can I get the lowest distortion over the largest frequency sweep range.

Answer

First of all, use the largest supply voltage available (±15V or +30V is convenient). This will minimize V_{BE} mismatch problems and allow a wide variation of voltage on pin 8. The potential on pin 8 may be swept from V_{CC} (and slightly higher) to 2/3 V_{CC} +2V) where V_{CC} is the total voltage across the 8038. Specifically for ±15V supplies (+30V), the voltage across the external resistors can be varied from 0V to nearly 8V before clipping of the triangle waveform occurs.

Second, keep the maximum currents relatively large (1mA or 2mA) to minimize the error due to Q_7. Higher currents could be used, but the small geometry transistors used in the 8038 could give problems due to $V_{CE(SAT)}$ and bulk resistance, etc.

Third, and this is important, use two separate resistors for R_A and R_B rather than one resistor with pins 4 and 5 connected together. This is because transistors Q_2 and Q_3 form a differential amplifier whose gain is determined by the impedance between pins 4 and 5 as well as the quiescent current. There are a number of implications in the differential amplifier connection (pins 4 and 5 shorted). The most obvious is that the gain determines the way the currents split between Q_2 and Q_3. Therefore, any small offset or differential voltage will cause a marked imbalance in the charge and discharge currents and hence the duty cycle. A more subtle result of this connection is the effective capacitance at pin 10. With pins 4 and 5 connected together, the "Miller Effect" as well as the compound transistor connection of Q_3 and Q_5 can produce several hundred picofarads at pin 10, seriously limiting the highest frequency of oscillation. The effective capacitance would have to be considered important in determining what value of external C would result in a particular frequency of oscillation. The single resistor connection is fine for very simple circuits, but where performance is critical, the two separate resistors for R_A and R_B are recommended.

Finally, trimming the various pins for lowest distortion deserves some attention. With pins 7 and 8 connected together and the pot at pin 7 and 8 externally set at its maximum, adjust the ratio of R_A and R_B for 50% duty cycle. Then adjust a pot on pin 12 or both pins 1 and 12 depending on minimum distortion desired. After these trims have been made, set the voltage on pin 8 for the lowest frequency of interest. The principle error here is due to the excess current of Q_7 causing a shift in the duty cycle. This can be partially compensated for by bleeding a small current away from pin 5. The simplest way to do this is to connect a high value of resistance (10MΩ to 20MΩ) from pin 5 to V- to bring the duty cycle back to 50%. This should result in a reasonable compromise between low distortion and large sweep range.

Question 7

This waveform generator is a piece of junk. The triangle wave is non-linear and has large glitches when it changes slope.

Answer

You're probably having trouble keeping the constant voltage across R_A and R_B really constant. The pulse output on pin 9 puts a moderate load on both supplies as it switches current on and off. Changes in the supply reflect as variations in charging current, hence non-linearity. Decoupling both power supply pins to ground right at the device pins is a good idea. Also, pins 7 and 8 are susceptible to picking up switching transients (this is especially true on printed circuit boards where pins 8 and 9 run side by side). Therefore, a capacitor (0.1μF or more) from V+ to pin 8 is often advisable. In the case when the pulse output is not required, leave pin 9 open to be sure of minimizing transients.

Question 8

What is the best supply voltage to use for lowest frequency drift with temperature?

Answer

The 8038AM, 8038AC, 8038BM and 8038BC are all temperature drift tested at V_{CC} = +20V (or ±10V). A curve in the lower right hand corner of Page 4 of the data sheet indicates frequency versus temperature at other supply voltages. It is important to connect pins 7 and 8 together.

Question 9

Why does connecting pin 7 to pin 8 give the best temperature performance?

Answer

There is a small temperature drift of the comparator thresholds in the 8038. To compensate for this, the voltage divider at pin 7 uses thin film resistors plus diffused resistors. The different temperature coefficients of these resistors causes the voltage at pins 7 and 8 to vary 0.5mV/°C to maintain overall low frequency drift at V_{CC} = 20V. At higher supply voltages, e.g., ±15V (+30V), the threshold drifts are smaller compared with the total supply voltage. In this case, an externally applied constant voltage at pin 8 will give reasonably low frequency drift with temperature.

Question 10

Your data sheet is very confusing about the phase relationship of the various waveforms.

Answer

Sorry about that! The thing to remember is that the triangle and sine wave must be in phase since one is derived from the other. A check on the way the circuit works shows that the pulse waveform on pin 9 will be high as the capacitor charges (positive slope on the triangle wave) and will be low during discharge (negative slope on the triangle wave).

The latest data sheet corrects the photograph Figure 7 on Page 5 of the data sheet. The 20% duty cycle square wave was inverted, i.e., should be 80% duty cycle. Also, on that page under "Waveform Timing" the related sentences should read "R_A controls the rising portion of the triangle and sine-wave and the 1 state of the square wave." Also, "the falling portion of the triangle and sine wave and the 0 state of the square wave is:"

Question 11

Under Parameter Test Conditions on Page 3 of your 8038 data sheet, the suggested value for Min and Max duty cycle adjust don't seem to work.

Answer

The positive charging current is determined by R_A alone since the current from R_B is switched off. (See 8038 Application Note AN012 for complete circuit description.) The negative discharge current is the ***difference*** between the R_A current and twice the R_B current. Therefore, changing R_B will affect only the discharge time, while changing R_A will affect both charge and discharge times. For short negative going pulses (greater than 50% duty cycle) we can lower the value of R_B (e.g., R_A = 50kΩ and R_B = 1.6kΩ). For short positive going pulses (duty cycles less than 50%) the limiting values are reached when the current in R_A is twice that in R_B (e.g., R_B = 50kΩ). This has been corrected on the latest data sheet.

Question 12

I need to switch the waveforms off and on. What's a good way to strobe the 8038?

Answer

With a dual supply voltage (e.g., ±15V) the external capacitor (pin 10) can be shorted to ground so that the sine wave and triangle wave always begin at a zero crossing point. Random switching has a 50/50 chance of starting on a positive or negative slope. A simple AND gate using pin 9 will allow the strobe to act only on one slope or the other, see Figure 2. Using only a single supply, the capacitor (pin 10) can be switched either to V+ or ground to force the comparator to set in either the charge or discharge mode. The disadvantage of this technique is that the beginning cycle of the next burst will be 30% longer than the normal cycle.

Question 13

How can I buffer the sine wave output without loading it down?

Answer

The simplest circuit is a simple op amp follower as shown in Figure 3A. Another circuit shown in Figure 3B allows amplitude and offset controls without disturbing the 8038. Either circuit can be DC or AC coupled. For AC coupling the op amp non-inverting input must be returned to ground with a 100kΩ resistor.

Question 14

Your 8038 data sheet implies that all waveforms can operate up to 1MHz. Is this true?

Answer

Unfortunately, only the square wave output is useful at that frequency. As can be seen from the curves on page 4 of the data sheet, distortion on the sine wave and linearity of the triangle wave fall off rapidly above 200kHz.

Question 15

Is it normal for this device to run hot to the touch?

Answer

Yes. The 8038 is essentially resistive. The power dissipation is then E^2/R and at ±15V, the device does run hot. Extensive life testing under this operating condition and maximum ambient temperature has verified the reliability of this product.

Question 16

How stable are the output amplitudes versus temperature?

Answer

The amplitude of the triangle waveform decreases slightly with temperature. The typical amplitude coefficient is -0.01%/°C, giving a drop of about 1% at 125°C. The sine output is less sensitive and decreases only about 0.6% at 125°C. For the square wave output the $V_{CE(SAT)}$ goes from 0.12V at 25°C to 0.17V at 125°C. Leakage current in the "1" state is less than a few nanoamperes even at 125°C and is usually negligible.

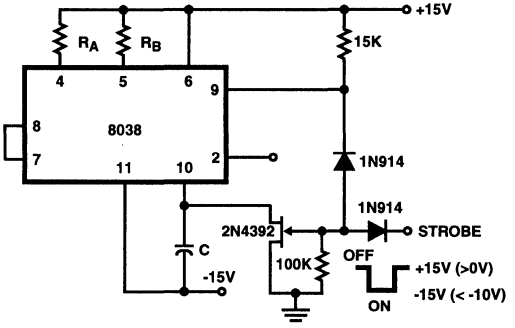


FIGURE 2. STROBE-TONE BURST GENERATOR

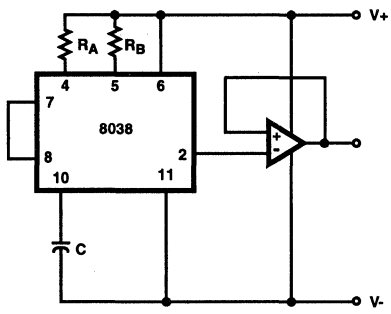


FIGURE 3A.

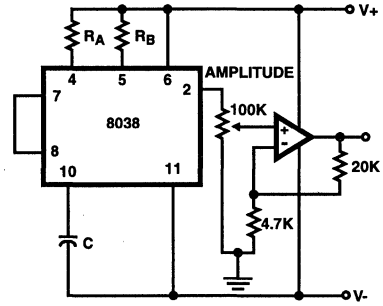
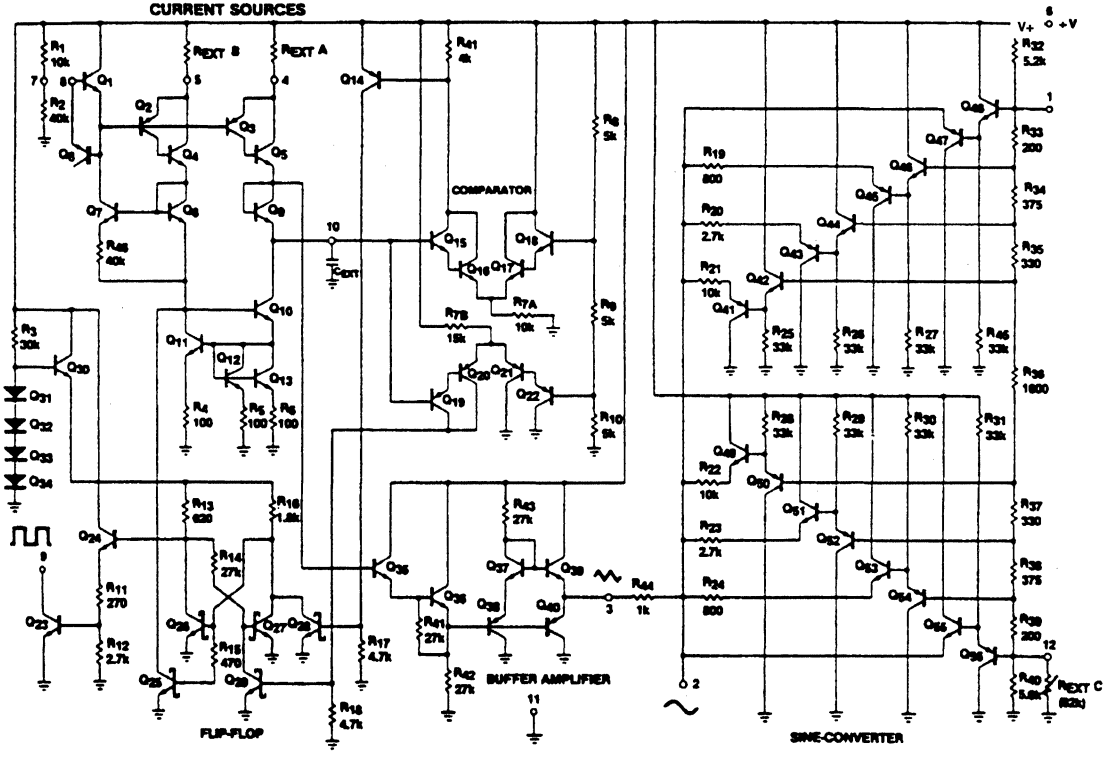


FIGURE 3B.

FIGURE 3. SINEWAVE OUTPUT BUFFER AMPLIFIERS

Schematic Diagram



APPNOTE

No. AN053.1 November 1996

Harris Linear

The ICL7650S: A New Era in Glitch-Free Chopper Stabilized Amplifiers

Author: Peter Bradshaw

Introduction

Op Amps

Historically, the biggest single problem with the application of op amps has been the input offset voltage. This is indicated by the fact that almost all important op amps from the µA741 and LM101 on have offered offset null adjustment pins, special screening to low offset voltage values, and/or internal V_{OS} trimming (laser or Zener-zap). Also consider the extensive series of specifications devoted to its variability with temperature, time, common-mode voltage (CMRR), power supply (PSRR), output voltage (A_{VOL}), and sometimes even down to variation of temperature drift with offset null correction. Contrast this with the treatment afforded one other important (error-causing) input parameter, input bias current, which usually gets lust a specified value under one set of conditions, a variation over temperature, and a term relating to its matching between the two inputs. If variation with common-mode voltage, power supply voltage, etc., is covered, it is generally only in a "typical curve" buried in the middle of the data sheet.

The answers to this concern have been many and varied. Several modules use chopper stabilization to provide very low offset voltages, although most of these do not provide differential inputs and they also have problems with input frequencies near the chopping rate (see Intermodulation Effects). The devices are typically bulky and expensive, and the two-path approach frequently used (Figure 1) tends to adversely affect settling times; the high-speed path and the low-speed path will settle to different points unless the pole-zero pairs are extremely well matched. The only monolithic chopper-stabilized devices previously available are probably best described as disappointing and expensive.

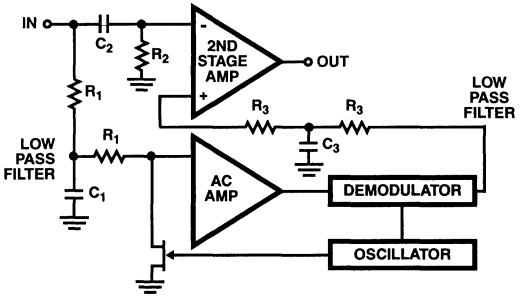


FIGURE 1. TYPICAL MODULE CHOPPER-STABILIZED AMPLIFIER

Therefore, considerable effort has been expended to improve the offset and drift characteristics of standard op amp devices, and some very good results have been achieved with several bipolar input devices, such as the OP-05 and OP-07. Careful die layout and circuit balance, in many cases combined with internal offset null trimming, bring initial offset voltages under 100µV, and temperature drifts below 0.5µV/°C. Although this is over an order of magnitude better than a good grade of µA741 or LM101A, there is still much room for, but little realistic hope of, substantial further improvement in this direction. In addition, the requisite screening of parts is expensive, even with currently available levels of automation.

Technology

In the last few years, a new technology, in the shape of CMOS, has entered the analog field, and has led to the introduction of a range of products previously only dreamed of. Most spectacular, perhaps, has been its rapid dominance of the A/D and D/A converter market (Figures 2 and 3). Today very few converter systems are being designed that don't use CMOS devices specifically intended for this purpose, and in most cases they provide virtually the whole function. More recently, CMOS technology has moved into the more traditional building blocks of analog circuits, so that now CMOS versions of the standard bipolar op amps, regulators, and timers are available, with comparable or better specifications, lower power dissipation, and close to competitive pricing (Figures 4-6). However, although these devices have solved many traditional op amp problems. input offset voltage and low frequency noise voltage were not among them. Using the op amp and analog switch capabilities of this CMOS technology, Intersil introduced in early 1979 a new approach to the low offset voltage requirement, the Commutating Auto-Zero or C_{AZ} amp, shown in Figure 7.

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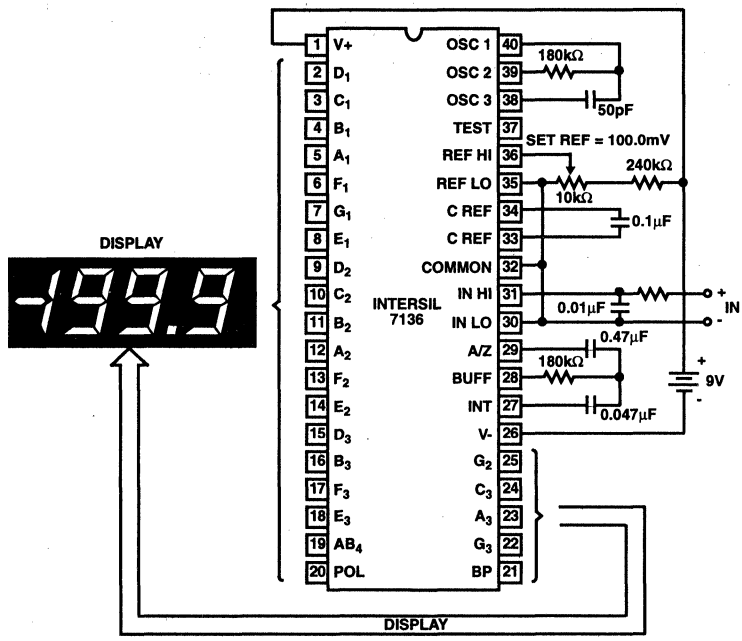


FIGURE 2. LCD DIGITAL PANEL METER USING THE ICL7136 CMOS A/D CONVERTER

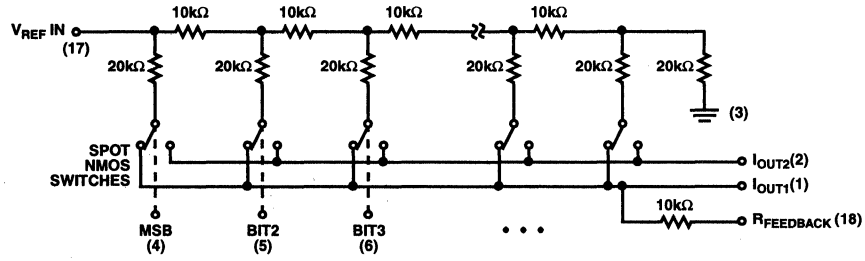


FIGURE 3. CMOS D/A CONVERTER FUNCTIONAL DIAGRAM (AD7541)

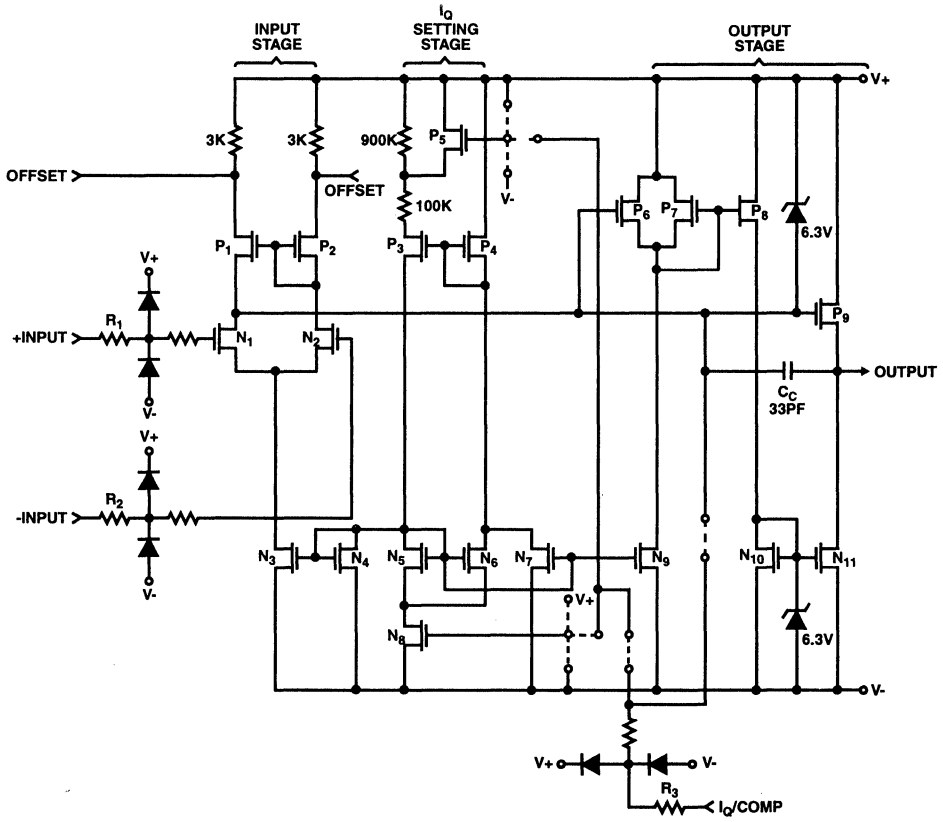


FIGURE 4. CMOS OP AMP SCHEMATIC (ICL7611 FAMILY)

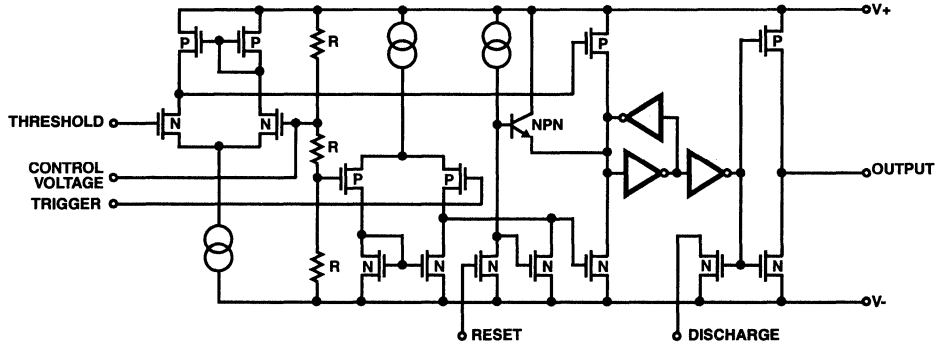


FIGURE 5. ICM7555/7556 CMOS SINGLE AND DUAL TIMERS

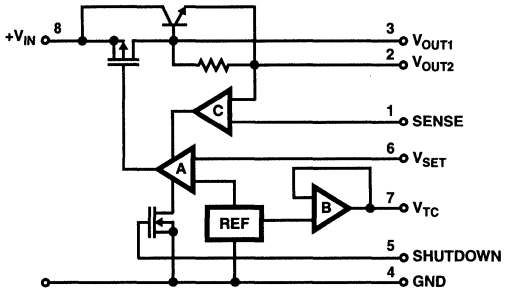


FIGURE 6. FUNCTIONAL DIAGRAM OF THE ICL7663 CMOS REGULATOR

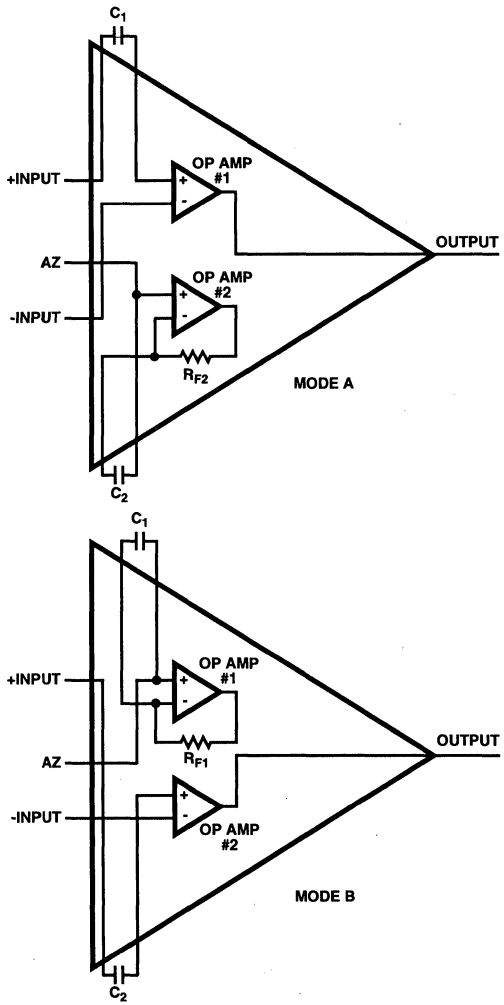


FIGURE 7. ICL7600/ICL7601 COMMUTATING AUTO-ZERO (C_{AZ}) OPERATIONAL AMPLIFIER SHOWING TWO-CYCLE OPERATION

These devices at once became the best monolithic amplifiers available in terms of offset voltage (at 5μV) and time and temperature drift. They utilize two internal op amps, one active while the other auto-zeroes itself into an external capacitor. Upon commutation, the roles change and the active op amp uses its capacitor to cancel its offset. Two capacitors are needed, but the values and characteristics are not critical. Although offering three orders of magnitude improvement over the input characteristics of the μA741/LM101A type, and nearly two orders of magnitude over the best bipolar devices in offset and drift, the C_{AZ} principle has some disadvantages. The input current does not exploit the CMOS capability fully, and there is appreciable spiking at both the input and output (Figure 8). This can be largely removed by filtering, but that limits the available bandwidth.

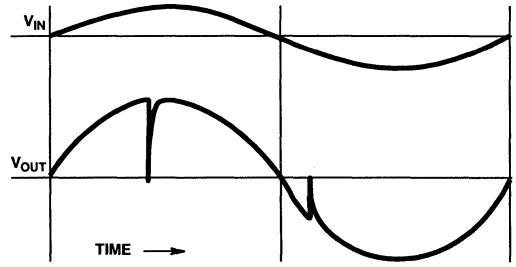


FIGURE 8. OUTPUT SPIKES DUE TO COMMUTATING OPERATION

Synthesis

Intersil therefore decided to try to overcome all these problems by applying the capabilities of CMOS technology to the principle of the chopper-stabilized amplifier. The result is the ICL7850, whose Functional Diagram is shown in Figure 9. The use of a single full-time main amplifier avoids any output glitches, and input switching glitches are minimized by careful area- and charge-balancing on the network of input switches. The chopping operation is performed by means of a nulling amplifier, which shares one input with the main amplifier. The other input is switched alternately between the two main amplifier inputs (Figure 10). When the inputs are shorted, its output drives a null point on itself, and when the inputs are across those of the main amplifier, it drives a null point on that amplifier. The two null points are the back-gates (often called "body connections") on the mirror transistors of the input stage, and by bypassing these to the equivalent point on the other leg with external capacitors, a simple low-leakage automatic offset null arrangement is achieved. Full differential input capability is retained, and the impedances on the two inputs are well balanced. The input stage legs are merged, as shown in Figure 11, to reduce the input noise and improve balance and high-frequency CMRR, etc.

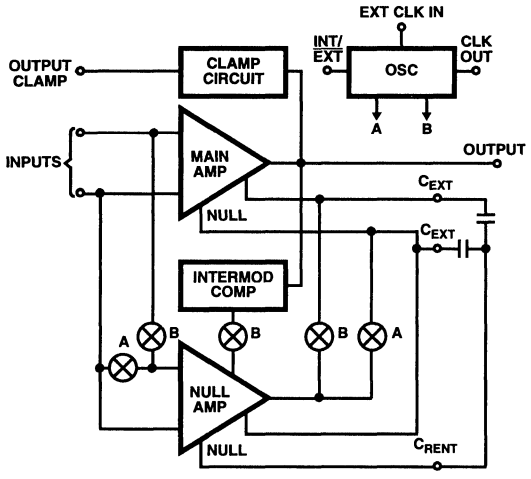


FIGURE 9. FUNCTIONAL DIAGRAM OF ICL7650S

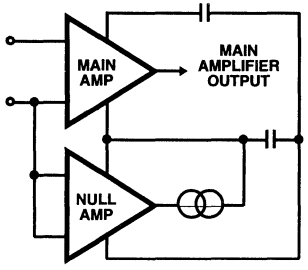


FIGURE 10A. NULLING ITSELF

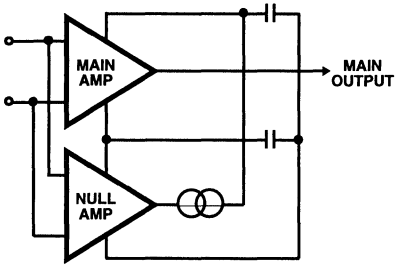


FIGURE 10B. NULLING MAIN AMPLIFIER

FIGURE 10. TWO PHASES OF NULLING OPERATION

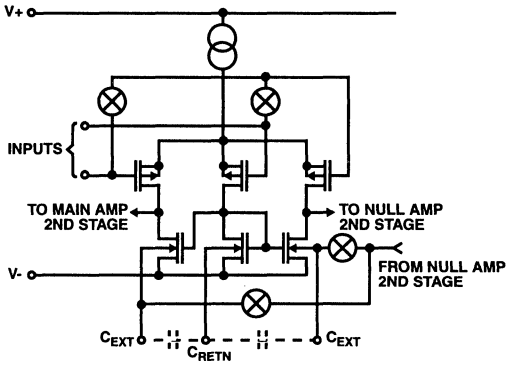
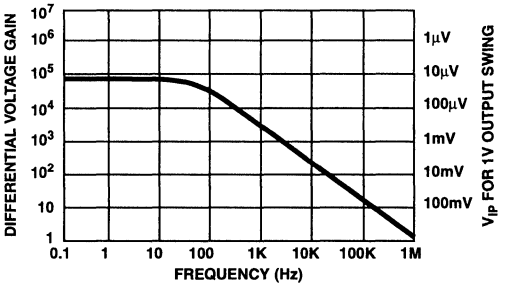


FIGURE 11. THREE-LEGGED INPUT STAGE (SIMPLIFIED)



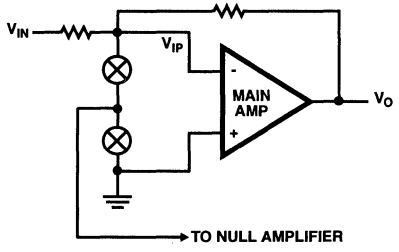


FIGURE 12. GAIN ROLL-OFF AND INPUT VOLTAGE (MAIN AMPLIFIER ALONE WITHOUT NULL SYSTEM) VS FREQUENCY

The circuit automatically provides correction (at DC) for CMRR, PSRR, and AVOL, to the same level as for VOS (typically under 1mV), and the IB remains in the low pA area, set by the leakage of the input switches (also acting as protection diodes) and the small net charge injection. The latter is doubly-balanced both by careful device matching and by the excellent recovery of any residual injection, due to the equipotential nature of the inputs. The open-loop gainbandwidth product and the slew-rate are set purely by the main amplifier. The null system time constant is controlled by the effective gm to the output of the nulling amplifier and the external capacitors, and is readily controlled to be much longer than the chopping period. In addition, the "injection" of the nulling signal into the first stage of the main amplifier ensures that the pole-zero match at this cross-over point is no problem.

Intermodulation Effects

Two residual problems remain with the usual chopper-stabilized amplifier circuits. One of these is the intermodulation between applied signals and the chopping frequency, as mentioned earlier. This arises because the main amplifier has finite gain near this frequency, and so develops a small differential input signal to sustain the requisite output (distinct from any DC offset voltage). This signal is, of course, at the signal frequency, and has an amplitude determined by the gain roll-off characteristics (Figure 12) and the signal amplitude, and will be seen by the nulling circuit as an error signal equivalent to an input offset voltage. This circuit will then attempt to null out the input signal during the active null time. If the difference in frequency between the signal and the chopping rate is large compared to the null circuit time constant, this attempt will essentially fail, since the proposed direction of change will vary between (or during) each null time in such a way to lead to little net resultant. On the other hand, if the signal and chopping frequencies are close together (in terms of the time constant), the null circuit will respond at the beat frequency, leading to two undesirable results. First, the gain and phase characteristics will be disturbed in the neighborhood of the chopping frequency, since the amplifier input signal will be partially reduced, with some delay. Second, the effective input will include a component at the beat frequency, not present in the true input.

The ICL7850 minimizes this problem by the simple expedient of introducing a compensating dynamic offset voltage in the nulling amplifier. This is possible since, at the frequency range of interest, the AC signal that causes the problem is a function only of the compensation capacitor, the input stage g_ms, and the output signal amplitude. By adding another capacitor from the output signal of the main amplifier to the corresponding summing point in the nulling amplifier, with a value which is correctly scaled to allow for the ratio of the input stage g_ms, and connecting it only during the time when the main amplifier is being nulled, the nulling amplifier does not see the input-related signal at the main amplifier. Thus, no nulling signal is generated, and no beat frequency is generated. The required matching of the g_m and capacitor values is readily achieved, since they are all on a monolithic die, and the result is a device with virtually no interference between the normal operation of the main amplifier and the chopping action of the nulling amplifier.

Overload Effects

The second traditional problem with chopper-stabilized amplifiers relates to their behavior under overload. Once again the problem arises through the presence of an input signal on the main amplifier which is not due to the input offset voltage. In this case, the presence of a large signal in the system leads to the output running up against the supply rails. Under these conditions the amplifier no longer has control, and the voltage at its input becomes only a function of the feedback network, the input signal, and the output swing limit of the amplifier, as shown in Figure 13. The nulling amplifier, however, has no means of knowing that this is the problem, and will attempt to "rectify" it by driving the null network to remove this input signal. This effort cannot succeed, and in fact will increase the depth of overload. If this condition is maintained long enough (compared to the nulling time constant), the null circuit itself will also be driven to its limit. Thus, when the input signal returns to an inrange value, the input offset voltage will be skewed heavily to one side. If the nulling range of the amplifier exceeds the input signal range, frequently the case in the high-gain applications common for such devices, the output will remain stuck at the supply rail until the null circuit has almost recovered. Since the null amplifier driving signal may be quite small, recovery may take a long time.

Several possible methods can be used to combat this effect. One is to detect the output limiting condition, and to stop the chopping operation during the time that this does (or can) occur. This has two disadvantages. It may not be possible to predict such overrange conditions, nor easy to detect their occurrence either. Further, even if this is done successfully, the nulling system will be unable to correct the inevitable loss of true null caused by leakage currents on the null points, etc. Thus, an extended overrange interval with the chopping stopped can leave the null badly disturbed, perhaps as much as when the chopping is active. Nevertheless, in situations where an overrange occurrence is predictable or readily detectable, and lasts only for a limited time, the technique is very useful. The ICL7650 facilitates this form of overload effect amelioration by providing an EXT CLK IN pin (in the 14-pin versions), which can be held "low", stopping the chopping action in a position where no capacitor charging can occur, and by allowing judicious use of the CLAMP pin (see below) as an overload detector.

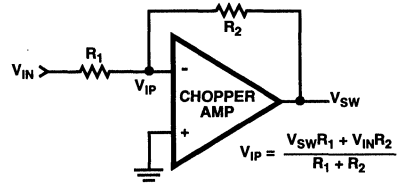


FIGURE 13. VOLTAGES IN INVERTING AMPLIFIER WITH OVERLOAD INPUT

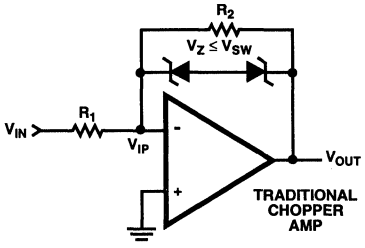


FIGURE 14. AVOIDING OVERLOAD WITH ZENER CLAMPS

The other technique for avoiding the overload problem involves adding a nonlinear element to the feedback network, so that overrange inputs do not cause the output to limit against the supply rail. One possible way of doing this is to parallel the feedback element with a pair of Zener diodes

which conduct just before the limiting would occur, as shown in Figure 14 for the inverting configuration. The noninverting arrangement is similar, but only reduces the gain to unity after the Zeners conduct. One disadvantage with this circuit is that the Zener voltage is quite critical, especially if the supply voltage variation is significant and the maximum allowable swing is desired. The ICL7850 avoids both of these problems by providing a CLAMP pin which will conduct current in the appropriate direction whenever the output voltage gets within a few hundred mV of either supply. The internal schematic is indicated in Figure 15A, and the output current characteristics as a function of the voltage margin to the supply rails in Figure 15B. The leakage currents due to the small N and P channel MOSFETs are negligible, and they can only be turned on if their common sources, tied to the output, get close to the relevant rail. If this pin is tied to the inverting input to the amplifier, and the impedance at this point is adequate, the desired limiting is readily achieved, with no disturbance to the null network, and usually negligible effect on the input bias current. The only penalties paid for this overload protection are a slight limitation on the output swing, and an increase in the input current on the inverting input when the output swings close to the rail. Also, the input circuit is not quite so easily guarded on a PC board if the CLAMP pin is used.

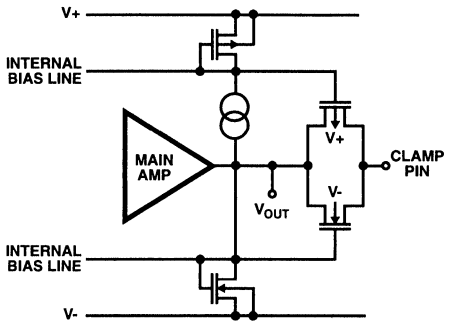


FIGURE 15A. OUTPUT CLAMP CIRCUIT

Device Characteristics

The net result, then, of all this technical wizardry is an op amp with quite remarkable characteristics. The input error-related parameters are unprecedented in a monolithic device, and rare indeed against all competitors, with a V_{OS} of under 5µV (typically under 1µV) and an input bias current of no more than 10pA. The V_{OS} value is maintained over the full range of the power supply, input common-mode, output swing, and temperature ranges. In other words the PSRR, CMRR, A_{VOL}, and dV_{OS}/dT or drift are all virtually unmeasurable, and well over 120dB, 120dB, 140dB, and under 10nV/°C, respectively. The long-term drift, which we can consider to be very low frequency noise (as indeed it is from a device physics point of view), is also undetectable.

The other device characteristics also compare favorably with those of the µA741 and LM101 type. The Gain-Bandwidth product and slew rate are both about 3 times higher, at 2MHz and 2.5V/µs respectively, the supply current is about the same, at 2mA (3.5mA Max), the stability margin is similar, and the output swings between the supply rails. The only significant limitations on its use are the reduced supply voltage range (±8V Max) and the 10kΩ load limitation. These are becoming less important with the growth of ±5V analog systems, and also can be readily side-stepped, as shown in the Applications section below.

And to cap it all, this paragon of op amp virtue is a moderate-sized monolithic die made with a high-yielding mature low-cost process, so the device cost is quite low.

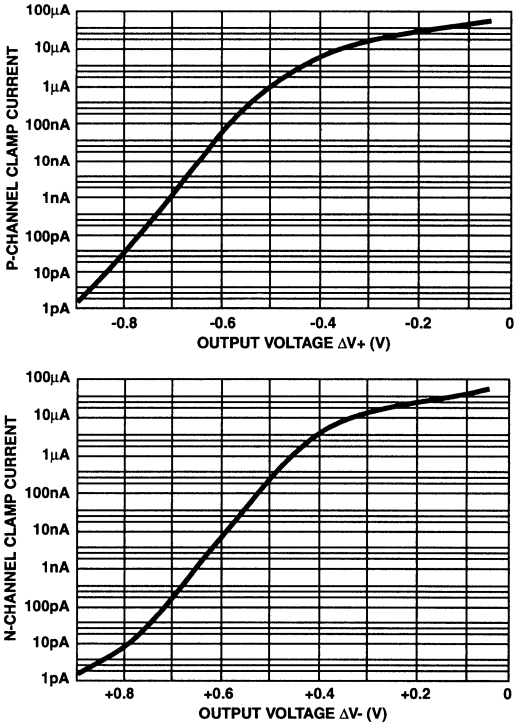


FIGURE 15B. CONDUCTION CHARACTERISTICS

Applications

So much has been written about op amp applications over the last few decades that there is little point in trying to reproduce it all, even with revised specifications and capabilities. The most important point to be appreciated is that in any application where the performance of the circuit can be significantly enhanced by a reduction of input offset voltage and/or bias current, the ICL7650S can be put right to work. Further, any circuit using a null-trimming pot is an immediate candidate for replacement, since the cost of purchase, insertion, initial adjustment, and especially periodic readjustment will generally be greater than the initial small premium for this device and two capacitors. Otherwise, the finite space available here will be used to present the particulars of this substitution as germane to the ICL7650S, followed by the details of some circuits that utilize the specific capabilities of the part particularly well, and some combinations with other devices that concatenate their respective features.

The normal substitution requires nothing but the replacement of any null trim pot with two required capacitors. In the case of the 14-pin devices, the pinout corresponds to that of the LM108 type device, so substitution of the ICL7650S for a (rare) 14-pin LM101/A, LM107, µA741, OP-05/OP-07, or any similar part, can be done most readily with the 8-pin version. The alternative involves a minor PC board change. If good overload recovery is a requirement for the application, the connections to the CLAMP pin (see Overload Effects) should be made according to the basic configurations of Figure 16. The impedance at the point of attachment needs to be high enough, at least at DC, to permit the worst case input signal to be accommodated within the capability of the CLAMP pin output current, according to the curve of Figure 15B. Usually this is easily managed in the case of the inverting configuration, but in the non-inverting case, some additional input clamping may be necessary. Some alternatives for doing this are shown in Figure 17.

One frequent use of an op amp is as a comparator. This cannot be done with the usual chopper amplifiers because of their terrible behavior under overload conditions, the normal operating mode for an op amp so used (see Overload Effects). However, the optional overload avoidance feature built-in to the ICL7650 allows its use in many of these applications, as shown in Figure 18. The current from the CLAMP pin forces the inverting input to follow the signal input (within the output swing and input common-mode ranges), and the transfer characteristic is essentially a reflection of the characteristic of Figure 15B. The comparison voltage must be capable of absorbing the CLAMP pin current without distress to itself or other parts of the system. Only one polarity of comparison is possible with a high input impedance, but if a low impedance drive input is available, the roles can be reversed to achieve the other polarity. The speed of the circuit is limited to input ramp rates under 100V/s for the most accurate performance, but above this rate the timing errors of most comparators exceed their input offset errors in any case.

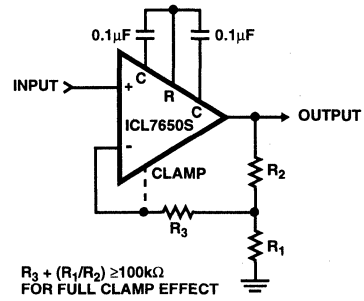


FIGURE 16A. NON-INVERTING AMPLIFIER

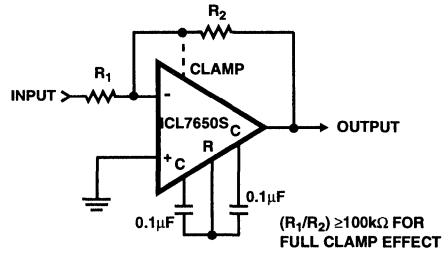


FIGURE 16B. INVERTING AMPLIFIER

FIGURE 16. NON-INVERTING AND INVERTING CONFIGURATIONS WITH (OPTIONAL) CLAMP CIRCUIT CONNECTION

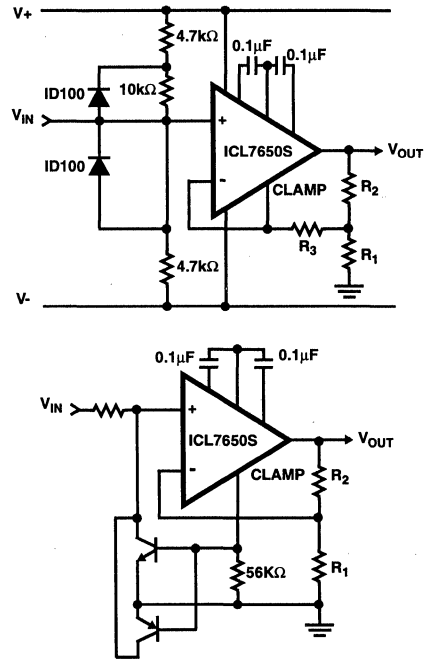


FIGURE 17. SOME OTHER CLAMPING CONFIGURATIONS FOR NON-INVERTING AMPLIFIERS

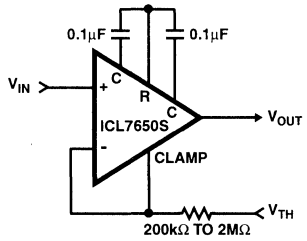


FIGURE 18. LOW OFFSET COMPARATOR

The usual instrumentation amplifier configurations work extremely well with the ICL7650. The standard three op amp configuration (Figure 19) has unbeatable CMRR, a function only of the resistors in practice. With a differential input A/D converter, such as the Intersil ICL71X6, 71X7, 7109 or 7135, just two ICL7650S will maintain high differential gain without any common-mode gain, ideal for pre-amplification of signals from such bridge-type transducers as strain gauges, etc. The arrangement is shown in Figure 20. This also works well with thermocouples whose shielding is grounded at the sensing end, especially in a noisy environment. Note that the offset and drift of the ICL7650 will contribute less than 1°C initial error and less than 0.2°C drift error to an absolute Platinum - Platinum/Rhodium Type S thermocouple between 0°C and 1750°C, or to a Type B thermocouple between 500°C and 1820°C (over the operating temperature range of the ICL7650). This is less than the errors associated with standard thermocouples themselves. Naturally, to realize this performance, all the other little thermocouples between the leads, the PC board, any IC socket, and the other components, etc., will have to be carefully handled. This topic is discussed in Achieving the Full Benefits.

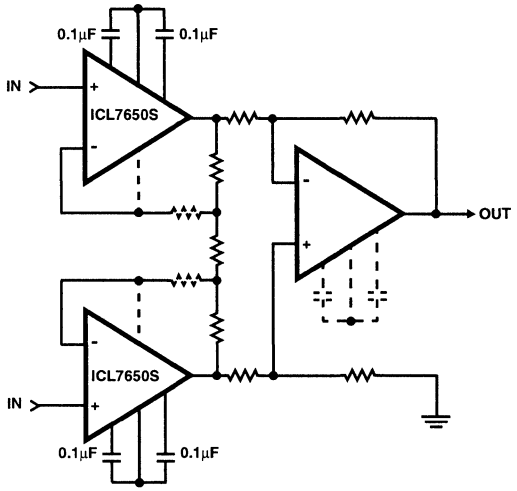


FIGURE 19. 3 OP AMP INSTRUMENTATION AMPLIFIER

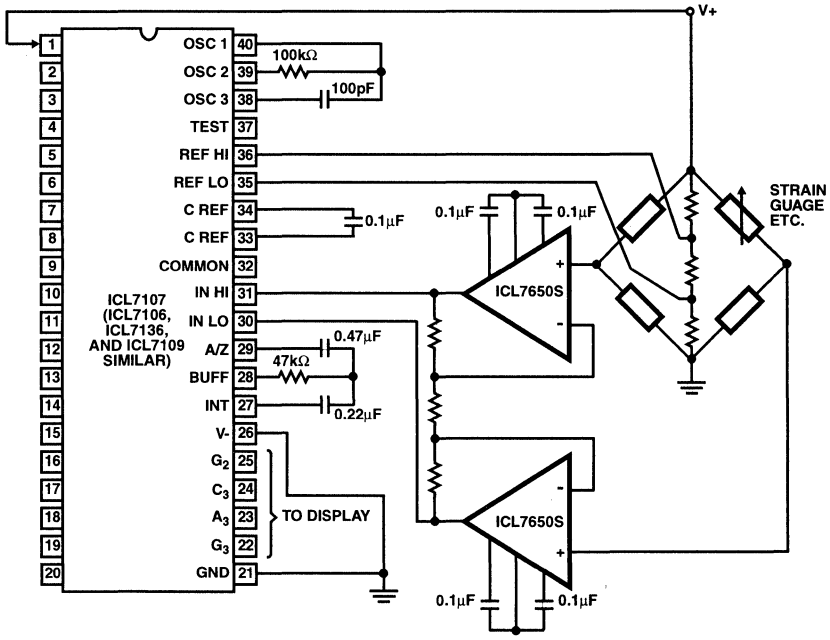


FIGURE 20. 2 OP AMP DIFFERENTIAL PREAMP FOR ICL7106/7/9 FAMILIES

Conventional logarithmic amplifiers have very high dynamic ranges in the current input mode, but in the voltage input mode they end up severely limited by errors associated with the input offset voltage of the input op amp. Two methods are available to combat this problem with the ICL7650. The device itself may be used as the main amplifier, as suggested in Figure 21. This will give a wide dynamic range of close to 6 decades. However, this arrangement lacks the built-in temperature compensation and scale factor adjustment of such monolithic log amps as the Intersil ICL8046. These can be combined with the same dynamic range enhancement by using the ICL7650 to offset null an ICL8048, as shown in Figure 22. The time constant of the nulling network needs to be high enough to avoid loop stability problems. The input current of the system will not be degraded by this configuration, so 6 decades of dynamic range will be available in both voltage and current input modes.

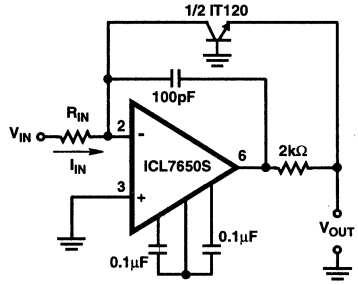


FIGURE 21. BASIC LOG AMPLIFIER

Although the overall performance of the ICL7650 is unprecedented, there are some parameters for which other devices remain better, and it does have some limitations. We have already mentioned the supply voltage limitation, for which the promised circumvention appears in Figure 23. The two JFETs have I_{DSS} values well above the supply current requirement of the ICL7650S, and so operate close to "pinch-off". These "pinch-off" voltages constitute the supply voltages to the ICL7650S, and must meet the specifications required, readily done with the parts listed. By bootstrapping the JFET gates to the output, a follower circuit whose input and output can span the full supply range can be constructed. High voltage JFETs would permit even higher supply voltages. A small amount of high-frequency roll-off is usually needed in the boot-strap to prevent RF instability.

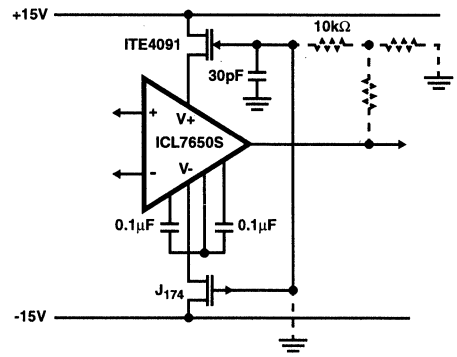


FIGURE 22. OPERATING WITH ±15V SUPPLIES

The output drive limitations may be readily overcome by buffering the ICL7650S with a device such as the μA741, after the fashion of Figure 24. This has the additional advantage of reducing the dissipation in the ICL7650S due to the load, and the thermal effects associated therewith (see Achieving the Full Benefits). These two circuits may be amalgamated in several ways to combine higher voltage operation with heavy load driving capability, such as those shown in Figure 25. One or more of these can be used to construct a configuration that will act correctly in any inverting or noninverting application, for any gain required. These circuits can be used to substitute for virtually any chopper-stabilized module, and most other standard op amps also, with a substantial improvement in input parameters and no loss in output characteristics.

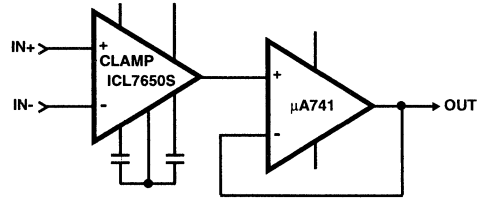


FIGURE 23. USING 741 TO BOOST OUTPUT DRIVE CAPABILITY

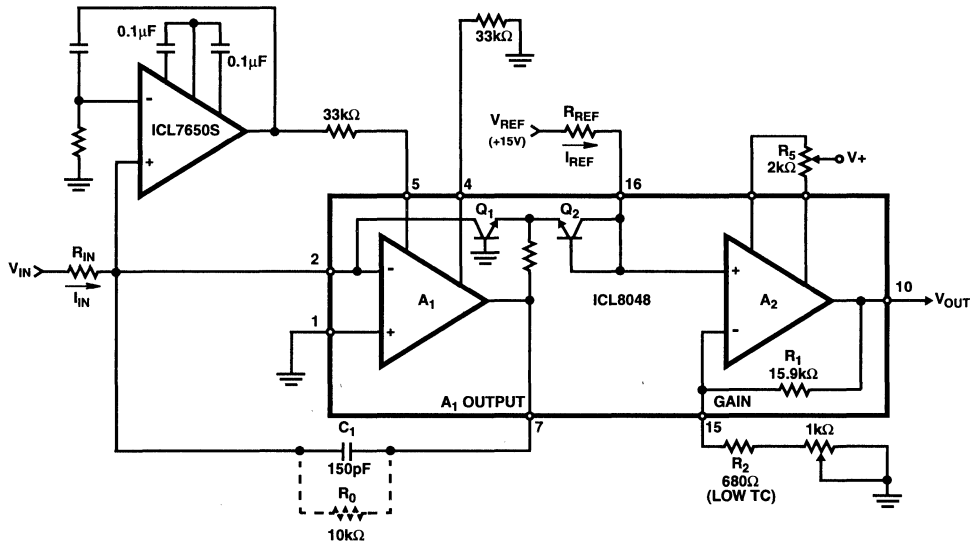


FIGURE 24. ICL8048 OFFSET NULLED BY ICL7650S

The high slew-rate and/or bandwidth of devices such as the HA2500/10/20 and the HA2600/20 families is not, of course, preserved by the arrangements of Figure 25. For these types of devices, the concept used in Figure 22 is preferable. Figure 26 shows two methods of doing this for several high speed devices, and Table 1 gives suitable component values. Note that although the input offset voltage is that of the ICL7650S, the input current will generally be dominated by that of the other device. Also, no protection is provided against overload, and intermodulation is back (see Intermodulation Effects and Overload Effects). These three can be reduced or eliminated by extra complexity in the circuits, at the expense of further loss in generality. Figure 27 shows one method of balancing out the intermodulation terms, and a similar clamp circuit to that of the ICL7650S added externally.

A similar combination of the exceptional low noise performance of the OP-05 (and OP-07) with the ICL7650S is also possible, and incidentally gives the lowest available overall noise performance in any bandwidth from true DC to any other frequency of use with op amps. In this case, the roll-off in the external nulling network should be low enough in frequency to ensure that the cross-over between the two devices does not degrade the performance in the bandwidth of concern. The schematic, in Figure 28, is otherwise the same as that of Figure 26, and Table 1 includes the values for this circuit also. Many other combination circuits have been published in the literature, and the ICL7650S can be used to advantage in the majority of them.

TABLE 1.

DEVICE FAMILY	WORST FAMILY V_{OE} (mV) OVER TEMP.	LOWEST SUPPLY VOLTAGE ±V	FIGURE 26A CIRCUIT				FIGURE 26B CIRCUIT		
			R_A(Ω)	R_S(Ω)	V_S	N_A PIN	R_A (Ω)	N_A PIN	N_G PIN
µA741	7.5	3.0	82K	2000	-	1	680K	1	5
LM101	10.0	3.0	2M	1M	-	5	1M	5	1
LM118	15.0	5.0	330K	180K	+	5	150K	5	1
LF155, 6, 7 (Note 1)	13.0	5.0	120K	5.1K	+	1	560K	1	5
HA2500 (Note 2)	14.0	10.0	6.8K	100	+	5	62K	5	1
HA2600	7.0	5.0	620K	18K	+	1	620K	1	5
CA3140	30.0 (Note 3)	4.5	1M	10K	-	5	240K	5	1
ICL8007	50.0 (Note 3)	5.0	100K	1.2K	-	5	150K	5	1
OP-05	1.6	3.0	1.6M	18K	+	8	2.4M	8	1
OP-07	0.25	3.0	10M	150K	+	8	10M	8	1

NOTES:

1. LF 155, 155, 157 require 12K resistors from pin 1 and 5 to V+, in addition to the resistors mentioned above.
2. ICL7650 supplies are ±8V Max; HA2500 is not specified, but will work, with supplies under ±10V.
3. Unspecified; Value inferred from other data.

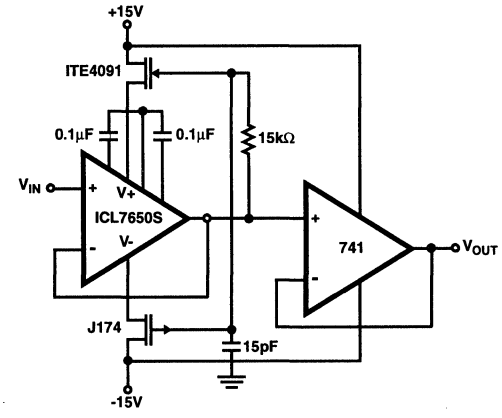


FIGURE 25A.

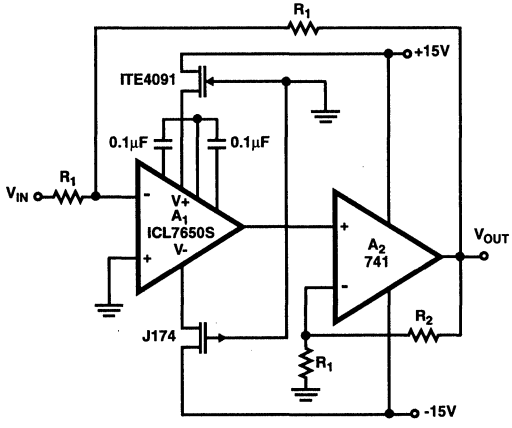


FIGURE 25B.

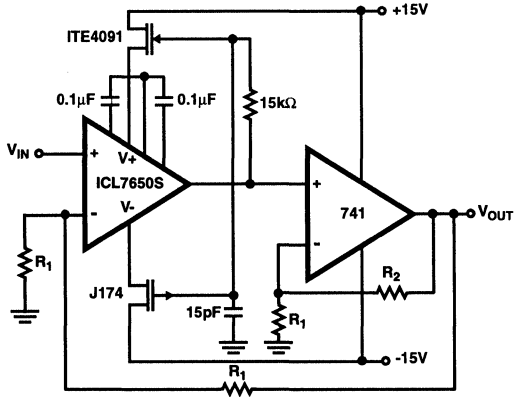


FIGURE 25C.

FIGURE 25. SEVERAL HIGH VOLTAGE-HIGH LOAD COMBINATION CIRCUITS

Achieving the Full Benefits

The ICL7650S brings a new level of accuracy to the analog world, and in doing so exposes a new set of problems and difficulties in the environment of the typical op amp, previously masked by device errors. The standard care taken with ground loops is even more necessary here, and the prevention of PC board leakage is also more important. The pinout on the 14-pin device has been arranged so as to allow easy guarding of the input pins, and the same can be done on the TO-99 device by using a 10-pin outline mounting configuration, as shown in Figure 29. If the CLAMP pin is being used, the configurations of Figure 30 may be found more useful. Careful cleaning with TCE or alcohol, followed by a compressed air blow-dry, is advisable, and an epoxy or silicone rubber coating will prevent subsequent contamination. Careful use of Teflon® or similar standoffs may be helpful in stubborn cases of PC board troubles.

The impedances of the driving nodes for the offset null storage capacitors are quite high, as explained above, and care should be taken in the PC board layout to avoid coupling stray signals into these points. A pseudo guard ring tied to V- could be applied in exceptionally difficult cases. The CAP RETN pin (14-pin parts only) is somewhat less sensitive, but should be treated with respect also.

Some consideration should be given to the capacitors themselves. On initial turn-on, and also if radical changes in common-mode or power supply voltages occur, the voltages on these capacitors must change to the (new) desired values. A capacitor with high dielectric absorption, such as a ceramic type, will absorb back part of the change in charge during the respective holding time during several clock cycles, or even for many seconds, leading to a significant initial (or recovery) settling time. If either of these is critical, a polypropylene capacitor should be used, although in many cases a mylar or similar film capacitor would be adequate. Another disadvantage of ceramic capacitors is that they frequently generate a significant amount of 1/f or "flicker" noise, which will be fed into the system through the null pins. For this reason, it is recommended that a film type capacitor be used. even though any low-leakage capacitor will "work".

The ultimate limitations to any high accuracy DC amplifier are the thermo-electric or Peltier effects in all the thermocouple junctions between dissimilar materials. The junctions of concern to us here are those between the silicon (N- or P- type) and the aluminum metallization on the die, the aluminum to bond-wire and bond-wire to header post or lead frame, and the post/lead to PC board junctions. If all these are at the same temperature, then no problems will arise, since an equal number of identical junctions are interposed on the return path. The power dissipation within the IC die is inherently low, and most applications will not add very much to that, so we can consider the die temperature to be fairly uniform. Thus, the thermocouples out to the bond-wires can be neglected unless a heavy load resistance is applied. The same is reasonably true for the bond-wire to post/lead junction. However, the post/lead to PC board junction can be a serious problem. The thermo-electric coefficient of the usual Kovar-copper junction present here is of

the order of 30μV/°C, and the thermal contact between the individual junctions is not very good. A temperature gradient of as little as 0.1°C/inch will lead to an error as large as the typical offset voltage of the ICL7650S! A point-source (power transistor, say) with a 10°C temperature rise must be kept 5 to 6 inches away, and a similar line-source would need to be many feet away. Even air currents from a standard forced-air heating system can cause gradients approaching this level. Similar effects can occur with other circuit elements, although generally their lead materials have lower thermo-electric coefficients.

The cure for these potential problems lies in exercising care in both the circuit design and the board layout. The power dissipation in the ICL7650S should be kept low (use the circuits of Figures 24-26 for load driving if needed), and power-dissipating components should be kept well away. A cooling fan or blower is undesirable unless an enclosure is used around the op amp and its associated components. and in any case the air flow should not pass over this area after a power-dissipating area. Low thermo-electric coefficient connections should be used wherever possible, and in all cases the PC board layout should emphasize thermal balance in loop paths.

An example of care in the electrical and thermal layout of a board, and appropriate choice of components to complement the performance of the ICL7650 may be found in the ICL7650SEV/Kit, an evaluation kit that includes a test board which can be used to measure most of the critical parameters of the device, and to simulate various possible applications. The kit includes all the necessary passive and active components to build the circuits of Figures 23 - 25 also, so that they may be substituted for another device in an operating system for checkout.

Summary

The ICL7650S represents a significant step-function in op amp performance (one that should not have occurred until 1990, according to one recent Wescon presentation). The design brings chopper-stabilized performance to a new level of availability, while making it virtually transparent to the user. Although it is too early to predict the demise of the trimming potentiometer industry, nevertheless this device and its successors can be expected to replace the need for many of them and their periodic re-adjustment, frequently without increasing the initial cost, and certainly with favorable lifetime cost benefits. The combination circuits suggested here allow an even closer approach to the "perfect op amp" than has ever been available before, and at remarkably low cost.

One side-effect of the remarkable performance potential of the ICL7650S is that several subtle error-causing effects that have previously been largely masked by the inherent errors of the available op amps, are now uncovered. Great care must be exercised to achieve the full performance benefits the device can offer. These caveats do not, of course, apply in cases where a simple replacement of a less accurate or less stable device is contemplated. The high degree of "user-transparency" achieved in the chopping operation promises a minimum of applications problems, borne out by the rapid acceptance of the device in a wide range of applications.

The author would like to acknowledge the design efforts of Lee Evans and Dane Snow in turning the concept of the device into such a magnificent reality, and Andy Wolff for refining, expanding, and testing many of the circuit application ideas presented here. An additional acknowledgment should go to Bob Darling of Rutgers University for the basic concept of Figure 23. A list of relevant application notes and article reprints that may be found helpful in pursuing the ideas opened up in this one follows:

A007 "Using the ICL8046/8049 Monolithic Log-Antilog Amplifier", by Ray Hendry.

A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing", by Ed Sliger.

R017 "CMOS Chopper Op Amp Does Away with Glitches", by Peter Bradshaw, Electronic Design, August 2, 1980.

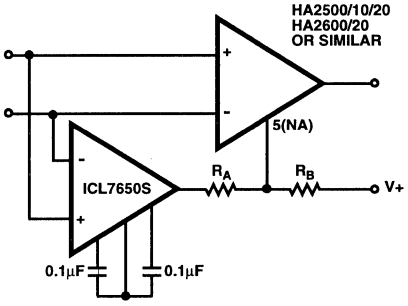


FIGURE 26A.

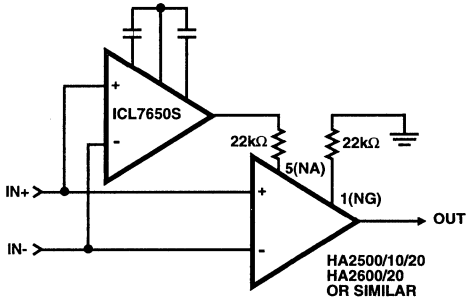


FIGURE 26B.

FIGURE 26. HA2500 OR HA2600 OFFSET NULLED BY

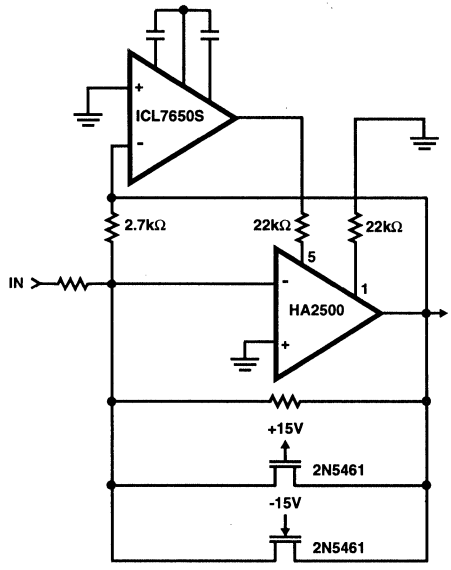


FIGURE 27. NULLED HA2500 WITH DYNAMIC CORRENTION AND OVERLOAD CLAMP

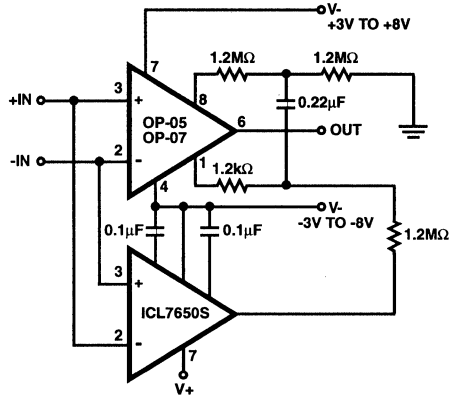


FIGURE 28. AUTO-NULLING CIRCUIT FOR OP-05/OP-07

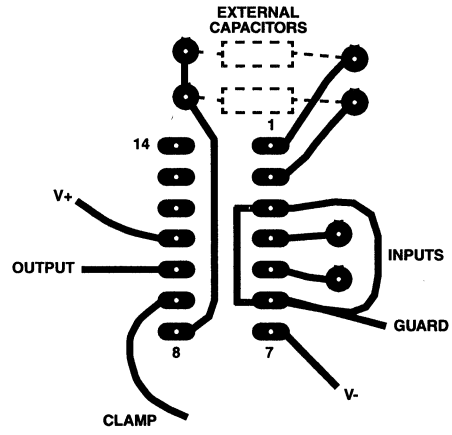


FIGURE 29A. 14-PIN PART

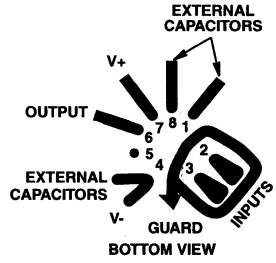


FIGURE 29B. TO-99 PACKAGE

FIGURE 29. BOARD LAYOUTS FOR INPUT GUARDING

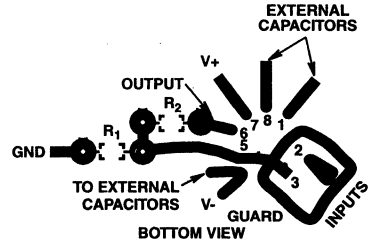


FIGURE 30A. NON-INVERTING AMPLIFIER WITH CLAMP

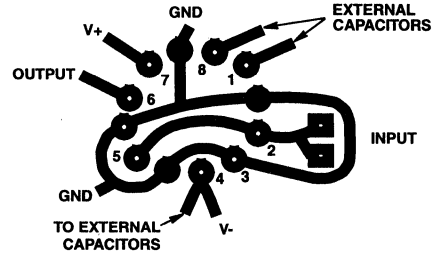


FIGURE 30B. INVERTING AMPLIFIER WITH CLAMP

FIGURE 30. INPUT GUARDING WITH CLAMP PIN

APP NOTE

No. AN514.1 November 1996

Harris Linear

The HA-2400 PRAM Four Channel Operational Amplifier

Author: Don Jones

Introduction

Harris Semiconductor has announced a new linear device, the HA-2400/HA-2405 Four Channel Operational Amplifier. This combines the functions of an analog switch and a high performance operational amplifier, and makes practical a large number of new linear circuit applications.

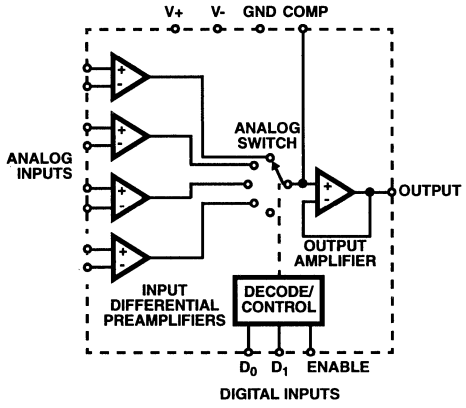


FIGURE 1.

A functional diagram of the HA-2400 is shown above. There are four preamplifier sections, one of which is selected through the DTL/TTL compatible inputs and connected to the output amplifier. The selected analog input terminals and the output terminal form a high performance operational amplifier.

In actuality, the circuit consists of four conventional op amp input circuits connected in parallel to a conventional op amp output circuit. The decode/control circuitry furnishes operating current only to the selected input section.

Circuit Connections

The digital inputs control the selection of the amplifier input channels in accordance with the following truth table:

D_1	D_0	ENABLE	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
L	L	H	ON	OFF	OFF	OFF
L	H	H	OFF	ON	OFF	OFF
H	L	H	OFF	OFF	ON	OFF
H	H	H	OFF	OFF	OFF	ON
L or H	L or H	L	OFF	OFF	OFF	OFF

$0V \le L \le +0.8V$ $+2V \le H \le +5V$

The digital inputs can be driven with any DTL or TTL circuit which uses a standard +5V supply.

Compensation

Frequency compensation for closed loop stability is recommended for closed loop gains less than 10. This is accomplished by connection of a single external capacitor from Pin 12 to AC ground (the V+ supply is recommended). The following table shows the minimum suggested compensation for various closed loop gains, with the resultant bandwidth and slew rate. Obviously, when the four channels are connected with different feedback networks, the channel with the lowest closed loop gain will govern the required compensation.

GAIN, V/V		C_{COMP} pF	BAND-WIDTH (TYPICAL) (-3dB), MHz	SLEW RATE (TYPICAL) V/µs
NON-INVERTING	INVERTING			
1	-	15	8.0	15
2	1	7	8.0	20
3	2	4	8.0	22
5	4	3	6.0	25
8	7	2	5.0	30
>10	>9	0	40 ÷ GAIN	50

Compensation capacitors of greater value can be used to obtain lower bandwidth, greater phase margin, and reduced overshoot, at the expense of proportionately reduced slew rate.

External lead-lag networks could also be used to optimize bandwidth and/or slew rate at a particular gain.

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Applications

Any circuit function which can be constructed using a conventional operational amplifier can also be constructed using any channel of the HA-2400. Similar or different networks can be wired from the output to each channel input pair. The device can therefore be used to select and condition different input signals, or to select between different op amp functions to be performed on a single input signal.

To wire a particular op amp function to a channel, simply connect the appropriate network between the two inputs for that channel and the common output in the same manner as in wiring a conventional op amp. It is often possible to design with fewer external components than would be required in wiring four separate op amps (see Application Numbers 2 and 3 on the following pages). It should be remembered that the networks for unselected channels may still constitute a load at the amplifier output and the signal input, as if the unselected input terminals were disconnected from the network.

If offset adjustment is required, it can generally be accomplished by resistive summation at either of the inputs for each channel (see Application Number 8).

The analog input terminals of the OFF channels draw the same bias current as the ON inputs. The maximum differential input voltage of these terminals must be observed and their voltage levels must never exceed the supply voltages.

When the Enable input is held low, all four input channels are disconnected from the output. When this occurs, the output voltage will generally slowly drift towards the negative supply. If a 0V output condition is required, one channel should be wired as a voltage follower with its positive input grounded.

The amplifier output impedance remains low, even when the inputs are disabled; so it is not generally practical to wire the outputs of two or more devices directly together. The compensation pins of two devices, however, could be wired together to produce a switch with one output and more than four input channels.

The voltage at the compensation pin is about 0.7V more positive than the output signal, but has a very high source impedance. Maximum current from this pin is about 300μA, which makes it a convenient point for limiting the output swing through clamping diodes and divider networks (see Application Number 13).

Even if the application only requires a single channel to be switched on and off, it is often more economical to use the HA-2400, rather than a separate analog switch and high performance op amp. Unused analog channel inputs should be grounded. Unused digital inputs may be wired to ground for a permanent "low" input, or either left open or wired to +5V for a permanent "high" input.

The circuits illustrated on the following pages are a few of the thousands of possible applications for the Four Channel Operational Amplifier. These will give the reader a general impression of how the units can be connected; and probably will help generate many other ideas for applications. Also included are some "challenges" for the reader to modify the illustrated designs to perform different functions.

Application No. 1

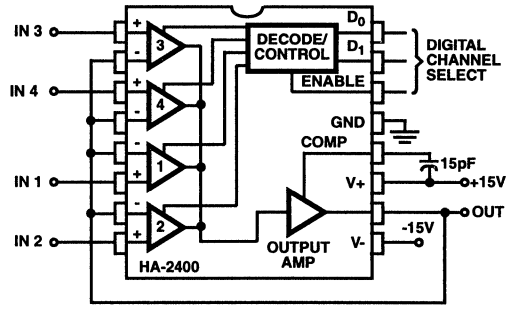

FIGURE 2. ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

This circuit is used for analog signal selection or time division multiplexing. As shown, the feedback signal places the selected amplifier channel in a voltage follower (non-inverting unity gain) configuration, and provides very high input impedance and low output impedance. The single package replaces four input buffer amplifiers, four analog switches with decoding, and one output buffer amplifier.

For low level input signals, gain can be added to one or more channels by connecting the (-) inputs to a voltage divider between output and ground. Bandwidth is approximately 8MHz, and the output will slew from one level to another at about 15V/μs.

Expansion to multiplex 5 to 12 channels can be accomplished by connecting the compensation pins of two or three devices together, and using the output of only one of the devices. The Enable input on the unselected devices must be low.

Expansion to 16 or more channels is accomplished in a straightforward manner by connecting outputs of 4 four-channel multiplexers to the inputs of another four-channel multiplexer.

Differential signals can be handled by two identical multiplexers addressed in parallel.

Inverting amplifier configurations can also be used, but the feedback resistors may cause crosstalk from the output to unselected inputs.

Application No. 2

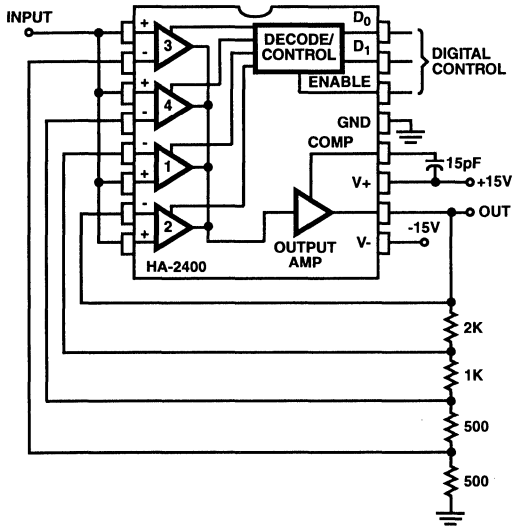

FIGURE 3. AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

This is a non-inverting amplifier configuration with feedback resistors chosen to produce a gain of 0, 1, 2, 4, or 8 depending on the Digital Control inputs.

Comparators at the output could be used for automatic gain selection for auto-ranging meters, etc.

CHALLENGE: Design a circuit using only two HA-2400s which can be programmed to any of 16 different gains.

Application No. 3

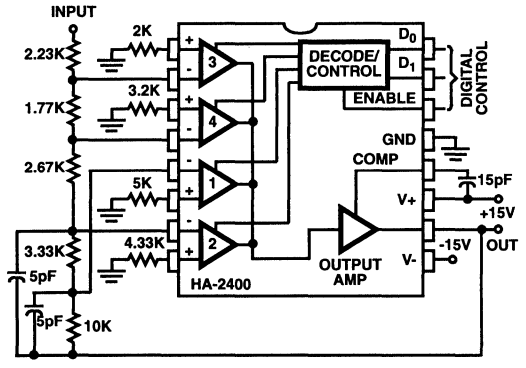

FIGURE 4. AMPLIFIER, INVERTING PROGRAMMABLE GAIN

The circuit above can be programmed for a gain of 0, -1, -2, -4, or -8.

This could also have been accomplished with one input resistor and one feedback resistor per channel in the conventional manner, but this would require eight resistors rather than five.

Application No. 4

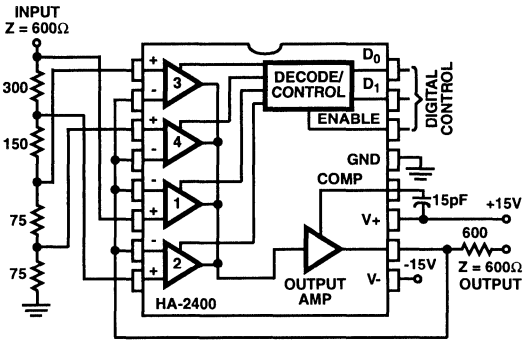

FIGURE 5. PROGRAMMABLE ATTENUATOR

This circuit performs the function of dividing the input signal by a selected constant (1, 2, 4, 8, or ∞ as illustrated). To multiply by a selected constant, see circuit No. 2. While T, π, or L sections could be used in the input attenuator, this is not necessary since the amplifier loading is negligible and a constant input impedance is maintained. The circuit is thus much simpler and more accurate than the usual method of constructing a constant impedance ladder and switching sections in and out with analog switches.

Two identical circuits may be used to attenuate a balanced line.

Application No. 5

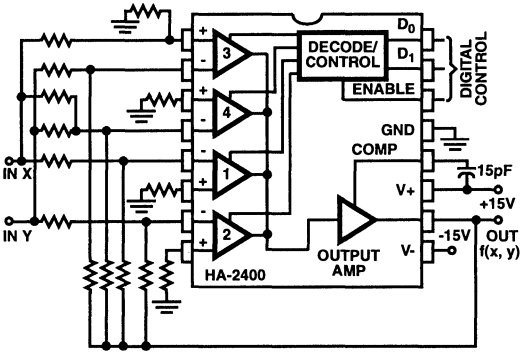

FIGURE 6. ADDER/SUBTRACTOR PROGRAMMABLE FUNCTION

The circuit shown above can be programmed to give the output functions $-K_1X$, $-K_2Y$, $-(K_3X + K_4Y)$, or $K_5X - K_6Y$. Obviously, many other functions of one or more variables can be constructed, including combinations with analog multiplier or logarithmic modules.

This device opens up many new design approaches in digitally controlled analog computation or signal manipulation.

Application No. 6

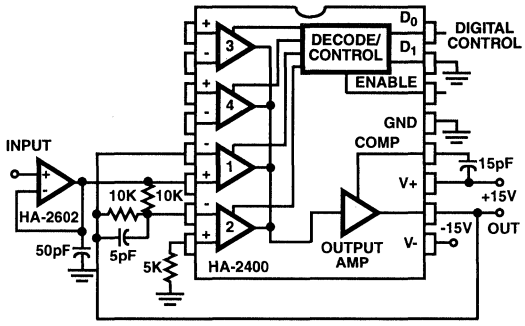

FIGURE 7. PHASE SELECTOR/PHASE DETECTOR/ SYNCHRONOUS RECTIFIER/BALANCED MODULATOR

This circuit passes the input signal at unity gain, either unchanged, or inverted depending on the Digital control input. A buffered input is shown, since low source impedance is essential. Gain can be added by modifications to the feedback networks. Signals up to 100kHz can be handled with $20V_{P-P}$ output. The circuit becomes a phase detector by driving the Digital Control input with a reference phase at the same frequency as the input signal, the average DC output being proportional to the phase difference, with 0V at +90 degrees. By connecting the output to a comparator, which in turn drives the Digital Control, a synchronous full-wave rectifier is formed.

With a low frequency input signal and a high frequency digital control signal, a balanced (supressed carrier) modulator is formed.

Application No. 7

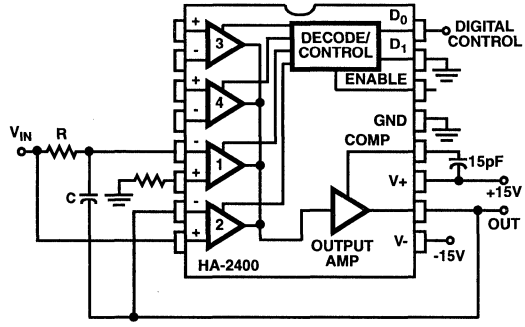

FIGURE 8. INTEGRATOR/RAMP GENERATOR WITH INITIAL CONDITION RESET

It is difficult in practice to set the initial conditions accurately in an integrator. This usually requires wiring contacts of a mechanical relay across the capacitor - leakage currents of solid state switches produce integration inaccuracy. The scheme shown above eliminates these reliability and accuracy problems.

Channel 1 is wired as a conventional integrator, Channel 2 as a voltage follower. When Channel 2 is switched on, the output will follow V_{IN}, and C will discharge to maintain 0V across it. When Channel 1 is then switched on the output will initially be at the instantaneous value of V_{IN}, and then will commence integrating towards the opposite polarity. This circuit is particularly suitable for timing ramp generation using a fixed DC input. Many variations are possible, such as programmable time constant integrators.

Application No. 8

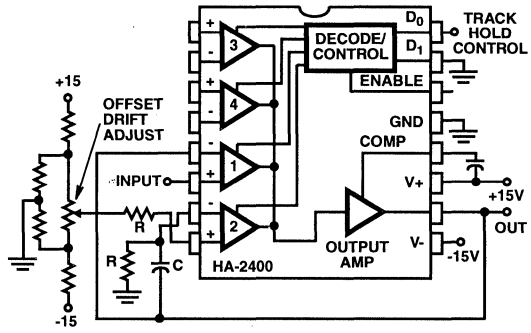

FIGURE 9. TRACK AND HOLD/SAMPLE AND HOLD

Channel 1 is wired as a voltage follower and is turned on during the track/sample time. If the product of R x C is sufficiently short compared to the period of maximum output frequency, or sample time, C will charge to the output level. Channel 2 is an integrator with zero input signal. When Channel 2 is then turned on, the output will remain at the voltage across C.

Application No. 9

Any oscillator which can be constructed using an op amp, such as the twin-T, phase shift, crystal controlled types, etc. can be made programmable by using the HA-2400. The following illustration is a Wien Bridge type, which is very popular for signal generators, since it is easily tunable over a wide frequency range, and has a very low distortion sine wave output. The frequency determining networks can be designed from about 10Hz to greater than 1MHz. Output level is about $6.0V_{RMS}$. By substituting a programmable attenuator (Circuit No. 4) for the Buffer Amplifier, a very versatile sine wave source for automatic testing, etc. can be constructed.

CHALLENGE: A high Q, narrow band filter can be made by feeding back greater than 1/3 of the output to the negative input. Design a circuit using the HA-2400 and an RC network which can be programmed either to generate or to detect an audio tone of the same frequency. Such a circuit would be quite useful for data communications.

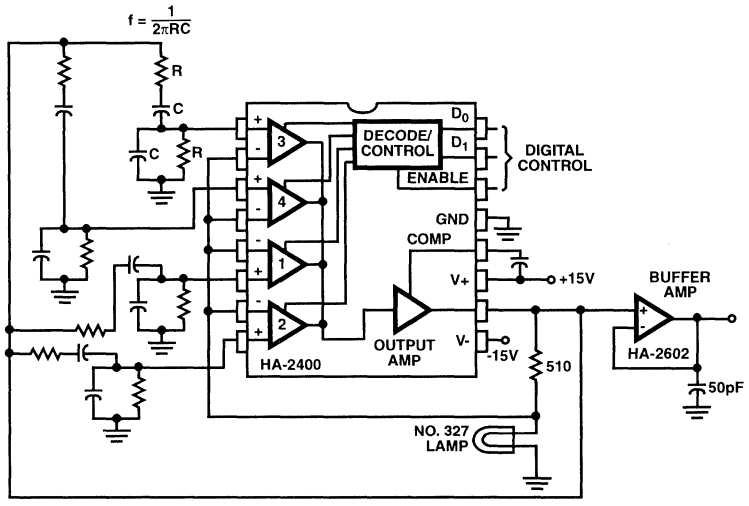

FIGURE 10. SINE WAVE OSCILLATOR PROGRAMMABLE FREQUENCY

An even simpler circuit can be made by wiring one channel as an amplifier, choosing the compensation capacitor to yield the minimum required bandwidth or slew rate. When the Enable input is pulled low, the output will tend to remain at its last level, because of the charge remaining on the compensating capacitor.

Application No. 10

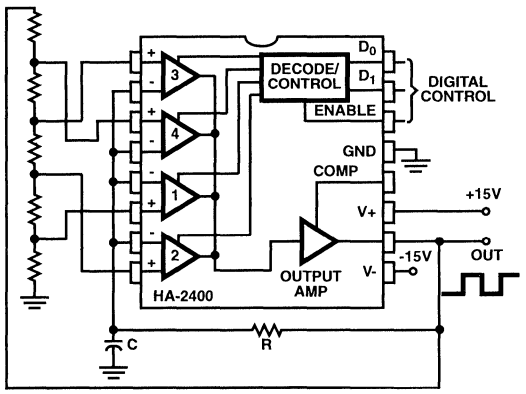

FIGURE 11. MULTIVIBRATOR, FREE RUNNING, PROGRAMMABLE FREQUENCY

This is the simplest of any programmable oscillator circuit, since only one stable timing capacitor is required. The output square wave is about $25V_{P-P}$ and has rise and fall times of about 0.5µs. If a programmable attenuator circuit (No. 4) is placed between the output and the divider network, 16 frequencies can be produced with two HA-2400s and still only one timing capacitor.

A precision programmable square-triangle generator can also be constructed by adapting circuit described in Harris Application Note AN507 to the HA-2400.

Application No. 11

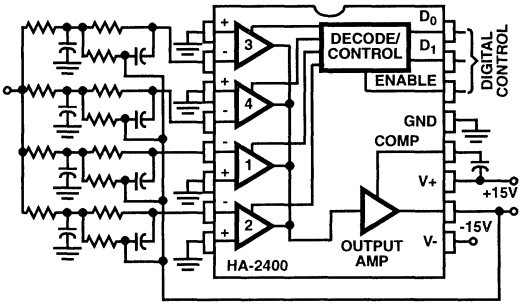

FIGURE 12. PROGRAMMABLE ACTIVE FILTER

Shown above is a second order low pass filter with programmable cutoff frequency. This circuit should be driven from a low source impedance since there are paths from the output to the input through the unselected networks.

Virtually any filter function which can be constructed with a conventional op amp can be made programmable with the HA-2400.

A useful variation would be to wire one channel as a unity gain amplifier, so that one could select the unfiltered signal, or the same signal filtered in various manners. These could be cascaded to provide a wide variety of programmable filter functions.

Application No. 12

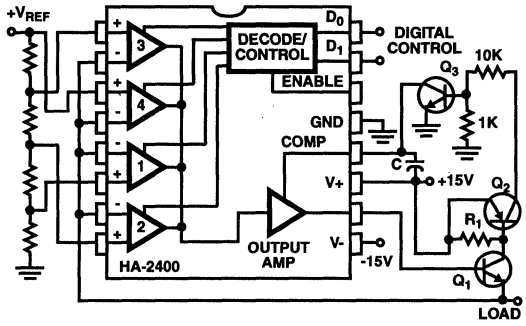

FIGURE 13. POWER SUPPLY PROGRAMMABLE

Many systems require one or more relatively low current voltage sources which can be programmed to a few predetermined levels. It is no longer necessary to purchase a programmable power supply with far more capability than needed. The circuit shown above produces positive output levels, but could be modified for negative or bipolar outputs. Q_1 is the series regulator transistor, selected for the required current and power capability. R_1, Q_2 and Q_3 form an optional short circuit protection circuit, with R_1 chosen to drop about 0.7V at the maximum output current. The compensation capacitor, C, should be chosen to keep the overshoot, when switching, to an acceptable level.

CHALLENGE: Design a supply using only two HA-2400s which can be programmed to 16 binary weighted (or 10 BCD weighted) output levels.

Application No. 13

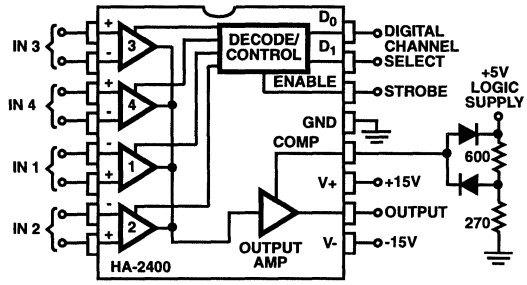

FIGURE 14. COMPARATOR, FOUR CHANNEL

Application No. 14

When operated open loop without compensation, the HA-2400 becomes a comparator with four selectable input channels. The clamping network at the compensation pin limits the output voltage to allow DTL or TTL digital circuits to be driven with a fanout of up to ten loads.

Output rise and fall times will be about 100ns for differential input signals of several hundred millivolts, but will be in the microsecond region for small differential signals.

The circuit can be used to compare several signals against each other or against fixed references; or a single signal can be compared against several references. A "window comparator", which assures that a signal is within a voltage range, can be formed by monitoring the output polarity while rapidly switching between two channels with different reference inputs and the same signal input.

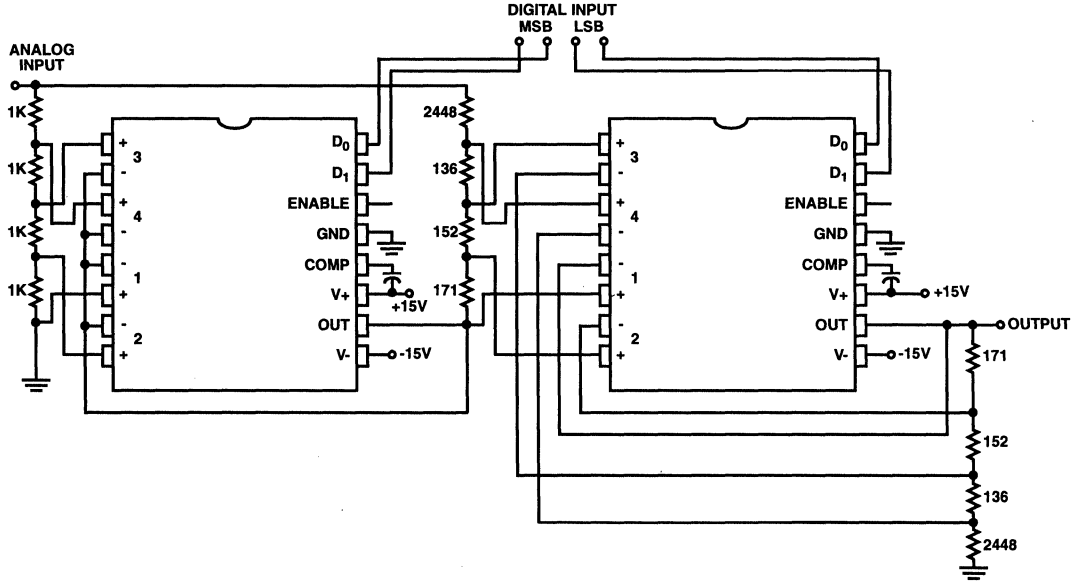

FIGURE 15. MULTIPLYING D TO A CONVERTER

The circuit above performs the function,

$$V_{OUT} = V_{IN} \times \frac{N}{16},$$

where N is the binary number from 0 to 15 formed by the digital input. If the analog input is a fixed DC reference, the circuit is conventional 4-bit D to A. The input could also be a variable or AC signal, in which case the output is the product of the analog signal and the digital signal.

The circuit on the left is a programmable attenuator with weights of 0, 1/4, 1/2, or 3/4. The circuit on the right is a noninverting adder which adds weights to the first output of 0, 1/6, 1/8 or 3/16.

If four quadrant multiplication is required, place the Phase Selector circuit (No. 6) in series with either the analog input or output. The D_0 input of that stage becomes the + or - sign bit of the digital input.

More Challenges

One of our favorite college textbooks paused at each climactic point with a statement to the effect that, "Proof of the following theorem is omitted and is suggested as an exercise for the student."

The following is the list of some additional applications in which we believe the HA-2400 will prove very valuable. The "proofs", at present, remain as exercises for our ingenious readers.

- A to D Converter, Dual Slope Integrating
- Active Filter, State Variable Type with Programmable Frequency and/or Programmable "Q"
- Amplifier with Programmable DC Level Shift
- Chopper Amplifiers
- Crossbar Switches
- Current Source, Programmable
- FM Stereo Modulator
- F.S.K. Modem
- Function Generators, Programmable
- Gyrator, Programmable
- Monostable Multivibrator, Programmable
- Multiplier, Pulse Averaging
- Peak Detector with Reset
- Resistance Bridge Amplifier/Comparator with Programmable Range
- Sense Amp/Line Receiver with Programmable Threshold
- Spectrum Analyzer, Scanning Type
- Sweep Generator, Programmable
- Switching Regulator
- Touch-Tone™ Generator/Detector (Use Harris HD-0165 Keyboard Encoder IC)

Feedback

We believe we have only scratched the surface of possible applications for a multiple channel operational amplifier.

If you have a solution for any of the previous "challenges" or any new application, please let us know. Anything from a one word description to a tested design will be welcome.

Harris Semiconductor

APPNOTE

No. AN519.1 November 1996

Harris Linear

Operational Amplifier Noise Prediction (All Op Amps)

Author: Richard Whitehead

Introduction

When working with op amp circuits an engineer is frequently required to predict the total RMS output noise in a given bandwidth for a certain feedback configuration. While op amp noise can be expressed in a number of ways, "spot noise" (RMS input voltage noise or current noise which would pass through 1Hz wide bandpass filters centered at various discrete frequencies), affords a universal method of predicting output noise in any op amp configuration.

The Noise Model

Figure 1 is a typical noise model depicting the noise voltage and noise current sources that are added together in the form of root mean square to give the total equivalent input voltage noise (RMS), therefore:

$E_{ni} = \sqrt{e_{ni}^2 + I_{ni}^2 R_G^2 + 4KTR_G}$ where,

E_{ni} is the total equivalent input voltage noise of the circuit,

e_{ni} is the equivalent input voltage noise of the amplifier, and

$I_{ni}^2 R_G^2$ is the voltage noise generated by the current noise.

$4KTR_G$ expresses the thermal noise generated by the external resistors in the circuit where K = 1.38 x 10^{-23} joules/°K; T = 300°K (27°C) and:

$$R_G = \left(\frac{R_1 R_3}{R_1 + R_3}\right) + R_2$$

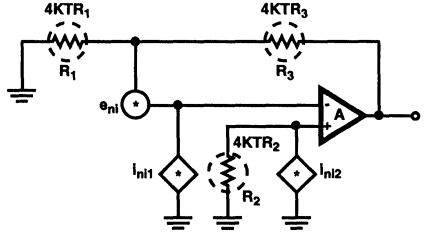

FIGURE 1.

The total RMS output noise (E_{no}) of an amplifier stage with gain = G in the bandwidth between f_1 and f_2 is:

$$E_{no} = G\left(\int_{f_1}^{f_2} (E_{ni})^2 df^{1/2}\right)$$

Note that in the amplifier stage shown, G is the non-inverting gain:

$$\left(G = 1 + \frac{R_3}{R_1}\right),$$

regardless of which input is normally driven.

Procedure for Computing Total Output Noise

1. Refer to the voltage noise curves for the amplifier to be used.
2. Enter values of e_{ni}^2 line (a) of the table below from the curve labeled "Noise spectral density" (the values must be squared).
3. From the current noise curves for the amplifier, obtain the values of i_{ni}^2 for each of the frequencies in the table, and multiply each by R_G^2, entering the products in line (b) of the table.
4. Obtain the value of $4KTR_G$ from Figure 8, and enter it on line (c) of the table. This is constant for all frequencies. The $4KTR_G$ value must be adjusted for temperatures other than normal room temperature.
5. Total each column in the table on line (d). This total is E_{ni}^2.

	10Hz	100Hz	1kHz	10kHz	100kHz
(a) e_{ni}^2					
(b) $I_{ni}^2 R_G^2$					
(c) $4KTR_G$					
(d) E_{ni}^2					

6. On linear scale graph paper enter each of the values for E_{ni}^2 versus frequency. In most cases, sufficient accuracy can be obtained simply by joining the points on the graph with straight line segments.
7. For the bandwidth of interest, calculate the area under the curve by adding the areas of trapezoidal segments. This procedure assumes a perfectly square bandpass condition; to allow for the more normal -6dB/octave bandpass skirts, multiply the upper (-3dB) frequency by 1.57 to obtain the effective bandwidth of the circuit, before computing the area. The total area obtained is equivalent to the square of the total input noise over the given bandwidth.

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8. Take the square root of the area found above and multiply by the gain (G) of the circuit to find the total Output RMS noise.

A Typical Example

It is necessary to find the output noise of the circuit shown below between 1kHz and 24kHz.

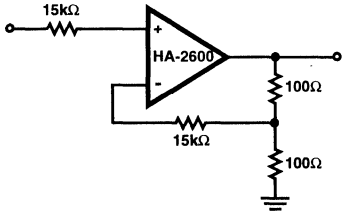

FIGURE 2. THE HA-2600 IN A TYPICAL G = 1000 CIRCUIT

Values are selected from the data sheet and Figure 8 to fill in the table as shown below. An R_G of 30kΩ was selected.

	10Hz	100Hz	1kHz	10kHz	100kHz
(a) e_{ni}^2	$3.6x10^{-15}$	$1.156x10^{-15}$	$7.84x10^{-16}$	$7.29x10^{-16}$	$7.29x10^{-16}$
(b) $I_{ni}^2R_G^2$	$9.9x10^{-16}$	$1.89x10^{-16}$	$3.15x10^{-17}$	$7.2x10^{-18}$	$72x10^{-18}$
(c) $4KTR_G$	$4.968x10^{-16}$	$4.968x10^{-16}$	$4.968x10^{-16}$	$4.968x10^{-16}$	$4.968x10^{-16}$
(d) E_{ni}^2	$5.09 x10^{-15}$	$1.86x10^{-15}$	$1.31x10^{-15}$	$1.23x10^{-15}$	$1.23x10^{-15}$

The totals of the selected values for each frequency is in the form of E_{ni}^2. This should be plotted on linear graph paper as shown below:

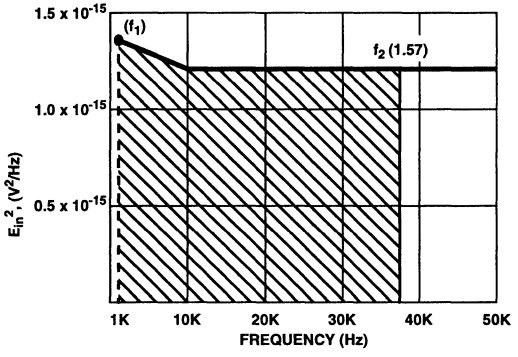

FIGURE 3. HA-2600 TOTAL EQUIVALENT INPUT NOISE

Since a noise figure is needed for the frequency of 1kHz to 24kHz, it is necessary to calculate the effective bandwidth of the circuit. With A_V = 60dB the upper 3dB point is approximately 24kHz. The product of 1.57 (24kHz) is 37.7kHz and is the effective bandwidth of the circuit.

The shaded area under the curve is approximately $45 \times 10^{-12}V^2$; the total equivalent input noise is $\sqrt{E_{in}^2}$ or 6.7μV, and the total output noise for the selected bandwidth is $\sqrt{E_{in}^2}$ x (closed loop gain) or $6.7mV_{RMS}$.

Actual Measurements for Comparison

The circuit shown below was used to actually measure the broadband noise of the HA-2600 for the selected bandwidth:

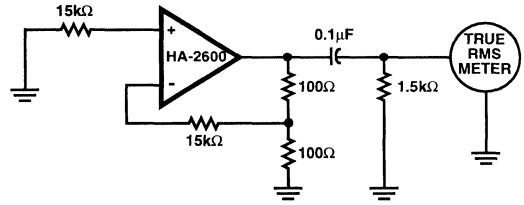

FIGURE 4. A TYPICAL TEST CIRCUIT FOR BROADBAND NOISE MEASUREMENTS

The frequencies below the f1 point of the bandwidth selected are filtered out by the RC network on the output of HA-2600. The measurement of the broadband noise is observed on the true RMS voltmeter. The measured output noise of the circuit is $4.7mV_{RMS}$ as compared to the calculated value of $6.7mV_{RMS}$.

Acquiring the Data for Calculations

Spot noise values must be generated in order to make the output noise prediction. The effects of "Popcorn" noise have been excluded due to the type of measurement system.

The Quan-Tech Control Unit, Model No. 2283 and Filter Unit, Model No. 2181 were used to acquire spot noise voltage values expressed in ($V/\sqrt{Hz}$). The test system performs measurements from 10Hz by orders of magnitude to 100kHz with an effective bandwidth of 1Hz at each tested frequency.

Several source resistance (R_G) values were used in the measuring system to reveal the effects of R_G on each type of Harris' op amps and to obtain proper voltage noise values essential for current noise calculations.

A Discussion On "Popcorn" Noise

"Popcorn" noise was first discovered in early 709 type op amps. Essentially it is an abrupt step-like shift in offset voltage (or current) lasting for several milliseconds and having amplitude from less than one microvolt to several hundred microvolts. Occurrence of the "pops" is quite random - an amplifier may exhibit several pops per second during one observation period and then remain "popless" for several minutes. Worst case conditions are usually at low temperatures with high values of R_G. Some amplifier designs and some manufacturer's products are notoriously bad in this respect. Although theories of the popcorn mechanism differ, it is known that devices with surface contamination of the semiconductor chip will be particularly bad "poppers". Advertising claims not withstanding, the author has never seen any manufacturer's op amp that was completely free of "popcorn." Some peak detector circuits have been developed to screen devices for low amplitude "pops", but 100% assurance is impossible because an infinite test time would be required. Some studies have shown that spot noise measurements at 10Hz and 100Hz, discarding units that are much higher than typical, is an effective screen for potentially high "popcorn" units.

The vast majority of Harris op amps will exhibit less than $3\mu V_{P-P}$ "popcorn". Screening can be performed, but it should be noted that the confidence level of the screen could be as low as 60%.

References

[1] Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design. New York: John Wiley and Sons, 1973.

[2] Instruction Manual, Model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New Jersey.

Typical Spot Noise Curves

Unless Otherwise Noted: $V_S = \pm 15V$, $T_A = 25^oC$

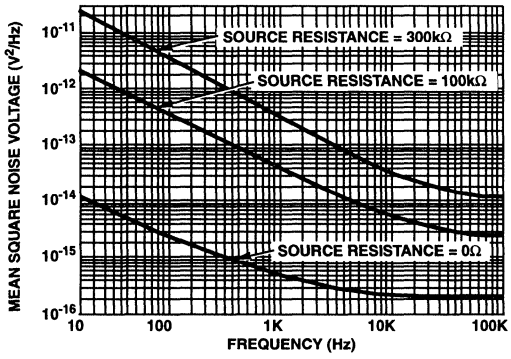

FIGURE 5. HA-2500/2510/2520 INPUT NOISE VOLTAGE

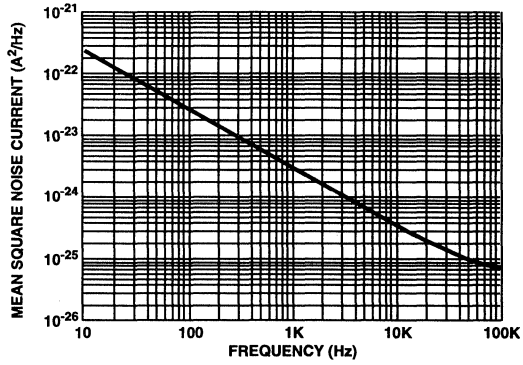

FIGURE 6. HA-2500/2510/2520 INPUT NOISE CURRENT

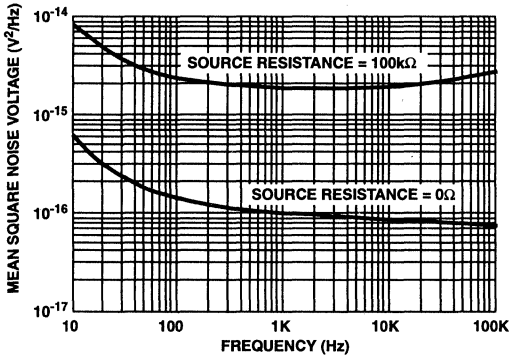

FIGURE 7. HA-4741 INPUT NOISE VOLTAGE

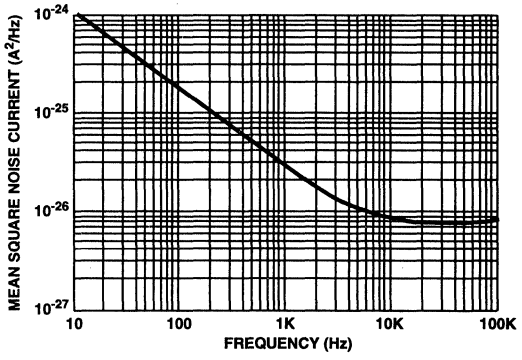

FIGURE 8. HA-4741 INPUT NOISE CURRENT

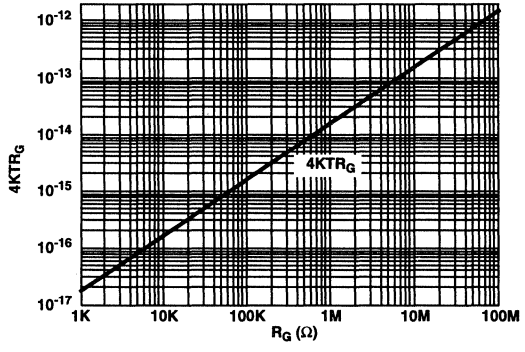

FIGURE 9. NOISE vs RESISTOR VALUE

Harris Semiconductor

APPNOTE

No. AN548.1 November 1996

Harris Linear

A Designers Guide for the HA-5033 Video Buffer

Author: Carl Wolfe

Introduction

Harris Semiconductor is an industry leader in the high speed, wideband, monolithic operational amplifier market. Due to the high performance of Harris products, designers in the more specialized areas of electronics have shown interest in utilizing these products in their applications. One such area is video design. In an effort to address this market, Harris has introduced the HA-5033 video buffer.

This paper will discuss the HA-5033 design and provide additional performance characteristics not shown in the data sheet.

HA-5033 Description

The HA-5033 is a unity gain monolithic IC designed for any application requiring a fast wideband buffer. A voltage follower by design, this product is optimized for high speed 50Ω and 75Ω coaxial cable driver applications common in color video systems.

Critical performance characteristics are summarized in Table 1. Outstanding differential phase/gain characteristics combined with an output current capability of ±100mA makes the HA-5033 an excellent choice for the line driver applications required in video circuit design.

TABLE 1. HA-5033 SPECIFICATIONS: T_A = 25°C; V_{SUPPLY} = ±12V (UNLESS OTHERWISE SHOWN)

PARAMETER	MIN	TYP	MAX	UNITS
Input Offset Voltage			15	mV
Input Bias Current			35	µA
Differential Phase		0.1		Degree
Differential Gain		0.1		%
Slew Rate (±15V)	1000			V/µs
Output Current		±100		mA
Bandwidth (Small Signal)		250		MHz
Bandwidth (V_{IN} = 1V_{RMS})		65		MHz
Supply Current			20	mA

Other features, which include a minimum slew rate of 1000V/µs, make the HA-5033 useful in high speed A/D data conversion and sample/hold circuits.

The HA-5033 is offered in three package configurations: the 12 lead metal can, the 8 lead PDIP, and the 8 lead Power Small Outline Package (PSOP). The pinouts for each package are illustrated in Figure 1.

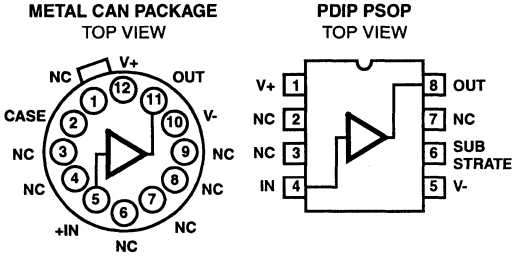

FIGURE 1. HA-5033 PINOUTS: METAL CAN-PIN COMPATIBLE WITH THE LH0033 HYBRID. 8-LEAD, PDIP-FABRICATED USING A COPPER LEAD FRAME. ADVANTAGES INCLUDE EXCELLENT THERMAL CHARACTERISTICS AND BOARD SPACE SAVINGS.

The high performance of this product (summarized in Table 1) is the result of the Harris High Frequency Dielectric Isolation Process. A major feature of this process is that it provides both PNP and NPN high frequency transistors which make wide bandwidth designs, such as the HA-5033, practical.

A Closer Look

Most manufacturer's data sheets provide a schematic diagram and depending upon the complexity of the product, this schematic may be comprehensive or possibly a simplified version. Schematics are a visual means of presenting information, ranging from reliability data, such as transistor counts, to circuit information for circuit analysis or computer simulation. But the most important reason for the schematic is to communicate to the customer the internal structure of the product and therefore, some insight into its operation.

At first glance, a schematic may appear as nothing more than a collection of resistors and transistors. But upon closer examination, particular areas of operation should become evident. Using the HA-5033 as an example (Figure 2), it will be shown that the HA-5033 consists of a signal path, bias network, and performance optimization circuitry.

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Signal buffering is accomplished by cascading two emitter followers. In order to achieve symmetrical positive and negative output drive capability, two pairs are paralleled. The first pair consists of Q_1 and Q_4 for positive drive while the second pair Q_2, Q_3, provide negative drive. The emitter resistors of Q_1, Q_2 ensure stability with respect to load resistance, enhance differential phase/gain performance, and stabilize the quiescent operating point. This signal path has been highlighted on the schematic.

The bias circuitry consists primarily of the diode-biasing located on the left portion of the schematic along with transistors Q_5, Q_6. This circuitry ensures the designed performance of the other active elements.

The performance optimization circuits are a slew enhancement circuit and a bias network buffer circuit. The transistors Q_7, Q_8, Q_9 and Q_{10} are for slew enhancement. If the input voltage exceeds the output by one V_{BE}, Q_7 will turn on Q_{10}, which in turn provides extra base drive to Q_1. Similarly, Q_9 will supply extra base drive to Q_2.

Transistors Q_{11}, Q_{12}, Q_{13} and Q_{14} prevent high frequency or transient signals from affecting the bias circuitry. This prevents C_{CB} multiplication of current sources Q_5 and Q_6, which also improves differential gain/phase performance.

Note that output current limiting was not designed into the HA-5033. If there is a possibility of the output being shorted to ground or the supplies, external current limiting will be necessary.

Any designer interested in using the HA-5033 should be aware of a characteristic related to output transistor operation. As the data sheet performance curves (reproduced in Figure 3) show, the output swing is a function of frequency. These curves show the point at which observable distortion occurs for a given frequency. However, if the signal amplitude, signal frequency or both are increased beyond the curves shown, thermal "runaway" will occur. This is due to both the NPN and PNP output transistors approaching a condition of being simultaneously on. This condition has been computer simulated and the results are shown in Figure 4.

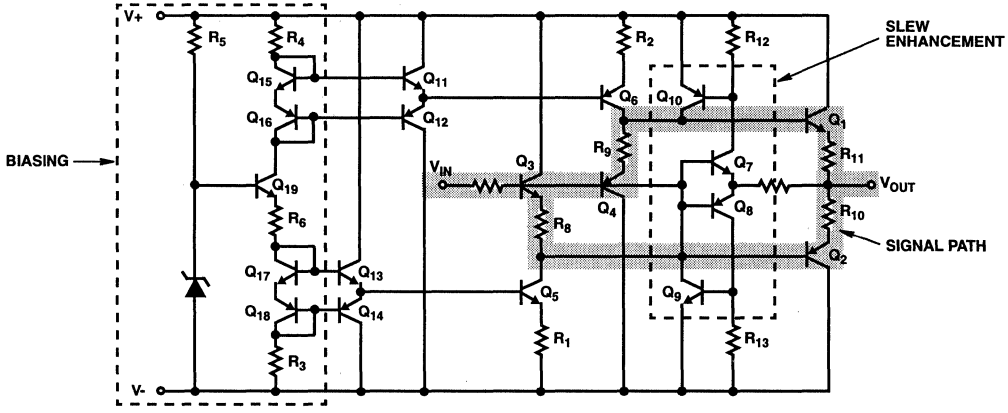


FIGURE 2. HA-5033 SCHEMATIC: VIDEO BUFFER DESIGN CONSISTS OF THREE OPERATING AREAS; SIGNAL PATH, BIAS NETWORK AND PERFORMANCE OPTIMIZATION CIRCUITRY.

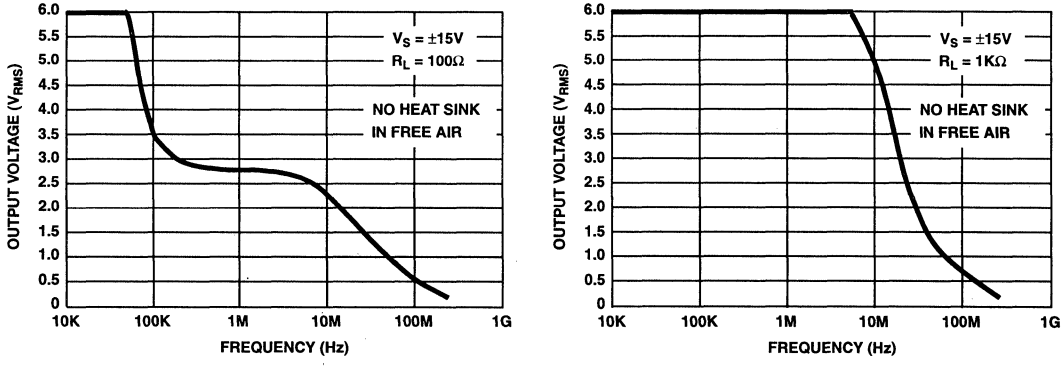


FIGURE 3. OUTPUT SWING vs FREQUENCY PERFORMANCE CURVES: CURVES SHOW POINT OF OBSERVABLE DISTORTION FOR GIVEN FREQUENCY. OPERATION BEYOND THE CURVES SHOWN WILL APPROACH CONDITIONS WHERE OUTPUT TRANSISTORS ARE SIMULTANEOUSLY ON. THE RESULTING INCREASE IN CHIP TEMPERATURE WILL LEAD TO THERMAL RUNAWAY.

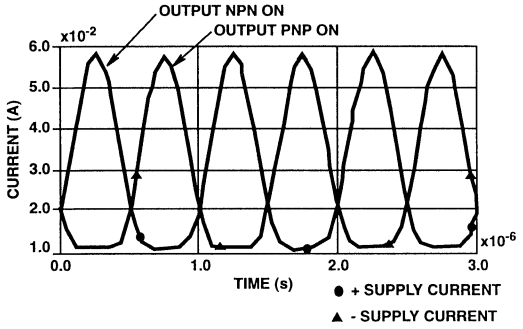


FIGURE 4A. V_{PEAK} = 5V, R_L = 100

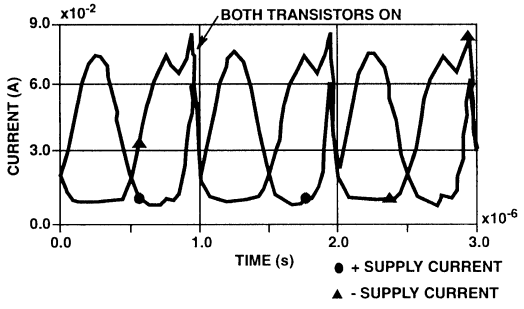


FIGURE 4B. V_{PEAK} = 7V, R_L = 100

FIGURE 4. OUTPUT TRANSISTOR COMPUTER SIMULATION RESULTS

This condition occurs if the frequency of the analog signal does not allow sufficient time for the output PNP transistor to turn off. The frequency which causes this "push-push" output stage can be determined by using the following relationship,

$$\text{Full Power Bandwidth (FPBW)} = \frac{SR}{2\pi V_{PEAK}}$$

Where: SR = Slew Rate
V_{PEAK} = Analog Signal Peak Voltage

Therefore, the designer can determine the approximate frequency of thermal runaway by supplying the peak analog voltage and measuring the buffer slew rate for a particular application.

For example, the slew rate for the HA-5033 with a load of R_L = 1kΩ and C_L = 1000pF was measured to be 83V/µs. The FPBW for a $5V_{PEAK}$ analog signal was calculated,

$$FPBW = \frac{83V/\mu s}{2\pi(5V)} = 2.6MHz$$

So the estimated frequency of thermal runaway for the given conditions is 2.6MHz. Measurements in the lab resulted in a thermal runaway frequency equal to 2.5MHz.

Although the FPBW relationship gives the designer a method of estimating the frequency of thermal runaway, it is recommended that the HA-5033 be operated to the left of the curves shown in Figure 3. Heat sinking the buffer will not prevent this condition from occurring.

The purpose of heat sinking a semiconductor is to maintain the device junction temperature below a specified maximum limit. This is a thermal problem and can be evaluated using the thermal analog of Ohm's Law illustrated in Figure 5.

Where:

P_{DMAX} = Power Dissipated (P_{DC} + P_{AC}), Watts
T_J = Maximum Junction Temperature, °C
T_A = Ambient Temperature, °C
θ_{JC} = Junction to Case Thermal Resistance, °C/W
θ_{CS} = Case to Heat Sink Thermal Resistance, °C/W
θ_{SA} = Heat Sink to Ambient Thermal Resistance, °C/W

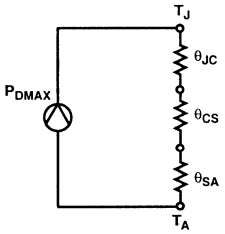


FIGURE 5. THERMAL ANALOG OF OHM'S LAW: SEMICONDUCTOR/HEAT SINK SYSTEM

In this thermal system, current is replaced by power, voltage by temperature, and electrical resistance by thermal resistance. By using Figure 5, the following expression is derived,

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

This expression allows the designer to determine the maximum power dissipation of a semiconductor/heat sink system.

The expression for the semiconductor in free air is,

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$$

In order to make use of these expressions, the following information is required. θ_{JC} and T_{JMAX}, from the semiconductor manufacturer and θ_{CS} and θ_{SA}, from the heat sink manufacturer.

For the HA-5033, the maximum junction temperature (T_{JMAX}) is 175°C for the metal can package, and 150°C for the PDIP and PSOP packages. The thermal impedances for the HA-5033 in the metal can package are θ_{JA} = 65°C/W and θ_{JC} = 34°C/W. The PDIP thermal resistance is θ_{JA} = 96°C/W, while the PSOP package has θ_{JA} = 129°C/W. These values have been used to generate the "Maximum Power Dissipation" graph in Figure 6.

Recommended heat sinks for the HA-5033 in the metal can package are the Thermalloy 2240A [1] and IERC-UP-T08-51CB [2] (base), IERC-UP-C7 (top). Thermal impedances

are θ_{SA} = 27°C/W and θ_{SA} = 10°C/W, respectively. θ_{CS} is dependent upon the type of insulator or thermal joint compound used. Both products are two piece heat sinks, but differ in design.

By using the given product information and supplying an operating ambient temperature, the designer can determine the maximum power the system will dissipate and not exceed the maximum junction temperature.

For example, Figure 6 shows the maximum power dissipation for the HA-5033 in a metal can package to be 2.31W at 25°C.

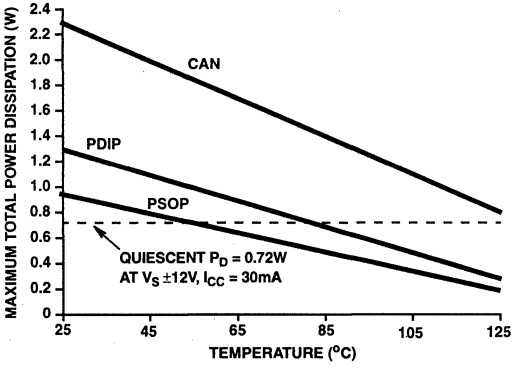


FIGURE 6. HA-5033 MAXIMUM POWER DISSIPATION VS AMBIENT TEMPERATURE: FREE AIR

The maximum power dissipation of the HA-5033/2240A metal can/heat sink system is calculated to be,

$$P_{DMAX} = \frac{175 - 25}{34 + 27} = 2.46$$

Therefore, the HA-5033 used with the Thermalloy 2240A can dissipate 2.46W at 25°C and not exceed the maximum junction temperature of 175°C.

The power dissipation limits shown in Figure 6 and those determined with the heat sink apply for both quiescent and load related power. Therefore,

$$P_{DMAX} \leq P_{DC} + P_{AC}$$

$$P_{DC} = (V+)(+I) + (V-)(-I)$$

$$P_{AC} = (1/T)_O \int T\ v(t)\ i(t)\ dt$$

Video Performance

The images which appear on your television picture tube are created by a process called scanning [3]. Scanning is a method of recreating the optical image of a scene one line at a time. Referring to Figure 7A, an electron beam moves or "scans" from left to right and quickly returns to a position below its starting spot. This process continues until the bottom of the picture is reached and the beam returns to the original top left hand position. This method is called sequential scanning.

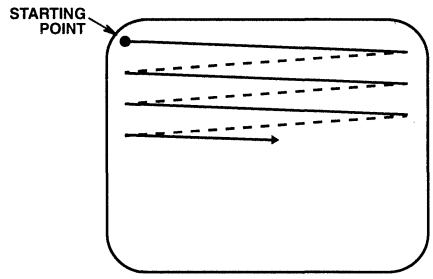


FIGURE 7A. SEQUENCIAL SCANNING

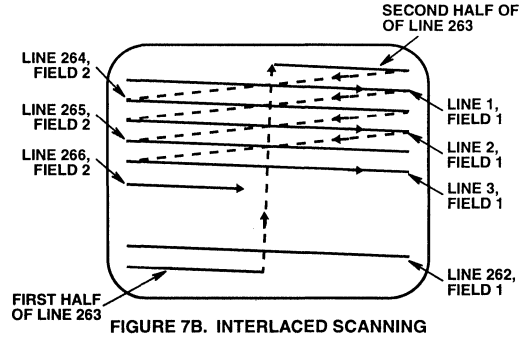


FIGURE 7B. INTERLACED SCANNING

FIGURE 7. SCANNING SEQUENCE

Incorporated into present television broadcast standards is a technique called interlaced scanning. Interlaced scanning recreates the scene by providing two half scans. As shown in Figure 7B, the first scan traces out the odd numbered lines, the second scan fills in the even numbered lines. This technique avoids the flicker problem and excessive bandwidths required for similar picture definition using sequential scanning.

The United States NTSC (National Television Systems Committee) broadcast standard is a 525 line standard. Each scan consists of 2621/2 lines. The first scan is known as field one, the second, field two. Therefore, the complete picture consists of two fields.

The first 21 lines of each field are blank. Those lines are left open and are not used to broadcast video information. Instead, these lines contain other important information, such as sync pulses, data transmission, and test signals. The test signals contained in these lines are called the Vertical Interval Test Signals (VITS) [4, 5], which allows realtime monitoring of the television broadcast signal quality. These test signals were used to evaluate the video performance of the HA-5033.

Four test signals are commonly used in the vertical interval. They are the multiburst, color bar, composite and vertical interval reference. These test signals are shown in Figures 8 through 11.

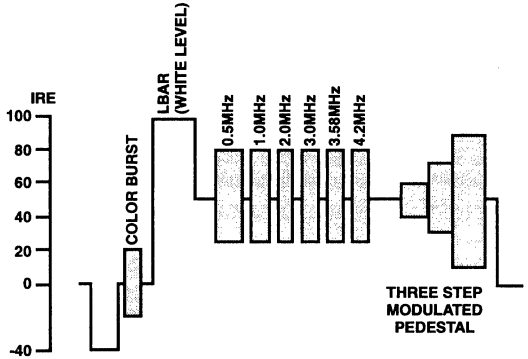


FIGURE 8. MULTIBURST SIGNAL (FIELD 1, LINE 17) ALLOWS FREQUENCY RESPONSE CHECKS

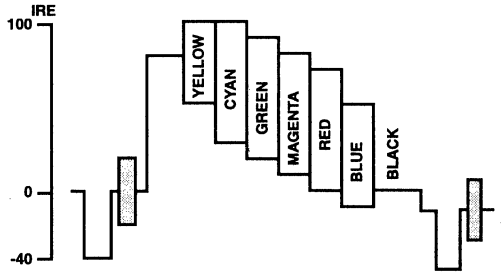


FIGURE 9. COLOR BAR (FIELD 2, LINE 17) ENABLES MONITORING OF COLOR TRANSMISSION QUALITY

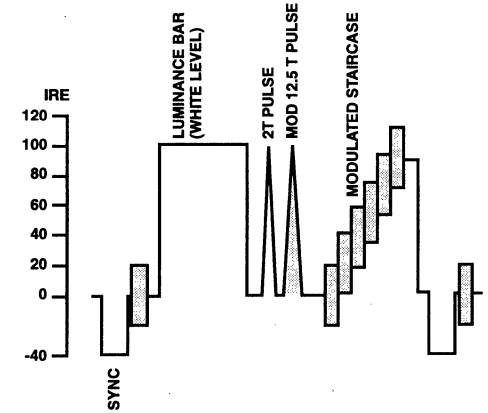


FIGURE 10. COMPOSITE SIGNAL (FIELD 1, AND 2, LINE 18) DESIGNED FOR GAIN AND TIME DELAY TESTS

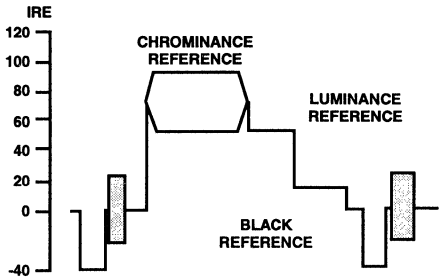
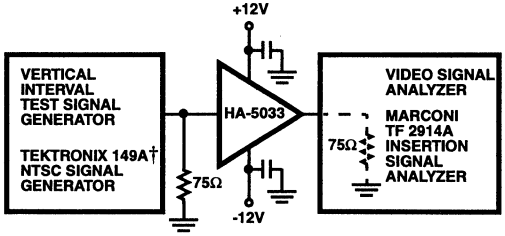


FIGURE 11. VERTICAL INTERVAL REFERENCE SIGNAL (FIELD 1 AND 2, LINE 19) PROVIDES COLOR AND GAIN REFERENCES

Each test signal was created to allow various distortions to be measured without interfering with the normal video transmission. These signal distortions which exist in television systems are defined as linear or non-linear. Non-linear distortion, such as differential phase and gain, vary with the amplitude of the picture signal. Linear distortions, usually dependent upon frequency response, are independent of signal level. For example, the multiburst test signal is very useful for frequency response checks, whereas the composite signal contains signals for checking gain error.

Determining the HA-5033's performance level with respect to the NTSC standard required the definition of a measurement method. Test equipment was needed that would produce the necessary NTSC test signals and also monitor the device under test performance. The test configuration, shown in Figure 12 consisted of a Tektronix 149A NTSC [6] generator and Marconi TF 2914A video analyzer [7].



†TEKTRONIX 1910 NTSC DIGITAL GENERATOR RECOMMENDED

FIGURE 12. HA-5033 NTSC PERFORMANCE TEST CONFIGURATION

The TF 2914A has the capability of measuring 24 separate video parameters. Other advantages include direct readout and much more accuracy than possible using scope methods. Table 2 lists the video parameters tested on the HA-5033 along with the particular VITS utilized by the TF 2914A.

TABLE 2. TF 2914A VIDEO MEASUREMENT PARAMETERS REFERRED TO VERTICAL INTERVAL TEST SIGNALS

VIDEO PARAMETER	VERTICAL INTERVAL TEST SIGNAL USED
Luminance Bar Amplitude	Luminance Bar, Composite Signal (Figure 10)
Sync Amplitude	Sync Pulse, Composite Signal (Figure 10)
2T Pulse to Bar Ratio	2T Pulse/Luminance Bar, Composite Signal (Figure 10)
Chrominance to Luminance Gain Inequality	Chrominance Component Amplitude of the 12.5T Pulse and Luminance Components of the 12.5T Pulse, Composite Signal (Figure 10)
Chrominance to Luminance Delay	Time Difference of Chrominance and Luminance Components of the 12.5T Pulse, Composite Signal (Figure 10)
Luminance Non-Linearity	Largest and Smallest Step Amplitude of the Modulated Step Staircase, Composite Signal (Figure 10)
Signal to Noise Ratio	Luminance Bar Level to Noise Voltage, Composite Signal (Figure 10)
Chrominance to Luminance Crosstalk	Chrominance Component of 3 Step Modulated Pedestal and Luminance Bar, Multiburst Signal (Figure 8)
Low Frequency Error	Amplitude of Low Frequency Signals
Bar Tilt	Difference of Luminance Bar Amplitude, Composite Signal (Figure 10)
2T K Factor	2T Pulse, Composite Signal (Figure 10)
Differential Gain	Amplitude Deviation of Modulated Step Staircase, Composite Signal (Figure 10)
Differential Phase	Phase Deviation of Modulated Step Staircase, Composite Signal (Figure 10)
Flag	Luminance Amplitude, Multiburst Signal (Figure 8)
Multiburst 1-6	Amplitude of Each Frequency Burst, Multiburst Signal (Figure 8)
Color Reference Burst Amplitude	Color Burst Amplitude, Multiburst Signal (Figure 8)

Since the TF 2914A measurement includes any inaccuracies of the NTSC signal generator, a "delta" measurement was neccesary. The NTSC generator was connected directly to the analyzer and the results recorded. Next, the HA-5033 was inserted and the results recorded. The difference between the two readings was considered the actual HA-5033 performance. Table 3 lists the video performance results of the HA-5033.

TABLE 3. HA-5033 NTSC VIDEO PERFORMANCE

VIDEO PARAMETER	HA-5033	UNITS
Luminance Bar Amplitude	93.6	IRE (Note)
Sync Amplitude	37.5	IRE
2T Pulse to Bar Ratio	99.9	IRE
Chrominance to Luminance Gain Inequality	99.9	IRE
Chrominance to Luminance Delay	1.5	ns
Luminance Non-Linearity	0.1	%
Signal-to-Noise Ratio	66	dB
Chrominance to Luminance Crosstalk	51.6	IRE
Low Frequency Error	0.3	mV
Bar Tilt	0.3	IRE
2T K Factor	0.1	K
Differential Gain	0.1	%
Differential Phase	0.1	Degree
Flag	99.5	IRE
Multiburst 1 Amplitude	49.2	IRE
Multiburst 2 Amplitude	49.3	IRE
Multiburst 3 Amplitude	51.0	IRE
Multiburst 4 Amplitude	50.4	IRE
Multiburst 5 Amplitude	49.7	IRE
Multiburst 6 Amplitude	50.0	IRE
Color Reference Burst Amplitude	40.4	IRE

NOTE: IEEE Standard 205-1958 defines the levels of television video signal in terms of IRE units. 100 IRE units = $0.714V_{P-P}$

Applying the HA-5033

The most important consideration when designing with the HA-5033 is layout. The wide bandwidth of the buffer necessitates that high frequency layout procedures be followed. Recommended procedures include the use of a ground plane, minimization of all lead lengths, avoiding sockets, and proper power supply decoupling.

Standard practice in RF/Video layout is the use of a ground plane. A ground plane minimizes distributed circuit capacitance and inductance which degrade high frequency performance. The ground plane can also incorporate the metal case of the HA-5033, since pin 2 is internally tied to the package. This feature allows the user to make contact between the ground plane and the package which extends shielding, provides additional heat sinking and eliminates the use of a socket. IC sockets contribute bandwidth limiting interlead capacitance and should be avoided.

For the PDIP, additional heatsinking can be derived from soldering the no connection leads 2, 3, and 7 to the ground plane. Also, lead 6 can be tied to either supply, grounded or left open. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Another method of enhancing device performance is power supply decoupling. For the HA-5033, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1mF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1mF or larger will optimize low frequency performance. It is also recommended that the bypass capacitors be connected as close to the HA-5033 as possible, preferably directly to the supply pins.

Finally, keeping all lead lengths as short as possible will minimize distributed capacitance and reduce board space. It is essential that the guidelines discussed above be followed to avoid marginal performance.

Another consideration when applying the HA-5033 is load capacitance. Although the HA-5033 is designed to handle load capacitance values up to 0.01μF, it has a worst case stability region in the area of 50pF. The computer simulation of the HA-5033 frequency response in Figure 13 illustrates the gain peaking which occurs in the 150MHz region.

There are three suggested methods of dealing with this particular characteristic of the HA-5033. Isolating the load capacitance from the buffer output is the object of the first

method. This is accomplished by placing a series resistor between the output and the load.

A second technique utilizes the HA-5033 frequency response with respect to load capacitance. Referring once again to Figure 13, notice that the gain peaking is removed with additional load capacitance. This is the basis of method two, adding additional load capacitance to approach a region of stability.

A drawback to adding more load capacitance is that the buffer's dynamic characteristic will degrade and bandwidth performance will be less than data sheet specifications. The third method solves this trade-off by using a "bootstrap" technique of adding capacitance from input to output. This method achieves stability without sacrificing performance.

An explanation of why adding capacitance will stabilize the HA-5033 can be found in the Y parameter data shown in Figure 14. The expression for the buffer gain in terms of Y parameter is:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{-Y_{21}}{Y_{22}+Y_L}$$

Y_{21} = Forward Transmittance
Y_{22} = Output Admittance
Y_L = Load Admittance

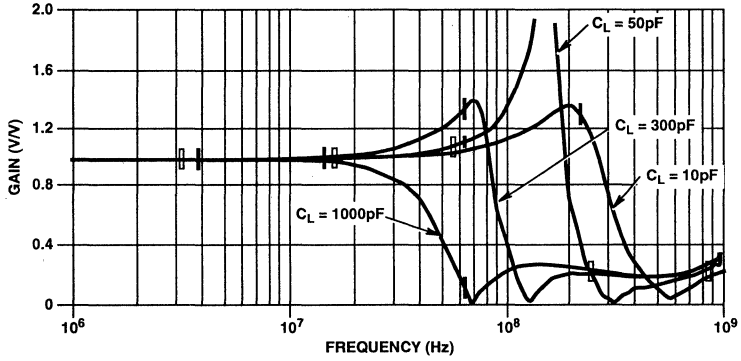
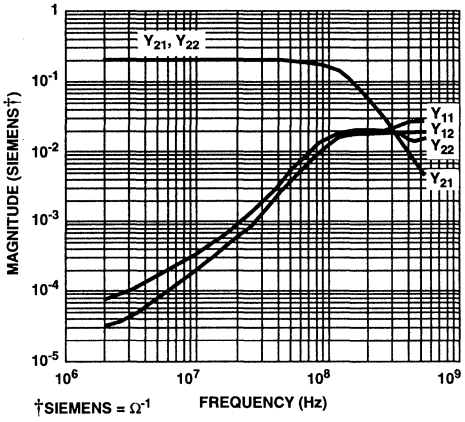


FIGURE 13. COMPUTER SIMULATION OF HA-5033 GAIN CHARACTERISTICS vs FREQUENCY AND LOAD CAPACITANCE



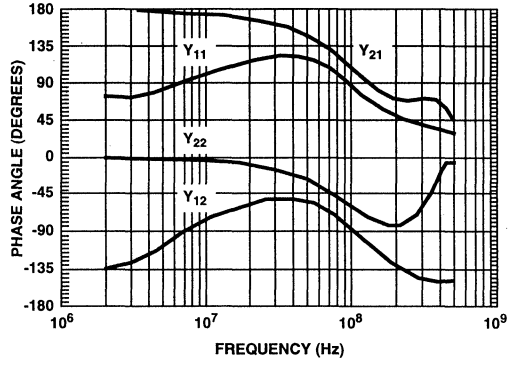


FIGURE 14. HA-5033 Y PARAMETER DATA

Notice that the output admittance, Y_{22}, phase becomes inductive ($-jY_L = -90^o$) at high frequency. So if the load, Y_L, is capacitive ($+jY_C = +90^o$) and the sum of $Y_{22} + Y_L$, become small, peaking occurs. Adding additional capacitance changes the effective phase angle and peaking can be reduced.

Using the HA-5033 as the analog input buffer of a flash converter is an example of an application where the suggested stabilization methods are useful. Although it has been stressed to keep all distributed capacitance to a minimum to optimize device operation, the load which a flash converter presents to the buffer represents a greater concern.

Flash or parallel converters are a special case, since the analog input circuit must drive a non-linear input impedance [8]. This non-linearity is due to the potential input impedance changes of the 255 parallel comparators which comprise the converter analog input. In addition to the non-linearity, the input capacitance of these converters tends to be relatively large, 100-300pF.

Examples of the various stabilization methods tested with the TRW 1007 8-bit video flash converter are shown in Figure 15. Figure 15A illustrates the series resistor method, Figure 15B is the load capacitance method, and Figure 15C is the bootstrap method. Photographs of the experimental results show the analog input sampling convert signal (pin 30), the MSB digital output (D1, pin 40), and the buffer output (converter input).

It is recommended that a complete evaluation for each method be conducted to determine the optimum component values. The value of the series resistor will depend upon the input capacitance of the particular converter used. A suggested starting value is 50Ω. With the capacitance methods, the distributed capacitance of the layout will affect component values. These experimental results were obtained using C = 240pF.

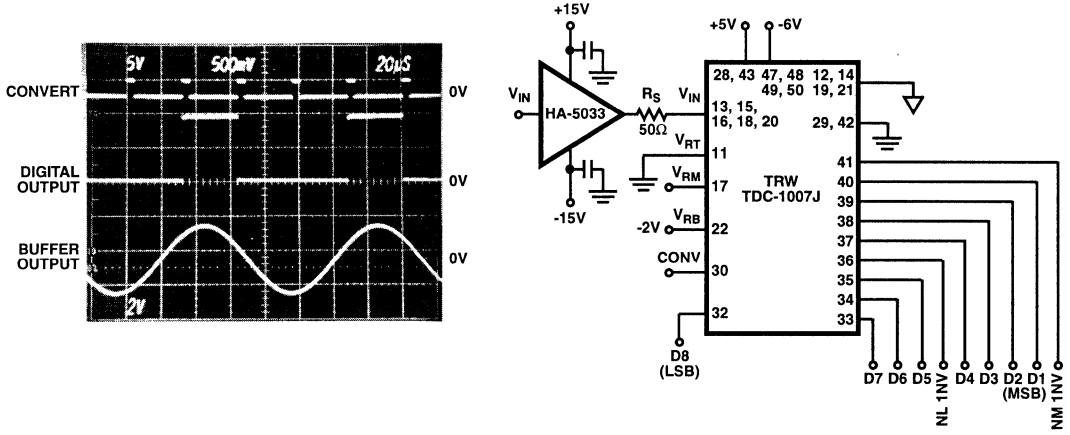


FIGURE 15A. ENHANCING 5033 PERFORMANCE IN FLASH CONVERTER APPLICATIONS: SERIES RESISTOR METHOD

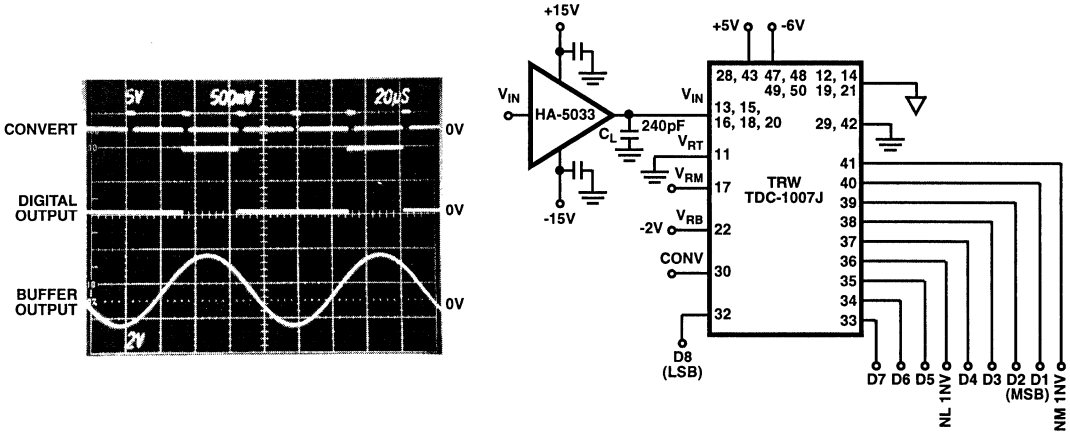


FIGURE 15B. LOAD CAPACITANCE METHOD

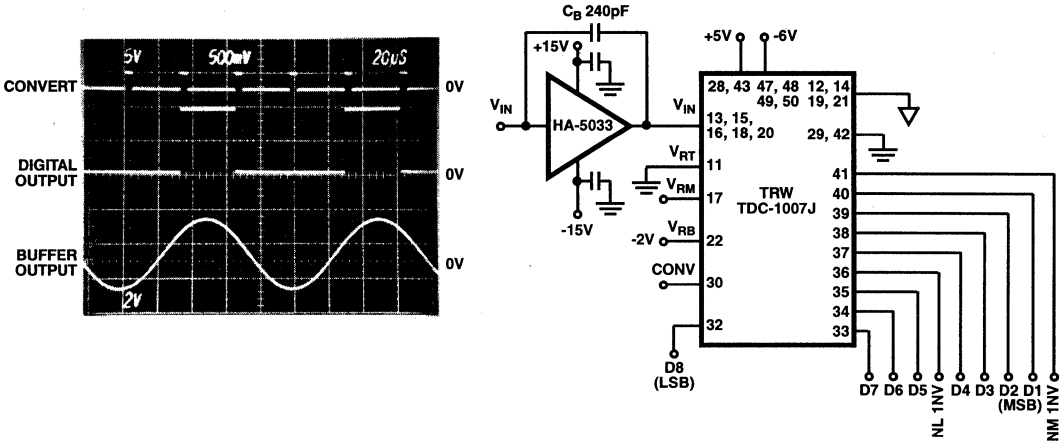
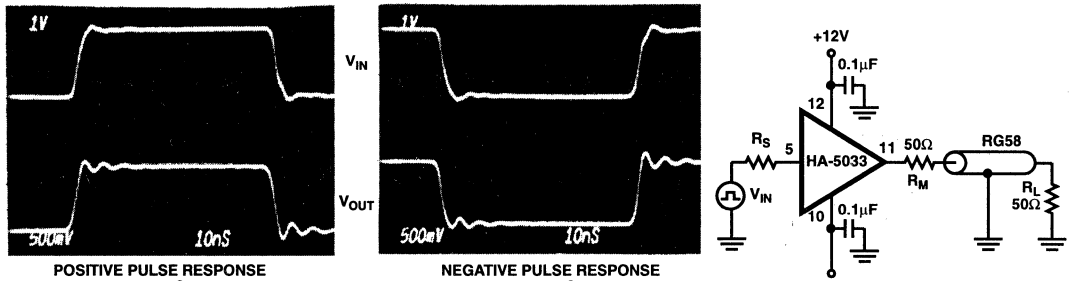


FIGURE 15C. BOOTSTRAP CAPACITANCE METHOD



POSITIVE PULSE RESPONSE
$T_A = 25°C$
$R_S = 50Ω$
$R_M = R_L = 50Ω$

$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = 1/2V_{IN}$$

NEGATIVE PULSE RESPONSE
$T_A = 25°C$
$R_S = 50Ω$
$R_M = R_L = 50Ω$

$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = 1/2V_{IN}$$

FIGURE 16. VIDEO COAXIAL LINE DRIVER - 50Ω SYSTEM

The signal levels in most video applications are $1V_{P-P}$ or less. Although the HA-5033 was shown with ±15V power supplies in the converter applications, lower power supplies will accommodate these video signal levels. For example, at ±5V power supplies, the HA-5033 can swing ±2V into a 75Ω load.

The HA-5033 is an excellent high speed line device capable of driving 50Ω and 75Ω coaxial cable.

These types of drive requirements are common in video circuit design. Figures 16 and 17 illustrate two typical application examples. Figure 16 is an example of a 50Ω system using the HA-5033 alone. R_M matches the buffer output impedance to the cables characteristic impedance. Depending upon the response required, this resistor may not be necessary. If used, the output voltage will be one-half the input voltage.

Figure 17 illustrates the use of the buffer within the feedback loop of an operational amplifier. This configuration provides additional output current capability for the HA-2539 op amp and gives the designer voltage gain control.

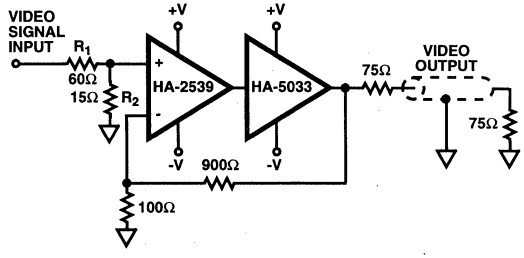


FIGURE 17. VIDEO GAIN BLOCK

Another application which utilizes the HA-5033's output drive capability is the high speed sample and hold circuit shown in Figure 18. The input buffer provides drive current to the hold capacitor while the output buffer functions as a data line

driver. The switching element in this application is the HI-201HS high speed CMOS switch which contributes it's own benefits to the application [9]. Depending upon the application requirements, using the HA-5033 as the output buffer in Figure 18A may not be acceptable. Lab tests have shown that the input bias current of the HA-5033 becomes a factor for low values of hold capacitance (<0.01μF) during the hold mode.

A solution is to add a low bias current FET input stage, as shown in Figure 18B. Q_1 acts as a voltage follower and Q_2 is a current source. Matching Q_1, Q_2 and R_1, R_2 are important considerations in order to minimize offset voltages.

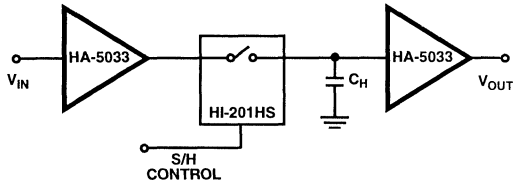


FIGURE 18A. HIGH SPEED SAMPLE/HOLD

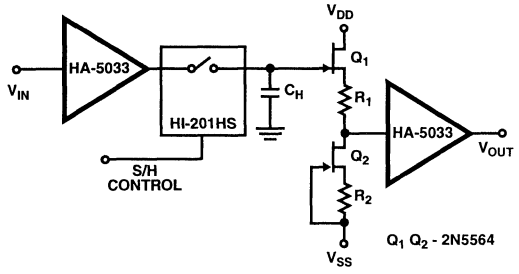


FIGURE 18A. MODIFIED OUTPUT BUFFER

When the drive capability of the HA-5033 is insufficient, consider adding an external output stage. Figure 19A illustrates an example where a push-pull complementary output stage has been added to the HA-5033. Although unable to drive the low impedances of speakers, typically 4Ω to 8Ω, the buffer can be used to drive audio output transistors. A variation of this configuration is shown in Figure 19B, where separate buffers individually drive each transistor base. A low noise input stage is provided by the HA-5102.

A common method of achieving an audio oscillator circuit is to use a transistor or IC amplifier with LC or RC feedback. An alternative technique of generating sinusoidal waveforms, using the HA-5033, is shown in Figure 20. Crystal oscillators offer improved frequency stability over time and temperature. This particular oscillator configuration [10] produces an 18.18MHz, $2.8V_{P-P}$ sinusoidal waveform into a 1kΩ load.

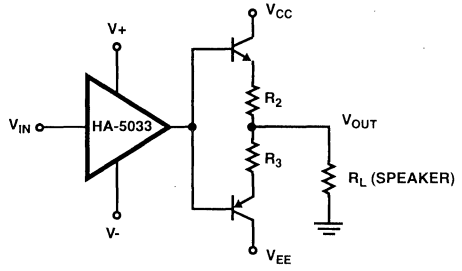


FIGURE 19A.

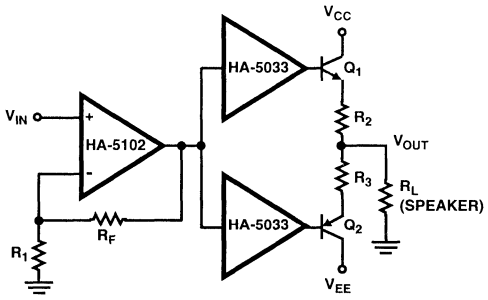


FIGURE 19B.

FIGURE 19. AUDIO DRIVERS

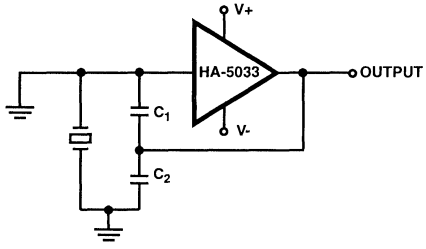


FIGURE 20. CRYSTAL OSCILLATOR: $V_S = \pm 15V$, $C_1 = 12pF$, $C_2 = 39pF$, 18MHz QUARTZ CRYSTAL

Conclusion

The HA-5033 is a high performance integrated circuit presently being utilized in a wide variety of applications. This paper has provided additional information to aid designers in applying the HA-5033 video buffer in future applications.

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Further Reading

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Acknowledgments

1. Technical contributions of John Prentice and Robert Junkins.

2. Sales and Technical Staff of Marconi Instruments.

NOTE: Information contained in application notes is intended solely for general guidance; use of the information for user's specific application is at user's risk.

Harris Semiconductor

APPNOTE

No. AN551.1 November 1996

Harris Linear

Recommended Test Procedures for Operational Amplifiers

Authors: Wes Kilgore and Brian Mathews

Introduction

The following text describes the basic test procedures that can be used for most Harris Op Amps. Note that all measurement conversions have been taken into account in the equations stated.

1. Offset Voltage

The offset voltage (V_{IO}) of the amplifier under test (AUT) is measured via Test Circuit 1 as follows:

1. Set V+ and V- supplies to values specified in Table 1, Column (1) and V_{DC} to 0V.
2. Close S_1 and S_2, open S_3.
3. Choose: R_F = 50K for non-precision amplifiers.
   R_F = 5M for precision amplifiers.
4. Measure voltage at E in volts (label as E_1).
   $V_{IO} = E_1$ (mV) for R_F = 50K, or
   $V_{IO} = E_1$ *10 (μV) for R_F = 5M

The gain of this circuit with R_F = 50K (R_F = 5M) requires the output to be driven to 1000 (100,000) times the offset voltage necessary to maintain the output of the AUT at 0V. Note that the AUT output is always identical to V_{DC}. Overall circuit stability is maintained by the adjustable feed-back capacitor C_A.

2. Input Bias Current

The bias current flowing in or out of the positive terminal of the AUT (I_{B}+) is obtained using Test Circuit 1 by:

1. Measuring E_1 as in procedure 1 (use R_S = 100K for JFET input devices).
2. Maintain V_{DC} at 0V.
3. Close S_2, open S_1 and S_3.
4. Measuring voltage at E in volts (label as E_2).
   $I_{B+} = (E_1 - E_2) \times 100$ (nA) for R_F = 50K, R_S = 10K, or
   $I_{B+} = (E_1 - E_2) \times 10$ (nA) for R_F = 50K, R_S = 100K

The bias current flowing in or out of the negative terminal (I_{B-}) is found by:

1. Following steps 1 and 2 for I_{B}+.
2. Close S_1, open S_2 and S_3.
3. Measuring voltage at E in volts (label as E_3).
   $I_{B-} = (E_1 - E_3) \times 100$ (nA) for R_F = 50K, R_S = 10K, or
   $I_{B-} = (E_1 - E_3) \times 10$ (nA) for R_F = 50K, R_S = 100K

3. Input Offset Current

Using Test Circuit 1, the input offset current (I_{IO}) of the AUT is determined by:

1. Measuring E_1 as in procedure 1.
2. Maintaining V_{DC} at 0V.
3. Open S_1, S_2 and S_3.
4. Measuring voltage at E in volts (label as E_4).
   $I_{IO} = (E_1 - E_4) \times 100$ (nA) for R_F = 50K, R_S = 10K, or
   $I_{IO} = (E_1 - E_4) \times 10$ (nA) for R_F = 50K, R_S = 100K

4. Power Supply Rejection Ratio

Both positive and negative PSRRs are measured via Test Circuit 1. For PSRR+:

1. Close S_1 and S_2, open S_3.
2. Choose: R_F = 50K
3. Set V_{DC} = 0, V+ = 10V, and V- = -15V.
4. Measure voltage at E in volts (label as E_5).
5. Change V+ to +20V.
6. Measure voltage at E in volts (label as E_6).

$$PSRR+ = 20 \log_{10}\left|\frac{10^4}{E_5 - E_6}\right| \text{(dB) for } R_F = 50K$$

Similarly for PSRR-:

1. Follow steps 1 and 2 for PSRR+ above.
2. Set V_{DC} = 0V, V+ = +15V, V- = -10.
3. Measure voltage at E in volts (label as E_7).
4. Change V- to -20V.
5. Measure voltage at E in volts (label as E_8).

$$PSRR- = 20 \log_{10}\left|\frac{10^4}{E_7 - E_8}\right| \text{(dB) for } R_F = 50K$$

5. Common Mode Rejection Ratio

The CMRR is determined by adjusting Test Circuit 1 as follows:

1. Close S_1 and S_2, open S_3.
2. Choose: R_F = 50K

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3. Set V+ = +5V, V- = -25V, and V_{DC} = -10V.
4. Measure voltage at E in volts (label as E_9).
5. Set V+ = 25V, V- = -5V, and V_{DC} = 10V.
6. Measure voltage at E in volts (label as E_{10}).

$$CMRR = 20 \log_{10}\left|\frac{2\times10^4}{E_9 - E_{10}}\right| \text{(dB) for } R_F = 50K$$

6. Output Voltage Swing

Test Circuit 2 is adjusted to measure V_{OUT}+ and V_{OUT}- the procedure is:

1. Select appropriate V+ and V- supply values from Table 1, Column 1.
2. Select specified R_L from Table 1, Column 2.
3. Set V_{IN} = 0.5V.
4. Measure voltage at E in volts. V_{OUT+} = E (V)

Similarly V_{OUT-} is found by:

1. Selecting specified R_L from Table 1, Column 1.
2. Setting V_{IN} = -0.5V.
3. Measuring voltage at E in volts. V_{OUT-} = E (V)

7. Output Current

The output current corresponding to the output voltage of procedure 6 is found by:

1. Measuring V_{OUT-} and V_{OUT+} as in procedure 6.

$$I_{OUT} = \frac{V_{OUT+}}{R_L} \text{ where } R_L \text{ is from Table 1, Column 2.}$$

$$I_{OUT} = \frac{V_{OUT-}}{R_L} \text{ where } R_L \text{ is from Table 1, Column 2.}$$

8. Open Loop Gain

Both positive (A_{VOL}+) and negative (A_{VOL}-) open loop gain measurements are determined by adjusting Test Circuit 1.

For A_{VOL}+:

1. Close S_1, S_2 and S_3.
2. Select specified R_L from Table 1, Column 3.
3. Set R_F = 50K.
4. Set V_{DC} = 0V, V+ = +15V, and V- = -15V.
5. Measure voltage at E in volts (label as E_{13}).
6. Set V_{DC} = 10V.
7. Measure voltage at E in volts (label as E_{14}).

$$A_{VOL+} = \frac{10}{E_{14} - E_{13}} \text{(V/mV) for } R_F = 50K$$

For A_{VOL}-:

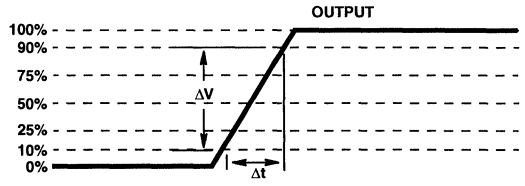
1. Follow steps 1, 2, 3, 4, and 5 above.
2. Set V_{DC} = -10V.
3. Measure voltage at E in volts (label as E_{15}).

$$A_{VOL-} = \frac{10}{E_{13} - E_{15}} \text{(V/mV) for } R_F = 50K$$

9. Slew Rate

Test Circuit 3 is used for measurement of positive and negative slew rate. For SR+:

1. Select specified R_L, A_{CL}, and C_L from Table 1, Columns 4, 5 and 6.
2. Apply a positive step voltage to V_{AC} (refer to data book for test waveform).
3. Observe ΔV and Δt at E. A standard approach is to use the 10% and 90% points or else the 25% and 75% points on the waveform.



$$SR = \frac{\Delta V}{\Delta t}$$

For SR- repeat above procedure with negative input pulse.

$$SR- = \frac{\Delta V}{\Delta t}$$

10. Full Power Bandwidth

Full power bandwidth is calculated by:

1. Measuring slew rate as above in procedure 9.
2. Measuring V_{OUT+} as in procedure 6. (Typically V_{OUT+} is assumed to be the guaranteed minimum V_{OUT}, usually 10V.)

$$FPBW = \frac{SR+}{2\pi V_{OUT(PEAK)}}$$

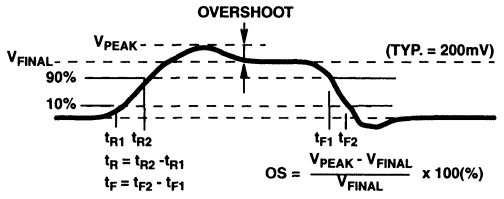
11. Rise Time, Fall Time and Overshoot

The small signal step response of the AUT is determined via Test Circuit 3. The procedure requires:

1. Selecting the appropriate R_L, A_{CL}, and C_L from Table 1, Columns 4, 5 and 6.
2. Applying a positive input step voltage for rise time t_R and positive overshoot OS+.

   Applying a negative input step voltage for fall time t_F and negative overshoot OS-.

   (Refer to data book for input waveforms.)
3. Observe output of AUT noting the key points as shown.



12. Settling Time

Test Circuit 6 is appropriate for settling time (t_S) measurement, the procedure is:

1. Select R_1 and R_2 such that AUT is at the A_{CL} stated in Table 1, Column 5.
2. Select R_3 and R_4 so that $R_3 \geq 2R_1$ and $R_4 \geq 2R_2$ with the condition that the ratio

$$\frac{R_3}{R_4} = \frac{R_1}{R_2}$$ be maintained.

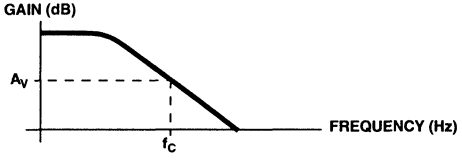
3. Apply step voltage as specified in data book.
4. Measure the time from t_1 (time input step applied) to t_2 (the time E_S settles to within a specified percentage of V_{OUT} - see data book). $t_S = t_2 - t_1$

NOTE: Clipping diodes of Test Circuit 6 prevent overdrive of oscilloscope. (Recommend fast Schottky diodes.)

13. Gain Bandwidth Product

Test Circuit 4 is used for measuring GBP. The procedure is:

1. Sweep V_{IN} thru the required frequency range.
2. With a network analyzer view gain (dB) versus frequency as below.

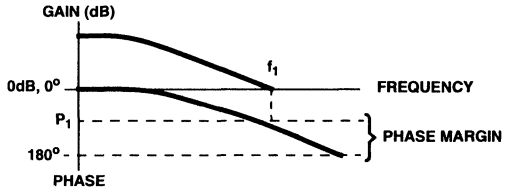


3. At the voltage gain of interest (A_V) determine the corresponding frequency f_C. Note that chosen A_V must be greater than or equal to that stated in column 5 of Table 1. GBP = $A_V \times f_C$ (Hz) where A_V is in V/V.

14. Phase Margin (Network Analyzer Method)

Test Circuit 4 is used to obtain phase margin measurement. The procedure is:

1. Sweep V_{IN} thru the required frequency range.
2. Display gain in dB and phase in degrees versus frequency on analyzer as shown.



3. At a gain of 0dB (if $A_{CL} = 1$ in Table 1, column 5), record frequency f_1 and corresponding phase P_1.
   Phase margin = 180 degrees - P_1 degrees.

15. Input Noise Voltage

Test Circuit 5 is designed for measuring input noise voltage. Use of the Quantec Noise Analyzer is recommended to obtain measurements at 1Hz bandwidth around a specific center frequency. The procedure is:

1. Set $R_G = 0$
2. Set circuit card to gain of 10.
3. Select measurement frequency of interest.
4. Record noise voltage (label as E_{n1}). Units are nV/$\sqrt{Hz}$.

16. Input Noise Current

Using Test Circuit 5, the input noise current is obtained by:

1. Measure E_{n1} as above for the desired frequency of interest.
2. Adjust R_G so that $V_O > 2E_{n1}$ (label V_O as E_{n2}).

$$I_n = \sqrt{\frac{(E_{n2})^2 - (E_{n1})^2 - 4kTR_G}{R_G^2}}$$

Where $K = 1.38 \times 10^{-23}$ (Boltzmann's Constant)
$T = 300°C$ (27°C)

17. Channel Separation (Crosstalk)

Test Circuit 7 is used to measure channel separation (CS). The procedure is as follows:

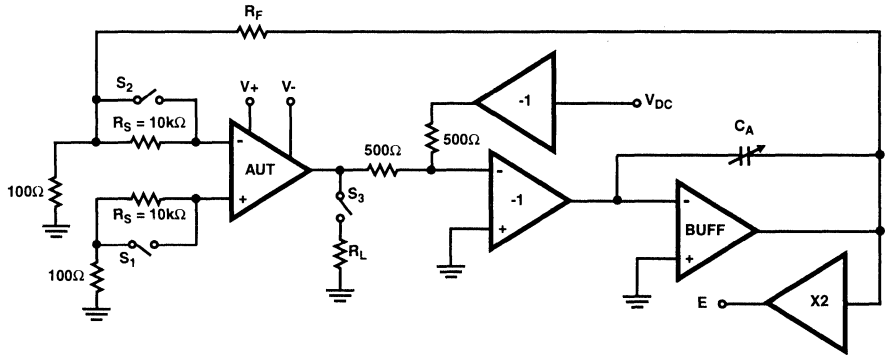
1. Apply V_{IN} at the frequency of interest to input of channel 1.
2. Select R_L from Table 1, column 4.
3. Measure V_{O1}.
4. Measure V_{O2} of channel 2.

$$CS = 20 \log_{10} \left| \frac{V_{O2}}{100V_{O1}} \right| dB$$

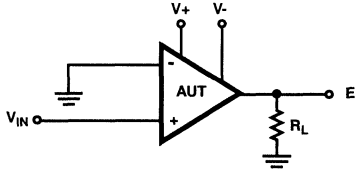
TABLE 1.

PART NUMBER	(1) SUPPLY VOLTAGE (V_S)	PARAMETERS TO MEASURE				
		(2) V_{OUT} $R_L(k\Omega)$	(3) A_{VOL} $R_L(k\Omega)$	SLEW RATE, OS, t_R, t_F		
				(4) $R_L(k\Omega)$	(5) A_{CL}	(6) $C_L(pF)$
HA-2400/04/05	±15	2	2	2	1	50
HA-2500/02/05	±15	2	2	2	1	50
HA-2510/12/15	±15	2	2	2	1	50
HA-2520/02/05	±15	2	2	2	3	50
HA-2539	±15	1	1	1	10	10
HA-2540	±15	1	1	1	10	10
HA-2541	±15	2	2	2	1	10
HA-2542	±15	1	1	1	2	10
HA-2600/02/05	±15	2	2	2	1	100
HA-2620/02/05	±15	2	2	2	5	50
HA-2640/05	±40	5	5	5	1	50
HA-4741	±15	10	2	2	1	50
HA-5101	±15	2	2	2	1	50
HA-5102/04	±15	2	2	2	1	50
HA-5111	±15	2	2	2	10	50
HA-5112/14	±15	2	2	2	10	50
HA-5127	±15	0.6	2	2	1	50
HA-5130/05	±15	0.6	2	2	1	100
HA-5134	±15	2	2	2	1	50
HA-5137	±15	0.6	2	2	5	50
HA-5141/12/14	+5/0	50	50	50	1	50
HA-5147	±15	0.6	2	2	10	50
HA-5151/12/14	±15	10	10	10	1	50
HA-5160/62	±15	2	2	2	10	50
HA-5170	±15	2	2	2	1	50
HA-5180	±15	2	2	2	1	50
HA-5190/95	±15	0.2	0.2	2	5	10

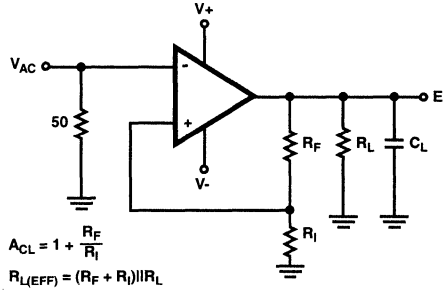
Test Circuits



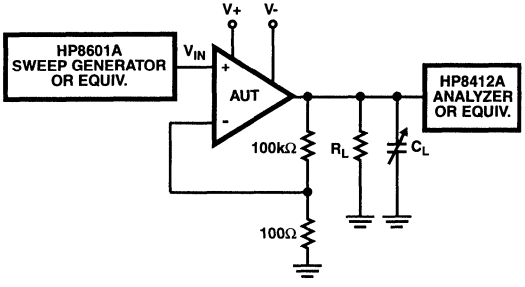
TEST CIRCUIT 1



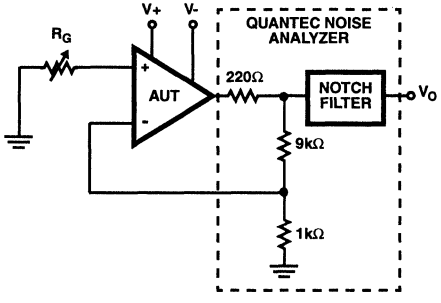
TEST CIRCUIT 2



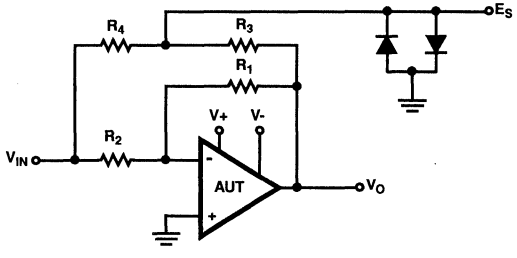
TEST CIRCUIT 3



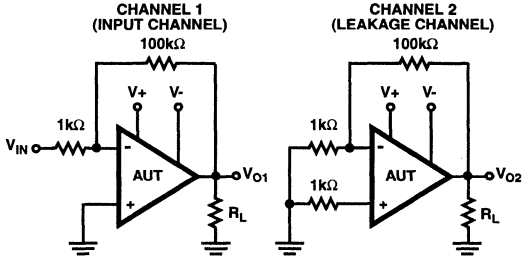
TEST CIRCUIT 4



TEST CIRCUIT 5



TEST CIRCUIT 6



TEST CIRCUIT 7

Harris Semiconductor

APPNOTE

No. AN6668.1 November 1996

Harris Linear

Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers

Author: H.A. Wittlinger

Introduction

The CA3080 and CA3080A are similar in generic form to conventional operational amplifiers, but differ sufficiently to justify an explanation of their unique characteristics. This new class of operational amplifier not only includes the usual differential input terminals, but also contains an additional control terminal which enhances the device's flexibility for use in a broad spectrum of applications. The amplifier incorporated in these devices is referred to as an Operational Transconductance Amplifier (OTA), because its output signal is best described in terms of the output-current that it can supply:

$$\text{Transconductance } g_M = \frac{\Delta i_{OUT}}{\Delta e_{IN}}$$

The amplifier's output-current is proportional to the voltage difference at its differential input terminals.

This Application Note describes the operation of the OTA and features various circuits using the OTA. For example, communications and industrial applications including modulators, multiplexers, sample-and-hold-circuits, gain control circuits and micropower comparators are shown and discussed. In addition, circuits have been included to show the operation of the OTA being used in conjunction with CMOS devices as post-amplifiers.

Figure 1 shows the equivalent circuit for the OTA. The output signal is a current which is proportional to the transconductance (g_M) of the OTA established by the amplifier bias current (I_{ABC}) and the differential input voltage (e_{IN}). The OTA can either source or sink current at the output terminal, depending on the polarity of the input signal.

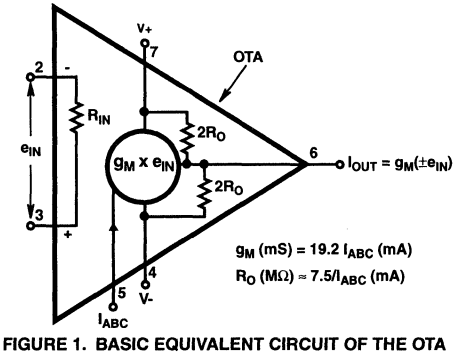


FIGURE 1. BASIC EQUIVALENT CIRCUIT OF THE OTA

The availability of the amplifier bias current (I_{ABC}) terminal significantly increases the flexibility of the OTA and permits the circuit designer to exercise his creativity in the utilization of this device in many unique applications not possible with the conventional operational amplifier.

Circuit Description

A simplified block diagram of the OTA is shown in Figure 2. Transistors Q_1 and Q_2 comprise the differential input amplifier found in most operational amplifiers, while the lettered-circles (with arrows leading either into or out of the circles) denote "current-mirrors". Figure 3A shows the basic type of current-mirror which is comprised of two transistors, one of which is diode-connected. In a current-mirror with similar geometries for Q_A and Q_B, the current I' establishes a second current I whose value is essentially equal to that of I'.

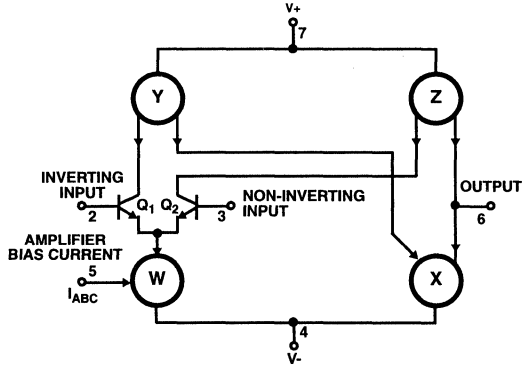


FIGURE 2. SIMPLIFIED DIAGRAM OF THE OTA

This basic current-mirror configuration is sensitive to the transistor beta (β). The addition of another active transistor, shown in Figure 3B, greatly diminishes the circuit sensitivity to transistor beta and increases the current-source output impedance in direct proportion to the transistor beta. Current-mirror W (Figure 2) uses the configuration shown in Figure 3A, while mirrors X, Y, and Z are basically the version shown in Figure 3B. Mirrors Y and Z employ PNP transistors, as depicted by the arrows pointing outward from the mirrors. Appendix 1 describes current-mirrors in more detail.

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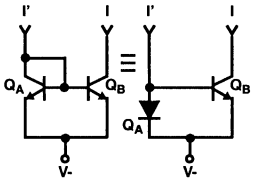


FIGURE 3A. DIODE-CONNECTED TRANSISTOR PAIRED WITH TRANSISTOR

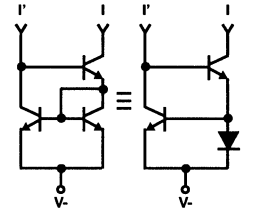


FIGURE 3B. IMPROVED VERSION: EMPLOYS AN EXTRA TRANSISTOR

FIGURE 3. BASIC TYPES OF CURRENT MIRRORS

Figure 4 is the complete schematic diagram of the OTA. The OTA employs only active devices (transistors and diodes). Current applied to the amplifier-bias-current terminal, I_{ABC}, establishes the emitter current of the input differential amplifier Q_1 and Q_2. Hence, effective control of the differential transconductance (g_M) is achieved.

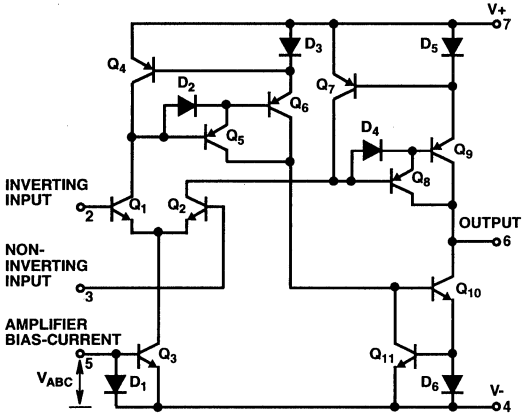


FIGURE 4. SCHEMATIC DIAGRAM OF OTA TYPES CA3080 AND CA3080A

The g_M of a differential amplifier is equal to:

$$\frac{q\alpha I_C}{2KT}$$

(see Reference 2 for derivation) where q is the charge on an electron, α is the ratio of collector current to emitter current of the differential amplifier transistors, (assumed to be 0.99 in this case), I_C is the collector current of the constant-current source (I_{ABC} in this case), K is Boltzman's constant, and T is the ambient temperature in degrees Kelvin. At room temperature, $g_M = 19.2 \times I_{ABC}$, where g_M is in mS and I_{ABC} is in milliamperes. The temperature coefficient of g_M is approximately -0.33%/°C (at room temperature).

Transistor Q_3 and diode D_1 (shown in Figure 4) comprise the current mirror "W" of Figure 2. Similarly, transistors Q_7, Q_8 and Q_9 and diode D_5 of Figure 4 comprise the generic current mirror "Z" of Figure 2. Darlington-connected transistors are employed in mirrors "Y" and "Z" to reduce the voltage sensitivity of the mirror, by the increase of the mirror output impedance. Transistors Q_{10}, Q_{11}, and diode D_6 of Figure 4 comprise the current-mirror "X" of Figure 2. Diodes D_2 and D_4 are connected across the base-emitter junctions of Q_5 and Q_8, respectively, to improve the circuit speed. The amplifier output signal is derived from the collectors of the "Z" and "X" current-mirror of Figure 2, providing a push-pull Class A output stage that produces full differential g_M. This circuit description applies to both the CA3080 and CA3080A. The CA3080A offers tighter control of g_M and input offset voltage, less variation of input offset voltage with variation of I_{ABC} and controlled cut-off leakage current. In the CA3080A, both the output and the input cut-off leakage resistances are greater than 1,000MΩ.

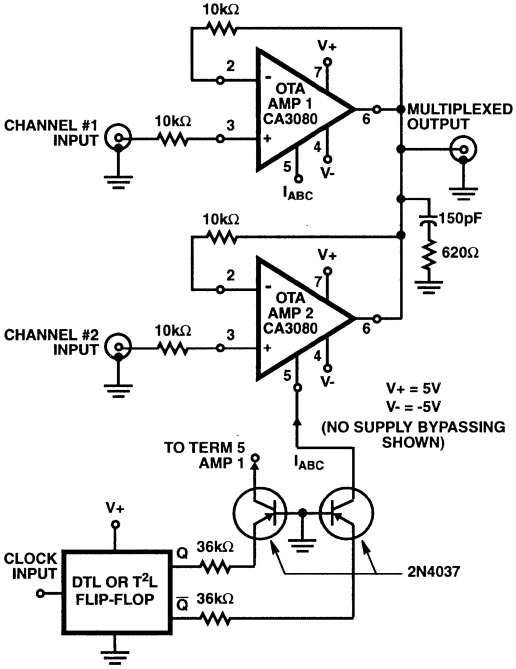


FIGURE 5. SCHEMATIC DIAGRAM OF OTAs IN A TWO-CHANNEL LINEAR TIME-SHARED MULTIPLEXER CIRCUIT

Applications

Multiplexing

The availability of the bias current terminal, I_{ABC}, allows the device to be gated for multiplexer applications. Figure 5 shows a simple two-channel multiplexer system using two CA3080

OTA devices. The maximum level-shift from input to output is low (approximately 2mV for the CA3080A and 5mV for the CA3080). This shift is determined by the amplifier input offset voltage of the particular device used, because the open-loop gain of the system is typically 100dB when the loading on the output of the CA3080A is low. To further increase the gain and reduce the effects of loading, an additional buffer and/or gain-stage may be added. Methods will be shown to successfully perform these functions.

In this example ±5V power-supplies were used, with the IC flip-flop powered by the positive supply. The negative supply-voltage may be increased to -15V, with the positive-supply at 5V to satisfy the logic supply voltage requirements. Outputs from the clocked flip-flop are applied through PNP transistors to gate the CA3080 amplifier-bias-current terminals. The grounded-base configuration is used to minimize capacitive feed-through coupling via the base-collector junction of the PNP transistor.

Another multiplexer system using the OTAs clocked by a CMOS flip-flop is shown in Figure 6. The high output voltage capability of the CMOS flip-flop permits the circuit to be driven directly without the need for PNP level-shifting transistors.

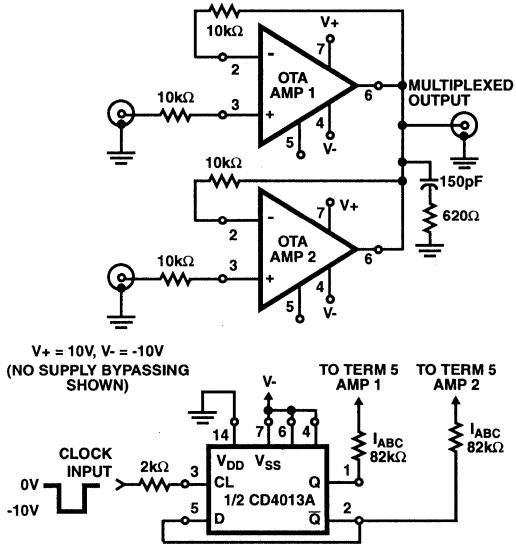
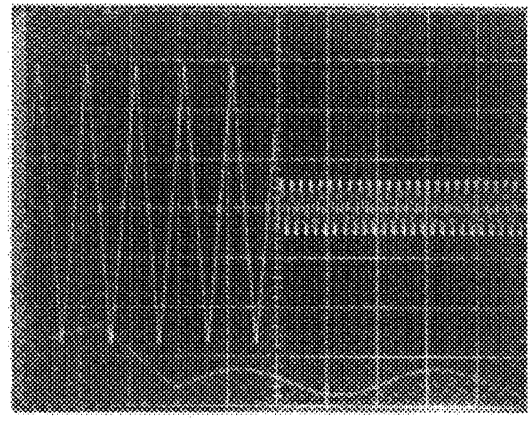


FIGURE 6. SCHEMATIC DIAGRAM OF A TWO-CHANNEL LINEAR MULTIPLEXER SYSTEM USING A CMOS FLIP-FLOP TO GATE TWO OTAs

A simple RC phase-compensation network is used on the output of the OTA in the circuits shown in Figures 5 and 6. The values of the RC-network are chosen so that:

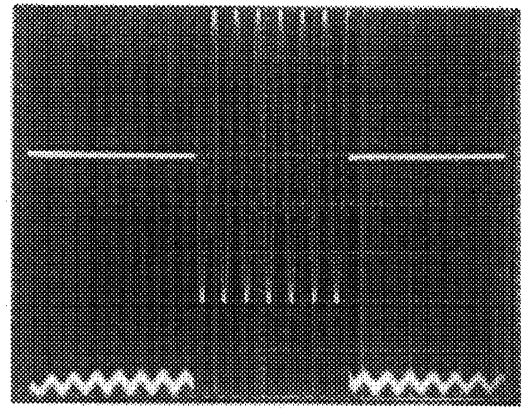
$$\frac{1}{2\pi RC} \cong 2\text{MHz}.$$

This RC network is connected to the point shown because the lowest-frequency pole for the system is usually found at this point. Figure 7 shows an oscilloscope photograph of the multiplexer circuit functioning with two input signals. Figure 8 shows an oscilloscope photograph of the output of the multiplexer with a $6V_{P-P}$, sine wave signal (22kHz) applied to one amplifier and the input to the other amplifier grounded. This photograph demonstrates an isolation of at least 80dB between channels.



Top Trace: Multiplexed Output; 1V/Div., 100µs/Div.
Bottom Trace: Time Expansion of Switching Between Inputs; 2V/Div., 5µs/Div.

FIGURE 7. VOLTAGE WAVEFORMS FOR CIRCUIT OF FIGURE 6



Top Trace: Output; 1V/Div., 100µs/Div.
Bottom Trace: Voltage Expansion of Output; 1mV/Div., 100µs/Div.

FIGURE 8. VOLTAGE WAVEFORMS FOR CIRCUIT OF FIGURE 6

Sample-and-Hold Circuits

An extension of the multiplex system application is a sample-and-hold circuit (Figure 9), using the strobing characteristics of the OTA amplifier bias-current (ABC) terminal as a means of control. Figure 9 shows the basic system using the CA3080A as an OTA in a simple voltage-follower configuration with the phase-compensation capacitor serving the additional function of sampled-signal storage. The major consideration for the use of this method to "hold" charge is that neither the

charging amplifier nor the signal readout device significantly alter the charge stored on the capacitor. The CA3080A is a particularly suitable capacitor-charging amplifier because its output resistance is more than 1000MΩ under cut-off conditions, and the loading on the storage capacitor during the hold-mode is minimized. An effective solution to the read-out requirement involves the use of a 3N138 insulated-gate field-effect transistor (MOSFET) in the feedback loop. This transistor has a maximum gate-leakage current of 10pA; its loading on the charge "holding" capacitor is negligible. The open-loop voltage-gain of the system (Figure 9) is approximately 100dB if the MOSFET is used in the source-follower mode with the CA3080A as the input amplifier. The open-loop output impedance ($1/g_M$) of the 3N138 is approximately 220Ω because its transconductance is about 4,600μS at an operating current of 5mA. When the CA3080A drives the 3N138, the closed loop operational-amplifier output impedance characteristic is:

$$Z_{OUT} \cong \frac{Z_O(\text{OPEN-LOOP})}{A(\text{OPEN-LOOP VOLTAGE-GAIN})}$$

$$\cong \frac{220\Omega}{100\text{dB}} \cong \frac{220\Omega}{10^5} \cong 0.0022\Omega$$

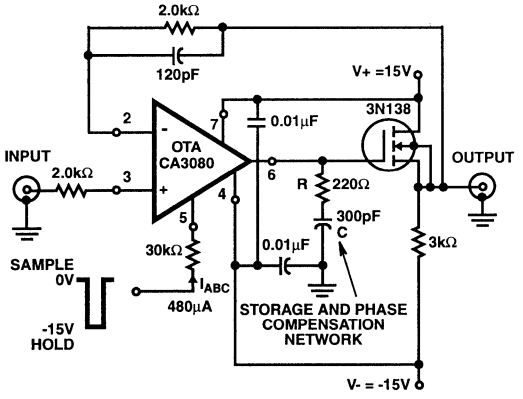
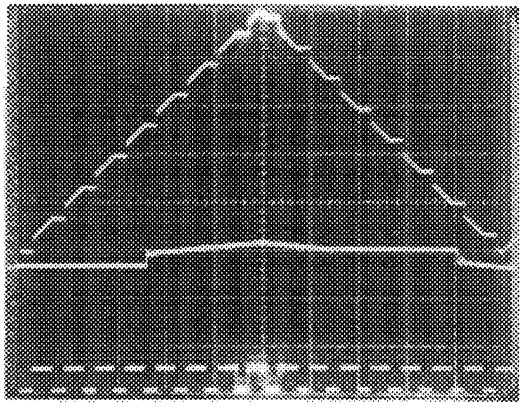


FIGURE 9. SCHEMATIC DIAGRAM OF OTA IN A SAMPLE-AND-HOLD CIRCUIT

Figure 10 shows a "sampled" triangular signal. The lower trace in the photograph is the sampling signal. When this signal goes negative, the CA3080A is cutoff and the signal is "held" on the storage capacitor, as shown by the plateaus on the triangular waveform. The center trace is a time expansion of the top-most transition (in the upper trace) with a time scale of 2μs/Div.

Once the signal is acquired, variation in the stored-signal level during the hold-period is of concern. This variation is primarily a function of the cutoff leakage current of the CA3080A (a maximum limit of 5nA), the leakage of the storage element, and other extraneous paths. These leakage currents may be either "positive" or "negative" and, consequently, the stored-signal may rise or fall during the "hold" interval. The term "tilt" is used to describe this condition. Figure 11 shows the expected pulse "tilt" in microvolts versus time for various values of the compensation/storage capacitor. The horizontal axis shows three scales representing leakage currents of 50nA, 5nA, 500pA.



Top Trace: Sampled Signal 1V/Div., 20μs/Div.
Center Trace: Top Portion of Upper Signal; 1V/Div., 2μs/Div.
Bottom Trace: Sampling Signal; 20V/Div., 20μs/Div.

FIGURE 10. WAVEFORMS FOR CIRCUIT OF FIGURE 9

Figure 12 shows a dual-trace photograph of a triangular signal being "sampled-and-held" for approximately 14ms with a 300pF storage capacitor. The center trace (expanded to 20mV/Div.) shows the worst-case "tilt" for all the steps shown in the upper trace. The total equivalent leakage current in this case is only 170pA (I = C dv/dt).

Figure 13 is an oscilloscope photograph of a ramp voltage being sampled by the "sample-and-hold" circuit of Figure 9. The input signal and sampled-output signal are superimposed. The lower trace shows the sampling signal. Data shown in Figure 13 were recorded with supply voltages of ±10V and the series input resistor at terminal 5 was 22kΩ.

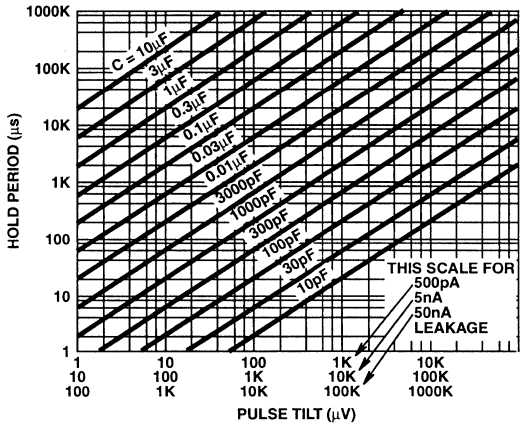
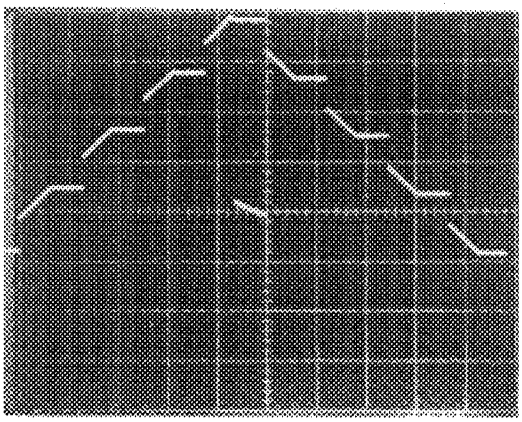
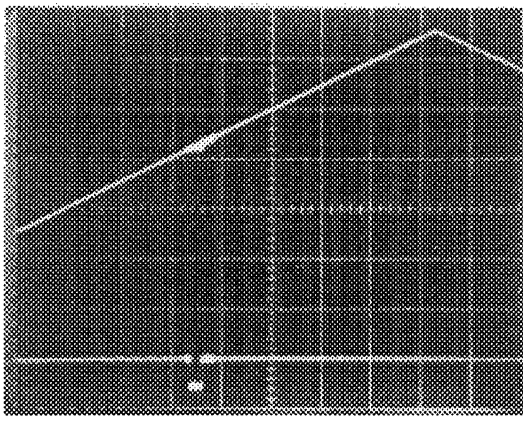


FIGURE 11. "TILT" IN "HELD" VOLTAGE vs HOLD TIME



Top Trace: Sampled Signal; 1V/Div., 20ms/Div.
Center Trace: Worse Case Tilt; 20mV/Div., 20ms/Div.

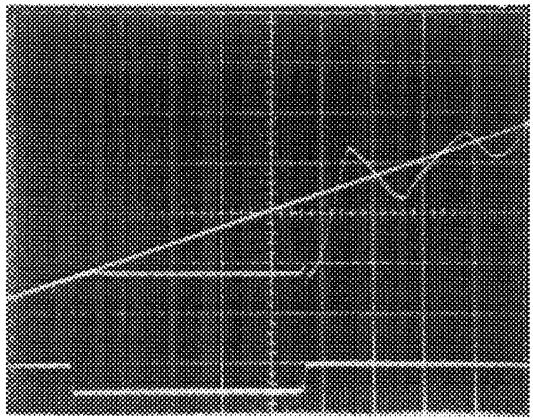
FIGURE 12. "TRIANGULAR-VOLTAGE" BEING SAMPLED BY CIRCUIT OF FIGURE 9



Top Trace: Input and Output Superimposed; 1V/Div., 2μs/Div.
Bottom Trace: Sampling Signal; 20V/Div., 2μs/Div.

FIGURE 13. "RAMP-VOLTAGE" BEING SAMPLED BY CIRCUIT OF FIGURE 9

In Figure 14, the trace of Figure 13 has been expanded (100mV/Div. and 100ns/Div.) to show the response of the sample-and-hold circuit with respect to the sampling signal. After the sampling interval, the amplifier overshoots the signal level and settles (within the amplifier offset voltage) in approximately 1μs. The resistor in series with the 300pF phase-compensation capacitor was adjusted to 68Ω for minimum recovery time.



Top Trace: Input and Sampled Output Superimposed; 100mV/Div., 100ns/Div.
Bottom Trace: Sampling Signal; 20V/Div., 100ns/Div.

FIGURE 14. "TRIANGULAR-VOLTAGE" BEING SAMPLED BY CIRCUIT OF FIGURE 9

Figure 15 shows the basic circuit of Figure 9 implemented with a 2N4037 PNP transistor to minimize capacitive feedthrough. Figure 16 shows oscilloscope photographs taken with the circuit of Figure 15 operating in the sampling mode at supply voltage of ±15V. The 9.1kΩ resistor in series with the PNP transistor emitter establishes amplifier-bias-current (I_{ABC}) conditions similar to those used in the circuit of Figure 9.

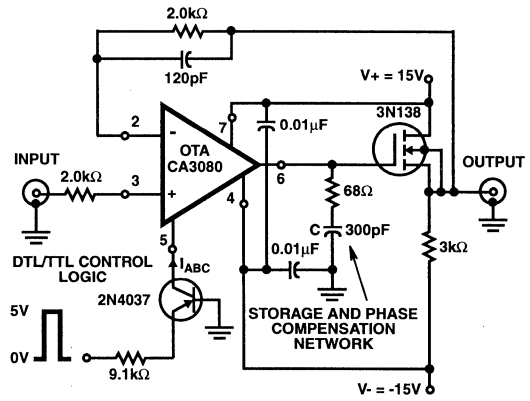
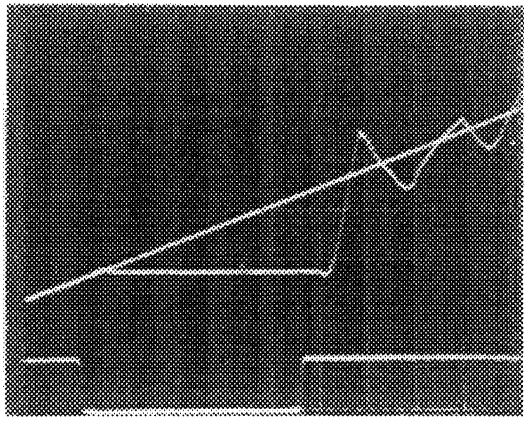


FIGURE 15. SCHEMATIC DIAGRAM OF THE OTA IN A SAMPLE-AND-HOLD CONFIGURATION (DTL/TTL CONTROL LOGIC)



Top Trace: Input and Sampled Output Superimposed; 100mV/Div., 100ns/Div.
Bottom Trace: Sampling Signal; 5V/Div., 100ns/Div.

FIGURE 16. CIRCUIT OF FIGURE 15 OPERATING IN SAMPLING MODE

Considerations of circuit stability and signal retention require the use of the largest possible phase-compensation capacitor, compatible with the required slew rate. In most systems the capacitor is chosen for the maximum allowable "tilt" in the storage mode and the resistor is chosen so that $1/2\pi RC \cong 2MHz$, corresponding to the first pole in the amplifier at an output current level of 500µA. It is frequently desirable to optimize the system response by the placement of a small variable resistor in series with the capacitor, as is shown in Figures 9 and 15. The 120pF capacitor shunting the 2kΩ resistor improves the amplifier transient response.

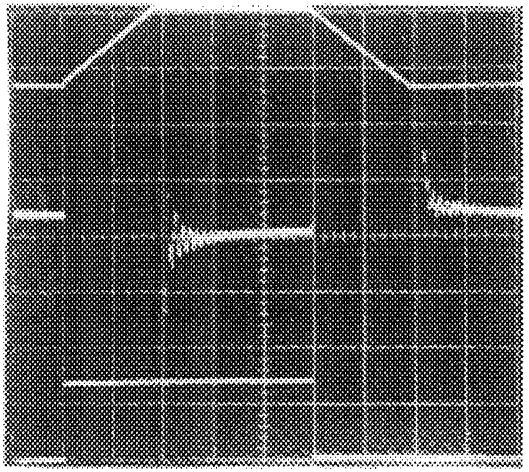
Figure 17 shows a multi-trace oscilloscope photograph of input and output signals for the circuit of Figure 9, operating in the linear mode. The lower portion of the photograph shows the input signal, and the upper portion shows the output signal. The amplifier slew-rate is determined by the output current and the capacitive loading: in this case the slew rate (dv/dt) = 1.8V/µs.

The center trace in Figure 17 shows the difference between the input and output signals as displayed on a Tektronix 7A13 differential amplifier at 2mV/Div. The output of the amplifier system settles to within 2mV (the offset voltage specification for the CA3080A) of the input level in 1µs after slewing.

Figure 18 is a curve of slew-rate versus amplifier-bias-current (I_{ABC}) for various storage/compensation capacitors. The magnitude of the current being supplied to the storage/compensation capacitor is equal to the amplifier-bias-current (I_{ABC}) when the OTA is supplying its maximum output current.

Gain Control - Amplitude Modulation

Effective gain control of a signal may be obtained by controlled variation of the amplifier-bias-current (I_{ABC}) in the OTA because its g_M is directly proportional to the amplifier-bias-current (I_{ABC}). For a specified value of amplifier-bias-current, the output current (I_O) is equal to the product of g_M and the input signal magnitude. The output voltage swing is the product of output current (I_O) and the load resistance (R_L).



Top Trace: Output; 5V/Div., 2µs/Div.
Center Trace: Differential Comparsion of Input and Output; 2mV/Div., 0V thru Center; 2µs/Div.
Bottom Trace: Input; 5V/Div., 2µs/Div.

FIGURE 17. CIRCUIT OF FIGURE 9 OPERATING IN THE LINEAR SAMPLE MODE

Figure 19 shows the configuration for this form of basic gain control (a modulation system). The output signal current (I_O) is equal to $-g_M \times V_X$; the sign of the output signal is negative because the input signal is applied to the inverting input terminal of the OTA. The transconductance of the OTA is controlled by adjustment of the amplifier bias current, I_{ABC}. In this circuit the level of the unmodulated carrier output is established by a particular amplifier-bias-current (I_{ABC}) through resistor R_M. Amplitude modulation of the carrier frequency occurs because variation of the voltage V_M forces a change in the amplifier-bias-current (I_{ABC}) supplied via resistor R_M. When V_M goes positive, the bias current increases which causes a corresponding increase in the g_M of the OTA. When the V_M goes in the negative direction (toward the amplifier-bias-current terminal potential), the amplifier-bias-current decreases, and reduces the g_M of the OTA.

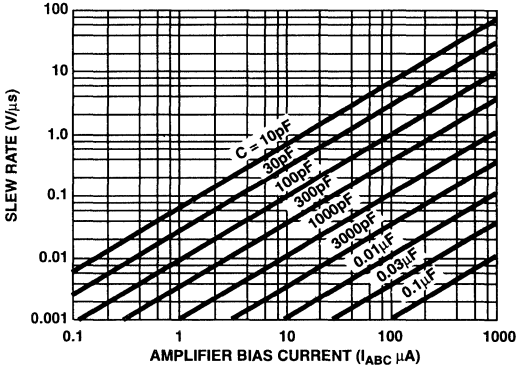


FIGURE 18. SLEW RATE vs AMPLIFIER-BIAS-CURRENT (I_{ABC})

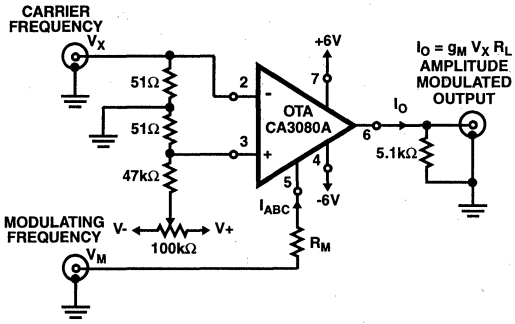


FIGURE 19. AMPLITUDE MODULATOR CIRCUIT USING THE OTA

As discussed earlier, g_M = 19.2 x I_{ABC}, where g_M is in millisiemens when I_{ABC} is in milliamperes. In this case, I_{ABC} is approximately equal to:

$$\frac{V_M - (V-)}{R_M} = I_{ABC}$$

$$I_O = -g_M V_X$$

$$g_M V_X = (19.2)(I_{ABC})(V_X)$$

$$I_O = \frac{-19.2[V_M - (V-)]V_X}{R_M}$$

$$I_O = \frac{19.2(V_X)(V-)}{R_M} - \frac{19.2(V_X)(V_M)}{R_M}$$

There are two terms in the modulation equation: the first term represents the fixed carrier input, independent of V_M and the second term represents the modulation, which either adds to or subtracts from the first term. When V_M is equal to the V- term, the output is reduced to zero.

In the preceding modulation equations the term,

$$(19.2)(V_X)\frac{V_{ABC}}{R_M}$$

involving the amplifier-bias-current terminal voltage (V_{ABC}) (see Figure 4 for V_{ABC}) was neglected. This term was assumed to be small because V_{ABC} is small compared with V- in the equation. If the amplifier-bias-current terminal is driven by a current-source (such as from the collector of a PNP transistor), the effect of V_{ABC} variation is eliminated and transferred to the involvement of the PNP transistor base-emitter junction characteristics. Figure 20 shows a method of driving the amplifier-bias-current terminal to effectively remove this latter variation.

If an NPN transistor is added to the circuit of Figure 20 as an emitter-follower to drive the PNP transistor, variations due to base-emitter characteristics are considerably reduced due to the complementary nature of the NPN base-emitter junctions. Moreover, the temperature coefficients of the two base-emitter junctions tend to cancel one another. Figure 21 shows a configuration using one transistor in the CA3018A NPN transistor-array as an input emitter-follower, with the three remaining transistors of the transistor-array connected as a current-source for the emitter followers.

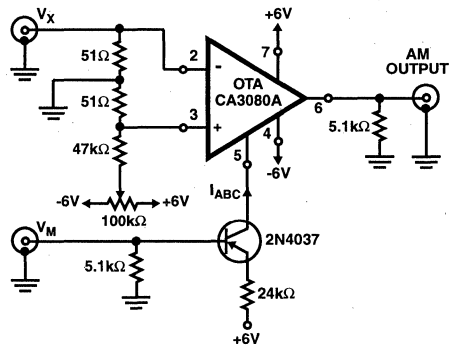


FIGURE 20. AMPLITUDE MODULATOR USING OTA CONTROLLED BY PNP TRANSISTOR

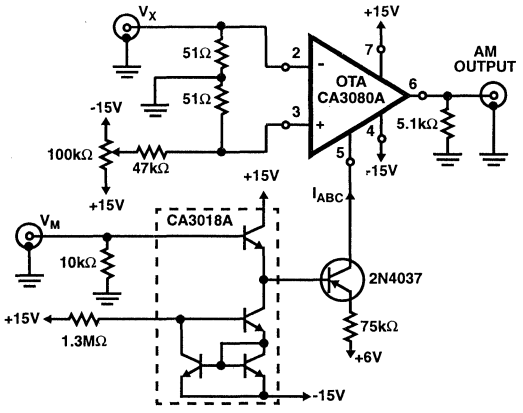


FIGURE 21. AMPLITUDE MODULATOR USING OTA CONTROLLED BY PNP AND NPN TRANSISTORS

The 100kΩ potentiometer shown in these schematics is used to null the effects of amplifier input offset voltage. This potentiometer is adjusted to set the output voltage symmetrically about zero. Figures 22A and 22B show oscilloscope photographs of the output voltages obtained when the circuit of Figure 19 is used as a modulator for both sinusoidal and triangular modulating signals. This method of modulation permits a range exceeding 1000:1 in the gain, and thus provides modulation of the carrier input in excess of 99%. The photo in Figure 22C shows the excellent isolation (>80dB at f = 100kHz) achieved in this modulator during the "gated-off" condition.

Four-Quadrant Multipliers

A single CA3080A is especially suited for many low-frequency, low-power four-quadrant multiplier applications. The basic multiplier circuit of Figure 23 is particularly useful for waveform generation, doubly balanced modulation, and other signal processing applications, in portable equipment, where low-power consumption is essential and accuracy

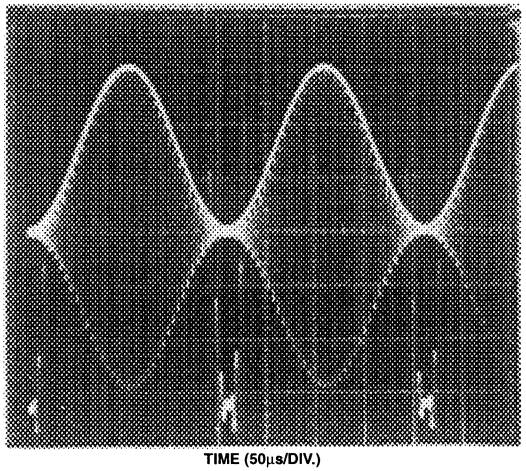
requirements are moderate. The multiplier configuration is basically an extension of the previously discussed gain-controlled configuration (Figure 19).

To obtain a four-quadrant multiplier, the first term of the modulation equation (which represents the fixed carrier) must be reduced to zero. This term is reduced to zero by the placement of a feedback resistor (R) between the output and the inverting input terminal of the CA3080A, with the value of the feedback resistor (R) equal to $1/g_M$. The output current is $I_O = g_M (-V_X)$ because the input is applied to the inverting terminal of the OTA. The output current due to the resistor (R) is V_X/R. Hence, the two signals cancel when $R = 1/g_M$. The current for this configuration is:

$$I_O = \frac{-19.2\ V_X V_M}{R_M}, \text{ and } V_M = V_Y$$

The output signal for these configurations is a current which is best terminated by a short-circuit. This condition can be satisfied by making the load resistance for the multiplier output very small. Alternatively, the output can be applied to a current-to-voltage converter as shown in Figure 24.

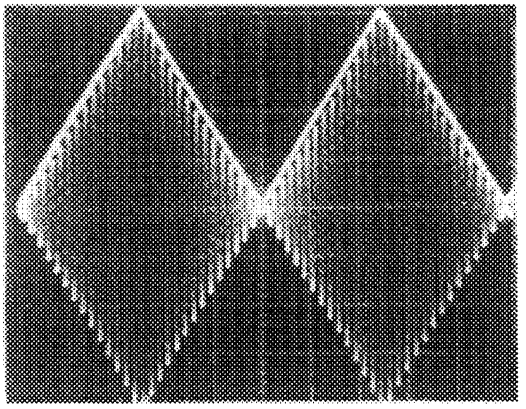
In Figure 23, the current "cancellation" in the resistor R is a direct function of the OTA differential amplifier linearity. In the following example, the signal excursion is limited to ±10mV to preserve this linearity. Greater signal-excursions on the input terminal will result in a significant departure from linear operation (which may be entirely satisfactory in many applications).



TIME (50µs/DIV.)

Top Trace: Modulation Input (≅ $20V_{P-P}$)
Center Trace: Amplitude Modulated Output; 500mV/Div.
Bottom Trace: Expanded Output to Show Depth of Modulation; 20mV/Div.

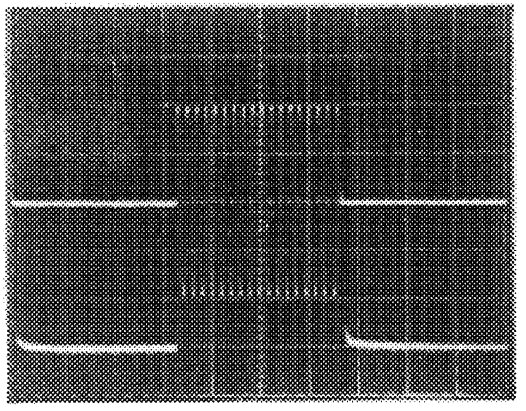
FIGURE 22A. RESPONSE FOR SINE WAVE MODULATION



TIME (50µs/DIV.)

Top Trace: Modulation Input (20V)
Bottom Trace: Amplitude Modulated Output; 500mV/Div.

FIGURE 22B. RESPONSE FOR TRIANGLE WAVE MODULATION



TIME (50µs/DIV.)

Top Trace: Gated Output; 1V/Div.
Bottom Trace: Voltage Expansion Of Above Signal Showing No Residual; 1mv/Div.

FIGURE 22C. RESPONSE FOR SQUARE WAVE MODULATION

FIGURE 22. AMPLITUDE MODULATOR CIRCUIT OF FIGURE 19 WITH $R_M = 40k\Omega$, $V_S = \pm 10V$

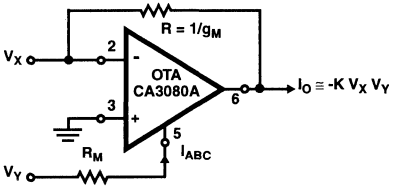


FIGURE 23. BASIC FOUR QUADRANT ANALOG MULTIPLIER USING AN OTA

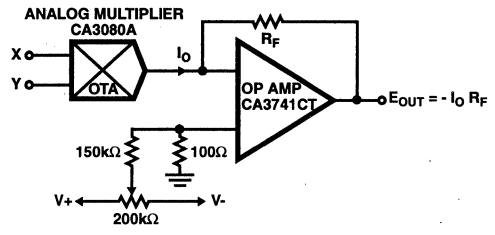


FIGURE 24. OTA ANALOG MULTIPLIER DRIVING A CURRENT-TO-VOLTAGE CONVERTER

Figure 25 shows a schematic diagram of the basic multiplier with the adjustments set-up to give the multiplier an accuracy of approximately ±7 percent full-scale. There are only three adjustments: 1) one is on the output, to compensate for slight variations in the current-transfer ratio of the current-mirrors (which would otherwise result in a symmetrical output about some current level other than zero); 2) the adjustment of the 20kΩ potentiometer establishes the g_M of the system equal to the value of the fixed resistor shunting the system when the Y-input is zero; 3) compensates for error due to input offset voltage.

Procedure for adjustment of the circuit:

1. a) Set the 1MΩ output-current balancing potentiometer to the center of its range
   b) Ground the X- and Y- inputs
   c) Adjust the 100kΩ potentiometer until a 0V reading is obtained at the output.
2. a) Ground the Y-input and apply a signal to the X-input through a low source-impedance generator (it is essential that a low impedance source be used; this minimizes any change in the g_M balance or zero-point due to the 50μA Y-input bias current).
   b) Adjust the 20kΩ potentiometer in series with Y-input until a reading of 0V is obtained at the output. This adjustment establishes the g_M of the CA3080A at the proper level to cancel the output signal. The output current is diverted through the 510kΩ resistor.
3. a) Ground the X-input and apply a signal to the Y-input through a low source-impedance generator.
   b) Adjust the 1MΩ resistor for an output voltage of 0V.

There will be some interaction among the adjustments and the procedure should be repeated to optimize the circuit performance.

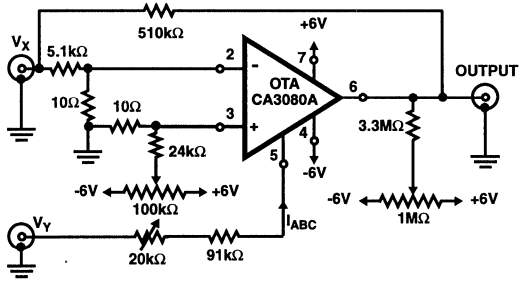


FIGURE 25. SCHEMATIC DIAGRAM OF ANALOG MULTIPLIER USING OTA

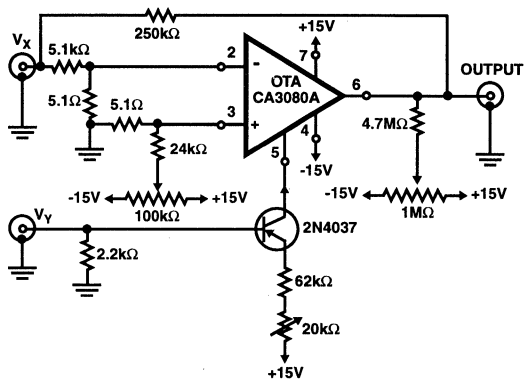
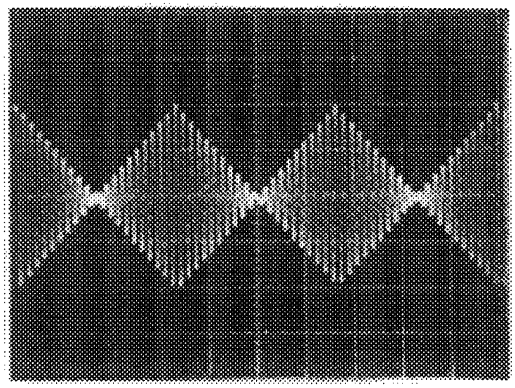


FIGURE 26. SCHEMATIC DIAGRAM OF ANALOG MULTIPLIER USING OTA CONTROLLED BY A PNP TRANSISTOR

Figure 26 shows the schematic of an analog multiplier circuit with a 2N4037 PNP transistor replacing the Y-input "current" resistor. The advantage of this system is the higher input resistance resulting from the current-gain of the PNP transistor. The addition of another emitter-follower preceeding the PNP transistor (shown in Figure 21) will further increase the current gain while markedly reducing the effect of the V_{be} temperature-dependent characteristic and the offset voltage of the two base-emitter junctions.

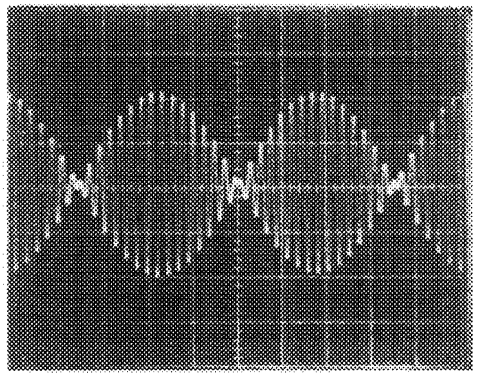
Figures 27A and 27B show oscilloscope photographs of the output signals delivered by the circuit of Figure 26 which is connected as a suppressed-carrier generator. Figures 28A and 28B contain photos of the outputs obtained in signal "squaring" circuits, i.e. "squaring" sine-wave and triangular- wave inputs.

If ±15V power supplies are used (shown in Figure 26), both inputs can accept ±10V input signals. Adjustment of this multiplier circuit is similar to that already described above.



500mV/Div., 200μs/Div.,
Triangular Input: 700Hz; $5V_{P-P}$ to V_Y Input
Carrier Input: 30kHz; $13.5V_{P-P}$ to V_X Input

FIGURE 27A.



500mV/Div., 200µs/Div.,
Modulating Frequency: 700Hz; $5V_{P-P}$ to V_Y Input
Carrier Input: 21kHz; $13.5V_{P-P}$ to V_X Input

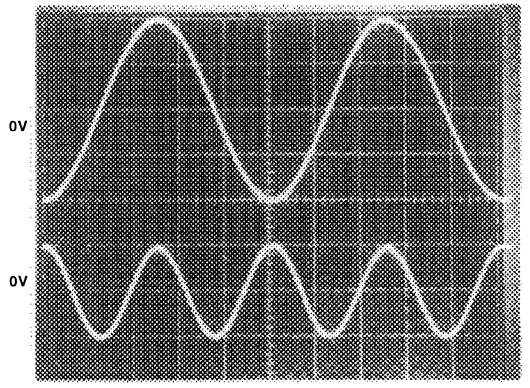
FIGURE 27B.

FIGURE 27. WAVEFORMS OBSERVED WITH OTA ANALOG MULTIPLIER USED AS A SUPPRESSED CARRIER GENERATOR

The accuracy and stability of these multipliers are a direct function of the power supply-voltage stability because the Y-input is referred to the negative supply-voltage. Tracking of the positive and negative supply is also important because the balance adjustments for both the offset voltage and output current are also referenced to these supplies.

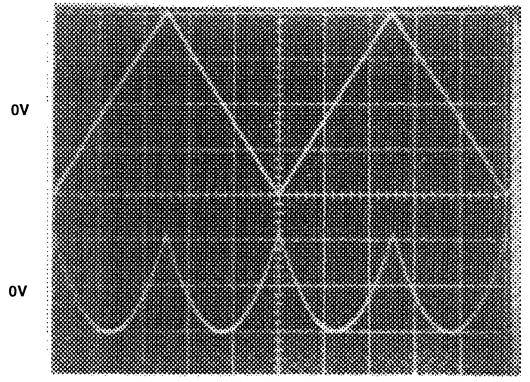
Linear Multiplexer - Decoder

A simple, but effective system for multiplexing and decoding can be assembled with the CA3080 shown in Figure 29. Only two channels are shown in this schematic, but the number of channels may be extended as desired. Figure 30 shows oscilloscope photos taken during operation of the multiplexer and decoder. A CA3080 is used as a 10µs delay-"one-shot" multivibrator in the decoder to insure that the sample-and-hold circuit can sample only after the input signal has settled. Thus, the trailing edge of the "one-shot" output-signal is used to sample the input at the sample-and-hold circuit for approximately 1µs. Figure 31 shows oscilloscope photos of various waveforms observed during operation of the multiplexer/decoder circuit. Either the Q or $\overline{Q}$ output from the flip-flop may be used to trigger the 10µs "one-shot" to decode a signal.



Top Trace: Input to X And Y; 2V/Div., 1ms/Div. (200Hz)
Bottom Trace: Output; 500mV/Div., 1ms/Div. (400Hz)

FIGURE 28A.



Top Trace: Input to X And Y; 2V/Div., 1ms/Div. (200Hz)
Bottom Trace: Output; 500mV/Div., 1ms/Div. (400Hz)

FIGURE 28B.

FIGURE 28. WAVEFORMS OBSERVED WITH OTA ANALOG MULTIPLIER USED IN SIGNAL-SQUARING CIRCUITS

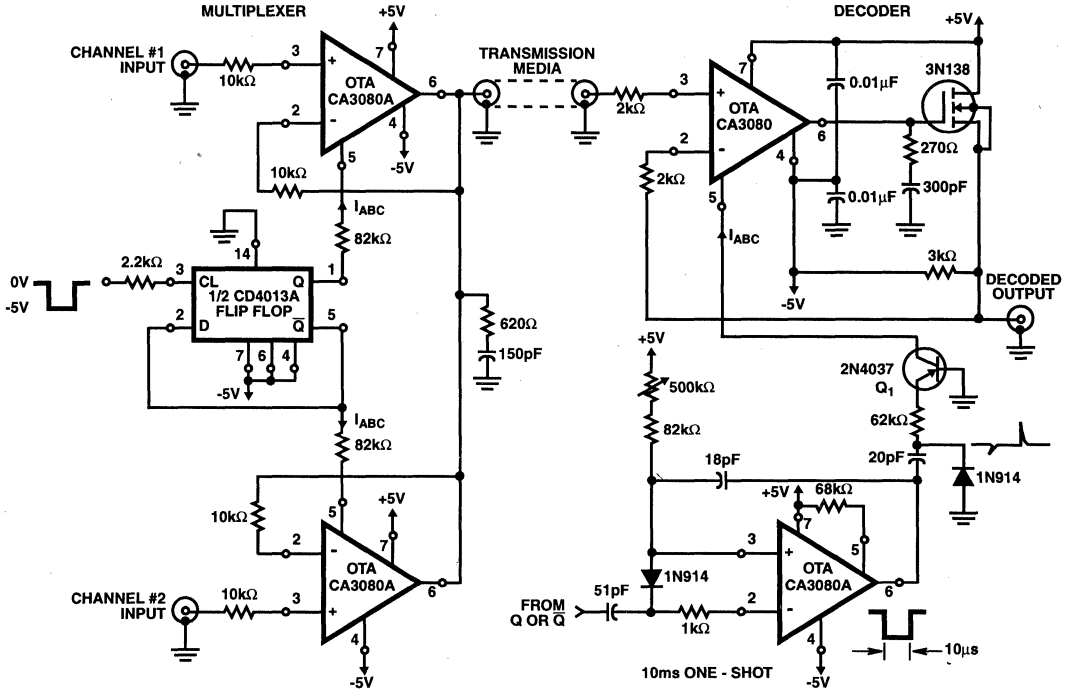
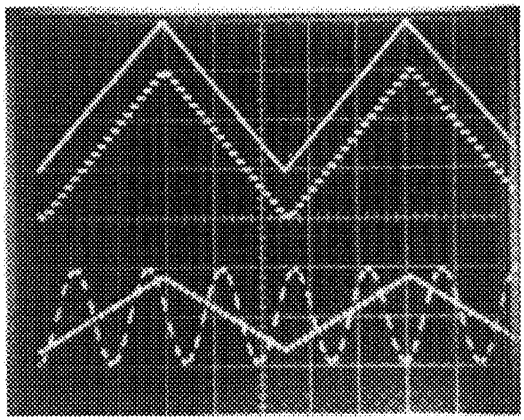
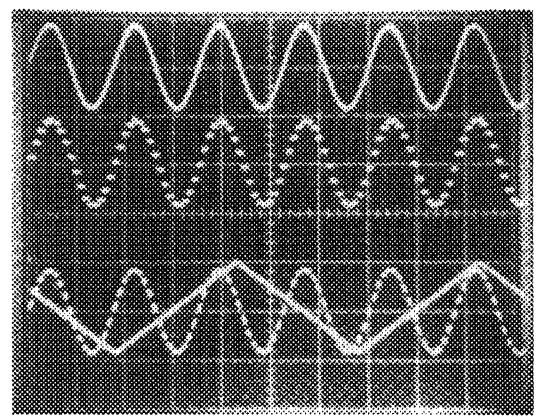


FIGURE 29. TWO-CHANNEL MULTIPLEXER AND DECODER USING OTAs

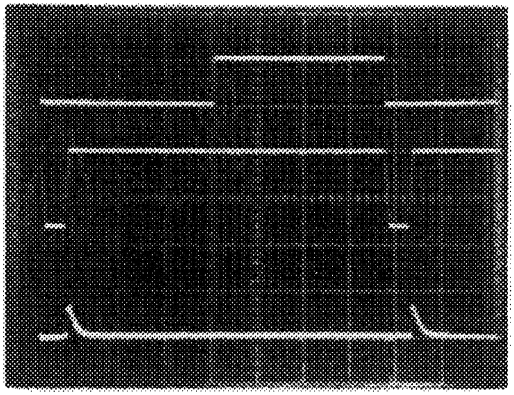


Top Trace: Input Signal; 1V/Div., 20ms/Div.
Center Trace: Recovered Output; 1V/Div., 20ms/Div.
Bottom Trace: Multiplexed Signals; 2V/Div., 20ms/Div.



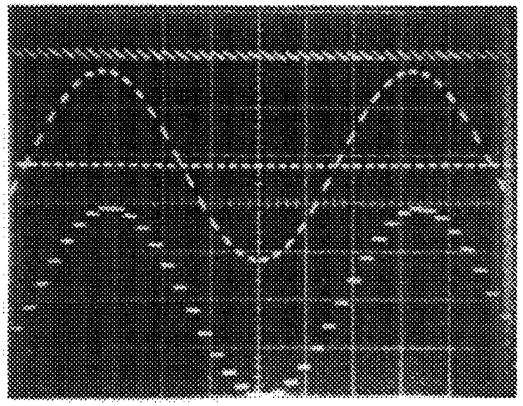
Top Trace: Input Signal; 1V/Div., 20ms/Div.
Center Trace: Recovered Output; 1V/Div., 20ms/Div.
Bottom Trace: Multiplexed Signals; 1V/Div., 20ms/Div.

FIGURE 30. WAVEFORMS SHOWING OPERATION OF LINEAR MULTIPLEXER/SAMPLE-AND-HOLD DECODE CIRCUITRY (FIGURE 29)



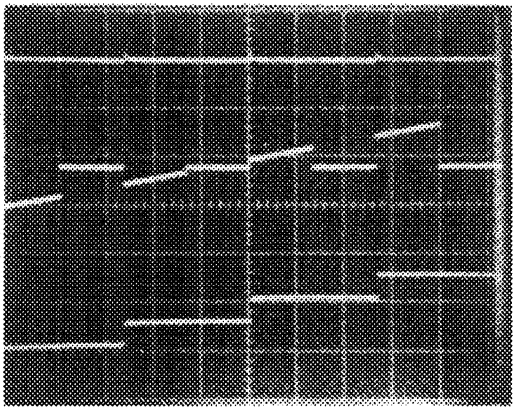
Top Trace: Flip-flop Output; 5V/Div., 20μs/Div.
Center Trace: "One-shot" Output; 5V/Div., 20μs/Div.
Bottom Trace: Strobe Pulse At The Collector of Q_1; 0.1V/Div., 20μs/Div.

FIGURE 31A. WAVEFORMS CONTROLLING DECODER ENABLE



Top Trace: Strobe Pulse at Q_1; 0.5V/Div., 5ms/Div.
Center Trace: Multiplexed Output With One Input at GND; 0.5V/Div., 5ms/Div.
Bottom Trace: Decoded Output; 0.5V/Div., 5ms/Div.

FIGURE 31B. WAVEFORMS SHOWING DECODER OPERATION



500μs/Div.

FIGURE 31C. SAME AS FIGURE 31B BUT WITH EXPANDED TIME SCALE

FIGURE 31. VARIOUS WAVEFORMS SHOWING THE OPERATION OF LINEAR MULTIPLEXER

High-Gain, High-Current Output Stages

In the previously discussed examples, the OTA has been buffered by a single insulated-gate field-effect-transistor (MOSFET) shown in Figure 9. This configuration yields a voltage gain equal to the (g_M) (R_O) product of the CA3080, which is typically 142,000 (103dB). The output voltage and current-swing of the operational amplifier formed by this configuration (Figure 9) are limited by the 3N138 MOSFET performance and its source-terminal load. In the positive direction, the MOSFET may be driven into saturation; the source-load resistance and the MOSFET characteristics become the factors limiting the output-voltage swing in the negative direction. The available negative-going load current may be kept constant by the return of the source-terminal to a constant-current transistor. Phase compensation is applied at the interface of the CA3080 and the 3N138 MOSFET shown in Figure 9.

Another variation of this generic form of amplifier utilizes the CD4007A (CMOS) inverter as an amplifier driven by the CA3080. Each of the three inverter/amplifiers in the CD4007A has a typical voltage gain of 30dB. The gain of a single CMOS inverter/amplifier coupled with the 100dB gain of the CA3080 yields a total forward-gain of about 130dB. Use of a two-stage CMOS amplifier configuration will increase the total open-loop gain of the system to about 160dB (100,000,000). Figures 32 through 35 show examples of these configurations. Each CMOS inverter/amplifier can sink or source a current of 6mA (Typ). In Figures 34 and 35, two CMOS inverter/amplifiers have been connected in parallel to provide additional output current.

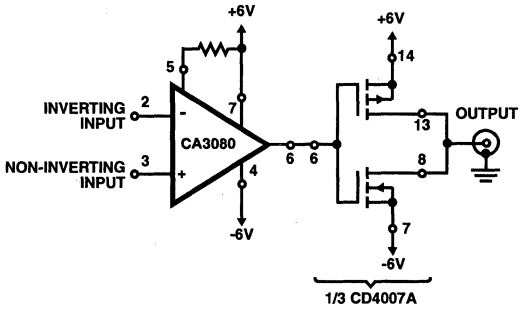


FIGURE 32. OTA DRIVING CMOS INVERTER/AMPLIFIER IN OPEN-LOOP MODE

The open-loop slew-rate of the circuit in Figure 32 is approximately 65V/μs. When compensated for the unity-gain voltage-follower mode, the slew-rate is about 1V/μs (shown in Figure 33). Even when the three inverter/amplifiers in the CD4007A are connected as shown in Figure 34, the open-loop slew-rate remains at 65V/μs. A slew-rate of about 1V/μs is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Figure 35. Figure 36 contains oscilloscope photos of input-output waveforms under small-signal and large-signal conditions for the circuits of Figures 33 and 35. These photos illustrate the inherent stability of the OTA and CMOS circuits operating in concert.

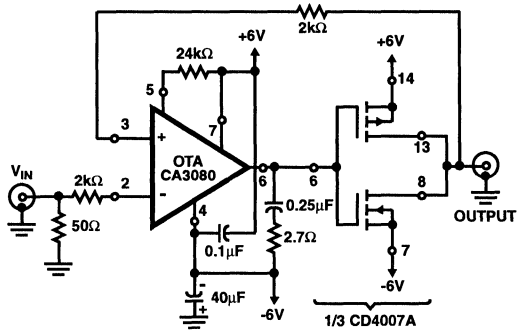


FIGURE 33. OTA DRIVING CMOS INVERTER/AMPLIFIER IN UNITY-GAIN CLOSED-LOOP MODE

Precision Multistable Circuits

The micropower capabilities of the CA3080, when combined with the characteristics of the CD4007A CMOS inverter/amplifiers, are ideally suited for use in connection with precision multistable circuits. In the circuits of Figures 32, 33, 34, and 35, for example, power-supply current drawn by the CMOS inverter/amplifier approaches zero as the output voltage swings either positive or negative, while the CA3080 current-drain remains constant.

Figure 37 shows a variety of circuits that can be assembled using the CA3080 to drive one inverter/amplifier in the CD4007A. For greater output current capability, the remaining amplifiers in the CD4007A may be connected in parallel with the single stage shown. Precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080. Moreover, speed vs power consumption trade-offs may be made by adjustment of the I_{ABC} current to the CA3080. The quiescent power consumption of the circuits shown in Figure 37 is typically 6mW, but can be made to operate in the micropower region by suitable circuit modifications.

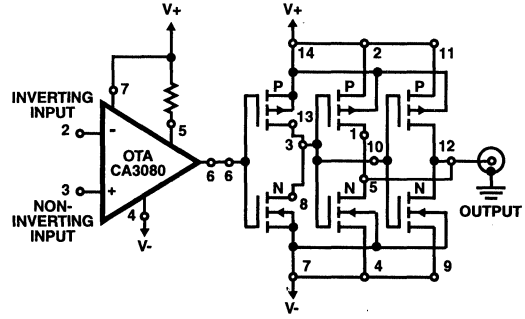


FIGURE 34. OTA DRIVING TWO-STAGE CMOS INVERTER/AMPLIFIER IN OPEN-LOOP MODE

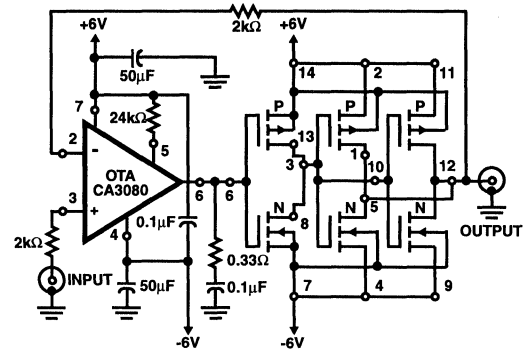
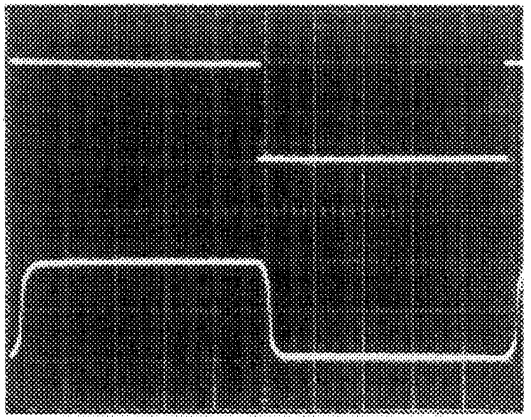
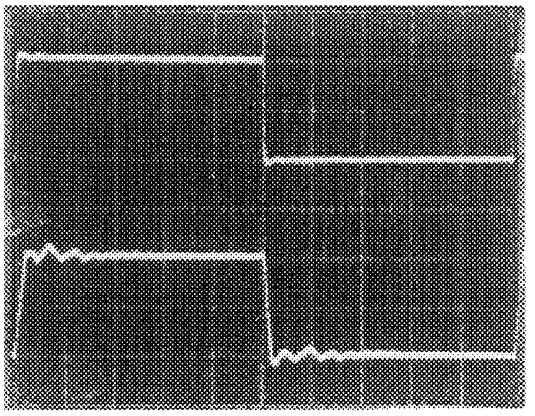


FIGURE 35. OTA DRIVING TWO-STAGE CMOS INVERTER/AMPLIFIER IN UNITY GAIN CLOSED-LOOP MODE



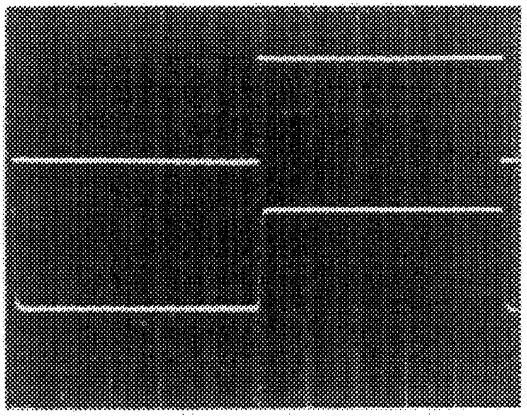
Top Trace: Input; 5V/Div., 100µs/Div.
Bottom Trace: Output; 5V/Div., 100µs/Div.

FIGURE 36A. LARGE SIGNAL RESPONSE FOR CIRCUIT IN FIGURE 33



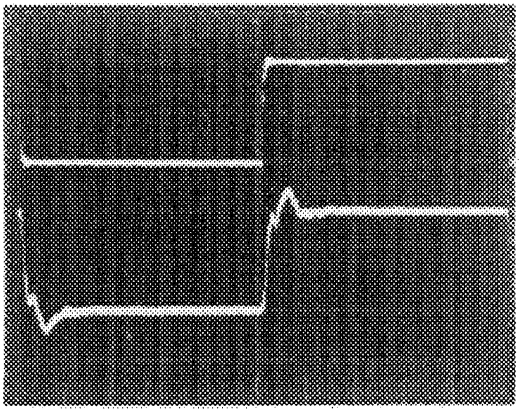
Top Trace: Input; 50mV/Div., 1µs/Div.
Bottom Trace: Output; 50mV/Div., 1µs/Div.

FIGURE 36B. SMALL SIGNAL RESPONSE FOR CIRCUIT IN FIGURE 33



Top Trace: Input; 5V/Div., 100µs/Div.
Bottom Trace: Output; 5V/Div., 100µs/Div.

FIGURE 36C. LARGE SIGNAL RESPONSE FOR CIRCUIT IN FIGURE 35



Top Trace: Input; 50mV/Div., 1µs/Div.
Bottom Trace: Output; 50mV/Div., 1µs/Div.

FIGURE 36D. SMALL SIGNAL RESPONSE FOR CIRCUIT IN FIGURE 35

FIGURE 36. PERFORMANCE OF OTA DRIVING CMOS INVERTER/AMPLIFIER

Micropower Comparator

The schematic diagram of a micropower comparator is shown in Figure 38. Quiescent power consumption of this circuit is about 10µW (Typ). When the comparator is strobed "ON", the CA3080A becomes active and consumes 420µW. Under these conditions, the circuit responds to a differential input signal in about 8µs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150ns, but the power consumption rises to 21mW.

The differential amplifier input common-mode range for the circuit of Figure 38 is -1V to +10.5V. Voltage gain of the micropower comparator is typically 130dB. For example, a 5µV input signal will switch the output.

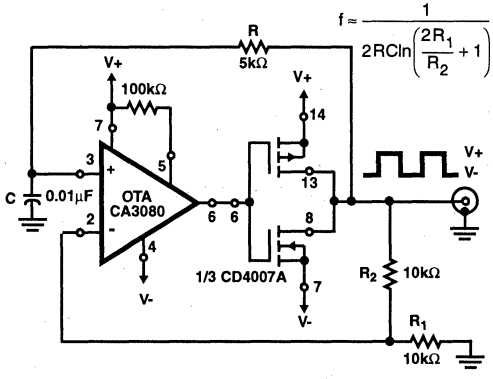


FIGURE 37A. ASTABLE MULTIVIBRATOR

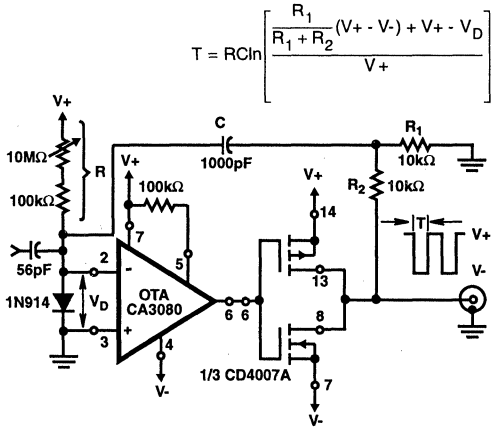


FIGURE 37B. MONOSTABLE MULTIVIBRATOR

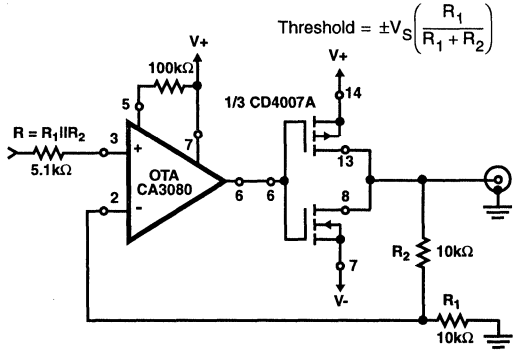


FIGURE 37C. THRESHOLD DETECTOR

FIGURE 37. MULTISTABLE CIRCUITS USING THE OTA AND CMOS INVERTER/AMPLIFIERS

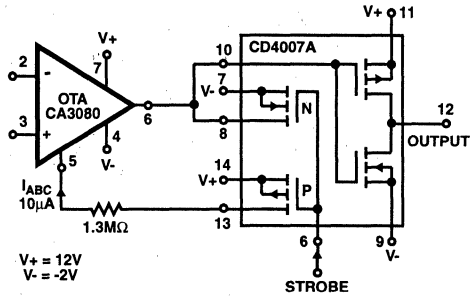


FIGURE 38. SCHEMATIC DIAGRAM OF MICROPOWER COMPARATOR USING THE CA3080A AND CMOS CD4007A

Appendix I

Current Mirrors

The basic current-mirror, described in the beginning of this note, in its rudimentary form, is a transistor with a second transistor connected as a diode. Figure A shows this basic configuration of the current-mirror. Q_2 is a diode connected transistor. Because this diode-connected transistor is not in saturation and is "active", the "diode" formed by this connection may be considered as a transistor with 100% feedback. Therefore, the base current still controls the collector current as is the case in normal transistor action, i.e., $I_C = \beta I_B$. If a current I_1 is forced into the diode-connected transistor, the base-to-emitter voltage will rise until equilibrium is reached and the total current being supplied is divided between the collector and base regions. Thus, a base-to-emitter voltage is established in Q_2 such that Q_2 "sinks" the applied current I_1.

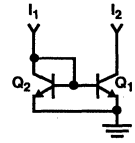


FIGURE 39A. DIODE - TRANSISTOR CURRENT SOURCE

If the base of a second transistor (Q_1) is connected to the base-to-collector junction of Q_2, shown in Figure 39A, Q_1 will also be able to "sink" a current approximately equal to that flowing in the collector lead of the diode-connected transistor Q_2. This assumes that both transistors have identical characteristics, a prerequisite established by the IC fabrication technique. The difference in current between the input current (I_1) and the collector current (I_2) of transistor Q_1, is due to the fact that the base-current for both transistors is supplied from I_1. Figure 39B shows this current division, using a "unit" of base current (1) to each transistor base. This base current causes a collector current to flow in direct proportion to the β of each transistor. The ratio of the "sinking" current I_2 to the input current I_1 is therefore:

$$\frac{I_2}{I_1} = \beta/(\beta + 2).$$

Thus, as β increases, the output current (I_2) approaches the input current (I_1). The curves in Figure 39C show this ratio as a function of the transistor β. When the transistor β is equal to 100, for example, the difference between the two currents is only two percent.

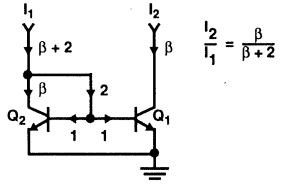


FIGURE 39B. DIODE - TRANSISTOR CURRENT SOURCE. ANALYSIS OF CURRENT FLOW

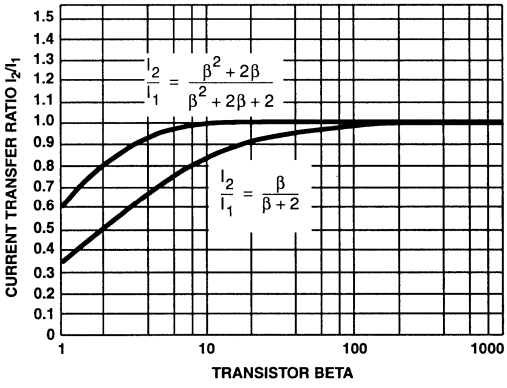
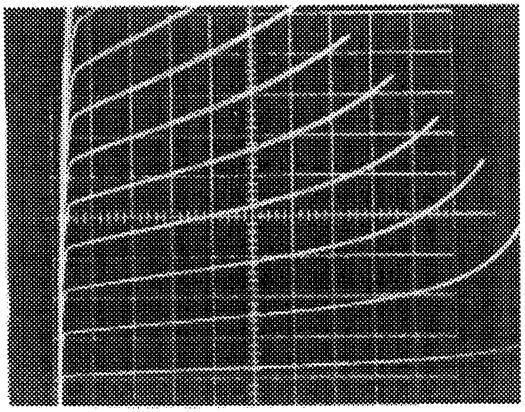


FIGURE 39C. CURRENT TRANSFER RATIO I_2/I_1 vs TRANSISTOR BETA

Figure 39D shows a curve-tracer photograph of characteristics for the circuit of Figure 39B. No consideration in this discussion is given to the variation of the transistor (Q_1) collector current as a function of its collector-to-emitter voltage. The output resistance characteristic of Q_1 retains its similarity to that of a single transistor operating under similar conditions. An improvement in its output resistance characteristic can be made by the insertion of a diode-connected transistor in series with the emitter of Q_1.



Scale: Horizontal = 2V/Div.
Vertical = 1mA/Div.
Steps = 1mA/STEP

FIGURE 39D. PHOTO SHOWING RESULTS OF FIGURE 39B

This diode-connected transistor (Q_3 in Figure 39E) may be considered as a current-sampling diode that senses the emitter-current of Q_1 and adjusts the base current Q_1 (via Q_2) to maintain a constant-current in I_2. Because all controlling transistors are operated at relatively fixed voltages, the previously discussed effects due to voltage coefficients do not exist. The curve-tracer photograph of Figure 39F shows the improved output resistance characteristics of the circuit of Figure 39E. (Compare Figure 39D and 39F).

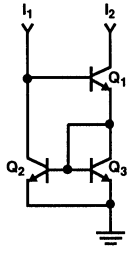
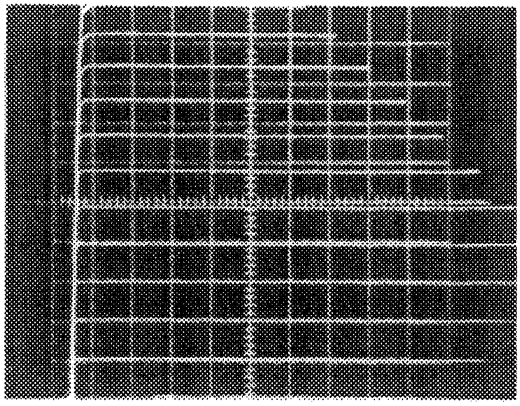


FIGURE 39E. DIODE - 2 TRANSISTOR CURRENT SOURCE



Scale: Horizontal = 2V/Div.
Vertical = 1mA/Div.
Steps = 1mA/STEP

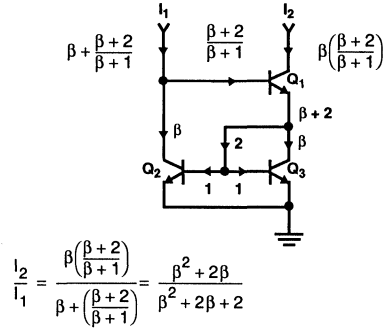
FIGURE 39F. PHOTO SHOWING RESULTS OF FIGURE 39E

Figure 39G shows the current-division within the mirror assuming a "unit" (1) of current in transistors (Q_2 and Q_3).

The resulting current transfer ratio

$$I_2/I_1 = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}.$$

Figure 39C shows this equation plotted as a function of beta. It is significant that the current transfer ratio (I_2/I_1) is improved by the β^2 term, and reduces the significance of the $2\beta + 2$ term in the denominator.



$$\frac{I_2}{I_1} = \frac{\beta\left(\frac{\beta+2}{\beta+1}\right)}{\beta + \left(\frac{\beta+2}{\beta+1}\right)} = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$$

FIGURE 39G. CURRENT FLOW ANALYSIS OF FIGURE 39E

Conclusions

The Operational Transconductance Amplifier (OTA) is a unique device with characteristics particularly suited to applications in multiplexing, amplitude modulation, analog multiplication, gain control, switching circuitry, multivibrators, comparators, and a broad spectrum of micropower circuitry. The CA3080 is ideal for use in conjunction with CMOS ICs being operated in the linear mode.

Acknowledgments

The author is indebted to C. F. Wheatly for many helpful discussions. Valued contributions in circuit evaluation were made by A. J. Visioli Jr. and J. H. Klinger.

No. AN9202 January 1992

Harris Linear

Using the HFA1100, HFA1130 Evaluation Fixture

Author: Jeff Lies

General Information

The HFA evaluation fixture is a special purpose board which frees users from the time-consuming task of developing their own evaluation hardware. It also serves as an example of the type of high frequency layout required by ultra high speed op amps. The board makes no provision for easy modification to other configurations. Modifications are strongly discouraged, since surface mount printed circuit pads tend to disintegrate after only a few resolderings.

The fixture is wired in a gain of +2 as shown in Figure 1. It is intended for use in a 50Ω environment, so input and output termination resistors have been incorporated. Figure 2 illustrates the typical frequency response of an HFA1100/30 in this fixture.

Evaluating the HFA1100

As delivered, the fixture is ideal for evaluating the HFA1100. The V_H and V_L connections have no effect, since pins 5 and 8 are not bonded out on the HFA1100. Figure 3 details a setup for evaluating the amplifier's pulse response, while Figure 4 illustrates the HFA1100 performance in this setup. The scope input trace accurately reflects the amplifier input, but the output trace is one-half the amplifier output voltage.

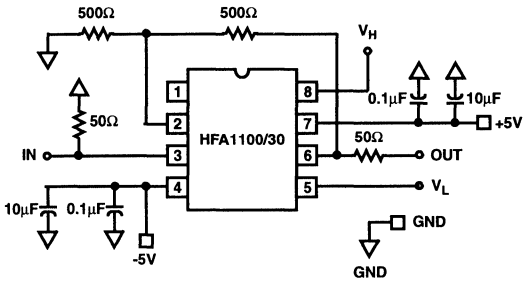


FIGURE 1. SCHEMATIC OF HFA1100/30 EVALUATION BOARD

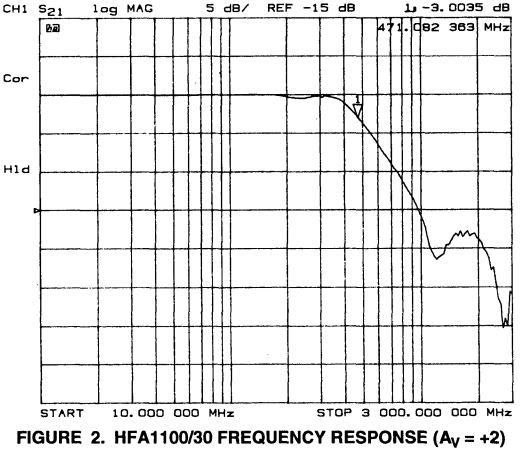


FIGURE 2. HFA1100/30 FREQUENCY RESPONSE (A_V = +2)

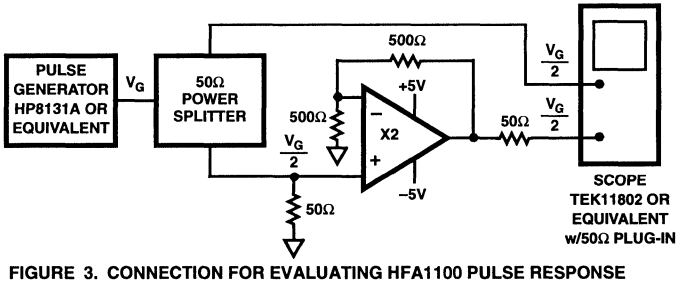


FIGURE 3. CONNECTION FOR EVALUATING HFA1100 PULSE RESPONSE

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Evaluating the HFA1120

This fixture is not recommended for evaluation of the HFA1120. The HFA1120 incorporates balance pins (pins 1 and 5) which are absent on the HFA1100. Pin 1 is unconnected on this fixture, while pin 5 is connected to the V_L terminal. The unequal capacitance on these pins may unbalance the amplifier and prevent any meaningful evaluation.

Evaluating the HFA1130

No fixture modifications are necessary when evaluating the HFA1130. When evaluating unclamped performance, the V_H and V_L inputs may be left floating. An unclamped HFA1130 performs like an HFA1100/20 in that the output is clamped to a default value of approximately ±4.2V. Even though the output swing is less than ±4.2V, the default clamp provides fast overdrive recovery on the HFA11XX family.

Figure 5 illustrates the HFA1130 clamped pulse response for a positive pulse. The set-up for evaluating the clamped overdrive recovery time is detailed in Figure 6. This set-up uses a slower pulse generator, since input transitions ≥2ns yield the best results.

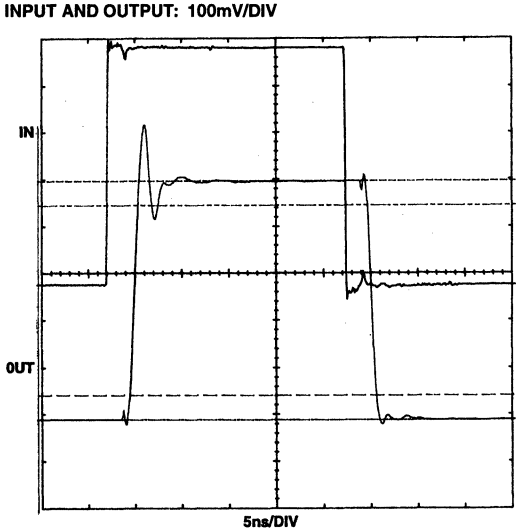

FIGURE 4. HFA1100 PULSE RESPONSE

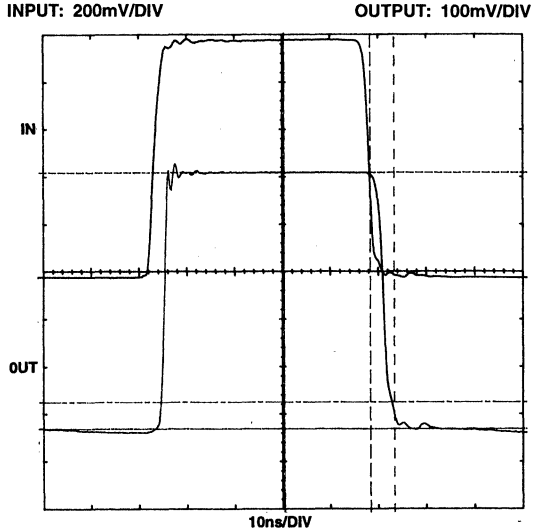

FIGURE 5. HFA1130 CLAMPED PULSE RESPONSE

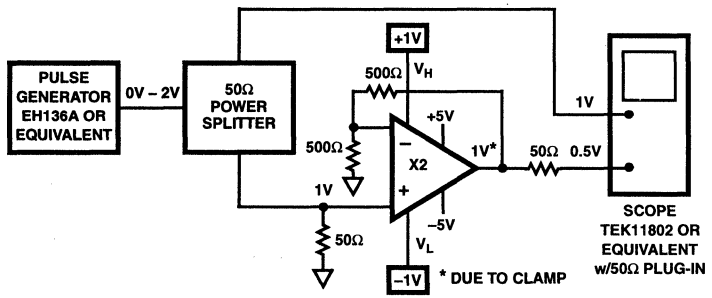

FIGURE 6. CONNECTION FOR EVALUATING HFA1130 OVERDRIVE RECOVERY

APP NOTE

No. AN9305 January 1995

Harris Linear

HA5020 Operational Amplifier Feedback Resistor Selection

Author: Steve Jost

Optimum AC performance of current feedback amplifiers in general and of the HA-5020 in particular depends upon careful selection of the feedback resistor, R_F. The benefit of higher usable bandwidth (compared with conventional voltage feedback amplifiers) and the ability to control the frequency response (by choosing the value of R_F) carries an expense in that the design process becomes more complicated. This is particularly true if an intuitive knowledge of how the device will behave in the end application is lacking. The purpose of this App Note is to provide a conceptual foundation on which this intuitive knowledge can be built.

The choice of the optimum resistor value depends upon design goals for the application subject to conditions of closed loop gain, source impedance, and load. As a point of reference, typical curves are provided in the data sheet that show how the frequency response is affected by closed loop gain, feedback resistor value, and load resistance. Source impedance, if it is large, becomes a factor only in conjunction with capacitance at the inputs. The data sheet curves are all generated with a 50Ω source impedance.

To illustrate how one might approach the problem of selecting a feedback resistor based on closed loop gain, consider the simple model of Figure 1. Between the inputs is a unity gain voltage buffer with non-zero output impedance indicated by R_I. The transimpedance gain, R_Z, is a function of frequency having a high DC value that forces I_ε to zero. The model's behavior is influenced by external elements consisting of a feedback network (R_F and R_G), source and load impedances (R_S and R_L), and stray capacitance at the amplifier's inputs (C_S).

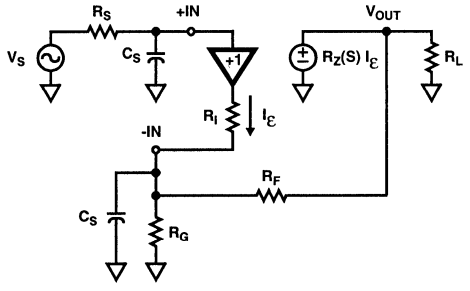

FIGURE 1. SIMPLE CURRENT FEEDBACK AMPLIFIER MODEL

Derivation of the transfer function will confirm that the non-zero inverting input impedance, R_I, causes the circuit's bandwidth to degrade as the closed loop gain increases, while stray capacitance at the negative input gives rise to gain peaking particularly at low gains (intuitively, C_S is in parallel with R_G causing the gain as determined by the feedback network to increase with frequency).

Gain peaking due to capacitance at the inverting input is most easily dealt with by placing a resistor in series with the positive input. If we assume that the stray capacitance at the positive input equals the stray at the negative input, we can choose R_S equal to the parallel combination of R_F and R_G. This introduces a pole at the positive input which cancels the zero at the negative input, thereby eliminating the gain peak. Note that any remaining gain peaking is a result of excessive phase shift around the loop. Excess phase shift around the loop can be reduced by increasing R_F.

Bandwidth degradation due to non-zero inverting input resistance is also easy to deal with as long as the product of the closed loop gain and the inverting input resistance does not exceed the optimum value for R_F in unity gain. By solving the transfer function for constant bandwidth, we arrive at the following equations for R_F and R_G:

$$R_F = R_{FO} - A_{CL} * R_I \quad \text{(EQ. 1)}$$

$$R_I = R_F / (A_{CL} - 1) \quad \text{(EQ. 2)}$$

Where,

R_{FO} is the optimum value for unity gain (1000Ω),

R_I is the inverting input impedance (75Ω), and

A_{CL} is the desired closed loop gain.

A comparison between actual measured results in Figures 2 and 3 provides graphic reinforcement for the utility of these equations. Figure 2 illustrates the failure to consider stray input capacitance and inverting input resistance, while Figure 3 incorporates the lessons learned from analyzing our simple model.

In Figure 2, a family of closed loop gain curves was obtained on a representative unit using R_S = 50Ω and constant R_F ($R_F = R_{FO}$ = 1000Ω). The measured stray capacitance at either input was 2pF. The results in Figure 3 were obtained from the same unit, except that (within the constraints of available standard resistor values) R_F and R_G were chosen according to the equations above and R_S was chosen to be equal to the parallel combination of R_F and R_G.

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One limitation of the above model is that it does not include the effects of the load. In general if R_L is 400Ω or above, the response is independent of the load. If R_L is less than 400Ω, the response becomes more damped and the bandwidth degrades. Here again the bandwidth degradation can be compensated for by lowering the value of R_F.

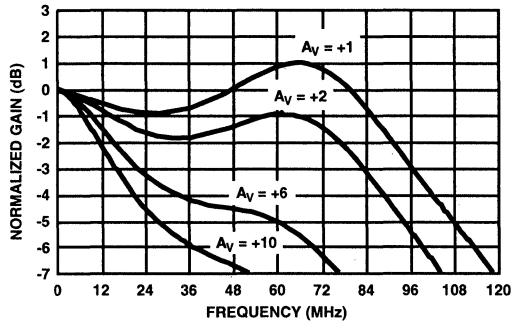


FIGURE 2. FREQUENCY RESPONSE vs CLOSED LOOP GAIN USING FIXED R_F = 1kΩ, R_S = 50Ω, R_L = 402Ω

TABLE 1. RESISTOR VALUES FOR FIGURE 2

A_V	R_F (Ω)	R_G (Ω)	R_S (Ω)	BW (MHz)	PEAKING (dB)
+1	1K	-	50	97	1
+2	1K	1K	50	84	<0
+6	1K	200	50	22	<0
+10	1K	110	50	16	<0

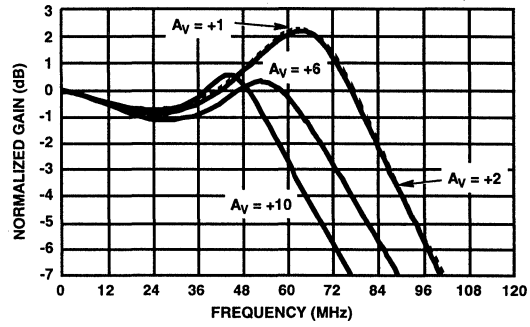


FIGURE 3. FREQUENCY RESPONSE vs CLOSED LOOP GAIN $R_F = 1000\text{-}A_V(75\Omega)$, $R_S = R_F \text{ II } R_G$, R_L = 402Ω

TABLE 2. RESISTOR VALUES FOR FIGURE 3

A_V	R_F (Ω)	R_G (Ω)	R_S (Ω)	BW (MHz)	PEAKING (dB)
+1	909	-	909	87	2
+2	825	825	422	87	2
+6	562	110	90.9	74	0.5
+10	237	26.1	23.7	62	0.5

NOTE: $R_F = 1000\text{-}A_V(75\Omega)$, $R_S = R_F \text{ II } R_G$, R_L = 402Ω

Harris Semiconductor

APPNOTE

No. AN9313.1 November 1996

Harris Data Acquisition

Circuit Considerations In Imaging Applications (HA-2546, HA-5020, HA-5033, HI-5700)

Author: Phil Louzon

Introduction

Present day image-processing systems perform many functions such as low pass filtering and pattern recognition in the digital domain. However, as shown in the block diagram, the analog input signal must first pass through some signal conditioning and then be digitized by an A/D before it can be manipulated by the Digital Signal Processing (DSP).

It is these front end components that will set the overall dynamic range and resolution of the system and hence the detail that can be resolved in the image. This note will describe the considerations involved in designing and testing the performance of this part of the system.

Video Format

RS-170 is a standard video format for monochrome television. It was later updated to RS-170A by NTSC to cover the requirements for color television broadcasting in the U.S. The FCC has control over broadcast video standards; but, since imaging processing systems are self contained, they do not have to follow a particular standard. For example, color cameras might provide three RGB outputs (component video) or a composite NTSC color signal. System synchronization schemes could also vary greatly.

A typical RS-170 image, or frame, is made up of two interlaced fields. The first field scanned represents the odd numbered lines; the second is the even numbered lines. A total of 525 lines per frame will be scanned in 1/30 of a second with 485 lines being visible. The number of active elements per line, or pixels, varies from system to system depending on the desired resolution.

The RS-170 monochrome composite video signal is shown in Figure 1. System timing is controlled by vertical and horizontal sync pulses. Horizontal sync controls the line by line timing and occurs during the 10.9µs blanking period. Vertical sync controls the field timing and occurs at 1/60 of a second rate. The brightness information for the video image is transmitted during the active line time and will vary from the reference black level (7.5 IRE) to the reference white level (100 IRE).

RS-170 normally has an aspect ratio of 4:3. However, because of frame buffer memory and DSP requirements many image-processing applications will use a 1:1 aspect ratio. Figure 2 depicts the resulting picture and timing requirements for a RS-170 video with a 1:1 aspect ratio. The active line time is 39.44µs centered with 6.575µs of "inactive" time on either side. Notice that for 512 active pixels per line and 485 lines one frame of digitized video information will fit into 248,320 of memory.

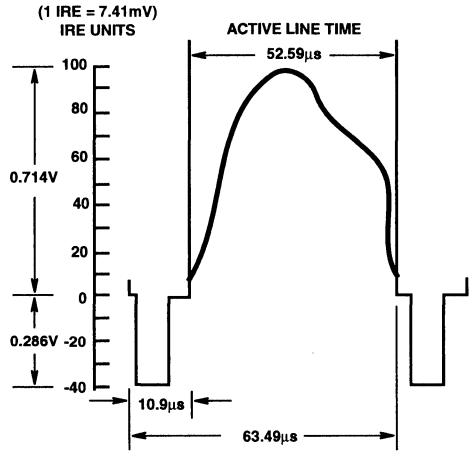
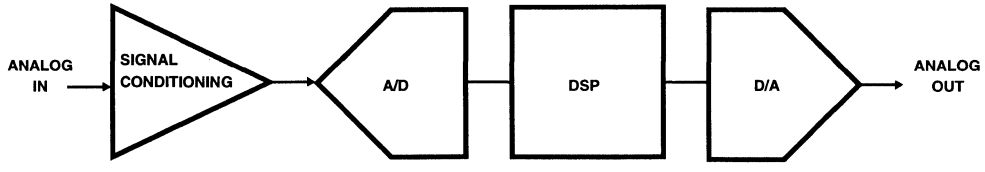


FIGURE 1. STANDARD RS-170 COMPOSITE VIDEO SIGNAL

Imaging System Block Diagram



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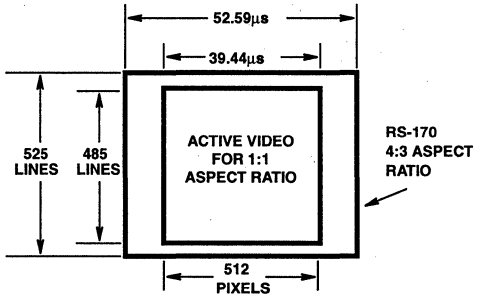


FIGURE 2. MODIFIED RS-170 VIDEO

Circuit Design Considerations

The analog waveforms seen by the signal conditioning front end to an image-processing system can be classified as small signal or large signal. The appropriate analysis should be used in each case. A good rule of thumb is to say any signal of less then a $1V_{P-P}$, like RS-170 video, should be considered as small signal.

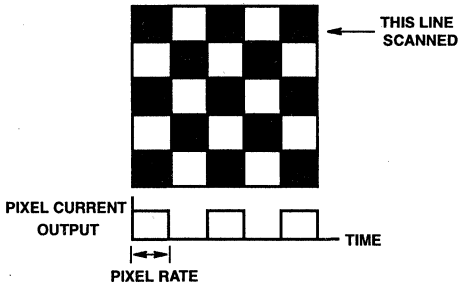


FIGURE 3. VIDEO

Figure 3 is an example of a worst case light pattern that might be seen by a small section of a Charge Coupled Device (CCD) array inside a video camera. Each square represents an individual pixel. The rate at which these pixels are scanned will determine the bandwidth requirements. If it takes 39.44ms to scan the 512 active pixels, then the pixel clock rate would be 12,981,174 elements per second. The video signal is a square-wave with a fundamental at half the pixel rate of 12,981,174/2 or 6.4MHz. To pass this signal undistorted would require a great deal of small signal bandwidth however, a bandwidth of 4MHz has been found to be adequate for video.

Insufficient high frequency response and phase distortion of a video signal will result in blurring of the fine detail in a picture and the overall image will look darker than normal. Therefore, the first requirement for the signal conditioning circuit is that its small signal bandwidth needs to be considerably wider than the bandwidth of the incoming video. This will ensure a constant gain over the frequency band of interest and avoid a loss of dynamic range as the input to the A/D rolls off.

The second requirement is that the system should have zero phase shift over its entire frequency range. Because this is impractical, a realistic goal is a phase shift that is proportional to frequency. That is, the second harmonic should be delayed twice as much as the fundamental, the third three times as much, and so on. When this occurs all the frequency components will end up having the same amount of time delay resulting in a image that is only delayed slightly in time and can easily be adjusted for.

For a single pole system, the attenuation factor and phase shift at a particular frequency relative to the f_{-3dB} can be calculated from:

$$A(f) = \frac{1}{\sqrt{1 + \left(\frac{f}{f_{-3dB}}\right)^2}} \quad \text{(EQ. 1)}$$

and

$$\theta(f) = \operatorname{atan}\left(\frac{f}{f_{-3dB}}\right) \quad \text{(EQ. 2)}$$

Taking these error terms into account, the complete equation for a sinewave including the effects of the system would now be:

$$V(t) = \frac{A}{\sqrt{1 + \left(\frac{f}{f_{-3dB}}\right)^2}} \times \sin\left(\omega t + \operatorname{atan}\left(\frac{f}{f_{-3dB}}\right)\right) \quad \text{(EQ. 3)}$$

In Equation 1, when f equals 4MHzand the attenuation A(f) is one 8-bit LSB (0.4%) the required small signal bandwidth f_{3dB} would be 40MHz. The corresponding phase shift at 4MHz from equation 2 would be 5.7 degrees.

By the time the video has reached the input to the A/D it has been amplified enough so that large signal parameters such as slew rate and full power bandwidth (FPBW) have to be considered. The required slew rate can be found by taking a conservative approach and forcing the video signal to slew through its range in 25% of the pixel clock. Therefore, if the pixel clock is 12.98MHz (pixel time is 77ns) and the reference for the A/D is 4V, then the minimum slew rate required would be:

$$SR_{MIN} = \frac{4V}{0.25 \times 77ns} = 208\frac{V}{\mu s} \quad \text{(EQ. 4)}$$

Now that the slew rate has been determined the minimum required full power bandwidth of the signal conditioning block and the converter can be calculated from:

$$FPBW = \frac{SR_{MIN}}{2 \times \pi \times V} = \frac{208}{2 \times \pi \times 4} = 8.3MHz \quad \text{(EQ. 5)}$$

Trying to relate the above equation for FPBW to the FPBW quoted for a converter should be done with caution by the user and requires a knowledge of the way it has been defined by the A/D manufacturer. One method used will test for the presence of sparkle codes. These are anomalous codes that show up when the input slew rate exceeds a certain value. The term sparkle code comes from the fact they will cause bright pixels in a video display.

Figure 4 is a plot of a sinewave input to a converter that has been digitally reconstructed and shows evidence of sparkle codes. The FPBW is then determined from the maximum fullscale input frequency that has sparkle free performance.

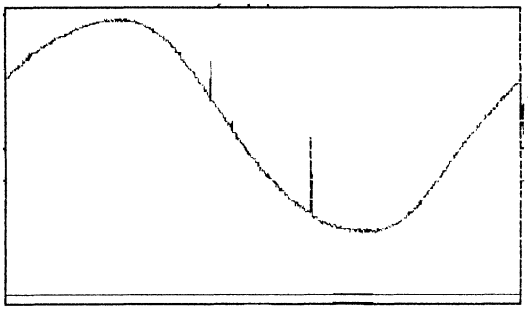


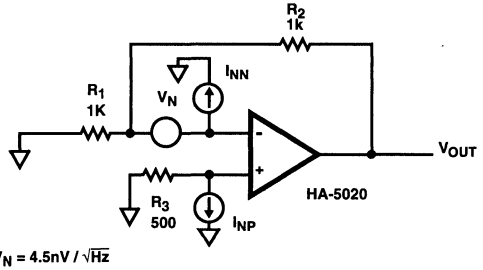
FIGURE 4. RECONSTRUCTED SINEWAVE

Some manufacturers will quote FPBW as the point in the frequency domain where the fundamental is 3dB down from the low frequency value. This method will tend to average out sparkle codes. Other A/Ds will have the FPBW specified as the point where a reconstructed sinewave in the time domain is 3dB down from the low frequency value. The user must determine if the test method used by the manufacturer to determine the quoted FPBW will ensure accurate sparkle free performance at their operating frequencies.

Sparkle codes can also occur if the maximum conversion rate of the A/D is exceeded. For example, the HI-5700 is an 8-bit CMOS flash converter that has datasheet limit for conversion rate of 20MHz. However, as is the case for many flash converters, by skewing the duty cycle of the sampling clock the part can be made to operate at 25MHz and higher.

The theoretical best dynamic range that can be expected from an A/D with n bits of resolution can be calculated from: $DR(dB) = 20 \log (2^n) = 6.02(n)$. An image-processing system would be expected to have a dynamic range of at least 36dB or about 6 bits.

In order to make use of the full dynamic range available from the converter, the overall system noise should be less than the theoretical quantization noise of the converter $q/(\sqrt{12})$ (q is the A/D lsb size). Figure 5 is a typical voltage feedback or current feedback op amp circuit that will be used to illustrate some basic noise calculations. The voltage noise (V_N) and noise current (I_N) sources have been modeled, but the Johnson noise of the resistors will be neglected because of the low resistor values normally used in high-speed circuits.



$V_N = 4.5nV / \sqrt{Hz}$

$I_{NN} = 25pA / \sqrt{Hz}$; $I_{NP} = 2.5pA / \sqrt{Hz}$

FIGURE 5. OP AMP NOISE MODEL

The equation for the total RMS noise over the bandwidth of interest is:

$$V_{TOT} = \sqrt{1.57 \times f_{BW}} \times \quad \text{(EQ. 6)}$$

$$\sqrt{(V_N)^2 \times \left(1 + \frac{R_2}{R_1}\right)^2 + (R_2)^2 \times (I_{NN})^2 + (R_3)^2 \times (I_{NP})^2 \times \left(1 + \frac{R_2}{R_1}\right)^2} \quad \text{(EQ. 7)}$$

Where:

V_{TOT} is the total RMS noise voltage.

R_1 is the feedforward resistor.

R_2 is the feedback resistor.

R_3 is the noninverting input resistor.

V_N is input voltage noise spectral density.

I_{NN} is the inverting input current noise spectral density.

I_{NP} is the noninverting input current noise spectral density.

f_{BW} is the bandwidth over the region of interest.

As is normal for current feedback op amps, the HA-5020 has unequal I_{NN} and I_{NP}.

For the values given in the figure over the 18MHz FPBW specified for the HI-5700 8-bit flash A/D the RMS noise V_{TOT} is found to be equal to 106mV. The peak noise value will be about five times this value or 530mV. This is significantly less than the 4.5mV of quantization noise for an 8-bit ADC with a 4V range.

This example has shown how to model the noise of a opamp. If there are other noise sources present, then the total noise can be found by taking the RMS sum of all the individual noise sources.

A wide dynamic range is usually required of a signal conditioning block to accommodate large incoming signal variations. Automatic Gain Control (AGC) will compensate for these variations and allow the user to design with a lower resolution A/D.

The AGC circuit should be considered a control loop, and its frequency and phase characteristics plotted. A slow AGC loop could compensate for slow offset or gain changes over temperature while a faster AGC loop could compensate for signal overload conditions.

There are a number of opinions on where the AGC should be applied. An easy way to do it is to vary the reference on the A/D depending on signal strength. This will work fine if the converter has been thoroughly characterized over the range of reference voltages it will see. Unfortunately this is usually not the case. Most datasheets will not specify the performance of the converter versus reference voltage. Therefore, the user is taking a significant chance that the part performance will stay the same over the life of the system for various manufacturing lots of the A/D. The second option is to let the AGC vary the gain of the signal conditioning circuitry while leaving the reference to the A/D at the value where the performance is guaranteed by the datasheet. This approach will guarantee the long term success of a circuit. The design section of this note will discuss a technique using a multiplier chip to accomplish this.

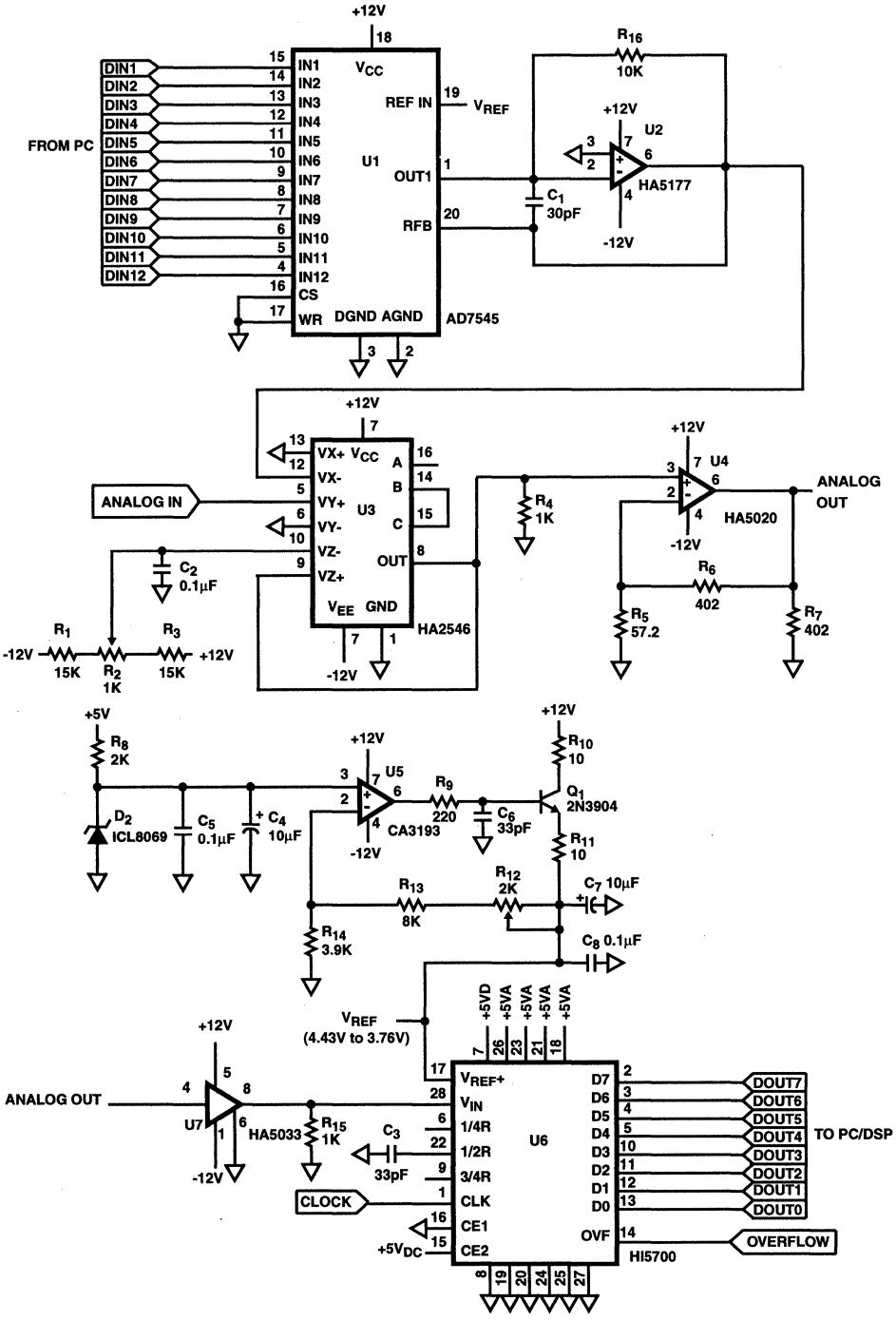


FIGURE 6. DESIGN FOR VIDEO IMAGING FRONT END

System Design

Figure 6 is a design for a signal conditioning and A/D front end to an image-processing system. The video input to the system will be assumed to have a positive picture phase. That is, the blanking and sync pulses will be the most negative portion of the video waveform. When the video is ac coupled, the black reference level has to be reinserted prior to the A/D. If this is not done, then, as the amplitude of the video signal is reduced, due to a reduced contrast image, the blanking level moves more positive. The resulting image will now appear a light shade of gray, rather than the preferred black level. Also, the DSP becomes more sensitive to coupled noise and may for example, during edge detect, show an edge where none exists.

Figure 7 is a simple circuit to DC restore the video. This circuit clamps the most negative point of the signal to -0.7V which can now be offset by the HA-2546 to provide a stable black level during changing contrast. Another 8-bit 20 MSPS converter from Harris Semiconductor, the HI1176, has an internal circuit which will clamp the back porch of a video signal to a voltage input on the reference pin.

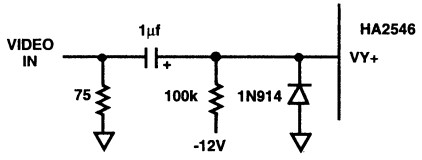


FIGURE 7. DC RESTORE CIRCUIT

The HA-2546 is a wideband two quadrant analog multiplier which makes the implementation of AGC offset and gain correction easy. It is configured in this design to give the transfer function:

$$V_{OUT} = \frac{(V_X \times V_Y)}{2} - V_Z \qquad \text{(EQ. 8)}$$

The V_Z pin can be used to correct for system offset as long as it does not exceed ±5V. The initial offset adjustment is set by pot R_2. The V_X pin can be used to adjust system gain.

U5 is part of a reference circuit in Figure 6 that provides the 4V reference required by the A/D and the DAC. It is capable of 8-bit performance over the industrial temperature range. Pot R_{12} will set the initial overall system gain.

For the reasons outlined above, it was decided to leave the reference to the flash at its nominal datasheet value and let the AGC adjust the gain of the signal conditioning components prior to the converter. A AD7545 12-bit DAC is used as part of a slow AGC loop which uses the V_X pin of the HA-2546 to control the gain of the system.

As illustrated in Figure 8, the feedback loop could be closed by a microprocessor using the overflow bit on the HI-5700 and could compensate for light intensity shifts or temperature drift. In order to avoid any glitches the DAC should be updated during the vertical retrace period.

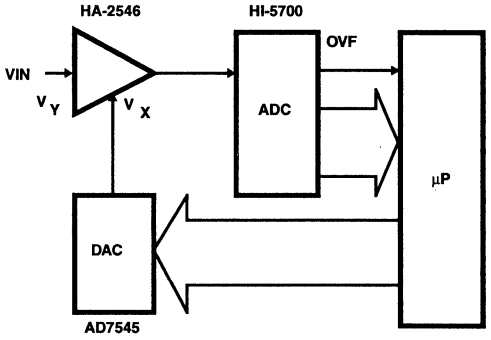


FIGURE 8. SLOW AGC LOOP

The HA-5177 op amp acts as an I/V converter for the DAC. Its feedback is set so that at all ones to the DAC the output voltage will be -2V which is the maximum voltage that is allowed on the V_X pin. At the normal operating point for the system the DAC will be at midscale and the overall system gain will result in a full scale swing to the A/D. Since the DAC is at midscale the system has an equal amount of gain correction range up and down.

The HA-5020 is a high-speed current feedback op amp which provides additional gain so that a nominal $1V_{P-P}$ signal input to the system the HI-5700 flash will see its full 0V to 4V swing. If the sync has been stripped from the video before it is digitized [8], then the gain could be adjusted so that the video reference black to reference white level will span the full range of the converter.

A high-speed unity gain op amp (HA-5033) buffers the input to the HI-5700 and provides the necessary low output impedance over frequency required by flash converters. Although the HA-5020 can drive the HI-5700 directly, the HA-5033 has superior current drive, lower output impedance, and better bandwidth.

The pixel clock of 12.98MHz will usually determine the minimum sampling rate of the A/D. In order to relax the filter requirements on the front end to the system the actual sampling rate used in this note is 15MHz. This will be more than adequate to cover all established sampling rates specified for the various published standards.

Additional timing circuitry might be added to gate the pixel clock so that it is only on during the active line period thereby conserving frame buffer memory size. If the system uses an interlaced video format then the circuitry could also define the even and odd fields of the image frame and update the memory accordingly.

The clock period for the HI-5700 8-bit flash is made up of an autozero time and sample time. It was found that the autozero time can be reduced down to as little as 15ns while the sampling time must remain at 24ns or greater. This timing allows the sparkle free operation of the circuit at pixel rates up to 25MHz.

There are many considerations which have to be taken into account when using high speed converters. These involve board layout, choosing the right op amp to drive the input, and designing a low drift reference. Refer to references 6 and 7 for a complete discussion of these topics and others.

Test Results

The IEEE has various standards which address the type of tests that need to be done on a broadcast video system to verify the performance of a video A/D and D/A combination (codec). Among them are DC linearity, Signal-To-Noise Ratio (SNR), bandwidth, and differential phase and gain. Since this note deals only with RS-170 monochrome video signals, the tests that deal with the color information, such as differential phase and gain, are not applicable. Also, adding a DAC on the output of the converter in order to use the IEEE test methods would tend to cloud its overall performance of the system with the errors of the DAC. Therefore, the system will be evaluated using a set of tests that are similar to those recommended by the IEEE but are done by analyzing the digital data out of the converter. These tests can also be found on a datasheet for a typical flash A/D. Hopefully, as a result of this approach the user will now also be able to more intelligently read and compare converter datasheets.

There is a great deal of information in the low frequency (30Hz) content of video. Historically, the low frequency performance of an A/D has been evaluated by the Differential (DNL) and Integral (INL) NonLinearity specs. DNL is a measure of the deviation of the code widths from the ideal value of one Least Significant Bit (LSB). INL is the deviation of the code edges from the ideal transfer curve of the A/D. Since the A/D in this system is initially calibrated for offset and gain, the line used as a reference will be one drawn through the first and last transition point.

The DNL and INL errors can not be calibrated out and is the best accuracy that can be expected of the system. Therefore, the INL error should ideally not exceed 1/2 LSB so that when it is combined with the inherent 1/2 LSB quantizing error of an A/D the total error would not exceed 1 LSB. A DNL error of more than -1 LSB means a code is missing from the transfer curve. An INL error of 1/2 LSB will ensure a DNL error of at most 1 LSB.

Figure 9 shows a plot for the transfer function of a converter with DNL and INL errors. The reference curve and the ideal transitions are pointed out. Transition point 3 is offset in the negative direction by 1/2 LSB therefore the ILE at this point is -1/2 LSB. The ILE of all the other transitions is zero. The DLE of code 2 is -1/2 LSB and the DLE of code 3 is +1/2 LSB.

The actual linearity test was done using a histogram approach. A triangle wave is input to the system and the number of occurrences of each code is kept track of. DNL error is then calculated in LSBs from:

$$DNL(i) = \frac{(P_m(i))}{(P_i(i))} - 1 \qquad \text{(EQ. 9)}$$

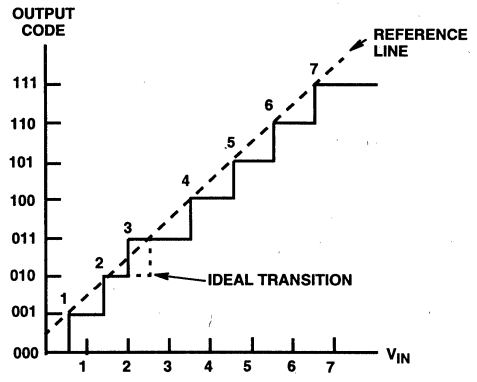


FIGURE 9. A/D TRANSFER FUNCTION

The ideal probability, P_i is a constant and is equal to the average of the number of counts per code divided by the total number of samples. P_m is the measured probability and is equal to the total number of counts for a particular code divided by the total number of samples. Once the DNL error has been determined the INL error is calculated from the sum of the DLE errors.

A histogram was done on the design discussed in this note by inputting a $1V_{P-P}$ 5kHz triangle wave, encoding the HI5700 at 15MHz, and capturing the digital data. Figure 10 and Figure 11 are plots of the DNL and INL error for the total system indicating an accuracy of better than 7 bits with no missing codes.

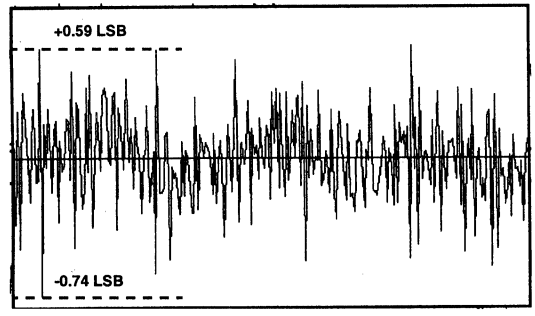


FIGURE 10. DIFFERENTIAL LINEARITY ERROR vs CODE

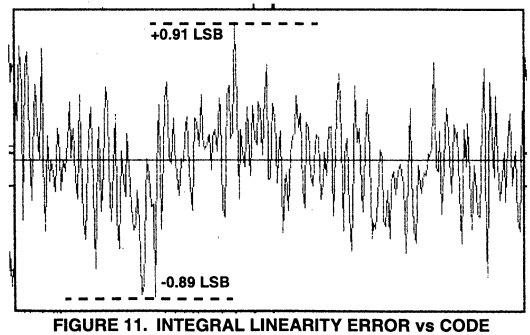


FIGURE 11. INTEGRAL LINEARITY ERROR vs CODE

Due to various dynamic effects such as slew rate limiting and bandwidth rolloff the static DNL and INL will degrade as the input frequency approaches the 4MHz bandwidth requirement of video. DNL will show up as an increase in the quantization noise which will tend to elevate the noise floor of the A/D. INL is a bend in the transfer curve of the converter and will generate harmonics. Both result in a loss of dynamic range of the system.These effects are usually evaluated in the frequency domain by finding the SIgnal-to-Noise-And-Distortion (SINAD) in dB.

The SINAD test requires performing a fourier transform on the data obtained by sampling a continuous time input waveform. The Discrete Fourier Transform (DFT) can be thought of as a frequency selective filter that calculates the RMS voltage at a particular frequency and will work for any number of samples.

The coefficient for a particular frequency can be found from:

$$X_d(k) = \sum_{n=0}^{N-1} x(n) \times e^{-j2\pi k(n/N)} \qquad \text{(EQ. 10)}$$

N is the number of samples.

n is the time sample index (n = 0, 1, 2, ... , N-1).

k is the index for the computed frequency components (k=0, 1, 2,...,N-1).

The Fast Fourier Transform (FFT) is an algorithm that will compute all the DFT coefficients at one time; but, unlike the DFT it will only work for sample sizes that are a power of two. The FFT will output the coefficients for N/2 discrete frequency bins that will have a resolution of F_{sample}/N.

Once the FFT has been performed SINAD can be calculated from:

$$SINAD_{dB} = 20 \times \log\left(\frac{RMS_{SIGNAL}}{RMS_{NOISE}}\right) \qquad \text{(EQ. 11)}$$

Where RMS_{SIGNAL} is the measured RMS signal in the fundamental bin and RMS_{NOISE} is the sum of all other spectral components below the Nyquist frequency excluding DC. It is important that the distortion components be included in this calculation in order to take into account all the system errors.

The Effective Number Of Bits (ENOB) of the system can be found by:

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02} \qquad \text{(EQ. 12)}$$

ENOB is a global indication of the accuracy of the system and, along with INL and DNL will degrade as the input frequency is increased. The low DNL and INL errors indicate the excellent low frequency performance of the design. This was again verified by inputting a $1V_{P-P}$ sinewave at 20kHz, encoding the part at 15MHz, and performing an FFT on the data. The SINAD was calculated to be 44.5dB for an ENOB of 7.1 bits. An indication of the overall low noise in the system.

The high frequency performance of the system was evaluated by changing the input frequency to 4MHz and again performing an FFT. Figure 12 is a spectrum plot of the system output. The SINAD for this plot was determined to be 38.2dB for an ENOB of 6.05 bits.

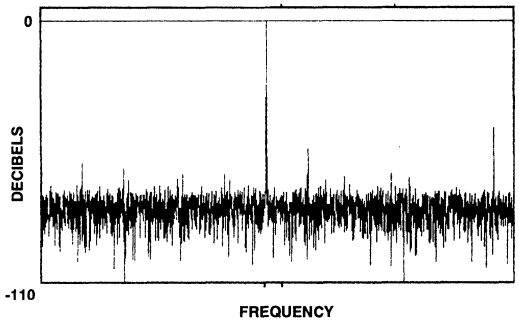


FIGURE 12. HIGH FREQUENCY SPECTRAL PLOT OF SYSTEM (f_I = 4MHz)

The full power bandwidth and slew rate capability of the system was checked by inputting a fullscale sinewave at 8MHz and sampling it at a 15MHz rate. Figure 13 shows the resulting reconstructed waveform. Notice the lack of distortion and sparkle codes.

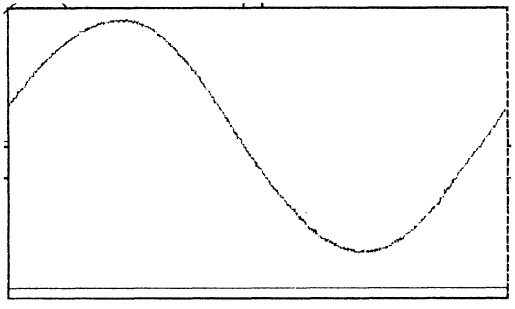


FIGURE 13. RECONSTRUCTED SINEWAVE (f_I = 8MHz)

Time Division Multiplexed Systems

This note is mainly concerned with RS-170 type video signals. However, it is instructive to briefly discuss the factors to consider when dealing with other time division multiplexed signals that might be seen from some types of CCD arrays, a multiplexed input, or an infrared sensor array.

The output of CCD arrays many times will have the signal of interest riding on a large DC offset. Figure 14 is an example of an inverting buffer that can be used to remove large offsets. Notice that since resistor R_3 sees a virtual ground Voffset can take on a value much higher than the supply voltage.

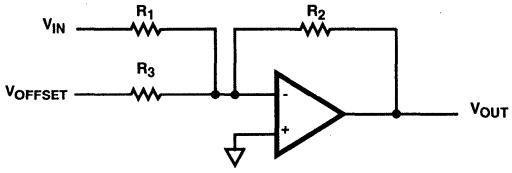


FIGURE 14. INVERTING BUFFER

The circuit gain can be calculated from:

$$V_{OUT} = (-R_2/R_1) \times V_{IN} - (R_2/R_3) \times V_{OFFSET} \quad \text{(EQ. 13)}$$

The circuits that process large signal pulse type waveforms must slew and settle quickly so, as depicted in Figure 15, the A/D can then accurately digitize the pixel information. Given the ever increasing pixel rates this can become quite a challenge.

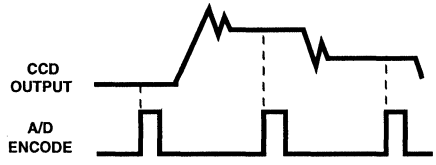


FIGURE 15. TIME DIVISION MULTIPLEXED SIGNAL

The overall system settling time is made up of two parts. Initially the signal must slew until it enters a region where small signal analysis takes over. Similar slew rate requirements as discussed in the design considerations section apply in this case also. For a single pole system, the error will then decay with a time constant determined by the small signal bandwidth of the system. The settling time in an actual system is very much a function of the circuit parasitics and the overall frequency response of the circuit. As such, it is difficult to calculate an accurate number beforehand. Reference 2 has a more thorough discussion of settling time and the calculations involved.

Additional large signal time domain converter specifications such as overvoltage recovery time and transient response time become important in these types of applications. As in the case of full power bandwidth, there are many ways to define these tests so be aware of the method used on the datasheet and how it applies to a particular application.

Once the circuits have settled then the A/D must digitize the level it sees at its input. The accuracy with which this can be done is a function dynamic range of the system and will be determined by the low frequency accuracy of the converter, the noise generated in the signal conditioning circuits, and the noise added by the converter. The INL, DNL, and low frequency SINAD specifications can be used to predict performance of the system with a particular converter.

The HI5800 is a low noise 12-bit 3 MSPS converter that is perfect for the applications which require a higher dynamic range at slower pixel rates. It is a complete sampling converter with on board sample and hold and reference. The low frequency (20kHz input) SINAD of typically 70dB reflects its outstanding low noise performance. The high frequency (1MHz input) SINAD number of 68dB illustrates how the performance is maintained at higher input frequencies.

Conclusion

This note has discussed the various considerations involved in designing the analog front end to an image-processing system. A system design was presented and proved to have accurate sparkle free performance at typical video frequencies.The methodology presented could be used to analyze the system requirements for systems with higher pixel rates.

References

[1] Joey Doernberg, Hae-Seung Lee, David A. Hodges, "Full Speed Testing of A/D Converters," IEEE Journal of Solid State Circuits, Vol. SC-19, No. 6, DEC. 1984.

[2] Fredrickson, Thomas M.,"Intuitive Operational Amplifiers," McGraw-Hill Inc., New York, NY, 1988.

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[5] "High Speed Design Seminar," Published by Analog Devices, 1990.

[6] "High Speed Signal Processing Applications Seminar", Published by Harris Semiconductor, 1992.

[7] "Using Harris High Speed A/D Converters," Application Note AN9214, Published by Harris Semiconductor, 1992.

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APPNOTE

No. AN9314.1 November 1996

Harris Linear

Harris UHF Pin Drivers

Author: Taewon Jung

Introduction

The HFA5250 [1] and HFA5251 are pin drivers designed for use in automatic test equipment (ATE) and high speed pulse generators. Pin drivers, especially those with very high-speed performance, have generally been implemented with discrete transistors (sometimes GaAs) on a circuit board or in a hybrid. Recent IC process improvements, specifically Harris' UHF1 process [2], have enabled the manufacturing of the 500MHz and 800MHz silicon monolithic pin drivers, HFA5250 and HFA5251.

The ultra-high speed performance of HFA5250 and HFA5251 is a result of UHF1 process leverages: low parasitic collector-to-substrate capacitance of the bonded wafer, low collector-to-base parasitic capacitance of the self-aligned base/emitter technology and ultra-high f_T NPN (8GHz) and PNP (5.5GHz) poly-silicon transistors.

Functional Block Diagram

HFA5250 and HFA5251 circuits share the common functional block diagram shown in Figure 1.

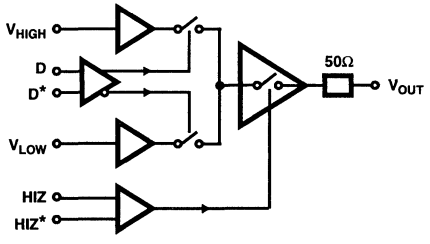

FIGURE 1. BLOCK DIAGRAM

The control inputs, D and D*, determine the output level. If D is at logic "1" and D* is at logic "0", the output level will be the same as V_{HIGH}. If D is at logic "0" and D* is at logic "1", the output will be the same as V_{LOW}. The control inputs, HiZ and HiZ*, make the output either active or high-impedance. If HiZ is at logic "1" and HiZ* is at logic "0", the output will be in high-impedence mode. If HiZ is at logic "0" and HiZ* is at logic "1", the output will be enabled. The output impedance in the enabled mode is trimmed to 50Ω.

Circuit Schematic

The Pin Driver circuit consists of a switch, an output buffer, and two differential control elements as shown in Figure 2.

A two stage approach, separating the switch from the output buffer, allows the speed and accuracy requirements of the switch to be decoupled from the load driving capability of the buffer.

The patent pending switch circuitry [3] uses cascaded emitter followers as input buffers and also to switch the input V_{HIGH} and V_{LOW} to node VSO. Dual differential pairs controlled by the data timing (D and D*) direct current to select either the V_{HIGH} or V_{LOW} switch. Matching transistor types and transdiodes improve linearity and lowers the voltage offset and offset drift. Stacking two emitter-base junctions allows the V_{HIGH} to V_{LOW} range to be extended to two BVebos of the process. The speed of the pin driver is largely determined by the current flowing through the switch stage and the collector-base capacitance of the output stage transistors connected to the node VSO.

The output stage consists of cascaded emitter followers constructed in a typical push-pull manner as shown in Figure 2. However, transdiodes are added to increase the voltage breakdown characteristics of the output during high-impedance mode. HiZ and HiZ* control the mode of the output stage. A trimmed, NiCr resistor is added to provide the 50Ω output impedance.

Overall, a symmetry of device types and paths is constructed to improve slew and delay symmetry. Both the V_{HIGH} to V_{OUT} path and the V_{LOW} to V_{OUT} path contain three NPN and three PNP transistors operating at similar collector currents. Thus the transient response of V_{HIGH} to V_{LOW} and V_{LOW} to V_{HIGH} are kept symmetrical. Also, a trimmable current reference (not shown) allows the AC parameters to be adjusted to maintain unit to unit consistency.

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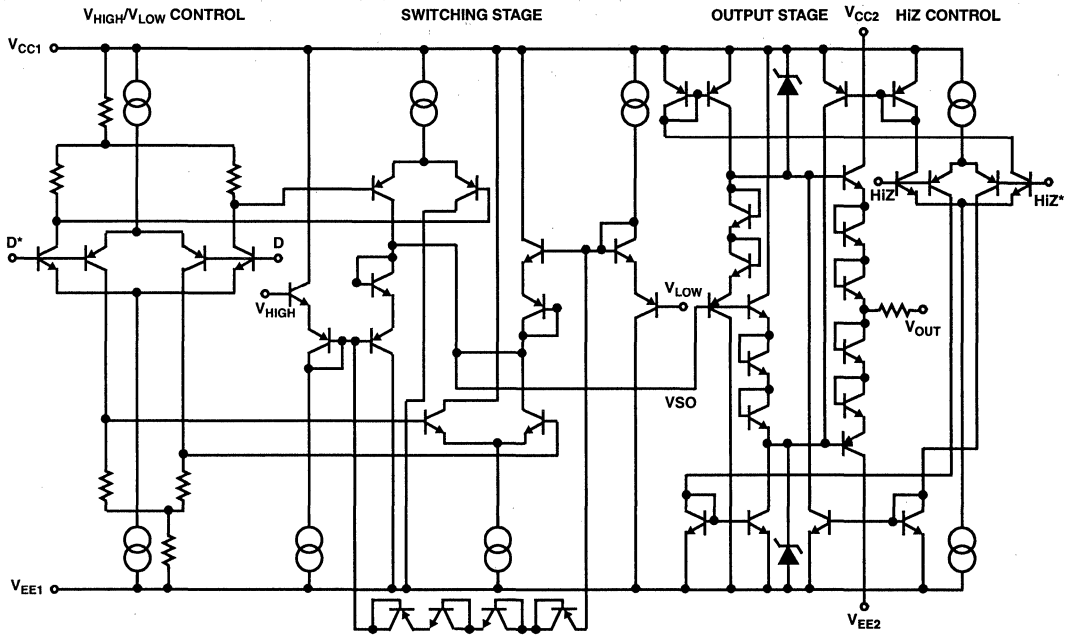

FIGURE 2. CIRCUIT SCHEMATIC

Speed Advantage

Harris Pin Drivers on bonded wafer technology definitely have a speed advantage, coming from the low collector-to-substrate capacitance and the high fT of the transistors. In addition, the patent-pending switching stage which fits uniquely to Harris' UHF1 process is another big contributor to the high speed. This switching circuitry requires low series resistance NPN and PNP transdiodes available in UHF1. The rise and fall times of the pin driver are largely determined by the slew rate at the node VSO in Figure 2. The dominant mechanism for the slew rate is the charging/discharging of the collector-base capacitors of the transistors connected to the node VSO. The charging/discharging currents are coming from the switching stage current sources. The fast rise and fall times are achieved because of the negligible collector-to-substrate capacitance and the small base-collector capacitance due to the self-aligned recessed oxide [2].

The D/D* differential stage is not a factor for the speed if its current sources have enough current not to bottleneck the transient. However it should be noted that the propagation delay mismatch is determined by this stage. Sufficient current is allocated to the differential stage current sources to best match the low-to-high and high-to-low transient propagation delays.

Figure 3 shows various output responses, 0V to 1V, 0V to 3V, 0V to 5V, and -2V to 7V (full swing). The load condition is a 16 inch 50Ω SMA cable with a 5pF capacitor at the end of the cable. The rise/fall time with $5V_{P-P}$ is typically 1.95ns for the HFA5250 and 1.45ns for the HFA5251. Pin drivers, built with the same circuit structure as shown in Figure 2, can be made faster by trimming for a higher power supply current. Currently the pin driver has rise/fall times of less than 1ns (10% to 90% of $5V_{P-P}$) when Icc is trimmed to 125mA. Further speed enhancement will be made if there is a market demand.

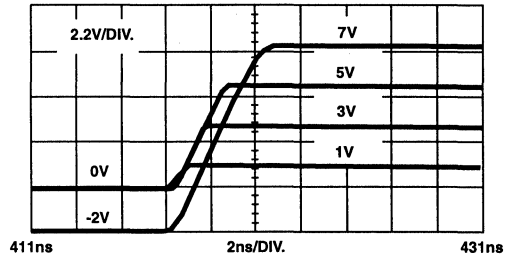

FIGURE 3. OUTPUT RESPONSE WITH VARIOUS V_{LOW} AND V_{HIGH} CONDITIONS

Basic ATE System Application

Figure 4 shows a pin driver in a typical per-pin ATE system. The pin driver works closely with the dual-level comparator and the active load. When the DUT pin acts as an input waiting for a series of digital signals, the pin driver becomes active with a logic "0" applied on the HiZ pin and provides

the DUT pin with digital signals. When the DUT pin acts as an output, the pin driver output will be in high-impedance mode (HiZ) with a logic "1" applied to the "HiZ" pin of the pin driver. During this high impedance mode the pin driver presents a capacitance of less than 5pF to the DUT. Special care has to be taken to match the impedance (to 50Ω) at the pin driver output to minimize reflections.

The dual level comparator detects the logic levels of the DUT pin when it acts as an output. The comparator has two threshold level inputs, V_{CH} and V_{CL}. The logic level information of DUT pin output is sent to the edge/window comparator through the dual level comparator. The edge/window comparator interprets this information in terms of corresponding transient performance in conjunction with the timing information. Thus it detects any possible failure transients.

The formatter sends a sequence of digital information to the pin driver which contains logic information over time. The active load is enabled when the DUT pin acts as an output. It simulates the load of the DUT pin by sinking or sourcing programmed current. Finally the sequencer controls the overall activities of the automatic testing.

Decoupling Circuit for Oscillation-Free Operation

To insure the oscillation-free operation in ATE or pulse generator applications, the pin driver needs an appropriate decoupling circuit on a printed circuit board which consists of chip capacitors and chip resistors. Figure 5 and Figure 6 refer to a proven decoupling circuit currently working in the lab and a 1X scale film of its associated PC board (metal level).

The control pins, D, D*, HiZ, and HiZ* are fed ECL signals through 50Ω micro-strip lines terminated with 50Ω for impedance matching since the input impedance at these pins is much higher than 50Ω. At the end of the micro-strip lines there is usually a high-speed pulse generator with an output impedance of 50Ω. A 50Ω micro-strip line is connected to each of the pins, D* and HiZ* through a 50Ω chip resistor to monitor the pulse signals.

The two input voltage pins, V_{HIGH} and V_{LOW}, need to be protected from any capacitively coupled AC noise. Normally this protection can be achieved by having a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this protection circuit the pin driver may oscillate due to signals fed back from the output through the PC board ground.

The power supply pins, V_{CC1}, V_{CC2}, V_{EE1}, and V_{EE2}, require decoupling chip capacitors of 470pF, 0.1μF, 10μF. Having decoupling capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through either V_{CC2} or V_{EE2} during transients.

The output of the pin driver is usually connected to the device-under-test (DUT) through 50Ω micro-strip line and coaxial cable which carries the signal to a high input impedance DUT pin.

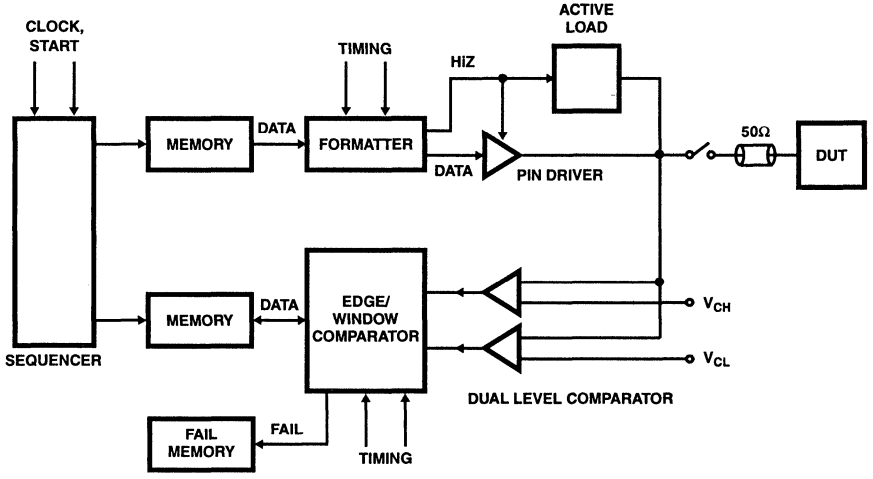

FIGURE 4. TYPICAL ATE SYSTEM

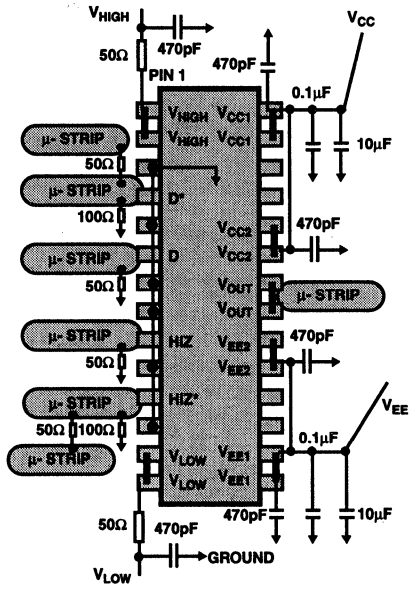

FIGURE 5. DECOUPLING CIRCUIT OF 28 LEAD SOIC HFA5250/ 5251 FOR OSCILLATION-FREE OPERATION

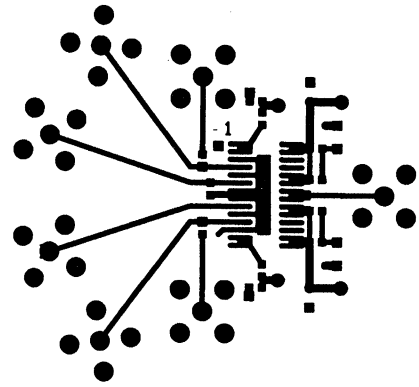

FIGURE 6. 1X FILM OF THE EVALUATION BOARD METAL

References

[1] Taewon Jung and Donald K. Whitney Jr., "A 500MHz ATE Pin Driver," Bipolar Circuits and Technology Meeting Proceedings, pp238-241, October 1992.

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APP NOTE

No. AN9315.1 November 1996

Harris Linear

RF Amplifier Design Using HFA3046, HFA3096, HFA3127, HFA3128 Transistor Arrays

Author: Sang-Gug Lee

Introduction

This application note is focused on exploiting the RF design capabilities of HFA3046/3096/3127/3128 transistor arrays. Detailed design procedures, using these transistor arrays, for a matched (800MHz to 2500MHz) high-gain low-noise amplifier and a 10MHz to 600MHz wideband feedback amplifier are described.

The HFA3046, HFA3096, HFA3127, HFA3128 transistor arrays are fabricated in a complementary bipolar bonded wafer silicon-on-insulator (SOI) technology, dubbed UHF-1 [1]. All four products make use of the same die, which has both NPN and PNP transistors on it. Figure 1 shows the pinouts of the four different products. Typical NPN and PNP transistor characteristics are shown in Table 1.

TABLE 1. UHF-1 DEVICE CHARACTERISTIC

PARAMETERS	NPN	PNP	UNITS
$BV_{CEO, MIN}$	8	8	V
$BV_{CBO, MIN}$	12	10	V
$BV_{EBO, MIN}$	5.5	4.5	V
I_{CBO}	0.1	0.1	nA
h_{FE}	70	40	
C_{CB}	500	600	fF
f_T	9	5.5	GHz
P_{1DB} (I_C = 10mA, V_{CE} = 5V, f_O = 1GHz)	7.6	6.2	dBm
IP3 (I_C = 10mA, V_{CE} = 5V, f_O = 1GHz)	17.6	16.2	dBm
NF (R_S = 50Ω, I_C = 5mA, V_{CE} = 3V, f_O = 1GHz)	3.5	3.0	dB

The SOI process has the advantage of lower DC and AC parasitic leakage currents as opposed to junction isolation, which leads to good isolation between transistors. Furthermore, an SOI process provides substantially lower collector to substrate capacitance, immunity to any possible latch-up between the devices, and superior radiation hardness.

The HFA3127 is used for the two stage matched (800MHz to 2500MHz) high-gain amplifier design, while the HFA3096 is used for the 10MHz to 600MHz wideband feedback amplifier.

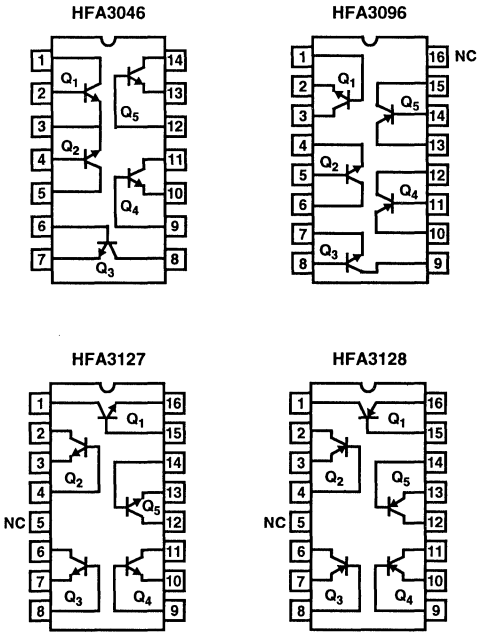

FIGURE 1. PINOUTS OF HFA3046/3096/3127/3128 SOIC PACKAGED TRANSISTOR ARRAYS

Circuit Design

High-Gain Low-Noise Amplifier

One important design requirement for an RF amplifier is the accurate control of input and output impedance levels. This is especially important if the amplifier is to interface with matched source and load impedances.

Based on S-parameter measurements, for a common-emitter configuration, transistors of HFA3127 exhibit a prematched condition on the input side over a wide range of frequencies. The package lead and bond wire inductances for these transistors make the input impedance close to 50Ω. For I_C = 5mA - 10mA, V_{CE} = 2V - 5V, the input VSWR of Q_2 and Q_5 was less than - 10dB for frequencies of 800MHz to 3000MHz. Furthermore, for these transistors, a good output match, output VSWR < -10dB

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for frequencies 300MHz to 3000MHz, could be accomplished through bypassing the collector with a 100Ω resistor. As the single stage amplifiers built with Q_2 and Q_5 both show good input and output matching, they can be cascaded for higher gain without requiring an impedance transforming network. Figure 2 shows the final two stage amplifier. The advantage of this circuit is its simplicity. This design does not use any tuning inductors or capacitors which would tend to increase the cost of the circuit. Furthermore, this circuit accomplishes higher gain by cascading two amplifier stages built with integrated transistors.

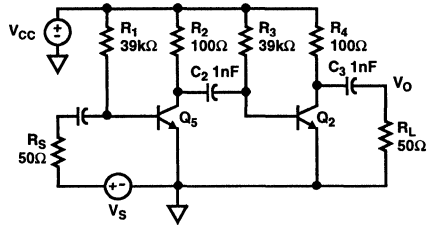

FIGURE 2. HIGH-GAIN LOW-NOISE AMPLIFIER REALIZED WITH HFA3127

Figure 3 shows the measured characteristics of the amplifier under two different bias conditions: V_{CC} = 3V, $I_{C2} = I_{C5}$ = 5mA; and V_{CC} = 5V, $I_{C2} = I_{C5}$ = 10mA. As can be seen from Figure 3, the input and output VSWR is less than -10dB for frequencies greater than 800MHz. The amplifier shows better performance at the expense of higher power dissipation (I_C = 10mA and V_{CC} = 5V) except the noise figure. For $I_{C2} = I_{C5}$ = 10mA, the amplifier gains are 18.7, 8.8, and 6.6dB at frequencies of 900MHz, 1800MHz, and 2200MHz, respectively.

From Figure 2, the noise figure of the whole circuit is mainly controlled by the noise characteristics of the transistor Q_5. As shown in Figure 3D, this high-gain amplifier demonstrates good noise performance. For $I_{C2} = I_{C5}$ = 5mA, the measured noise figure is 3.9dB at 900MHz, making this useful as a high-gain, low-noise amplifier.

The complete microstrip board layout is shown in Figure 4. A 0.031 inch thick FR-4 (G-10) glass epoxy board is used for the layout. The dielectric constant of the material is 4.7 at 1000MHz.

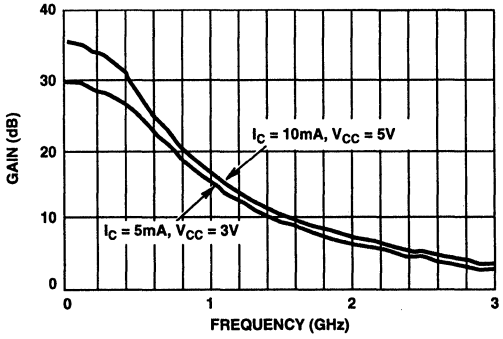

FIGURE 3A. GAIN

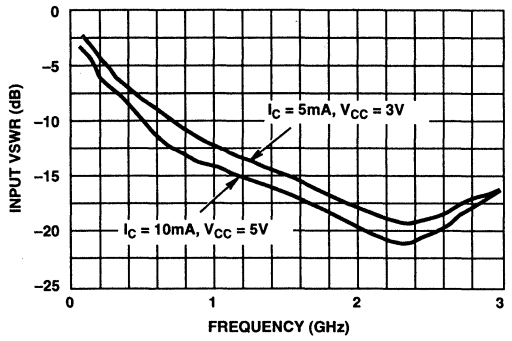

FIGURE 3B. INPUT VSWR

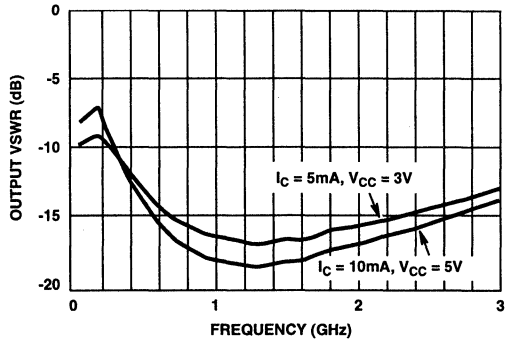

FIGURE 3C. OUTPUT VSWR

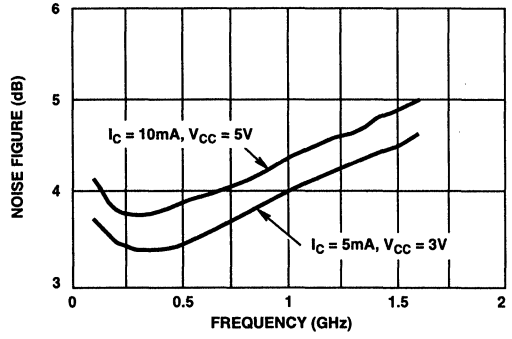

FIGURE 3D. NOISE

FIGURE 3. MEASURED CHARACTERISTICS OF THE HIGH GAIN LOW-NOISE AMPLIFIER

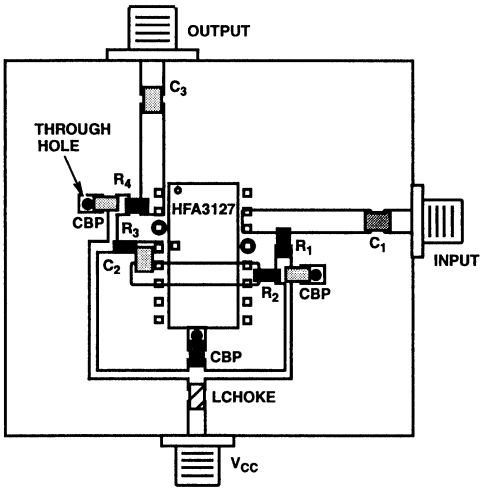

FIGURE 4. MICROSTRIP BOARD LAYOUT FOR THE HIGH-GAIN LOW-NOISE AMPLIFIER

The key rule for the circuit board layout is to make the physical length of the conductors as short as possible where the RF signal is involved. Although it seems obvious, it is easy to forget that the impedance looking into a microstrip line, that has load attached at the end, can be totally different from the attached load impedance depending on the length of the microstrip line and frequency. Outside the RF signal path, it does not matter.

At RF frequencies, the value of chip resistors, capacitors, and inductors should not be taken for granted. In general, the smaller the size of the component, the better the performance. However, it is important to evaluate the components before use. For the RF frequencies, these components can be evaluated easily using a network analyzer by mounting them as shown in Figure 5. The SMA connector itself contributes about 0.7pF of capacitance between the signal and ground terminals.

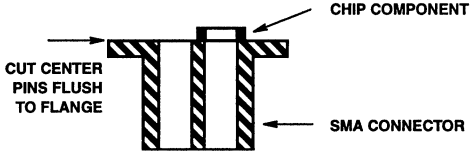

FIGURE 5. A CHIP COMPONENT MOUNTED ON AN SMA CONNECTOR

Wideband Amplifier

A well known simple amplifier configuration which achieves flat gain and broadband matching without losing excessive signal power is shown in Figure 6. The simultaneous use of both shunt and series feedback gives rise to broadband resistive input and output impedances [2, 3].

Figure 7 shows a similar version of the double feedback wideband amplifier circuit realized with the HFA3096. This design takes advantage of the PNP transistors (Q_4 and Q_5) available on the HFA3096, to bias amplifying transistor Q_2 for good temperature stability.

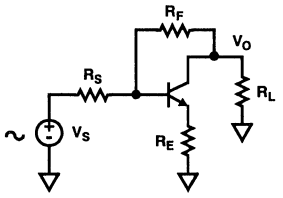

FIGURE 6. SINGLE STAGE SHUNT AND SERIES FEEDBACK CIRCUIT

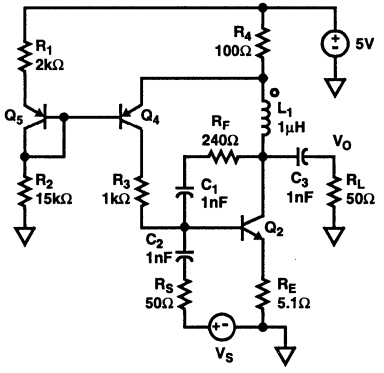

FIGURE 7. WIDEBAND AMPLIFIER REALIZED WITH HFA3096

The frequency response of the wideband amplifier is shown in Figure 8. As can be seen from Figure 8, the amplifier shows 10dB of flat gain with 600MHz bandwidth.The input and output matching is very good over the range of frequency where gains are flat. The low frequency performance is limited by the 1000pF capacitor.

The microstrip board layout for the wideband amplifier is shown in Figure 9. A 0.031 inch thick FR-4 (G-10) glass epoxy board is used for the layout.

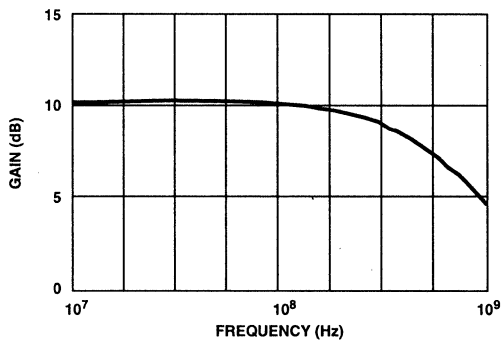

FIGURE 8A. GAIN

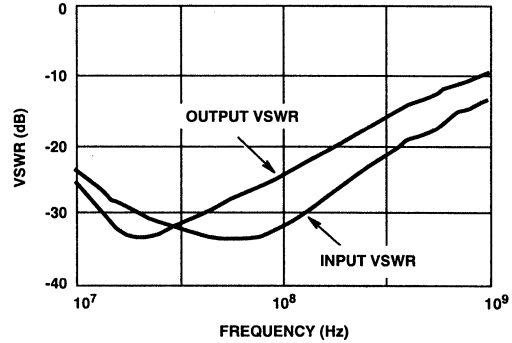

FIGURE 8B. INPUT-OUTPUT VSWR

FIGURE 8. MEASURED CHARACTERISTICS OF THE WIDEBAND AMPLIFIER

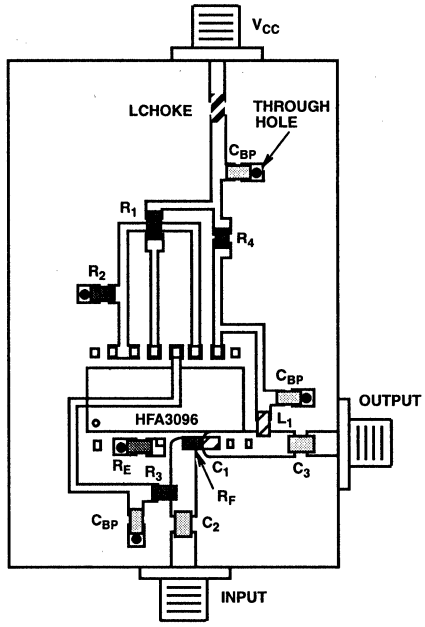

FIGURE 9. MICROSTRIP BOARD LAYOUT FOR THE WIDEBAND AMPLIFIER

Summary

A detailed process of designing a high-gain low-noise and a wideband amplifier using the Harris UHF transistor arrays is summarized.

A two-stage, high-gain, low-noise amplifier built with the HFA3127 demonstrates 50Ω input and output impedance over a wide frequency range of 800MHz to 2500MHz without the use of external matching networks. The gain at 900MHz is in excess of 17dB with a noise figure of 3.9dB.

A wideband amplifier built with the HFA3096 demonstrates excellent input and output matching with 10dB of constant gain. The -3dB bandwidth of this amplifier is 600MHz. PNP transistors available on the HFA3096 are used for temperature stable biasing of the amplifying transistor.

References

[1] C. Davis, et al, "UHF-1: A High Speed Complementary Bipolar Analog Process on SOI," Proceeding of BCTM 92, pp260-263, Oct. 1992.

[2] J. B. Couglin, et al, "A Monolithic Silicon wideband Amplifier from DC to 1 GHz," IEEE J. Solid-State Circuits, vol. SC-8, pp414-419, Dec. 1973.

[3] R. G. Meyer, et al, "A wideband Ultralinear Amplifier from 3 to 300 MHz," IEEE J. Solid-State Circuits, vol. SC-9, pp167-175, Aug. 1974.

Harris Semiconductor

APPNOTE

No. AN9317.1 November 1996

Harris Linear

Micropower Clock Oscillator and Op Amps Provide System Control for Battery Operated Circuits (HA7210)

Author: Al Little and James Ho

The HA7210 low power oscillator is ideal for battery powered circuits that require a precision clock. It operates well from a single 3V to 5V supply, uses extremely low current, and produces a clock output that is very stable over temperature and supply voltage. In addition, it requires only an external crystal and can operate from under 32kHz to over 10MHz.

This application note shows how the HA7210 can be used with a quad CMOS op amp to make a control circuit that will automatically switch a battery-powered digital system into micropower "sleep mode" when not in use and trigger the system on again when an external event (sound, pressure, etc.) is detected. This function is extremely useful for applications like remote metering, where a battery-powered system may need to record occasional events yet remain in a power down state most of the time.

This control circuit can be configured to turn on with an AC or DC coupled event sensor and turn off using either a preset time delay or an external digital system command. When triggered into the power-up mode, it supplies a precision system clock, a buffered analog ground reference and a scaling signal amplifier for an A/D converter. In the power-down mode, it draws less than 50µA of standby current.

Circuit Operation

As shown in Figure 1, the control circuit operates from a single 3V to 5V battery and uses only a quad CMOS op amp (ICL7642) and a HA7210 low power oscillator chip. Two Power-Down Reset options are available: one for a preset time delay after turn-on, and another for external digital command as explained in the following text.

R_1 and R_2 create an analog signal ground reference voltage, V_{REF}, at 1/2 of the battery voltage. C_2 is used to filter noise from this high impedance point. The analog reference voltage is then buffered by IC1A and output to the other three amplifiers.

Amplifier B is used as a high-pass filter and amplifier such that a fast edge (like a sudden noise into a microphone) will produce a large positive swing at the output. Diode D_1 prevents the output from moving very much below the analog reference voltage. C_1 can be determined experimentally depending on the application, sensor type, and sensitivity required.

Amplifier C is used as a comparator and latch. The inverting terminal is nominally at the analog reference, V_{REF}, but the non-inverting terminal is lower than V_{REF} due to the hysteresis of R_5. In the absence of a microphone/sensor signal, the output of amplifier B is also at V_{REF}, so that $V_{REF}(R_5/(R_4 + R_5))$ appears at the non-inverting input of amplifier C.

When the output of amplifier B produces a voltage at the non-inverting terminal of amplifier C higher than V_{REF}, the output of C latches into the high state. This state cannot be changed by any condition at the input of IC1B due to the hysteresis provided by R_5. Because the output stage of amplifier C is CMOS, it can drive a light load nearly to the positive supply rail.

Voltage from the output of amplifier C is provided to the supply and ENable pins of the HA7210 low power oscillator. When this happens, the oscillator turns on and provides a clock output to the rest of the system. C_3 is used as a bypass capacitor for the supply pin. If faster oscillator turn-on is required, the HA7210 supply pin (pin 1) may be tied directly to the battery and the output of amplifier C used to enable the HA7210. In this case, the oscillator will draw some quiescent current when not in use, but significantly lower than when enabled. Capacitance at the output of the HA7210 should be minimized to keep the active supply current as low as possible.

As shown, amplifier D can be used as a scaling amplifier for a system A/D converter. R_7 and R_8 are used to scale the gain of the amplifier ($G = 1 + R_8/R_7$). The input of the amplifier is extremely high impedance, so that any type of high impedance sensor may be used.

Resetting the System

To put the system back into "sleep mode", two options are available. The digital system can send a logic high state to the Reset input, forcing the IC1C comparator/latch to reset to the low state. Alternatively, if desired, an auto-reset RC timer (shown in the dotted lines) will cause the circuit to automatically reset after a preset time interval. This time is determined by the time it takes for the capacitor at the inverting terminal to charge higher than the voltage at the non-inverting terminal of IC1C.

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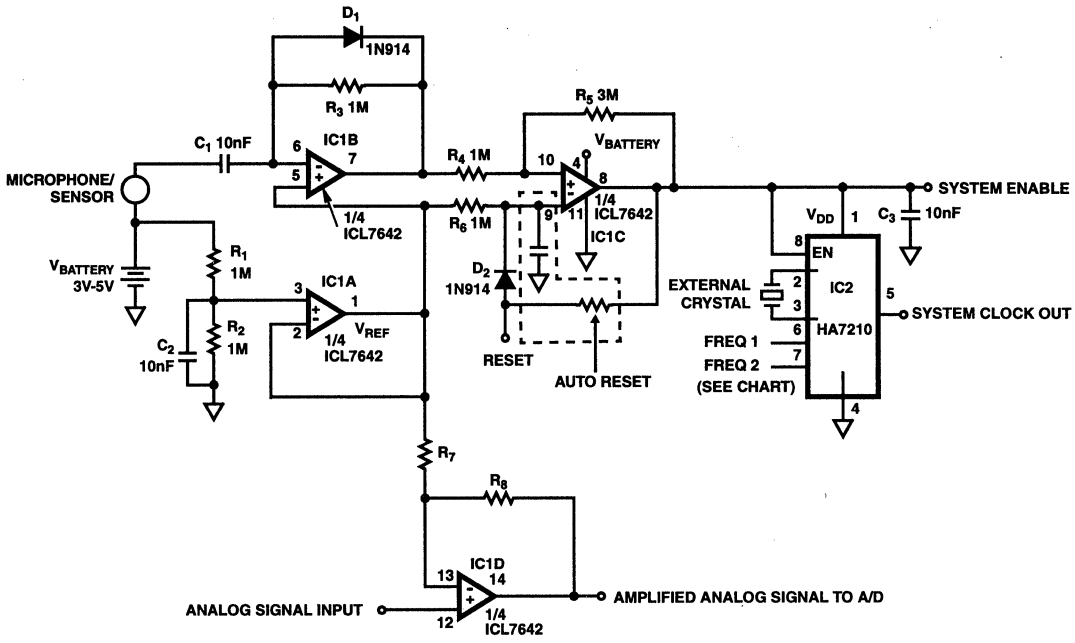

NOTE: Provides Sleep Mode, Power-up Trigger, Optional Auto-reset, Scaling Amp for A/D, Precision System Clock Oscillator, and Analog Ground Reference

FIGURE 1. 2-CHIP MICROPOWER CONTROL CIRCUIT OPERATES FROM 3V BATTERY

TABLE 1. HA7210 OSCILLATOR CONTROL INPUTS

ENABLE	FREQ 1	FREQ 2	OUTPUT RANGE
1	1	1	10kHz to 100kHz
1	1	0	100kHz to 1MHz
1	0	1	1MHz to 5MHz
1	0	0	5MHz to 10MHz+
0	X	X	High Impedance

APPNOTE

No. AN9334.1 October 1996

Harris Linear

Improving Start-up Time at 32kHz for the HA7210 Low Power Crystal Oscillator

Author: Robert Rood

The HA7210 is a very low power crystal-controlled oscillator that can be programmed to operate between 10kHz and 10MHz. In the lowest frequency range setting (FREQ 1 = 1, FREQ 2 = 1), at 32kHz with a 5V supply and a 40pF load, the HA7210 will draw a mere 10µA. In this range (10kHz to 100kHz), the low power consumption may result in extended oscillator start-up time. In higher frequency ranges, power consumption gradually increases and start-up time is not an issue. Several approaches to address low frequency start-up time will be presented.

The first approach is to use the Enable/Disable Mode Pin. This pin, when pulled low, will switch the output to a high impedance state while an internal inverter continues to drive the crystal in normal oscillation. This will result in a power savings because very often a majority of the power dissipation is used to drive the output load. In the disabled mode the HA7210 will draw only 5µA of standby current as compared to 10µA above. This small amount of standby current gives the benefit of instant start-up of a reliable and stable clock. The Enable Time of the HA7210 is typically 800ns.

For applications where the voltage supply is removed from the circuit or standby mode is not desired, the time from power being applied until a stable square wave is generated can be unexpectedly long. It should be noted that 32kHz crystal parameters vary significantly from vendor to vendor and can greatly affect the HA7210 (or any Pierce Oscillator) start-up characteristic. Of particular importance is the Effective Series Resistance (ESR) of the crystal, with lower ESR generally providing faster start-up times (32kHz crystals with ESR greater than 50kΩ should be avoided). Using the circuit in Figure 1 the start-up characteristic of a 32.768kHz crystal, set in the recommended lowest frequency range (FREQ 1 = 1, FREQ 2 = 1) has a delay of 1.9s as shown in Figure 2.

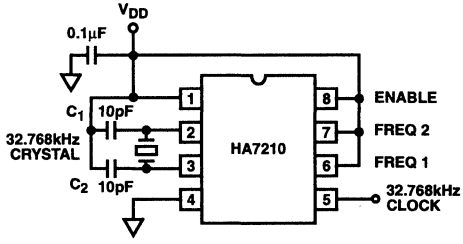

FIGURE 1. TYPICAL APPLICATION CIRCUIT

FREQUENCY SELECTION TRUTH TABLE

ENABLE	FREQ 1	FREQ 2	OUTPUT RANGE
1	1	1	10kHz to 100kHz
1	1	0	100kHz to 1MHz
1	0	1	1MHz to 5MHz
1	0	0	5MHz to 10MHz
0	X	X	High-Z

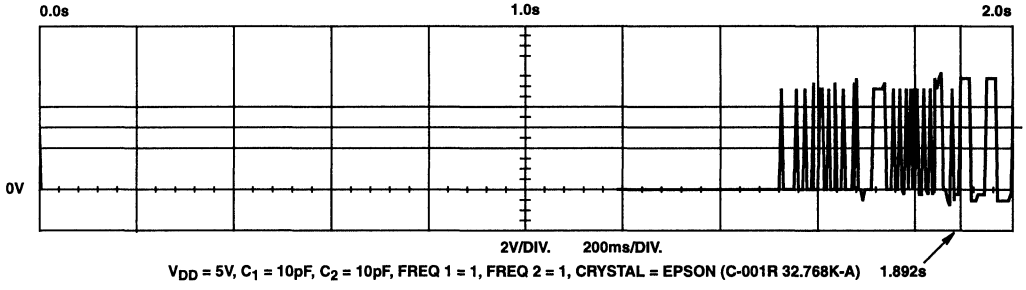

FIGURE 2. START-UP CHARACTERISTIC AT 32kHz WITH FREQ 1 = 1 AND FREQ 2 = 1

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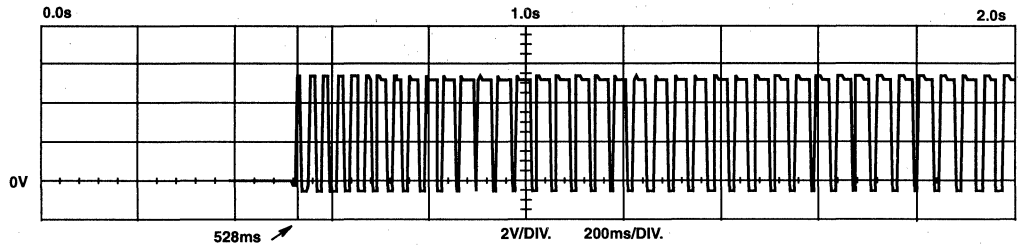

V_{DD} = 5V, C_1 = 10pF, C_2 = 10pF, FREQ 1 = 1, FREQ 2 = 0, CRYSTAL = EPSON (C-001R 32.768K-A)

FIGURE 3. START-UP CHARACTERISTIC AT 32kHz WITH FREQ 1 = 1 AND FREQ 2 = 0

The start-up time can be improved by switching to the next higher frequency range setting, where FREQ 1 = 1 and FREQ 2 = 0. In this setting the voltage that is internally applied to the oscillating inverter increases from 1.4V to 2.2V providing more power and higher transconductance. This increased power comes at the expense of increased supply current. For a 32kHz crystal, with V_{DD} = 5V and a 40pF load the FREQ 1 = 1, FREQ 2 = 0 setting will draw 30MA as compared to 10MA for the FREQ 1 = 1, FREQ 2 = 1 range setting. Another concern when using the next higher range is that the internal 15pF crystal loading capacitors are disconnected. This means that the user must provide external crystal loading capacitors for the crystal to start properly in the higher range. The minimum values for C_1 and C_2 to provide reliable start-up was found to be 10pF each. The start-up time in the FREQ 1 = 1, FREQ 2 = 0 mode is shown in Figure 3 at 528ms, significantly faster than the FREQ 1 = 1, FREQ 2 = 1 setting.

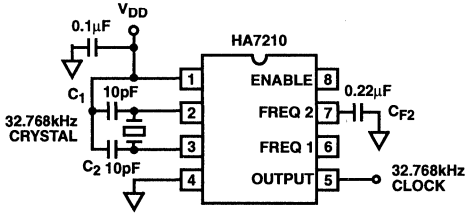

FIGURE 4. FAST START-UP AT 32kHz WITH NO SUPPLY CURRENT PENALTY

How can the benefits of faster start-up be gained without the penalty of increased supply current? A solution to this problem is provided with the addition of a single capacitor C_{F2} as shown in Figure 4.

The digital inputs (ENABLE, FREQ 1, FREQ 2) provide internal pull-up devices. These P-Channel devices provide 0.4µA of current to insure that an input will go to the "1" state if left open. This pull-up current is used to charge a 0.22µF capacitor (C_{F2}) connected to the FREQ 2 pin. At power-up C_{F2} has zero charge and holds FREQ 2 "low", (FREQ 1 = 1, FREQ 2 = 0) so that the HA7210 will give a fast start-up. Then the 0.4µA pull-up current will slowly charge C_{F2} until it reaches a "high" state (FREQ 1 = 1, FREQ 2 = 1) and the part draws lower supply current. The FREQ 2 pin must be held low until the oscillation has fully started to insure a start-up time improvement. The digital input threshold is about 1.5V, providing a delay determined by:

$$i = C\frac{dv}{dt} \qquad dt = \frac{(0.22\mu F)(1.5V)}{0.4\mu A} = 0.825s$$

The results are shown in Figure 5. Notice that CH 2 doesn't go all the way to 5V as expected. This is due to the 10MΩ scope probe loading the 0.4µA current source. This probe loading also causes CH 2 (FREQ 2 pin) to have an RC shape rather that the expected linear trace.

In summary, start-up time is an important consideration in the design and crystal selection for low frequency crystal oscillators. This Application Note describes several alternatives to improve start-up time utilizing unique features of the HA7210 while taking advantage of its extremely low supply current.

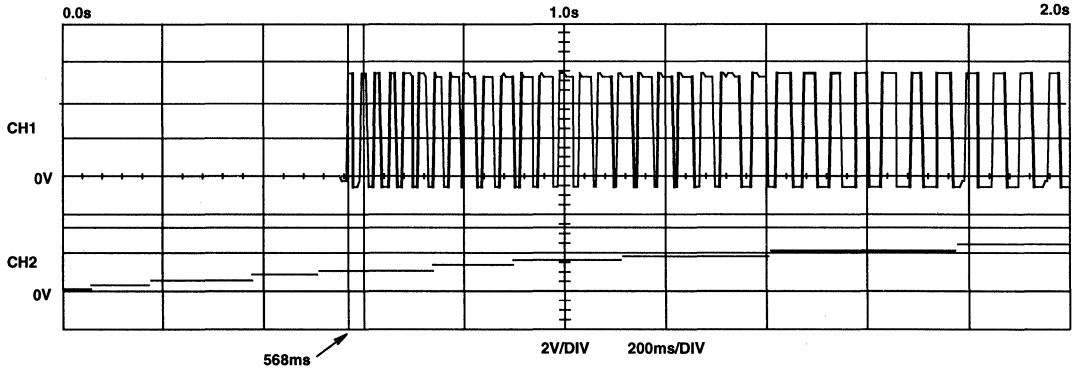

FIGURE 5. START-UP CHARACTERISTIC AT 32kHz WITH SPEED-UP CIRCUIT

Harris Semiconductor

APPNOTE

No. AN9415.3 November 1996

Harris Linear

Feedback, Op Amps and Compensation

Ron Mancini

Introduction

There are many benefits [1] which result from the use of feedback in electronic circuits, but the drawbacks are the increased complexity of the calculations and the opportunity for the resulting circuit to ring or oscillate. This paper employs graphical techniques to simplify stability calculations, thus enabling the designer to achieve a stable, well behaved circuit which meets all reasonable performance criteria. Now the designer can obtain the advantages of feedback without worrying about ringing or oscillation.

Development of the General Feedback Equation

Referring to the block diagram shown in Figure 1, Equation 1, Equation 2 and Equation 3 can be written by inspection if it is assumed that there are no loading concerns between the blocks. The no loading assumption is implicit in all block diagram calculations, and this requires that the output impedance of a block be much lower than the input impedance of the block it is driving. This is usually true by one or two orders of magnitude. Algebraic manipulation of Equation 1, Equation 2 and Equation 3 yield Equation 4 and Equation 5 which are the defining equations for a feedback system.

$$V_O = EA \quad \text{(EQ. 1)}$$

$$E = V_I - \beta V_O \quad \text{(EQ. 2)}$$

$$E = V_O/A \quad \text{(EQ. 3)}$$

$$V_O/V_I = A/(1 + A\beta) \quad \text{(EQ. 4)}$$

$$E/V_I = 1/(1 + A\beta) \quad \text{(EQ. 5)}$$

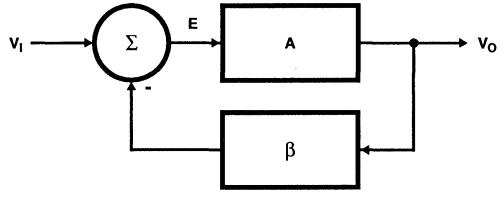

FIGURE 1. FEEDBACK SYSTEM BLOCK DIAGRAM

The parameter A, which usually includes the amplifier and thus contains active elements, is called the direct gain in this analysis. The parameter β, which normally contains only passive components, is called the feedback factor. Notice that in Equation 4 as the value of A approaches infinity, the quantity Aβ, which is called the loop gain, becomes much larger than one; thus, Equation 4 can be approximated by Equation 6. V_O/V_I is called the closed loop gain, and since the direct gain, or the amplifier response, is not included, the equation for the closed loop gain it is independent of amplifier parameter changes. This is the major benefit of feedback circuits.

$$V_O/V_I = 1/\beta \text{ for } A\beta >> 1 \quad \text{(EQ. 6)}$$

Equation 4 is adequate to describe the stability of any feedback circuit because all feedback circuits can be reduced to the this form through block diagram reduction techniques [2]. The stability of the feedback circuit is determined by setting the denominator of Equation 4 equal to zero.

$$1 + A\beta = 0 \quad \text{(EQ. 7)}$$

$$A\beta = -1 = |1| \angle -180 \quad \text{(EQ. 8)}$$

Referring to Equation 4 and Equation 8, it is observed that if the magnitude of the loop gain, Aβ, can achieve one while the phase equals -180 degrees, the closed loop gain becomes infinity because of division by zero. Since this state is unstable, the circuit will oscillate, and it will oscillate at the frequency where the phase shift equals to -180 degrees. If the loop gain at the frequency of oscillation is slightly greater than one it will be reduced to one by the reduction in gain suffered by the active elements as they approach the limits of saturation, but if the value of Aβ is much greater than one, gross nonlinearities can occur and the circuit may then cycle between saturation limits. Preventing instability is the essence of feedback circuit design, thus this topic will be touched lightly here and covered in detail later. A good starting point for discussing stability is finding an easy method to calculate it. Figure 2 shows that the loop gain, Aβ, can be calculated from a block diagram by opening current inputs, shorting voltage inputs, breaking the loop and calculating the response to a test input signal.

$$V_{TO}/V_{TI} = A\beta \quad \text{(EQ. 9)}$$

The block diagram techniques can be applied to op amps thus reducing the stability analysis to a simple task. The schematic for a non-inverting amplifier is shown in Figure 3, and the block diagram equivalent is shown in Figure 4. Equation 10 and Equation 11 are combined to yield Equation 12 which describes the block diagram shown in Figure 4A, while block diagram transformations [3] are employed to get to Figure 4B.

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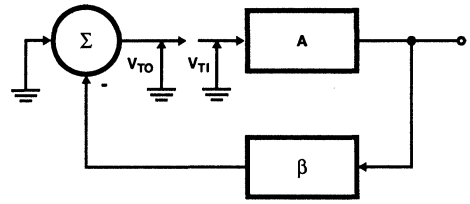

FIGURE 2. BLOCK DIAGRAM FOR COMPUTING THE LOOP GAIN

$$V_O = a(V_I - V_B) \quad \text{(EQ. 10)}$$

$$V_B = V_O Z_1/(Z_1 + Z_2),\ I_B = 0 \quad \text{(EQ. 11)}$$

$$V_O = aV_I - aZ_1V_O/(Z_1 + Z_2) \quad \text{(EQ. 12)}$$

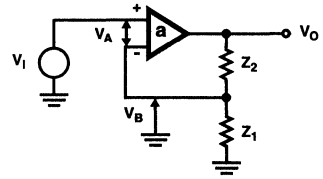

FIGURE 3. NON-INVERTING CIRCUIT

The block diagram shown in Figure 4A is written by inspection of Equation 12. The block diagram shown in Figure 4B is derived from Figure 4A by block diagram manipulations. Equation 13 is derived from Equation 12 by algebraic manipulation, or it can be written by inspection of Figure 4B because the system is shown in standard form.

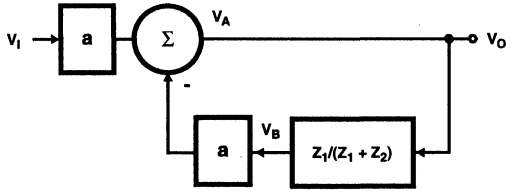

FIGURE 4A. BLOCK DIAGRAM AS WRITTEN FROM EQUATION 12

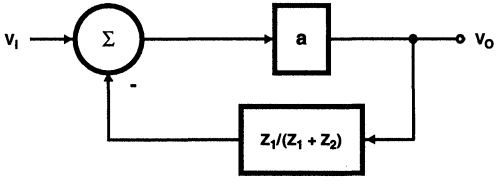

FIGURE 4B. AFTER BLOCK DIAGRAM MANIPULATION

FIGURE 4. BLOCK DIAGRAM OF THE NON-INVERTING OP AMP AS SHOWN IN EQUATION 12

$$V_O/V_I = a/(1 + aZ_1 / (Z_1 + Z_2)) \quad \text{(EQ. 13)}$$

The loop gain, Aβ, is equal to $aZ_1/(Z_1+Z_2)$, the closed loop gain, 1/β, is equal to $(Z_1+Z_2)/Z_1$, and the direct gain, A, is equal to the op amp gain, a. The loop gain can be determined from Figure 4B by inspection, or if the system block is not available the loop gain can be obtained directly from the amplifier schematic as shown in Figure 5. First set voltage sources to zero by grounding them, then open current sources, break the feedback loop at any convenient place and then calculate the loop gain. Remember, the output impedance of the op amp must be much lower than the feedback impedance so that block diagram techniques can be used. The test input is V_{TI}, and it is amplified by the op amp gain, a. The op amp output, aV_{TI} is divided by β before it is fed back as V_{TO}.

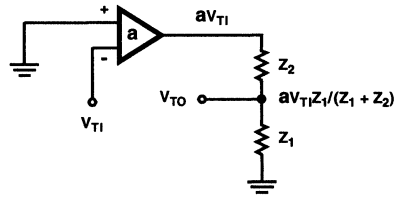

FIGURE 5. NON-INVERTING OP AMP WITH INPUT GROUNDED AND FEEDBACK LOOP BROKEN

$$\frac{V_{TO}}{V_{TI}} = \frac{aZ_1}{Z_1 + Z_2} = A\beta \quad \text{(EQ. 14)}$$

Referring to the inverting op amp configuration shown in Figure 6, the analysis will be performed by working from the amplifier circuit to the block diagram. The closed loop gain equations are derived in references one and six as well as most electronic text books. The closed loop gain which is equal to 1/β is known to be $-Z_2/Z_1$; thus, β is calculated as Z_1/Z_2 with the minus sign indicating a negative input. Referring to Figure 6, if V_I is set to zero and the loop is broken at the negative input to the op amp the circuit is identical to that shown in Figure 5.

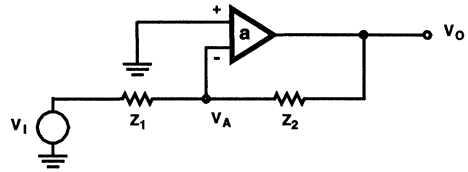

FIGURE 6. INVERTING OP AMP SCHEMATIC

An examination of Figure 5 and Figure 6 reveals that the loop gain, Aβ, is identical for both the inverting and non-inverting circuit configurations. The loop gain is the only parameter that determines stability, and it is not a function of the location of the inputs. Hence the loop gain for the inverting op amp is given to us by Equation 14. Now that Aβ and 1/β are both known, A can be determined by multiplication to be $aZ_2/(Z_1 + Z_2)$. Since the direct gain and the loop gain are both known Figure 7 can be constructed from these quantities.

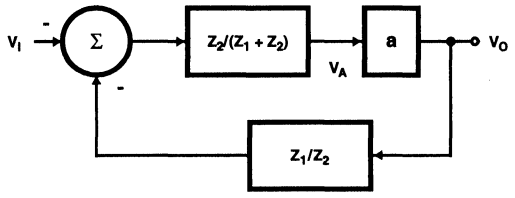

FIGURE 7. BLOCK DIAGRAM OF THE INVERTING OP AMP

Equation 15, which is the closed loop gain equation for an inverting op amp can be written directly from Figure 7. As (a) approaches infinity in Equation 15, the closed loop gain approaches $-Z_2/Z_1$.

$$\frac{V_O}{V_I} = -\frac{\frac{aZ_2}{Z_1+Z_2}}{1+\frac{aZ_1}{Z_1+Z_2}} \qquad \text{(EQ. 15)}$$

The closed loop gain for the non-inverting circuit, $V_O/V_I = (Z_1 + Z_2)/Z_1$, is different from the closed loop gain for the inverting circuit, $V_O/V_I = -Z_2/Z_1$. It will always be the case that the loop gain, hence the stability, is independent of the location of the inputs, but the closed loop performance is highly dependent on the placement of the input. Many circuits take advantage of this phenomena to gain better performance as will be shown in the benefits section.

$A_{NON\text{-}INV} = a$; which is $\neq$ to $A_{INV} = aZ_2/(Z_1 + Z_2)$ (EQ. 16)

Comparing the block diagrams of the non-inverting and inverting circuits reveals that their direct gains are different, and this explains why there are some slight performance differences between the configurations. The non-inverting circuit with the higher direct gain has less closed loop error; at a closed loop gain of 2 for both circuits the non-inverting circuit has a 3.5dB more loop gain. The inverting circuit is more stable for the same magnitude of closed loop gain; i.e., for a closed loop gain of 2, $A\beta_{INV} = 0.33a$ and $A\beta_{NON\text{-}INV} = 0.5a$. Normally these differences are minor, but they are pointed out because they may be taken advantage of or they can cause very subtle problems in unique situations.

There are many other op amp circuit configurations, but they will all reduce to these two basic forms; each of which is a variation of the basic feedback circuit shown in Figure 1. Letting Z_1 and or Z_2 equal various combinations of RLCs will give different closed loop performance, but the analysis techniques remain the same. More complicated circuit configurations can all be reduced to these simple circuits through block diagram reduction techniques and superposition.

Benefits of Feedback

The tolerances and drift coefficients of passive components are much less than those associated with active components. If the circuit transfer function can be made to be dependent only on the passive component parameters it will be a much more stable circuit; feedback accomplishes this through the direct gain as shown here. Differentiating the closed loop Equation 4, with respect to the direct gain yields Equations 17 and Equation 18 shown below. Notice that the percentage change in the closed loop gain is the percentage change in the direct gain divided by the loop gain. Thus for very high loop gains the initial accuracy and drift will be a function of the passive components rather than of the direct or amplifier gain. Although the feedback reduces the gain errors, other amplifier errors such as input voltage offset are not affected by the feedback because they occur as an input rather than within the feedback loop.

$$\frac{dV_O/V_I}{dA} = \frac{1}{(1+A\beta)^2} = \frac{1}{(1+A\beta)}\frac{V_O/V_I}{A} \qquad \text{(EQ. 17)}$$

$$\frac{dV_O/V_I}{V_O/V_I} = \frac{dA}{A}\frac{1}{(1+A\beta)} \qquad \text{(EQ. 18)}$$

All amplifiers have noise and distortion characteristics associated with them, and low noise or low distortion amplifiers command a premium price. Very often feedback can be used at no cost increase to reduce the effects of distortion and noise. Both closed loop and open loop systems are shown in Figure 8 and Figure 9; notice that both systems have the same number of components except for the passive feedback elements.

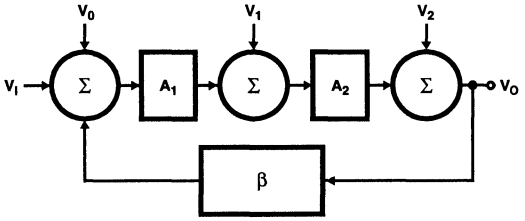

FIGURE 8. CLOSED LOOP SYSTEM

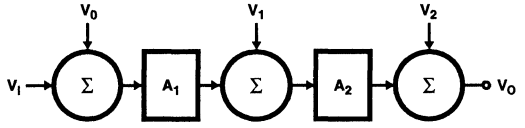

FIGURE 9. OPEN LOOP SYSTEM

Equation 19 and Equation 20 are derived from the closed loop and open loop systems shown in Figure 8 and Figure 9. If Equation 19 is rewritten as shown in Equation 21 it is obvious that Equation 22 results when the quantity A_1A_2 approaches infinity as it will in an ideal system.

$$V_O = \frac{A_1A_2(V_I+V_0)}{1+A_1A_2\beta} + \frac{A_2V_1}{1+A_1A_2\beta} + \frac{V_2}{1+A_1A_2\beta} \qquad \text{(EQ. 19)}$$

$$V_O = A_1A_2(V_I+V_0) + A_2V_1 + V_2 \qquad \text{(EQ. 20)}$$

$$V_O = \frac{V_I+V_0}{1/(A_1A_2)+\beta} + \frac{V_1/A_1}{1/(A_1A_2)+\beta} + \frac{V_2/A_1A_2}{1/(A_1A_2)+\beta} \qquad \text{(EQ. 21)}$$

$$V_O = \frac{V_I+V_0}{\beta} + \frac{V_1/A_1}{\beta} \quad \text{For } A_1A_2 \text{ approaching infinity} \qquad \text{(EQ. 22)}$$

Now let V_0 and V_1 represent the amplifier's internal noise referred to the input, and let V_2 represent the noise from the any other system components. Notice from Equation 22 that in the closed loop system V_2 has disappeared, V_1 is decreased proportional to the gain A_1 and that the input noise has only been multiplied by the closed loop gain, $1/\beta$. Conversely, Equation 20 indicates that in the open loop system the input noise has been multiplied by A_1A_2 (which would be equivalent to the closed loop gain), that V_1 is multiplied by A_2 and that V_2 is present. The feedback in the closed loop system has dramatically reduced the noise from the sources which follow the amplifier A_1 so this can become a big design advantage. In the closed loop system the amplifier A_1 should be selected for it's excellent noise performance, but the amplifier A_2 can be selected based on some other criteria such as cost. This option is not available in the open loop system.

Very often when driving low impedances like speakers, the output amplifiers are driven as close to the power supply rails as possible to obtain the maximum dynamic range. One result of this practice is that some distortion of the signal occurs as active device parameters are driven so that they become nonlinear. This and most other sources of distortion usually occur in the output stages of the amplifier. Because the distortion occurs at the output it can be represented by V_2 in Equation 19, and this quantity goes to zero as the direct gain approaches infinity, so it is essentially eliminated by feedback. The connection from the speaker driver output to the preamplifier input in audio amplifiers is there to provide the feedback which reduces the amplifier's distortion when the amplifier is driven to its limits. Some amplifiers such as guitar amplifiers purposely introduce distortion into the sound, so open loop amplifiers are used in these cases, but closed loop amplifiers are usually employed in high fidelity applications.

If the noise source, V_1, is set to zero in Equation 22, then the amplifier input noise represented by V_0 is multiplied by the closed loop gain $1/\beta$. There is a method to further reduce the effects of V_0 by using frequency discrimination methods. If V_0 is examined as a function of frequency, it will be noticed that the noise is made up of many different frequency components, see Figure 10.

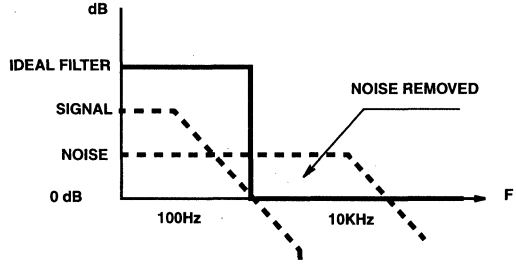

FIGURE 10. INSERTING AN IDEAL FILTER IN THE TRANSFER FUNCTION REDUCES NOISE

The signal of interest has a finite bandwidth, and if the noise bandwidth is larger than the signal bandwidth, the noise can be reduced by making the loop gain a function of frequency. Assuming that the noise bandwidth is 10KHz and that the signal bandwidth is 100Hz, the noise beyond 100Hz can be reduced to a minimum if $1/\beta$ is reduced to zero beyond 100Hz. One method available to accomplish this bandwidth reduction is through the ideal filter inserted in the closed loop, as shown in Figure 10. This filter can be approximated with passive components.

The input and output impedance of the closed loop circuit can be controlled by the amount of feedback and by the circuit configuration [4]. Through the use of feedback it is possible for the same amplifier IC to appear to have an output impedance approaching zero or approaching infinity, depending on the circuit configuration employed.

Another interesting aspect of feedback systems is that if a function is put in the feedback loop, in a manner similar to the feedback factor, β, the inverse function will appear at the output.

Graphical Representation of the Feedback Equation

The mathematical manipulations required to analyze a feedback circuit are complicated because they involve multiplication and division; H. W. Bode [5] developed a technique called a Bode plot which simplifies the analysis through the use of graphical techniques. The Bode equations are log equations which take the form of $20LOG(F(t)) = 20LOG(|F(t)|)$ + phase angle. Since these are log equations, the terms which were multiplied and divided can be now added and subtracted; thus, they can easily be solved graphically as will be shown. The transfer function for the integrator shown in Figure 11 is given in Equation 23.

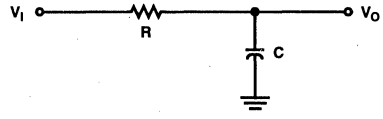

FIGURE 11. INTEGRATOR CIRCUIT

$$\frac{V_O}{V_I} = \frac{1}{(1 + RCs)} \qquad \text{(EQ. 23)}$$

Where $s = j\omega$ and $j = \sqrt{(-1)}$

The magnitude of the transfer function is given by the equation $|V_O/V_I| = 1/\sqrt{(1+(RC\omega)2)}$. The approximate magnitude or $|V_O/V_I| = 1$ when $\omega = 0.1/RC$, $|V_O/V_I| = 0.707$ when $\omega = 1/RC$ and $|V_O/V_I| = 0.1$ when $\omega = 10/RC$. These values are plotted in Figure 12 using straight line approximations.

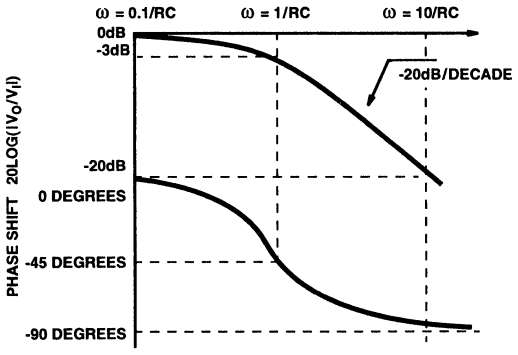

FIGURE 12. BODE PLOT OF INTEGRATING CIRCUIT TRANSFER FUNCTION

The downward slope of the amplitude curve in Figure 12 is -20dB/decade, and the point at which the slope changes, at $\omega = 1/RC$, is termed the breakpoint. Reading the curve, it can be seen that gain initially is one, 0dB, at very low frequencies, falling off to 0.707, -3dB, at the break frequency and decreases at a rate of -20dB/decade for higher frequencies. The phase shift for the integrator is given in Equation 24 and plotted in Figure 12. Notice that the phase shift is -45 degrees at the breakpoint where $\omega = 1/RC$.

$$\phi = -\text{tangent}^{-1}\,(1/\omega RC) \qquad \text{(EQ. 24)}$$

When the breakpoint occurs in the denominator, its slope is negative and is called a pole. Conversely, when the breakpoint occurs in the numerator, its slope is positive and it is called a zero.

The band reject circuit shown in Figure 13 has two poles, two zeros and a DC gain. Each pole and zero is plotted separately in Figure 14. The DC gain component is plotted as a straight line at -6dB because it is frequency independent. The two zeros in the numerator both occur at $\omega = 1/RC$; thus they are plotted on top of each other, and this results in a positive sloped line rising at 40dB/decade. The two poles in the denominator occur at $\omega = 0.44/RC$ and $\omega = 4.56/RC$, and they are each plotted with a negative slope of -20dB/decade.

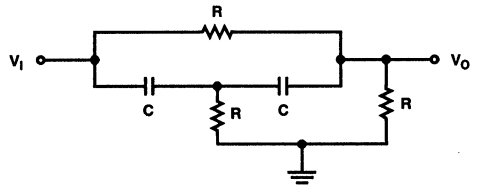

FIGURE 13. BAND REJECT FILTER CIRCUIT

$$\frac{V_O}{V_I} = \frac{(1 + RCs)(1 + RCs)}{2(1 + RCs/0.44)(1 + RCs/4.56)} \qquad \text{(EQ. 25)}$$

Where $s = j\omega$.

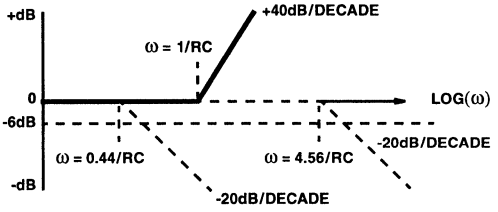

FIGURE 14. BODE PLOT OF THE INDIVIDUAL COMPONENTS OF THE BAND REJECT FILTER

Each of the separate Bode plots shown in Figure 14 are combined into one composite plot in Figure 15. The phase plots are treated much like the amplitude plots because the separate phase responses from the poles and zeros can be combined into one plot such as is shown in Figure 15. Now the complete amplitude or phase response of the circuit can be observed by looking at Figure 15. Although the phase shift at a pole is -45 degrees, the plot indicates -5 degrees at $\omega = 0.44/RC$ because the double zero located at $\omega = 1/RC$ has already accumulated significant positive phase shift at the pole frequency. The non-linearity of the phase plot, a result of the tangent function, makes it hard to approximate accurately when several poles and zeros congregate in the same vicinity.

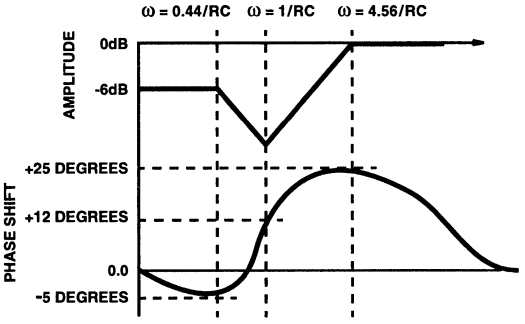

FIGURE 15. COMPOSITE BODE PLOT FOR THE BAND REJECT FILTER

Spacing the poles and zeros by a decade enables an accurate phase plot using approximate methods, but the circuit performance criteria usually will not allow this luxury. The amplitude plot also becomes smeared by the close proximity of the poles and zeros, but the exact values are not usually plotted because the approximate values usually suffice for analysis [6]. The demand for the phase accuracy stems from the oscillation or stability criteria which is dependent on phase.

Applying logarithms to the system equations will enable a quick and rather complete analysis. Equation 4 is repeated in Equation 26 in log form; i.e., both sides of the equation have been operated on by the function $20LOG_{10}\,(F(t))$.

$$20\text{LOG}(V_O/V_I) = 20\text{LOG}(A) - 20\text{LOG}(1 + A\beta) \qquad \text{(EQ. 26)}$$

As would be expected from the preceding analysis, the shape of the plot will be determined by the breakpoints, if any, contained in A or β.The magnitude portion of the closed

loop system equation is plotted in Figure 16 for the case where A and β are not a function of frequency. Notice that both plots are flat lines, and there is no phase plot. Obviously this case is trivial and of no interest to the circuit designer because it does not represent the real world since the gain of all amplifiers is a function of frequency [7].

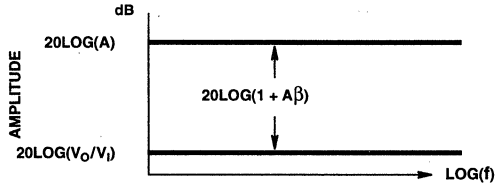

FIGURE 16. PLOT OF EQUATION 4 WHEN A AND β ARE NOT FREQUENCY DEPENDENT

Most high gain amplifiers such as operational amplifiers have multiple poles, two per transistor, with the amplifier having as many as 20 transistors leading to a potential of 40 or more poles. Normally only a few poles are important because the other poles occur at very high frequencies where the gain is less than one so that they can not cause oscillation. In many amplifiers the manufacturer compensates the amplifier with a single pole usually called a dominant pole (f_{AMP}), and the amplifier's performance can be approximated by the transfer function $A = a/(1 + j\,(f/f_{AMP}))$. Equation 4 is plotted in Figure 17 with the assumption that A is frequency dependent and β is resistive or frequency independent.

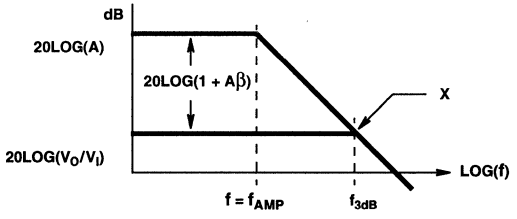

FIGURE 17. PLOT OF EQUATION 4 WHEN $A = a/(1 + j\,(f/f_{AMP}))$ AND β IS FREQUENCY INDEPENDENT

The closed loop gain graphical approximation is constant until its projection intersects the amplifier gain at point X. The actual closed loop gain starts rolling off prior to point X, and it is down -3dB at point X. If $20LOG(V_O/V_I)$ -20LOG(A) = -3dB then -20LOG(1 + Aβ) = -3dB, and if the magnitude of (1 + Aβ) is considered, then the square root of $(1 + (A\beta)^2) = 1.414$ resulting in Aβ = 1. In other words, A = 1/β at the intersection of the two curves. There is a method [8] of relating the phase shift, and thus the stability, to the slope of the curves at the intersect point, but this method will not be covered here in favor of the Bode Aβ method.

The dominant pole causes the open loop gain to have a breakpoint at the frequency f_{AMP}. The internally compensated op amp acts like a dominant pole characteristic so its AC parameters can be determined by referring to the "Open-Loop Frequency Response" curve contained in the data sheet. Although the curve is called "Open-Loop Frequency Response", it really is the direct gain (A). Notice that the CA158 op amp as shown in the Harris Semiconductor catalog [9] has a breakpoint which occurs at f_{AMP} = 5Hz., and the DC gain is 110dB. If the transfer function shown in Figure 17 was for the CA158 then the direct gain would be $A = a/(1 + j\,(f/f_{AMP}))$, or $A = 316{,}227/(1 + j\,(f/5))$. Consider for a moment the difficulty and hence the probable error associated with measuring the DC gain and the break point. A popular method of measuring the op amp gain and phase is to configure the op amp in the inverting mode and then measure the error voltage; i.e., the voltage from the inverting input to ground. Then Equation 3, $E = V_O/A$, is employed to calculate the op amp gain from the measured error. Assume that the op amp is configured in a gain of -100; then the direct gain is A = 100/101 times the op amp gain so a small offset must be accounted for because the measurement is not a direct measurement in the inverting circuit configuration. If the output voltage, V_O, is kept small to guarantee small signal accuracy, say one volt, then for the CA158, V_{ERROR} = 1/316,217 = 3.16μV. Measuring this small voltage especially considering that noise may be present is a formidable task so designers must assume that there may be a considerable tolerance associated with these measurements. The numbers given in this paper are for explanation purposes; professional test engineers will often configure the op amp with a gain of A = -10,000 and then be measuring errors in the nano-volt range. These measurements require considerable skill, and even then there may be a 24dB difference between the minimum specification point and the typical value such as in the HA5177 data sheet.

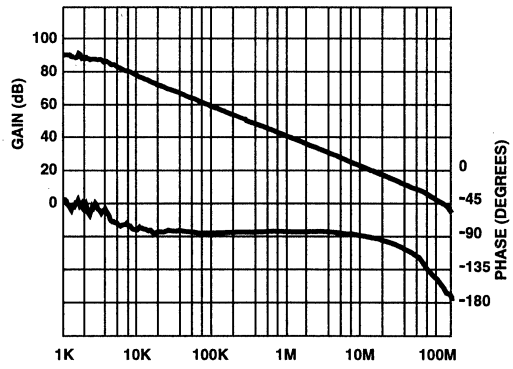

FIGURE 18. OPEN LOOP FREQUENCY RESPONSE OF THE HA2842C

Figure 18 is a plot of the gain phase relationship for a high frequency op amp, the HA2842C. The DC gain is 90dB, and since the phase shift reaches -45 degrees at 1200Hz the first pole must occur at approximately 1200Hz. This is a high frequency op amp so the internal compensation capacitor has been reduced significantly to increase the bandwidth available to the designer, and it is apparent that a second pole exists because the phase shift approaches -135 degrees at 70MHz. Looking closely at the point where the gain crosses the 0dB axis, and then following that constant frequency line, 120MHz, down to the phase curve indicates that the phase shift is about -165 degrees. This op amp is marginally stable, and the op amp is susceptible to stability problems unless external compensation techniques are employed. The HA2842C can be modeled with a DC gain of

31,623, the first break point at 1200Hz and the second breakpoint at 145MHz. The equation for the HA2842C is then A = 31,623/(1 + j (f/1200))(1 + j (f/145E6)).

Stability as Determined from Loop Plots

$A\beta = -1 = |1|\angle -180$ (EQ. 27)

Equation 8 has been repeated above as Equation 27. If the magnitude of the gain is greater than one in Equation 27, the equation will be satisfied because the non-linear effects of the active devices as they enter saturation will reduce the gain to one. This is demonstrated in oscillator design where the designer must design for a worse case gain of at least one, so the circuit will oscillate under all conditions, and the nominal gain usually is much greater than one. The oscillator designers are caught in a trap, for if they design for a worse case low gain greater than one, then the worse case high gain will be much greater than one. In the low gain case, the circuit barely oscillates, but the sinewave is very pure. In the high gain case, the circuit always oscillates, but there is significant distortion in the sinewave. Just as the oscillator designer must make compromises for the sake of instability, so, the analog designer make compromises for the sake of stability. In the case of amplifier design, the phase shift must never become -180 degrees, at a gain greater than one, or oscillation will occur. The compromise occurs when the amplifier designer trades off gain and/or bandwidth for positive phase shift because the methods which produce a safe phase shift tend to reduce gain or bandwidth, as will be shown later. In many cases oscillation is not the limiting factor because as the phase shift gets much greater than -135 degrees, the amplifier output will have increasing overshoot and ringing. Plotting the loop gain gives great insight into both the stability and closed loop performance; stability will be discussed in this section and closed loop performance predictions from open loop plots will be discussed in the next section.

$$A\beta = \frac{K}{(1+R_1C_1s)(1+R_2C_2s)} \quad \text{(EQ. 28)}$$

where K = DC gain.

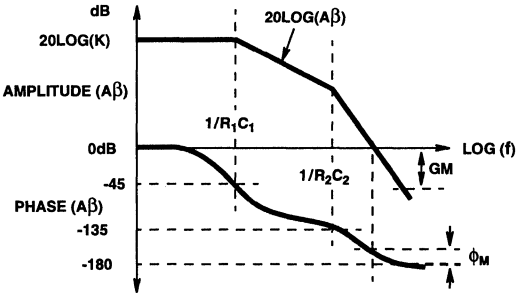

FIGURE 19. LOOP PHASE AND GAIN PLOT OF EQUATION 27

Figure 19 is used to help define the industry standard terms, phase margin, ϕ_M, and gain margin, GM. Phase margin is a measure of relative stability, and it is defined as the amount of phase shift between the point where the loop gain equals 0dB and -180 degrees. Equation 29 defines the phase margin mathematically.

$\phi_M = 180 - \text{tangent}^{-1}(A\beta)$ (EQ. 29)

Gain margin is defined as the gain at the point where the phase equals -180 degrees. Gain margin is always a negative (dB), or less than one, in a stable system, and it does not contain much information about stability or closed loop performance. The phase margin shown in Figure 19 is approximately 16 degrees; attempting to measure the phase margin in Figure 19 points out how important it is to plot phase margin accurately. This circuit will be stable since the phase margin is positive; the phase shift cannot ever reach the -180 degrees required for oscillation if the circuit is to remain stable. Because the phase margin is very small, the overshoot will be very large, and the output will exhibit a damped oscillation commonly known as ringing. If the gain, K, were increased in the loop transfer function until it crossed the 0dB axis at -180 degrees phase shift, then the circuit would oscillate; thus, there is a definite limit on the loop gain. The loop transfer function, shown as Figure 19, is repeated in Figure 20 with the gain increased by a factor of C. Notice that indeed the -180 degree phase crossover point occurs prior to the 0dB crossover point, so the phase margin is negative and the circuit will oscillate. Conversely, the transfer function shown in Figure 20 does not even have enough gain at the -180 degree point to ensure oscillation under production tolerances, so the circuit is good for nothing in its present condition.

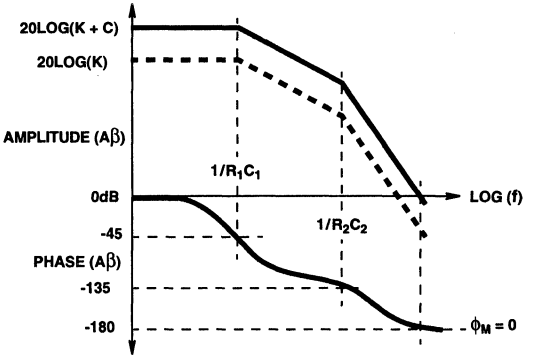

FIGURE 20. LOOP PHASE AND GAIN PLOT OF EQUATION 27 WITH ADDED GAIN C

Extremely high gain systems have very low errors, but they are limited in the bandwidth they can obtain without oscillating, so designers resort to other techniques such as non-linear transfer functions. An example of a high gain, accurate system which employs non-linear techniques to achieve stability, is a gyro stabilization platform which would go into a limit cycle if the gain was not reduced upon start-up.

If the second breakpoint, $1/R_2C_2$, were moved closer to the first breakpoint, then the circuit would accumulate phase shift from the breakpoint earlier and it may become unstable. Figure 19 is repeated as Figure 21, where the second breakpoint has been moved closer to the first breakpoint. Notice that the -45 degree phase point is not affected, the -135

degree phase point has moved in towards the -45 degree phase point, and that the -180 degree phase point occurs prior to the 0dB crossover point. Generally, moving the two poles closer together can cause instability.

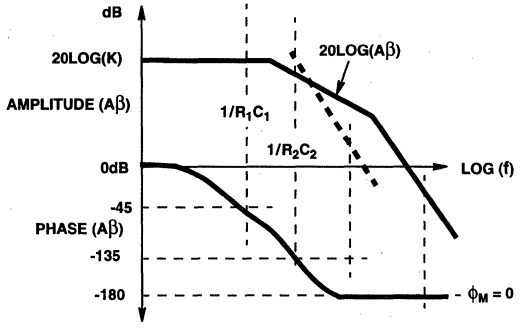

FIGURE 21. LOOP PHASE AND GAIN PLOT OF EQUATION 27 WITH $1/R_2C_2$ CLOSER TO $1/R_1C_1$

The single pole system cannot accumulate more than -90 degrees of phase shift so it cannot become unstable; thus single pole systems will not be discussed here. This does not mean that an internally compensated op amp, which acts like a dominant pole, cannot become unstable because all op amps have more than one pole. The proof of this is the data sheet, consider the HA2500 [10] which is internally compensated for unity gain, where the Open Loop Frequency and Phase Response curve shows phase shifts beyond -90 degrees. Lots of good data can be gathered from these curves; i.e., the phase margin for the HA2500 is approximately 30 degrees so there will be some overshoot, and there is a second pole at about 3MHz. There is no such thing as an unconditionally stable op amp unless it lies on the table with power disconnected, because all op amps are multiple pole devices especially when stray capacitances are considered. This conclusion may lead someone to wonder where to draw the line when doing an analysis, and most engineers draw the line at two poles because the mathematics are easy to handle. If required, they obtain a solution for larger systems through the use of superposition, but usually the poles are separated far enough for some of them to be ignored or the circuit is modified to achieve the separation. The next section will delve into the second order stability analysis more deeply. Poles and zeros always occur in pairs, although sometimes either the pole or zero may be at the origin or infinity, thus they will not always appear in the transfer function. Whenever a pole is referred to, its corresponding zero is also considered.

Predicting Stability and Performance from Closed Loop Plots

The closed loop AC performance of a feedback circuit is dependent on the order of the denominator equation which is often considered equivalent to the number of poles contained in the circuit. If the circuit has no poles then its AC performance does not vary with frequency. If the circuit has one pole then the closed loop AC performance is rather easy to describe; the gain on a Bode plot will be 20LOG(K) and the amplitude response will start falling off at the breakpoint with a -20dB/decade slope. If the circuit has two or more poles the closed loop AC response is much more complicated, the circuit can overshoot, then ring and finally oscillate. The second order circuit, which contains two poles, is so popular that it is described extensively in the literature [11], and it is the one that will be dwelled on here. Higher order circuits can usually be reduced to second order for closed loop performance analysis, so this analysis will be restricted to stability and closed loop performance for second order circuits. Equation 7 is written here as Equation 30 with a second order loop transfer function substituted for Aβ. Equation 31 is obtained from Equation 30 through algebraic manipulation.

$$1 + A\beta(s) = 1 + \frac{K}{(1+s\tau_1)(1+s\tau_2)} = 0 \qquad \text{(EQ. 30)}$$

where $\tau = RC$

$$s^2 + \frac{\tau_1+\tau_2}{\tau_1\tau_2}s + \frac{1+K}{\tau_1\tau_2} = 0 \qquad \text{(EQ. 31)}$$

Equation 32 is the standard second order control equation, and it is compared to Equation 31 to obtain Equation 33 and Equation 34 which define the damping ratio, ζ, and undamped natural frequency, ω_N.

$$s^2 + 2\zeta\omega_N s + \omega_N^2 = 0 \qquad \text{(EQ. 32)}$$

$\omega = 2\pi f$

$$\omega_N^2 = \frac{1+K}{\tau_1\tau_2} \qquad \text{(EQ. 33)}$$

$$2\zeta\omega_N = \frac{\tau_1+\tau_2}{\tau_1\tau_2} \qquad \text{(EQ. 34)}$$

The frequency where the magnitude of the loop transfer function, Aβ, is equal to one is defined as the crossover frequency, ω_C; this is expressed in Equation 35 with ω_C substituted for ω. Then Equation 35 is algebraically manipulated to obtain Equation 36 from which the phase functions shown in Equation 37 and Equation 38 are obtained.

$$\frac{K}{\sqrt{\left(1+\omega_C^2\tau_1^2\right)}\sqrt{\left(1+\omega_C^2\tau_2^2\right)}} = 1 \qquad \text{(EQ. 35)}$$

$$\omega_C^4 + 2\zeta\omega_N^2\omega_C^2 - \omega_N^4 = 0 \qquad \text{(EQ. 36)}$$

$$\phi_M = TAN^{-1}\left|\frac{\omega_C(\tau_1+\tau_2)}{1-\omega_C^2\tau_1\tau_2}\right| \qquad \text{(EQ. 37)}$$

$$\phi_M = TAN^{-1}\left|2\zeta\omega_N/\omega_C\right| \qquad \text{(EQ. 38)}$$

Considering the transfer function shown in Figure 22, if the 0dB crossover frequency, $\omega = \omega_C$, occurs well after the break frequency, $1/\tau_2$, then Equation 39 can be simplified to Equation 40. Solving Equation 40 for ω_C yields Equation 41.

$$20LOG(A\beta) = 20LOG(K) - 20LOG(1+\omega^2\tau_1^2)^{1/2} - 20LOG(1+\omega^2\tau_2^2)^{1/2} \qquad \text{(EQ. 39)}$$

$$20LOG(A\beta) = 20LOG(K) - 20LOG(\omega\tau_1) - 20LOG(\omega\tau_2) \text{ for } \omega \gg 1/\tau_2 \qquad \text{(EQ. 40)}$$

$$\omega_C = \sqrt{\frac{K}{\tau_1\tau_2}} \approx \omega_N \quad \text{for} \omega \gg 1/\tau_2 \qquad \text{(EQ. 41)}$$

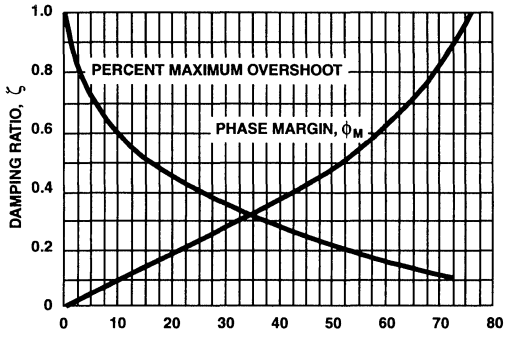

FIGURE 22. PHASE MARGIN AND PERCENT OVERSHOOT AS A FUNCTION OF DAMPING RATIO

Figure 22 is a plot of Equation 38; now the phase margin is expressed in terms of known quantities so it can be calculated from a knowledge the pole locations. The estimation procedure is to determine the pole locations from knowing the op amp pole locations and from the external circuitry. Once the pole locations and the gain are known or estimated the phase margin, damping ratio and cutoff frequency can be calculated. Then using Figure 22 yields the percent overshoot. The pole locations and gain can be varied to obtain different solutions to the problem. After all of this data is satisfactory, then the loop transfer function should be plotted to determine stability. While only the poles were used in the estimation procedure, both the poles and zeros must be used to plot the open transfer function. After several iterations a workable solution should pop out if one exists. Remember that this procedure is an approximation, thus it must always be verified in the laboratory.

Compensation Schemes

All op amps are compensated; some are compensated with internal components thus saving the designer time and money. Many op amps are not compensated internally because leaving out the compensation gives the designer an extra degree of freedom, and these op amps must have some kind of external compensation or they will oscillate. The internally compensated op amps are usually compensated with a method called 'dominant pole' or 'lag' compensation several forms of which are shown in Figure 23.

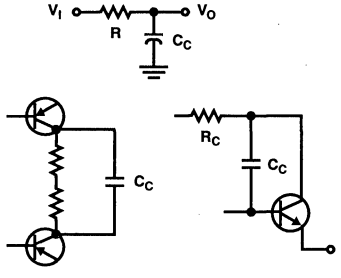

FIGURE 23. EXAMPLES OF DOMINANT POLE COMPENSATION

Dominant pole compensation circuits tend to be associated with the op amp, and they usually are not part of the feedback circuit. The loop transfer function for an op amp is shown in Figure 24 in solid lines. There are two poles accumulating phase shift prior to the 0dB crossover point; thus this circuit may very well be unstable. The first pole, $1/\tau_1$, is the low frequency break point of the op amp, and the second pole, $1/\tau_2$, is the high frequency break point. Since these pole locations are inherent in the op amp design, the circuit designer must live with them, but the effects of these poles can be modified with external feedback components. Locating the dominant pole, $1/\tau_{DP}$, so that the 0dB crossover point coincides with the first op amp pole,τ_1, yields a phase margin of 45 degrees. By locating the dominant pole zero crossing at $1/\tau_1$ the circuit sacrifices significant bandwidth which can be regained by moving the pole further out. The exact pole placement will be a function of the circuit specifications such as the allowed overshoot or the bandwidth required.

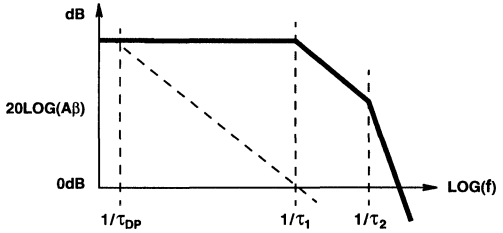

FIGURE 24. DOMINANT POLE COMPENSATION PLOT

Because of the loop gain loss and the bandwidth loss dominant pole compensation is only used inside the op amp, when the closed loop bandwidth requirements are not great, or if noise reduction is desired. A simpler method of compensating the op amp is with gain compensation. Consider Equation 14 which is repeated here as Equation 42; this equation is for the loop gain and it is valid for both inverting and non-inverting op amps. If the closed loop inverting gain is increased to 9, then Equation 42 becomes A/10 a decrease of 20dB in the DC intercept. Plotting these results in Figure 25 reveals that the circuit has become stable without much of a bandwidth reduction.

$$\frac{V_{\tau O}}{V_{\tau I}} = \frac{aZ_1}{Z_1 + Z_2} = A\beta \qquad \text{(EQ. 42)}$$

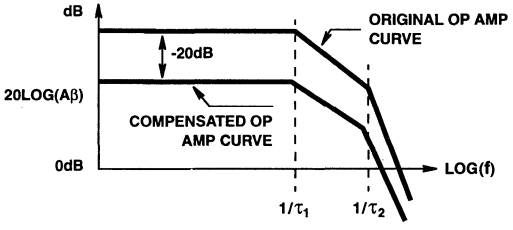

FIGURE 25. GAIN COMPENSATION

The occasion always arises where the closed loop gain must be one or less, thereby precluding the use of gain compensation; thus the designer must resort to other techniques to achieve the circuit performance. An alternate method of

compensation is called lead compensation, and it consists of putting a zero in the loop transfer function to cancel out one of the poles. The best place to locate the zero is on top of the second pole, since this cancels the negative phase shift caused by the second pole. The schematic of a circuit which employs lead compensation is shown in Figure 26, and Equation 43 is for the loop transfer function.

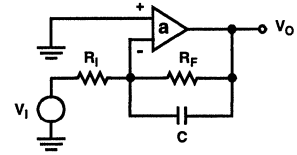

FIGURE 26. LEAD COMPENSATION

The zero in Equation 43 occurs before the pole, so it can be used to cancel out the pole at $1/\tau_2$ by placing the zero on top of the pole. Now the 135 degree phase shift point has moved out to $1/R_F||R_I Cs$ yielding better phase margin. There are always compromises to be made when designing a feedback circuit, and the one made here is to add external components. If the op amp has additional poles close to $1/\tau_2$, and many op amps do, then the pole placement is critical. Some op amps have so many poles in the area of $1/\tau_2$ that this method of compensation cannot be used.

$$A\beta = \frac{aR_I}{R_I + R_F}\frac{(R_F Cs + 1)}{(R_I||R_F Cs + 1)} \qquad \text{(EQ. 43)}$$

Unless specified otherwise, the amplifier gain (a) will be assumed to have the form $a = K/(1 + \tau_1 s)(1 + \tau_2 s)$.

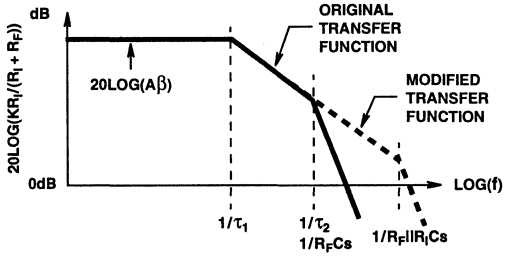

FIGURE 27. LEAD COMPENSATION PLOT

Sometimes a good look at the problem reveals a potential solution, so the case of stray input capacitance will be investigated. An inverting amplifier with a stray input capacitance, C_I, is shown in Figure 28. Looking at Equation 44 for the open loop transfer function, it is obvious that the stray capacitance adds a pole to the transfer function, and if the added pole is close to $1/\tau_2$ the circuit will become unstable. The capacitor, C_F shown in dotted lines, is added to the circuit to yield the transfer function shown in Equation 45. Inspection of Equation 45 reveals that if $R_I C_I = R_F C_F$, then the poles and zeros in the transfer function will cancel each other, and the transfer function will appear to be independent of frequency. This type of compensation is named after the same idea used in the compensated attenuator, which is an old instrument design trick. Which just proves that little in circuit design is really new.

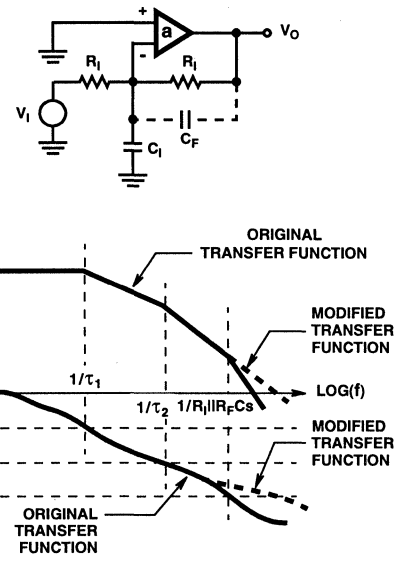

FIGURE 28. COMPENSATED ATTENUATOR CIRCUIT SCHEMATIC, GAIN PLOT AND PHASE PLOT

No C_F:

$$A\beta = \frac{aR_I}{R_I + R_F}\frac{1}{1 + R_I||R_F Cs} \qquad \text{(EQ. 44)}$$

C_F in circuit:

$$A\beta = \frac{a\dfrac{R_I}{(R_I C_I s + 1)}}{\dfrac{R_I}{(R_I C_I s + 1)} + \dfrac{R_F}{(R_F C_F s + 1)}} \qquad \text{(EQ. 45)}$$

There are times when an extra degree of freedom is required and the lead-lag, sometimes called the feed-forward, form of compensation yields this freedom. This method of compensation puts a pole and a zero in the loop transfer function. If the pole and zero locations must be independent of each other, then separate compensation networks need to be used. An example of this would be to use a lag circuit similar to that shown in Figure 24, and a lead circuit similar to that shown in Figure 26. The lead and lag would then be independent in the example so they could be placed conveniently for compensation purposes. The circuit shown in Figure 29 has both a pole and a zero, but their placement is not independent.

$$A\beta = \frac{aR_I}{R_I + R_F}\frac{(RCs + 1)}{\dfrac{(RR_I + R_F R + R_F R_I)}{R_F + R_I}Cs + 1} \qquad \text{(EQ. 46)}$$

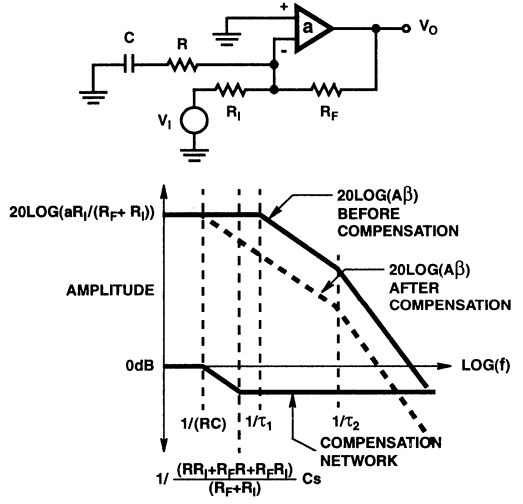

FIGURE 29. LEAD-LAG COMPENSATION SCHEMATIC AND Aβ AMPLITUDE PLOT

Referring to Figure 29, it can be seen that the lead-lag compensated circuit crosses 0dB at a lower frequency than the uncompensated circuit, thus the compensation has made the circuit more stable. Also, the transfer function of the compensation has been shown in Figure 29 for clarity. There is an additional advantage to lead-lag compensation in that it yields higher gain at high frequencies. The closed loop gain plots, Figure 30, show that the zero precedes the pole; the poles and zeros interchange when the plot changes from the loop gain to the closed loop gain. Also, the high frequency gain is emphasized with lead-lag compensation. The high frequency emphasis may be desirable when a high overall gain is needed, but some unwanted effects, such as DC offset, must be minimized. The lead-lag method of compensation usually requires the precise placement of the poles and zeros so a detailed and accurate [12] phase plot is generally constructed for this case.

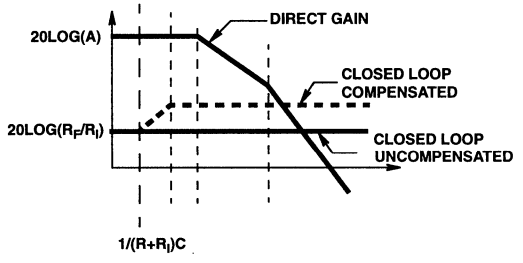

FIGURE 30. LEAD-LAG CLOSED LOOP GAIN PLOTS FOR COMPENSATED AND UNCOMPENSATED CIRCUITS

Comparison of Compensation Results

Dominant pole compensation is the easiest method of compensation to implement within an IC, but it rolls off the closed loop gain so quickly that it is seldom used except in op amp design. The circuit resulting from dominant pole design is very well behaved because the phase margin is usually about 45 degrees, but the frequency response is very poor. If the transfer function for the HA2842C shown in Figure 18 is compensated by dominant pole compensation, the pole would be placed at 1200Hz; the loop gain when moving to a lower frequency would then rise at a rate of 20dB/decade until it hit the 90dB point at 0.06Hz. This is an effective bandwidth reduction of 4.5 decades, from 120MHz to 1200Hz, so this method is only used when no other type of compensation is available, noise reduction is more important than bandwidth or bandwidth is not important.

Gain compensation is always the preferred method of compensation if the resulting higher closed loop gain meets the performance criteria, but many times the design specifications call for a buffer or an inverter both with a gain of one, which precludes gain compensation. Gain compensation does not require any additional external components beyond the gain setting resistors, it preserves the op amp bandwidth and it is easy to implement. In a single pole system, increasing gain will reduce the bandwidth by the same factor.

Lead compensation offers an AC compensation which can function for any DC gain, and it is has a much higher frequency response than dominant pole compensation. One deficiency with lead compensation is that the DC gain, the zero and the pole are all tied together tightly. For example if the HA2842C shown in Figure 18 is lead compensated for a closed loop gain of -1 then $R_I = R_F$. This means that the pole and zero are only separated by an octave so the compensation must be done in an area of the loop gain plot which is very close to 0dB. Observing Figure 18, it can be seen that the best place that lead compensation can improve stability significantly is at the second pole where the phase equals -135 degrees phase shift and the frequency is 75MHz. Placing the zero at 75MHz yields a phase margin of about 60 degrees resulting a nice stable circuit with 10% overshoot per Figure 22. The closed loop response equation is $V_I/V_F = R/R_I 1/(R_F Cs + 1)$, and the closed loop gain is -1 until it reaches the frequency $f = 1/2\pi R_F C$, 150MHz, where it is down by -3dB. Lead compensation rolls off the closed loop frequency response dramatically.

The compensated attenuator approach works well for negating the effects of an input capacitance because both the open loop and closed loop transfer functions have a flat frequency response. Also, the compensation required is very small. When the output resistance of an op amp gets very high, the stray capacitance seen across the resistor acts like a lead circuit and rolls off the high frequency gain. Adding an input capacitor, the reverse of attenuator compensation, serves to restore the high frequency performance. Both digital-to-analog converters and optical receiving diodes

have large associated capacitances, so when they are put into the input circuit of an op amp, often in an I-to-V converter configuration, the circuit oscillates. The compensated attenuator tames these circuits, but beware, the compensation must consider the worst case especially for current DACs which have a wide range of output capacitance.

The lead-lag compensation scheme is very similar to the lead compensation scheme but it has two advantages. First, setting the DC gain does not fix the pole zero separation, so for low gains the pole and zero could be separated by more than an octave. Second, a zero shows up in the closed loop transfer function where it increases the gain at high frequencies. The combination of these two advantages are great enough to outweigh the cost of the extra components added to the circuit.

The compensation techniques demonstrated here serve as a good foundation for feedback circuit design, but like all foundations it is meant to be built on [13]. There are other methods of treating compensation such as closed loop stability plots, Nichols charts, root locus plots and Nyquist analysis. Each technique offers some advantages and disadvantages; the Bode method simply is the author's personal choice so the other techniques deserve investigation.

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Harris Semiconductor

APPNOTE

No. AN9420.1 April 1995

Harris Linear

Current Feedback Amplifier Theory and Applications

Authors: Ronald Mancini and Jeffrey Lies

Introduction

Current feedback amplifiers (CFA) have sacrificed the DC precision of voltage feedback amplifiers (VFA) in a trade-off for increased slew rate and a bandwidth that is relatively independent of the closed loop gain. Although CFAs do not have the DC precision of their VFA counterparts, they are good enough to be DC coupled in video applications without sacrificing too much dynamic range. The days when high frequency amplifiers had to be AC coupled are gone forever, because some CFAs are approaching the GHz gain bandwidth region. The slew rate of CFAs is not limited by the linear rate of rise that is seen in VFAs, so it is much faster and leads to faster rise/fall times and less intermodulation distortion.

The general feedback theory used in this paper is developed in Harris Semiconductor Application Note Number AN9415 entitled "Feedback, Op Amps and Compensation." The approach to the development of the circuit equations is the same as in the referenced application note, and the symbology/terminology is the same with one exception. The impedance connected from the negative op amp input to ground, or to the source driving the negative input, will be called Z_G rather than Z_1 or Z_I, because this has become the accepted terminology in CFA papers.

Development of the General Feedback Equation

Referring to the block diagram shown in Figure 1, Equation 1, Equation 2 and Equation 3 can be written by inspection if it is assumed that there are no loading concerns between the blocks. This assumption is implicit in all block diagram calculations, and requires that the output impedance of a block be much less than input impedance of the block it is driving. This is usually true by one or two orders of magnitude. Algebraic manipulation of Equation 1, Equation 2 and Equation 3 yields Equation 4 and Equation 5 which are the defining equations for a feedback system.

$$V_O = EA \quad \text{(EQ. 1)}$$

$$E = V_I - \beta V_O \quad \text{(EQ. 2)}$$

$$E = V_O/A \quad \text{(EQ. 3)}$$

$$V_O/V_I = A/(1 + A\beta) \quad \text{(EQ. 4)}$$

$$E/V_I = 1/(1 + A\beta) \quad \text{(EQ. 5)}$$

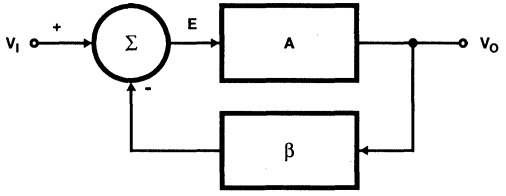

FIGURE 1. FEEDBACK SYSTEM BLOCK DIAGRAM

In this analysis the parameter A, which usually includes the amplifier and thus contains active elements, is called the direct gain. The parameter β, which normally contains only passive components, is called the feedback factor. Notice that in Equation 4 as the value of A approaches infinity the quantity Aβ, which is called the loop gain, becomes much larger than one; thus, Equation 4 can be approximated by Equation 6.

$$V_O/V_I = 1/\beta \quad \text{for } A\beta >> 1 \quad \text{(EQ. 6)}$$

V_O/V_I is called the closed loop gain. Because the direct gain, or amplifier response, is not included in Equation 6, the closed loop gain (for A >> 1) is independent of amplifier parameter changes. This is the major benefit of feedback circuits.

Equation 4 is adequate to describe the stability of any feedback circuit because these circuits can be reduced to this generic form through block diagram reduction techniques [1]. The stability of the feedback circuit is determined by setting the denominator of Equation 4 equal to zero.

$$1 + A\beta = 0 \quad \text{(EQ. 7)}$$

$$A\beta = -1 = |1| \angle -180 \quad \text{(EQ. 8)}$$

Observe from Equation 4 and Equation 8, that if the magnitude of the loop gain can achieve a magnitude of one while the phase shift equals -180 degrees, the closed loop gain becomes undefined because of division by zero. The undefined state is unstable, causing the circuit to oscillate at the frequency where the phase shift equals -180 degrees. If the loop gain at the frequency of oscillation is slightly greater than one, it will be reduced to one by the reduction in gain suffered by the active elements as they approach the limits of saturation. If the value of Aβ is much greater than one, gross nonlinearities can occur and the circuit may cycle between saturation limits. Preventing instability is the essence of feedback circuit design, so this topic will be touched lightly here and covered in detail later in this application note.

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A good starting point for discussing stability is finding an easy method to calculate it. Figure 2 shows that the loop gain can be calculated from a block diagram by opening current inputs, shorting voltage inputs, breaking the circuit and calculating the response (V_{TO}) to a test input signal (V_{TI}).

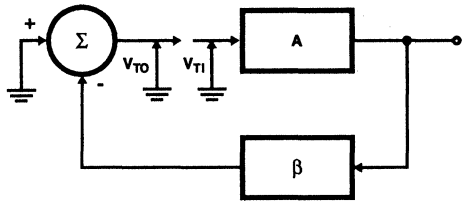

FIGURE 2. BLOCK DIAGRAM FOR COMPUTING THE LOOP GAIN

$$V_{TO}/V_{TI} = A\beta \qquad \text{(EQ. 9)}$$

Current Feedback Stability Equation Development

The CFA model is shown in Figure 3. The non-inverting input connects to the input of a buffer, so it is a very high impedance on the order of a bipolar transistor VFA's input impedance. The inverting input ties to the buffer output; Z_B models the buffer output impedance, which is usually very small, often less than 50Ω. The buffer gain, G_B, is nearly but always less than one because modern integrated circuit design methods and capabilities make it easy to achieve. G_B is overshadowed in the transfer function by the transimpedance, Z, so it will be neglected in this analysis.

The output buffer must present a low impedance to the load. Its gain, G_{OUT}, is one, and is neglected for the same reason as the input buffer's gain is neglected. The output buffer's impedance, Z_{OUT}, affects the response when there is some output capacitance; otherwise, it can be neglected unless DC precision is required when driving low impedance loads.

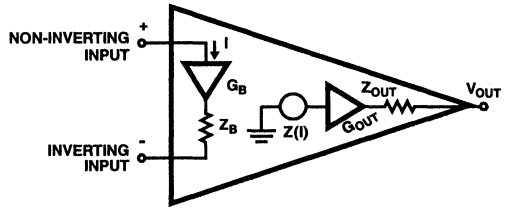

FIGURE 3. CURRENT FEEDBACK AMPLIFIER MODEL

Figure 4 is used to develop the stability equation for the inverting and non-inverting circuits. Remember, stability is a function of the loop gain, Aβ, and does not depend on the placement of the amplifier's inputs or outputs.

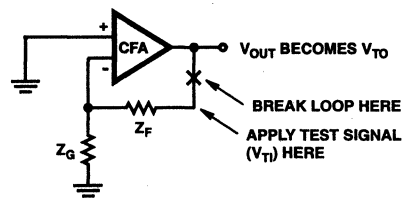

FIGURE 4. BLOCK DIAGRAM FOR STABILITY ANALYSIS

Breaking the loop at point X, inserting a test signal, V_{TI}, and calculating the output signal, V_{TO}, yields the stability equation. The circuit is redrawn in Figure 5 to make the calculation more obvious. Notice that the output buffer and its impedance have been eliminated because they are insignificant in the stability calculation. Although the input buffer is shown in the diagram, it will be neglected in the stability analysis for the previously mentioned reasons.

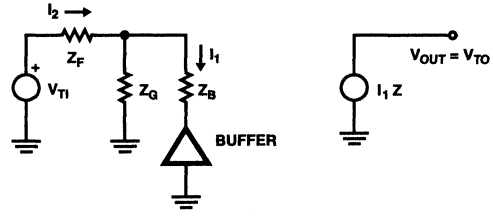

FIGURE 5. CIRCUIT DIAGRAM FOR STABILITY ANALYSIS

The current loop equations for the input loop and the output loop are given below along with the equation relating I_1 to I_2.

$$V_{TI} = I_2(Z_F + Z_G \| Z_B) \qquad \text{(EQ. 10)}$$

$$V_{TO} = I_1 Z \qquad \text{(EQ. 11)}$$

$$I_2(Z_G \| Z_B) = I_1 Z_B; \text{ For } G_B = 1 \qquad \text{(EQ. 12)}$$

Equation 10 and Equation 12 are combined to obtain Equation 13.

$$V_{TI} = I_1(Z_F + Z_G \| Z_B)(1 + Z_B/Z_G) = I_1 Z_F \ (1 + Z_B/Z_F \| Z_G) \qquad \text{(EQ. 13)}$$

Dividing Equation 11 by Equation 13 yields Equation 14 which is the defining equation for stability. Equation 14 will be examined in detail later, but first the circuit equations for the inverting and non-inverting circuits must be developed so that all of the equations can be examined at once.

$$A\beta = V_{TO}/V_{TI} = Z/(Z_F(1 + Z_B/Z_F \| Z_G)) \qquad \text{(EQ. 14)}$$

Developing the Non-Inverting Circuit Equation and Model

Equation 15 is the current equation at the inverting input of the circuit shown in Figure 6. Equation 16 is the loop equation for the input circuit, and Equation 17 is the output circuit equation. Combining these equations yields Equation 18, in the form of Equation 4, which is the non-inverting circuit equation.

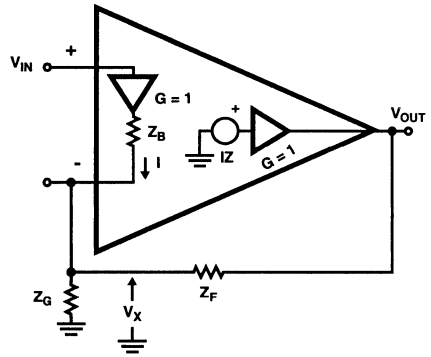

FIGURE 6. NON-INVERTING CIRCUIT DIAGRAM

$$I = (V_X/Z_G) - (V_{OUT} - V_X)/Z_F \quad \text{(EQ. 15)}$$

$$V_X = V_{IN} - IZ_B \quad \text{(EQ. 16)}$$

$$V_{OUT} = IZ \quad \text{(EQ. 17)}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{Z(1+Z_F/Z_G)}{Z_F(1+Z_B/Z_F \| Z_G)}}{1+\dfrac{Z}{Z_F(1+Z_B/Z_F \| Z_G)}} \quad \text{(EQ. 18)}$$

The block diagram equivalent for the non-inverting circuit is shown in Figure 7.

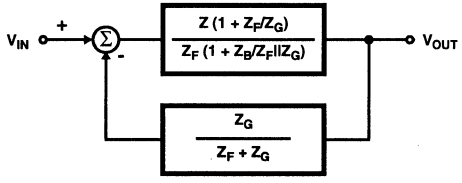

FIGURE 7. BLOCK DIAGRAM OF THE NON-INVERTING CFA

Developing the Inverting Circuit Equation and Model

Equation 19 is the current equation at the inverting input of the circuit shown in Figure 8. Equation 20 defines the dummy variable V_X, and Equation 21 is the output circuit equation. Equation 22 is developed by substituting Equation 20 and Equation 21 into Equation 19, simplifying the result, and manipulating it into the form of Equation 4.

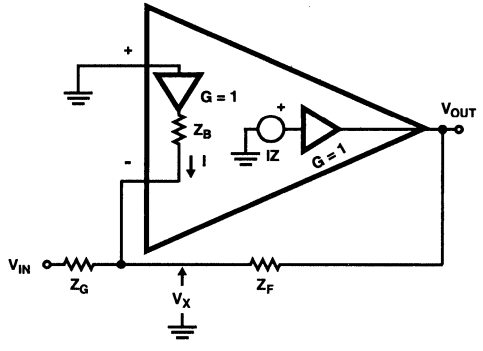

FIGURE 8. INVERTING CIRCUIT DIAGRAM

$$\frac{V_{IN} - V_X}{Z_G} + I = \frac{V_X - V_{OUT}}{Z_F} \quad \text{(EQ. 19)}$$

$$IZ_B = -V_X \quad \text{(EQ. 20)}$$

$$IZ = V_{OUT} \quad \text{(EQ. 21)}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\dfrac{Z}{Z_G(1+Z_B/Z_F \| Z_G)}}{1+\dfrac{Z}{Z_F(1+Z_B/Z_F \| Z_G)}} \quad \text{(EQ. 22)}$$

The block diagram equivalent for the inverting circuit is given in Figure 9.

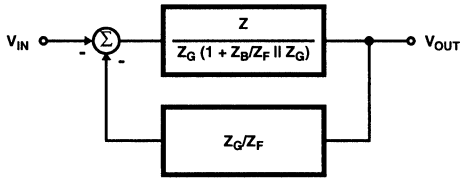

FIGURE 9. INVERTING BLOCK DIAGRAM

Stability

Equation 8 states the criteria for stability, but there are several methods for evaluating this criteria. The method that will be used in this paper is called the Bode plot [2] which is a log plot of the stability equation. A brief explanation of the Bode plot procedure is given in "Feedback, Op Amps and Compensation" [3]. The magnitude and phase of the open loop transfer function are both plotted on logarithmic scales, and if the gain decreases below zero dB before the phase shift reaches 180 degrees the circuit is stable. In practice the phase shift should be ≤140 degrees, i.e., greater than 40 degrees phase margin, to obtain a well behaved circuit. A sample Bode plot of a single pole circuit is given in Figure 10.

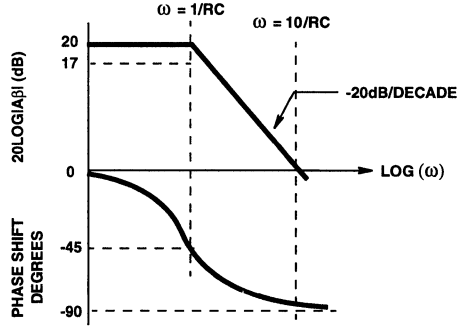

FIGURE 10. SAMPLE BODE PLOT

Referring to Figure 10, notice that the DC gain is 20dB, thus the circuit gain must be equal to 10. The amplitude is down 3dB at the break point, ω = 1/RC, and the phase shift is -45 degrees at this point. The circuit can not become unstable with only a single pole response because the maximum phase shift of the response is -90 degrees.

CFA circuits often oscillate, intentionally or not, so there are at least two poles in their loop gain transfer function. Actually, there are multiple poles in the loop gain transfer function, but the CFA circuits are represented by two poles for two reasons: a two pole approximation gives satisfactory correlation with laboratory results, and the two pole mathematics are well known and easy to understand. Equation 14, the stability equation for the CFA, is given in logarithmic form as Equation 23 and Equation 24.

$$20LOG|A\beta| = 20LOG|Z/(Z_F(1+Z_B/Z_F||Z_G))| \quad \text{(EQ. 23)}$$

$$\phi = TANGENT^{-1}(Z/(Z_F(1+Z_B/Z_F||Z_G))) \quad \text{(EQ. 24)}$$

The answer to the stability question is found by plotting these functions on log paper. The stability equation, $20log|A\beta|$, has the form 20logx/y which can be written as 20logx/y = 20logx - 20logy. The numerator and denominator of Equation 23 will be operated on separately, plotted independently and then added graphically for analysis. Using this procedure the independent variables can be manipulated separately to show their individual effects. Figure 11 is the plot of Equation 23 and Equation 24 for a typical CFA where $Z = 1M\Omega/(\tau_1 s + 1)(\tau_2 s + 1)$, $Z_F = Z_G = 1k\Omega$, and $Z_B = 70\Omega$.

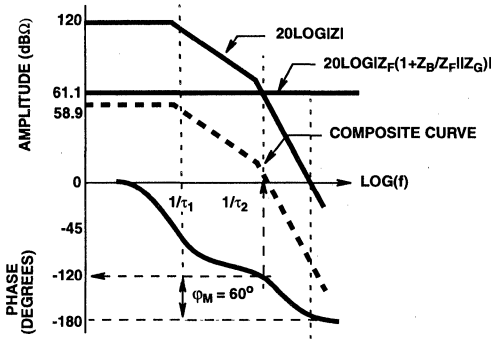

FIGURE 11. CFA TRANSIMPEDANCE PLOT

If $20log|Z_F(1+Z_B/Z_F||Z_G)|$ were equal to 0dB the circuit would oscillate because the phase shift of Z reaches -180 degrees before 20log|Z| decreases below zero. Since $20log|Z_F(1 + Z_B/Z_F||Z_G)| = 61.1dB\Omega$, the composite curve moves down by that amount to 58.9dBΩ where it is stable because it has 120 degrees phase shift or 60 degrees phase margin. If $Z_B = 0\Omega$ and $Z_F = R_F$, then $A\beta = Z/R_F$. In this special case, stability is dependent on the transfer function of Z and R_F, and R_F can always be specified to guarantee stability. The first conclusion drawn here is that $Z_F(1+Z_B/Z_F||Z_G)$ has an impact on stability, and that the feedback resistor is the dominant part of that quantity so it has the dominant impact on stability. The dominant selection criteria for R_F is to obtain the widest bandwidth with an accepted amount of peaking; 60 degrees phase margin is equivalent to approximately 10% or, 0.83dB, overshoot. The second conclusion is that the input buffer's output impedance, Z_B, will have a minor effect on stability because it is small compared to the feedback resistor, even though it is multiplied by $1/Z_F||Z_G$ which is related to the closed loop gain. Rewriting Equation 14 as $A\beta = Z/(Z_F+Z_B(1+R_F/R_G))$ leads to the third conclusion which is that the closed loop gain has a minor effect on stability and bandwidth because it is multiplied by Z_B which is a small quantity relative to Z_F. It is because of the third conclusion that many people claim closed loop gain versus bandwidth independence for the CFA, but that claim is dependent on the value of Z_B relative to Z_F.

CFAs are usually characterized at a closed loop gain (G_{CL}) of one. If the closed loop gain is increased then the circuit becomes more stable, and there is the possibility of gaining some bandwidth by decreasing Z_F. Assume that $A\beta_1 = A\beta_N$ where $A\beta_1$ is the loop gain at a closed loop gain of one and $A\beta_N$ is the loop gain at a closed loop gain of N; this insures that stability stays constant. Through algebraic manipulation, Equation 14 can be rewritten in the form of Equation 25 and solved to yield Equation 27 and a new Z_{FN} value.

$$\frac{Z}{Z_{F1}+Z_B(1+Z_{F1}/Z_{G1})} = \frac{Z}{Z_{FN}+Z_B(1+Z_{FN}/Z_{GN})} \quad \text{(EQ. 25)}$$

$$\frac{Z}{Z_{F1}+Z_B G_{CL1}} = \frac{Z}{Z_{FN}+Z_B G_{CLN}} \quad \text{(EQ. 26)}$$

$$Z_{FN} = Z_{F1}+Z_B(G_{CL1}-G_{CLN}) \quad \text{(EQ. 27)}$$

For the HA5020 at a closed loop gain of 1, if $Z = 6M\Omega$, $Z_{F1} = 1k\Omega$, and $Z_B = 75\Omega$, then $Z_{F2} = 925\Omega$. Experimentation has shown, however, that $Z_{F2} = 681\Omega$ yields better results. The difference in the predicted versus the measured results is that Z_B is a frequency dependent term which adds a zero in the loop gain transfer function that has a much larger effect on stability. The equation for Z_B[5] is given below.

$$Z_B = h_{IB} + \frac{R_B}{\beta_0+1}\left(\frac{1+S\beta_0/\omega_T}{1+S\beta_0/(\beta_0+1)\omega_T}\right) \quad \text{(EQ. 28)}$$

At low frequencies $h_{IB} = 50\Omega$ and $R_B/(\beta_o+1) = 25\Omega$ which corresponds to $Z_B = 75\Omega$, but at higher frequencies Z_B will vary according to Equation 28. This calculation is further complicated because β_0 and ω_T are different for NPN and PNP transistors, so Z_B also is a function of the polarity of the output. Refer to Figure 12 and Figure 13 for plots of the transimpedance (Z) and Z_B for the HA5020 [5]. Notice that Z starts to level off at 20MHz which indicates that there is a zero in the transfer function. Z_B also has a zero in its transfer function located at about 65MHz. The two curves are related, and it is hard to determine mathematically exactly which parameter is affecting the performance, thus considerable lab work is required to obtain the maximum performance from the device.

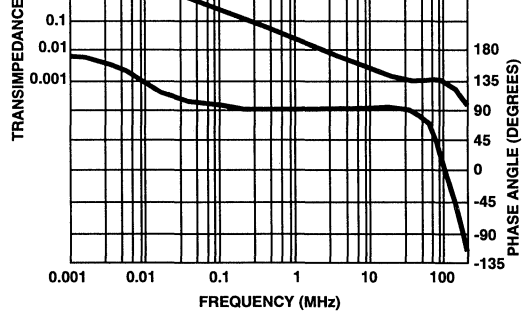

FIGURE 12. HA5020 TRANSIMPEDANCE vs FREQUENCY

Equation 27 yields an excellent starting point for designing a circuit, but strays and the interaction of parameters can make an otherwise sound design perform poorly. After the math analysis an equal amount of time must be spent on the circuit layout if an optimum design is going to be achieved. Then the design must be tested in detail to verify the performance, but more importantly, the testing must determine that unwanted anomalies have not crept into the design.

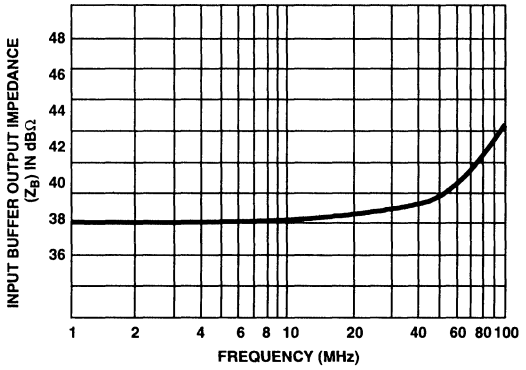

FIGURE 13. HA5020 INPUT BUFFER OUTPUT RESISTANCE vs FREQUENCY

Performance Analysis

Table 1 shows that the closed loop equations for both the CFA and VFA are the same, but the direct gain and loop gain equations are quite different. The VFA loop gain equation contains the ratio Z_F/Z_I, where Z_I is equivalent to Z_G, which is also contained in the closed loop gain equation. Because the loop gain and closed loop equations contain the same quantity, they are interdependent. The amplifier gain, a, is contained in the loop gain equation so the closed loop gain is a function of the amplifier gain. Because the amplifier gain decreases with an increase in frequency, the direct gain will decrease until at some frequency it equals the closed loop gain. This intersection always happens on a constant -20dB/decade line in a single pole system, which is why the VFA is considered to be a constant gain bandwidth device.

TABLE 1. SUMMARY OF OP AMP EQUATIONS

CIRCUIT CONFIGURATION	CURRENT FEEDBACK AMPLIFIER	VOLTAGE FEEDBACK AMPLIFIER
NON-INVERTING		
Direct Gain	$\frac{Z(1 + Z_F/Z_G)}{Z_F(1 + Z_B/Z_F \,\|\|\, Z_G)}$	a
Loop Gain	$Z/Z_F(1 + Z_B/Z_F \,\|\|\, Z_G)$	$aZ_G/(Z_G + Z_F)$
Closed Loop Gain	$1 + Z_F/Z_G$	$1 + Z_F/Z_G$
INVERTING		
Direct Gain	$\frac{Z}{Z_G(1 + Z_B/Z_F \,\|\|\, Z_G)}$	$aZ_F/(Z_F + Z_G)$
Loop Gain	$Z/Z_F(1 + Z_B/Z_F \,\|\|\, Z_G)$	$aZ_G/(Z_G + Z_F)$
Closed Loop Gain	$-Z_F/Z_G$	$-Z_F/Z_G$

The CFA's transimpedance, which is also a function of frequency, shows up in both the loop gain and closed loop gain equations, Equations 18 and 22. The gain setting impedances, Z_F and Z_G, do not appear in the loop gain as a ratio unless they are multiplied by a secondary quantity, Z_B, so Z_F can be adjusted independently for maximum bandwidth. This is why the bandwidth of CFA's are relatively independent of closed loop gain. When Z_B becomes a significant portion of the loop gain the CFA becomes more of a constant gain-bandwidth device.

Equation 5, which is rewritten here as Equation 29, expresses the error signal as a function of the loop gain for any feedback system. Consider a VFA non-inverting configuration where the closed loop gain is +1; then the loop gain, Aβ, is a. It is not uncommon to have VFA amplifier gains of 50,000 in high frequency op amps, such as the HA2841 [6], so the DC precision is then 100% (1/50,000) = 0.002%. In a good CFA the transimpedance is Z = 6MΩ, but Z_F =1kΩ so the DC precision is 100% (1075Ω/6MΩ) = 0.02%. The CFA often sacrifices DC precision for stability.

$$\text{Error} = V_I/(1 + A\beta) \qquad \text{(EQ. 29)}$$

The DC precision is the best accuracy that an op amp can obtain, because as frequency increases the gain, a, or the transimpedance, Z, decreases causing the loop gain to decrease. As the frequency increases the constant gain-bandwidth VFA starts to lose gain first, then the CFA starts to lose gain. There is a crossover point, which is gain dependent, where the AC accuracy for both op amps is equal. Beyond this point the CFA has better AC accuracy.

The VFA input structure is a differential transistor pair, and this configuration makes it is easy to match the input bias currents, so only the offset current generates an offset error voltage. The time honored method of inserting a resistor, equal to the parallel combination of the input and feedback resistors, in series with the non-inverting input causes the bias current to be converted to a common mode voltage. VFAs are very good at rejecting common mode voltages, so the bias current error is cancelled. One input of a CFA is the base terminal of a transistor while the other input is the output of a low impedance buffer. This explains why the input currents don't cancel, and why the non-inverting input impedance is high while the inverting input impedance is low. Some CFAs, such as the HFA1120 [7], have input pins which enable the adjustment of the offset current. Newer CFAs are finding solutions to the DC precision problem.

Stability Calculations for Input Capacitance

When there is a capacitance from the inverting input to ground, the impedance Z_G becomes $R_G/(R_GC_Gs+1)$, and Equation 14 can be written in the form of Equation 30. Then the new values for Z_G are put into the equation to yield Equation 31. Notice that the loop gain has another pole in it: an added pole might cause an oscillation if it gets too close to the pole(s) included in Z. Since Z_B is small it will dominate the added pole location and force the pole to be at very high frequencies. When C_G becomes large the pole will move in towards the poles in Z, and the circuit may become unstable.

$$A\beta = Z/(Z_B + Z_F/Z_G(Z_G + Z_B)) \qquad \text{(EQ. 30)}$$

If $Z_B = R_B$, $Z_F = R_F$, and $Z_G = R_G||C_G$, Equation 30 becomes:

$$A\beta = \frac{Z}{R_F(1 + R_B/R_F||R_G)(R_B||R_F||R_G C_G s + 1)} \quad \text{(EQ. 31)}$$

Stability Calculations for Feedback Capacitance

When a capacitor is placed in parallel with the feedback resistor, the feedback impedance becomes $Z_F = R_F/(R_F C_F s + 1)$. After the new value of Z_F is substituted into Equation 30, and with considerable algebraic manipulation, it becomes Equation 32.

$$A\beta = \frac{Z(R_F C_F s + 1)}{R_F(1 + (R_B/R_F||R_G)(R_B||R_F||R_G C_F s + 1)} \quad \text{(EQ. 32)}$$

The new loop gain transfer function now has a zero and a pole; thus, depending on the placement of the pole relative to the zero oscillations can result.

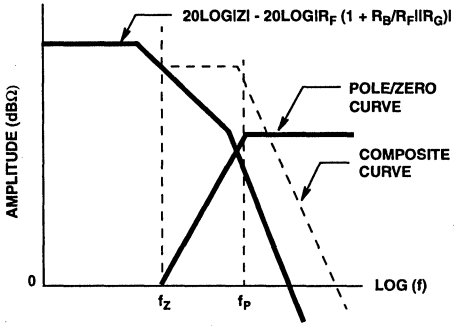

FIGURE 14. EFFECT OF C_F ON STABILITY

The loop gain plot for a CFA with a feedback capacitor is shown in Figure 14. The composite curve crosses the 0dBΩ axis with a slope of -40dB/decade, and it has more time to accumulate phase shift, so it is more unstable than it would be without the added poles and zeros. If the pole occurred at a frequency much beyond the highest frequency pole in Z then the Z pole would have a chance to roll off the gain before any phase shift from Z could add to the phase shift from the pole. In this case, C_F would be very small and the circuit would be stable. In practice almost any feedback capacitance will cause ringing and eventually oscillation if the capacitor gets large enough. There is the case where the zero occurs just before the Aβ curve goes through the 0dBΩ axis. In this case the positive phase shift from the zero cancels out some of the negative phase shift from the second pole in Z: thus, it makes the circuit stable, and then the pole occurs after the composite curve has passed through 0dBΩ.

Calculations and Compensation for C_G and C_F

Z_G and Z_F are modified as they were in the previous two sections, and the results are incorporated into Equation 30, yielding Equation 33.

$$A\beta = \frac{Z(R_F C_F s + 1)}{R_F(1 + R_B/R_F||R_G)(R_B||R_F||R_G(C_F + C_G)s + 1)} \quad \text{(EQ. 33)}$$

Notice that if the zero cancelled the pole in equation that the circuit AC response would only depend on Z, so Equation 34 is arrived at by doing this. Equation 35 is obtained by algebraic manipulation.

$$(R_F C_F s + 1) = (R_B||R_F||R_G(C_F + C_G)s + 1) \quad \text{(EQ. 34)}$$

$$R_F C_F = C_G R_G R_B/(R_G + R_B) \quad \text{(EQ. 35)}$$

Beware, R_B is a frequency sensitive parameter, and the capacitances may be hard to hold constant in production, but the concept does work with careful tuning. As Murphy's law predicts, any other combination of these components tends to cause ringing and instability, so it is usually best to minimize the capacitances.

Summary

The CFA is not limited by the constant gain bandwidth phenomena of the VFA, thus the feedback resistor can be adjusted to achieve maximum performance for any given gain. The stability of the CFA is very dependent on the feedback resistor, and an excellent starting point is the device data sheet which lists the optimum feedback resistor for various gains. Decreasing R_F tends to cause ringing, possible instability, and an increase in bandwidth, while increasing R_F has the opposite effect. The selection of R_F is critical in a CFA design; start with the data sheet recommendations, test the circuit thoroughly, modify R_F as required and then test some more. Remember, as Z_F approaches zero ohms, the stability decreases while the bandwidth increases; thus, placing diodes or capacitors across the feedback resistor will cause oscillations in a CFA.

The laboratory work cannot be neglected during CFA circuit design because so much of the performance is dependent on the circuit layout. Much of this work can be simplified by starting with the manufacturers recommended layout; Harris Semiconductor appreciates the amount of effort it takes to complete a successful CFA design so they have made evaluation boards available. The layout effort has already been expended in designing the evaluation board, so use it in your breadboard; cut it, patch it, solder to it, add or subtract components and change the layout in the search for excellence. Remember ground planes and grounding technology! These circuits will not function without good grounding techniques because the oscillations will be unending. Coupled with good grounding techniques is good decoupling. Decouple the IC at the IC pins with surface mount parts, or be prepared to fight phantoms and ghosts.

Several excellent equations have been developed here, and they are all good design tools, but remember the assumptions. A typical CFA has enough gain bandwidth to ridicule most assumptions under some conditions. All of the CFA parameters are frequency sensitive to a degree, and the art of circuit design is to push the parameters to their limit.

Although CFAs are harder to design with than VFAs, they offer more bandwidth, and the DC precision is getting better. They are found in many different varieties; clamped outputs, externally compensated, singles, duals, quads and many special functions so it is worth the effort to learn to design with them.

References

[1] Del Toro, Vincent and Parker, Sydney, "Principles of Control Systems Engineering", McGraw-Hall Book Company, 1960

[2] Bode H.W., "Network Analysis and Feedback Amplifier Design", D. VanNostrand, Inc., 1945

[3] Harris Semiconductor, Application Note 9415, Author: Ronald Mancini, 1994

[4] Jost, Steve, "Conversations About the HA5020 and CFA Circuit Design", Harris Semiconductor, 1994

[5] Harris Semiconductor, "Linear and Telecom ICs for Analog Signal Processing Applications", 1993 - 1994

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APP NOTE

No. AN9502.1 November 1996

Harris Linear

Oscillator Produces Quadrature Waves (HA5025)

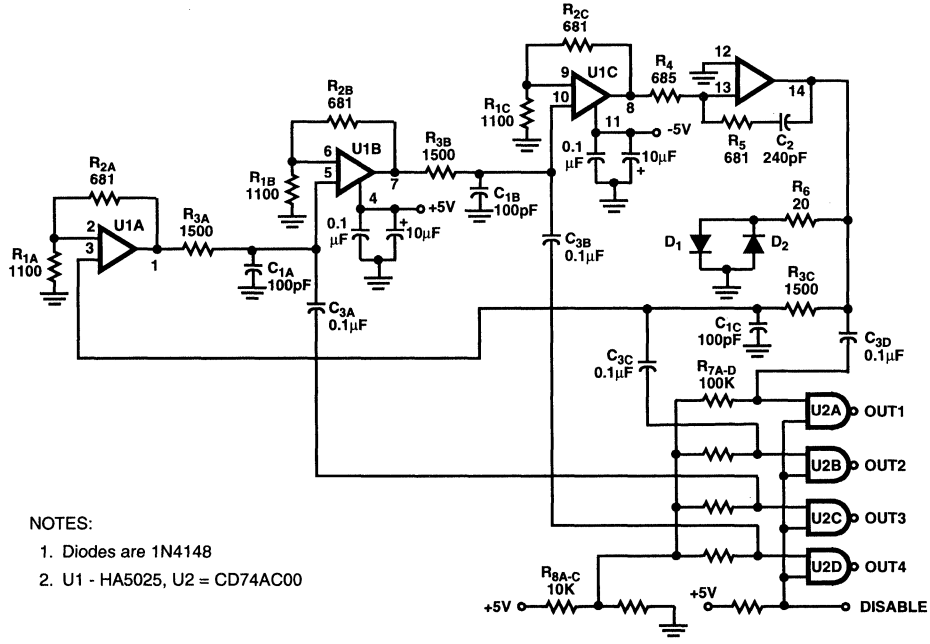
Author: Ronald Mancini

By employing a high-frequency quad current-feedback amplifier (the HA5025) as an RC oscillator, four quadrature sine waves can be generated, see Figure 1. The HA5025's four separate amplifiers generate the sine waves, while the quad NAND gate, U2, is biased at its threshold, so it acts as a sine-wave to square-wave converter when the sine waves are AC-coupled into its input.

The criterion for oscillation is that the open-loop gain be ≥1 when the feedback phase shift is zero. In this design, there are three noninverting phase-shifting stages and one inverting phase-shift stage (U1D); thus the phase shift of each stage must equal 45 degrees lag. This phase shift plus the 180 degrees introduced by the phase inversion of U1D equals 360 degrees or 0 degrees, resulting in in-phase feedback at the oscillation frequency.

Because the HA5025 features such high open-loop gain-bandwidth characteristics, amplifier phase shift is negligible in the low MHz range. Thus, each stage's phase shift is solely determined by the passive components. At ϕ = 45 degrees, $R_3C_1 = R_5C_2 = 1/(2\pi f)$; the component values shown for f = 1MHz. The rate of change of phase shift with respect to frequency ($d\phi/df$) is maximum at ϕ = 45 degrees for this type RC circuit. Therefore, the stability is highest for the four-RC configuration. The combination of good phase sensitivity with no active amplifier phase shift yields a stable RC oscillator whose temperature performance depends only on passive components.

Most RC oscillators described in the literature employ a lead circuit as the phase-shifting element. While that practice is fine for voltage-feedback amplifiers, it results in multiple



NOTES:

1. Diodes are 1N4148
2. U1 - HA5025, U2 = CD74AC00

FIGURE 1. FOUR QUADRATURE SINE WAVES CAN BE GENERATED WITH THIS OSCILLATOR DESIGN, WHICH USES THE HA5025 HIGH-FREQUENCY QUAD CURRENT-FEEDBACK AMPLIFIER. THE FOUR SEPARATE AMPLIFIERS PRODUCE THE FOUR SINE WAVES.

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frequency oscillations in current-feedback amplifiers because of their ideal gain flatness performance. The voltage-feedback amplifier's gain rapidly falls off at higher frequencies, preventing oscillation beyond the design frequency. This also is an indicator of the deleterious phase performance associated with the voltage-feedback amplifier.

Because the voltage gain of each RC network is 0.707, the noninverting amplifiers are arbitrarily set at gain of 1.6; the inverting stage over all gain also is slightly above one at 1MHz. By distributing the gain over four amplifiers, the resultant open-loop gain can be well controlled. As a result, with the aid of R_6, D_1, and D_2, the amplitude limiting can be limited to minimize sine-wave distortion. Rather good sine-wave outputs are available across C_{1A}, C_{1B}, C_{1C}, and the output of U1D. This RC concept can be extended to well above 20MHz using the HA5025 with just a slight frequency drift. The quadrature sine waves are AC-coupled to a quad CMOS gate biased at its threshold by R_7 and R_8 to obtain quadrature square waves. If these square waves aren't exactly 45 degrees phase-shifted from each other, adjust the bias circuit or add independent bias networks.

Harris Semiconductor

APPNOTE

No. AN9503.1 November 1996

Harris Linear

Low Output Impedance MUX (HA5022)

Author: Ronald Mancini

Two common problems will surface when trying to multiplex multiple high-speed signals into a low-impedance load, such as an analog-to-digital converter. The first is the low load impedance, which tends to make amplifiers oscillate and thus causes gain errors. The second problem involves the multiplexer, which supplies no gain, introduces distortion, and limits the frequency response.

Using op amps that have an enable/disable function, such as the HA5022, will eliminate the multiplexer problems. That's because the external multiplexer chip isn't needed, and the HA5022 can drive low-impedance (large capacitance) loads if a series isolation resistor is employed.

Looking more closely at the circuit, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications, see Figure 1. Because the output cables usually are terminated in their characteristic impedance, the gain is 0.5. Consequently, amplifiers U2A and U2B are configured in a gain of +2 to set the circuit gain at 1. R_2 and R_3 determine the amplifier gain; if a different gain is desired, R_2 should be changed according to the equation:
$G = (1 + R_3/R_2)$.

R_3 sets the amplifier's frequency response, so it's best to check the manufacturer's data sheet before changing its value.

R_5, C_1, and D_1 make up an asymmetrical charge/discharge time circuit that configures U1 as a break-before-make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels, the drive logic must be designed to be break-before-make. Also, the inhibit input is only functional when the channel switch input is high. R_4 is enclosed in the feedback loop of the amplifier so that the large open-loop amplifier gain of U2 will present the load with a small closed-loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown was tested for the full range of capacitor values with no oscillations observed. Thus, the problem is solved. The circuit's frequency and gain characteristics are now those of the amplifier independent of any multiplexing action. This essentially solves the second problem. The multiplexer transition time is approximately 15µs with the component values shown.

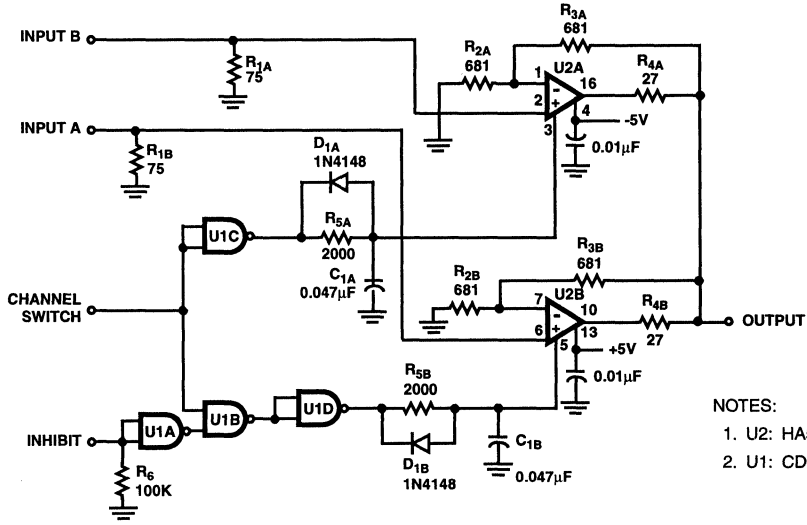

FIGURE 1. THIS LOW-OUTPUT IMPEDANCE MULTIPLEXER WILL SOLVE PROBLEMS OF OSCILLATION CAUSED BY LOW LOAD IMPEDANCE, AS WELL AS DISTORTION AND LIMITED FREQUENCY RESPONSE INTRODUCED BY THE MULTIPLEXER. THE SECOND PROBLEM IS SOLVED BECAUSE THE FREQUENCY AND GAIN CHARACTERISTICS BECOME THOSE OF THE AMPLIFIER, INDEPENDENT OF THE MULTIPLEXER.

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APPNOTE

No. AN9507.1 November 1996

Harris Linear

Video Cable Drivers Save Board Space, Increase Bandwidth (HFA1112, HFA1114)

Author: Jeff Lies

Designing video cable drivers seems to be a fairly simple task. Just buy an amplifier with enough bandwidth, high output current, a gain of two or greater (eliminating most buffers) to counteract attenuation from back-terminating the cable, and good video specifications (gain flatness if you are designing for component video; differential gain and phase if you are designing for composite video), and you're in business.

Of course, picking a current feedback amplifier adds a few additional worries such as choosing the optimum feedback resistor, and minimizing the capacitance on both the summing node (-Input) and output. Still another problem is achieving the desired performance at typical video loads (≤75Ω if driving multiple back-terminated cables).

Choosing dual or quad amplifiers and/or SOIC packaging complicates the equation even further. How does the engineer find a way to optimally place eight gain-setting resistors, not to mention termination resistors, around a quad amplifier in an SOIC package? There is no easy solution. Compromises must be made, which usually result in inadequate terminations or long trace lengths.

Specialized ICs can simplify the task of cable driver design and board layout. However, even the best cable driver can't solve all problems.

A common complaint when working with long cables involves a particular type of image degradation. The display in question exhibits bright horizontal lines but gray vertical lines. Since it is well known that narrow vertical lines require higher bandwidth to be displayed properly, the bandwidth obviously is being limited somewhere in the system. Invariably, substituting a shorter cable dramatically improves the image quality, leading to the hypothesis that the cable driver's performance degrades when driving long cables. This hypothesis requires some scrutiny.

It's true that circuit performance changes when driving cables, but is it really the cable driver that is at fault? Figure 1 illustrates the performance of Harris Semiconductor's HFA1112 amplifier driving 100 feet of back-terminated cable. It shows that the amplifier's 550MHz bandwidth decreases to 40MHz over the measured range, lending credence to the previous hypothesis. But what's really happening?

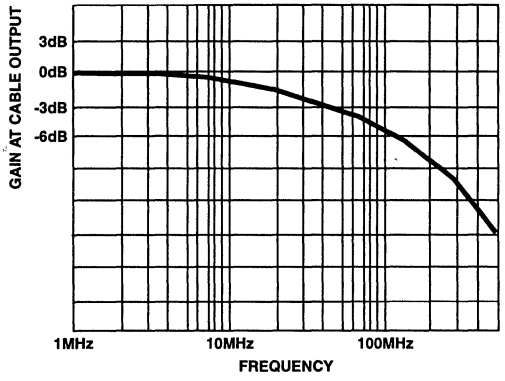

FIGURE 1. PERFORMANCE RESULTS INDICATE THAT THE HFA1112 AMPLIFIER'S 550MHz BANDWIDTH DECREASES TO 40MHz WHEN DRIVING 100 FEET OF BACK-TERMINATED CABLE. THIS SUPPORTS THE HYPOTHESIS THAT A CABLE DRIVER'S PERFORMANCE DEGRADES WHEN DRIVING LONG CABLES.

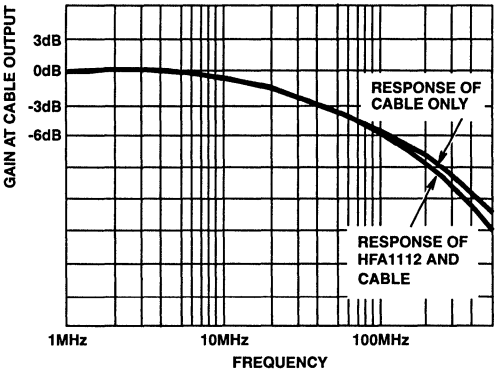

FIGURE 2. ALTHOUGH USUALLY TAKEN FOR GRANTED, LONG CABLES CAN LIMIT SYSTEM BANDWIDTH TO LOW FREQUENCIES, AS IS EVIDENT IN THIS COMPARISON BETWEEN THE FREQUENCY RESPONSE OF THE HFA1112 DRIVING THE CABLE AND THE RESPONSE OF THE CABLE ALONE.

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Many engineers forget that all electrical elements have finite bandwidth. Cables are usually taken for granted, but long cables can limit system bandwidth to surprisingly low frequencies. For example, a comparison of the frequency response of the HFA1112 driving the same 100 feet of cable to the response of the cable alone shows that the problem isn't the cable driver, but rather the cable itself (see Figure 2).

It is abundantly clear from Figure 2 that the cable performance itself limits the system performance for most of the frequency range. Throwing a higher bandwidth driver at the cable will, in fact, gain the engineer designing the system nothing, because you can't get more bandwidth than the cable allows.

Upgrading to a higher performance cable, such as a Belden 8281 or equivalent, is one solution to boosting system bandwidth. There are at least two downsides to this option, however. The first is that it introduces significantly higher cable costs. The second is problems presented to technicians who have to work with more rigid cables.

A better solution may be to use a cable driving buffer such as Harris' HFA1114. The driver's frequency response is tunable for a specific cable length via components connected to the summing node (see Figure 3). By shunting R_1, R_C acts to increase the amplifier's gain while C_C controls the cut-in frequency of the compensation.

These three components peak the amplifier's frequency response to counteract the cable's roll-off characteristic. By squeezing more bandwidth out of a given cable, higher-performance cables aren't needed.

An unexpected but welcome side effect of this particular solution is that using the on-chip gain-setting resistors frees up board space for the compensation components.

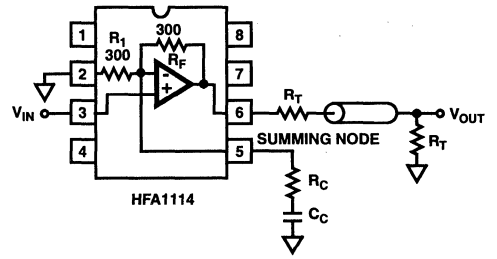


FIGURE 3. INSTEAD OF UPGRADING TO A HIGHER PERFORMANCE CABLE TO INCREASE SYSTEM BANDWIDTH, A CABLE DRIVER LIKE THE HFA1114 CAN BE EMPLOYED. THE DRIVER'S FREQUENCY RESPONSE IS TUNABLE FOR A SPECIFIC CABLE LENGTH VIA THE COMPONENTS CONNECTED TO THE SUMMING NODE.

APPNOTE

No. AN9508.1 November 1996

Harris Linear

Video Multiplexer Delivers Lower Signal Degradation (HA5024)

Author: Ronald Mancini

Video multiplexers pose a difficult design challenge. They must perform several functions, such as matching the input line impedance, signal amplification, signal switching, and driving the output line, without degrading or adding noise and transients to the signal. Typically, the signal flows through the multiplexer where it's degraded by the multiplexers errors. In this design, the signal flows through the op amp and thus isn't degraded by the multiplexer.

This circuit can multiplex several sources like VCRs, tuners, or cameras into a single monitor, see Figure 1. The HA5024IP quad op amp performs all of the multiplexer and amplification functions with the aid of the TTL decoder. It exceeds the gain flatness, differential phase, and differential gain specifications for NTSC video, without adding the offset voltages, gain variability, or transients associated with multiplexers.

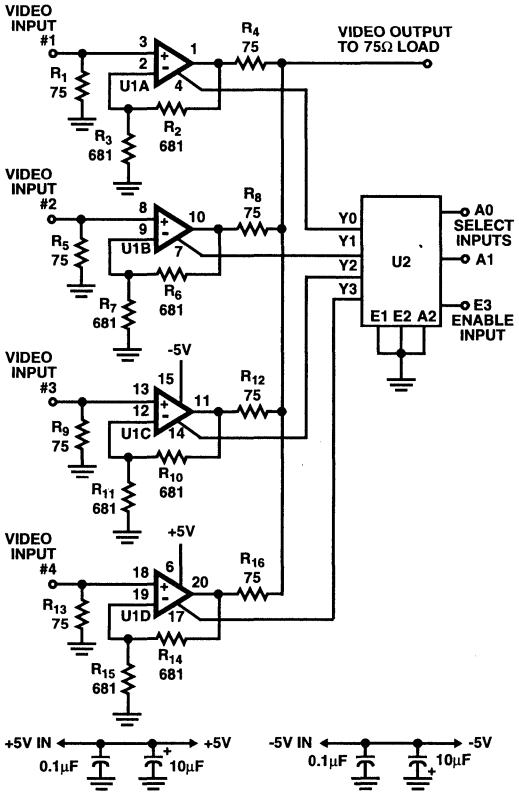
Turning our attention to op amp U1A, R_1 terminates the input cable in its characteristic impedance, which usually is 75Ω in video systems. R_4 back terminates the output cable in its characteristic impedance of 75Ω. Because the cable termination is 75Ω, it forms a voltage divider with R_4, which has a gain of 0.5. The op amp is configured for a gain of two, therefore the circuit has an overall gain of one when driving a double terminated cable. The value of R_3 can be changed according to the formula $G = 0.5\ (1 + R_2/R_3)$. R_2 determines the video performance of the op amp, so it should not be changed. The circuits U1B through U1D, perform similarly.

If more than one video output is needed, R_4, R_8, R_{12}, and R_{16} can be paralleled with 75Ω resistors. Each resistor is connected from the respective op amp output to a second video output that can drive another 75Ω cable.

U2 is configured as a two-to-four line decoder, with A0 and A1 acting as the select inputs and E3 as the enable input. All of the amplifiers are disabled when E3 is low, so there's no output signal. When E3 is high, the select inputs determine the video input that's connected to the video output. If E3 is used to disable the outputs when the select inputs are changed, there will be minimal bus contention transients during switching. However, if hot switching is desired, a break-before-make delay circuit should be placed in series with the Y_X lines. Because all of the signal switching occurs within the HA5024IP, the amplifier's differential phase and gain parameters (0.03 degrees and 0.03%, respectively) determine the circuit's performance.

It's easy to multiplex any number of channels with this scheme because the single and dual versions of the op amp help minimize the number of ICs required for a given design.

In addition, the decoder can be easily extended to 3 to 8 using the same IC or 4 to 16 using a different decoder. The circuit given here switches in less than a microsecond.



NOTES:
1. U1 is HA5024IP
2. All resistors in Ω
3. U2 is CD74HC238
4. Use ground plane

FIGURE 1. SEVERAL DIFFERENT SOURCES, SUCH AS VCRs, TUNERS, OR CAMERAS, CAN BE MULTIPLEXED INTO A SINGLE MONITOR USING THIS VIDEO MULTIPLEXER. WITH THE AID OF TTL DECODER, THE HA5024IP QUAD OP AMP PERFORMS ALL MULTIPLEXER AND AMPLIFICATION FUNCTIONS.

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APPNOTE

No. AN9510.1 November 1996

Harris Linear

Basic Analog for Digital Designers

Authors: Ron Mancini and Chris Henningsen

What Is This Application Note Trying To Accomplish?

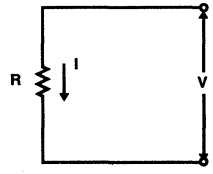
There is a long gap between engineering college and mid career in a non-engineering position, but technology marches on so a simple method of keeping abreast with the latest developments is required. This application note starts with an overview of the basic laws of physics, progresses through circuits 1 and 2, and explains op amp operation through the use of feedback principles. Math is the foundation of circuit design, but it is kept to the simplest level possible in this application note. For more advanced op amp topics please refer to the technical papers listed in references 1 and 2.

Basic Physics Laws, Circuit Theorems and Analysis

Good news and bad news. The bad news is that it takes a certain amount of dog work, like relearning physics and circuit theorems, before proficiency becomes second nature. The good news is that if you just hang in for a few pages you will experience the joy of analyzing circuits like an expert. You will gain ten years experience in a few hours. You will be able to write op amp equations like a design engineer. You might think this is a worthless effort, but imagine the look on the analog engineer's face, the one who thinks non-analog engineers are as dumb as a box of rocks, when you write your own op amp circuit equations.

Ohm's and Kirchoff's Laws

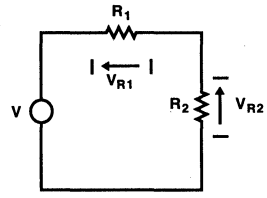
Ohm's law states that there is a relationship between the current in a circuit and the voltage potential across a circuit. This relationship is a function of a constant called the resistance.



$V = IR$ (EQ.1)

FIGURE 1. ILLUSTRATION OF OHM'S LAW

Kirchoff's voltage law states that the algebraic sum of the voltages around any closed loop equals zero. The sum includes independent voltage sources, dependent voltage sources and voltage drops across resistors (called IR drops).

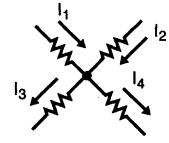


$V - V_{R1} - V_{R2} = 0$ or $V = V_{R1} + V_{R2}$ (EQ. 2)

Σ voltage sources = Σ voltage drops (EQ. 3)

FIGURE 2. ILLUSTRATION OF KIRCHOFF'S VOLTAGE LAW

Kirchoff's current law states that the algebraic sum of all the currents leaving a node equals zero. The sum includes independent current sources, dependent current sources, and component currents.



$I_1 + I_2 = I_3 + I_4$ (EQ. 4)

$I_1 + I_2 - I_3 - I_4 = 0$ (EQ. 5)

Σ currents into a junction = 0 (EQ. 6)

FIGURE 3. ILLUSTRATION OF KIRCHOFF'S CURRENT LAW

Voltage and Current Dividers

Voltage dividers are seen often in circuit design because they are useful for generating a reference voltage, for biasing active devices, and acting as feedback elements. Current dividers are seen less often, but they are still important so we will develop the equations for them. The voltage divider equations, which assume that the load does not draw any current, are developed in Figure 4.

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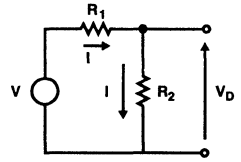


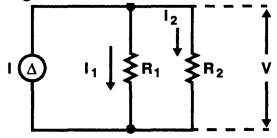
$$V = IR_1 + IR_2 = I(R_1 + R_2) \quad \text{(EQ. 7)}$$

$$I = \frac{V}{(R_1 + R_2)} \quad \text{(EQ. 8)}$$

$$V_D = IR_2 = \frac{V}{(R_1 + R_2)}(R_2) = V\frac{R_2}{R_1 + R_2} \quad \text{(EQ. 9)}$$

FIGURE 4. DERIVATION OF THE VOLTAGE DIVIDER RULE

The current divider equations, assuming that the only load is R_2, is given in Figure 5.



$$I = I_1 + I_2 \quad \text{(EQ. 10)}$$

$$V = I_1R_1 = I_2R_2 \quad \text{(EQ. 11)}$$

$$I_1 = I_2\frac{R_2}{R_1} \quad \text{(EQ. 12)}$$

$$I = I_1 + I_2 = I_2\frac{R_2}{R_1} + I_2 = I_2\left(1 + \frac{R_2}{R_1}\right) = I_2\left(\frac{R_1 + R_2}{R_1}\right) \quad \text{(EQ. 13)}$$

$$\text{Then: } I_2 = I\frac{R_1}{R_1 + R_2} \quad \text{(EQ. 14)}$$

FIGURE 5. DERIVATION OF THE CURRENT DIVIDER RULE

Thevenin's and Norton's Theorems

There are situations where it is simpler to concentrate on one component rather than write equations for the complete circuit. When the input source is a voltage source, Thevenin's theorem is used to isolate the component of interest, but if the input source is a current source, Norton's theorem is used to isolate the component of interest.

To apply Thevenin's theorem one must look back into the terminals of the component being replaced. Now calculate the open circuit voltage seen at these terminals, and during this calculation consider that there is no load current so the voltage divider rule can be used. Next short independent voltage sources and open independent current sources; now calculate the impedance seen looking into the terminals. The final step is to replace the original circuit with the Thevenin equivalent voltage, V_{th}, and Thevenin equivalent impedance, Z_{th}.

Thevenin's theorem is illustrated in Figure 6.

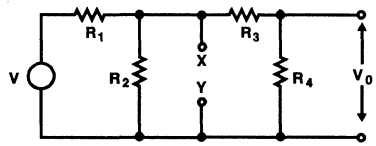


FIGURE 6. THE ORIGINAL CIRCUIT

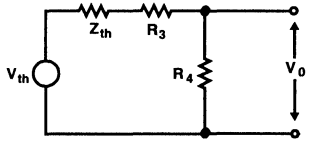
The open circuit voltage is calculated by looking into the terminals X - Y, and then calculating the open circuit voltage with the voltage divider rule.

$$V_{th} = V\frac{R_2}{R_1 + R_2} \quad \text{(EQ. 15)}$$

The impedance looking back into the terminals X - Y with the independent source, V, shorted is given below.

$$Z_{th} = Z_{x-y} = \frac{R_1R_2}{R_1 + R_2} \equiv R_1 \parallel R_2 \quad \text{(EQ. 16)}$$

The circuit to the left of X - Y is now replaced by the Thevenin equivalents.

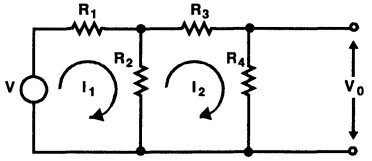


$$V_0 = V_{th}\frac{R_4}{Z_{th} + R_3 + R_4} \quad \text{(EQ. 17)}$$

$$= V\frac{\frac{R_2}{R_1 + R_2}\,R_4}{\frac{R_1R_2}{R_1 + R_2} + R_3 + R_4}$$

FIGURE 7. THE THEVENIN EQUIVALENT CIRCUIT

The loop equations are worked out below. Notice that not only is the derivation of the equations more laborious, but the labor will get out of hand with the addition of another loop. This is why Thevenin's theorem is preferred over loop equations.



$$V = I_1(R_1 + R_2) - I_2R_2 \quad \text{(EQ. 18)}$$

$$I_2(R_2 + R_3 + R_4) = I_1R_2 \quad \text{(EQ. 19)}$$

$$I_1 = \frac{R_2 + R_3 + R_4}{R_2}\,I_2 \quad \text{(EQ. 20)}$$

$$I_2\frac{(R_2 + R_3 + R_4)}{R_2}(R_1 + R_2) - I_2R_2 \quad \text{(EQ. 21)}$$

$$I_2 = \frac{V}{\frac{R_2 + R_3 + R_4}{R_2}(R_1 + R_2) - R_2} \quad \text{(EQ. 22)}$$

$$V_0 = I_2R_4 \quad \text{(EQ. 23)}$$

$$V_0 = V\frac{R_4}{\frac{(R_2 + R_3 + R_4)(R_1 + R_2)}{R_2} - R_2} \quad \text{(EQ. 24)}$$

FIGURE 8. LOOP EQUATION ANALYSIS OF THE SAME CIRCUIT

The Norton equivalent circuit is seldom used in circuit design, so it's derivation [3] and illustration will be left to the serious student.

Superposition

The principle of superposition states that the equation for each independent source can be calculated separately, and then the equations (or results) can be added to give the total result. When implementing superposition the equation for each source is calculated with the other independent voltage sources short circuited and the independent current sources open circuited. The equations for all the sources are added together to obtain the final answer.

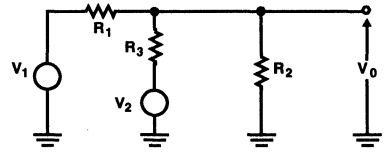


FIGURE 9. SUPERPOSITION EXAMPLE

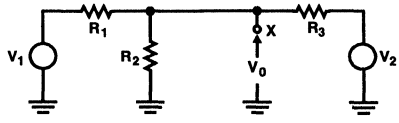
$$V_{01}\big|_{V_2=0} = \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} V_1 \quad V_{02}\big|_{V_1=0} = \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2} V_2$$

(EQ. 25)

$$V_0 = V_{01} + V_{02} = V_1 \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} + V_2 \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2} \quad \text{(EQ. 26)}$$

Analysis Tools - Why Do We Need More Than One?

Each one of the analysis tools shown has a place where it is optimal. Later during the op amp analysis the tools will be employed to relieve the burden of detailed calculation. Figures 10 and 11 illustrate an example of the extra calculations caused by using the less optimal tool to perform the analysis.



$$V_{th} = \frac{R_2}{R_1 + R_2} V_1 \quad R_{th} = R_1 \parallel R_2 \quad \text{(EQ. 27)}$$

FIGURE 10. SUPERPOSITION EXAMPLE REDRAW

$$I = \frac{V_2 - V_{th}}{R_{th} + R_3} \qquad V_0 = V_2 - IR_3 \quad \text{(EQ. 28)}$$

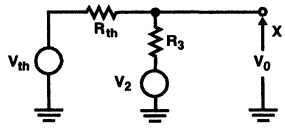


FIGURE 11. THEVENIN EQUIVALENT CIRCUIT MODEL

$$V_0 = V_2 - \frac{V_2 - V_{th}}{R_{th} + R_3} R_3 = V_2 - \frac{V_2 - \frac{R_2 V_1}{R_1 + R_2}}{R_1 \parallel R_2 + R_3} R_3 \quad \text{(EQ. 29)}$$

Notice that the Thevenin method used twice as many equations to describe the circuit as were required to arrive at the same result with superposition. Also, the form of the final equation arrived at by superposition is much easier to analyze.

Feedback Principles

This discussion of feedback principles is simple because they are easy to understand. The application of the principles can be very complicated for the design engineer, but we can grasp the principles without understanding all of the nuances. If this material creates a thirst it may be slaked by reading references 2 and 3.

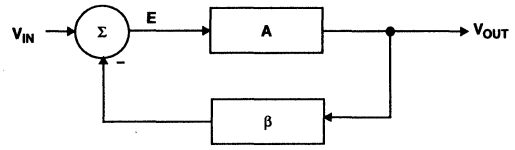


FIGURE 12. FEEDBACK BLOCK DIAGRAM

$$V_{OUT} = EA \quad \text{(EQ. 30)}$$

$$E = V_{IN} - \beta V_{OUT} \quad \text{(EQ. 31)}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \quad \text{(EQ. 32)}$$

Equations 30 and 31 are written on the block diagram, and Equation 32 is obtained by combining them to eliminate the error, E. If $\beta = 1$ in Equation 32 $V_{OUT} = V_{IN}$, or the feedback circuit has turned into a unity gain buffer. If $\beta = 0$ in Equation 32 $V_{OUT} = AV_{IN}$, or there is no feedback. Notice that the direct gain, A, does not control the feedback circuit closed loop gain; rather, the feedback factor, β, controls the closed loop gain in a feedback circuit. This is the essence of a feedback circuit; now the closed loop gain is a function of the feedback factor which is comprised of passive components. The closed loop gain error, stability and drift are now dependent on stable, accurate, and inexpensive passive components. The closed loop gain assumption is valid as long as $A\beta >> 1$, also $E \Rightarrow 0$ if this assumption is valid.

If $A\beta = -1$ then Equation 32 becomes $V_{OUT}/V_{IN} = 1/0$, or it is indeterminate. If the energy in the circuit was unlimited the circuit would consume the world, but luckily it is limited, so the circuit oscillates from positive to negative saturation. This is an oscillator, thus the definition of an oscillator is that the gain be ≥ 1 while the phase shift equals -180 degrees. Now we conclude that the feedback factor controls the closed loop gain, and the direct gain/feedback factor combination determines if the circuit will be stable or will be an oscillator.

The Op Amp Symbol

It is important to understand the op amp symbol shown in Figure 13. The -input, V-, is the inverting input, and the +input, V+, is the non-inverting input. The point of the triangle is the op amp output, and the op amp multiplies the differential voltage, (V+ - V-), by a large gain, a.

The Inverting Op Amp

Three assumptions are made in the calculation of the inverting op amp circuit equations. First, the current into the op amp inputs, I_B in Figure 13, is assumed to be zero; this is a valid assumption because the bias currents are usually much lower than signal currents. The second assumption is that the op amp gain, a, is extremely high, and this is a valid assumption in most situations where the op amp's bandwidth is much greater than the signal bandwidth. The third assumption, which is that the error voltage, V_E, equals zero, is a result of assuming an extremely high op amp gain. When a is very large V_{OUT}, can assume any value required to drive the inverting input voltage to the non-inverting input voltage, so V_E will always be forced to zero.

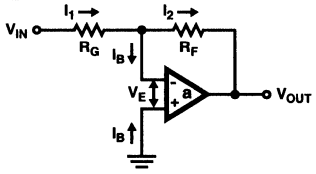


FIGURE 13. INVERTING OP AMP CIRCUIT

Assume $I_B = 0$, $V_E = 0$, $a = \infty$
Then:

$$I_1 = \frac{V_{IN}}{R_G} = I_2 = -\frac{V_{OUT}}{R_F} \quad \text{(EQ. 33)}$$

$$V_{IN} R_F = -V_{OUT} R_G \quad \text{(EQ. 34)}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G} \quad \text{(EQ. 35)}$$

Equation 33 is written by applying Kirchoff's current law to the inverting node. Equation 35 is obtained through algebraic manipulation of Equations 33 and 34. Note that the ideal closed loop gain, Equation 33, does not contain the op amp gain, so it is independent of the op amp gain so long as the assumptions are valid.

The inverting op amp can be configured as an inverting adder as shown in Figure 14. The analysis is similar to that shown for the inverting amplifier, but it is easier to understand if the concept of a virtual ground is understood. Virtual is defined as "existing or resulting in effect though not in actual fact". The inverting node acts as a real ground because no voltage is developed across it, but the current path is restricted to the PC traces attached to the node. The non-inverting input of the op amp is connected to ground, thus if the error voltage is to be zero as was assumed, the inverting input functions as though it were tied to ground. Considering the virtual ground, the three currents flowing through R_{G1}, R_{G2}, and R_{G3} can be calculated separately. Now superposition can be applied to the circuit; Equation 36 calculates the gain for each independent source, and Equation 37 recombines the separate gains.

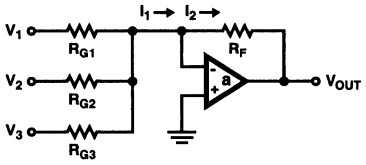


FIGURE 14. THE INVERTING ADDER

$$V_{01} = -V_1\frac{R_F}{R_{G1}},\ V_{02} = -V_2\frac{R_F}{R_{G2}},\ V_{03} = -V_3\frac{R_F}{R_{G3}} \quad \text{(EQ. 36)}$$

$$V_{OUT} = V_{01} + V_{02} + V_{03} = -V_1\frac{R_F}{R_{G1}} - V_2\frac{R_F}{R_{G2}} - V_3\frac{R_F}{R_{G3}} \quad \text{(EQ. 37)}$$

If $R_F / R_{GX} = 1$ Then;

$$V_{OUT} = -(V_1 + V_2 + V_3) \quad \text{(EQ. 38)}$$

The Non-Inverting Op Amp

Referring to Figure 15, because V_E is equal to zero the voltage at point X is equal to V_{IN}. There is voltage divider formed by the feedback resistor, R_F, and the gain setting resistor, R_G, and the voltage divider input voltage is the output voltage of the op amp. Equation 39 is written using the voltage divider rule, and Equation 40 is obtained through algebraic manipulation. Notice that the ideal closed loop gain is again independent of the op amp gain.

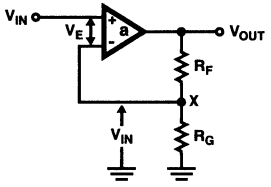


FIGURE 15. NON-INVERTING OP AMP

$$V_{IN} = \frac{V_{OUT} R_G}{R_F + R_G} \quad \text{(EQ. 39)}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_F + R_G}{R_G} \quad \text{(EQ. 40)}$$

The Differential Amplifier

The differential amplifier schematic is given in Figure 16, and the analysis will be done in two parts because we will use superposition. Two output voltages, one corresponding to each input voltage source, will be calculated separately and added together. The output from V_1 is calculated in Equation 42; V+ is first calculated with the voltage divider rule, and then it is substituted into the non-inverting gain equation yielding Equation 43. The output from V_2 is calculated from the inverting gain equation in Equation 44. The

results of Equations 43 and 44 are added in Equation 45 to obtain the complete circuit equation. Notice that the output is a function of the difference between the two input voltages, this accounts for the name differential amplifier.

If a small signal is riding on a large signal, say 10mV, 0.001Hz riding on $5V_{DC}$, the DC can be stripped off by putting the combined signal into the non-inverting input, and putting $5V_{DC}$ into the inverting input. The $5V_{DC}$ becomes a common mode signal (a signal which is common to both inputs), so it is rejected by the differential amplifier if $R_1 = R_3$, and $R_2 = R_4$.

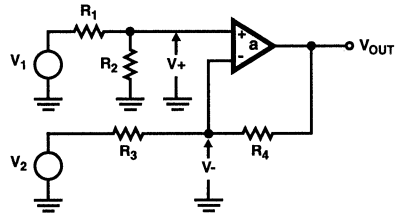


FIGURE 16. THE DIFFERENTIAL AMPLIFIER

$$V_{OUT} = V_{OUT_1} + V_{OUT_2} \quad \text{(EQ. 41)}$$

$$V_{OUT_1} = V+\left(1+\frac{R_4}{R_3}\right) \quad V+ = V_1\frac{R_2}{R_1+R_2} \quad \text{(EQ. 42)}$$

$$V_{OUT_1} = V_1\frac{R_2}{R_1+R_2}\left(\frac{R_3+R_4}{R_3}\right) \quad \text{(EQ. 43)}$$

$$V_{OUT_2} = V_2\left(-\frac{R_4}{R_3}\right) \quad \text{(EQ. 44)}$$

$$V_{OUT} = V_1\frac{R_2}{R_2+R_1}\left(\frac{R_3+R_4}{R_3}\right) - V_2\frac{R_4}{R_3} \quad \text{(EQ. 45)}$$

If $R_1 = R_3$ and $R_2 = R_4$

$$V_{OUT} = (V_1 - V_2)\frac{R_4}{R_3} \quad \text{(EQ. 46)}$$

This effect could be accomplished through the use of a coupling capacitor, but because the frequency of the signal is so low the capacitor value and size would be too big. The differential amplifier also rejects AC common mode signals. Data transmission schemes often use twisted pairs for the interconnections so that any noise coupled on the lines will be common mode. Differential amplifiers are used as receivers in this data transmission scheme because they reject the common mode noise while amplifying the signal.

T Networks in the Feedback Path

Putting a T network in the feedback path as shown in Figure 17 complicates the analysis, but offers the advantage of high closed loop gain coupled with low value feedback resistors. This configuration is also useful for some filter configurations. Thevenin's theorem is applied as shown in Figure 18. Look into R_4 from X, Y and calculate the Thevenin equivalent voltage and resistance, then redraw the circuit as shown in Figure 18. Now the inverting gain can be calculated in the normal manner using the algebraic simplification shown in Equation 48.

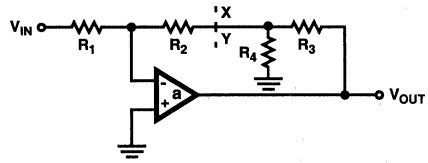


FIGURE 17. T NETWORK IN THE FEEDBACK PATH

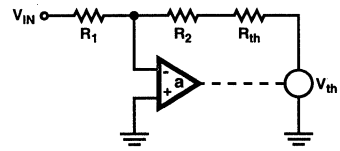


FIGURE 18. THEVENIN ANALYSIS OF T NETWORKS IN THE FEEDBACK PATH

$$V_{th} = \frac{V_0 R_4}{R_3+R_4} \quad R_{th} = R_3 \| R_4 \quad -\frac{V_{th}}{V_{IN}} = \frac{R_2+R_{th}}{R_1} \quad \text{(EQ. 47)}$$

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R_2+R_{th}}{R_1}\frac{R_3+R_4}{R_4} = \frac{R_2+\dfrac{R_3R_4}{R_3+R_4}}{R_1}\frac{R_3+R_4}{R_4}$$

$$= \frac{R_2+R_3+\dfrac{R_2R_3}{R_4}}{R_1} \quad \text{(EQ. 48)}$$

Video Amplifiers

Until now we have implicitly assumed that all op amps are the same. This is not true, but because the ideal closed loop equations are identical, it is a workable assumption. The two big classifications of op amps are voltage feedback and current feedback. The type of feedback is not the only difference between these op amps. The internal circuit configurations are dramatically different, so much so that recommended reference #1 dwells on voltage feedback while reference #2 dwells on current feedback. Whenever an op amp is used in a high frequency circuit such as a video amp there is a strong likelihood that it will be a current feedback op amp. Again, because the closed loop ideal gain equations are identical for voltage and current feedback op amps we will not distinguish between them.

In Figure 19, R_{IN} is usually the terminating resistance for the input cable, and it is usually 50Ω or 75Ω. R_M is the matching resistance for the cable being driven, and R_T is the terminating resistance for the driven cable. R_T is often shown here for gain calculations while it is physically placed at the cable end. Using Equation 49, we see that when $R_G = R_F$ and $R_M = R_T$, the overall circuit gain is one.

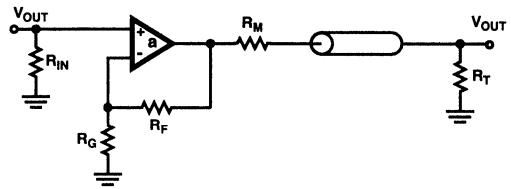


FIGURE 19. A TYPICAL VIDEO AMPLIFIER

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_F + R_G}{R_G}\,\frac{R_T}{R_M + R_T} \qquad \text{(EQ.49)}$$

AC Theory

The emphasis here is on capacitors because they are responsible for the vast majority of AC effects. The capacitor has an impedance and a phase shift both of which are a function of frequency. Although it is paramount in stability calculations, we will neglect the phase shift because you can obtain a reasonable understanding of circuit performance by just considering the impedance. Referring to Equation 50 it is apparent that when the frequency is very high, $s = j\omega$ is very high, so the capacitor impedance, X_C, is very low. The converse happens when the frequency is very low.

The key to this section of AC theory is that high frequency means low capacitive impedance, and low frequency means high capacitive impedance. At $F = \infty$, $X_C = 0$, and at $F = 0$, $X_C = \infty$. At intermediate values of frequency the capacitive impedance must be calculated with the assistance of Equation 50.

FIGURE 20. CAPACITOR IMPEDANCE

$$X_C = \frac{1}{SC} = \frac{1}{j\omega C} \qquad \text{where } S = jw \text{ and } j = \sqrt{-1} \qquad \text{(EQ.50)}$$

Op Amp Circuits Containing Capacitors

Referring to Figure 21, when $F = 0$, $X_C = \infty$ so the gain, $G = -R_F/R_G$. When $F = \infty$, $X_C = 0$ then $G = 0$. The gain starts off high and decreases to zero at very high frequencies. Very often C_F is an unwanted stray capacitor which yields an undesirable effect; namely, the circuit loses high frequency performance.

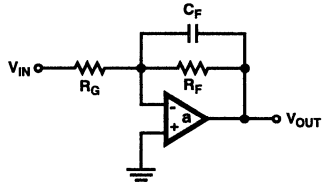


FIGURE 21. LOW PASS FILTER

A high pass filter is shown in Figure 22. At $F = 0$ the gain is $(R_F + R_G)/R_F$, and at very high frequencies the gain tries to approach the op amp gain, a. Sometimes the stray input capacitance forms this circuit, and the result is unwanted peaking or overshoot because the capacitor phase shift tends to make the circuit unstable.

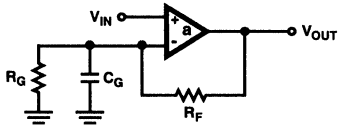


FIGURE 22. HIGH PASS FILTER

This general method is useful for analyzing the performance of op amp circuits which have capacitors. Depending on where they are connected the capacitors can stabilize or destabilize the op amp, but they always shape the transfer function in the frequency domain.

Conclusion

Some algebra, the basic laws of physics, and the basic circuit laws are adequate to gain an understanding of op amp circuits. By applying these tools to various circuit configurations it is possible to predict performance. Further in-depth knowledge is required to do op amp design, and there are many sources where this knowledge can be obtained. Don't hesitate to try some of these tricks on your local circuit design engineer, but be aware that it may result in a long lecture about circuit design.

References

[1] Harris Semiconductor, Application Note 9415, Author: Ronald Mancini, 1994.

[2] Harris Semiconductor, Application Note 9420, Authors: Ronald Mancini and Jeffrey Lies, 1995.

[3] Van Valkenberg, N.E., Network Analysis, Prentice-Hall, 1964.

Harris Semiconductor

APPNOTE

No. AN9513 October 1996

Harris Linear

Component Video Sync Formats (HFA1103)

Author: Chris Henningsen

Introduction

This application note will examine a variety of sync formats and a method for removing the sync pulse from component video signals (see Figure 1). The HFA1103 is a Video Op Amp with an open emitter NPN transistor output stage that is ideal for video signal amplification and sync stripping functions. This product was developed for video design engineers who need to remove sync from component RGB (red, green, blue) and monochrome RS-170 video data (see Figure 7). Recently the term RGB has been turned around and called GBR (green, blue, red) as video distribution systems normally put green on channel 1, blue on channel 2 and red on channel 3. This is consistent with the hook-up of the color difference standards.

TABLE 1. RGB STANDARDS SPECIFICATIONS (BROADCAST ENGINEERING 11/94)

	SMPTE/ EBU N10	NTSC (NO SETUP)	NTSC (SETUP)
Max	700mV	714mV	714mV
Min	0mV	0mV	54mV
Range	700mV	714mV	660mV
Sync	-300mV	-286mV	-286mV
Peak-To-Peak	1V	1V	1V

Table 1 lists standards specifications for SMPTE and NTSC video signals. All have $1V_{P-P}$ signals with sync signals ranging from -286mV to -300mV. A typical $1V_{P-P}$ video signal consists of up to +700mV of active video on top of a -300mV sync pulse. The application circuit shown in Figure 2 will strip off the sync pulse and transmit only the positive video data. See the Harris Application Note AN9514 titled "Video Amplifier with Sync Stripper and DC Restore" for additional details on this circuit. This circuit is useful in a variety of video processing applications such as; RGB video digitizing, RGB video distribution amplifiers for workstations and PC networks, and RGB monitor preamplifiers. When digitizing RGB video it is not necessary to digitize the sync pulse, so removing sync allows the full dynamic range of the A/D converter to be used on just the video data, resulting in a 30% increase in image resolution. In video distribution amplifiers, which are driving a number of video channels, it is undesirable to require separate switching channels for the sync signals. Sync is generally combined with the video signal, resulting in lower system costs by minimizing the total number of switching channels required. Certain applications, such as some RGB monitors, can't handle sync on the video signal and it must be stripped off, usually by a stage on the output of the distribution amplifier. Now that we know some of the applications where sync removal is important, let's look at why and where sync signals are used.

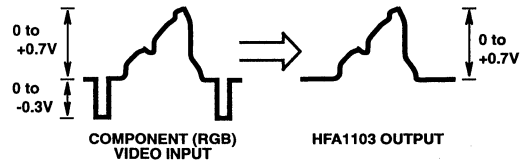


FIGURE 1. SYNC STRIPPER WAVEFORMS

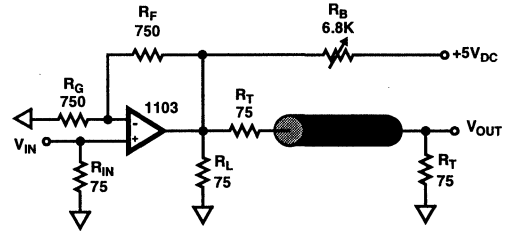


FIGURE 2. HFA1103 APPLICATION CIRCUIT VIDEO AMPLIFIER WITH SYNC STRIPPER

Transmitting two-dimensional moving pictures electronically requires the handling of a large amount of information and this is done by slicing the 2-D picture into horizontal strips of video and sending them sequentially. At the receiving end, or video monitor, the video information is recreated in scan lines on the display screen. This process continues until all of the scan lines needed for the picture are complete. Each complete picture refresh is called a frame, and typical frame refresh rates vary from 25 to 30 frames/s for broadcast video up to 72 frames/s in high performance video systems.

Sync signals are used to ensure that the scan lines are correctly placed on the display screen. A horizontal sync pulse is used to indicate the end of each scan line and signals the mon-

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itor to return to the left edge of the screen to begin the next scan line, below the one just completed. A vertical sync pulse is used to tell the monitor that the bottom of the picture has been reached, and that the next scan line will start at the top again. This is similar to a carriage return on a typewriter, where a scan line is equivalent to a single line of text and a frame of video is equivalent to a complete page of text (see Figure 3).

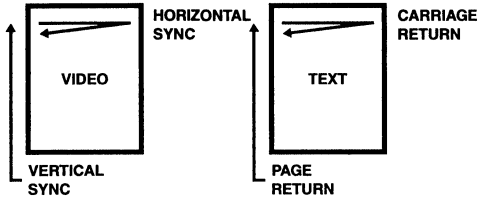

FIGURE 3. HORIZONTAL AND VERTICAL SYNC IS ANALOGOUS TO TEXT CARRIAGE RETURN AND END OF PAGE

The scan lines are formed by moving a spot of light, scanning left to right and top to bottom, in a pattern called a raster. As the spot traces out the raster pattern, it is modulated by the video signal to form the picture. Monochrome (black and white) systems require just one video signal, plus the horizontal (H) and vertical (V) sync pulses, for a total of three signals. Color computer systems require one signal each for red, green and blue, plus V and H sync pulses for a total of five signals. There are a variety of techniques used to reduce the number of wires needed to transmit these five signals.

Computer Systems

In computer systems the monitor is generally located close to the CPU and separate wires can be used for Red, Green, Blue and Horizontal and Vertical sync signals. It is common for monitors to be hooked up using a single connector housing the five separate wires. This approach is referred to as RGBHV. As the distance between the monitor and the computer increases, it is more convenient and less costly to use fewer wires. Combining both the horizontal and vertical sync into a single composite sync signal results in a four wire system, eliminating one wire. This approach is referred to as RGBS, where S is the composite sync signal. RGBS system monitors contain circuits to recreate the horizontal and vertical sync signals from the composite sync. Another wire can be eliminated by combining sync with a video channel. This is possible because sync pulses only occur between scan lines (horizontal sync) and between frames (vertical sync), when video signals are not present. Typically the composite sync is carried by the green channel and this 3-wire system is referred to as RGsB or SOG for sync-on-green. RGsB system monitors have circuits to identify composite sync from the RGsB video and to separate it into its horizontal and vertical sync components. In some cases sync is combined with all three color channels; red, green and blue, and is referred to as RsGsBs. We have now discussed how to transmit video using 5 wire RGBHV, 4 wire RGBS and 3 wire RGsB approaches (see Figure 4), with the major differences being the way in which the horizontal and vertical sync signals are handled. Using fewer wires is an obvious advantage in applications with long cable lengths between the computer and monitor. Many multisync monitors accept all three formats of RGB and sync, as they have circuits to adapt automatically to the type of RGB signal present. Other monitors are designed to work specifically with one of the RGB formats and the sync must be removed from green in RGsB or from all three channels in RsGsBs before driving the monitor. This is one of the primary applications for the HFA1103 video op amp with sync stripper.

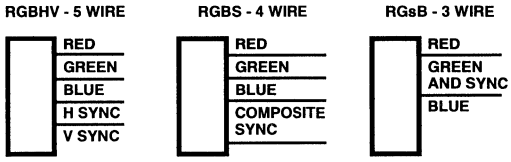

FIGURE 4. WIRES REQUIRED FOR RGBHV vs RGBS vs RGsB VIDEO

Now let's see if we can further reduce the number of wires by doing something with the way we transmit video. RGB video signals can be color space transformed into a separate black and white (monochrome) picture plus two additional pictures that describe the difference between the monochrome picture and the full color representation. The monochrome picture is called "luminance", and is referred to as "Y". The pair of color difference pictures are referred to as "U" and "V". This YUV video signal can be color space transformed back into RGB, if needed. The advantage of the YUV signal is that it reduces the transmission and storage requirements in video transmission and distribution systems, as the total amount of video information is reduced. This is due to the fact that the human eye does not need as much color difference information as it does luminance information. Now the color difference information "U" and "V" can be combined into a single "chrominance" signal, referred to as "C". We have now reduced the signal total to two wires. A new type of sync signal must be included so the video monitor can separate the two color difference signals again. This new sync information is called color burst, and is added to the chrominance, "C", just after each horizontal sync pulse. The "Y" channel carries the composite sync information.

S-VHS videotape is the most popular YC format.

Television Broadcast Systems

Television Broadcast Systems must take the five original signals (R, G, B, H, and V) and transmit them through a single transmitter. Here luminance "Y" and chrominance "C" are combined into a single video signal called composite video. Broadcast video systems are required to be compatible with monochrome and color receivers, and black and white receivers only need to process the Y portion of the signal. The broadcast standard in North and Central America, Korea, Taiwan and Japan is called NTSC and uses a 3.58MHz color subcarrier. Europe, Australia and the Middle East use PAL while France and Russia use SECAM, both 4.43MHz color subcarriers (Figures 5 and 6). Note that the application circuit for video sync stripping, shown in Figure 2,

is not useful for composite video applications, as some of the color information (blue) resides below the black level (Figures 7 and 8) and would be lost by the sync stripping function.

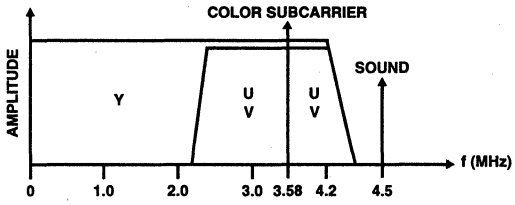

FIGURE 5. NTSC SYSTEM BANDWIDTH

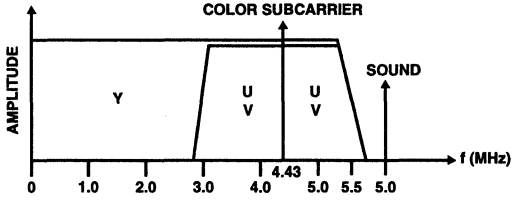

FIGURE 6. PAL SYSTEM BANDWIDTH

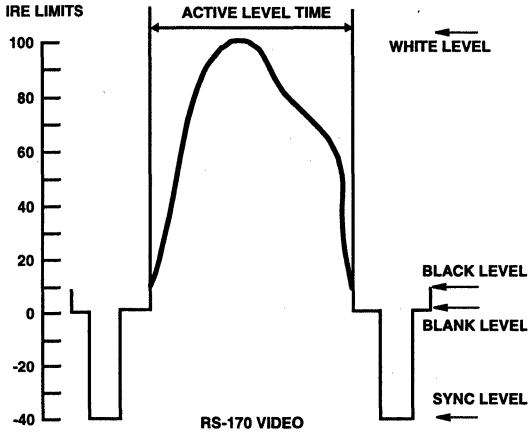

FIGURE 7. MONOCHROME VIDEO STANDARD

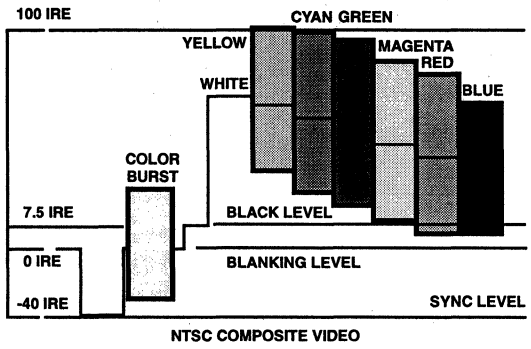

FIGURE 8. COMPOSITE VIDEO STANDARD

References

[1] Harris Semiconductor, High Speed Signal Processing Seminar, 1994 (Publication #BR-043A)

[2] Lies, Jeff and Henningsen, Chris, "Video Amplifier With Sync Stripper and DC Restore", Harris Semiconductor Application Note AN9514 April 1995

[3] Epstein, Steve, Component Analog Video - So Many Standards, Broadcast Engineering, Nov. 1994

[4] Atwood Research Inc., Video Sync Formats, Application Note #3, 1994

APPNOTE

No. AN9514 June 1995

Video Amplifier with Sync Stripper and DC Restore (HFA1103)

Authors: Jeff Lies and Chris Henningsen

Introduction

The circuit in Figure 1 transmits 200MHz (-3dB bandwidth) video signals while stripping off the sync pulse and performing DC restoration. It is configured for a typical video cable driver application driving a double-terminated 75Ω load, where the HFA1103 (IC3) is configured for a gain of +2 to ensure unity gain throughout.

Sync Stripping

In component video systems it is frequently necessary to remove the sync pulse from an RGB signal. Sync is often combined with one or more of the red, green, and blue video signals in video distribution amplifiers, routers and switchers to decrease the number of input and output channels required in a switching network. In many applications, however, as the video signals exit the switching network the sync pulse must be removed.

The HFA1103 video op amp is specially designed to perform sync stripping. Its open emitter NPN output forms an emitter-follower with the load resistor, and passes the active video signal while virtually eliminating the negative sync pulse (see Figure 2). Residual sync of the HFA1103, defined as the remainder of the original -300mV sync pulse, referenced to ground, is only 8mV at the cable output. A particular advantage of sync stripping with the HFA1103 is the resultant larger (by 0.7V) output voltage swing, compared to simply using a wideband video op amp with an external emitter-follower.

Because the HFA1103 contains no active pull-down, output linearity degrades as the signal approaches ground. To deal with this a 6.8kΩ pull-up resistor (R_8) and a 75Ω pull down resistor (R_{10}) on the output ensure a fixed positive voltage offset, in this case +50mV. This offset was arbitrarily chosen as a good compromise between linearity near the DC level and minimum residual sync. Increasing R_8 decreases residual sync, at the expense of linearity. Conversely, decreasing R_8 decreases linearity error, but increases residual sync.

Other applications benefitting from sync removal are HDTV systems and video digitizing circuits. Consider a typical $1V_{P-P}$ RGB video signal with a -300mV sync pulse and +700mV video data. By stripping off the unwanted sync

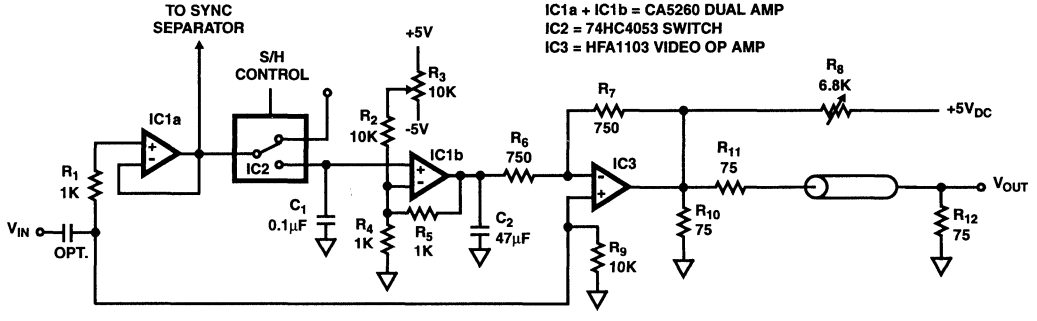

FIGURE 1. HFA1103 BASED VIDEO AMPLIFIER WITH SYNC STRIPPING AND DC RESTORE

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pulse and digitizing only the active video, designers can use the full dynamic range of the A/D converter for the +700mV video data. This results in a 30% increase in resolution using the same A/D converter.

DC Restore

Another common video function is DC restoration, used when AC coupled signals have lost their DC reference and must have it periodically reset in order to retain brightness information.

This circuit accomplishes DC restoration using a CA5260 dual op amp (IC1a, IC1b) coupled with a sample-and-hold circuit based on the 74HC4053 switch (IC2). V_{IN}, consisting of the input video signal and a DC offset (V_{DC}), is routed to the non-inverting input of the HFA1103 (IC3). The HFA1103 is configured in a gain of +2 (to compensate for the attenuation resulting from double terminating the cable), which would result in an output of 2 x V_{IN} = (2 x Video + 2 x V_{DC}), if not for the DC restore circuit.

V_{IN} also travels through half of the dual CA5260 amplifier to the sample-and-hold circuit, where the 0.1µF capacitor (C_1) is the hold capacitor. The sample-and-hold control is triggered by a back-porch pulse from a sync separator or by a horizontal video blanking signal. The DC output signal (V_{DC}) from the sample-and-hold circuit is then amplified at a gain of +2 by the second op amp (IC1b); the gain is required because V_{DC} is input to the HFA1103s inverting input which provides only a gain of -1, but as discussed earlier, the output contains a term of 2 x V_{DC}. Thus 2 x V_{DC} is summed into the HFA1103 inverting input, is subtracted from the output signal, and yields a DC restored video signal.

Because the output impedance of IC1b is high, and would affect the gain at the non-inverting input of the HFA1103, a 47µF capacitor (C_2) is used to provide an AC ground and to maintain good high-frequency gain accuracy.

A potentiometer (R_3) is used prior to IC1b to null out any offset voltage contributed by the DC restore circuitry.

Conclusion

The circuit's resultant output is a 200MHz, DC restored video signal in which the sync pulse has been stripped to a residual level of no more than 8mV.

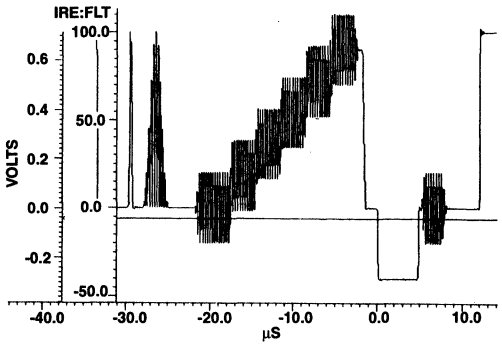

FIGURE 2A. VIDEO AND SYNC GO IN

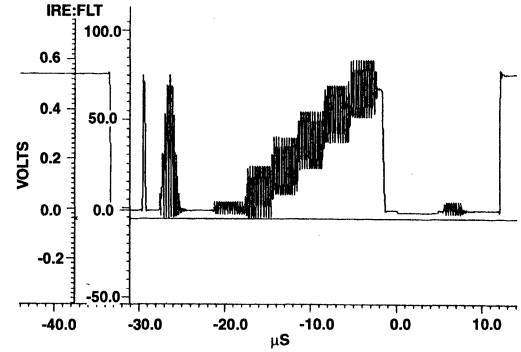

FIGURE 2B. ONLY VIDEO COMES OUT

FIGURE 2. SIGNALS AT HFA1103 INPUT AND CABLE OUTPUT

APPNOTE

No. AN9515.1 November 1996

Harris Linear

Multiplier Improves the Dynamic Range of Echo Systems (HA-2556, HA-5177)

Author: Ron Mancini

Introduction

In an echo system the returned signal amplitude is a function of the distance to the target, and it can be expressed mathematically as function of time. An echo system with a fixed gain preamp has poor dynamic range because close targets (short return times) have high signal amplitudes while distant targets (long return times) have much lower signal amplitudes. In fixed gain systems, the biggest signals establish the upper preamp gain limit based on not saturating the system, and this gain may not be high enough to process small returns properly.

The solution is a preamplifier which has a gain proportional to time, such that the gain will be small for close targets and large for distant targets. The preamp still has to meet all the other normal preamp criteria such as bandwidth and noise performance, and the added time dependent gain function must not degrade the signal. The circuit shown in the figure implements the variable gain preamp with the Harris Semiconductor HA-2556 multiplier. This IC establishes the signal bandwidth and noise figure because it is the only component in the signal path. The equation for the multiplier gain, as shown in the accompanying figure, is given below:

$$V_{OUT} = \frac{V_X V_Y}{5}\left(\frac{R_7}{R_8} + 1\right) = 10V_X V_Y$$

The HA-5177 and its associated circuitry comprise a constant current source whose current is $V_{D1}/R_2 = I = 51\mu A$. If S_1 is in the L_{IN} position with Q_2's gate held high, the current source is shorted to ground by Q_2 and the multiplier gain is set to zero. When the received signal from the closest target can be present, Q_2's gate is brought low forcing it into a very high drain resistance state (almost an open circuit) allowing the HA-5177 current to charge C_1 in a linear manner. The voltage across C_1 ramps up from 0V to 5V in 1ms which is the time it takes sound to travel approximately one foot through air. During the first portion of the ramp, when the returned signal is very large, the multiplier gain is small because V_X is small. As time increases V_X also increases providing more gain through the multiplier as the expected echo decreases in amplitude. Thus, the output voltage swing of the multiplier tends to stay constant for large changes in input signal, and the dynamic range is improved to the amount of the ramp change, which is more than 60dB with the values shown in Figure 1.

Often the returned signal is a nonlinear function and it may be desirable to linearize it. An inverse nonlinear ramp can be employed to linearize the overall function. R_3, R_4 and C_1 generate a logarithmic ramp when S_1 is in the Log position thus yielding a logarithmic gain function adequate for linearizing some transducers. Many other time-gain transfer functions can be generated by employing different types of ramps.

It is important to eliminate the multiplier offsets with the adjustments [1] provided because offsets will appear in the output signal, reduce the dynamic range and contribute errors. As the circuit is configured it will sweep from a gain of 0.01, as the ramp begins, to 10 as the ramp ends. Returned signal amplitude is usually small but should not exceed $100mV_{P-P}$ unless distortion can be tolerated. The circuit bandwidth can be as high as 57MHz in low gain applications, and is 5MHz as configured.

References

[1] Wideband Four Quadrant Voltage Output Analog Multiplier Data Sheet HA-2556, File Number 2477, Harris Semiconductor, Melbourne, Florida

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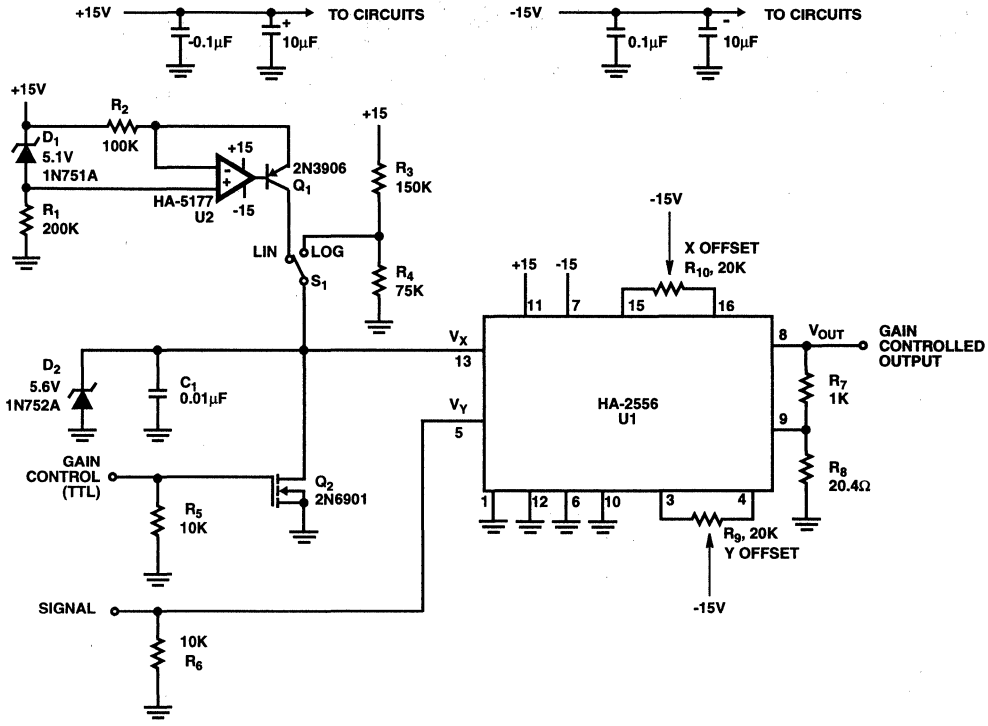

FIGURE 1. MULTIPLIER IMPROVES DUAL RANGE OF ECHO SYSTEMS

APPNOTE

No. AN9516.1 June 1996

Harris Linear

Adjustable Bandpass or Bandreject Filter (HA-2841)

Author: Ron Mancini

Introduction

The filter described here has an easily adjustable center frequency, symmetrical skirts and an attenuation (gain) of -40(+40)dB at an octave either side of the center frequency (f_C). The filter Q ($Q = f_C/BW3dB \cong 250$) does not vary significantly when the center frequency is changed, thus, the shape of the skirts is essentially independent of the pot setting. This feature yields filters that can be adjusted over a much wider frequency range than "T" type filters, the only other type of filter with such a deep notch or narrow bandpass. Now one filter type is useful in many designs. The calculation of the center frequency for the circuits shown in Figure 1 and Figure 2 is given in Equation 1 and Equation 2.

$$f_C = \frac{1}{2\pi C\sqrt{3R_1R_2}} \quad \text{(EQ. 1)}$$

Where $R_1 = R_{1A} + \alpha R_P$

$R_2 = R_{2A} + (1-\alpha)R_P$

$$R_3 = 6(R_1 + R_2) \quad \text{(EQ. 2)}$$

A basic theorem of feedback circuits is that a function generator included in a negative feedback loop computes the inverse function at the output. This approach has been used to change an excellent bandreject filter into an excellent bandpass filter. The schematic of the bandreject filter, which is passive and comprised of C, R_1, R_2 and R_3 is shown in Figure 1. The bandpass filter, which includes the passive network in the feedback loop, is shown in Figure 2. The bandpass filter has the advantage of high input impedance and low output impedance because of the location of the op amp. With the values shown the center frequency is adjustable from 55kHz to 550kHz producing a decade of frequency adjustment. The Harris Semiconductor HA-2841 op amp is chosen as the amplifier because it has good DC characteristics and has the high gain bandwidth required to achieve the bandpass gain without distorting the filter response. R_1 should be split into R_{1A} and R_{1B} to prevent R_1 from becoming zero, and the split may be selected to obtain maximum resolution over the desired center frequency range.

A PSPICE™ plot of the circuit using the SPICE Model for the HA-2841 is shown in Figure 3. The plots are the logarithmic transfer function of both the filters (in dB). Notice that the bandreject filter transfer function, represented by the diamonds, is the mirror image of the bandpass transfer function, represented by the squares. These transfer functions change very little when they are adjusted to 550kHz center frequency. Bench test results show some deviation from the PSPICE™ simulations because of component tolerances and layout capacitances, but generally they correlate well with the simulations. The transfer functions change radically and tend to degenerate at high frequencies if low gain bandwidth op amps are used.

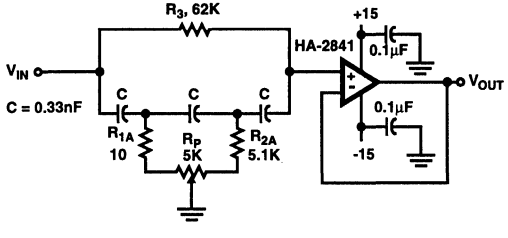

FIGURE 1. ADJUSTABLE BANDREJECT FILTER

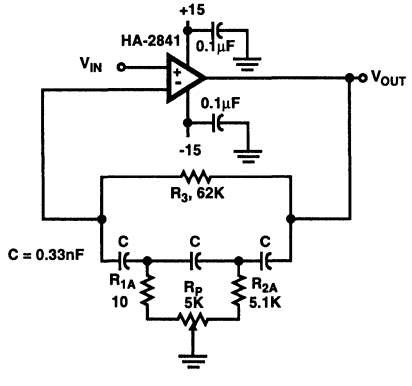

FIGURE 2. ADJUSTABLE BANDPASS FILTER

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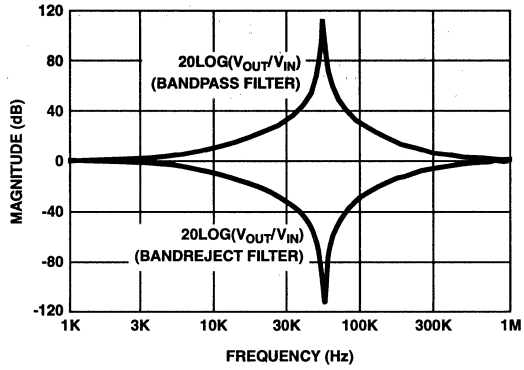

FIGURE 3. PSPICE PLOT OF FILTERS TRANSFER FUNCTION

Harris Semiconductor

APPNOTE

No. AN9523 January 1996

Harris Linear

Evaluation Programs for SPICE Op Amp Models

Authors: Ron Mancini and Jeff Lies

Introduction

There is no consistent method for evaluating SPICE models in the industry, so it is hard to reproduce a specific manufacturer's results or to compare models between manufacturers. Furthermore, many of the SPICE models available from vendors do not correlate the vendor's data sheet for the corresponding op amp; hence, there is confusion about the validity of the model, the evaluation program, and/or the data sheet. This paper includes a collection of SPICE programs that have been used to evaluate some of the latest Harris Semiconductor current feedback op amps. The programs illustrated here will be used to evaluate new Harris op amp designs, both current and voltage feedback, so they will serve as a standard until modified by common agreement. These programs have several advantages: they are written, they have been debugged, macros exist to eliminate the plotting effort, they cover the pertinent parameters, and they contain equations to normalize the output for "Bode" type plots.

Six programs which cover 13 parameters including: inverting gain, non-inverting gain, positive power supply current, negative power supply current, positive input bias current, negative input bias current,offset current, positive offset voltage, negative offset voltage, differential offset voltage, non-inverting common-mode voltage, transient response, and enable/disable response are used to evaluate the op amp. These thirteen parameters are displayed in eight plots which have seventeen curves.

Printed copies of these programs are given here, and electronic copies are available on the "Harris Semiconductor-Analog SPICE Macromodels" disk dated January 1996 or later.

AC Transfer Function For An Inverting Op Amp

The first program (see Figures 1, 2, and 3) is named cfaig.cir, and it simulates the AC transfer function for an inverting op amp. This program uses three op amps so it computes the transfer function for three different gains in one pass. The program requires the user to supply the feedback resistance values for each gain, the gain settings, the load resistance, the load capacitance, and the power supply voltage in volts. The program assumes that the op amp is run off two power supplies of equal and opposite polarity each of which is referenced to ground, so it applies the entered voltage to the op amp as a positive and negative supply with equal magnitudes. If a single supply op amp is to be evaluated with these programs just enter half the power supply voltage, and the analysis will be equivalent.

Unless the output is normalized the vertical scale will have to be large enough to accommodate the difference in gains, so small effects such as peaking may be hard to discern or measure. The program configures the load resistor as a voltage divider, and the output is taken at the voltage divider output. If the op amp gain is 10 the load resistor gain will be 0.1. If a load resistor is not required by the data sheet enter a large value such as 1000GΩ; the large resistor will not affect the circuit operation while the normalization feature is retained. Now the three curves will plot on top of each other similar to the GBW curves shown in most data books.

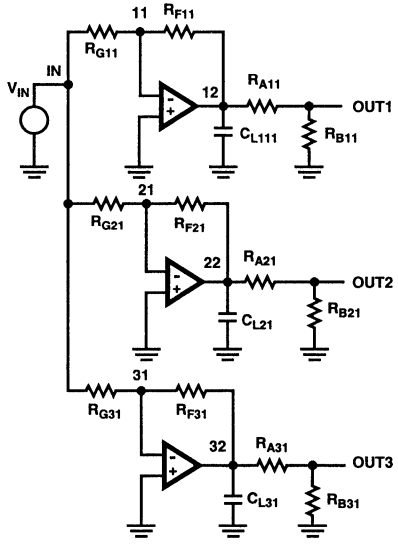

FIGURE 1. SCHEMATIC OF INVERTING OP AMP

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```
*This program simulates the AC transfer function for an inverting op amp.
*It has three op amps; each with a gain that is specified by the
*user with a .param statement. The user must specify the load RL, CL, the
*feedback resistors RF1, RF2, RF3 and the corresponding gains G1, G2, G3.
*The power supply voltage is set by the parameter "vsupply". The load resistors
*are automatically split into voltage dividers to normalize the gain plot,
*and the gains can be plotted in dB by calling the macros G1, G2, and G3.
*The inputs are tied together, and the outputs are called OUT1, OUT2, and
*OUT3 corresponding to the respective gains. The op amp model is entered with
*a .lib statement. The model in the subcircuit call (x statement) must correspond to the model
*called in the .lib statement (3 times).
.param CL=10pf
.param RL=400
.param RF1=750
.param RF2=750
.param RF3=750
.param G1=1
.param G2=2
.param G3=3
.param vsupply=5
.lib b:ha502x.cir
x1 0 11 3 4 12 3 ha502x
x2 0 21 3 4 22 3 ha502x
x3 0 31 3 4 32 3 ha502x
VIN in 0 ac 1
RF11 11 12 {RF1}
RF21 21 22 {RF2}
RF31 31 32 {RF3}
RG11 in 11 {RF1/abs(G1) }
RG21 in 21 {RF2/abs(G2) }
RG31 in 31 {RF3/abs(G3) }
RA11 12 OUT1 {RL* (abs(G1)-.99999) /abs(G1) }
RA21 22 OUT2 {RL* (abs(G2)-.99999) /abs(G2) }
RA31 32 OUT3 {RL* (abs(G3)-.99999) /abs(G3) }
RB11 0 OUT1 {RL/abs(G1) }
RB21 0 OUT2 {RL/abs(G2) }
RB31 0 OUT3  {RL/abs(G3) }
CL11 0 12 {CL}
CL21 0 22 {CL}
CL31 0 32 {CL}
VCC 3 0 {vsupply}
VEE 4 0 {-1*vsupply}
.ac dec 50 1meg 3000meg
.probe
.end
```

FIGURE 2. INVERTING OP AMP AC TRANSFER FUNCTION PROGRAM

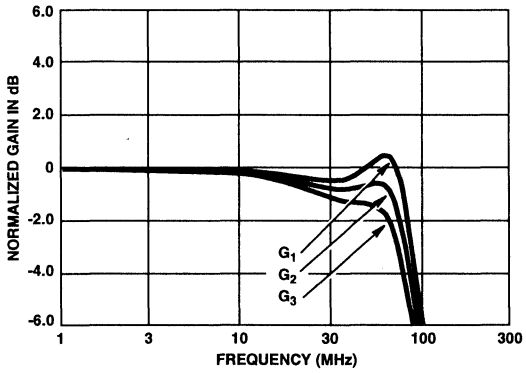


FIGURE 3. INVERTING OP AMP AC TRANSFER FUNCTION PLOT

AC Transfer Function for a Non-Inverting Op Amp

The second program (see Figures 4, 5, and 6) is named cfanig.cir, and it simulates the AC transfer function for a non-inverting op amp. This program uses three op amps so it can compute the transfer function for three different gains in one pass. The program requires the user to supply the feedback resistance values for each gain, the gain settings, the load resistance, the load capacitance, and the power supply voltage in volts. The program assumes that the op amp is run off two power supplies of equal and opposite polarity each of which is referenced to ground, so it applies the entered voltage to the op amp as a positive and negative supply with equal magnitudes. If a single supply op amp needs to be evaluated just enter half the power supply voltage, and the analysis will be equivalent.

Unless the output is normalized the vertical scale will have to be large enough to accommodate the difference in gains, so small effects such as peaking may be hard to discern or measure. The program configures the load resistor as a voltage divider, and the output is taken at the voltage divider output. If the op amp gain is 10, the load resistor gain will be 0.1. If a load resistor is not required by the data sheet enter a large value such as 1000GΩ; the large resistor will not affect the circuit operation while the normalization feature is retained. Now the three curves will plot on top of each other similar to the GBW curves shown in most data books.

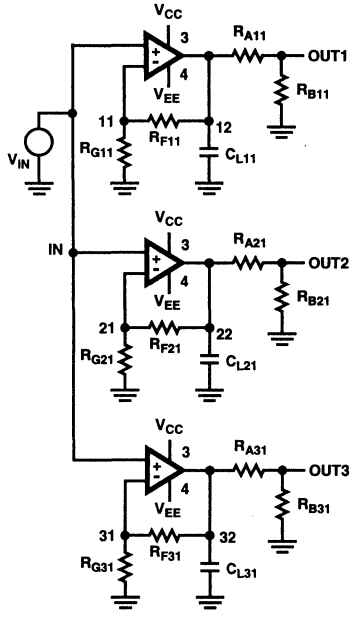


FIGURE 4. NON-INVERTING OP AMP SCHEMATIC

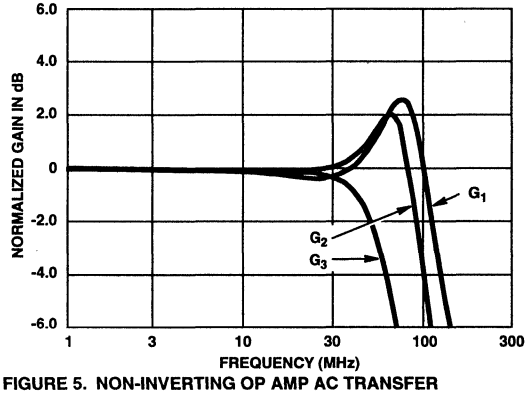


FIGURE 5. NON-INVERTING OP AMP AC TRANSFER FUNCTION PLOT

```
*This program simulates the transfer function for a non-inverting op amp.
*It has three op amps; each with a gain that is specified by the user
*with a .param statement. The user must specify the load RL, CL, the
*feedback resistors RF1, RF2, RF3 and the corresponding gains G1, G2, G3.
*The power supply voltage is set by the parameter "vsupply". The load resistors
*are automatically split into voltage dividers to normalize the gain plot,
*and they can be plotted in dB by calling the macros G1, G2 and G3.
*The inputs are tied together, and the outputs are called OUT1, OUT2, and
*OUT3 corresponding to the respective gains. The op amp model is entered with
*a .lib statement. The model in the subcircuit call (x statement) must correspond to the model
*called in the .lib statement (3 times).
.param CL=10pf
.param RL=400
.param RF1=1000
.param RF2=681
.param RF3=383
.param G1=1
.param G2=2
.param G3=10
.param vsupply=5
.lib b:ha502x.cir
x1 in 11 3 4 12 3 ha502x
x2 in 21 3 4 22 3 ha502x
x3 in 31 3 4 32 3 has02x
vin in 0 ac 1
RF11 11 12 {RF1}
RF21 21 22 {RF2}
RF31 31 32 {RF3}
RG11 0 11 {RF1/(G1-.99999) }
RG21 0 21 {RF2/(G2-.99999) }
RG31 0 31 {RF3/(G3-.99999) }
RA11 12 OUT1 {RL*(G1-.99999)/G1}
RA21 22 OUT2 {RL*(G2-.99999)/G2}
RA31 32 OUT3 {RL*(G3-.99999)/G3}
RB11 0 OUT1 {RL-(RL*(G1-.99999)/G1) }
RB21 0 OUT2 {RL-(RL*(G2-.99999)/G2) }
RB31 0 OUT3 {RL-(RL*(G3-.99999)/G3) }
CL11 0 12 {CL}
CL21 0 22 {CL}
CL31 0 32 {CL}
VCC 3 0 {vsupply}
VEE 4 0 {-1*vsupply}
.ac dec 50 1meg 3000meg
.probe
.end
```

FIGURE 6. NON-INVERTING OP AMP AC TRANSFER FUNCTION PROGRAM

DC Parameters For a Non-Inverting Op Amp

The third program (see Figures 7 through 11) is named cfadc.cir, and it simulates the salient DC parameters for a non-inverting op amp. The program requires the user to supply the feedback resistance values, the load resistance, and the power supply voltage in volts. The program assumes that the op amp is run off two power supplies of equal and opposite polarity each of which is referenced to ground, so it applies the entered voltage to the op amp as a positive and negative supply with equal magnitudes. If a single supply op amp needs to be evaluated just enter half the power supply voltage, and the analysis will be equivalent.

The input signal to the op amp is a DC sweep. The sweep input enables a data analysis at V_{IN} = 0V which is often a data book point, and the parameters can be evaluated at various other points of interest. The input currents can be examined by plotting the currents through the feedback resistor, R_F, and the input resistor, R_I. The difference between these currents is the input offset current. When the voltage is swept through zero the offset voltage for zero input voltage can be calculated. Either input offset voltage can be plotted by selecting the correct node voltage, or the differential input voltage can be plotted be selecting V(11)-V(13). The supply currents are plotted by selecting I(V_{EE}) or I(V_{CC}) for the negative and positive power supplies respectively.

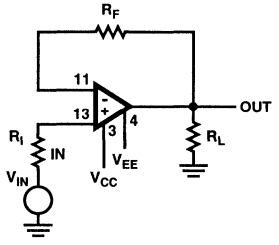


FIGURE 7. NON-INVERTING OP AMP SCHEMATIC (DC)

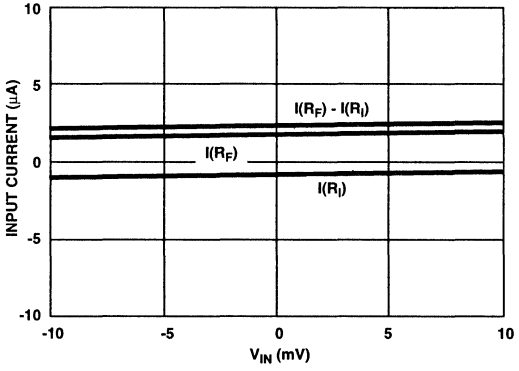


FIGURE 8. NON-INVERTING OP AMP INPUT CURRENT PLOT

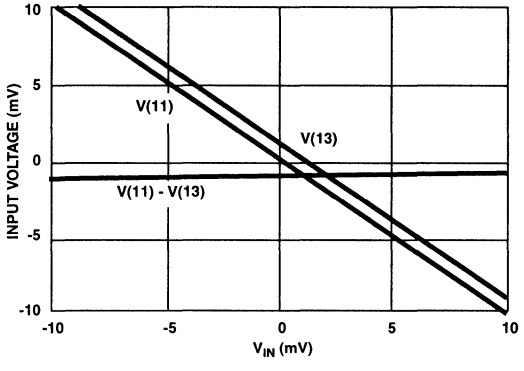


FIGURE 9. NON-INVERTING OP AMP INPUT OFFSET VOLTAGE PLOT

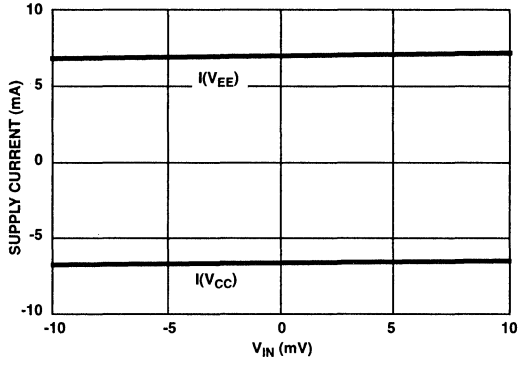


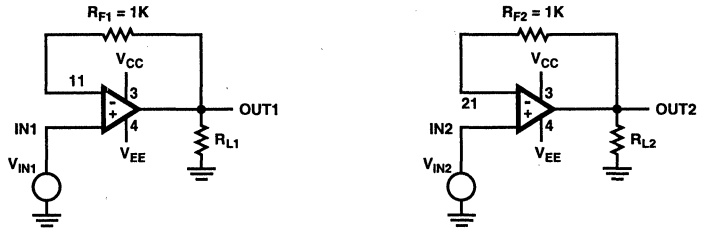
FIGURE 10. NON-INVERTING OP AMP POWER SUPPLY CURRENT PLOT

```
*This program simulates the salient DC parameters for a non-inverting op amp.
*The user must specify the feedback and load resistance with a .param
*statement. The power supply voltage is set by the parameter "vsupply". Input
*currents are measured as I_RI, the non-inverting input current, I_RF, the
*inverting input current, and (I_RF-I_RI) the offset current. The offset
*voltage is calculated with the equation Vos=v(13)-v(11). The power supply
*currents can be determined by looking at the parameter I_CC and I_EE. The
*model is entered with a .lib statement. The model in the subcircuit call (x statement)
*must correspond to the model called in the .lib statement.
.param R_F = 1000
.param R_L = 400
.param vsupply = 5
.lib b:ha502x.cir
x1 13 11 3 4 out 3 ha502x
V_IN in 0
R_F1 11 out {R_F}
R_I in 13 {R_F}
R_L1 0 out {R_L}
V_CC 3 0 {vsupply}
V_EE 4 0 {-1*vsupply}
.dc V_IN -.1 .1 .001
.probe
.end
```

FIGURE 11. NON-INVERTING OP AMP DC TRANSFER FUNCTION PROGRAM

CMRR For A Non-Inverting Op Amp

The fourth program (see Figures 12, 13, and 14) is called cfacmrr.cir, and it simulates the common mode rejection ratio for a non-inverting op amp. The program uses two identical non-inverting op amps to implement the equation CMRR = change in input offset voltage divided by the common mode input voltage change. The CMRR equation is shown in circuit parameters in Figure 12. Referring to Figure 13, it is seen that the common mode difference voltage is 2V. The input is a square wave so the measurement should be made in an area which has settled out. Notice that the worse common-mode input voltage is negative so that value of -1.3mV was used in the calculation. Using a square wave rather than a DC signal enables the inspection of both quadrants prior to calculating the CMRR. The program requires the user to supply the feedback resistance value, the load resistance, and the power supply voltage in volts.



$$CMMR = DB\frac{(V(IN1)-V(11))-(V(IN2)-V(21))}{(V(IN2)-V(IN1))} = DB\frac{\Delta V_{IO}}{\Delta V_{CM}}$$

FIGURE 12. SCHEMATIC AND EQUATION FOR COMMON-MODE REJECTION CIRCUIT

```
*This program simulates the common-mode rejection ratio for a non-inverting op
*amp. The equation recommended for the calculation is
*CMRR=dB((V(IN1)-V(11)) -(V(IN2)-V(21)))/(V(IN2)-(VIN1)) and this program uses
*two identical op amps to obtain the calculation data. The user
*must specify the feedback resistance, RF, and the load resistance, RL.
*The power supply voltage is set by the parameter "vsupply". The op amp model
*is entered with a .lib statement. The model in the subcircuit call (x statement) must
*correspond to the model in the .lib statement (2 times).
.param RF=1K
.param RL=400
.param vsupply=5
.lib b:ha502x.cir
x1 IN1 11 3 4 OUT1 3 ha502x
x2 IN2 21 3 4 OUT2 3 ha502x
VIN1 IN1 0 pulse (0 1m .1ns .1ns .1ns 100ns 200ns)
VIN2 IN2 0 pulse (0 2.001 .1ns .1ns.1ns 100ns 200ns)
RF1 11 OUT1 {RF}
RF2 21 OUT2 {RF}
RI1 OUT1 0 {RL}
RL2 OUT2 0 {RL}
VCC 3 0 {vsupply}
VEE 4 0 {-1*vsupply
.tran 20ns 420ns
.probe
.end
```

FIGURE 13. COMMON-MODE REJECTION PROGRAM

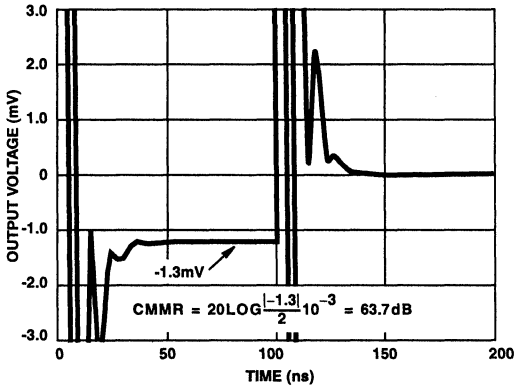


FIGURE 14. PLOT OF COMMON-MODE REJECTION PROGRAM OUTPUT

Transient Response For A Non-Inverting Op Amp

The fifth program (see Figures 15, 16, and 17) is called cfatran.cir, and it simulates the transient response for a non-inverting op amp. If the input signal is small, about 100mv as shown in Figure 16, the analysis will be small signal. Larger input signals will yield a large signal analysis. The program requires the user to supply the feedback resistance, the load resistance, the input resistance, and the power supply voltage in volts. The program assumes that the op amp is run off two power supplies of equal and opposite polarity each of which is referenced to ground, so it applies the entered voltage to the op amp as a positive and negative supply with equal magnitudes. If a single supply op amp needs to be evaluated just enter half the power supply voltage, and the analysis will be equivalent. The rise time, fall time, slew rate, and delay time can be read off the plot shown in Figure 16.

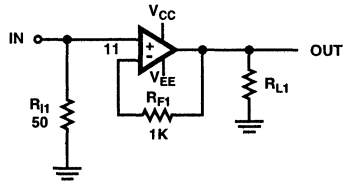


FIGURE 15. TRANSIENT RESPONSE CIRCUIT SCHEMATIC

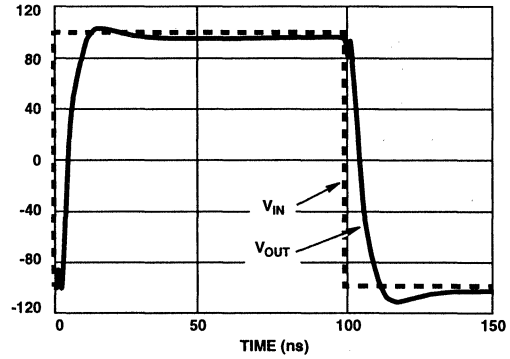


FIGURE 16. TRANSIENT RESPONSE PROGRAM OUTPUT PLOT

```
*This program simulates the time domain response for a non-inverting op amp.
*The response will be small signal or large signal depending on the amplitude
*of the input signal. The user must specify the load resistance, RL, the
*feedback resistance, RF, and the input resistance, RI. The power supply
*voltage is set by the parameter "vsupply". The op amp model is entered with
*a .lib statement. The model in the x statement must correspond to the
*model called in the .lib statement.
.param RI = 50
.param RF = 1K
.param RL = 100
.param vsupply=5
.lib b:ha502x.cir
x1 in 11 3 4 out 3 ha502x
VIN1 in 0 PULSE (-.1 .1 .1ns .1ns .1ns 100ns 200ns)
RF1 11 out {RF}
RL1 out 0 {RL}
RI1 0 in {RI}
VCC 3 0 {vsupply}
VEE 4 0 [-1*vsupply}
.tran 20ns 420ns
.probe
.end
```

FIGURE 17. TRANSIENT RESPONSE PROGRAM

Enable Response For A Non-Inverting Op Amp

The Sixth program (see Figures 18, 19, and 20) is called cfaenabl.cir, and it computes the response of a non-inverting op amp to an enable control signal. A $2V_{DC}$ excitation is applied to the positive op amp input, and a square wave is applied to the enable input. The enable signal swings from ground to the positive power supply rail, thus simulating an open collector driver. This signal can be modified as required, but it must be disconnected from the supply voltage by removing the {vsupply} term prior to modification. The program requires the user to supply the feedback resistance, the load resistance, the input resistance, and the power supply voltage in volts. The program assumes that the op amp is run off two power supplies of equal and opposite polarity each of which is referenced to ground, so it applies the entered voltage to the op amp as a positive and negative supply with equal magnitudes. If a single supply op amp needs to be evaluated just enter half the power supply voltage, and the analysis will be equivalent. The enable response times can be read off of Figure 19.

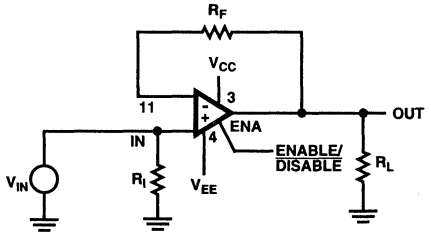


FIGURE 18. ENABLE RESPONSE CIRCUIT SCHEMATIC

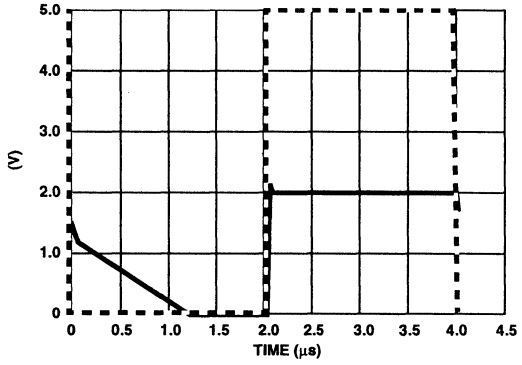


FIGURE 19. ENABLE RESPONSE PROGRAM OUTPUT PLOT

```
*This program simulates the time response of the enable/disable function of
*the non-inverting op amp. The response is obtained with a 2VDC
*input signal, while the voltage on the enable pin swings from VCC to ground.
*The user must specify the load resistance, RL, the feedback resistance, RF,
*and the input resistance, RI. The power supply voltage is set by a parameter
*"vsupply". The op amp model is entered with a .lib statement. The model in the subcircuit call
*(x statement) must correspond to the model called in the .lib statement. If
*the rise and fall times of the enable signal are too fast the program may
*not converge (10ns is optimal).
.param RI = 50
.param RF = 1K
.param RL = 100
.param vsupply=5
.lib b:ha502x.cir
x1 in 11 3 4 out ena ha502x
VIN in 0 2
vena ena 0 PULSE ({vsupply} 0 0ns 10ns 10ns 2000ns 4000ns)
RF1 11 out {RF}
RL1 out 0 {RL}
RI1 0 in {RI}
VCC 3 0 {vsupply}
VEE 4 0 {-1*vsupply}
.tran 20ns 4020ns
.probe
.end
```

FIGURE 20. ENABLE RESPONSE PROGRAM

Summary

Six programs which compute and plot the response of an op amp are described here. These programs make it easy to complete the SPICE analysis, and by using them the results may be compared to new Harris Semiconductor data sheets. This approach gives the minimum data required to evaluate the model, but the actual evaluation must be made by the design engineer. If the model indicates 2dB peaking at the -3dB point while the data sheet shows 3dB peaking at the same point, which does the engineer believe? Since the model is an approximation, the data sheet should be more correct than the model, but because the data sheet is based on "typicals" their curves are sometimes hard to reproduce. This vague area must be resolved through the experience of the design engineer coupled with laboratory data. There is no substitute for accurate measurements! When the data sheet curves, the model curves and the lab curves all fit within a reasonable tolerance the design engineer can begin to trust the models. Keep testing though, because models have been known to be very unpredictable.

Any comments, deletions or additions should be directed to one of the authors for inclusion in revisions on this document.

APPNOTE

No. AN9524 October 1995

Harris Linear

HFA1212 Dual Video Buffer Forms Differential Line Driver/Receiver

Author: Mark Amarandos

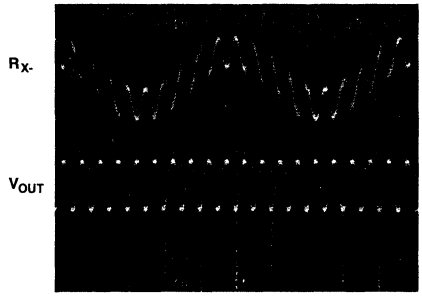
The HFA1212 Dual Video Buffer can be used to implement differential line drivers and receivers with a minimum of external components (see Figure 2). Common mode rejection is set by the internal matched thin film resistors which are pin strapped to set the various closed loop gains that are required.

V_{IN} is terminated into 75Ω and drives both amplifiers in U1. U1A has a gain of -1 while U1B has a gain of +1. These amplifiers create a differential signal with a gain of 2. Series 75Ω resistors provide impedance matching to the transmission line.

The 150Ω termination resistor on the receive side of the transmission line provides proper impedance matching and attenuation for a gain of one at the receive input. U2 performs differential to single ended conversion and provides common mode rejection.

U2A is configured in a gain of +2. U2B subtracts out common mode signals and applies a gain of +2 to differential signals. When V_{OUT} is terminated into 75Ω, the overall gain from V_{IN} to V_{OUT} is unity. Because of the gain of +2 in U2A, the peak voltage at the receiver may not exceed 1.5V.

The oscilloscope photograph illustrates the common mode rejection of the receiver. V_{IN} is a 10MHz, $1.5V_{P-P}$ sine wave. The ground reference of U1 is driven by a 1MHz, $1.5V_{P-P}$ common mode signal. The combined signal, seen on the top trace is measured at R_X-. V_{OUT}, on the bottom trace, is a faithful reproduction of V_{IN} with the common mode signal removed.



V_{IN} = 10MHz, $1.5V_{P-P}$
V_{CM} = 1MHz, $1.5V_{P-P}$ ON GROUND OF U1 WITH RESPECT TO U2

FIGURE 1. COMMON MODE REJECTION

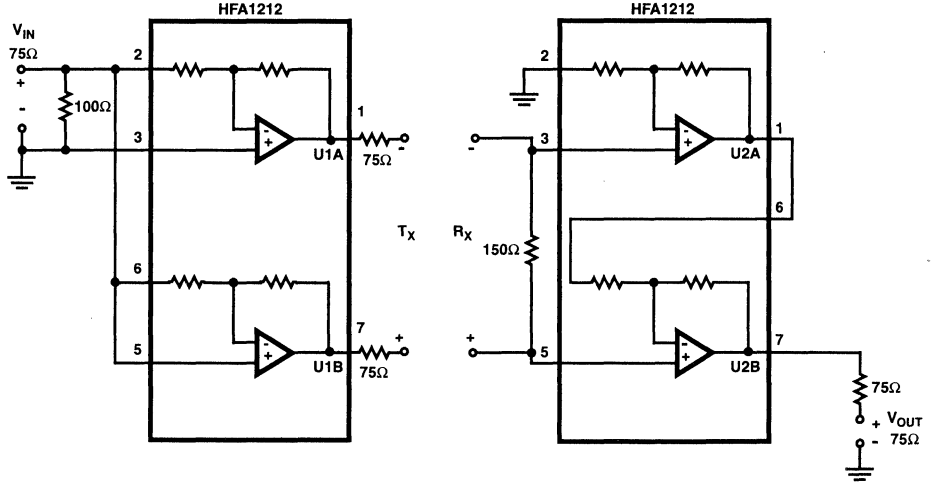


FIGURE 2. DIFFERENTIAL VIDEO LINE DRIVER/RECEIVER

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Harris Semiconductor

APPNOTE

No. AN9528.1 November 1996

Harris Linear

900MHz Down Converter Consumes Little Power (HFA3101)

Authors: Ronald Mancini and Raphael Matarazzo

Most 900MHz down converter designs are proprietary and, thus, are unavailable to the industry. The designs that are available are usually discrete or require high voltage, which excludes them from the portable market. The down converter in Figure 1 is nonproprietary and suits battery powered applications. Moreover, you can use the IC manufacturer's PC board artwork to get a head start.

The heart of the down converter is a Gilbert cell, which consists of two long-tailed, differential-amplifier stages connected as two variable transconductance amplifiers. Because the cell is constructed from the HFA3101 transistor array, the differential amplifier stages are inherently matched. The inherent matching also reduces distortion resulting from thermal effects and mismatches in transistor beta and ohmic resistances. With the HFA3101 configured as shown, each pair of bases acts as a multiplier input. Thus, if you connect a local oscillator and an RF signal to the two inputs, the circuit generates the sum and difference frequency for the down conversion.

R_1, R_2, and R_3 form a voltage bias network to bias the long-tailed pairs; the circuit holds the bases of the current source, Q_5, and Q_6, at 1V and the bases of the inputs, Q_1 and Q_4, at 2.5V. Setting R_E at 27Ω yields emitter currents of approximately 5.5mA, which is adequate to achieve the required bandwidth. This value of R_E is high enough so the quantity βR_E does not load the RF signal source. R_{B1} and R_{B2} terminate the transistor bases with 50Ω through the 0.01μF decoupling capacitors, so the capacitors should be of high quality.

All the components should be leadless, with self-resonant frequencies exceeding 1GHz. The output matching circuit comprising L_C, C_C, and R_C maximizes the gain. The selection of these components maximizes gain while allowing a 50Ω termination; the tuned, medium-Q matching network yields a 50Ω to 2kΩ transformation.

With the component values and frequencies in Figure 1, the circuit down converts 900MHz to 75MHz by using an 825MHz local oscillator signal, and it does so with 50Ω terminations. The circuit functions with supplies lower than 3V and draws comparatively low current for a down converter of this frequency. Thus, it's well suited for battery powered systems. You can obtain the PC board artwork from the HFA3101 data sheet; you need no permission from Harris Semiconductor to use the pattern.

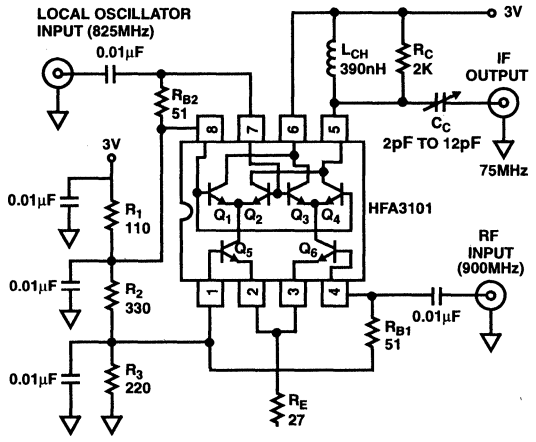

FIGURE 1. 3V DOWN CONVERTER APPLICATION

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APP NOTE

No. AN9536.1 November 1996

PSPICE Performs Op Amp Open Loop Stability Analysis (HA5112)

Authors: Ron Mancini and Doug Youngblood

The open loop stability plot of an op amp circuit, which is commonly called a Bode [1] plot, is often difficult to observe in the lab because most op amps saturate when the loop is opened. Since most op amps have a very high open loop gain, one must work with very small signals when attempting to measure the open loop transfer function, so even if an answer is obtained it usually contains a large error. When PSPICE is employed for the open loop analysis an identical saturation problem occurs because the PSPICE model is built to emulate all of the op amp characteristics. The PSPICE saturation will manifest itself in either of two ways: the program will not be able to calculate a DC bias point or the results of any calculations will be in error.

A method of obtaining an accurate open loop PSPICE plot of an op amp is to fool the circuit as shown in Figure 1A. The capacitor, CINV, is added from the inverting node to ground where it acts like an AC short for the feedback signal. There is still DC feedback, so the program will converge to a DC bias point. The plot will show the op amp open loop gain characteristics if the AC output of PSPICE is configured to be a dB plot of the ratio of the output to input voltage. Although the phase characteristic can be plotted by PSPICE, it is simpler to approximate it from the gain plot by noting where the slope changes (the -3dB breakpoints), and assuming a 45 degree phase shift resulted from the slope change. Several open loop plots are shown in Figure 2. The curve marked with inverted triangles is for the op amp circuit with no feedback resistance (RFT1 and CINV omitted), and it has no relation to the open loop op amp curve shown in the HA-5112 Data Sheet [2] because PSPICE did not calculate the correct bias point. This illustrates the problems that occur when the circuit DC feedback path is broken in an attempt to plot the open loop transfer function. The curve marked with the non-inverted triangles is for the op amp with RFT1 included and CINV connected from the inverting node to ground. Notice that the resulting curve closely approximates the open loop curve shown in the HA-5112 Data Sheet. Also, note that the slope changes to -40dB/decade (called a -2 slope) before the curve passes through 0dB, so the op amp will probably oscillate if it is connected in a gain of one configuration.

Because C_{INV} grounds the inverting node for AC, R_{FT1} appears as a small load to the op amp and has negligible effect on the AC performance. The output of the op amp shown in Figure 1A is the op amp open loop transfer function, so when R_{F1} and R_{G1} are added as shown in Figure 1B, the circuit calculates the open loop stability equation $A\beta = A(R_{G1})/(R_{F1}+R_{G1})$.

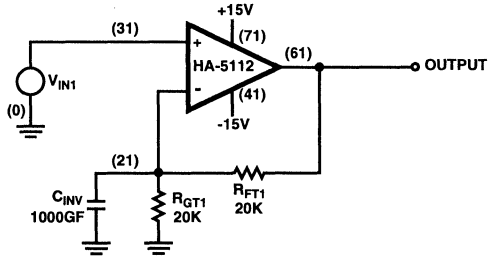

FIGURE 1A. CIRCUIT FOR DETERMINING THE OP AMP OPEN LOOP TRANSFER FUNCTION

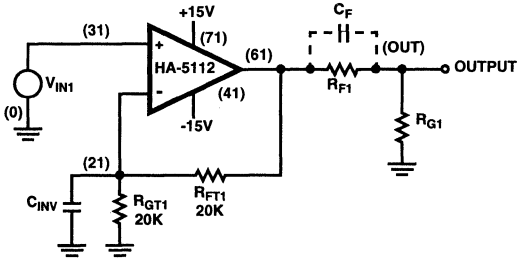

FIGURE 1B. STABILITY ANALYSIS MODEL DESCRIBED IN THE PSPICE LISTING

The curve marked with the diamonds is for R_{F1} = 10K and R_{G1} = 1K. The closed loop non-inverting gain would be 11, thus it should be stable according to the data sheet. Notice that the slope is -1 when it passes through 0dB so the closed loop circuit will be stable. The curve marked with the squares is for a closed loop non-inverting gain of 5 with a feedback capacitor, C_F, added in parallel with RF1. Without C_F the circuit is marginally stable at best because the op amp open loop transfer function (see Figure 2) has a gain of about 9dB when the slope changes from -1 to -2, and the attenuation per the stability equation is -13.9dB. C_F was added to the circuit to introduce a zero into the open loop transfer function, and the zero cancels out the pole at the second breakpoint causing the curve to pass through 0dB with a -1 slope. Thus, C_F stabilizes the circuit for a closed loop gain of 5.

This analysis does not account for manufacturing tolerances which can be as large as 2 to 1. There are two factors to keep in mind when considering manufacturing tolerances, and they are the 0dB frequency intercept tolerance and the open loop gain intercept tolerance.

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The gain intercept has a tolerance of ±6dB, or a factor of two. The gain of the op amp is proportional to gmR_H where gm is the input transconductance and R_H is the effective impedance seen by gm. The first pole frequency is proportional to $1/R_HC$, so the gain bandwidth is constant with respect to variations in R_H. This means that if the gain intercept has increased by 6dB the first pole frequency has moved in by an octave, or conversely, if the gain intercept has decreased by 6dB the first pole has moved out by an octave. The constant gain bandwidth criteria tends to keep the 0dB intercept constant for a given gain intercept change, but there is enough movement to bear watching.

The value of the op amp's internal compensation capacitor might have a ±15% tolerance, and the value of this capacitor determines the 0dB frequency intercept. When this tolerance is added to the gmR_H error the tolerance may be as much as ±30%. The curve for the op amp open loop gain has a 27MHz 0dB frequency intercept, so a prudent design must be able to function with any 0dB frequency intercept from 19MHz to 35MHz.

Op amp stability can be modeled quite well with SPICE, and it often obtains excellent stability results, but it is not prudent to neglect the testing. If the closed loop circuit is driven by a step function, the peak of the overshoot [3] is an excellent indicator of the phase margin or stability.

References

[1] Bode, H.W., Network Analysis and Feedback Amplifier Design, D. Van Nostrand, Inc., 1945.

[2] Harris Semiconductor, Linear and Telecom ICs for Analog Signal Processing Applications, 1993-94.

[3] Mancini, R.A., Feedback, Op Amps and Compensation, Harris Semiconductor, Application Note 9415.

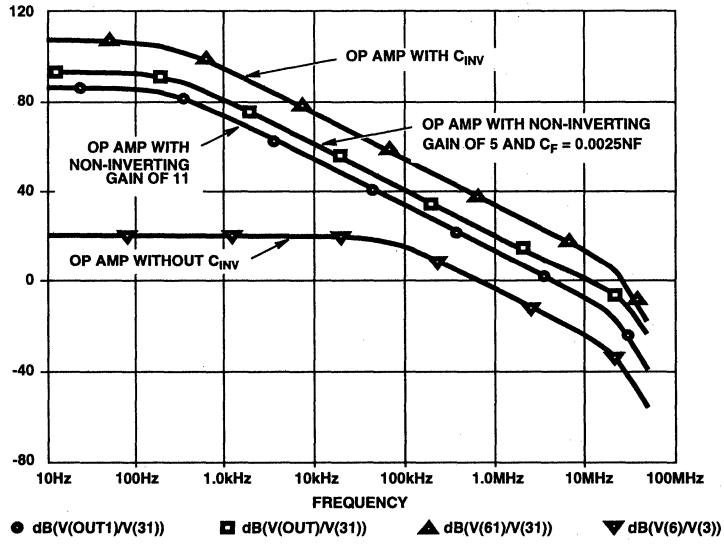

FIGURE 2. TRANSFER FUNCTIONS OF THE OP AMP

```
*ha-5112 open loop parameter circuit
.lib a:HA-5112.cir
x2 31 21 71 41 61 ha-5112
vin1 0 31 ac 1
rgt1 0 21 20k
rft1 21 61 20k
rf1 61 out 10k
rg1 0 out 1k
cinv 0 21 1000Gf
vcc1 71 0 15
vee1 41 0 -15
.ac dec 100 10 50meg
.probe
.end
```

FIGURE 3. PSPICE LISTING

Harris Semiconductor

APPNOTE

No. AN9621.1 November 1996

Harris Linear

Comparison of Current Feedback Op Amp SPICE Models (HA5013)

Author: Ron Mancini

Introduction

Op amp SPICE models are widely used to simulate circuit performance, but there is always the question of how well does the SPICE simulation fit the real world. Bottom line this boils down to another question, "can you bet your design career on it"? The answer is an emphatic no! SPICE is an important tool, and it should be used wherever appropriate, but don't begin to trust it unless you have tested it's answers. First, SPICE is a computer program, thus it is subject to all the vagaries of a machine/software package. Second, the SPICE model is an approximation, and you can't trust approximations until you understand them and their limitations. Before a SPICE model can be trusted it must be tested in a known circuit, and it must yield results comparable to the op amp data sheet. This paper tests four SPICE models from four different major current feedback amplifier manufacturers, and presents the results for your perusal. If you are not going to use one of the tested op amps the actual test results will not be as important as the test procedure, programs, and philosophy.

Model Test Procedure

The model testing was completed using a standard set of PSPICE programs which are contained in Harris Semiconductor Application Note AN9523 titled "Evaluation Programs For SPICE Op Amp Models", AnswerFAX Doc. # 99523. The inverting gain, non-inverting gain, and transient response programs were selected for the model testing because they yield data adequate for a model/data sheet comparison. The application note contains six programs which cover most op amp parameters. Almost any program can be used for the evaluation, but it must use the op amp in the same configuration as the data sheet.

The program must enable the selection of the pertinent component values, such as the feedback resistor, so that the evaluation can be done at the data sheet conditions. This is required for the comparison to be valid because the op amp must be evaluated at the exact data sheet operating conditions so the SPICE generated data and curves can match the data sheet data and curves. The component values that need to be considered are the feedback resistor, input and/or output terminating resistor, load resistor, load capacitor, gain setting resistor, and power supply voltage.

During the evaluation you must keep in mind that the idea is to determine how closely the model matches the op amp as it is characterized in the manufacturer's data sheet. Remember, you are not trying to characterize the op amp. You may find a better method to characterize the op amp, and this is good information for future use, but it is not germane for evaluating the model. Application note AN9523 is a handy tool to use for model evaluations because it allows for and encourages the incorporation of the data sheet operating conditions. In addition it runs three parallel circuits and automatically normalizes the data for three different gains, inverting or non-inverting, in one pass of the program. The programs are the closest thing to an industry standard, and they are available in the application note or on the Harris Semiconductor SPICE model disk.

Comparison Criteria

The comparison criteria results from the distillation of a series of conversations with design engineers. Some might call it an arbitrary or even punitive standard, but it is the only one in existence, so it will be used. When the peaking is within 2dB, this is considered to be good correlation, while peaking in excess of 2dB is designated as marginal. Although the best case is where the data sheet matches the model results, data sheet peaking less than the model peaking is preferable because it is less likely to lead the designer to optimistic conclusions. Peaking causes the emphasis of the high frequencies contained in the signal so it usually leads to distortion.

Bandwidth correlation of the model to the data sheet within 20 percent is acceptable. Data sheet bandwidth greater than the model bandwidth is preferable because it leads to conservative design.

The transient response correlation should be within 20 percent, but this parameter is secondary to the peaking and bandwidth. It is extremely difficult to get good transient response from a model, so many model designers sacrifice this parameter in favor of the frequency response plots.

The data sheet curves are obtained from measurements made on a "typical" IC, and considering the difficulties encountered when measuring CFAs, these curves are only repeatable to a few percent. The model approximates the IC performance, so it should be expected that there will be some differences between the curves produced by the model and the data sheet curves. The tolerances set out above are meant to account for these differences.

Op Amps Compared In The Evaluation

The following op amps were selected for evaluation: the Harris Semiconductor HA5013 [1], the Analog Devices

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TABLE 1. RESULTS OF THE NON-INVERTING GAIN EVALUATION

OP AMP	GAIN	DATA SHEET PEAK/DIP	MODEL PEAK/DIP	DATA SHEET -3dB BW	MODEL -3dB BW
HA5013	1	3.2dB	2.5dB	125MHz	120MHz
	2	3.1dB	1.9dB	110MHz	98MHz
	10	0dB	0dB	70MHz	58MHz
AD811	1	0dB	2.3dB	119MHz	110MHz
	2	0dB	0.3dB	115MHz	115MHz
	10	0dB	0dB	100MHz	105MHz
CLC414	2	0dB	2dB	70MHz	210MHz
	6	0dB	0dB	96MHz	125MHz
	10	0dB	0dB	60MHz	68MHz
LT1229	2	0.2dB Peak	0.8dB Dip	102MHz	120MHz
	10	0dB	0dB	60MHz	70MHz
	100	0dB	0dB	13MHz	7MHz

AD811 [2], the Comlinear CLC414 [3], and the Linear Technology LT1229 [4]. These op amps were selected on the following criteria: availability, current feedback architecture, available SPICE models, the bandwidths are similar, and the remaining parameters are similar. No attempt was made to review the model to determine if one model appeared to be superior to another; the only criteria for selection is given above. There are some other companies that might have been included in the comparison, but their models were not on hand when the comparison was done.

Test Results For Non-Inverting Op Amps

The conditions for each test are exactly the same as those given on the vendor's data sheet. At first glance this may seem unfair because one vendor tests with a 10pF load and another does not specify a load capacitor (how do they get probes and loads that don't have capacitance?), but because we are evaluating each model against its data sheet, it is a fair comparison. The load conditions for each op amp comparison are given in Table 2. A separate simulation with a small capacitive load was run for each op amp model to check for instability. The results of the non-inverting gain evaluation are summarized in Table 1.

The HA5013 data is shown in Figure 1. The HA5013 model indicates 0.7dB less peaking than the data sheet, and it indicates 5MHz less bandwidth than the data sheet. Both of these numbers are well within the comparison criteria so it is safe to assume that the model represents the IC very well for the non-inverting gain configuration.

The AD811 data is shown in Figure 2. The AD811 model has 2.3dB peaking while the data sheet shows 0dB peaking. The model bandwidth is 9MHz less than the data sheet bandwidth. This is marginal performance for the model, but if it is used to evaluate a circuit the results will be pessimistic so the designer should be safe.

This model, see Figure 3, shows a spike in the frequency response at 900MHz when a 4pF load capacitor is added to the circuit. If the spike is just an artifact produced by the model it may have no effect on the actual circuit performance, but if it shows up in the IC transfer function it could cause high frequency oscillation problems. Clearly, the spike needs to be investigated further before the designer can be comfortable with the IC and the model. The data sheet shows quite a bit of difference between the frequency response curves at ±15V and ±5V power supply operation. The SPICE model analysis shows no difference between these curves, so unless further information comes to light, it must be assumed that the model does not include effects due to power supply variations.

The CLC414 data is shown in Figure 4. The CLC414 model has 2dB of peaking versus the data sheet peaking of 0dB, and the model bandwidth is 210MHz versus the data sheet bandwidth of 70MHz. The difference in the peaking numbers is within our criteria with the high number being in the model so it is acceptable. The bandwidth difference is so large that the model might be not be usable because it will predict overly optimistic results. Also, the model may need some help; sometimes these models need the addition of external components to aid convergence or measurements. It would be in the designer's best interest to contact the manufacturer's applications department prior to proceeding with a design based on this model.

Figure 5 shows the effect of adding a 4pF load capacitance. Notice that the peaking increases about 1dB, and the -3dB bandwidth increases about 7 percent when the load capacitor is added to the circuit. This is normal operation for a CFA, and it can be countered by increasing the feedback resistor a few percent [5].

The LT1229 data is shown in Figure 6. The LT1229 model has a 0.8dB dip, while the data sheet shows a 0.2dB peak. The numbers are small, but they go in opposite directions, so overall it adds up to a 1dB error which is acceptable. The model bandwidth is 120MHz, and the data sheet bandwidth is 102MHz, so this does not meet the evaluation criteria. Furthermore, the model will predict a much better high fre-

TABLE 2. LOAD CONDITION FOR EACH NON-INVERTING GAIN EVALUATION

OP AMP	POWER SUPPLY	LOAD RESISTOR	LOAD CAPACITOR	GAIN	FEEDBACK RESISTOR
HA5013	±15V	400Ω	10pF	1	1000Ω
				2	681Ω
				10	383Ω
AD811	±15V	150Ω	0pF	1	750Ω
				2	649Ω
				10	511Ω
CLC414	±5V	100Ω	0pF	2	500Ω
				6	500Ω
				10	500Ω
LT1229	±15V	100Ω	0pF	2	750Ω
				10	750Ω
				100	750Ω

quency performance than the IC can deliver, so the designers must factor this into their calculations.

Figure 7 shows the effect of adding a 4pF load capacitance to the LT1229. The dip decreases about 0.4dB, while the -3dB bandwidth increases about 12 percent. Again, this is normal operation for a CFA, and it can be countered by increasing the feedback resistor a few percent.

Figure 8 shows the non-inverting frequency response at ±5V power supplies. The data sheet predicts a bandwidth change from 102MHz to 60MHz when the power supplies are changed from ±15V to ±5V. The model shows a change from 120MHz to 60MHz when the supply voltage is changed. This is an example of why the model needs to be examined before doing any design is with it. At 15V supplies the designer has to worry about getting optimistic results, while at 5V supplies the design results should be right on target. This is also a good example of a SPICE model which includes a good supply voltage dependency function.

Test Results For The Inverting Op Amps

The conditions for each test are exactly the same as those given on the vendor's data sheet. The load conditions for each op amp comparison are given in Table 4. The results of the inverting gain evaluation are summarized in Table 3. The LT1229 data sheet did not include any inverting gain curves, so it was not included in this evaluation.

The HA5013 data is shown in Figure 9. The HA5013 model indicates 1dB less peaking than the data sheet, and it indicates 15MHz less bandwidth than the data sheet. Both of these numbers are well within the comparison criteria, so it is safe to assume that the model represents the IC very well for non-inverting gain. The model bandwidth for the gain of 10 configuration is 70MHz compared to a data sheet bandwidth of 22MHz, thus this model will yield overly optimistic answers at high inverting gains. If the model designer has to make a compromise, it will usually happen at high inverting gains. The compromises are made at high inverting gains because this is where CFAs are used the least.

The AD811 data is shown in Figure 10. The AD811 model indicates 0.8dB of peaking, and when this is compared to the data sheet which has no peaking it all looks fine. The model does have 2.3dB peaking when it is in a gain of -10 configuration, thus, depending on what gain the designer is working at, allowances may have to be made for this error. Again, the compromise has been made at high inverting gains. The model bandwidth matches the data sheet bandwidth very well.

The CLC414 data is shown in Figure 11. The CLC14 model indicates 0.3dB of peaking, and when this is compared to the 0.8dB peaking shown on the data sheet it is well within the comparison criteria. The model bandwidth is 180MHz compared to the data sheet bandwidth of 97MHz, so the model will predict overly optimistic frequency performance. The -10dB performance of this model is excellent, which proves that not all model designers push the poorer performance into the high inverting gain configurations.

Time Domain Testing

Each op amp was evaluated with a ±100mV square wave input signal to determine the small signal time domain response. If a photograph of this response is in the data sheet, then a comparison can be made to find out how well the PSPICE simulation mirrors the time domain response. If the photograph is not contained in the data sheet, this data still has value because it can be compared to the theoretical time domain response as calculated from the second order transfer function equation [6].

The HA5013 small signal pulse response (equivalent to the time domain response) is shown in Figure 12. The model and the data sheet both show a few percent of overshoot which is very good correlation.

The AD811 small signal pulse response is shown in Figure 13. The PSPICE program was not able to complete the analysis because the time domain response never settled down. The program chooses the time step size according to the activity of the response, and the AD811's very active response dictated a small time step, which resulted in too

TABLE 3. RESULTS OF THE INVERTING GAIN EVALUATION

OP AMP	GAIN	DATA SHT. PEAK/DIP	MODEL PEAK/DIP	DATA SHT. -3dB BW	MODEL -3dB BW
HA5013	-1	1.5dB	0.5dB	100MHz	85MHz
	-2	0.4dBDip	0.6DipdB	80MHz	80MHz
	-10	0dB	0dB	22MHz	70MHz
AD811	-1	0dB	0.8dB	115MHZ	110MHZ
	-10	0dB	2.3dB	95MHz	105MHz
CLC414	-1	0.8dB	0.3dB	97MHz	180MHz
	-5	0.6dB	0dB	88MHz	98MHz
	-10	0dB	0dB	70MHz	55MHz

TABLE 4. LOAD CONDITION FOR EACH INVERTING GAIN EVALUATION

OP AMP	POWER SUPPLY	LOAD RESISTOR	LOAD CAPACITOR	GAIN	FEEDBACK RESISTOR
HA5013	±15V	400Ω	10pF	-1	750Ω
				-2	750Ω
				-10	750Ω
AD811	±15V	150Ω	0pF	-1	590Ω
				-10	511Ω
CLC414	±5V	100Ω	0pF	-1	500Ω
				-5	500Ω
				-10	500Ω

many calculations. The time domain response overshoots the final value by 160mV for a 200mV step. This is almost a complete reflection of the input step, and it is very unusual. This phenomena may be related to the spike in the non-inverting frequency response curve, but wherever it comes from, it must be investigated and resolved before the model is usable for time domain analysis.

The CLC414 small signal pulse response is shown in Figure 14. The model overshoot is 100mV, and it settles out in 30ms. There is no photograph of the small signal pulse response in the data sheet, so the model cannot be compared to the data sheet. How much can the model's transient response be trusted? The only way to determine this is to test the op amp, and then compare the test results to the model results. Considering the large amount of overshoot, and the bandwidth results, this may be a wasted effort.

The LT1229 small signal pulse response is shown in Figure 15. The model overshoot is 85mV, and it does not settle out for 43ns. The small signal rise time is shown in the data sheet, and the photograph has very little overshoot. The model overshoot is much more than one would expect from an op amp which has very little peaking in its frequency transfer function, thus it seems safe to assume that the model adds overshoot to the time domain response. The model is usable for transient analysis, but picking the model artifacts out of the plots will be laborious and possibly misleading.

Summary

No model meets the evaluation criteria in every case, and this is because the models are approximations of reality. Also, the data sheets, which in this analysis have been considered to be the standard, contain some degree of error. This lack of correlation between the data sheet and the models will always exist; and the proof is that the op amp design engineers always complain that the process models are not accurate enough. The paradox is that when the process models evolve enough to become really accurate the process has usually aged and is becoming obsolete.

The HA5013 model is the most accurate by any standard. It meets all the evaluation criteria except at one point. This is because the model performance standards were set first, and then the model was constructed to meet the performance standards. Designing the model involves a trade-off between complexity, run time, convergence capability and

accuracy. The HA5013 model was able to optimize these parameters through the use of some special techniques.

The LT1229 model is acceptable except for its transient performance. The other models will be hard to use with good accuracy.

The model should be first evaluated against the data sheet. If excellent correlation is obtained, such as the HA5013 gave, then the model results can be trusted. If any doubt exists about the model, then electronic circuit theory, a good calculator and the lab must be employed to settle the questions.

When the model performance matches the data sheet performance, and both match the lab performance the results are trustworthy. This model can be used to predict the performance of any linear circuit configuration which converges.

References

[1] Data sheet for HA5013, Harris Semiconductor, 1994. AnswerFAX Document No. 3654

[2] Data sheet for AD811, Analog Devices, 1994

[3] Data sheet for CLC414, Comlinear Corporation, 1993

[4] Data sheet for LT1229, Linear Technology, 1992

[5] Mancini, Ronald, "Converting From Voltage-Feedback To Current-Feedback Amplifiers", Electronic Design, 6/95

[6] Mancini, Ronald, "Feedback, Op Amps And Compensation", Harris Semiconductor 9415, 1995

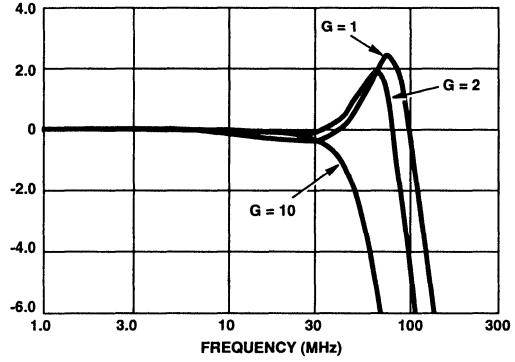

FIGURE 1. NON-INVERTING FREQUENCY RESPONSE OF THE HA5013

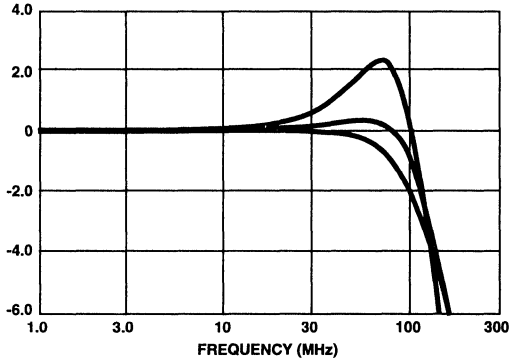

FIGURE 2. NON-INVERTING FREQUENCY RESPONSE OF THE AD811

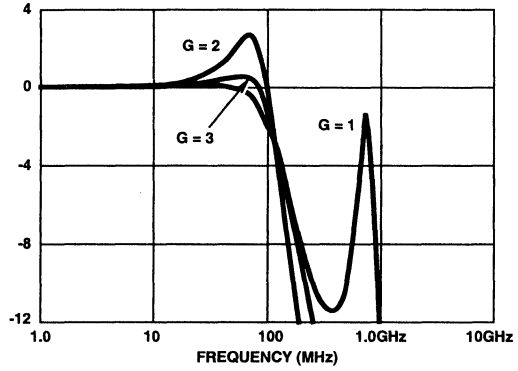

FIGURE 3. UNEXPECTED NON-INVERTING FREQUENCY PLOT FOR THE AD811

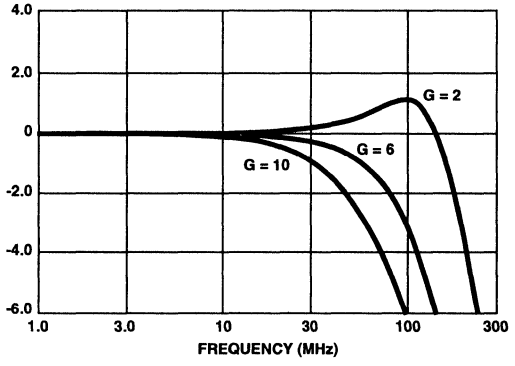

FIGURE 4. NON-INVERTING FREQUENCY RESPONSE OF THE CLC414

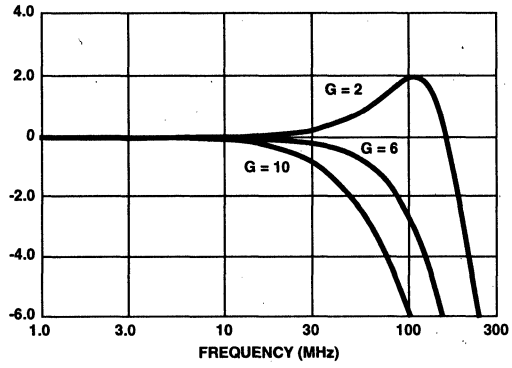

FIGURE 5. EFFECT OF 4pF LOAD ON THE CLC414

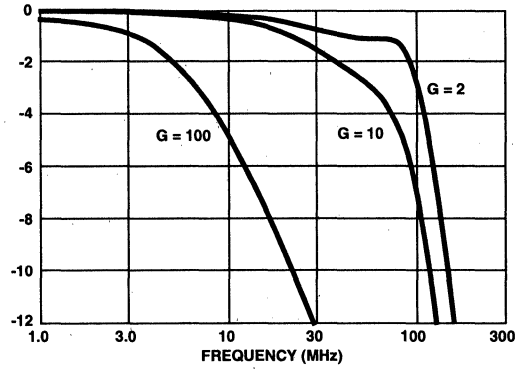

FIGURE 6. NON-INVERTING FREQUENCY RESPONSE OF THE LT1229

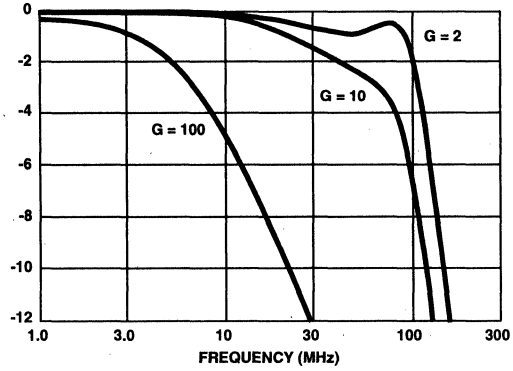

FIGURE 7. EFFECT OF THE 4pF LOAD ON THE LT1229

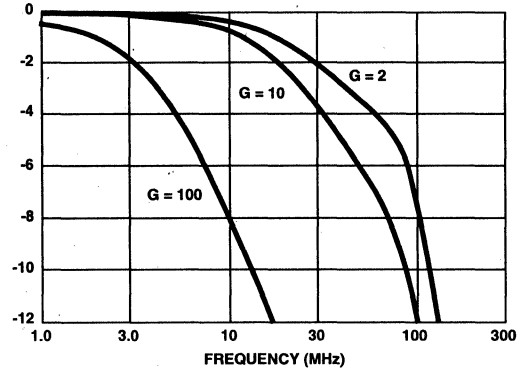

FIGURE 8. NON-INVERTING FREQUENCY RESPONSE OF THE LT1229 AT ±5V

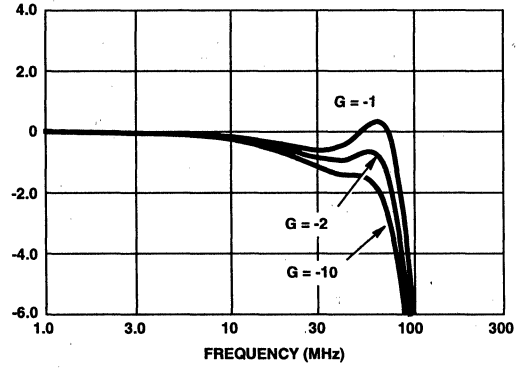

FIGURE 9. INVERTING FREQUENCY RESPONSE OF THE HA5013

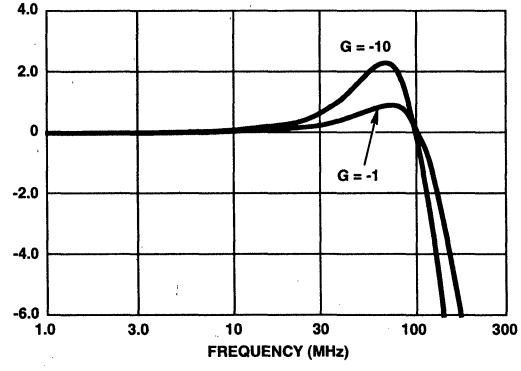

FIGURE 10. INVERTING FREQUENCY RESPONSE OF THE AD811

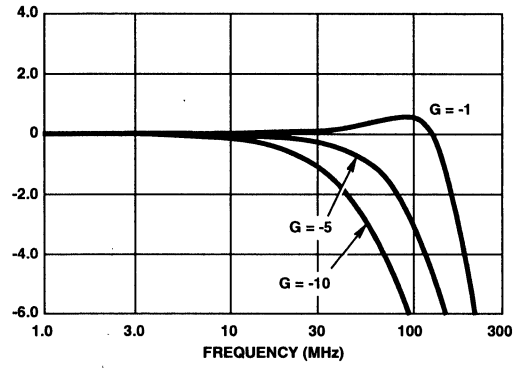

FIGURE 11. INVERTING FREQUENCY RESPONSE OF THE CLC414

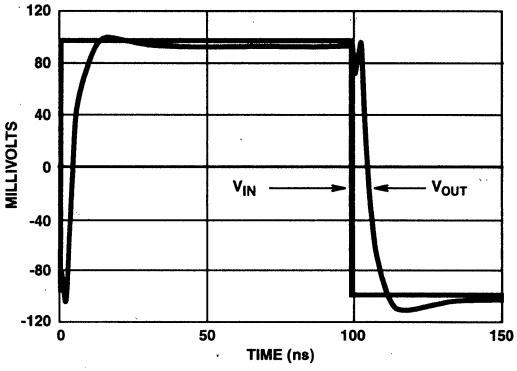

FIGURE 12. HA5013 SMALL SIGNAL PULSE RESPONSE

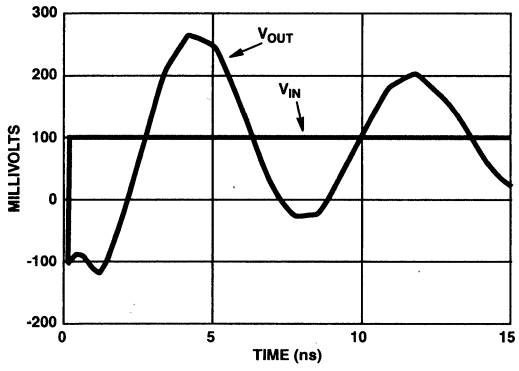

FIGURE 13. AD811 SMALL SIGNAL PULSE RESPONSE

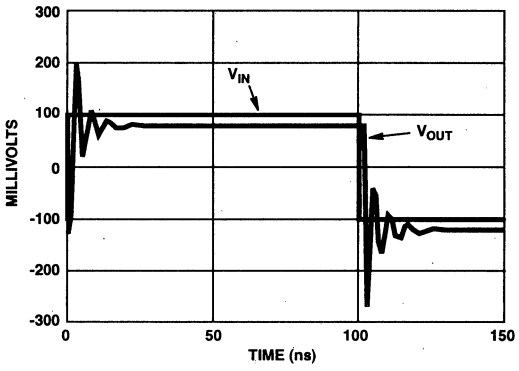

FIGURE 14. CLC414 SMALL SIGNAL RESPONSE

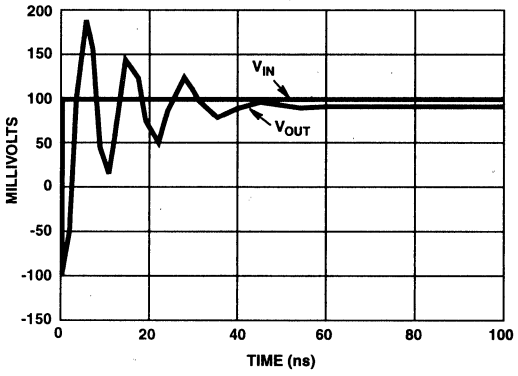

FIGURE 15. LT1229 SMALL SIGNAL PULSE RESPONSE

Harris Semiconductor

APPNOTE

No. AN9641 September 1996

Harris Linear

High-Frequency VGA Has Digital Control

Author: Ronald Mancini

Introduction

You can use variable-gain amplifiers (VGAs) in many types of systems, such as radio receivers, in which the input signal voltage depends on an uncontrolled variable, such as distance to the transmitter. In this type of system, you can use a VGA to ensure that the input signal amplitude matches the input voltage range of key components, such as ADCs and DACs, thereby maximizing the converters' dynamic range. The VGA in Figure 1 has high bandwidth, ranging from 115MHz at high gain to 225MHz at low gain, so you can use this circuit in the RF-signal path without degrading the signal. You can update the DAC in this circuit at 100MHz, but the level-shifter op amp limits the speed at which you can update the gain of the VGA to 3MHz. As configured, this VGA implements a calibration function with a 3MHz DAC update rate.

The VGA design comprises a three-transistor, long-tailed pair configuration comprising Q_1, Q_2, and Q_3. By changing the base voltage of Q_3, the DAC (IC_1) varies the emitter currents of the long-tailed pair. Changing Q_3's base voltage controls the gain according to the following equation, where K is a function of the emitter current and VB_3 is the base voltage of Q_3:

$$G = KV_{IN}|V_{B3}|.$$

The gain control and bias-stability parameters of the circuit depend on transistor matching, so the circuit uses an HFA3102 matched, long-tailed array for Q_1 through Q_3. The usable range of V_{B3} is -0.8 to -4.4V, which corresponds to a gain range of 11.8 to -16.9dB, respectively. This gain span is a total of 28.7dB. The gain is proportional to R_4. Increasing R_4 increases the gain, but the gain span stays constant at approximately 28.7dB. Increasing the gain causes a corresponding decrease in the frequency response.

R_2, R_3, and the -5V supply form a bias circuit that sets V_{B3} to -4.4V when there is no DAC output current (the voltage across R_1 is zero), which occurs at a digital input of all ones. When the digital input is all zeros, the DAC output current is 20mA, which develops -1V across R_1. IC_2 level-shifts and amplifies this voltage to yield V_{B3} = -0.8V. The CA5160 works well as the level shifter because its low bias currents do not affect the DC performance, and its bandwidth enables the gain to change at a rate as high as 4MHz.

You should keep the input signal level at about 25mV to prevent distortion. The signal path has an excellent frequency response because the HFA3102 is the only component in the signal path. A frequency response plot for V_{B3} = -3V (gain of 10dB) shows that the transfer function is well-behaved with no peaking and that the frequency response is 131MHz at the -3dB point. The DAC transfers the digital input to the internal registers on the rising edge of the clock pulses. This circuit uses the inverting DAC output to yield a positive increasing-transfer function, but you can obtain the inverse-transfer function by using the noninverting input (Table 1).

TABLE 1. VGA PERFORMANCE SUMMARY

PARAMETER	MINIMUM	MAXIMUM
Gain (dB)	-16.9	11.8
V_{B3} (V)	-4.4	-0.8
F_{-3dB}, (MHz)	225	115
Digital Input/Invelting Output	0000 0000 0000	1111 1111 1111
Digital Input/Noninventing Output	1111 1111 1111	0000 0000 0000

If fast updates are unnecessary, you can use a slower DAC than IC. However, you may also have to redesign the interface circuit (IC_2 and associated conponents) if the DAC output voltage swing changes (DI #1895).

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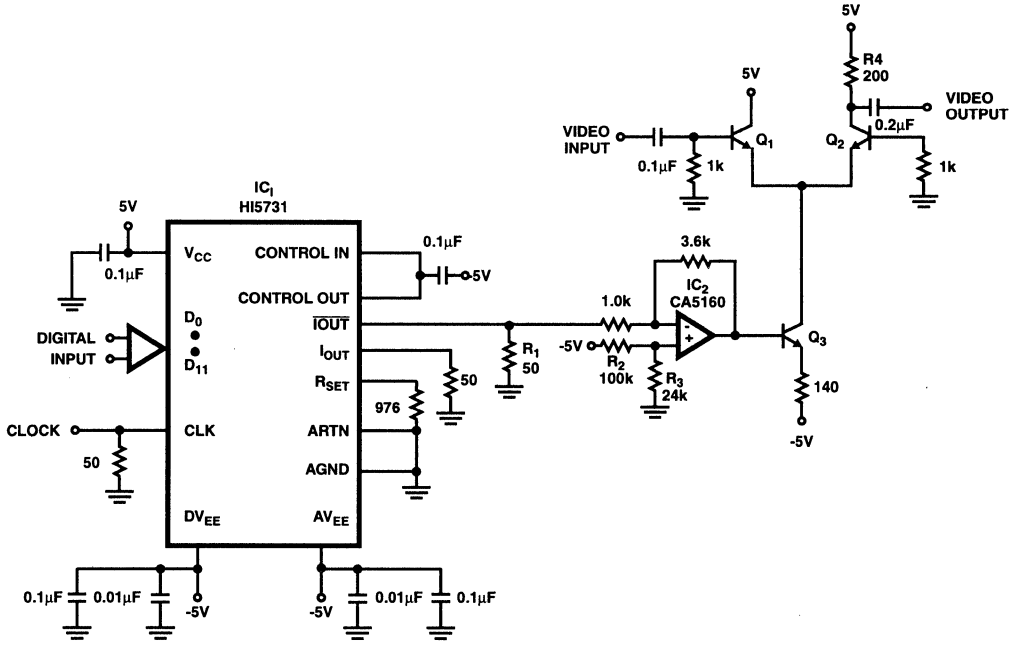

NOTE:

1. Q_1, Q_2, Q_3 = HFA3102.

FIGURE 1.

This variable-gain amplifier has high bandwidth ranging from 115MHz at high gain to 225MHz at low gain, and you can update the gain at a -3MHz rate.

Harris Semiconductor

APPNOTE

No. AN9653 November 1996

Harris Linear

Use and Application of Output Limiting Amplifiers (HFA1115, HFA1130, HFA1135)

Authors: Mark Amarandos and Jeff Lies

Introduction

Amplifiers with internal voltage clamps, also known as limiting amplifiers, have a wide range of practical uses. They are most commonly used to protect load circuitry that has a limited input range. By connecting the high and low clamp pins to DC levels, the output voltage may be restricted to the desired range. The internal clamp circuitry also avoids saturation of the output stage devices and assures fast overload recovery.

Prior to the introduction of limiting amplifiers, design engineers had to develop their own limiting networks. This network was as simple as two Schottky diodes and a current limiting resistor, or as complicated as an adjustable limiting network that might employ several transistors, resistors and diodes. With limiting amplifiers, adjustable limiting networks are realized with a simple resistor divider network connected to the high and/or low limit pins.

Many other applications exist for limiting amplifiers. Because of their fast response time and flexibility in output voltage range, they make excellent high performance comparators. Several applications make use of the wide bandwidth of the clamp inputs. Through appropriate modulation of the clamp input voltages, an AM modulator, soft clipping circuit and sync stripper can be realized. This application note describes how amplifiers with internal clamps work, the advantages of using these amplifiers for limiting and a number of application circuits.

Input vs Output Limiting

There are two classes of limiting amplifiers on the market today, those that employ input limiting to constrain the output voltage, and those that utilize output limiting. Each has their own advantages, and users should understand these issues and pick the best one for their application. Advantages of input limiting amplifiers include: better clamp accuracy, continued low closed loop output impedance during limiting, and depending on the implementation, input limiting may or may not prevent input stage saturation.

Input limiting amplifiers have some serious limitations, however, which are not shared by output limiting versions. The input limiting amplifier offers no limiting action when configured in inverting gains, and does not protect against transients introduced at the inverting input, because the input limiting function applies only to the positive input.

Additionally, because the limiting voltages are applied to the input stage, they are amplified by the op amp's gain. This precludes the use of input limiting amps in open loop configurations (e.g., comparators) and makes the setting of the limit voltages much more critical. Consider a limiting amplifier in a closed loop gain of 10. A 10mV error in setting the limit voltage translates into a 100mV error at the output of an input limiting amplifier, while the output limiting amp delivers only the 10mV error. If an input limiting amplifier becomes damaged and goes open loop, the rail-to-rail output swing will likely take out the expensive A/D it was designed to protect. Output limiting controls the output excursions as long as the limiting circuitry remains functional. This application note focuses on output limiting amplifiers due to their greater flexibility.

Output Limiting Current Feedback Amplifiers

Harris Semiconductor's line of output limiting amplifiers are current feedback op amps which feature user programmable output clamps to limit output voltage excursions. Limiting action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H, or V_L ($\pm$ the clamp accuracy) respectively. The output voltage remains at the clamp level as long as the overdrive condition remains.

When the input voltage drops below the overdrive level (V_{CLAMP} / A_{VCL}) the amplifier returns to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The clamped overdrive recovery time may be an order of magnitude faster than the amplifier's normal saturation recovery time. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or D/A converters. Because the clamp circuit is part of the amplifier, and the amp has been characterized with the clamp circuit present, the user can be confident that the clamp circuitry will induce minimal performance degradation during normal linear operation.

Clamp Circuitry

Figure 1 shows a simplified schematic of the HFA1130 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (Q_{X1} - Q_{X2}) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current equal to the

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current flowing through the inverting input. This current is mirrored onto the high impedance node (Z) by Q_{X3} - Q_{X4}, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by Q_{P4} and Q_{N4}. Note that when the output reaches its quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

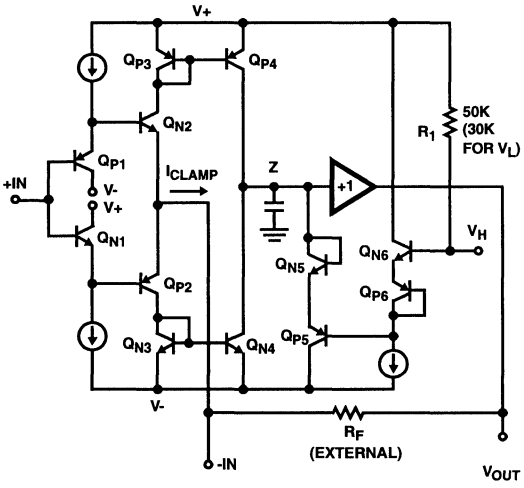

FIGURE 1. HFA1130 SIMPLIFIED V_H CLAMP CIRCUITRY

Tracing the path from node V_H to node Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (Q_{N6} and Q_{P6}) to set up the base voltage on Q_{P5}. Q_{P5} begins to conduct whenever the high impedance node reaches a voltage equal to Q_{P5}'s base + $2V_{BE}$ (Q_{P5} and Q_{N5}). Thus, Q_{P5} clamps node Z whenever Z reaches V_H. R_1 provides a pull-up network to ensure functionality with the clamp input floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. Q_{P5} must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, cause inaccuracies in the clamping level. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 1, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the Q_{X6} transistors, and the Q_{X5} transistors. If the transistors are run at the same current level there is no V_{BE} mismatch, and no contribution to the inaccuracy. The Q_{X6} transistors are biased at a constant current, but as described earlier, the current through Q_{X5} is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level and R_F, so clamp accuracy degrades as the overdrive increases, and as R_F decreases. Consideration must also be given to the fact that the clamp voltages have an effect on amplifier linearity. As the output voltage approaches the clamp level the clamp circuitry starts to conduct and linearity degrades. Most limiting amplifier data sheets detail the impact on linearity in a graph entitled: "Non-linearity Near Clamp Voltage".

Clamp Range

Unlike some limiting amplifiers, both V_H and V_L of HFA series amplifiers have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1130 output could be limited to ECL levels by setting V_H = -0.8V and V_L = -1.8V.

Use as a Protection Circuit

Limiting amplifiers are frequently used to protect circuitry that has a limited input range. A classic example is a buffer for an A/D converter. Many A/D converters can be damaged if their input is taken much beyond their specified input range. In addition to providing necessary input voltage clamping, a limiting amplifier can provide the peak currents needed to charge the A/D converter input capacitance and remain stable with step changes in input voltage. Of course, the limiting amplifier can also provide the gain and level shifting frequently required preceding an A/D converter.

In Figure 2, the HFA1135 limiting amplifier is used to drive the HI1175 8-bit, 20 MSPS A/D Converter. The HFA1135 is configured as a level shifting amplifier with an offset of 0.5V and a gain of 2. This allows a ground referenced, 1V Max signal to span the full 2V input range of the HI1175. The HI1175 is typical of many single supply A/D converters which have an input range that does not include ground. The V_{RT} and V_{RB} voltages of 2.5V and 0.5V respectively set the limits of the HI1175 input range. The V_L clamp voltage of 0V keeps the lower limit of the input to the HI1175 within its absolute maximum range. The 0.5V difference between the nominal minimum input voltage and the clamp voltage assures that the clamp circuitry does not effect the linearity of the circuit. A voltage divider sets the V_H voltage to approximately 3V.

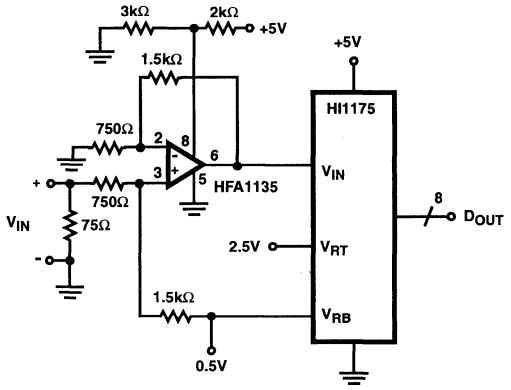

FIGURE 2. HFA1135 DRIVING THE HI1175 ADC

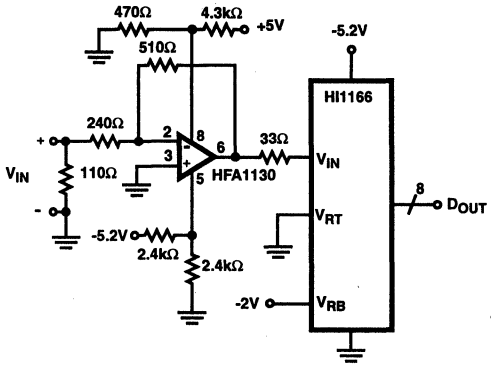

FIGURE 3. HFA1130 DRIVING THE HI1166 ADC

In Figure 3, the HFA1130 is used in a gain of -2 to drive the input of the HI1166 8-bit, 250 MSPS A/D Converter. Typical of A/D converters that operate above 100Msps, the HI1166 is an ECL part that runs from power supplies of GND and -5.2V. The HFA1130 allows a 0V to 1V input to span the 0V to -2V range of the A/D converter. Resistor dividers set the V_H and V_L limit levels to 0.5V and -2.5V, respectively.

Using Current Feedback Amplifiers as Comparators

Current feedback amplifiers, especially those with output limiting, make excellent high speed, open loop comparators. Recall that the non-inverting input connects to the input of a unity gain buffer, while the inverting input connects to the buffer output. This buffer sources or sinks current until the error current is minimized, and this buffer current is mirrored onto the high impedance node to provide the slewing current. Since the slewing current is proportional to the current flowing through the amplifier's inverting input, the slew rate may be adjusted by the external resistance on the inverting input.

If a voltage is applied to the non-inverting input, the internal buffer forces the inverting input to the same voltage, the buffer will sink or source current accordingly, and the amplifier output will fall or rise respectively. With no provision for feedback, the buffer's current remains constant, and the output drives into the stops resulting in output saturation with its undesirable effects.

Consider the HFA1130 based inverting comparator circuit (Figure 4). The GND at the HFA1130's non-inverting input forces the internal buffer to output 0V at the inverting input. As soon as V_{IN} rises above 0V, the input buffer begins sinking current, and the output signal falls to its negative stop. When V_{IN} returns below GND, the output transitions high.

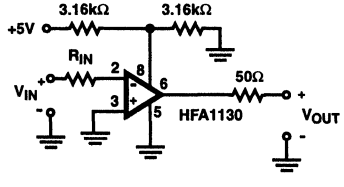

FIGURE 4. HFA1130 IMPLEMENTED AS AN INVERTING, 2ns, TTL COMPATIBLE OUTPUT COMPARATOR

Because of the HFA1130's relatively small propagation delay of 0.5ns, the dominant component of the comparator's response time is the op amp's slew rate. Since the slew rate is a function of I_{IN}, the response time is strongly influenced by V_{IN}, and the choice of R_{IN}. Decreasing R_{IN} decreases the response time, with a slight decrease in limiting accuracy, (Figure 5). However, if R_{IN} is too small the internal current mirrors can saturate and reverse the effect. To implement a non-inverting comparator, simply ground the outboard side of R_{IN}, and apply the input signal to the amplifier's non-inverting input.

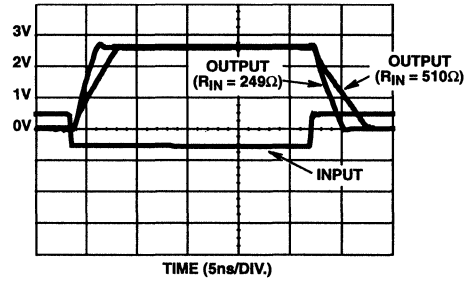

FIGURE 5. DECREASING R_{IN} REDUCES THE COMPARATOR RESPONSE TIME FROM 2.5ns TO 1.2ns

Comparator Benefits From Output Limiting

The HFA1130's open loop response plot (Figure 6) illustrates the key advantages of using output limiting amplifiers for comparator applications. Besides the obvious benefit of constraining the output swing to a defined logic range, limiting the output excursions also keeps the output transistors from saturating which prevents unwanted saturation artifacts from distorting the output signal. Utilizing the output limiting function also takes advantage of the HFA1130's ultra-fast recovery from clamped overdrive (<1ns). Instead of the >10ns propagation delay (the HFA1130's normal saturation recovery time) obtained with the unrestricted output, limiting the positive swing to 2.5V yields a 2ns response time.

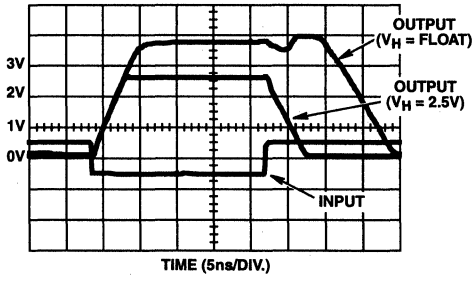

FIGURE 6. COMPARISON OF COMPARATOR RESPONSE WITH AND WITHOUT OUTPUT LIMITING

AM Modulator Circuit

The fast overdrive recovery time and wide bandwidth of the clamp inputs allows these inputs to be driven by high frequency AC as well as DC signals. When driven at the appropriate

levels, the clamp inputs may be used to form an AM modulator. Figure 7 shows a complete AM modulator circuit. The HFA1130 Limiting Amplifier is driven by a $4V_{P-P}$ carrier signal. The gain of 2 through the HFA1130 insures that the carrier amplitude is sufficient to drive the output over its ±3.3V range.

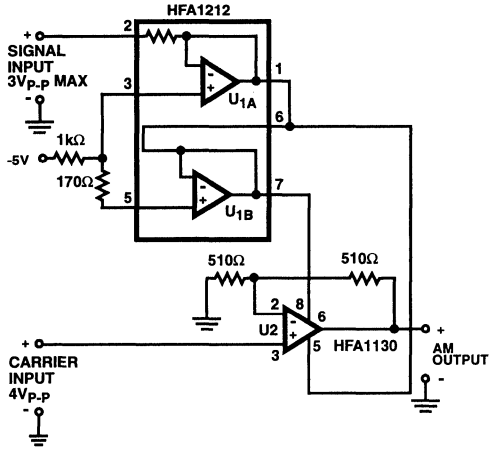

FIGURE 7. AM MODULATOR UTILIZING THE HFA1130 LIMITING CAPABIILITY

The HFA1212 performs the necessary level shifting and inversion to convert the modulating signal input into a pair of antiphase signals that control the high and low clamp inputs. U_{1A} inverts the signal and level shifts to -1.5V. U_{1B} inverts that signal forming a complimentary signal centered at +1.5V.

With a signal input of 0V, U_2 produces a $3V_{P-P}$ output at the carrier frequency. As the signal input varies, U_2 produces a symmetrically modulated carrier with a maximum amplitude of $6V_{P-P}$. The oscilloscope photograph in Figure 8 shows a 5MHz carrier AM modulated by a 100kHz signal. The 2300V/µs slew rate of the HFA1130 limits $6V_{P-P}$ amplitude carrier signals to a frequency of 61MHz. If adjusted for lower output signal levels, the carrier and modulating frequencies can be increased to well above 100MHz.

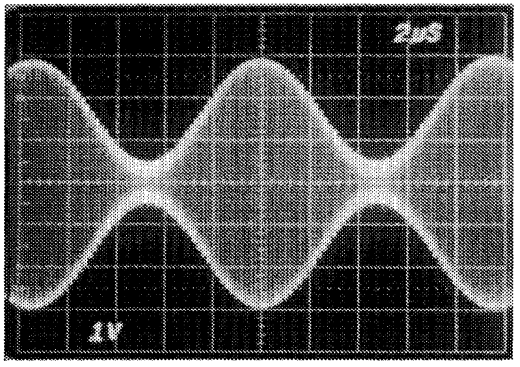

FIGURE 8. A 5MHz CARRIER IS AM MODULATED BY A 100kHz SIGNAL

Soft Clipping Circuit

Any amplifier stage driven to the limit of its linear range will cause signal clipping. The circuit described here establishes a clipping level that is a function of the input signal. The result is a soft clamp function where the amplifier has one gain in its linear operating range and a user programmable lower gain when the output reaches an arbitrary threshold. The circuit may be used in imaging applications to expand the contrast of low level signals. It can be used in audio circuits to avoid generation of objectionable harmonics due to hard clipping. It also has application in control loops that otherwise would become unstable when their error amplifiers saturate. This circuit can be used in a broad range of applications that require a combination of high sensitivity for low level signals and wide dynamic range.

The basic soft clipping circuit, based on the HFA1135, is shown in Figure 9. The nominal value of R_1 is 1.5kΩ which is the optimum feedback resistor for the HFA1135. Hard clamping results with R_2 and R_4 shorted, and R_3 and R_5 removed. Figure 10 illustrates the hard clamping operation with a 100kHz input signal and clamp levels set at ±1V. The circuit has unity gain for inputs that fall between the clamp levels. The addition of R_2 through R_5 make the clamp level a function of the input signal. The output for signals in excess of V_{CH} (Voltage Clamp High) is given by:

$$V_O = (V_{IN}R_2 + V_{CH}R_3) / (R_2 + R_3).$$

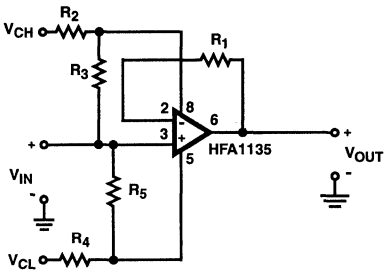

FIGURE 9. HFA1135 OUTPUT LIMITING AMPLIFIER CONFIGURED FOR SOFT LIMITING

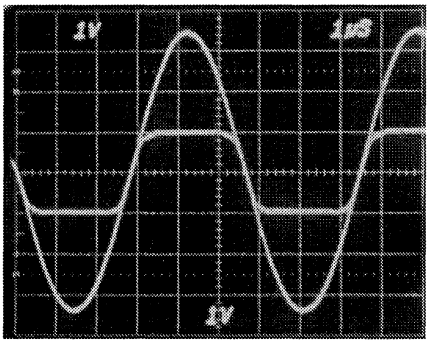

FIGURE 10. HARD CLIPPING RESULTS FROM A GAIN OF ZERO ABOVE THE CLAMP LEVEL

Figure 11 shows the result with R_2 and R_4 set to 1kΩ, and R_3 and R_5 set to 5kΩ. The gain for signals greater than 1V is 1/6. In Figure 12, R_2 through R_5 have been set to 1kΩ, and the gain above 1V is 1/2. Note that the high and low clamp levels need not be symmetrical, and the attenuation factors above and below those levels may be different.

Limiting amplifiers are frequently used at the front end of systems to accommodate wide dynamic range signals that may extend beyond the common mode range of the system.

While the circuit in Figure 9 performs soft clipping, it is restricted to signals within the ±2.4V input voltage range of the HFA1135. The circuit in Figure 13 incorporates an additional clamp network that allows the circuit to be used with signals that exceed the input voltage range. Using the values shown, the circuit has unity gain for signals that range between ±1V. The gain for inputs beyond that range is 1/6. Soft clipping works for signals up to ±9.4V which is well in excess of the ±5V power supply levels for the HFA1135.

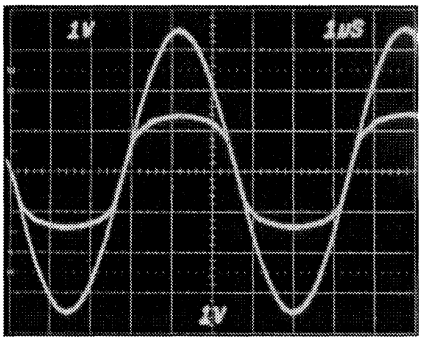

FIGURE 11. SOFT CLIPPING WITH A GAIN OF 1/6 ABOVE THE CLAMP LEVEL

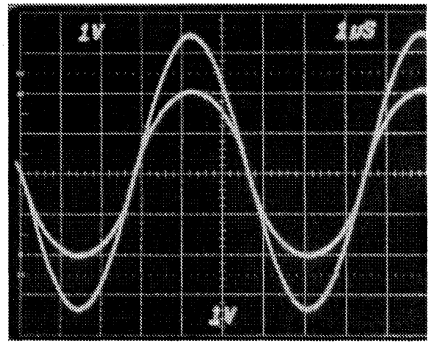

FIGURE 12. SOFT CLIPPING WITH A GAIN OF 1/2 ABOVE THE CLAMP LEVEL

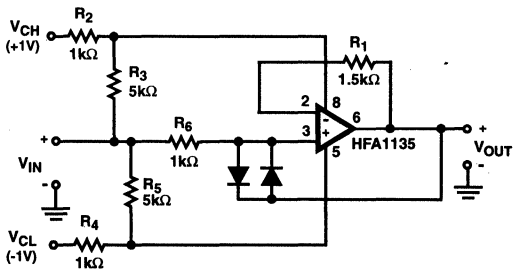

FIGURE 13. SOFT CLIPPING CIRCUIT WITH EXTENDED INPUT RANGE

Harris Semiconductor

TechBrief

No. TB334 September 1995

Guidelines for Soldering Surface Mount Components to PC Boards

Author: Maury Rosenfield

The most commonly used techniques for mounting SMDs (Surface Mounted Devices) to PC boards are Infrared (IR) and Vapor Phase (VP) reflow. IR and VP reflow are preferred over wave soldering. Wave soldering typically involves increased heating rate, higher temperatures and increased flux exposure.

The dynamics of the reflow process are influenced by the type of equipment used. The variables involved must be understood to properly control the board level interconnection of SMDs.

The primary phases of the reflow process are: flux activation, melting the solder particles in the solder paste, wetting the surfaces to be joined, and solidifying the solder into a strong metallurgical bond

Optimum fusing of the component leads with the solder paste on the board is achieved when the leads attain the melting temperature of the plated solder alloy. To avoid thermal shock of the SMDs the maximum heating and cooling rates (i.e., ramp rate) should be controlled.

IR Reflow

The IR reflow technique involves thermal energy supplied via lamps radiating at a given range of wavelength. This heating approach in its basic form is essentially a line-of-sight surface-heating technique. Therefore, the amount of thermal energy absorbed varies with board size, component size, component orientation, and materials used. The surface temperature of the board is not uniform throughout and board edges tend to run 10°C to 20°C higher than the center. If not properly planned, component overheating is possible.

Vapor Phase Reflow

The vapor phase reflow technique uses vapor from a boiling inert fluorocarbon liquid. The heat of condensation provides a thermal constraint dependent on the liquid selected. A typical material in the industry has a boiling point of 215°C. PC board temperature exposure should be very uniform. With essentially no temperature gradient across the surface of the board, component location design rules for even heating is not significant compared to IR reflow.

Solder Profile Development

Heating Rate - To avoid thermal shock to sensitive components the maximum heating rate should be controlled. It is desirable to hold the heating rate to less than 5°C/s.

Preheat Zone - Boards should be preheated prior to the reflow step. Over-baking the solder paste and exceeding the glass transition temperature of the epoxy in FR-4 boards should be avoided. Depending on the type of IR or VP equipment, the temperature of the component and the PC board should be within the range from 105°C to 145°C.

Time above Solder Melting Point - It is recommended that the solder at the joint be kept above its melting point for sufficient time to flow and wet the lands and the leads. Depending on type of equipment and component size; time above 180°C could range from 10s to 150s. Extended duration above the solder melting point may damage the board and sensitive components. This value should be minimized but sufficient to allow for good solder joint formation.

Peak Reflow Temperature - The peak temperature of the solder joint during reflow should be high enough for adequate flux action and solder flow to obtain good wetting. The preferred peak temperatures for IR and VP reflow are 215°C - 220°C. Residence time at peak temperatures should be minimized.

Cooling Rate - The cooling rate of the solder joint after reflow is important because the faster the cooling rate, the smaller the grain size of the solder, and the higher the fatigue resistance. However, care should be taken to avoid an excessive temperature gradient resulting in potential damage due to mechanical stress.

Summary of Soldering Precautions

The soldering process can create a thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time for wave soldering must not exceed 260°C for 5s on the leads and case of the device.
6. After soldering is complete, forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

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LINEAR 11

PACKAGING INFORMATION

Linear Package Selection Guide

Using the Selection Guide:

The first character of each entry indicates the package type, while the number preceding the decimal point details the package lead count. Except for Can packages, the decimal point and succeeding numbers specify the package width in inches (e.g. __.15 = 150 mil width). The entire entry indicates the table containing the appropriate package dimensions (e.g. 8 lead PDIP dimensions are detailed in Table E8.3).

PART NUMBER	PDIP	SOIC, SSOP, TSSOP, PSOP	PLCC	CERDIP (F), SBDIP (D)	QUAD FLATPACK	CAN
CA124	E14.3	M14.15	-	-	-	-
CA1391	E8.3	-	-	-	-	-
CA1394	E8.3	-	-	-	-	-
CA139	E14.3	M14.15	-	F14.3	-	-
CA1458	E8.3	-	-	-	-	T8.C
CA1558	E8.3	-	-	-	-	T8.C
CA158	E8.3	M8.15	-	-	-	T8.C
CA224	E14.3	M14.15	-	-	-	-
CA239	E14.3	M14.15	-	F14.3	-	-
CA258	E8.3	M8.15	-	-	-	T8.C
CA2904	E8.3	M8.15	-	-	-	-
CA3018	-	-	-	-	-	T12.B
CA3020	-	-	-	-	-	T12.B
CA3028	E8.3	M8.15	-	-	-	T8.C
CA3039	-	M14.15	-	-	-	T12.B
CA3045	-	-	-	F14.3, D14.3	-	-
CA3046	E14.3	M14.15	-	-	-	-
CA3049	-	-	-	-	-	T12.B
CA3053	E8.3	-	-	-	-	T8.C
CA3054	E14.3	M14.15	-	-	-	-
CA3060	E16.3	-	-	-	-	-
CA3078	E8.3	M8.15	-	-	-	T8.C
CA3080	E8.3	M8.15	-	-	-	T8.C
CA3081	E16.3	M16.15	-	F16.3	-	-
CA3082	E16.3	M16.15	-	F16.3	-	-
CA3083	E16.3	M16.15	-	F16.3	-	-
CA3086	E14.3	M14.15	-	F14.3	-	-
CA3089	E16.3	M20.3	-	-	-	-
CA3094	E8.3	M8.15	-	-	-	T8.C
CA3096	E16.3	M16.15	-	-	-	-
CA3098	E8.3	-	-	-	-	-
CA3100	E8.3	M8.15	-	-	-	T8.C
CA3102	E14.3	M14.15	-	-	-	-
CA3126	E16.3	M20.3	-	-	-	-

EXAMPLE: M 16 .15

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Linear Package Selection Guide

PART NUMBER	PDIP	SOIC, SSOP, TSSOP, PSOP	PLCC	CERDIP (F), SBDIP (D)	QUAD FLATPACK	CAN
CA3127	E16.3	M16.15	-	-	-	-
CA3130	E8.3	M8.15	-	-	-	T8.C
CA3140	E8.3	M8.15	-	-	-	T8.C
CA3141	E16.3	-	-	-	-	-
CA3146	E14.3	M14.15	-	-	-	-
CA3160	E8.3	-	-	-	-	T8.C
CA3183	E16.3	M16.15	-	-	-	-
CA3189	E16.3	-	-	-	-	-
CA3193	E8.3	-	-	-	-	T8.C
CA3227	E16.3	M16.15	-	-	-	-
CA324	E14.3	M14.15	-	-	-	-
CA3240	E8.3, E14.3	-	-	-	-	-
CA3246	E14.3	M14.15	-	-	-	-
CA3256	E18.3	M20.3	-	-	-	-
CA3260	E8.3	-	-	-	-	T8.C
CA3280	E16.3	-	-	F16.3	-	-
CA3290	E8.3, E14.3	-	-	-	-	T8.C
CA339	E14.3	M14.15	-	-	-	-
CA3420	E8.3	-	-	-	-	T8.C
CA3440	E8.3	M8.15	-	-	-	-
CA3450	E16.3	-	-	-	-	-
CA358	E8.3	M8.15	-	-	-	T8.C
CA5130	E8.3	M8.15	-	-	-	T8.C
CA5160	E8.3	M8.15	-	-	-	T8.C
CA5260	E8.3	M8.15	-	-	-	-
CA5420	E8.3	M8.15	-	-	-	T8.C
CA5470	E14.3	M14.15	-	-	-	-
CA555	E8.3	M8.15	-	-	-	T8.C
CA741	E8.3	-	-	-	-	T8.C
CD22402	E24.6	-	-	D24.6	-	-
HA-2400	-	-	-	F16.3	-	-
HA-2404	-	-	-	F16.3	-	-
HA-2405	E16.3	-	-	F16.3	-	-
HA-2406	E16.3	M16.3	-	F16.3	-	-
HA-2420	-	-	-	F14.3	-	-
HA-2425	E14.3	M14.15	N20.35	F14.3	-	-
HA-2444	E16.3	M16.3	-	-	-	-
HA-2500	-	-	-	F8.3A	-	T8.C
HA-2502	-	-	-	F8.3A	-	T8.C

EXAMPLE: **M 16 .15**

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Linear Package Selection Guide

PART NUMBER	PDIP	SOIC, SSOP, TSSOP, PSOP	PLCC	CERDIP (F), SBDIP (D)	QUAD FLATPACK	CAN
HA-2505	E8.3	-	-	F8.3A	-	T8.C
HA-2510	-	-	-	F8.3A	-	T8.C
HA-2512	-	-	-	F8.3A	-	T8.C
HA-2515	E8.3	-	-	F8.3A	-	T8.C
HA-2520	-	-	-	F8.3A	-	T8.C
HA-2522	-	-	-	F8.3A	-	T8.C
HA-2525	E8.3	M8.15	N20.35	F8.3A	-	T8.C
HA-2529	E8.3	M8.15	-	F8.3A	-	T8.C
HA-2539	E14.3	M14.15	-	F14.3	-	-
HA-2540	E14.3	M14.15	-	F14.3	-	-
HA-2541	-	-	-	F14.3	-	T12.C
HA-2542	E14.3	-	-	F14.3	-	T12.C
HA-2544	E8.3	M8.15	-	F8.3A	-	T8.C
HA-2546	E16.3	M16.3	-	F16.3	-	-
HA-2547	-	-	-	F16.3	-	-
HA-2548	E8.3	M16.3	-	D8.3	-	T8.C
HA-2556	E16.3	M16.3	-	F16.3	-	-
HA-2557	E16.3	M16.3	-	F16.3	-	-
HA-2600	-	-	-	F8.3A	-	T8.C
HA-2602	-	-	-	F8.3A	-	T8.C
HA-2605	E8.3	M8.15	-	F8.3A	-	T8.C
HA-2620	-	-	-	F8.3A	-	T8.C
HA-2622	-	-	-	F8.3A	-	T8.C
HA-2625	E8.3	M8.15	-	F8.3A	-	T8.C
HA-2640	-	-	-	F8.3A	-	T8.C
HA-2645	-	-	-	F8.3A	-	T8.C
HA-2839	E14.3	-	-	F14.3	-	-
HA-2840	E8.3, E14.3	M8.15	-	F8.3A	-	-
HA-2841	E8.3, E14.3	M8.15	-	-	-	-
HA-2842	E8.3, E14.3	M8.15	-	-	-	-
HA-2850	E8.3, E14.3	M8.15	-	-	-	-
HA4201	E8.3	M8.15	-	-	-	-
HA4244	-	M8.15	-	-	-	-
HA4314B	E14.3	M14.15	-	-	-	-
HA4344B	E16.3	M16.15	-	-	-	-
HA4404B	E16.3	M16.15	-	-	-	-
HA456	-	-	N44.65	-	Q44.10X10	-
HA457	-	-	-	-	Q44.10X10	-
HA4600	E8.3	M8.15	-	-	-	-

EXAMPLE: **M 16 .15**

Linear Package Selection Guide

PART NUMBER	PDIP	SOIC, SSOP, TSSOP, PSOP	PLCC	CERDIP (F), SBDIP (D)	QUAD FLATPACK	CAN
HA-4741	E14.3	M16.3	-	F14.3	-	-
HA-4900	-	-	-	F16.3	-	-
HA-4902	-	-	-	F16.3	-	-
HA-4905	E16.3	M16.3	N20.35	F16.3	-	-
HA-5002	E8.3	M8.15	N20.35	F8.3A	-	T8.C
HA-5004	-	-	-	F14.3	-	-
HA5013	E14.3	M14.15	-	-	-	-
HA-5020	E8.3	M8.15	-	F8.3A	-	-
HA5022	E16.3	M16.15	-	-	-	-
HA5023	E8.3	M8.15	-	-	-	-
HA5024	E20.3	M20.3	-	-	-	-
HA5025	E14.3	M14.15	-	-	-	-
HA-5033	E8.3	M8.15A	-	-	-	T12.C
HA-5101	E8.3	M8.15	-	F8.3A	-	T8.C
HA-5102	E8.3	M16.3	-	F8.3A	-	T8.C
HA-5104	E14.3	M16.3	-	F14.3	-	-
HA-5111	E8.3	M8.15	-	F8.3A	-	-
HA-5112	E8.3	M16.3	-	F8.3A	-	-
HA-5114	E14.3	M16.3	-	F14.3	-	-
HA-5127	E8.3	M8.15	-	F8.3A	-	-
HA-5130	-	-	-	F8.3A	-	T8.C
HA-5134	-	-	-	F14.3	-	-
HA-5135	-	-	-	F8.3A	-	T8.C
HA-5137	E8.3	M8.15	-	F8.3A	-	-
HA-5142	E8.3	M16.3	-	F8.3A	-	T8.C
HA-5144	E14.3	M16.3	-	F14.3	-	-
HA-5147	E8.3	-	-	F8.3A	-	T8.C
HA-5160	-	-	-	-	-	T8.C
HA-5162	-	-	-	-	-	T8.C
HA-5170	-	-	-	F8.3A	-	T8.C
HA-5177	E8.3	-	-	F8.3A	-	-
HA-5190	-	-	-	F14.3	-	T12.C
HA-5195	-	M14.15	-	F14.3	-	T12.C
HA-5221	E8.3	M8.15	-	F8.3A	-	T8.C
HA-5222	E16.3	M16.3	-	F8.3A	-	-
HA-5320	E14.3	M16.3	-	F14.3	-	-
HA-5330	E14.3	-	-	F14.3	-	-
HA-5340	E14.3	M16.3	-	F14.3	-	-
HA5351	E8.3	M8.15	-	-	-	-

EXAMPLE: **M 16 .15**

Linear Package Selection Guide

PART NUMBER	PDIP	SOIC, SSOP, TSSOP, PSOP	PLCC	CERDIP (F), SBDIP (D)	QUAD FLATPACK	CAN
HA7210	E8.3	M8.15	-	-	-	-
HA7211	-	M8.15	-	-	-	-
HFA1100	E8.3	M8.15	-	F8.3A	-	-
HFA1102	E8.3	M8.15	-	F8.3A	-	-
HFA1103	E8.3	M8.15	-	-	-	-
HFA1105	E8.3	M8.15	-	-	-	-
HFA1106	E8.3	M8.15	-	-	-	-
HFA1109	E8.3	M8.15	-	-	-	-
HFA1110	E8.3	M8.15	-	F8.3A	-	-
HFA1112	E8.3	M8.15	-	F8.3A	-	-
HFA1113	E8.3	M8.15	-	F8.3A	-	-
HFA1114	E8.3	M8.15	-	-	-	-
HFA1115	E8.3	M8.15		-	-	-
HFA1118	E8.3	M8.15	-	-	-	-
HFA1119	E8.3	M8.15	-	-	-	-
HFA1120	E8.3	M8.15	-	F8.3A	-	-
HFA1130	E8.3	M8.15	-	F8.3A	-	-
HFA1135	E8.3	M8.15	-	-	-	-
HFA1145	E8.3	M8.15	-	-	-	-
HFA1149	E8.3	M8.15	-	-	-	-
HFA1205	E8.3	M8.15	-	-	-	-
HFA1212	E8.3	M8.15	-	-	-	-
HFA1245	E14.3	M14.15	-	-	-	-
HFA1405	E14.3	M14.15	-	-	-	-
HFA1412	E14.3	M14.15	-	-	-	-
HFA3046	-	M14.15	-	-	-	-
HFA3096	-	M16.15	-	-	-	-
HFA3101	-	M8.15	-	-	-	-
HFA3102	-	M14.15	-	-	-	-
HFA3127	-	M16.15	-	-	-	-
HFA3128	-	M16.15	-	-	-	-
HFA3600	-	M14.15	-	-	-	-
HFA5250	-	M28.3	-	-	-	-
HFA5253	-	M20.3A	-	-	-	-
ICL7611	E8.3	M8.15	-	-	-	T8.C
ICL7612	E8.3	M8.15	-	-	-	T8.C
ICL7621	E8.3	M8.15	-	-	-	T8.C
ICL7641	E14.3	-	-	-	-	-
ICL7642	E14.3	-	-	-	-	-

EXAMPLE: **M 16 .15**

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

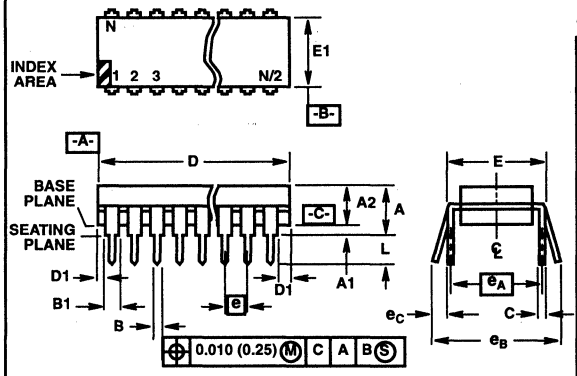
Linear Package Selection Guide

PART NUMBER	PDIP	SOIC, SSOP, TSSOP, PSOP	PLCC	CERDIP (F), SBDIP (D)	QUAD FLATPACK	CAN
ICL7650S	E8.3, E14.3	M8.15, M14.15	-	F14.3	-	T8.C
ICL8013	-	-	-	-	-	T10.C
ICL8038	E14.3	-	-	F14.3	-	-
ICM7242	E8.3	M8.15	-	-	-	-
ICM7555	E8.3	M8.15	-	-	-	T8.C
ICM7556	E14.3	-	-	F14.3	-	-
LM1458	E8.3	-	-	-	-	-
LM2901	E14.3	M14.15	-	-	-	-
LM2902	E14.3	M14.15	-	-	-	-
LM2904	E8.3	-	-	-	-	-
LM324	E14.3	-	-	-	-	-
LM3302	E14.3	M14.15	-	-	-	-
LM339	E14.3	-	-	-	-	-
LM358	E8.3	-	-	-	-	-
LM555	E8.3	-	-	-	-	-
LM741	E8.3	-	-	-	-	T8.C

EXAMPLE: **M 16 .15**

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

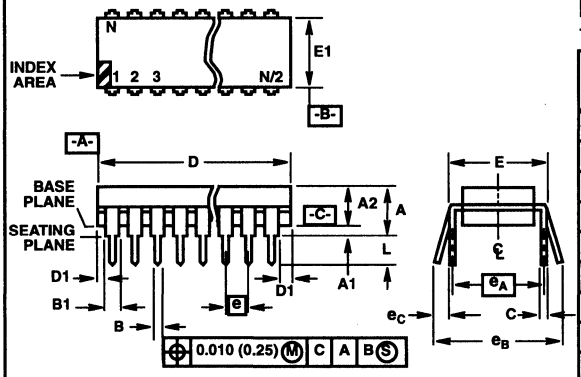
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

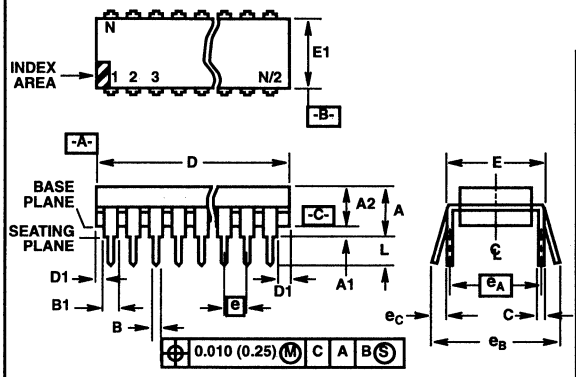
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

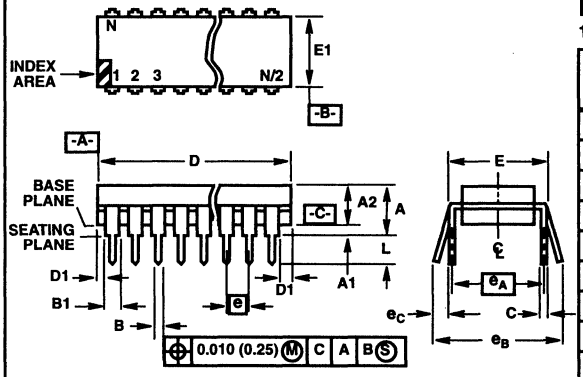
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E18.3 (JEDEC MS-001-BC ISSUE D)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

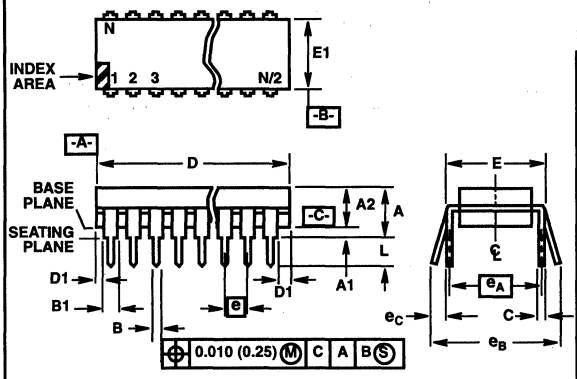
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.845	0.880	21.47	22.35	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

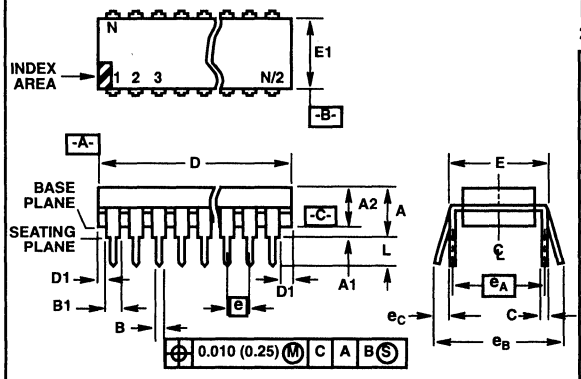
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

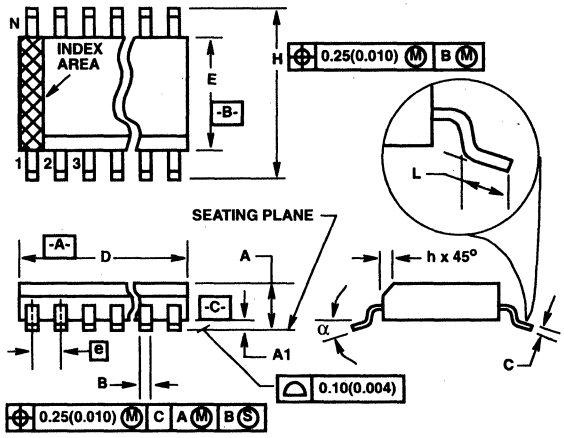
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

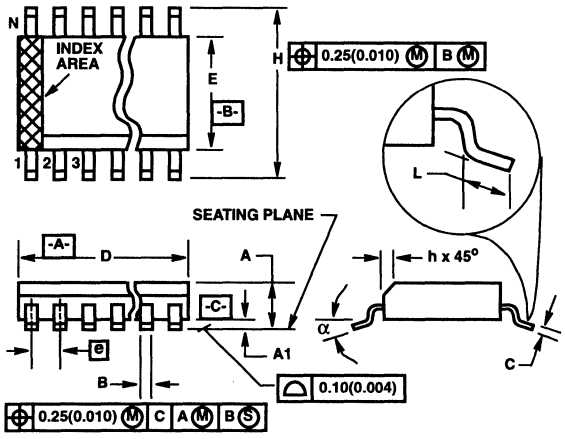
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

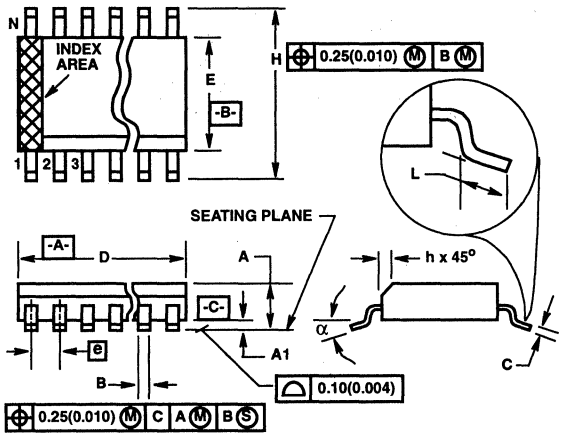
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

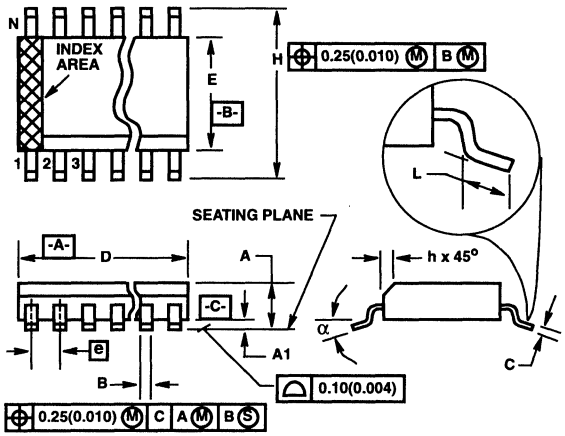
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

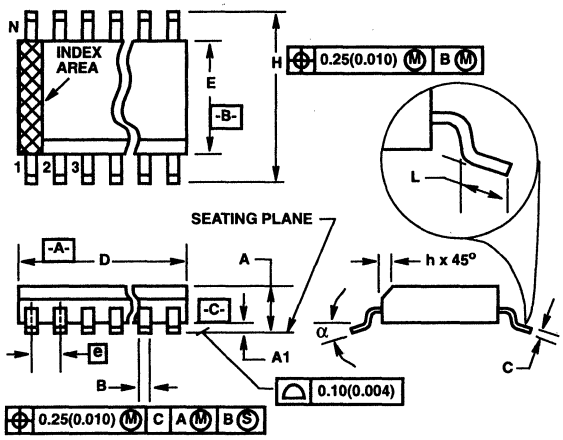
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

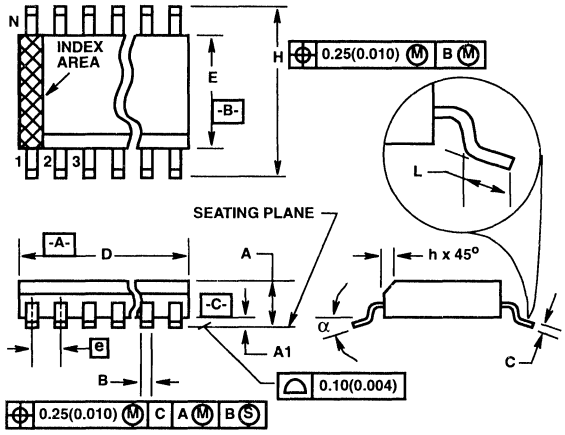
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

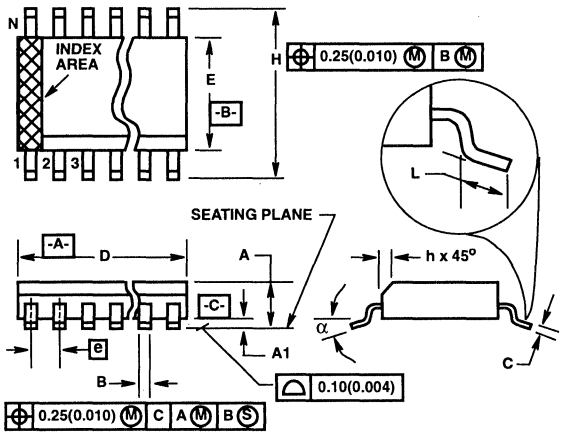
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

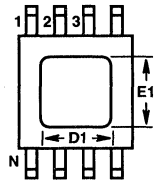
NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Power Small Outline Plastic Packages (PSOP)



BOTTOM VIEW



POWER SOP PACKAGE
(HEAT SLUG SURFACE IS ELECTRICALLY FLOATING)

M8.15A

8 LEAD POWER SMALL OUTLINE PLASTIC PACKAGE

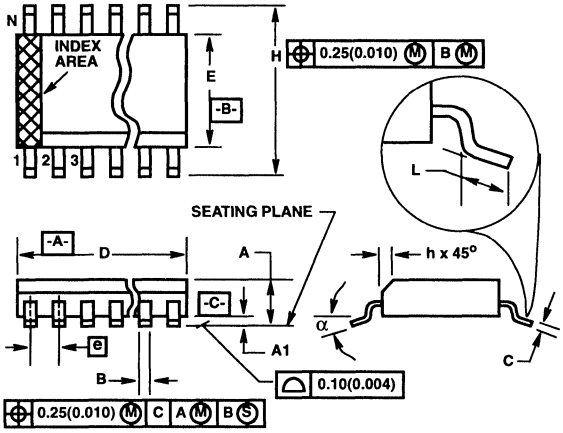
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.0130	0.0200	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
D1	0.107	0.123	2.72	3.12	10
E	0.1497	0.1574	3.80	4.00	4
E1	0.071	0.087	1.80	2.21	10
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

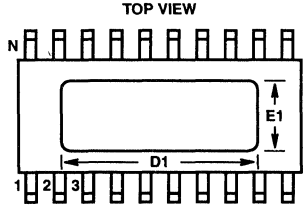
Rev. 0 10/96

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Exposed copper heat slug flush with bottom surface of package. All other dimensions conform to JEDEC MS-012 Issue C.
11. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Power Small Outline Plastic Packages (PSOP)





POWER SOP PACKAGE
(HEAT SLUG SURFACE IS ELECTRICALLY FLOATING)

M20.3A

20 LEAD POWER SMALL OUTLINE PLASTIC PACKAGE

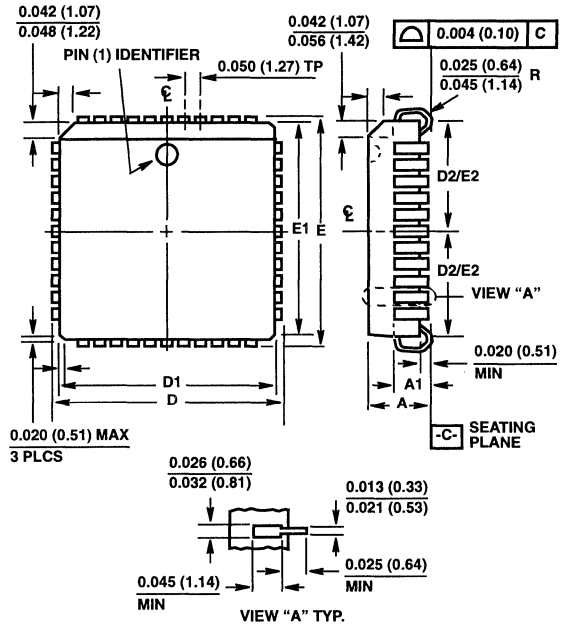
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
D1	0.325	0.340	8.25	8.63	10
E	0.2914	0.2992	7.40	7.60	4
E1	0.175	0.190	4.44	4.82	10
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 6/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Exposed copper heat slug flush with top surface of package. All other dimensions conform to JEDEC MS-013AC Issue C.
11. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Plastic Leaded Chip Carrier Packages (PLCC)



N20.35 (JEDEC MS-018AA ISSUE A)
20 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

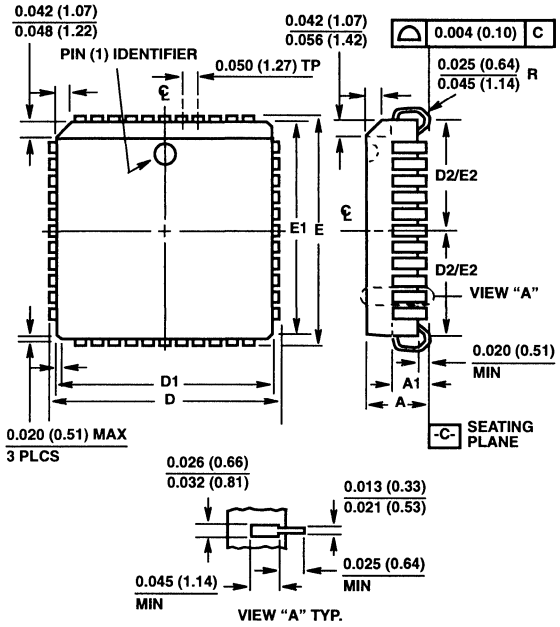
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.385	0.395	9.78	10.03	-
D1	0.350	0.356	8.89	9.04	3
D2	0.141	0.169	3.59	4.29	4, 5
E	0.385	0.395	9.78	10.03	-
E1	0.350	0.356	8.89	9.04	3
E2	0.141	0.169	3.59	4.29	4, 5
N	20		20		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N44.65 (JEDEC MS-018AC ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

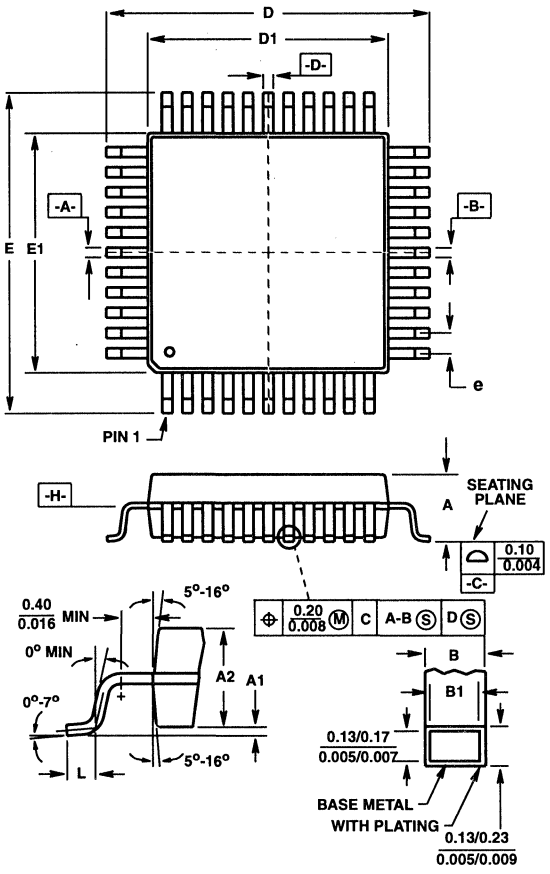
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q44.10x10 (JEDEC MO-108AA-2 ISSUE A)

44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

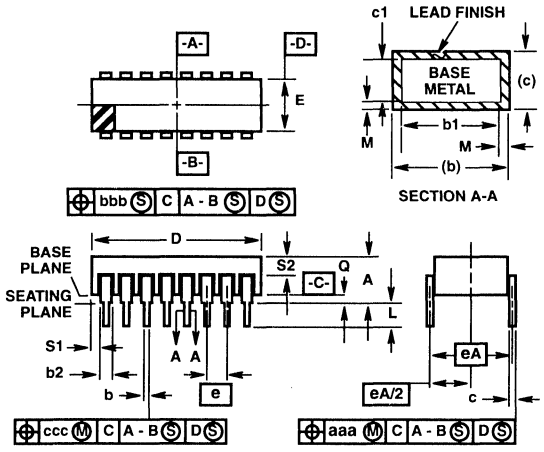
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.510	0.530	12.95	13.45	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.510	0.530	12.95	13.45	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 1 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D8.3 MIL-STD-1835 CDIP2-T8 (D-4, CONFIGURATION C)
8 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

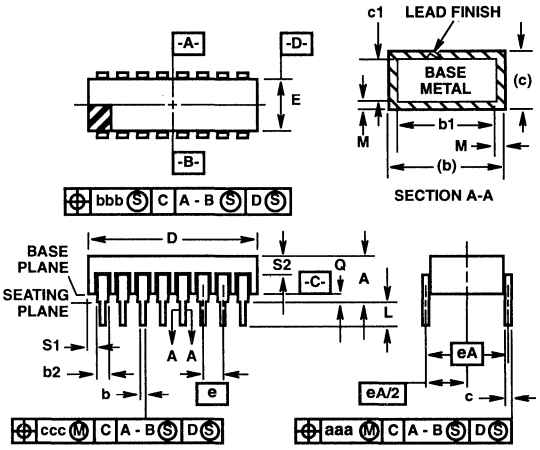
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

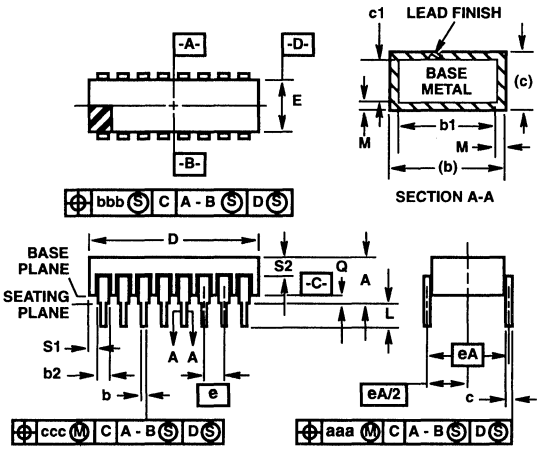
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D24.6 MIL-STD-1835 CDIP2-T24 (D-3, CONFIGURATION C)
24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

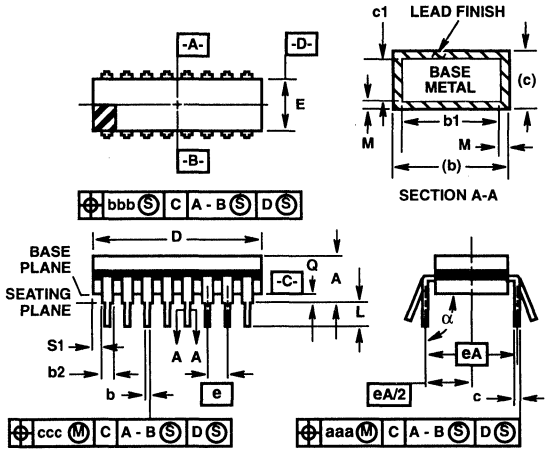
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

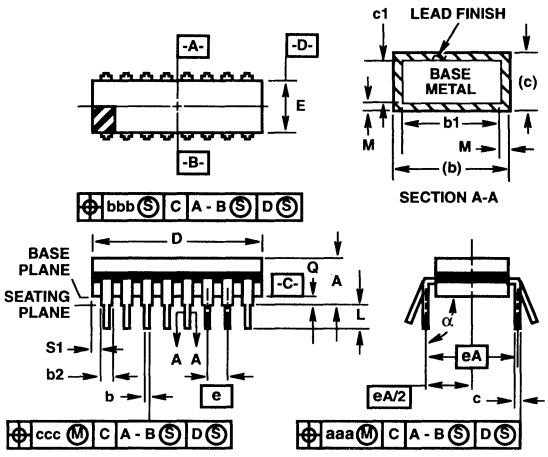
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

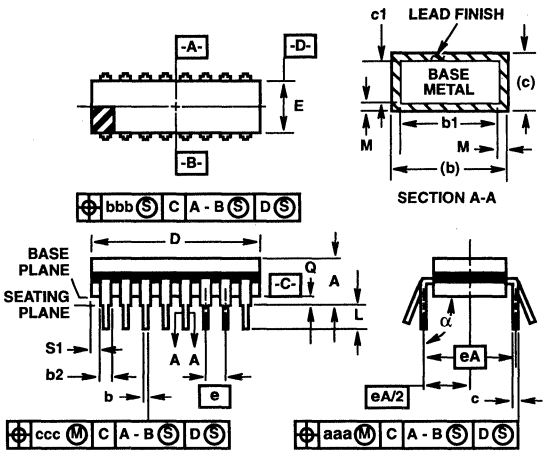
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

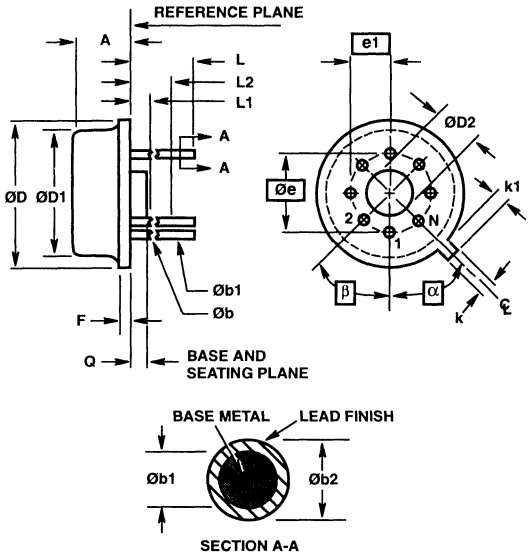
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Metal Can Packages (Can)



NOTES:

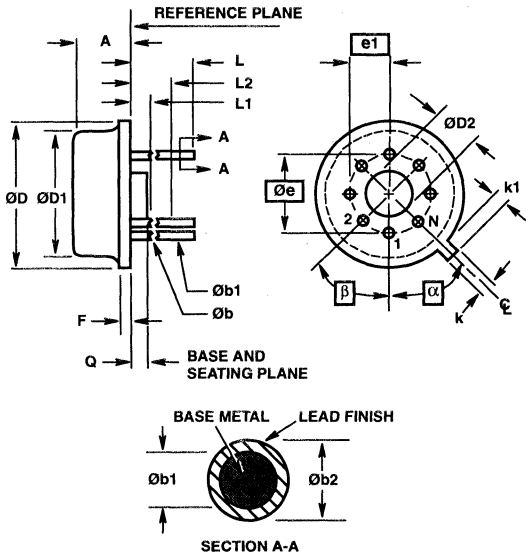
1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45^{o} BSC		45^{o} BSC		3
β	45^{o} BSC		45^{o} BSC		3
N	8		8		4

Rev. 0 5/18/94

Metal Can Packages (Can)



T10.C

10 LEAD METAL CAN PACKAGE

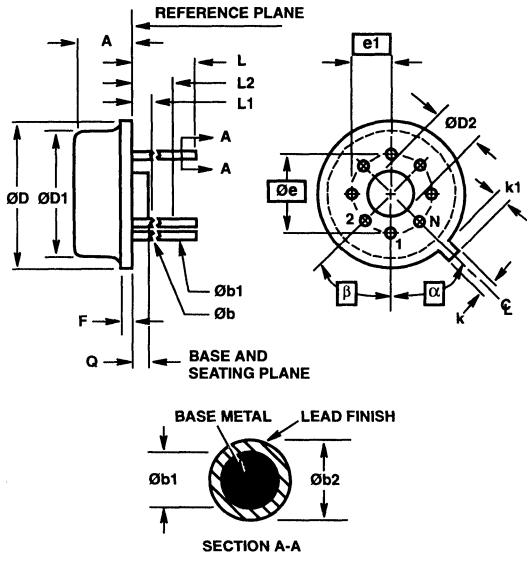
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	-	-	-	-	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	-	-	-	-	-
α	36° BSC		36° BSC		3
β	36° BSC		36° BSC		3
N	10		10		4

Rev. 0 5/18/94

NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

Metal Can Packages (Can)



NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

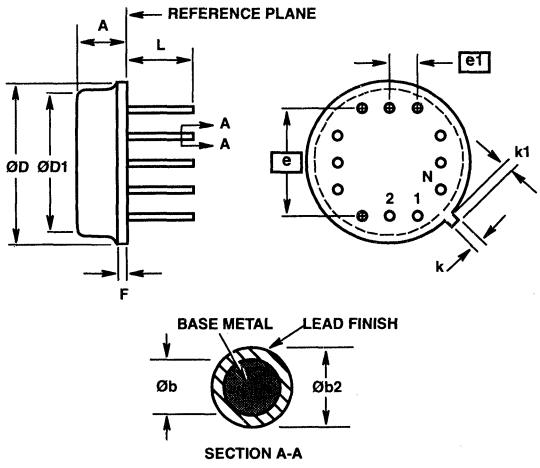
T12.B

12 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	-	-	-	-	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	-	-	-	-	-
α	30^{o} BSC		30^{o} BSC		3
β	30^{o} BSC		30^{o} BSC		3
N	12		12		4

Rev. 0 5/18/94

Metal Can Packages (Can)



T12.C

12 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.30	3.81	-
Øb	0.016	0.019	0.41	0.48	-
Øb2	0.016	0.021	0.41	0.53	-
ØD	0.585	0.615	14.86	15.62	-
ØD1	0.540	0.560	13.72	14.22	-
e	0.400 BSC		10.16 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	0.020	0.040	0.51	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.560	12.70	14.22	-
N	12		12		3

Rev. 0 5/18/94

NOTES:

1. The reference, base, and seating planes are the same for this variation.
2. Measured from maximum diameter of the product.
3. N is the maximum number of terminal positions.
4. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
5. Controlling dimension: INCH.

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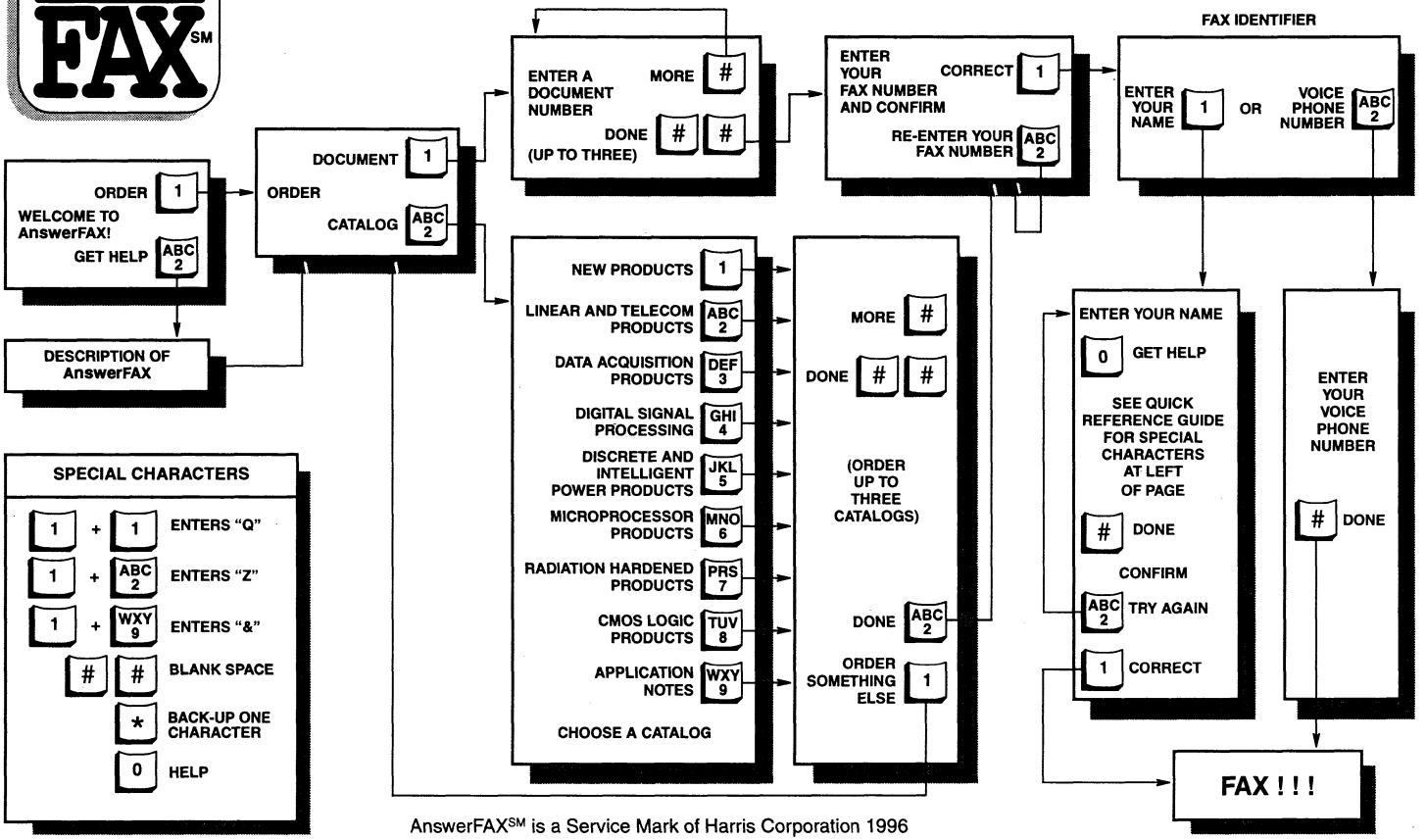

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	PSG201.23	**PRODUCT SELECTION GUIDE** (1996: 834pp) Key product information on all Harris Semiconductor devices. Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric part number index.
	SG103	**CMOS LOGIC SELECTION GUIDE** (1994: 288pp) This product selection guide contains technical information on Harris Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.
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1929	CA5260	BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output (5 pages)
1925	CA5420	Low Supply Voltage, Low Input Current BiMOS Operational Amplifier (7 pages)
1946	CA5470	Quad Microprocessor BiMOS-E Operational Amplifiers with MOSFET Input/Bipolar Output (5 pages)
1686	CD22402	Sync Generator for TV Applications and Video Processing Systems (10 pages)
2891	HA-2400, HA-2404, HA-2405	PRAM Four Channel Programmable Amplifiers (6 pages)
3926	HA-2400/883	PRAM Four Channel Programmable Operational Amplifier (11 pages)
2892	HA-2406	Digitally Selectable Four Channel Operational Amplifier (6 pages)
2856	HA-2420, HA-2425	Fast Sample and Hold Amplifiers (9 pages)
2490	HA-2444	Selectable, Four Channel Video Operational Amplifier (3 pages)
3608	HA-2444/883	Selectable, Four Channel Video Operational Amplifier (8 pages)
2890	HA-2500, HA-2502, HA-2505	Precision High Slew Rate Operational Amplifiers (6 pages)
3734	HA-2500/883, HA-2502/883	Precision High Slew Rate Operational Amplifiers (10 pages)
2893	HA-2510, HA-2512, HA-2515	High Slew Rate Operational Amplifiers (5 pages)
3697	HA-2510/883, HA-2512/883	High Slew Rate Operational Amplifiers (11 pages)

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3735	HA-2520/883, HA-2522/883	Uncompensated, High Slew Rate Operational Amplifiers (11 pages)
2895	HA-2529	Uncompensated, High Slew Rate High Output Current, Operational Amplifier (7 pages)
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2899	HA-2542	Wideband, High Slew Rate, High Output Current Operational Amplifier (10 pages)
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3699	HA-2544/883	Video Operational Amplifier (13 pages)
2861	HA-2546	Wideband Two Quadrant Analog Multiplier (13 pages)
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2904	HA-2640, HA-2645	High Voltage Operational Amplifiers (6 pages)
3702	HA-2640/883	High Voltage Operational Amplifier (11 pages)
2841	HA-2839	Very High Slew Rate Wideband Operational Amplifier (8 pages)
3593	HA-2839/883	Very High Slew Rate, Wideband Operational Amplifier (13 pages)
2842	HA-2840	Very High Slew Rate Wideband Operational Amplifier (8 pages)
3594	HA-2840/883	Very High Slew Rate, Wideband Operational Amplifier (13 pages)
2843	HA-2841	Wideband, Fast Settling, Unity Gain Stable, Video Operational Amplifier (9 pages)
3621	HA-2841/883	Wideband, Fast Settling, Unity Gain Stable, Video Operational Amplifier (14 pages)
2766	HA-2842	Wideband, High Slew Rate, High Output Current, Video Operational Amplifier (9 pages)

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3595	HA-2850/883	Low Power, High Slew Rate, Wideband Operational Amplifier (13 pages)
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2855	HA-4900, HA-4902, HA-4905	Precision Quad Comparator (8 pages)
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2909	HA-5142, HA-5144	Dual/Quad Ultra-Low Power Operational Amplifiers (7 pages)
3732	HA-5142/883	Dual, Ultra Low Power Operational Amplifier (12 pages)
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3715	HA-5147/883	Ultra Low Noise, Precision, High Slew Rate Wideband Operational Amplifier (13 pages)
2911	HA-5160, HA-5162	Wideband, JFET Input High Slew Rate, Uncompensated, Operational Amplifiers (8 pages) FN2911.2
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2927	HA-5320/883	High Speed Precision Sample and Hold Amplifier (12 pages)
2858	HA-5330	Very High Speed Precision Monolithic Sample and Hold Amplifier (4 pages)
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96182	**CA3058, CA3059, CA3079** AN6182	Features and Applications of Integrated Circuit Zero-Voltage Switches (CA3059 and CA3079) (31 pages)

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96077	**CA3094, OTA** AN6077	An IC Operational-Transconductance-Amplifier (OTA) With Power Capability (12 pages)
96459	**CA3130** AN6459	Why Use the CMOS Operational Amplifiers and How to Use it (4 pages)
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