DECEMBER 1974

HARRIS SEMICONDUCTOR

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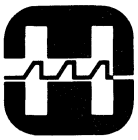
HARRIS SEMICONDUCTOR CMOS

Harris
CMOS DATA BOOK

This data book is your complete guide to CMOS. Full descriptions of devices featuring low power dissipation, high noise immunity, and wide power supply voltage ranges, are available for both the popular 54C/74C and 4000 series logic families. Harris is pleased to be a fully qualified supplier of both CMOS logic families with total pin for pin and function for function compatibility. A handy cross reference guide is located at the front of the book cross referencing alternate sources both by manufacturer and by device function. For additional convenience each logic family section is preceeded by a complete index of product availability. Users of CMOS will decide for themselves the relative merits of 54C/74C and 4000 series product. Whatever the relative merits, users of Harris CMOS will have the added advantages of being able to obtain both from a single manufacturer.

December 1974



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cross-reference guide

HD-54C/74C* SERIES
MANUFACTURER CROSS REFERENCE

FUNCTION	HARRIS	NATIONAL	TELEDYNE	PAGE REFERENCE
Quad 2 Input NAND	HD-74C00	MM74C00	MM74C00	3 - 2
Quad 2 Input NOR	HD-74C02	MM74C02	MM74C02	3 - 2
Hex Inverter	HD-74C04	MM74C04	MM74C04	3 - 2
Quad 2 Input AND	HD-74C08	MM74C08	MM74C08	3 - 6
Triple 3 Input NAND	HD-74C10	MM74C10	–	3 - 2
Hex Schmitt Trigger	HD-74C14	MM74C14	–	3 - 9
Dual 4 Input NAND	HD-74C20	MM74C20	MM74C20	3 - 2
8 Input NAND	HD-74C30	MM74C30	–	3 - 10
Quad 2 Input OR	HD-74C32	MM74C32	–	3 - 10
BCD to Decimal Decoder	HD-74C42	MM74C42	MM74C42	3 - 11
BCD to 7 Segment Decoder	HD-74C48	MM74C48	–	3 - 13
Dual J-K Flip-Flops with Clear	HD-74C73	MM74C73	MM74C73	3 - 14
Dual D Flip-Flop	HD-74C74	MM74C74	MM74C74	3 - 17
Dual J-K Flip-Flops with Clear and Preset	HD-74C76	MM74C76	MM74C76	3 - 14
4 Bit Binary Full Adder	HD-74C83	MM74C83	–	3 - 20
4 Bit Magnitude Comparator	HD-74C85	MM74C85	–	3 - 21
Quad 2 Input Exclusive OR	HD-74C86	MM74C86	–	3 - 6
64 Bit Three State Random Access Read/Write Memory	HD-74C89	MM74C89	–	3 - 24
4 Bit Right-Shift Left-Shift Register	HD-74C95	MM74C95	MM74C95	3 - 28
Dual J-K Flip-Flops with Clear	HD-74C107	MM74C107	MM74C107	3 - 14
8 Channel Digital Multiplexer	HD-74C151	MM74C151	MM74C151	3 - 10
4 Line to 16 Line Decoder/ Demultiplexer	HD-74C154	MM74C154	MM74C154	3 - 33
Quad 2 Input Multiplexers	HD-74C157	MM74C157	MM74C157	3 - 35
Decade Counter with Asynchronous Clear	HD-74C160	MM74C160	MM74C160	3 - 37
Binary Counter with Asynchronous Clear	HD-74C161	MM74C161	MM74C161	3 - 37
Decade Counter with Synchronous Clear	HD-74C162	MM74C162	MM74C162	3 - 37
Binary Counter with Synchronous Clear	HD-74C163	MM74C163	MM74C163	3 - 37
8 Bit Parallel Out Serial Shift Register	HD-74C164	MM74C164	MM74C164	3 - 40
Parallel Load 8 Bit Shift Register	HD-74C165	MM74C165	–	3 - 43

* All Listed 74C Devices Are Available Also As 54C.

FUNCTION	HARRIS	NATIONAL	TELEDYNE	PAGE REFERENCE
Three State Quad D Flip-Flop	HD-74C173	MM74C173	MM74C173	3 - 44
Hex D Flip-Flop	HD-74C174	MM74C174	–	3 - 46
Quad D Flip-Flop	HD-74C175	MM74C175	–	3 - 46
Synchronous 4 Bit Up/ Down Decade Counter	HD-74C192	MM74C192	MM74C192	3 - 47
Synchronous 4 Bit Up/ Down Binary Counter	HD-74C193	MM74C193	MM74C193	3 - 47
4 Bit Registers	HD-74C195	MM74C195	MM74C195	3 - 50
256 Bit Three State Random Access Read/Write Memory	HD-74C200	MM74C200	–	3 - 53
Dual Monostable Multivibrator	HD-74C221	MM74C221	–	3 - 56
Hex Inverting TTL Buffer	HD-74C901	MM74C901	–	3 - 57
Hex Non-Inverting TTL Buffer	HD-74C902	MM74C902	–	3 - 57
Hex Inverting PMOS Buffer	HD-74C903	MM74C903	–	3 - 57
Hex Non-Inverting PMOS Buffer	HD-74C904	MM74C904	–	3 - 57
Three State Hex Non-Inverting Buffer	HD-80C95**	MM80C95	–	3 - 61
Three State Hex Non-Inverting Buffer	HD-80C97**	MM80C97	–	3 - 61

*All Listed 74C Devices Are Also Available As 54C.
**All Listed 80C Devices Are Also Available As 70C.

HD-4000 SERIES
MANUFACTURER CROSS REFERENCE

FUNCTION	HARRIS	RCA	NATIONAL	MOTOROLA	PAGE REFERENCE
Dual 3 Input NOR Gate + Inverter	HD-4000	CD4000	–	MC14000	4 - 2
Quad 2 Input NOR	HD-4001	CD4001	MM4601	MC14001	4 - 5
Dual 4 Input NOR	HD-4002	CD4002	MM4602	MC14002	4 - 8
Dual Complementary Pair + Inverter	HD-4007	CD4007	–	MC14007	4 - 11
Quad 2 Input NAND	HD-4011	CD4011	MM4611	MC14011	4 - 14
Dual 4 Input NAND	HD-4012	CD4012	MM4612	MC14012	4 - 17
Dual D Flip-Flop	HD-4013	CD4013	MM4613	MC14013	4 -20
8 Stage Static Shift Register	HD-4014	CD4014	MM4614	MC14014	4 - 20
Dual 4 Static Shift Register	HD-4015	CD4015	–	MC14015	4 - 26
Decade Counter	HD-4017	CD4017	MM4617	MC14017	4 - 29
Preset/Divide by N Counter	HD-4018	CD4018	–	–	4 - 32
Quad AND/OR Select	HD-4019	CD4019	MM4619	–	4 - 35
14 Stage Binary/ Ripple Counter	HD-4020	CD4020	MM4620	MC14020	4 - 38
8 Stage Static Shift Register	HD-4021	CD4021	MM4621	MC14021	4 - 41
Divide by 8 Counter	HD-4022	CD4022	MM4622	MC14022	4 - 44
Triple 3 Input NAND	HD-4023	CD4023	MM4623	MC14023	4 - 47
7 Stage Binary Counter	HD-4024	CD4024	–	MC14024	4 - 50
Triple 3 Input NOR	HD-4025	CD4025	MM4625	MC14025	4 - 53
Dual J-K Flip-Flop	HD-4027	CD4027	MM4627	MC14027	4 - 56
BCD/Decimal Decoder	HD-4028	CD4028	–	MC14028	4 - 59
Preset Up-Down Counter	HD-4029	CD4029	–	–	4 - 62
Quad Exclusive OR	HD-4030	CD4030	MM4630	–	4 - 66
4 Stage Parallel In/ Parallel Out Shift Register	HD-4035	CD4035	MM4635	MC14035	4 - 69
12 Stage Binary/ Ripple Counter	HD-4040	CD4040	–	MC14040	4 - 72
Quad Clocked "D" Latch	HD-4042	CD4042	–	MC14042	4 - 75
Quad Three State L/S Latch NOR	HD-4043	CD4043	–	–	4 - 78
Quad Three State NAND R/S Latch	HD-4044	CD4044	–	–	4 - 78
Hex Buffer, Inverting	HD-4049	CD4049	MM4649	MC14049	4 - 81
Hex Buffer, Non-Inverting	HD-4050	CD4050	MM4650	MC14050	4 - 81
Quad Bilateral Switch	HD-4066	CD4066	MM4666	MC14066	4 - 84

FUNCTIONAL CROSS REFERENCE OF HD-4000 SERIES AND HD-54C/74C SERIES

(Does not imply pin compatibility)

ARITHMETIC FUNCTIONS	4000 SERIES	PAGE REFERENCE	54C/74C* SERIES	PAGE REFERENCE
Four Bit Binary Full Adder	—	—	HD-74C83	3 - 20
Four Bit Magnitude Comparator	—	—	HD-74C85	3 - 21
COUNTERS				
7 Stage Binary	HD-4024	4 - 50	—	—
12 Stage Ripple-Carry Binary	HD-4040	4 - 72	—	—
14 Stage Ripple-Carry Binary	HD-4020	4 - 38	—	—
Decade Counter/Divider + 10 Decoded Decimal Outputs	HD-4017	4 - 29	—	—
Divide by 8 Counter/Divider with 8 Decimal Outputs	HD-4022	4 - 44	—	—
Presettable Divide by "N" Counter Fixed or Programmable	HD-4018	4 - 32	—	—
Presettable Up/Down Counter Binary or BCD Decade	HD-4029	4 - 62	—	—
Synchronous Decade	—	—	HD-74C160	3 - 37
Synchronous Binary	—	—	HD-74C161	3 - 37
Fully Synchronous Decade	—	—	HD-74C162	3 - 37
Fully Synchronous Binary	—	—	HD-74C163	3 - 37
Synchronous Up/Down Decade	—	—	HD-74C192	3 - 47
Synchronous Up/Down Binary	—	—	HD-74C193	3 - 47
DECODERS/MULTIPLEXERS				
Quad Bilateral Switch	HD-4066	4 - 84	—	—
BCD to Decimal Decoders	HD-4028	4 - 59	HD-74C42	3 - 11
BCD to 7 Segment Decoder	—	—	HD-74C48	3 - 13
8 Channel Digital Multiplexer	—	—	HD-74C151	3 - 30
4 Line to 16 Line	—	—	HD-74C154	3 - 33
Quad 2 Input	—	—	HD-74C157	3 - 35

*All Listed 74C Devices Are Available Also As 54C.

FLIP-FLOPS	4000 SERIES	PAGE REFERENCE	54C/74C* SERIES	PAGE REFERENCE
Dual "D" with Set/Reset	HD-4013	4 - 20	HD-74C74	3 - 17
Dual "J-K" with Set/Reset	HD-4027	4 - 56	–	–
Quad Clocked "D" Latch	HD-4042	4 - 70	–	–
Quad Three State NOR Reset/Set Latch	HD-4043	4 - 78	–	–
Quad Three State NAND Reset/Set Latch	HD-4044	4 - 78	–	–
Dual "J-K" Master/Slave	–	–	HD-74C73	3 - 14
Dual "J-K" Master/Slave with Preset	–	–	HD-74C76	3 - 14
Dual "J-K"	–	–	HD-74C107	3 - 14
Quad "D" Three State (Quad Latch)	CD4076 (RCA)**	–	HD-74C173	3 - 44
Hex "D"	–	–	HD-74C174	3 - 46
Quad "D"	–	–	HD-74C175	3 - 46
GATES/BUFFERS/INVERTERS				
Dual 3 Input NOR Gate + Inverter	HD-4000	4 - 2	–	–
Quad 2 Input NOR	HD-4001	4 - 5	HD-74C02	3 - 2
Dual 4 Input NOR	HD-4002	4 - 8	–	–
Quad 2 Input NAND	HD-4011	4 - 14	HD-74C00	3 - 2
Dual 4 Input NAND	HD-4012	4 - 17	HD-74C20	3 - 2
Triple 3 Input NAND	HD-4023	4 - 47	HD-74C10	3 - 2
Triple 3 Input NOR	HD-4025	4 - 53	–	–
Hex Inverter	CD4069 (RCA)**	–	HD-74C04	3 - 2
Quad 2 Input AND	–		HD-74C08	3 - 6
8 Inputs NAND	–	–	HD-74C30	3 - 10
Quad 2 Input OR	–	–	HD-74C32	3 - 10
Quad 2 Input Exclusive OR	HD-4030**	4 - 66	HD-74C86	3 - 6
Quad AND-OR Select	HD-4019	4 - 35	–	–
Dual Complementary Pair + Inverter	HD-4007	4 - 11	–	–
Hex Buffer/Converter, Inverting	HD-4049	4 - 81	HD-74C901	3 - 57
Hex Buffer/Converter, Non-Inverting	HD-4050	4 - 81	HD-74C902	3 - 57
Hex Inverting PMOS Buffer	–	–	HD-74C903	3 - 57
Hex Non-Inverting PMOS Buffer	–	–	HD-74C904	3 - 57
Three State Hex Buffer	–	–	HD-80C95***	3 - 61
Three State Hex Buffer	–	–	HD-80C97***	3 - 61

*All Listed 74C Devices Are Also Available As 54C.
**Pin Compatible with 54C/74C.
***All Listed 80C Devices Are Available Also As 70C.

SHIFT REGISTERS	4000 SERIES	PAGE REFERENCE	54C/74C * SERIES	PAGE REFERENCE
Dual 4 Stage with Serial Input/ Parallel Output	HD-4015	4 - 26	–	–
8 Stage Synchronous Parallel Input/ Serial Output	HD-4014	4 - 23	HD-74C165	3 - 43
8 Stage Asynchronous Parallel Input/ Serial Output	HD-4021	4 - 41	–	–
4 Stage with J-$\overline{K}$ Input and True/ Complement Output	HD-4035	4 - 69	–	–
4 Bit Right-Shift Left-Shift	–	–	HD-74C95	3 - 28
8 Bit Serial-In Parallel Out	–	–	HD-74C164	3 - 40
4 Bit Parallel-In Parallel-Out	–	–	HD-74C195	3 - 50
SPECIAL FUNCTIONS				
Hex Schmitt Trigger	–	–	HD-74C14	3 - 9
Dual Monostable Multivibrator	–	–	HD-74C221	3 - 56
64 Bit Three State Random Access Read/Write Memory	–	–	HD-74C89	3 - 24
256 Bit Three State Random Access Read/Write Memory	–	–	HD-74C200	3 - 53

*All Listed 74C Devices Are Available Also As 54C.

technical introduction 2

Technical Introduction

CMOS, as a general category of logic circuits,has properties which make it unique. The potential for low power, high noise immunity, high fanout and wide operating power supply range are equalled by no other technology available today. Best utilization of these characteristics can, however, only be made with an understanding of the technology, circuit configurations and operating characteristics.

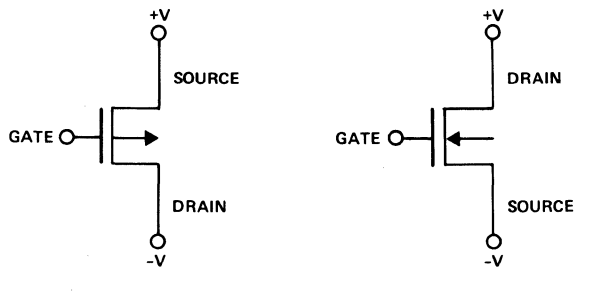
The intention of this introduction is to provide the system designer with sufficient technical background in CMOS to realize its full capabilities.

The Introduction is divided into three sections covering the following topics:

- The MOS transistor
- The CMOS configuration — Logic implementation and circuits
- CMOS design rules

The MOS Transistor

The basic building blocks for all CMOS logic functions are N-channel and P-channel Metal Oxide Semiconductor (MOS) transistors. Referring to Figure 1, these devices function as voltage control switches in that a high or low impedance can be generated between source and drain terminals as a function of the voltage applied between the gate and source. Both elements in the referenced figure are also capable of bilateral current flow between source and drain.

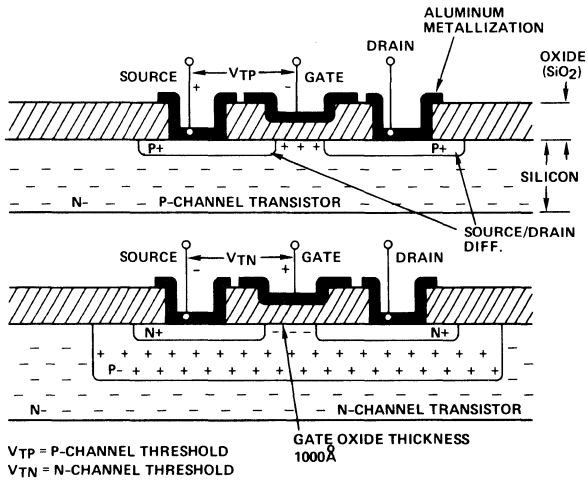


P-CHANNEL MOS TRANSISTOR N-CHANNEL MOS TRANSISTOR

SCHEMATIC REPRESENTATION OF P AND N-CHANNEL TRANSISTORS

Figure 1

An MOS transistor consists of heavily doped source and drain diffusions separated by a narrow gap over which there is a thin gate oxide and aluminum metallization as shown in Figure 2. In order for the transistor to conduct current from source to drain a voltage in excess of its threshold must be applied from gate to source. The threshold is that voltage which must be exceeded in order to invert the silicon between the source and drain to form a conducting channel. An increase in the gate to source bias beyond the threshold voltage further inverts material under the gate electrode increasing transistor conductivity.

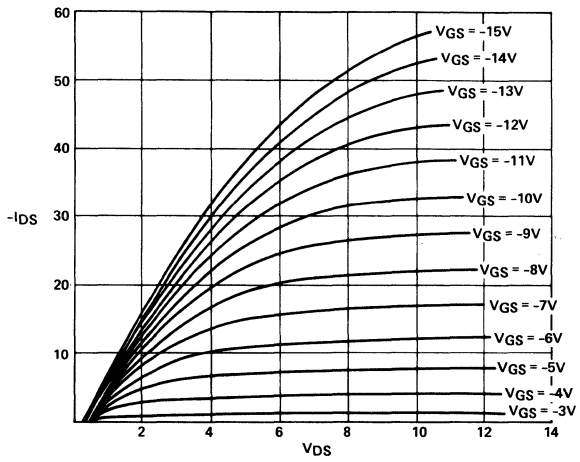


Application of a negative voltage in excess of one V_{TP} from gate to source, or a positive voltage in excess of one V_{TN} from gate to source of a P-channel or N-channel transistor respectively inverts the channel material, inducing a conductive path from source to drain.

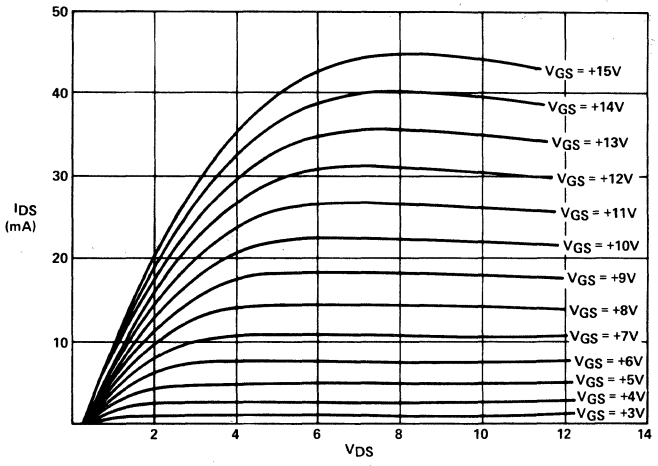
Figure 2

The following equations[1] are a simplified representation of MOS operation, not taking into account some higher order effects. The MOS characteristic is represented by two curve segments, an inverted parabola for nonsaturated operation $(V_{GS}-V_T) \geq V_{DS}$ and a straight line for saturated operation $(V_{GS}-V_T) \leq V_{DS}$.

[1] C.T. SAH "Characteristics of the Metal Oxide Semiconductor Transistors" IEEE Transactions of Electron Devices, July, 1964.



P-CHANNEL



N-CHANNEL

Drain characteristics measured on HD-4007 P-channel and N-channel transistors. Roll off of mobility at high power levels is illustrated by the decrease in I_{DS} with increasing V_{DS} on the N-channel characteristic.

Figure 3

NONSATURATED OPERATION

$(V_{GS} - V_T) \geq V_{DS}$

$$I_{DS} = K' \frac{W}{L} \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2 \right]$$

SATURATED OPERATION

$(V_{GS} - V_T) \leq V_{DS}$

$$I_{DS} = K' \frac{W}{L} (V_{GS} - V_T)^2$$

Where:

V_{GS} = Gate to Source Voltage

V_{DS} = Drain to Source Voltage

V_T = MOS Threshold Voltage

$$K' = \frac{\mu \epsilon}{2T_{ox}}$$

μ = Channel Mobility

ϵ = Dielectric Constant of the Gate Oxide

T_{ox} = Thickness of the Gate Oxide

T_A = Ambient Temperature, ^oK

W = Effective Channel Width

L = Effective Channel Length

Channel Mobility in the above equation is a function decreasing in magnitude with increasing temperature and is primarily responsible for most temperature dependent variations in performance. Figure 3 shows actual drain characteristics measured on an HD-4007. An obvious roll off of current at higher power levels is observed on the N-channel characteristic due to degradation of mobility. The P-channel characteristics exhibit the same effect, however it is less noticeable due to the greater slope of the curves in saturated operation. These curves graphically illustrate degradation of performance at elevated temperatures. Characteristics were recorded on an XY plotter allowing sufficient time for device temperature to rise. The low duty cycle operation of a CRT curve tracer would have eliminated display of this effect.

The CMOS Configuration

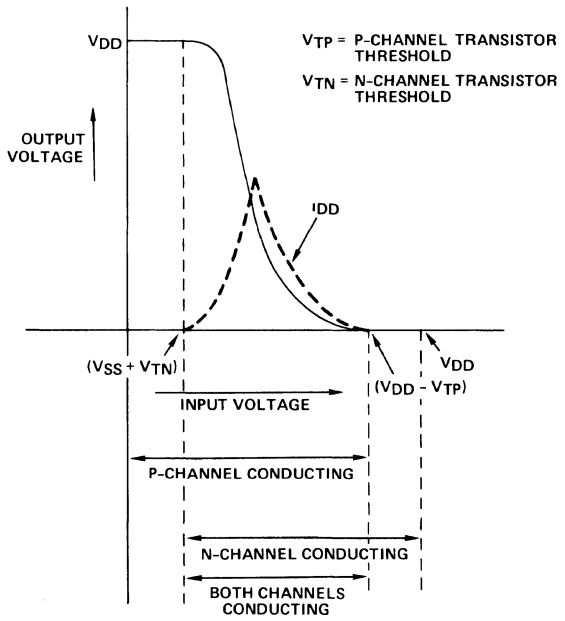
Virtually any logic function can be performed using parallel/series combinations of N and P-channel transistors. In addition Complementary MOS configurations offer many advantages over circuits using P or N-channel transistors exclusively. Speed, power, noise immunity, fanout and power supply regulation considerations all shift in favor of the system designer, the reasons easily derived from a study of the basic inverter circuit. Figure 4 illustrates a CMOS inverter voltage transfer curve with the I_{DD} current superimposed over the transfer curve. Note the following characteristics:

The inverter threshold is centered around the midpoint of the input voltage swing. Proper selection of transistor dimensions results in balanced impedances and an approximately centered gate threshold regardless of the V_{DD} supply voltage. This factor coupled with the V_{DD} to V_{SS} logic voltage swing is responsible for the high voltage noise immunity of CMOS for both logic "one" and "zero" levels.

From the I_{DD} curve note that no DC current flows with the input voltage within one threshold voltage of either V_{DD} or V_{SS}. A series current path exists from V_{DD} to V_{SS} only during transitions of the input voltage through the range for which both channels are conducting.

CMOS transistor thresholds (N and P) of approximately 1.5 volts result in a lower operating limit for V_{DD}-V_{SS} of 3 volts or the sum of the N and P channel thresholds. Under this condition, as the inverter input swings through its voltage range there is no overlap in conduction of the N and P-channels.

The basic operating characteristics which were illustrated above using an inverter also apply to gate and complex logic functions.

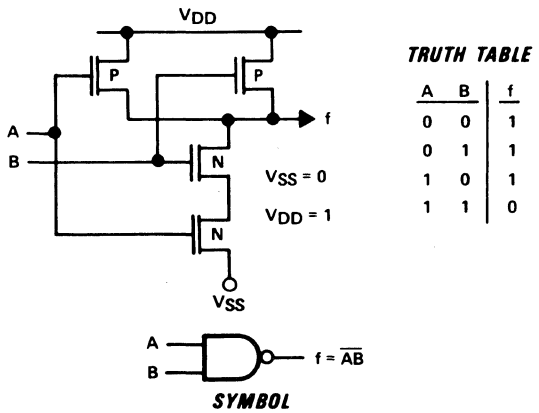


CMOS VOLTAGE TRANSFER CURVE

Figure 4

CMOS Logic

A NAND gate is implemented in CMOS by the series/parallel transistor combination illustrated in Figure 5.



TRUTH TABLE

A	B	f
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NAND GATE – A multiple input NAND gate can be configured with parallel P-channel transistors and series N-channel transistors in the manner shown here. NAND gates with more than two inputs would require one P-channel/N-channel pair per additional input.

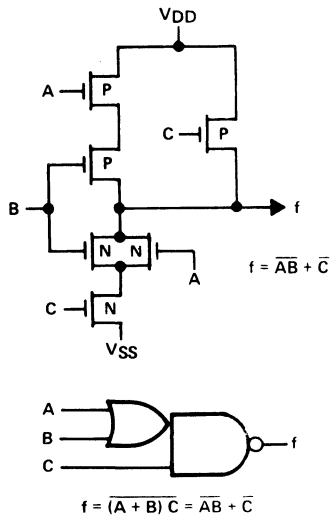
Figure 5

Comparing the truth table and circuit schematic, the only way to switch the output to a zero level (V_{SS}) is to apply two ones (V_{DD}) at the inputs. This closes the series path through the two N-channel devices to V_{SS}. For all other input logic combinations, the series N-channel path is open with one or more of the parallel P-channel devices pulling the output to a one level.

The CMOS NOR gate is analogous to the NAND function, the variation being that the P-channel devices are in series with the N-channels in parallel.

"Functional Logic" is a term referring to the merging of two or more conventional gate functions into a single "complex" gate in order to affect a transistor count or performance advantage. The individual gate identity normally associated with logic is lost when the conventional gate to functional conversion is made.

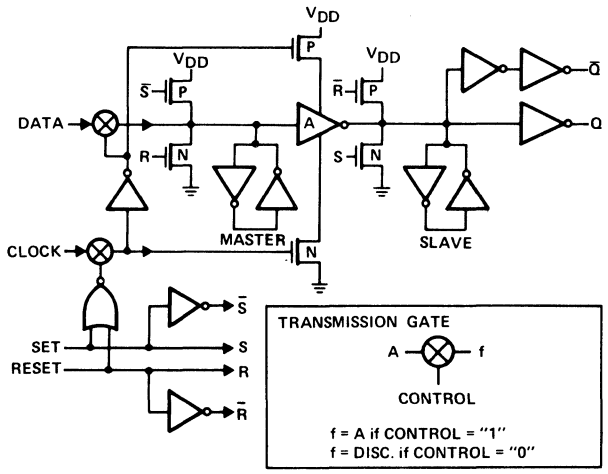
Functional logic is easily implemented with only a fraction of the transistor count required for more straightforward gate techniques. For example, the conversion of the function $f = \overline{AB} + \overline{C}$ to functional logic shown in Figure 6 uses only six transistors, the gate implementation would require ten. Such a reduction in transistor count has a dramatic effect on chip size when applied to a large complex logic function.



CMOS FUNCTIONAL LOGIC – Implementation of the function $f = \overline{AB} + \overline{C}$ utilizing functional logic results in a savings of four transistors. The straightforward gate implementation requires ten transistors, functional logic uses only six.

Figure 6

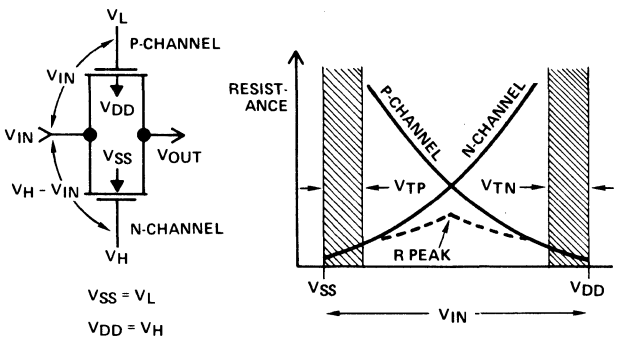
Isolation elements are needed in the implementation of some digital functions, notably master/slave flip-flop configurations. Two techniques are illustrated in Figure 7. Master to slave isolation is provided by decoupling V_{DD} and V_{SS} from inverter element "A" by use of series P and N-channel transistors. Data input to the master flip-flop and clock isolation utilize transmission gates.



Master/Slave "D" type flip-flop — This application shows the use of transmission gates to isolate Data and Clock inputs during the appropriate portions of the operating cycle. With Clock a logic one level Data is isolated from the master. With Set or Reset, a one clock is isolated from the internal circuitry.

Figure 7

The transmission gate is a voltage controlled coupling device. P and N-channel transistors are placed in a parallel configuration as illustrated in Figure 8. Either parallel transistor by itself varies widely in impedance as its source swings through its signal range, varying the gate to source bias. The parallel combination results in a relatively flat characteristic over the entire V_{DD} to V_{SS} input swing.



CMOS TRANSMISSION GATE — The resistance between the input and output of a transmission gate is a function of the input voltage and the gate to substrate voltage. The effective resistance between the input and the output is the parallel combination of the P-channel and N-channel devices indicated by the dashed line.

Figure 8

CMOS Design Rules

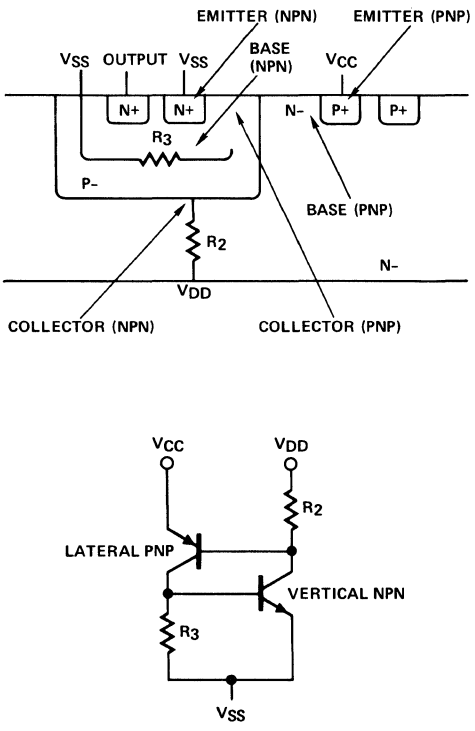
FLOATING INPUTS

CMOS inputs that are not connected are undefined and will drift due to the leakage characteristics of the input structure. Under dynamic system conditions, coupled noise can propagate through floating inputs possibly leading to increased power dissipation and/or apparent circuit malfunction. For these reasons it is recommended that all inputs be connected either to a gate output or voltage supply.

Forward Biasing Inputs or Outputs

Under normal conditions, switching junctions on the CMOS chip operate under reverse bias. There are, however, possible situations under which forward bias could occur. The consequences vary depending on the specific technology and degree of forward bias.

If a CMOS input or output is driven by a low impedance source sufficiently beyond the supply range to heavily forward bias either of the drain to substrate junctions current flow could be sufficient to damage either the chip or wire bonding. Lower levels of drive can also cause damage due to activation of Lateral or Vertical Parasitic bipolar transistors. The most serious such effect is an NPN/PNP parasitic combination which latches up in SCR fashion and shorts V_{DD} to V_{SS} ultimately destroying the chip. The SCR phenomenon is shown in Figure 9. A general rule when using CMOS is to avoid a forward bias condition sufficient to supply drive to parasitics by keeping all pins within the range V_{SS} 0.3 $\leq V_{Pin} \leq V_{DD}$ + 0.3. When a forward bias condition is unavoidable a resistor can be used to limit current to a level not sufficient to activate parasitic transistors.



The SCR configuration shown above when properly biased can latch up conducting sufficient current to damage a CMOS device. The latch mode can be triggered by forward biasing either an NPN or PNP base emitter junction in the above configuration, both of which normally operate under reverse bias.

Figure 9

Derating Switching Parameters

Switching Characteristics as well as DC drive capabilities exhibit a negative temperature coefficient of 0.3%/°C due to degradation of the channel mobility with increasing temperature. Switching parameters are normally specified at 25°C and must be derated by the user according to his specific operating requirements.

Static Discharge

CMOS as well as other MOS technologies derive much of their advantage from the high gate input impedance, on the order of $10^{12}\Omega$. The high input impedance, however, is also responsible for what is its most serious handling problem, damage due to application of static charge across device terminals. Application of such charge to a CMOS input usually results in a Gate to Drain or Gate to Source short, a catastrophic failure. This phenomenon is more common in low humidity climates, but can be serious in any assembly area employing commonly used environmental control methods.

The failure mode is the rupture of the thin gate oxide due to the high voltage built up on application of a static charge.

In all assembly environments some simple procedures can be followed in order to minimize device losses.

1. Use conductive work stations. Metallic or conductive plastic tops on work benches connected to ground help eliminate static buildup.

2. Ground all handling equipment if possible.

3. Ground all handling personnel through a conductive bracelet through $1M\Omega$ to ground. The $1M\Omega$ resistor is to prevent operator injury.

4. Smocks, clothing, and especially shoes of certain insulating materials should not be worn in areas where devices are handled. These materials are highly dielectric in nature and will hold, or aid in the generation of a static charge.

5. Control relative humidity to as high a level as is practical. A higher level of humidity helps to bleed away static charge as it collects.

6. Ionized air blowers can be used to reduce charge buildup in areas where grounding is not possible or desirable.

7. Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil. Printed circuit boards should have shorting bars on the connectors.

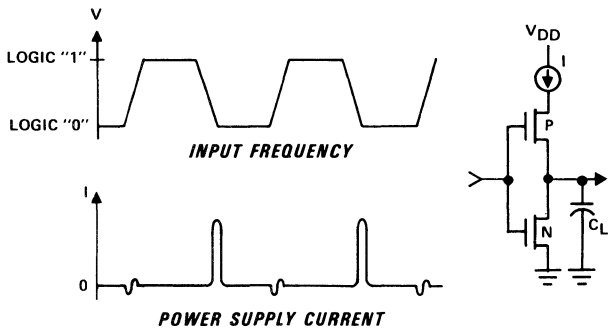
8. In automated handling equipment belts, chutes, or other surfaces the leads contact should be of a conducting nature. If this is not possible, ionized air blowers may help reduce static charge problems.

9. Voltages of magnitude high enough to cause damage may be generated in high speed test equipment due to the effects of inductance or improper termination of driven lines. Steps should be taken to eliminate the possible application of such voltages to device pins or pads. This problem is not one of static discharge, but the result is so similar, they may be confused. Harris application note 208 is available further covering the subject of CMOS input protection techniques and handling procedures.

Minimizing Power

DC power consumption is a function of leakage currents. Over the specified supply range the Total I_{DD} leakage is typically in the pico-ampere to nano-ampere range. For circuits operating at moderate to high speeds this component can normally be ignored in the determination of total power.

Most CMOS power at high operating frequencies is consumed in driving capacitance. Figure 10 shows the power supply current waveform for an inverter or gate circuit under a transient condition. The large positive current coinciding with the negative going input transition is pulled from V_{DD} through P-channel device to charge C_L.



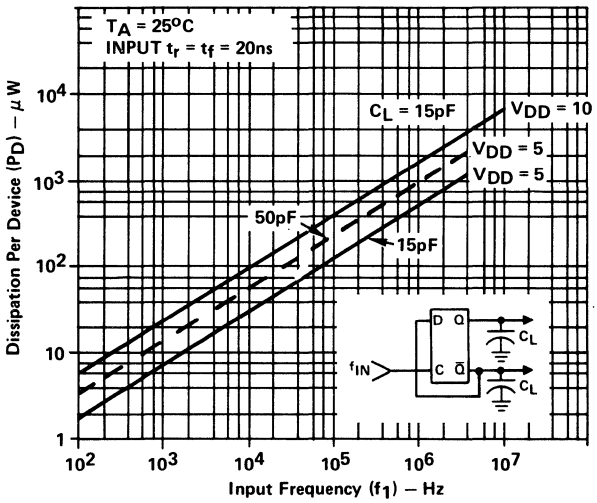
Power Supply Current — The majority of power supply current flows through the P-channel transistor to charge C_L during the negative going input transition. The current variation during the positive going input transition has two components.

1. Momentary capacitive coupling through the overlap capacitance of a voltage greater than V_{DD} contributes a negative component.

2. Serial current flows through both P and N-channels during the input transition while both transistors are thresholded.

Figure 10

Capacitive power for a given CMOS function can be determined from the equation $P = f \times C_L \times V_{DD}^2$ where f is the operating frequency, at which the output is switching.



To illustrate the $P = fC_L V_{DD}^2$ relationship, the average power dissipation versus clock frequency for ½ of an HD-4013 set up for the toggle mode is shown above. Both Q and $\overline{Q}$ are loaded with C_L.

Figure 11

This formula can be derived as follows:

The energy stored in the load capacitance when charged to V_{DD} is :

$$E = \tfrac{1}{2} C_L V_{DD}^2$$

For a gate this energy must be delivered to the load capacitance through the P-channel device as the output switches to V_{DD} and removed as it switches to V_{SS}. Thus, the total energy required to charge and discharge the load capacitance during one cycle is:

$$E_{Total} = C_L V_{DD}^2$$

Power = Energy per unit time where time is the period of the operating frequency.

$$T = \frac{1}{f} \qquad \text{Where } T = \text{Period}, \; f = \text{Frequency of Operation}$$

$$\text{Power} = \frac{E_{Total}}{T} = \frac{E_{Total}}{\frac{1}{f}} = f C_L V_{DD}^2$$

As mentioned earlier some current does flow serially through the complementary devices during that portion of the input transition when both P and N-channel devices are on. This condition becomes more prominent with higher values of V_{DD}-V_{SS} due to increased conductivity as well as increased input voltage range for which complementary devices are simultaneously conducting. Longer transition times at a gate input will extend the period during which this series path from V_{DD} to V_{SS} is conducting and increase total power consumption.

With bipolar or single channel MOS technologies switching (capacitive load) power is often insignificant due to high quiescent power levels. CMOS reverses this with switching related power dominating the total system power. Significant savings in power can therefore, be gained by careful attention to such factors as input rise and fall time and load capacitance.

Interfacing

CMOS/TTL

The CMOS interface with other technologies can in many cases be accomplished with no buffering. The HD-54C/74C product line, for example, has adequate output capabilities to drive two low power TTL loads. For devices not capable of driving TTL directly CMOS buffers are available to perform the CMOS to TTL interface.

The TTL output "one" level (V_{OH}) of 2.4 volts is not sufficiently high to guarantee recognition as a logic "one" at a CMOS input. A pull up resistor from the TTL output to V_{DD} provides an adequate interface for many applications by pulling the driven CMOS input nearly to V_{DD} restoring an adequate noise margin.

CMOS/PMOS

The primary requirement on PMOS to CMOS or CMOS to PMOS interfaces is signal voltage compatibility, which can normally be met by using common supplies. The wide V_{DD}-V_{SS} operating range of CMOS provides the required voltage supply/signal compatibility.

CMOS/THREE STATE

A wide selection of devices are available as part of the HD-54C/74C series providing three state capabilities useful for a common bus interface. Output drive transistors to both logic "one" and "zero" levels are turned off when the "disable" input is held high yielding the "third" high impedance output state. Selective disabling of three state outputs allows two or more three state buffers to time share a single bus.

HD-54/74C Series

3

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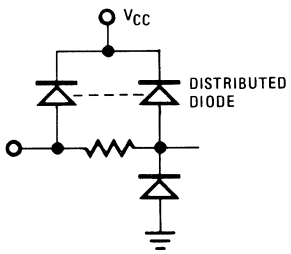
HD-54C/74C Series

These circuits employ complementary MOS (CMOS) to achieve low power dissipation, high noise immunity and wide power supply voltage ranges with symmetric rise and fall times. Features such as these make the 54/74C logic family ideal for use in digital systems and a must for "worse case" noise immunity design. Function and pin out compatibility with series 54/74 TTL devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

Family Features

■ Wide Supply Voltage Range	3.0V to 15V
■ Guaranteed Noise Margin	1.0V
■ High Noise Immunity	0.45 V_{CC} Typ.
■ Low Power	10nW Typ. for Gates 10 µW Typ. for MSI Circuits
■ Low Power TTL Compatibility	Fan Out of 2 Driving 74L
■ All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND unless otherwise noted.	

HD-54C00/HD-74C00 *Quad Two-Input NAND Gate*
HD-54C02/HD-74C02 *Quad Two-Input NOR Gate*
HD-54C04/HD-74C04 *Hex Inverter*
HD-54C10/HD-74C10 *Triple Three-Input NAND Gate*
HD-54C20/HD-74C20 *Dual Four-Input NAND Gate*

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V to 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45V_{CC} TYP.
- LOW POWER CONSUMPTION — 10nW/PACKAGE TYP.
- LOW POWER TTL COMPATIBILITY — FAN OUT OF 2 DRIVING 74L

Description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static dischrage by diode clamps to V_{CC} and GND.

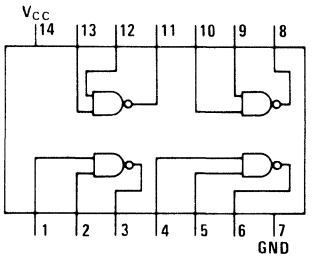
Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

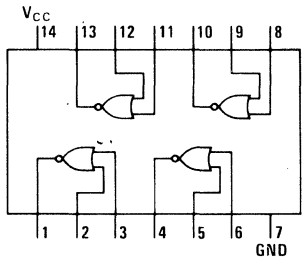
See package outline Code 1U and Code 9V.

Connection Diagrams (Top View)

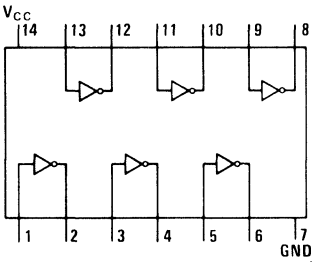
HD-54C00/HD-74C00



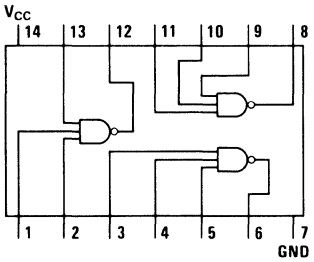
HD-54C02/HD-74C02



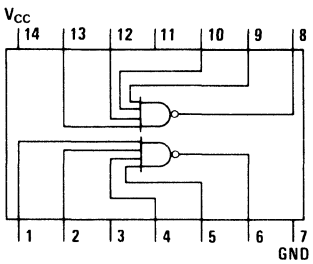
HD-54C04/HD-74C04



HD-54C10/HD-74C10



HD-54C20/HD-74C20



Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin	-0.3V to V_{CC} + 0.3V	Storage Temperature Range	-65°C to +150°C
Operating Temperature Range		Maximum V_{CC} Voltage	16V
54C	-55°C to +125°C	Package Dissipation	500mW
74C	-40°C to +85°C	Lead Temperature (Soldering, 10 Seconds)	300°C

ELECTRICAL CHARACTERISTICS

Min/Max limits apply across the guaranteed temperature range unless otherwise noted.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5			V	V_{CC} = 5.0V
			8.0			V	V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5	V	V_{CC} = 5.0V
					2.0	V	V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5			V	V_{CC} = 5.0V, I_O = -10μA
			9.0			V	V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5	V	V_{CC} = 5.0V, I_O = -10μA
					1.0	V	V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Supply Current	I_{CC}		0.01	15	μA	V_{CC} = 15V
	LOW POWER TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} -1.5			V	54C, V_{CC} = 4.5V
			V_{CC} -1.5			V	74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V
					0.8	V	74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.4			V	54C, V_{CC} = 4.5V, I_O = -10μA
			4.4			V	74C, V_{CC} = 4.75V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = +10μA
					0.4	V	74C, V_{CC} = 4.75V, I_O = +10μA
	CMOS TO LOW POWER						
	Logical "1" Input Voltage	$V_{IN(1)}$	4.0			V	54C, V_{CC} = 4.5V
			4.0			V	74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.0	V	54C, V_{CC} = 4.5V
					1.0	V	74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = -360μA
			2.4			V	74C, V_{CC} = 4.75V, I_O = -360μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = 360μA
					0.4	V	74C, V_{CC} = 4.75V, I_O = 360μA
	OUTPUT DRIVE						
	Output Source Current	I_{Source}	1.75			mA	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{Out} = 0V
	Output Source Current	I_{Source}	8.0			mA	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{Out} = 0V
	Output Sink Current	I_{Sink}	1.75			mA	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{Out} = V_{CC}
	Output Sink Current	I_{Sink}	8.0			mA	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{Out} = V_{CC}

Specifications

ELECTRICAL CHARACTERISTICS

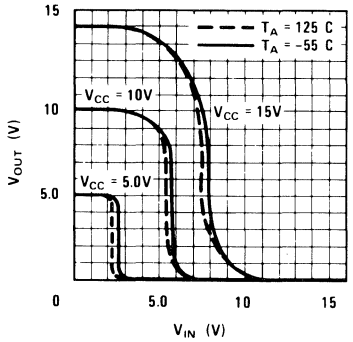
$T_A = 25^0C$, $C_L = 50pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
A.C.	HD-54C00/HD 74C00 HD-54C02/HD-74C02 HD-54C04/HD-74C04						
	Propagation Delay Time to Logical "1" or "0"	t_{pd}		50 30	90 60	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Input Capacitance	C_{IN}		12		pF	(Note 2)
	Power Dissipation Capacitance	C_{PD}		12		pF	(Note 3) Per gate or inverter
	HD-54C10/HD-74C10						
	Propagation Delay Time to Logical "1" or "0"	t_{pd}		60 35	100 70	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Input Capacitance	C_{IN}		7.0		pF	(Note 2)
	Power Dissipation Capacitance	C_{PD}		18		pF	(Note 3) Per gate
	HD-54C20/HD-74C20						
	Propagation Delay Time to Logical "1" or "0"	t_{pd}		70 40	115 80	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Input Capacitance	C_{IN}		13		pF	(Note 2)
	Power Dissipation Capacitance	C_{PD}		30		pF	(Note 3) Per gate

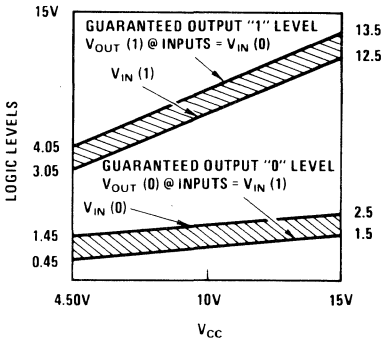
NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. C_{PD} determines the no load ac power consumption of any CMOS device.

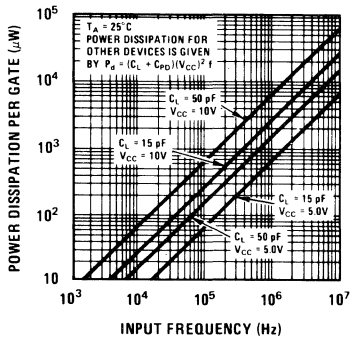
Typical Performance Characteristics

Gate Transfer Characteristics

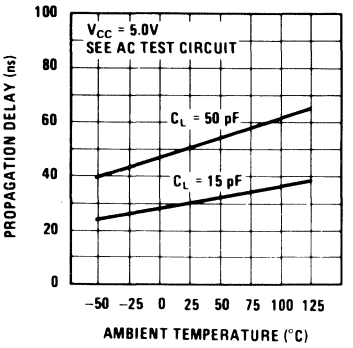


Guaranteed Noise Margin Over Temperature vs V_{CC}

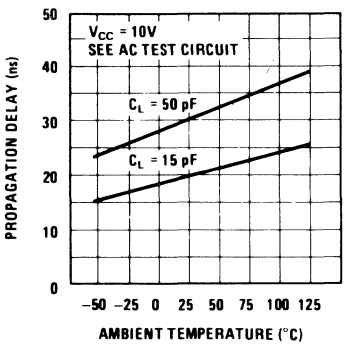




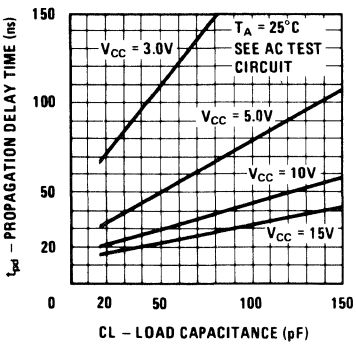
Propagation Delay vs Ambient Temperature
HD-54C00/HD-74C00
HD-54C02/HD-74C02
HD-54C04/HD-74C04



Propagation Delay vs Ambient Temperature
HD-54C00/HD-74C00
HD-54C02/HD-74C02
HD-54C04/HD-74C04

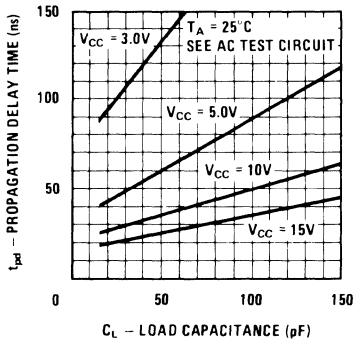


Propgation Delay Time vs Load Capacitance
HD-54C00/HD-74C00
HD-54C02/HD-74C02
HD-54C04/HD-74C04

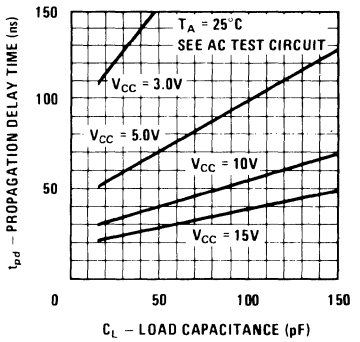


Typical Performance Characteristics (continued)

Propagation Delay Time vs
Load Capacitance
HD-54C10/HD-74C10

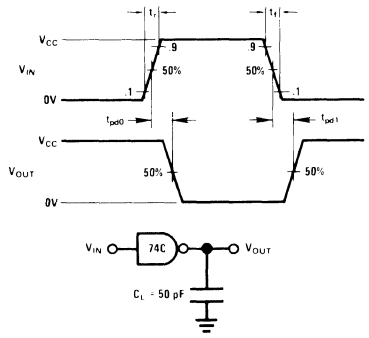


Propagation Delay Time vs
Load Capacitance
HD-54C20/HD-74C20



Waveforms and AC Test Circuits

CMOS to CMOS



NOTE DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

HD-54C08/HD-74C08

Quad 2-Input AND Gate

HD-54C86/HD-74C86

Quad 2-Input EXCLUSIVE-OR Gate

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER TTL COMPATIBILITY — FAN OUT OF 2 DRIVING 74L
- LOW POWER CONSUMPTION — 10nW/PACKAGE TYP.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Truth Tables

HD-54C08/HD-74C08

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

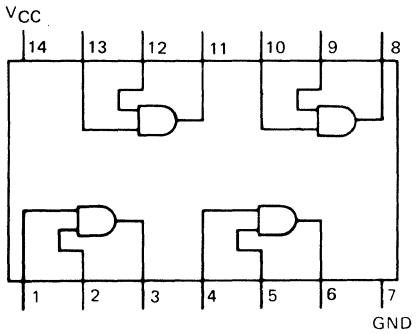
HD-54C86/HD-74C86

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

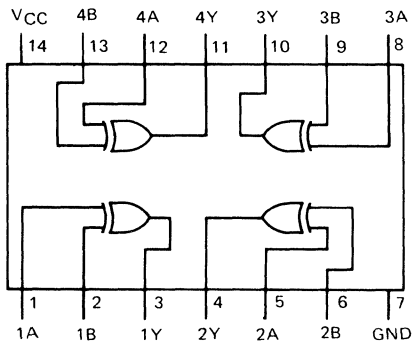
H = High Level L= Low Level

Connection Diagrams

HD-54C08/HD-74C08



HD-54C86/HD-74C86



Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin		-0.3V to V_{CC} +0.3V	Package Dissipation	500mW
Operating Temperature Range	HD-54C08, HD-54C86	-55°C to +125°C	Operating V_{CC} Range	3.0V to 15.0V
	HD-74C08, HD-74C86	-40°C to +85°C	Absolute Maximum V_{CC}	16.0V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

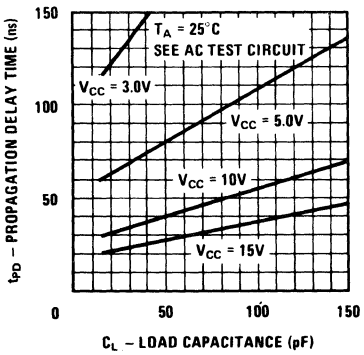
Min/Max limits apply across temperature range, unless otherwise noted.
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Supply Current	I_{CC}		0.01	15	μA	V_{CC} = 15V
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} —1.5			V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4 0.4	V V	54C, V_{CC} = 4.5V, I_O = +360μA 74C, V_{CC} = 4.75V, I_O = 360μA
	OUTPUT DRIVE						
	Output Source Current (P-Channel)	I_{Source}	-1.75	-3.3		mA	V_{CC} = 5.0V, V_{Out} = 0V T_A = 25°C
	Output Source Current (P-Channel)	I_{Source}	-8.0	-15		mA	V_{CC} = 10V, V_{Out} = 0V T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	1.75	3.6		mA	V_{CC} = 5.0V, V_{Out} = V_{CC} T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	8.0	16		mA	V_{CC} = 10V, V_{Out} = V_{CC} T_A = 25°C
A.C.	**HD-54C08/HD-74C08**						
	Propagation Delay Time to Logical "1" or "0"	t_{pd}		80 40	140 70	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Input Capacitance	C_{IN}		5.0		pF	Note 2
	Power Dissipation Capacitance	C_{pd}		14		pF	Note 3
	HD-54C86/HD-74C86						
	Propagation Delay Time to Logical "1" or "0"	t_{pd}		110 50	185 90	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Input Capacitance	C_{IN}		5.0		pF	Note 2
	Power Dissipation Capacitance	C_{pd}		20		pF	Note 3

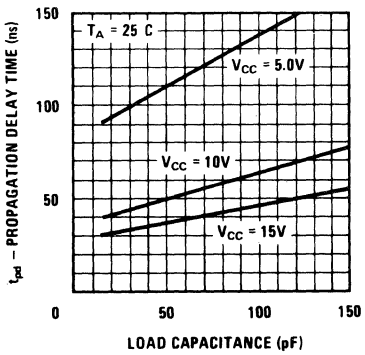
NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodeic testing.
3. C_{PD} determines the no load AC power consumption of any CMOS device.

Typical Performance Characteristics

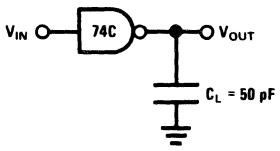
Propagation Delay Time
vs Load Capacitance
HD-54C08/HD-74C08



Propagation Delay Time
vs Load Capacitance
HD-54C86/HD-74C86

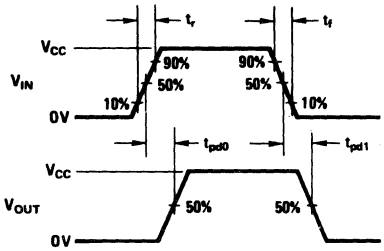


AC Test Circuit



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

Waveforms



HARRIS SEMICONDUCTOR
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Advanced Information

HD-54C14/HD-74C14

Hex Schmitt Trigger

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- LOW POWER T^2L COMPATIBLE — DRIVE 2 LT^2L LOADS

Package

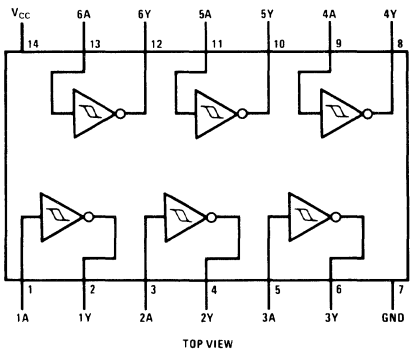
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

The HD-54C14/HD-74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors.

Connection Diagrams



TOP VIEW

HD-54C14/HD-74C14 HEX SCHMITT TRIGGER

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C30/HD-74C30

8-Input NAND Gate

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15V
- GURANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER — FAN OUT OF 2
- TTL COMPATIBILITY — DRIVING 74L

Package

See CMOS Packaging Section 5 for complete Package information. This device is available in Ceramic Dual In-Line and Flat Packs.

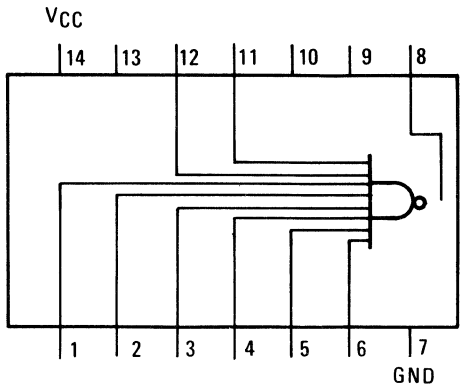
See package outline Code 1U and Code 9V.

Description

The logic gate employs complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption and high noise immunity. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers familiar with the standard 54/74 logic family.

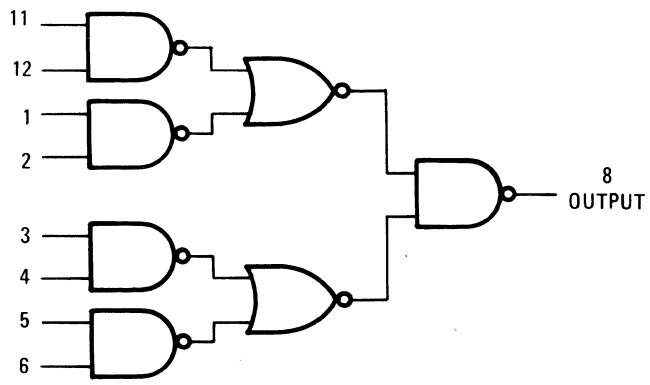
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Connection Diagrams



TOP VIEW

Logic Diagrams



ABSOLUTE MAXIMUM RATING

Voltage at any Pin		-0.3V to V_{CC} +0.3C	Package Dissipation	500mW
Operating Temperature Range	HD-54C30	-55°C to +125°C	Operating V_{CC} Range	4.5V to 15V
	HD-74C30	-40°C to +85°C	Absolute Maximum V_{CC}	16V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTISTICS Min/Max limits apply across temperature range, unless otherwise noted.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Supply Current	I_{CC}		0.01	15	μA	V_{CC} = 15V
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC}- 1.5			V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4 0.4	V V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
	OUTPUT DRIVE						
	Output Source Current (P-Channel)	I_{Source}	-1.75	-3.3		mA	V_{CC} = 5.0V, V_{Out} = 0V T_A = 25°C
	Output Source Current (P-Channel)	I_{Source}	-8.0	-15		mA	V_{CC} = 10V, V_{Out} = 0V T_A = 25°C
	Output Sink Current (N-CHannel)	I_{Sink}	1.75	3.6		mA	V_{CC} = 5.0V, V_{Out} = V_{CC} T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	8.0	16		mA	V_{CC} = 10V, V_{Out} = V_{CC} T_A = 25°C

Specifications

ELECTRICAL CHARACTISTICS

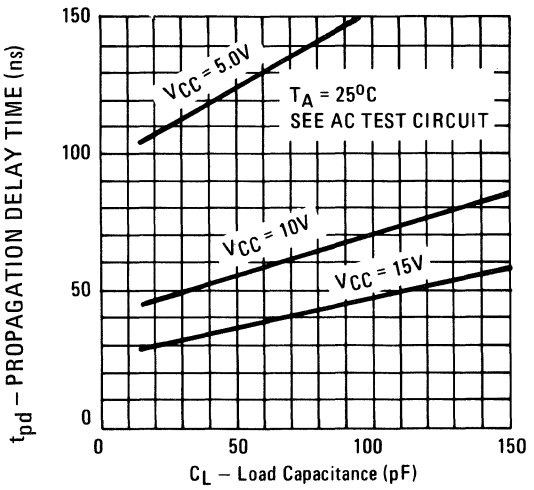
$T_A = 25^0C$, $C_L = 50pF$, Unless Otherwise Specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Propagation Delay Time to Logical "1" or "0"	t_{pd}		125	180	ns	V_{CC} = 5.0V
				55	90	ns	V_{CC} = 10V
A.C.	Input Capacitance	C_{IN}		4.0		pF	(Note 2)
	Power Dissipation Capacitance	C_{pd}		26		pF	(Note 3) Per Gate

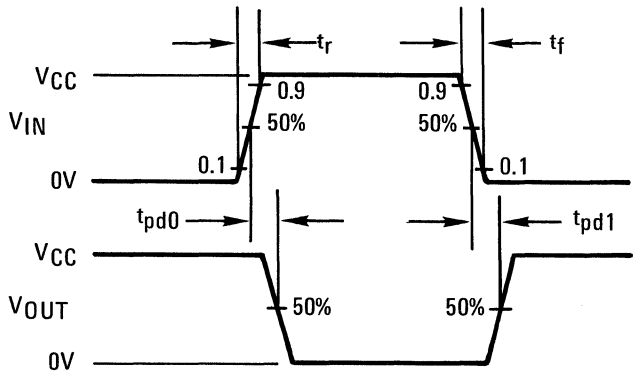
NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual operation.
2. Capacitance is guaranteed by periodic testing.
3. C_{PD} determines the no load AC power consumption of any CMOS device.

Typical Characteristics

PROPAGATION DELAY TIME vs. LOAD CAPACITANCE

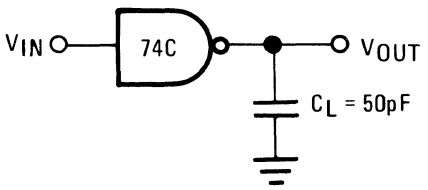


Switching Time Waveforms



NOTE: Delays measured with Input t_f, t_r = 20ns.

AC Test Circuit



HD-54C32/HD-74C32

Quad 2-Input OR Gate

Description

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER — 10nW TYP.
- LOW POWER T^2L COMPATIBLE — DRIVE 2 LT^2L LOADS

Package

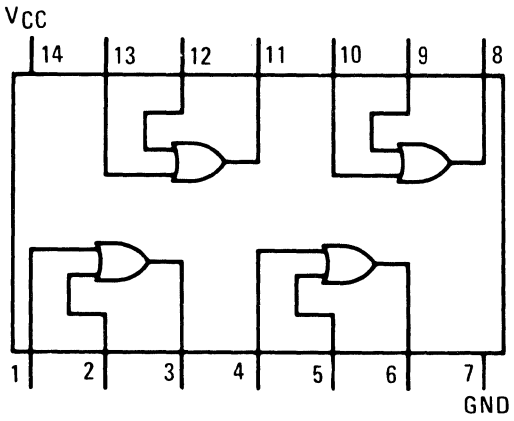
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Features

Employing complementary MOS (CMOS) transistor to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

Connection Diagrams



HD-54C30/HD-74C30
HD-54C32/HD-74C32

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C42/HD-74C42

BCD to Decimal Decoder

Features

- SUPPLY VOLTAGE RANGE — 3V TO 15V
- LOW POWER TTL COMPATIBLE — DRIVE 2 LPTTL LOADS
- HIGH NOISE IMMUNITY — 0.45V V_{CC} (TYP.)
- LOW POWER — 50nW (TYP.)
- MEDIUM SPEED OPERATION — 10MHz (TYP.) WITH 10V V_{CC}

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

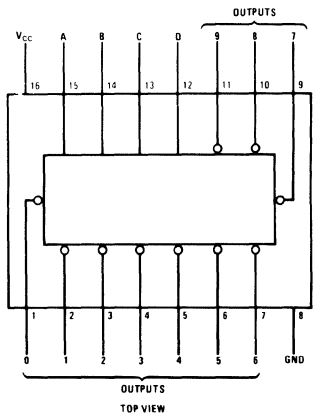
See package outline Code 1W and Code 9L.

Description

The HD-54C42/HD-74C42 one-of-ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. This decoder produces a logical "0" at the output corresponding to a four bit binary input from zero to nine and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1".

Functional Diagram

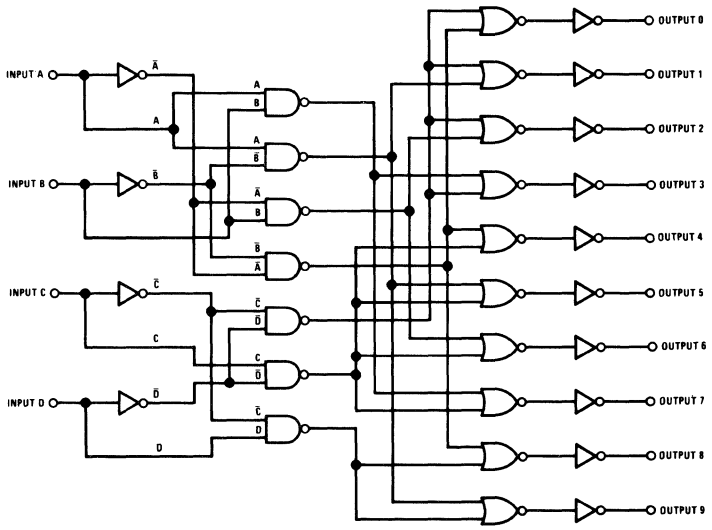
Dual-In-Line Package

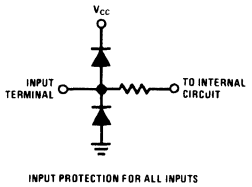


Truth Table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Schematic Diagram





INPUT PROTECTION FOR ALL INPUTS

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} +0.3V	Storage Temperature	-65°C to +150°C
Operating Temperature	HD-54C42	-55°C to +125°C	Package Dissipation	500mW
	HD-74C42	-40°C to +85°C	Operating V_{CC} Range	3.0V to 15.0V
Maximum V_{CC} Voltage		16.0V	Lead Temperature (Soldering, 10 Seconds)	300°C

ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range unless otherwise specified.
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8			V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2	V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10.0V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10.0V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$			1	μA	V_{CC} = 15.0V, V_{IN} = 15V
Logical "0" Input Current	$I_{IN(0)}$	-1			μA	V_{CC} = 15.0V, V_{IN} = 0V
Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15.0V
Input Capacitance	C_{IN}		5		pF	Any Input
Propagation Delay Time to a Logical "0" or Logical "1"			200 90	300 140	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
CMOS TO LOW POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} -1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O =-360μA 74C, V_{CC} = 4.75V, I_O = -360μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
Propagation Delay Time to a Logical "0" or Logical "1"			250	400	ns	V_{CC} = 5.0V

NOTE: 1. This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

HARRIS SEMICONDUCTOR
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HD-54C48/HD-74C48

BCD to 7 Segment Decoder

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.

Package

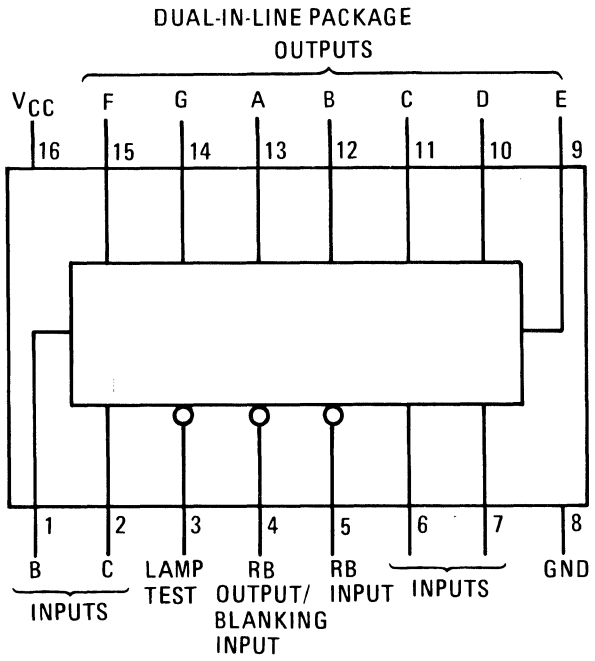
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Description

The HD-54C48/HD-74C48 BCD to 7 segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test blanking input/ripple-blanking output, and ripple-blanking inputs.

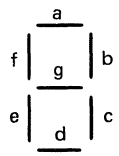
Connection Diagram



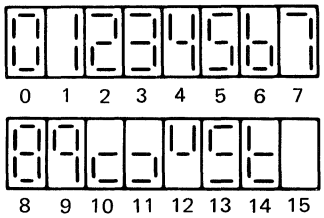
TOP VIEW

MM54C48/MM74C48
BCD TO SEVEN SEGMENT DECODER

Segment Identification



NUMERICAL DESIGNATIONS
AND RESULTANT DISPLAYS



ABSOLUTE MAXIMUM RATING

Voltage at any pin		-0.3V to V_{CC} +0.3V	Package Dissipation	500mW
Operating Temperature Range	HD-54C48	-55°C to +125°C	Operating V_{CC} Range	3.0V to 15V
	HD-74C48	-40°C to +85°C	Absolute Maximum V_{CC}	16V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTISTICS

Min/Max Limits apply across temperature range, unless otherwise specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5			V	V_{CC} = 5.0V
			8.0			V	V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5	V	V_{CC} = 5.0V
					2.0	V	V_{CC} = 10V
	Logical "1" Output Voltage (RB Output Only)	$V_{Out(1)}$	4.5			V	V_{CC} = 5.0V, I_O = -10μA
			9.0			V	V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5	V	V_{CC} = 5.0V, I_O = +10μA
					1.0	V	V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15V
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC}-1.5			V	54C, V_{CC} = 4.5V
						V	74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V
					0.8	V	74C, V_{CC} = 4.75V
	Logical "1" Output Voltage (RB Output Only)	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = -50μA
			2.4			V	74C, V_{CC} = 4.75V, I_O = -50μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = 360μA
					0.4	V	74C, V_{CC} = 4.75V, I_O = 360μA
	OUTPUT DRIVE						
	Output Source Current (P-Channel) (RB Output Only)	I_{Source}			-0.80	mA	V_{CC} = 4.75V, V_{Out} = 0.4V
	Output Sink Current (N-Channel)	I_{Sink}	1.75	3.6		mA	V_{CC} = 5.0V, V_{Out} = V_{CC}, T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	8.0	16		mA	V_{CC} = 10V, V_{Out} = V_{CC}, T_A = 25°C
	Output Source Current (NPN Bipolar)		20	50		mA	V_{CC} = 5.0V, V_{Out} = 3.4
				65		mA	V_{CC} = 5.0V, V_{Out} = 3.0
			20	50		mA	V_{CC} = 10V, V_{Out} = 8.4
				65		mA	V_{CC} = 10V, V_{Out} = 8.0

NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. C_{PD} determines the no load AC power consumption of any CMOS device.

ELECTRICAL CHARACTISTICS

$T_A = 25^oC$, $C_L = 50pF$, Unless Otherwise Specified.

	PARAMETER	MIN.	TYP.	MAX,	UNITS	CONDITIONS
A.C.	Propagation Delay to a "1" or "0" on Segment Outputs from Data Inputs	450 160	1500 500		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay to a "0" on Segment Outputs from RB Input	500 180	1600 550		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay to a "0" on Segment Outputs from Blanking Input	350 140	1200 450		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay to a "1" on Segment Outputs from Lamp Test	450 160	1500 500		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay to a "1" on RB Output from RB Input	600 250	2000 800		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay to a "0" on RB Output from RB Input	140 50	450 150		ns ns	V_{CC} = 5.0V V_{CC} = 10V

HD-54C73/HD-74C73 *Dual J-K Flip-Flops with Clear*
HD-54C76/HD-74C76 *Dual J-K Flip-Flops with Clear and Preset*
HD-54C107/HD-74C107 *Dual J-K Flip-Flops with Clear*

Features

- SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- LOW POWER TTL COMPATIBLE — DRIVE 2 LPTTL LOADS
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER — 50nW TYP.
- MEDIUM SPEED OPERATION — 10MHz TYP. WITH 10V SUPPLY

Description

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The HD-54C76/HD-74C76 flip-flops also include preset inputs and are supplied in 16 pin packages. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

Truth Table

t_n		$t_n + 1$
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = Bit time before clock pulse.

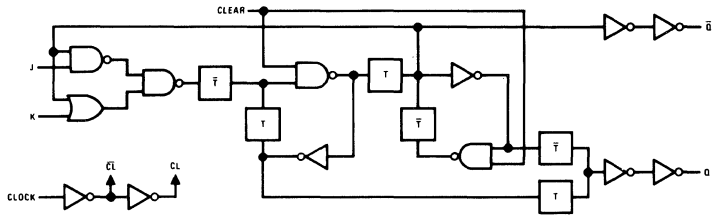
$t_n + 1$ = bit time after clock pulse.

Package

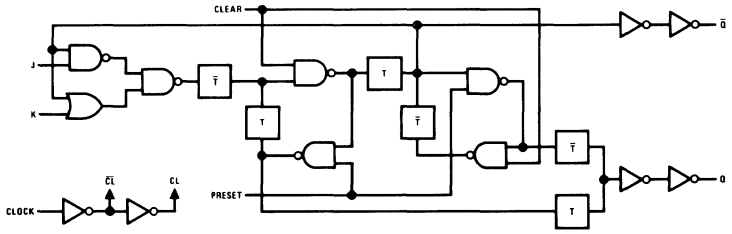
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package Code 1U and 9V.

Logic Diagrams

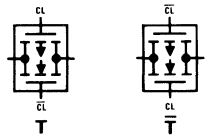


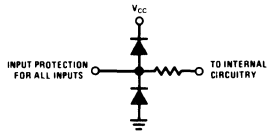
HD-54C73/HD-74C73 and HD-54C107/HD-74C107



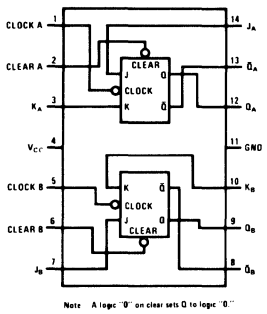
HD-54C76/HD-74C76

Transmission Gate

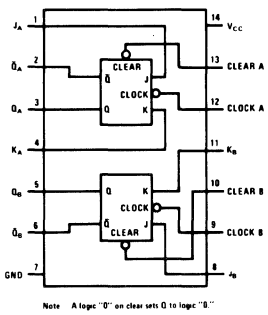




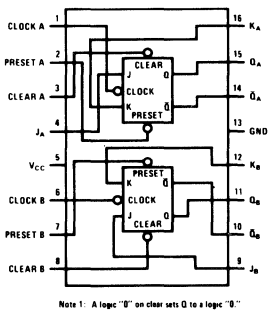
Connection Diagrams



HD-54C73/HD-74C73



HD-54C107/HD-74C107



HD-54C76/HD-74C76

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} + 0.3V	Maximum V_{CC} Voltage	16.0V
Operating Temperature	HD-54CXX	-55°C to +125°C	Package Dissipation	500mW
	HD-74CXX	-40°C to +85°C	Lead Temperature (Soldering, 10 Sec.)	300°C
Storage Temperature		-65°C to +150°C	Operating V_{CC} Range	+3.0V to 15.0V

ELECTRICAL CHARACTERISTICS

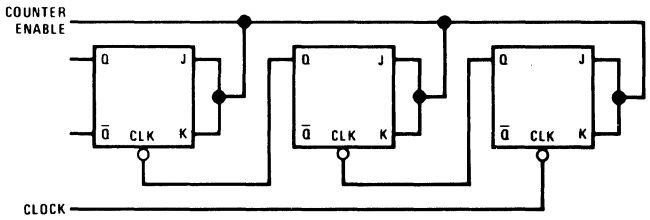
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8			V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5. 0V, I_O = -10μA V_{CC} = 5. 0V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10.0V , I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$			1.0	μA	V_{CC} = 15.0V
Logical "0" Input Current	$I_{IN(0)}$	-1.0			μA	V_{CC} = 15.0V
Supply Current	I_{CC}		0.050	60	μA	V_{CC} = 15.0V
Input Capacitance	C_{IN}		5		pF	Any input
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" tpd1 from Clock to Q or $\overline{Q}$			180 70	300 110	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Propagation Delay Time to a Logical "0" from Preset or Clear			200 80	300 130	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Propagation Delay Time to a Logical "1" from Preset or Clear			200 80	300 130	ns ns	V_{CC} = 5.0V V_{CC} = 10V
Time Prior to Clock Pulse that Data must be Present	t_{setup}		110 45	175 70	ns ns	V_{CC} = 5.0V V_{CC} = 10V
Time after Clock Pulse that J and K must be Held			-40 -20	0 0	ns ns	V_{CC} = 5.0V V_{CC} = 10V
Minimum Clock Pulse Width	$t_{WL} = t_{WH}$		120 50	190 80	ns ns	V_{CC} = 5.0V V_{CC} = 10V
Minimum Preset and Clear Pulse Width			90 40	130 60	ns ns	V_{CC} = 5.0V V_{CC} = 10V
Maximum Toggle Frequency		2.5 7.0	4.0 11.0		MHz MHz	V_{CC} = 5.0V V_{CC} = 10V
Clock Pulse Rise and Fall Time				15 5	μs μs	V_{CC} = 5.0V V_{CC} = 10V
LOW POWER TTL TO CMOS INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} —1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" from Clock			250		ns	V_{CC} = 5.0V

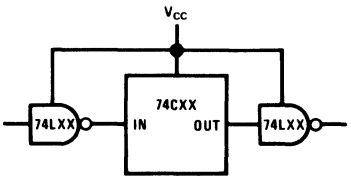
NOTE: 1. This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

Typical Applications

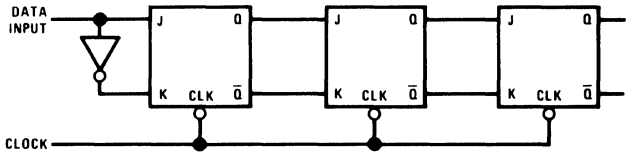
Ripple Binary Counters



74C Compatibility

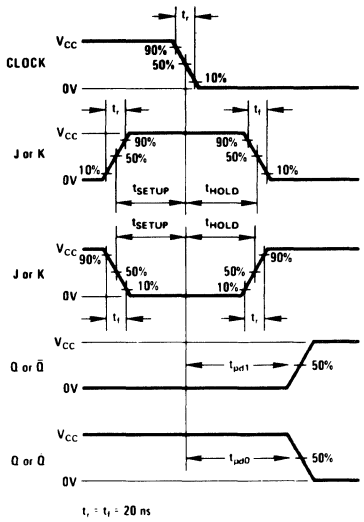


Shift Registers

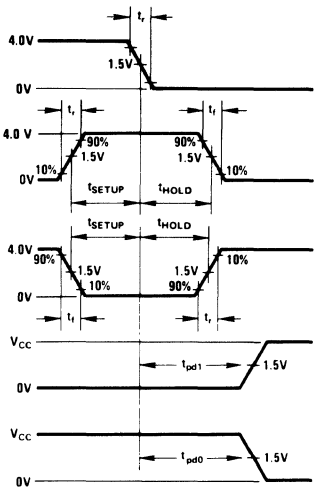


Waveforms

CMOS to CMOS

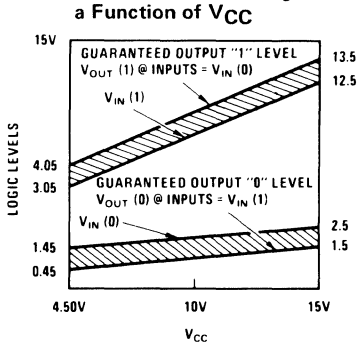


TTL to CMOS

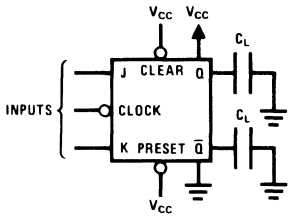


Noise Margin

Guaranteed Noise Margin as a Function of V_{CC}



AC Test Circuit



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C74/HD-74C74

Dual D Flip-Flop

Features

- SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- LOW POWER TTL COMPATIBLE — DRIVE 2LPT^{2}L LOADS
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER — 50nW TYP.
- MEDIUM SPEED OPERATION — 10MHz TYP. WITH 10.0V SUPPLY

Package

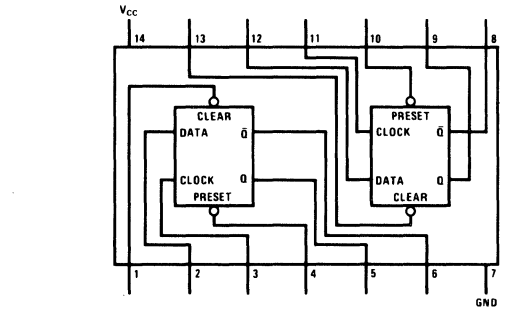
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package Code 1U and Code 9V.

Description

The HD-54C74/HD-74C74 dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. Each flip-flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

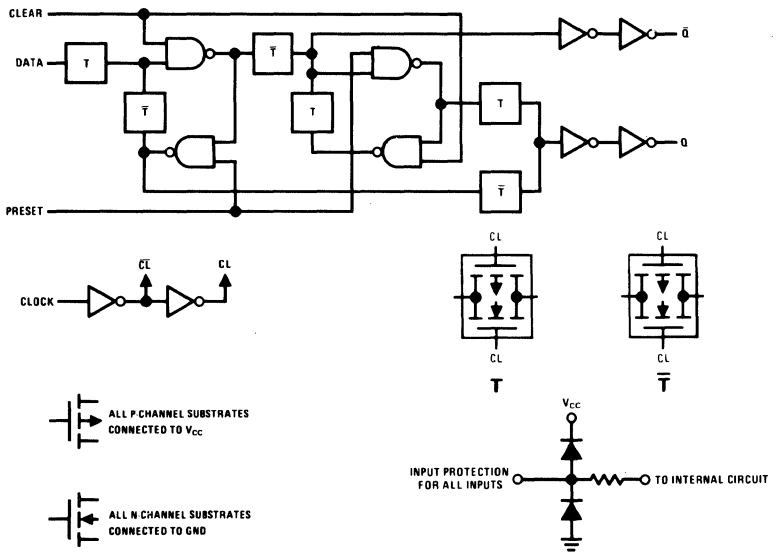
Functional Diagram



NOTE: A logic "0" on clear sets Q to logic "0"
A logic "0" on preset sets Q to logic "1"

TOP VIEW

Connection Diagrams



Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} + 0.3V	Maximum V_{CC} Voltage	16.0V
Operating Temperature	HD-54C74	-55°C to +125°C	Package Dissipation	500mW
	HD-74C74	-40°C to +85°C	Lead Temperature (Soldering, 10 Sec.)	300°C
Storage Temperature		-65°C to +150°C	Operating V_{CC} Range	+3.0V to +15.0V

ELECTRICAL CHARACTERISTICS

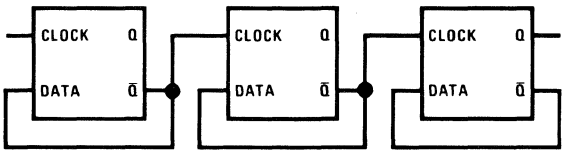
Min/Max limits apply across temperature range unless otherwise specified.
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5			V	V_{CC} = 5.0V
		8.0			V	V_{CC} = 10.0V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5	V	V_{CC} = 5.0V
				2.0	V	V_{CC} = 10.0V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5			V	V_{CC} = 5.0V, I_O = -10μA
		9.0			V	V_{CC} = 10.0V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5	V	V_{CC} = 5.0V, I_O = +10μA
				1.0	V	V_{CC} = 10.0V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$			1.0	μA	V_{CC} = 15.0V
Logical "0" Input Current	$I_{IN(0)}$	-1.0			μA	V_{CC} = 15.0V
Supply Current	I_{CC}		0.05	60	μA	V_{CC} = 15.0V
Input Capacitance	C_{IN}		5.0		pF	Any input
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" from Clock to Q or $\overline{Q}$			180	300	ns	V_{CC} = 5.0V
			70	110	ns	V_{CC} = 10.0V
Propagation Delay Time to a Logical "0" from Preset or Clear			180	300	ns	V_{CC} = 5.0V
			70	110	ns	V_{CC} = 10.0V
Propagation Delay Time to a Logical "1" from Preset or Clear			250	400	ns	V_{CC} = 5.0V
			100	150	ns	V_{CC} = 10.0V
Time Prior to Clock Pulse that Data must be Present	t_{set}		50	100	ns	V_{CC} = 5.0V
			20	40	ns	V_{CC} = 10.0V
Time After Clock Pulse that Data must be Held			-20	0	ns	V_{CC} = 5.0V
			-8.0	0	ns	V_{CC} = 10.0V
Minimum Clock Pulse Width	t_{WL}=t_{WH}		100		ns	V_{CC} = 5.0V
			40		ns	V_{CC} = 10.0V
Minimum Preset and Clear Pulse Width			100	160	ns	V_{CC} = 5.0V
			40	70	ns	V_{CC} = 10.0V
Maximum Clock Rise and Fall Time		15.0			μs	V_{CC} = 5.0V
		5.0			μs	V_{CC} = 10.0V
Maximum Clock Frequency		2.0	3.5		MHz	V_{CC} = 5.0V
		5.0	8.0		MHz	V_{CC} = 10.0V
LOW POWER TTL/CMOS INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} −1.5			V	54C, V_{CC} = 4.5V
						74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.75V
						74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_D = -360μA
						74C, V_{CC} = 4.75V, I_D = -360μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.50V, I_D = 360μA
						74C, V_{CC} = 4.75V, I_D = 360μA
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" from Clock			250		V	V_{CC} = 5.0V, C_L = 50pF, T_A = 25°C

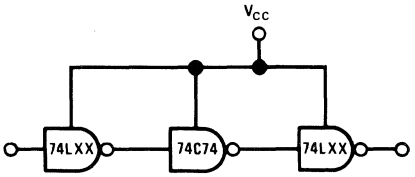
NOTE: 1. These devices should not be connected under power on conditions.

Typical Applications

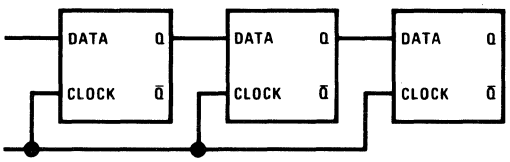
Ripple Counter (Divide by 2^n)



74C Compatibility

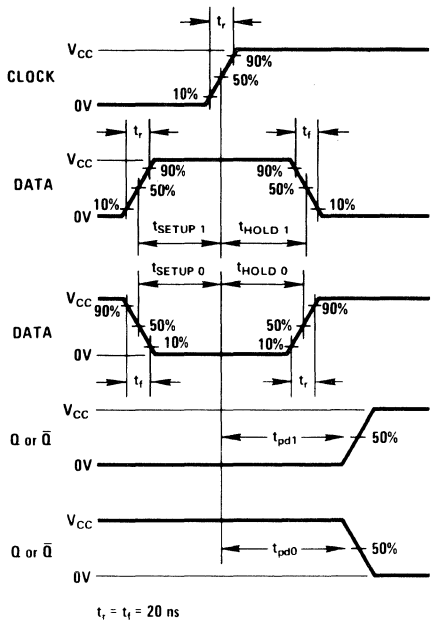


Shift Register



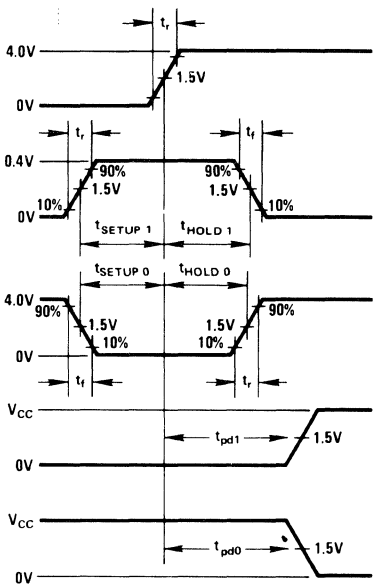
Switching Time Waveforms

CMOS to CMOS



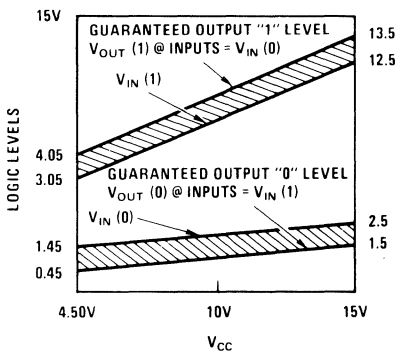
$t_r = t_f = 20$ ns

TTL to CMOS

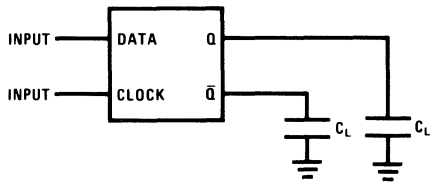


Typical Characteristics

Guaranteed Noise Margin as a Function of V_{CC}



AC Test Circuit



HD-54C83/HD-74C83

4-Bit Binary Full Adder

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER T^2L COMPATIBLE — DRIVE 2LT^{2}L LOADS

Package

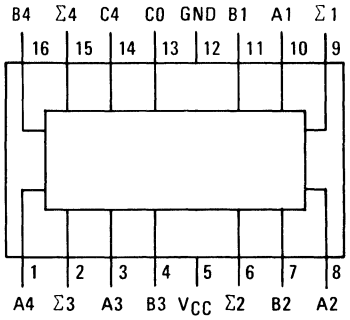
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Description

The HD-54C83/HD-74C83 4-bit binary full adder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. The adders are designed so that logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

Connection Diagram



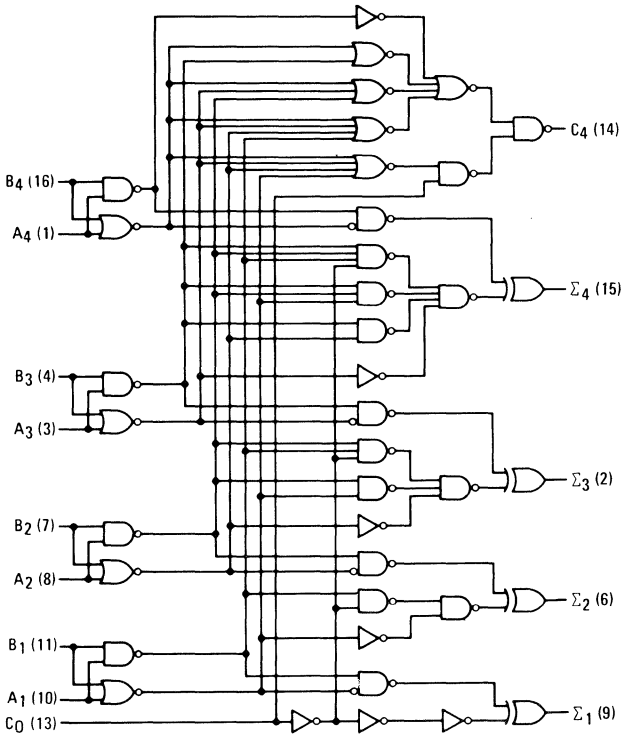
Truth Table

INPUT				OUTPUT					
				WHEN C0=L			WHEN C0=H		
				WHEN C2=L			WHEN C2=H		
A1/A3	B1/B3	A2/A4	B2/B4	Σ1/Σ3	Σ2/Σ4	C2/C4	Σ1/Σ3	Σ2/Σ4	C2/C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	L	H	H	H	H	H	H

H = High Level L = Low Level

NOTE: Input conditions at A3, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs Σ3, Σ4 and C4.

Logic Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at any Pin		-0.3V to V_{CC} +0.3V	Package Dissipation	500mW
Operating Temperature Range	HD-54C83	-55°C to +125°C	Operating V_{CC} Range	3V to 15V
	HD-74C83	-40°C to +85°C	Absolute Maximum V_{CC}	16V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

Min/Max Limits apply across temperature range, unless otherwise specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15V
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC}-1.5			V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4 0.4	V V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
	OUTPUT DRIVE						
	Output Source Current (P-Channel)	I_{Source}	-1.75	-3.3		mA	V_{CC} = 5.0V, V_{Out} = 0V T_A = 25°C
	Output Source Current (P-Channel)	I_{Source}	-8.0	-15		mA	V_{CC} = 10V, V_{Out} = 0V T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	1.75	3.6		mA	V_{CC} = 5.0V, V_{Out} = V_{CC} T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	8.0	16		mA	V_{CC} = 10V, V_{Out} = V_{CC} T_A = 25°C

NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. C_{PD} determines the no load AC power consumption of any CMOS device.

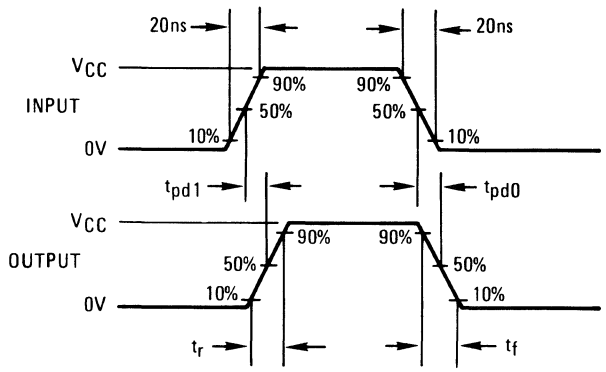
Specifications

ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $C_L = 50pF$, Unless Otherwise Specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
A.C.	Propagation Delay from C_0 to C_4	t_{pd0} or t_{pd1}		120 50	200 80	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay from Sum Inputs to C_4	t_{pd0} or t_{pd1}		250 90	450 150	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Dealy from C_0 to Sum Outputs	t_{pd0} or t_{pd1}		350 125	550 200	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay from Sum Inputs to Sum Outputs	t_{pd0} or t_{pd1}		300 110	550 180	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Input Capacitance			5.0		pF	Any Input (Note 2)
	Power Dissipation Capacitance	C_{PD}		120		pF	Per Package (Note 3)

Switching Time Waveforms



Inputs must be tied to appropriate logic level.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C85/HD-74C85

4-Bit Magnitude Comparator

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER TTL COMPATIBILITY — FAN OUT OF 2 DRIVING 74L
- EXPANDABLE TO "N" STAGES
- APPLICABLE TO BINARY OR BCD

Package

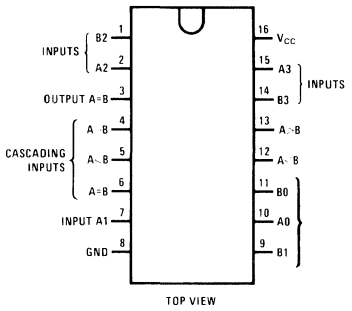
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Description

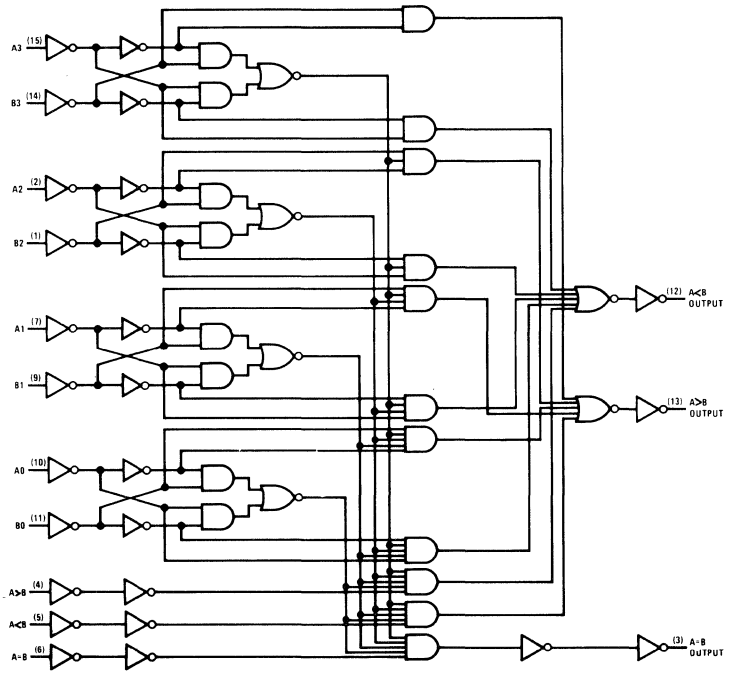
The HD-54C85/HD-74C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A>B, A<B and A = B), and three outputs (A>B, A<B and A = B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A>B, A<B and A = B) of the least-significant stage to the cascade inputs (A<B, A<B and A = B) of the next-significant stage. In addition, the least significant stage must have a high level voltage ($V_{IN(1)}$) applied to the A = B input and low level voltages ($V_{IN(0)}$) applied to A>B and A<B inputs.

Functional Diagram



TOP VIEW

Logic Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin		-0.3V to V_{CC} + 0.3V	Package Dissipation	500mW
Operating Temperature Range	HD-54C85	-55°C to +125°C	Operating V_{CC} Range	3.0V to 15.0V
	HD-74C85	-40°C to +85°C	V_{CC}	16.0V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

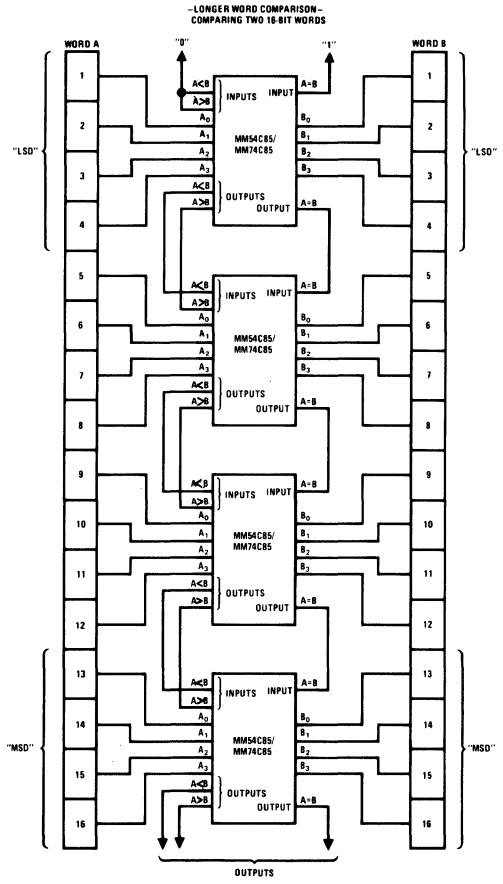
Min/Max limits apply across temperature range, unless otherwise noted.

T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15V
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} -1.5			V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4 0.4	V V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
	OUTPUT DRIVE						
	Output Source Current (P-Channel)	I_{Source}	-1.75	-3.3		mA	V_{CC} = 5.0V, V_{Out} = 0V T_A = 25°C
	Output Source Current (P-Channel)	I_{Source}	-8.0	-15		mA	V_{CC} = 10V, V_{Out} = 0V T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	1.75	3.6		mA	V_{CC} = 5.0V, V_{Out} = V_{CC} T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	8.0	16		mA	V_{CC} = 10V, V_{Out} = V_{CC} T_A = 25°C
A.C.	Propagation Delay Time from any A or B Data Input to any Data Output	t_{pd0} or t_{pd1}		250 100	600 300	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay Time from any Cascade Input to any Output	t_{pd0} or t_{pd1}		200 100	500 250	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Input Capacitance	C_{IN}		5.0		pF	Any Input
	power Dissipation Capacitance	C_{pd}		45		pF	(Note 3) per Package

NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. C_{pd} determines the no load AC power consumption of any CMOS device.

Typical Application

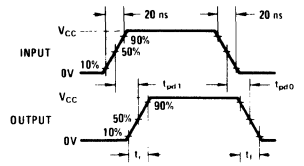


Truth Table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

Switching Time Waveform



UNUSED INPUTS MUST BE TIED TO AN APPROPRIATE LOGIC LEVEL

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C89/HD-74C89

64-Bit Three-State Random Access Read/Write Memory

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45V_{CC} TYP.
- LOW POWER TTL COMPATIBILITY — FAN OUT OF 2 DRIVING 74L
- INPUT ADDRESS REGISTER
- LOW POWER CONSUMPTION — 100nW/PACKAGE TYP.
- LOW POWER CONSUMPTION — 100nW/PACKAGE TYP.
- FAST ACCESS TIME — 130ns TYP. AT V_{CC} = 10.0V
- THREE STATE OUTPUT

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Description

The HD-54C89/HD-74C89 is a 16 word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four three state data output lines working in conjunction with the memory enable input provides for easy memory expansion.

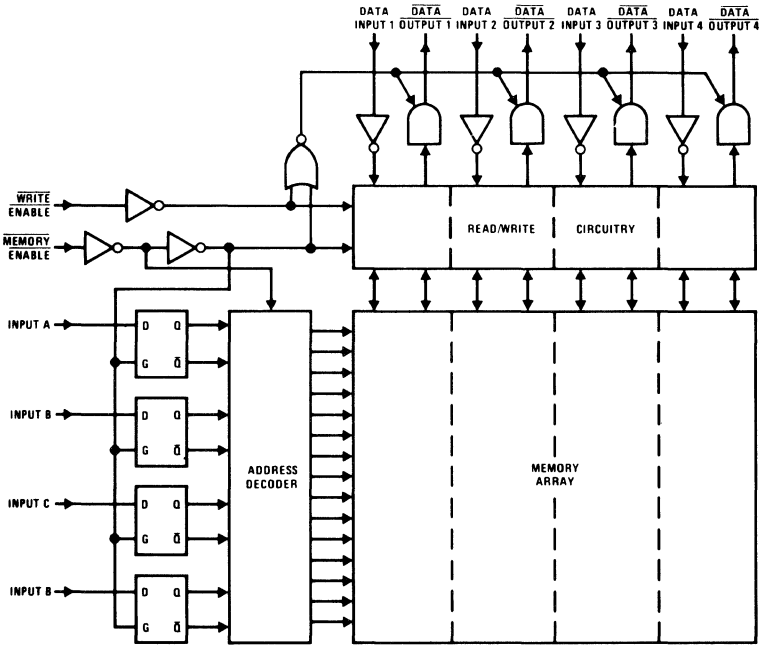
ADDRESS OPERATION: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable.)

WRITE OPERATION: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

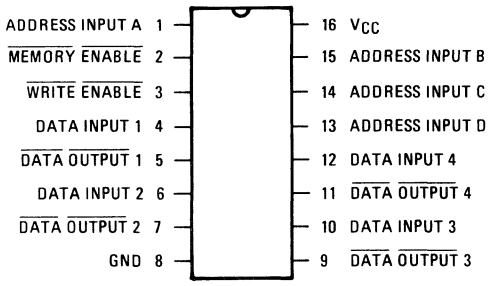
READ OPERATION: The complement of the information which was written into the memory is nondestructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a three state (HI-Z) condition.

Circuit Diagram



Connection Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin		-0.3V to V_{CC} + 0.3V	Package Dissipation	500mW
Operating Temperature Range	HD-54C89	-55°C to +125°C	Operating V_{CC} Range	3.0V to 15.0V
	HD-74C89	-40°C to +85°C	Absolute Maximum V_{CC}	16.0V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range, unless otherwise noted.

	PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Output Current in High Impedance State		 -1.0	0.005 -0.005	1.0	μA μA	V_{CC} = 15V, V_O = 15V V_{CC} = 15V, V_O = 0V
	Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15V
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} -1.5			V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
	Logical "0" output Voltage	$V_{Out(0)}$			0.4 0.4	V V	54C, V_{CC} = 4.5V, I_O = +360μA 74C, V_{CC} = 4.75V, I_O = +360μA
	OUTPUT DRIVE						
	Output Source Current (P-Channel)	I_{Source}	-1.75	-3.3		mA	V_{CC} = 5.0V, V_{Out} = 0V T_A = 25°C
	Output Source Current (P-Channel)	I_{Source}	-8.0	-15		mA	V_{CC} = 10V, V_{Out} = 0V T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	1.75	3.6		mA	V_{CC} = 5.0V, V_{Out} = V_{CC} T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	8.0	16		mA	V_{CC} = 10V, V_{Out} = V_{CC} T_A = 25°C

Specifications (continued)

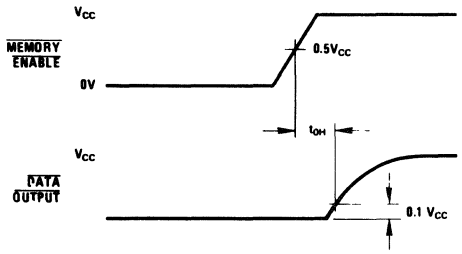
$T_A = 25^oC$, $C_L = 50pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	CONDITIONS
A.C.	Propagation Delay from Memory Enable	t_{pd}		270 100	500 220	ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Access Time from Address Input	t_{acc}		350 130	650 280	ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Address Input Setup Time	t_{SA}	150 60			ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Address Input Hold Time	t_{HA}	60 40			ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Memory Enable Pulse Width	t_{ME}	400 150	250 90		ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Memory Enable Pulse Width	$t_{\overline{ME}}$	400 150	200 70		ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Write Enable Setup Time for a Read	t_{SR}	0 0			ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Write Enable Setup Time for a Write	t_{WS}			t_{ME} t_{ME}	ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Write Enable Pulse Width	$t_{\overline{WE}}$		160 60	300 100	ns ns	$V_{CC} = 5.0V$, $t_{WS} = 0$ $V_{CC} = 10V$, $t_{WS} = 0$
	Data Input Hold Time	t_{HD}	50 25			ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Data Input Setup	t_{SD}	50 25			ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Memory Enable	t_{IH}, t_{OH}		180 85	300 120	ns ns	$V_{CC} = 5.0V$, $C_L = 5.0pF$, $R_L = 10K$ $V_{CC} = 10V$, $C_L = 5.0pF$, $R_L = 10K$
	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Write Enable	t_{IH}, t_{OH}		180 85	300 120	ns ns	$V_{CC} = 5.0V$, $C_L = 5.0pF$, $R_L = 10K$ $V_{CC} = 10V$, $C_L = 5.0pF$, $R_L = 10K$
	Input Capacity	C_{IN}		5.0		pF	Any Input (Note 2)
	Output Capacity	C_{Out}		6.5		pF	Any Output (Note 2)
	Power Dissipation Capacity	C_{pd}		230		pF	(Note 3)

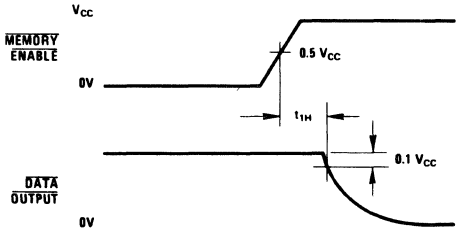
NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. C_{PD} determines the no load AC power consumption of any CMOS device.

Waveforms

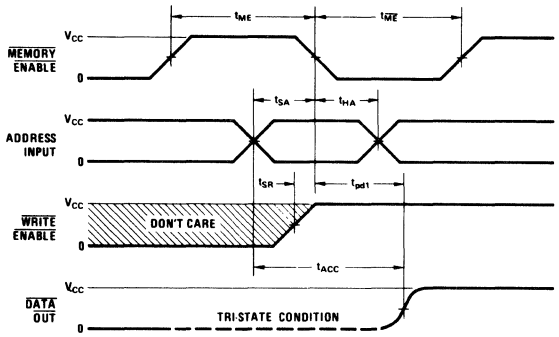
t_{0H}



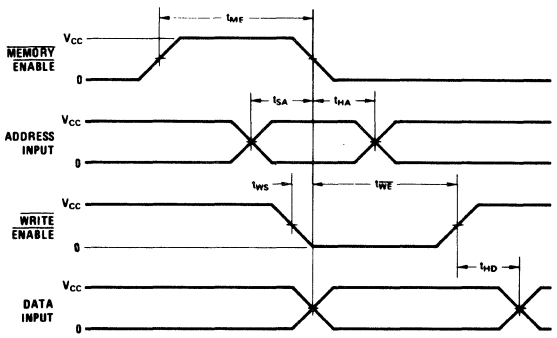
t_{1H}



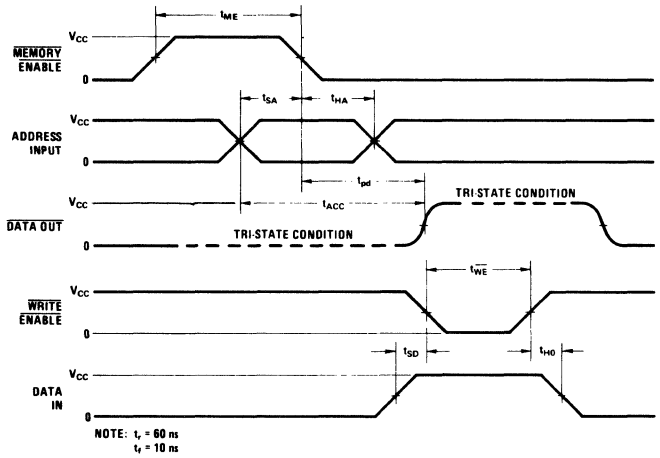
Read Cycle



Write Cycle



Read Modify Write Cycle

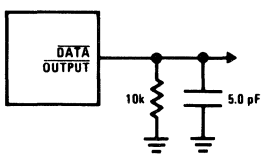


Truth Table

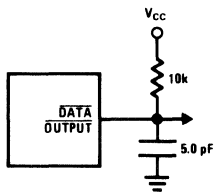
ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Three State
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	Three State
H	H	Do Nothing	Three State

AC Test Circuits

t_{1H}



t_{0H}



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C95/HD-74C95

4-Bit Right-Shift, Left-Shift Register

Features

- MEDIUM SPEED OPERATION — 10MHz TYP. V_{CC} = 10.0V C_L = 50pF
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER — 100nW TYP.
- LOW POWER TTL COMPATIBLE — DRIVE 2 LTTL LOADS
- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- SYNCHRONOUS PARALLEL LOAD
- PARALLEL INPUTS AND OUTPUTS FROM EACH FLIP-FLOP
- NEGATIVE EDGE TRIGGERED CLOCKING

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

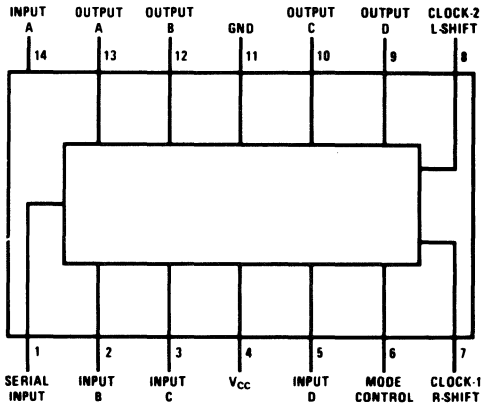
Description

This four-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right-shift or left-shift register.

When a logical "0" level is applied to the mode control input, the output of each flip-flop is coupled to the D input of the succeeding flip-flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop and serial data is entered at input D.

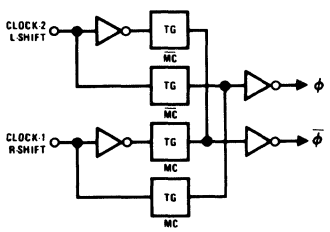
Connection Diagram

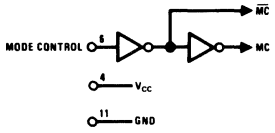
Dual-In-Line Package

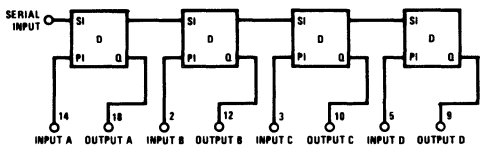


TOP VIEW

Circuit Diagrams







MODE CONTROL = 0 FOR RIGHT SHIFT
MODE CONTROL = 1 FOR LEFT SHIFT OR PARALLEL LOAD

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} + 0.3V	Maximum V_{CC} Voltage	16.0V
Operating Temperature	HD-54C95	-55°C to +125°C	Package Dissipation	500mW
	HD-74C95	-40°C to +85°	Operating V_{CC} Range	+3.0V to +15.0V
Storage Temperature		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

Max/Min limits apply across temperature range unless otherwise specified.
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8			V V	V_{CC} = 5.0V V_{CC} = 10V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2	V V	V_{CC} = 5.0V V_{CC} = 10V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			.5 1	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$			1	μA	V_{CC} = 15V
Logical "0" Input Current	$I_{IN(0)}$	-1			μA	V_{CC} = 15V
Supply Current	I_{CC}		0.050	300	μA	V_{CC} = 15V
Input Capacitance	C_{IN}		5		pF	Any input
Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	t_{pd0} or t_{pd1}		200 80	400 160	ns ns	V_{CC} = 5.0V V_{CC} = 10V
Time Prior to Clock Pulse that Data Must be Preset	t_{setup}		15 10		ns ns	V_{CC} = 5.0V V_{CC} = 10V
Time After Clcok Pulse that Data Must be Held			0 0		ns ns	V_{CC} = 5.0V V_{CC} = 10V
Minimum Clock Pulse Width	t_{WL} = t_{WH}		100 50		ns ns	V_{CC} = 5.0V V_{CC} = 10V
Minimum Mode Control Pulse Width			100 40		ns ns	V_{CC} = 5.0V V_{CC} = 10V
Maximum Input Clock Frequency		3 6.5	4.5 10		MHz MHz	V_{CC} = 5.0V V_{CC} = 10V
LOW POWER TTL/ CMOS INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} −1.5			V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_D = -100μA 74C, V_{CC} = 4.75V, I_D = -100μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_D = 360μA 74C, V_{CC} = 4.75V, I_D = 360μA
Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	t_{pd0} or t_{pd1}		175		ns	V_{CC} = 5.0V

NOTE: These devices should not be connected under "Power On" conditions.

Truth Table

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	L	H	X	X	X	X	X	Undefined			
↓	H	L	X	X	X	X	X	Operating Conditions			

† Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C or D respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D respecitively before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D respecitvely before the most-recent ↓ transition of the clock.

HD-54C151/HD-74C151

8 Channel Digital Multiplexer

Description

- SUPPLY VOLTAGE RANGE — 3V to 15V
- LOW POWER TTL COMPATIBLE — DRIVE 2 LPTTL LOADS
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP
- LOW POWER — 50nW TYP

Features

The HD-54C151/HD-74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P- channel enhancement transistors.

This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical "1" on the strobe input forces W to a logical "1" and Y to a logical "0"

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

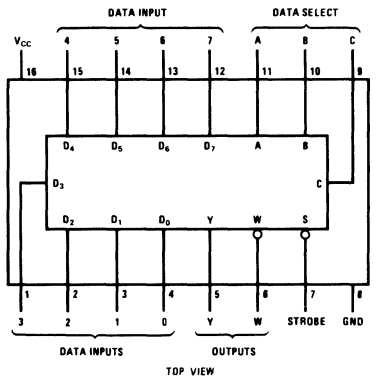
See package outline Code 1W and Code 9L.

Truth Table

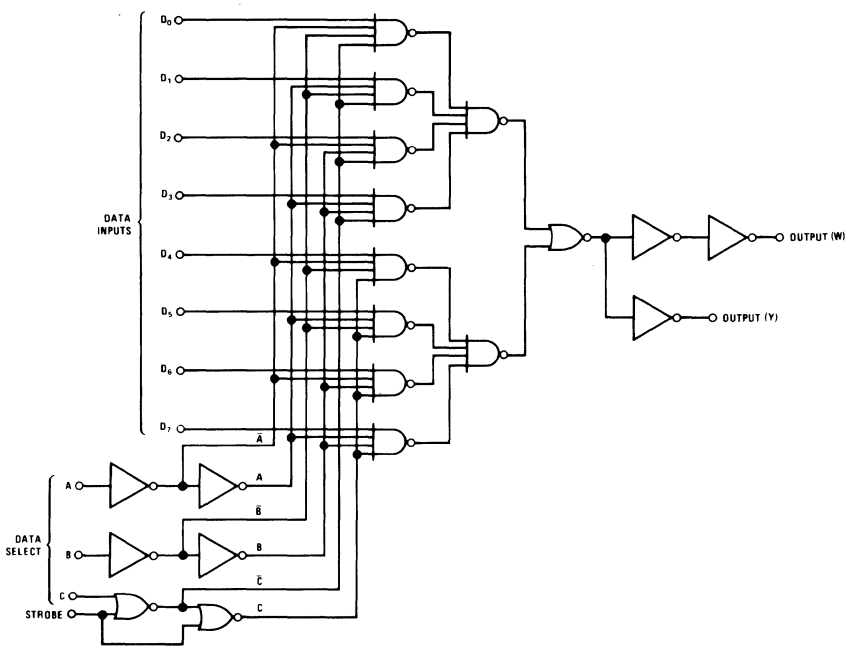
INPUTS											OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

Functional Diagram

Dual-In-Line Package



Logic Diagrams



Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} +0.3V	Maximum V_{CC} Voltage	16V
Operating Temperature	HD-54C151	-55°C to +125°C	Package Dissipation	500mW
	HD-74C151	-40°C to +85°C	Operating V_{CC} Range	3V to 15V
Storage Temperature		-65°C to +150°C	Lead Temperature (Soldering, 10 sec.)	300°C

ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range across otherwise specified

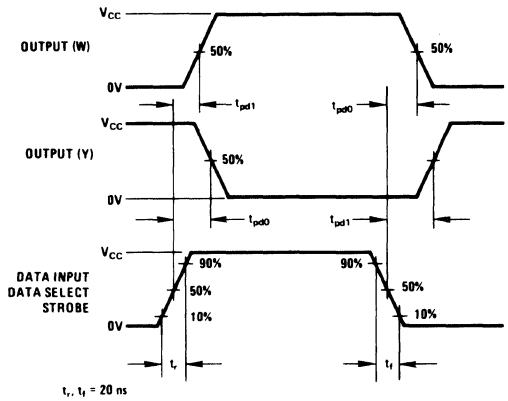
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8			V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "0" INput Voltage	$V_{IN(0)}$			1.5 2	V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10.0V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10.0V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$			1	μA	V_{CC} = 15.0V, V_{IN} = 15V
Logical "0" Input Current	$I_{IN(0)}$	-1			μA	V_{CC} = 15.0V, V_{IN} = 0V
Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15.0V
Input Capacitance	C_{IN}		5		pF	Any input
Propagation Delay Time to a Logical "0" or Logical "1" from Data to Y			170 80	270 130	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Propagation Dealy Time to a Logical "0" or Logical "1" from Data to W			200 90	300 140	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Propagation Delay Time to a Logical "0" or Logical "1" from Strobe or Data Select to Y			240 110	360 170	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
CMOS TO LOW POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} −1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
Propagation Delay Time to a Logical "0" t_{pd0} or a Logical "1" t_{pd1} from Data Input , to Y			200	320	ns	V_{CC} = 5.0V

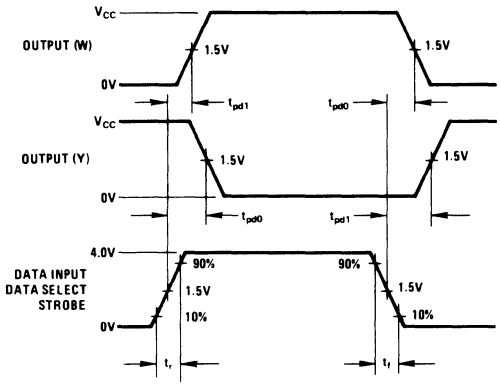
NOTE: 1. This device should not be connected under power on conditions.

Switching Time Waveforms

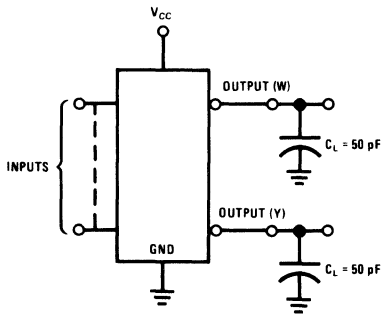
TTL to CMOS (t_{pd1} & t_{pd0})



TTL to CMOS (t_{pd1} & t_{pd0})



A.C. Test Circuit



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C154/HD-74C154

4-Line to 16-Line Decoder/Demultiplexer

Features

- SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- LOW POWER TLL COMPATIBLE — DRIVE 2 LPTTL LOADS
- HIGH NOISE MARGIN — 1V GUARANTEED
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER — 100nW TYP.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

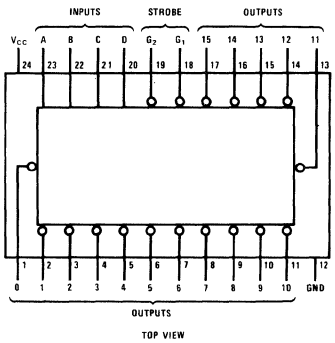
See package outline Code 1U and Code 9V.

Description

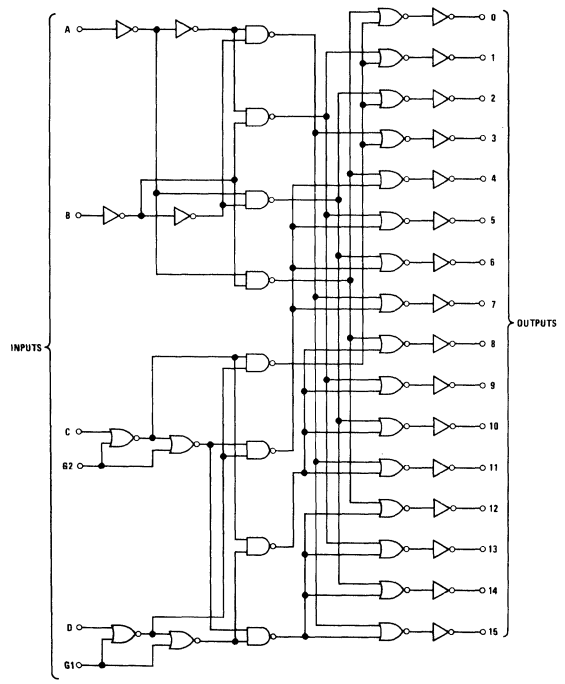
The HD-54C154/HD-74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the four-line input address.

Connection Diagram



Circuit Diagram



Truth Table

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} + 0.3V	Maximum V_{CC} Voltage	16.0V
Operating Temperature Range	HD-54C154	-55°C to +125°C	Package Dissipation	500mW
	HD-74C154	-40°C to +85°C	Operating Range, V_{CC}	+3.0V to +15.0V
Storage Temperature RAnge		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

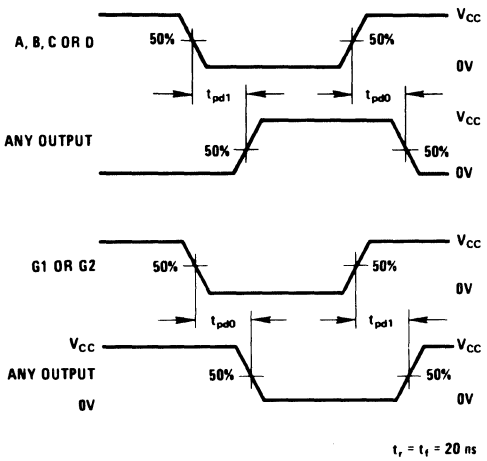
ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range unless otherwise specified.
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8			V V	V_{CC} = 5V V_{CC} = 10V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2	V V	V_{CC} = 5V V_{CC} = 10V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9			V V	V_{CC} = 5V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1	V V	V_{CC} = 5V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$		0.005	1	μA	V_{CC} = 15V, V_{IN} = 15V
Logical "0" Input Current	$I_{IN(0)}$	-1	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15V
Input Capacitance	C_{IN}		5		pF	Any input
Propagation Delay to a Logical "0" from any Input to any output	t_{pd0}		275	400	ns	V_{CC} = 5V
Propagation Delay to a Logical "0" from G1 or G2 to any Output	t_{pd0}		275	400	ns	V_{CC} = 5V
Propagation Delay to a Logical "1" from any Input to any Output	t_{pd1}		265	400	ns	V_{CC} = 5V
Propagation Delay to a Logical "1" from G1 or G2 to any Output	t_{pd1}		265	400	ns	V_{CC} = 5V
LOW POWER TTL/ CMOS INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} −1.5				54C, V_{CC} = 4.5 74C, V_{CC} = 4.75
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5 74C, V_{CC} = 4.75
Logical "1" Output Voltage	$V_{Out(1)}$	2.4				54C, V_{CC} = 4.5V, I_O = -100μA 74C, V_{CC} = 4.75V, I_O = -100μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75, I_O = 360μA

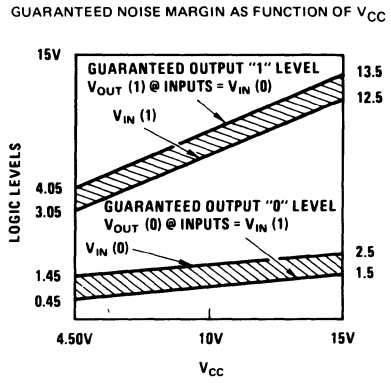
NOTE: 1. This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

Waveforms



$t_r = t_f$ = 20 ns

Noise Margin



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C157/HD-74C157

Quad 2-Input Multiplexers

Features

- SUPPLY VOLTAGE RANGE — 3V to 15V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP
- LOW POWER — 50nW (TYP)
- LOW POWER TTL COMPATIBLE — DRIVE 2 LPTTL LOADS

Description

These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement transistors. They consist of four 2-input multiplexers with a common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1" the outputs assume logical "0". Select decoding is done internally resulting in a single select input only.

Truth Table

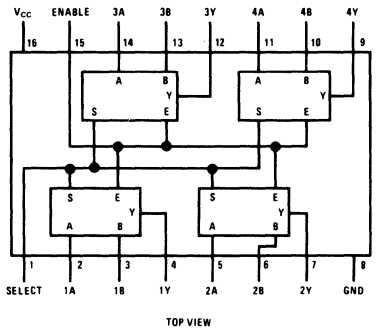
ENABLE	SELECT	A	B	OUTPUT Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

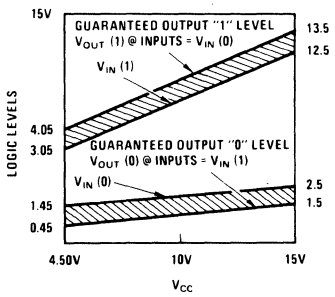
Connection Diagram



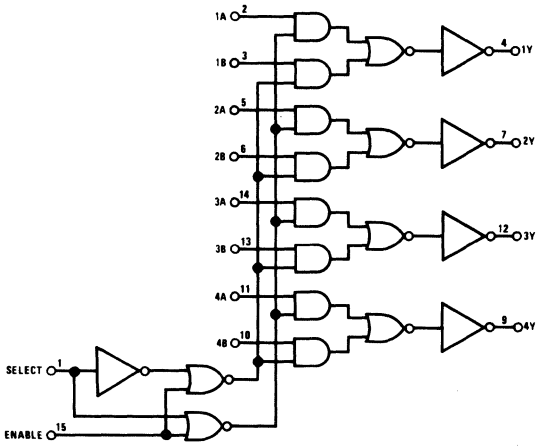
TOP VIEW

Noise Margin

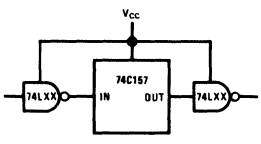
Guaranteed Noise Margin as a Function of V_{CC}.



Logic Diagrams



Typical Applications



74L COMPATIBILITY

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} to 0.3V	Storage Temperature	-65°C to 150°C
Operating Temperature	HD-54C157	-55°C to 125°C	Package Dissipation	500nW
	HD-74C157	-40°C to +85°C	Lead Temperature (Soldering, 10 sec)	300°C
Maximum V_{CC} Voltage		16V	Operating V_{CC} Range	+3V to 15V

ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range unless otherwise specified.

T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8			V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μa V_{CC} = 10.0V, I_O = -10μa
Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = -10μa V_{CC} = 10.0V, I_O = -10μa
Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15.0V
Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15.0V
Supply Current	I_{CC}		0.050	15	μA	V_{CC} = 15.0V
Input Capacitance	C_{IN}		5		pF	Any input
Propagation Delay from Data to Output	t_{pd0} or t_{pd1}		150 70	250 110	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Propagation Delay from Select to Output	t_{pd0} or t_{pd1}		180 80	300 130	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Propagation Delay from Enable to Output	t_{pd0}		180 80	300 130	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
CMOS TO LOW POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} -1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = 360 A 74C, V_{CC} = 4.75V, I_O = -360μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
Propagation Delay from Select to Output	t_{pd0} or t_{pd1}		250		ns	V_{CC} = 5.0V

NOTE: 1. This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C160/HD-74C160 *Decade Counter with Asynchronous Clear*
HD-54C161/HD-74C161 *Binary Counter with Asynchronous Clear*
HD-54C162/HD-74C162 *Decade Counter with Synchronous Clear*
HD-54C163/HD-74C163 *Binary Counter with Synchronous Clear*

Features

- HIGH NOISE MARGIN — 1V GUARANTEED
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER TLL COMPATIBLE — DRIVES 2 LPTTL LOADS
- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- INTERNAL LOOK-AHEAD FOR FAST COUNTING SCHEMES
- CARRY OUTPUT FOR N-BIT CASCADING
- LOAD CONTROL LINE
- SYNCHRONOUSLY PROGRAMMABLE

Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous and a low level at the clear input sets all our outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

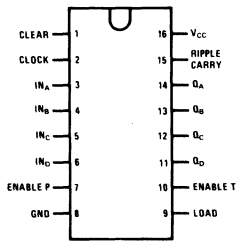
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive protion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual in-Line and Flat Packs.

See package outline Code 1W and Code 9L.

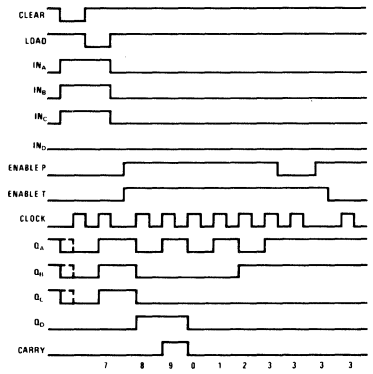
Connection Diagram



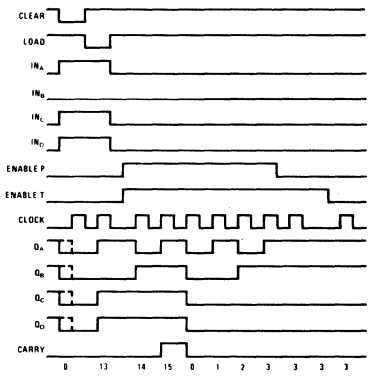
TOP VIEW

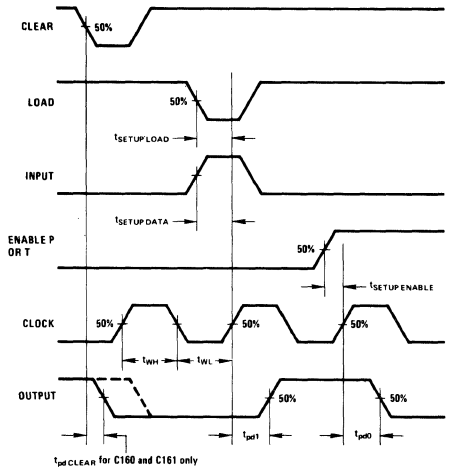
Waveforms

C160, --- C162 Decade Counters



C161, --- C163 Binary Counters





NOTE 1: ALL INPUT PULSES ARE FROM GENERATORS HAVING THE FOLLOWING CHARACTERISTICS: $t_r = t_f = 20$ ns PRR $\leq$ 1 MHz DUTY CYCLE $\leq$ 50%, $Z_{OUT} \approx 50\Omega$.

NOTE 2: ALL TIMES ARE MEASURED FROM 50% TO 50%.

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} + 0.3V	Maximum V_{CC} Voltage	16.0V
Operating Temperature	HD-54C160/1/2/3	-55°C to +125°C	Package Dissipation	500mW
	HD-74C160/1/2/3	-40°C to +85°C	Operating V_{CC} Range	+3.0V to +15.0V
Storage Temperature		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

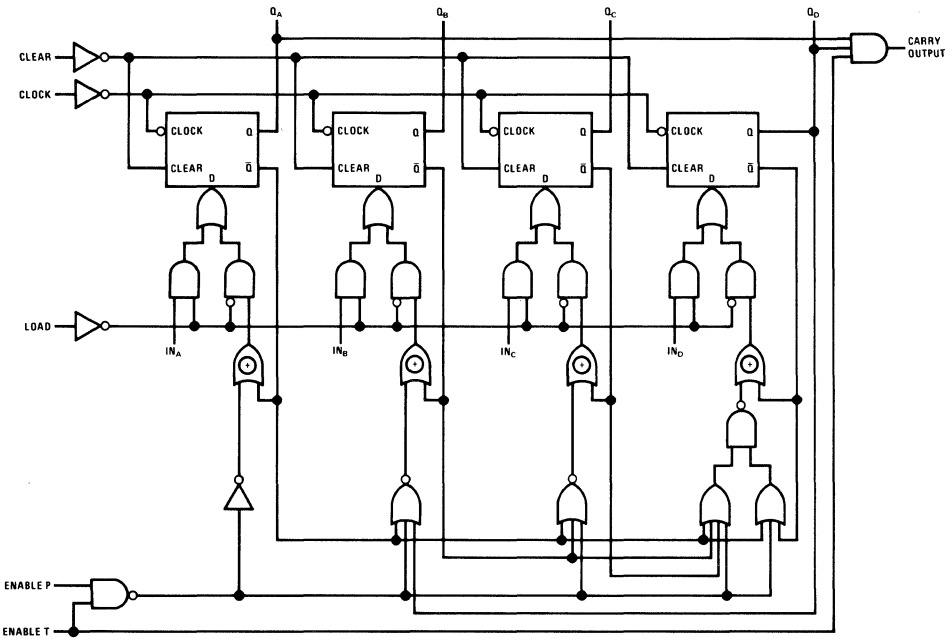
Min/Max limits apply across temperature range unless otherwise specified.
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified. .

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" INput Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5V V_{CC} = 10V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5V V_{CC} = 10V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} =15V
Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15V
Input Capacitance	C_{IN}		5		pF	Any input
Propagation delay time from Clock to Q	t_{pd0} or t_{pd1}		250 100	400 160	ns ns	V_{CC} = 5V V_{CC} = 10V
Propagation delay time from Clock to Carry Out	t_{pd0} or t_{pd1}		290 120	450 190	ns ns	V_{CC} = 5V V_{CC} = 10V
Propagation delay time from T enable to Carry Out	t_{pd0} or t_{pd1}		180 70	290	ns ns	V_{CC} = 5V V_{CC} = 10V
Propagation time from clear to Q(C162 and C163 only)	t_{pd0}		190 80	300	ns ns	V_{CC} = 5V V_{CC} = 10V
Time prior to clock that data or load must be present	$t_{set\ up}$		120 30		ns ns	V_{CC} = 5V V_{CC} = 10V
Time prior to clock that enable P or T must be present	$t_{set\ up}$		170 70	280 120	ns ns	V_{CC} = 5V V_{CC} = 10V
Time prior to clock that clear must be present(162,163 only)	$t_{set\ up}$		120 50	190 80	ns ns	V_{CC} = 5V V_{CC} = 10V
Minimum clock pulses width	t_{WL} or t_{WH}		90 35	170 70	ns ns	V_{CC} = 5V V_{CC} = 10V
Maximum clock rise or fall time				15 5.0	μs μs	V_{CC} = 5V V_{CC} =10V
Maximum clock frequency		2.0 5.5	3.0 8.5		MHz MHz	V_{CC} = 5V V_{CC} = 10V
CMOS/LPTTL INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} -1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{IN(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} =4.75, I_O = -360μA
Logical "0" Output Voltage	$V_{IN(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O =360μA 74C, V_{CC} = 4. 75V, I_O = 360μA

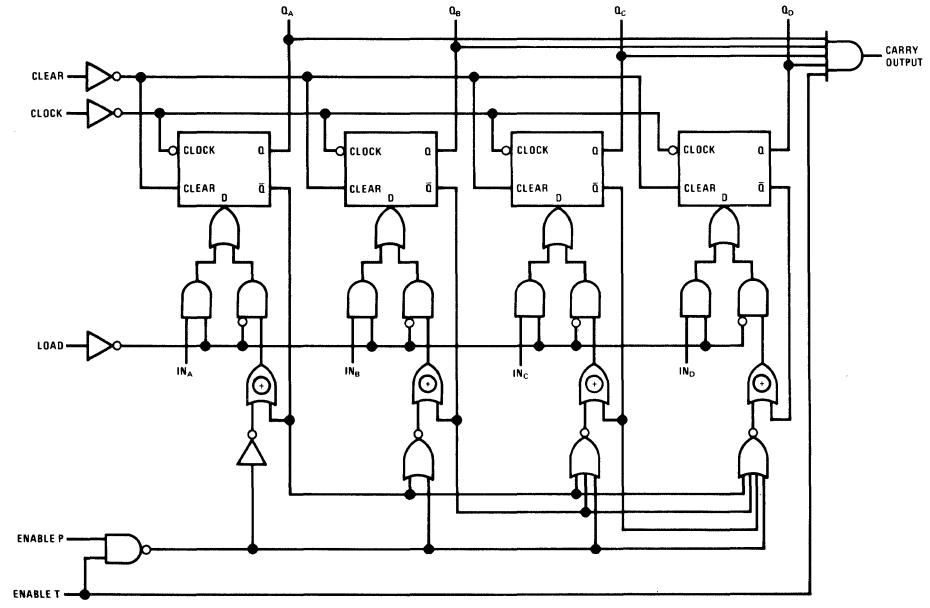
NOTE: 1. This device should not be connected during power on conditions.

Circuit Diagrams

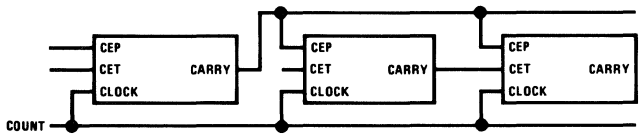
C160/C162; Clear is Synchronous for the C162



C161/C163; Clear is Synchronous for the C163



Cascading Packages



HD-54C164/HD-74C164

8-Bit Parallel-Out Serial Shift Register

Features

- SUPPLY VOLTAGE RANGE — 3V to 15V
- LOW POWER TTL COMPATIBLE — DRIVE 2 LPTTL LOADS
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP
- LOW POWER — 50nW TYP
- MEDIUN SPEED OPERATION — 8.0 MHz TYP WITH 10V SUPPLY

Truth Table

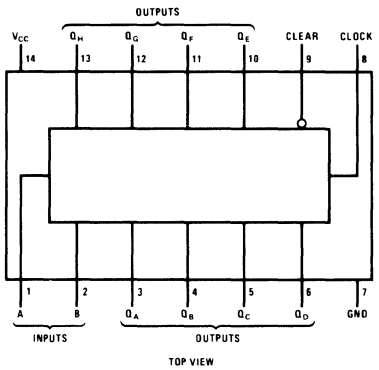
INPUTS t_n		OUTPUT t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

Decription

The HD-54C164/HD-74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P- channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. A high-level input enables the other input which will then determine the state of the flip-flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

Connection Diagrams



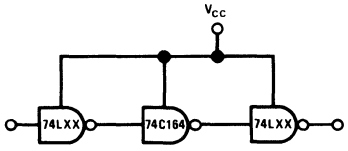
Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

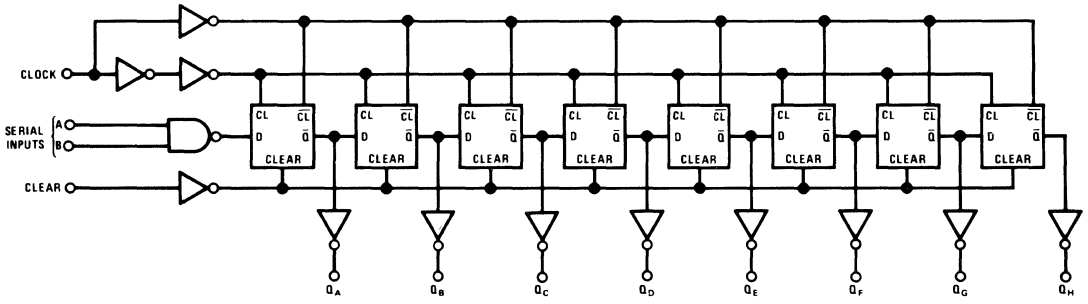
See package outline Code 1U and Code 9V.

Typical Applications

74C Compatibility



Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} +0.3V	Package Dissipation	500mW
Operating Temperature	HD-54C164	-55°C to +125°C	Maximum V_{CC} Voltage	16V
	HD-74C164	-40°C to +85°C	Operating V_{CC} Range	3V to 15V
Storage Temperature		-65°C to +150°C	Lead Temperature (Soldering, 10sec)	300°C

ELECTRICAL CHARACTERISTICS

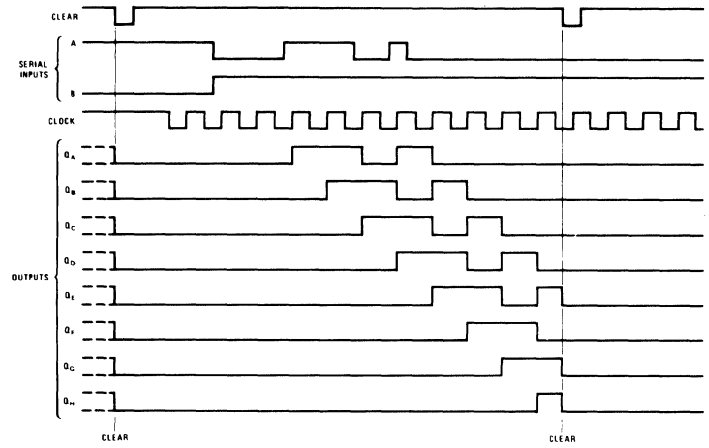
Min/Max limits apply across temperature range unless otherwise specified.

T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

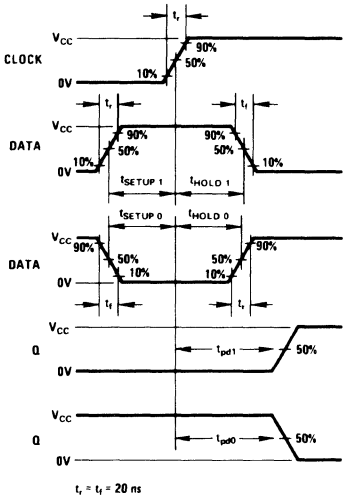
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8			V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2	V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10.0V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1	V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10.0V, I_O = -10μA
Logical "1" Input Current	$I_{IN(1)}$		0.005	1	μA	V_{CC} = 15.0V, V_{IN} = 15V
Logical "0" Input Current	$I_{IN(0)}$	-1	-0.005		μA	V_{CC} = 15.0V, V_{IN} = 0V
Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15.0V
Input Capacitance	C_{IN}		5		pF	Any input
Propagation delay time to a Logical "1" from Clock to Q			230 90	310 120	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Propagation delay time to a Logical "1" from Clear to Q			280 110	380 150	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Time prior to Clock Pulse that Data must be Present	$t_{set\ up}$		110 30		ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Time after Clock Pulse that Data must be Held			0 0		ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Maximum Clock Frequency		2 5.5	3 8		MHz MHz	V_{CC} = 5.0V V_{CC} = 10.0V
Minimum Clear Pulse Width			150 55		ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Maximum Clock Rise and Fall Time			1 130		ms μs	V_{CC} = 5.0V V_{CC} = 10.0V
CMOS TO LOW POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} −1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
Propagation delay time to a Logical "0" or Logical "1" from Clock to Q			320		ns	

NOTE: 1. These devices should not be connected under power on conditions.

Waveforms

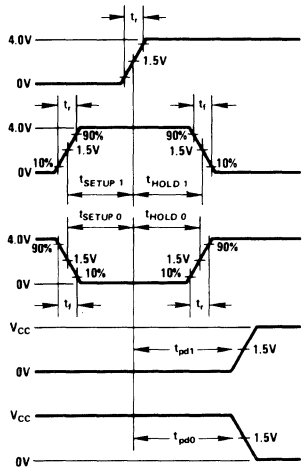


CMOS to CMOS

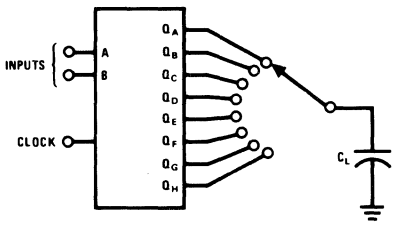


$t_r = t_f = 20$ ns

TTL to CMOS

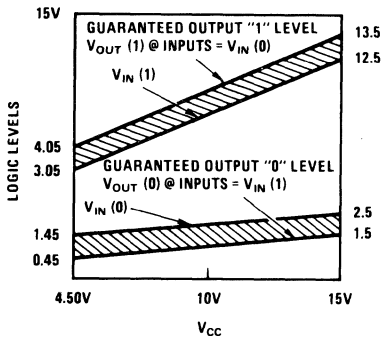


AC Test Circuit



Noise Margin

GUARANTEED NOISE MARGIN AS FUNCTION OF V_{CC}



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-54C165/HD-74C165

Parallel-Load 8-Bit Shift Register

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER T^2L COMPATIBLE — DRIVE 2 LT^2L LOADS

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Description

The HD54C165/HD74C165 is an 8-bit serial shift register which shifts data from Q_A to Q_H when clocked. Parrallel inputs to each stage are enabled by a low level at the shift/load input. Also included is a gated clock input and a complementary output from the eight-bit.

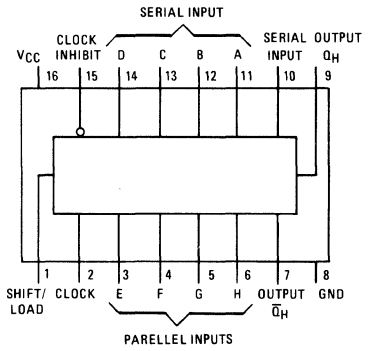
Clocking is accomplished through a 2-input NOR-gate permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the shift/load input high enables the other clock input. Data transfer occurs on the positive edge of the clock. The clock inhibit input should be changed to a high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

Truth Table

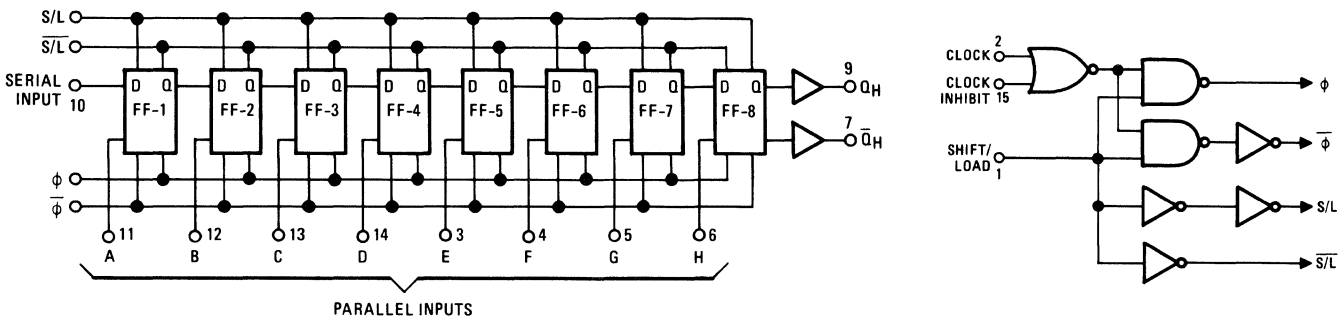
INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = $V_{IN(1)}$, L = $V_{IN(0)}$
X = Irrelevant
↑ = Transition from $V_{IN(0)}$ to $V_{IN(1)}$
a . . h = The level at data inputs A through H
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B or Q_H, before the indicated input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock.

Connection Diagrams



Block Diagram



ABSOLUTE MAXIMUM RATING

Voltage at any Pin		-0.3V to V_{CC} +0.3V	Package Dissipation	500mW
Operating Temperature Range	HD-54C165	-55°C to +125°C	Operating V_{CC} Range	3.0V to 15V
	HD-74C165	-40°C to +85°C	Absolute Maximum V_{CC}	16V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range, unless otherwise noted.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15V
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC}- 1.5			V V	54C, V_{CC} = 4.5V 75C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4 0.4	V V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
	OUTPUT DRIVE						
	Output Source Current (P-Channel)	I_{Source}	-1.75	-3.3		mA	V_{CC} = 5.0V, V_{Out} = 0V T_A = 25°C
	Output Source Current (P-Channel)	I_{Source}	-8.0	-15		mA	V_{CC} = 10V, V_{Out} = 0V T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	1.75	3.6		mA	V_{CC} = 5.0V, V_{Out} = V_{CC} T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	8.0	16		mA	V_{CC} = 10V, V_{Out} = V_{CC} T_A = 25°C

Specifications

ELECTRICAL CHARACTERISTICS

$T_A = 25^0C$, $C_L = 50$ pF, Input rise and fall times = 20 ns unless otherwise specified.

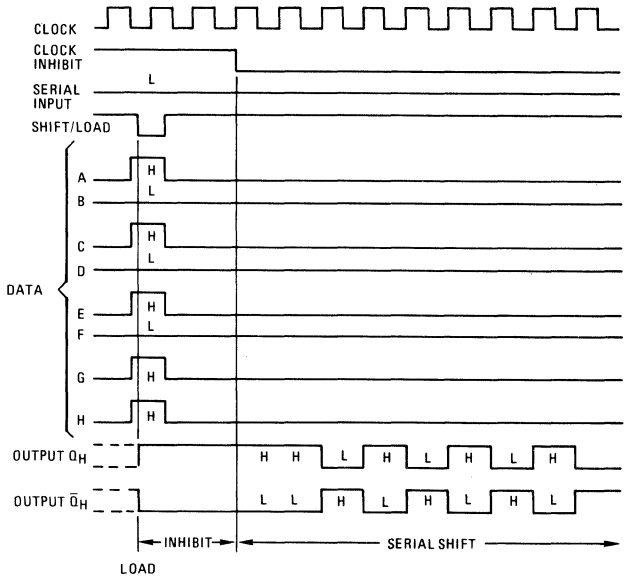
	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
A.C.	Propagation Delay Time to a Logical "0" or Logical "1" from Clock or Load to Q or $\overline{Q}$	t_{pd0}, t_{pd1}		200 80	400 200	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay Time to a Logical "0" or Logical "1" from H to Q or $\overline{Q}$	t_{pd0}, t_{pd1}		200 80	400 200	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Clock Inhibit Set Up Time		150 60	75 30		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Serial Input Set Up Time		50 30	25 15		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Serial Input Hold Time		50 30	0 0		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Parallel Input Set Up Time		150 60	75 30		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Parallel Input Hold Time		50 30	0 0		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Minimum Clock Pulse Width			70 30	200 100	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Minimum Load Pulse Width			85 30	180 90	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Maximum Clock Frequency			6.0 12	2.5 5.0	MHz MHz	V_{CC} = 5.0V V_{CC} = 10V
	Maximum Clock Rise and Fall Time		10 5.0			μs μs	V_{CC} = 5.0V V_{CC} = 10V
	Input Capacitance	C_{IN}		5.0		pF	(Note 2)
	Power Dissipation Capacitance	C_{pd}		65		pF	(Note 3)

NOTES: 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

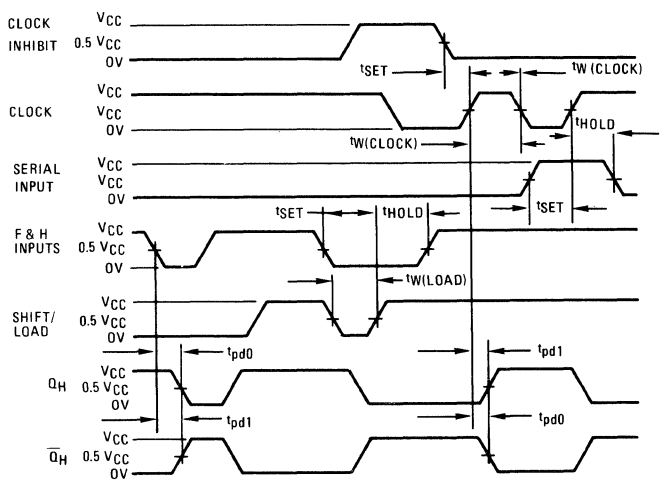
2. Capacitance is guaranteed by periodic testing.

3. C_{pd} determines the no load AC power consumption of any CMOS device.

Logic Waveforms



Switching Time Waveforms



NOTES: 1. The remaining six data and the serial input are low.
2. Prior to test, high level data is loaded into H input.

HD-54C173/HD-74C173

Three-State Quad D Flip-Flop

Features

- SUPPLY VOLTAGE RANGE — 3V TO 15V
- LOW POWER TTL COMPATIBLE — DRIVE 2 LPTTL LOADS
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER
- MEDIUM SPEED OPERATION — 12MHz TYP. WITH 10V SUPPLY
- HIGH IMPEDANCE THREE-STATE INPUT DISABLE WITHOUT GATING THE CLOCK

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Truth Table

Both Output Disables Low

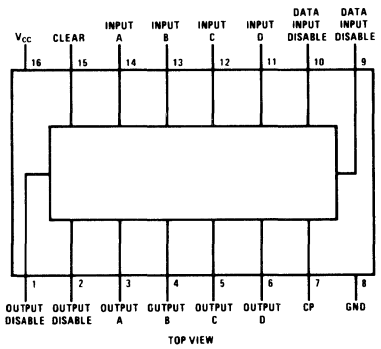
t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

Description

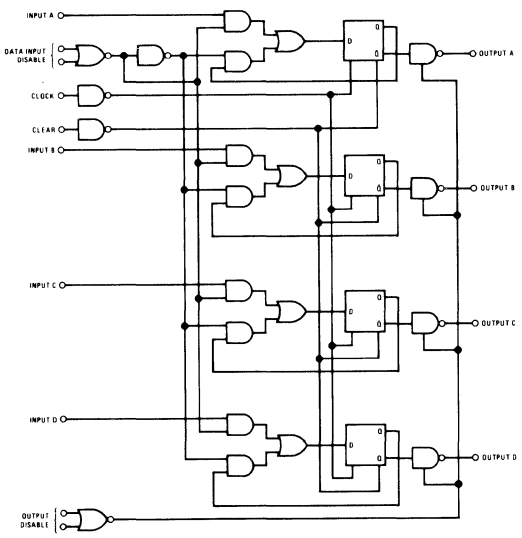
The HD-54C173/HD-74C173 three-state quad D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P- channel enhancement transistors. The four D type flip-flops operate synchronously from a common clock. The three-state output allows the device to be used in bus organized systems. The outputs are placed in the three-state mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip-flop to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip-flops do not change state.

Clearing is enable by taking the input to a logic "1" level. Clocking occurs on the positive going transition.

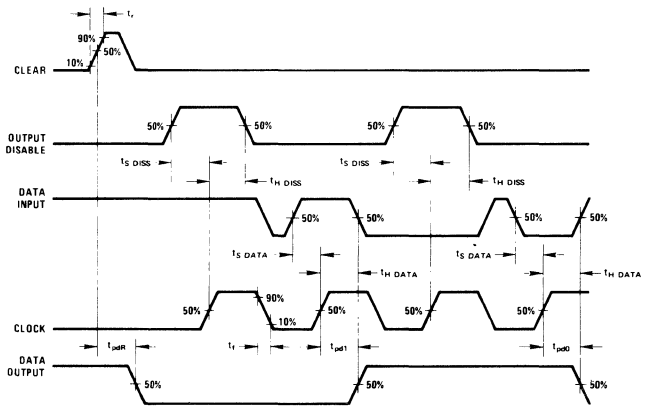
Connection Diagrams



Circuit Diagrams



Waveforms



Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3 to V_{CC} +0.3V	Maximum V_{CC} Voltage	16V
Operating Temperature	HD-54C173	-55°C to +125°C	Package Dissipation	500mW
	HD-74C173	-40°C to +85°C	Operating V_{CC} Range	+3V to +15V
Storage Temperature		-65°C to +150°C	Lead Temperature (Soldering, 10sec)	300°C

ELECTRICAL CHARACTERISTICS

Min/max limits apply across temperature range unless otherwise specified.

T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8			V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2	V V	V_{CC} = 5.0V V_{CC} = 10.0V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10.0V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10.0V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$		0.005	1	μA	V_{CC} = 15.0V
Logical "0" Input Current	$I_{IN(0)}$	-1	-0.005		μA	
Output current in High Impedance State			0.001 0.001		μA μA	V_{CC} = 15V, V_O = 15V V_O = 0V
Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15V
Input Capacitance	C_{IN}		5		pF	Any input
Propagation delay time to a Logical "0" or Logical "1" from Clock to Output	t_{pd0} or t_{pd1}		220 80	400 200	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Input Data setup Time	$t_{S\,DATA}$		40 15	80 30	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Input Data Hold Time	$t_{H\,DATA}$		0 0		ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Input Disable Setup Time	$t_{S\,DISS}$		100 35	200 70	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Input Disable Hold Time	$t_{H\,DISS}$		0 0		ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Delay from output disable to high impedance state(from logical "1" or Logical "0" level	t_{IH}, t_{OH}		170 70	340 140	ns ns	VCC = 5.0V V_{CC} = 10.0V
Delay from output disable to logical "1" level,(from high Impedance state)	t_{HI}		170 70	340 140	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Delay from output disable to Logical "0" Level(from High Impedance State)	t_{HO}		170 70	340 140	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Propagation Delay from Clear to Output	t_{pdR}		240 90	490 180	ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Maximum Clock Frequency		3.0 7	4.0 12		MHz MHz	V_{CC} = 5.0V V_{CC} = 10.0V
Minimum Clear Pulse Width			150 70		ns ns	V_{CC} = 5.0V V_{CC} = 10.0V
Maximum Clock Rise and Fall Time		10 5			μs μs	V_{CC} = 5.0V V_{CC} = 10.0V
LOW POWER TTL/ CMOS INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} —1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			.8	V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = -360μA 74C, V_{CC} = 4.75V, I_O = -360μA
Logical "0" Output Voltage	$V_{Out(0)}$			.4	V	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA
Propagation Delay Time to a Logical "0" or Logical "1" from Clock	t_{pd0} or t_{pd1}		500		ns	V_{CC} = 5.0V

NOTE: 1. These devices should not be connected under 'Power On' conditions.

HD-54C174/HD-74C174

Hex D Flip-Flop

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V to 15V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — $0.45V_{CC}$ typ
- LOW POWER T^2L COMPATIBILITY — fan out of 2 driving 74L

Package

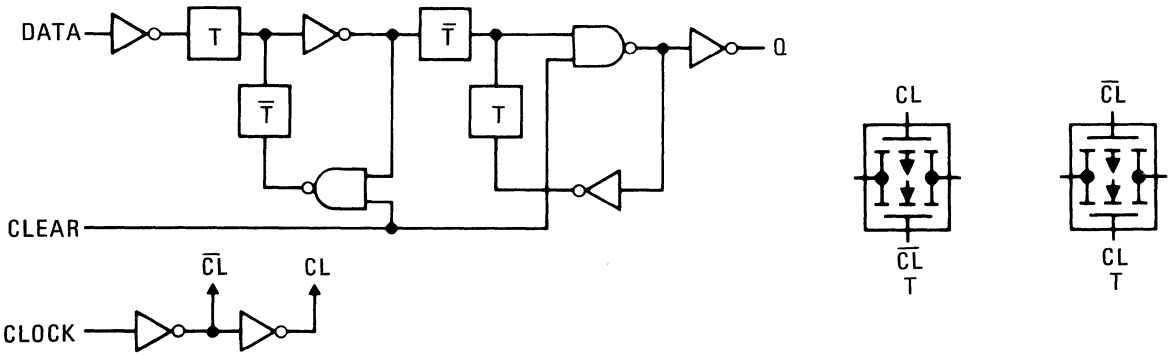
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Description

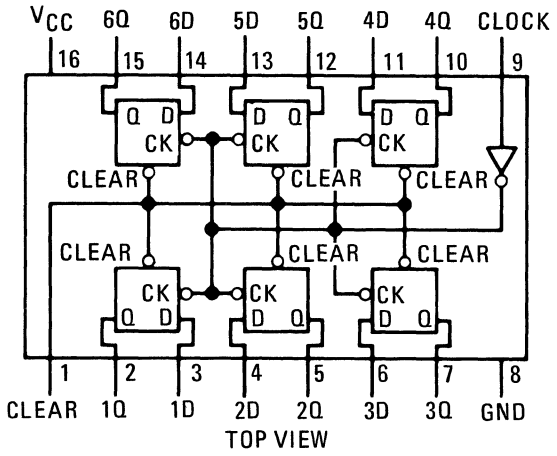
The HD54C174/HD74C174 hex D flip-flop is a monolithic complementary MOS(CMOS) integrated circuit constructed with N-and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes to V_{CC} and GND.

Logic Diagram



Connection Diagrams

DUAL-IN-LINE PACKAGE



TOP VIEW

Truth Table

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

Specifications

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage at Any Pin		-0.3V to V_{CC} +0.4V	Package Dissipation	500 mW
Operating Temperature Range	HD54C174	-55°C to +125°C	Operating V_{CC} range	3.0V to 15V
	HD74C174	0°C to +70°C	Absolute Maximum V_{CC}	16V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	CMOS TO CMOS					
D.C.	Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
	Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
	Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = -10 μA	4.5			V
		V_{CC} = 10V, I_O = -10 μA	9.0			V
	Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10 μA			0.5	V
		V_{CC} = 10V, I_O = +10 μA			1.0	V
	Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
	Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	-1.0	-0.005		μA
	Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
	CMOS/LPTL INTERFACE					
	Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}-1.5			V
		74C, V_{CC} = 4.75V	V_{CC}-1.5			V
	Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
	Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = -360 μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = -360 μA	2.4			V
	Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360 μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = 360 μA			0.4	V
	OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
	Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	-1.75	-3.3		mA
	Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	-8.0	-15		mA
	Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
	Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

NOTE 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device connot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply thatthe devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $C_L = 50$ pf, unless otnerwise specified

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
A.C.	Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) from Clock to Q	V_{CC} = 5.0V		150	300	ns
		V_{CC} = 10V		70	110	ns
	Propagation Delay Time to a Logical "0" from Clear	V_{CC} = 5.0		110	300	ns
		V_{CC} = 10V		50	110	ns
	Time Prior to Clock Pulse that Data Must be Present ($t_{SET\ UP}$)	V_{CC} = 5.0V	75			ns
		V_{CC} = 10V	25			ns
	Time After Clock Pulse that Data Must be Held (t_{HOLD})	V_{CC} = 5.0V	75			ns
		V_{CC} = 10V	25			ns
	Minimum Clock Pulse Width	V_{CC} = 5.0V		50		ns
		V_{CC} = 10V		35		ns
	Minimum Clear Pulse Width	V_{CC} = 5.0V		65		ns
		V_{CC} = 10V		35		ns
	Maximum Clock Rise and Fall Time	V_{CC} = 5.0V	15	1200		s
		V_{CC} = 10V	5.0	1200		s
	Maximum Clock Frequency	V_{CC} = 5.0V	2.0	6.5		MHz
		V_{CC} = 10V	5.0	12		MHz
	Input Capacitance (C_{IN})	Clear Input (Note 2)		11		pf
		Any Other Input		5.0		pf
	Power Dissipation Capacitance (C_{pd})	Per Package (Note 3)		95		pf

NOTE 2: Capacitance is guaranteed by periodic testing.

NOTE 3: C_{pd} determines the no load ad power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

HARRIS SEMICONDUCTOR
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Advanced Information

HD-54C175/HD-74C175

Quad D Flip-Flop

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- LOW POWER T^2L COMPATIBLE — DRIVE 2 LT^2L LOADS

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Description

These monolithic positive-edge-triggered flip-flops utilize complementary MOS (CMOS) integrated circuitry to implement D-type flip-flop logic. Both have a direct clear input and the 'C175 features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

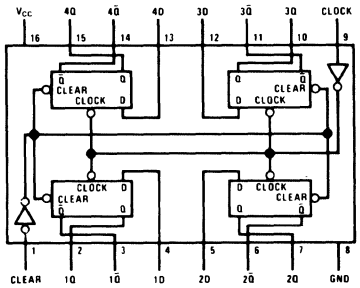
Truth Table

EACH FLIP-FLOP

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = C175 only

Connection Diagram



HD-54C175/HD-74C175
Quad D Flip-Flop

HARRIS SEMICONDUCTOR
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HD-54C192/HD-74C192

Synchronous 4-Bit Up/Down Decade Counter

HD-54C193/HD-74C193

Synchronous 4-Bit Up/Down Binary Counter

Features

- HIGH NOISE MARGIN — 1V GUARANTEED
- LOW POWER TTL COMPATIBLE — DRIVE 2 LPTTL LOADS
- WIDE SUPPLY RANGE — 3.0V TO 15.0V
- CARRY AND BORROW OUTPUTS FOR N-BIT CASCADING
- ASYNCHRONOUS CLEAR
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

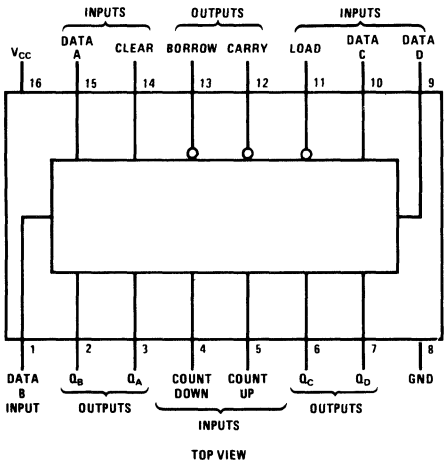
Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The HD-54C192 and HD-74C192 are BCD counters. While the HD-54C193 and HD-74C193 are binary counters.

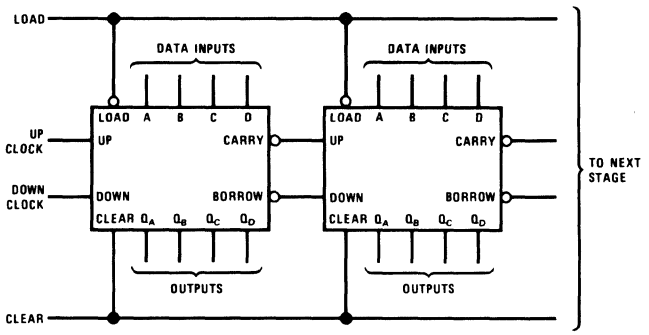
Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive going transition of this clock.

These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

Connection Diagram

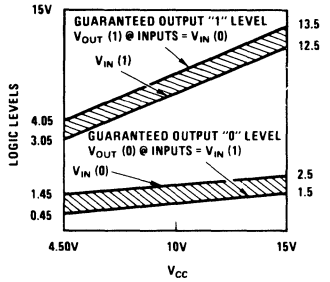


Functional Diagram



Noise Margin

GUARAUTEED NOISE MARGIN AS FUNCTION OF V_{CC}



Specifications

ABSOLUTE MAXIMUM RATINGS

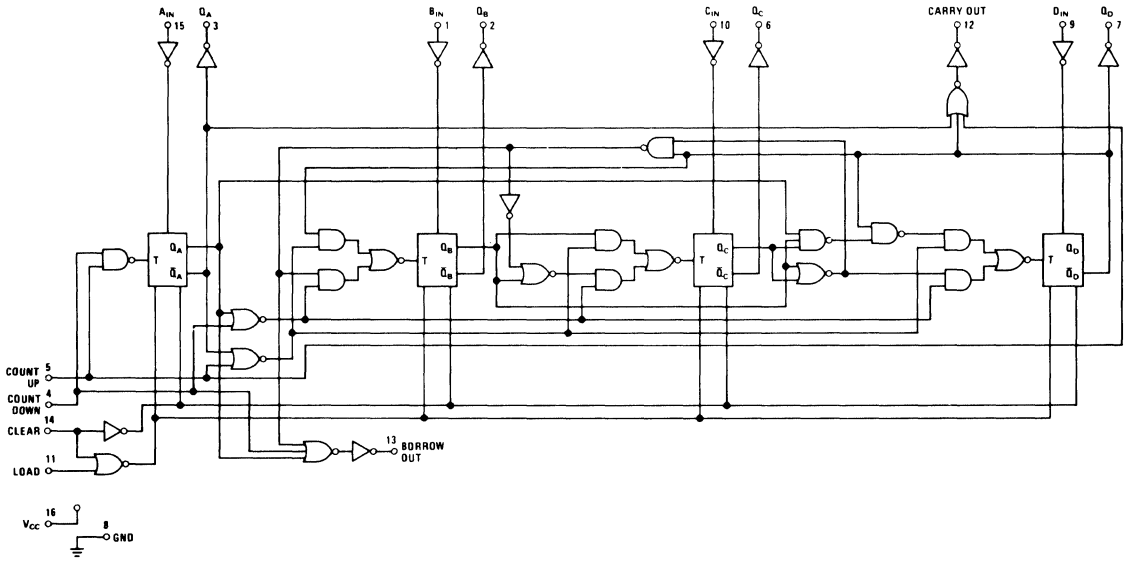
Voltage at Any Pin (Note 1)		-0.3V to V_{CC} +0.3V	Maximum V_{CC} Voltage	16.0V
Operating Temperature Range	HD-54C192, HD-54C193	-55°C to +125°C	Package Dissipation	500mW
	HD-74C192, HD-74C193	-40°C to +85°C	Operating V_{CC} Range	+3.0V to +15.0V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

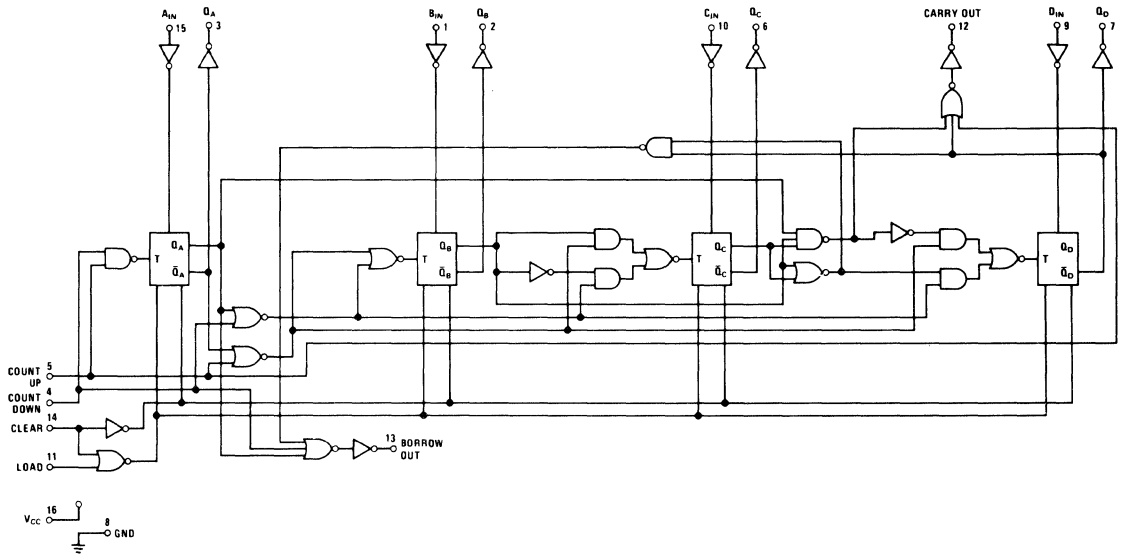
Min/Max limits apply across temperature range unless otherwise specified.
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO MOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5			V	V_{CC} = 5V
		8			V	V_{CC} = 10V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5	V	V_{CC} = 5V
				2	V	V_{CC} = 10V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5			V	V_{CC} = 5V, I_O = -10μA
		9			V	V_{CC} = 10V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5	V	V_{CC} = 5V, I_O = +10μA
				1	V	V_{CC} = 10V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
Supply Current	I_{CC}		0.05	300	μA	V_{CC} = 15V
Input Capacitance	C_{IN}		5		pF	Any input
Propagation Delay Time to Q From Count up or Down	t_{pd0} or t_{pd1}		250	400	ns	V_{CC} = 5V
			100	160	ns	V_{CC} = 10V
Propagation Delay Time to Borrow from Count Down	t_{pd0} or t_{pd1}		120	200	ns	V_{CC} = 5V
			50	80	ns	V_{CC} = 10V
Propagation Delay Time to Carry from Count Up	t_{pd0} or t_{pd1}		120	200	ns	V_{CC} = 5V
			50	80	ns	V_{CC} = 10V
Time Prior to Load that Data must be Present	t_{setup}		100	160	ns	V_{CC} = 5V
			30	50	ns	V_{CC} = 10V
Minimum Clear Pulse Width			300	480	ns	V_{CC} = 5V
			120	190	ns	V_{CC} = 10V
Minimum Load Pulse Width			100	160	ns	V_{CC} = 5V
			40	65	ns	V_{CC} = 10V
Propagation Delay Time to Q from Load	t_{pd0} or t_{pd1}		300	480	ns	V_{CC} = 5V
			120	190	ns	V_{CC} = 10V
Minimum Count Pulse Width			120	200	ns	V_{CC} = 5V
			35	80	ns	V_{CC} = 10V
Maximum Count Frequency		2.5	4		MHz	V_{CC} = 5V
		6	10		MHz	V_{CC} = 10V
Count Rise and Fall Time				15	μs	V_{CC} = 5V
				5	μs	V_{CC} = 10V
CMOS TO LOW POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC}			V	54C, V_{CC} = 4.5V
		—1.5			V	74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V
				0.8	V	74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = -100μA
		2.4			V	74C, V_{CC} = 4.75, I_O = -100μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_O = 360μA
				0.4	V	74C, V_{CC} = 4.75V, I_O = 360μA

NOTE: 1. This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.



HD-54C192 Synchronous 4-Bit Up/Down Decade Counter



HD-54C193 Synchronous 4-Bit Up/Down Binary Counter

HARRIS SEMICONDUCTOR
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HD-54C195/HD-74C195

4-Bit Registers

Features

- MEDIUM SPEED OPERATION – 10MHz TYP. WITH 10.0V SUPPLY AND 50pF LOAD
- HIGH NOISE IMMUNITY 0.45 V_{CC} (TYP.)
- LOW POWER 100nW (TYP.)
- LOW POWER TTL COMPATIBLE – DRIVE 2 LPTTL LOADS
- SUPPLY VOLTAGE RANGE – 3.0V TO 15.0V
- SYNCHRONOUS PARALLEL LOAD
- PARALLEL INPUTS AND OUTPUTS FROM EACH FLIP-FLOP
- DIRECT OVERRIDING CLEAR
- J AND $\overline{K}$ INPUTS TO FIRST STAGE
- COMPLEMENTARY OUTPUTS FROM LAST STAGE
- POSITIVE EDGE TRIGGERED CLOCKING
- DIODE CLAMPED INPUTS TO PROTECT AGAINST STATIC CHARGE

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Truth Table

INPUTS AT t_n		OUTPUTS AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Note: H = HIGH LEVEL, L = LOW LEVEL
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_{An} = State of Q_A at t_n.

Description

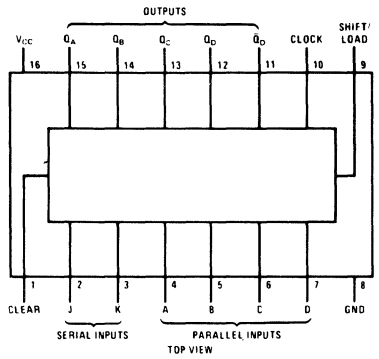
The HD-54C195/HD-74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible.

Parallel Load
Shift in direction Q_A towards Q_D

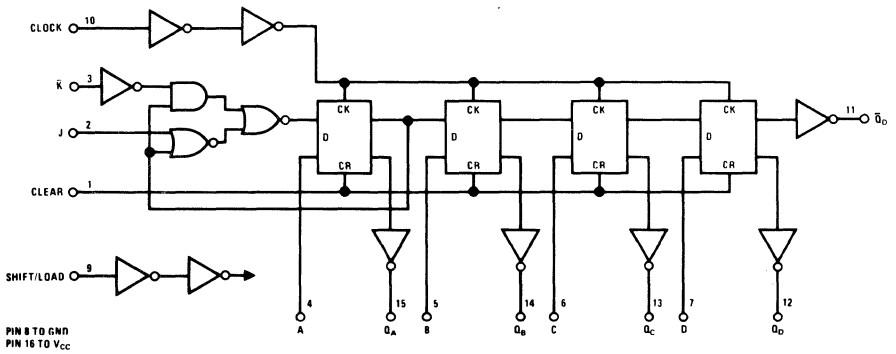
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$, D or T-type flip-flop as shown in the truth table.

Connection Diagram



Circuit Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)		-0.3V to V_{CC} +0.3V	Maximum V_{CC} Voltage	16.0V
Operating Temperature	HD-54C195	-55°C to +125°C	Package Dissipation	500mW
	HD-74C195	-40°C to +85°C	Lead Temperature (Soldering, 10 Sec.)	300°C
Storage Temperature		-65°C to +150°C	Operating V_{CC} Range	+3.0V to +15.0V

ELECTRICAL CHARACTERISTICS

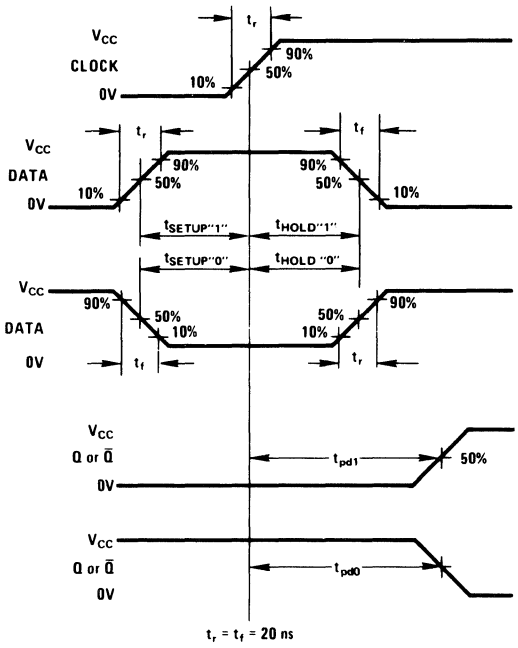
Min/Max limits apply across temperature range unless otherwise specified.
T_A = 25°C, C_L = 50pF, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5			V	V_{CC} = 5.0V
		8.0			V	V_{CC} = 10V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5	V	V_{CC} = 5.0V
				2.0	V	V_{CC} = 10V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5			V	V_{CC} = 5.0V, I_O = -10μA
		9.0			V	V_{CC} = 10V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5	V	V_{CC} = 5.0V, I_O = +10μA
				1.0	V	V_{CC} = 10.0V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V
Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V
Supply Current	I_{CC}		0.050	300	μA	V_{CC} = 15V
Input Capacitance	C_{IN}		5.0		pF	Any input
Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	t_{pd0} or t_{pd1}		200	300	ns	V_{CC} = 5.0V
			75	130	ns	V_{CC} = 10V
Propagation Delay Time to a Logical "0" from Clear			100	300	ns	V_{CC} = 5V
			50	130	ns	V_{CC} = 10V
Time Prior to Clock Pulse that Data must be Present	t_{setup}		60	100	ns	V_{CC} = 5V
			15	50	ns	V_{CC} = 10V
Time Prior to Clock Pulse that Shift/Load must be Present	t_{setup}		110	150	ns	V_{CC} = 5V
			60	90	ns	V_{CC} = 10V
Time after Clock Pulse that Data must be Held			-10	0	ns	V_{CC} = 5V
			-5	0	ns	V_{CC} = 10V
Minimum Clock Pulse Width	t_{WL} = t_{WH}		100	200	ns	V_{CC} = 5.0V
			50	100	ns	V_{CC} = 10V
Minimum Clear Pulse Width			90	130	ns	V_{CC} = 5.0V
			40	60	ns	V_{CC} = 10.0V
Maximum Clock Rise and Fall Time		5.0			μs	V_{CC} = 5.0V
		2.0			μs	V_{CC} = 10V
Maximum Input Clock Frequency		2.0	3.0		MHz	V_{CC} = 5.0V
		5.5	8.5		MHz	V_{CC} = 10V
LOW POWER TTL/CMOS INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} −1.5			V	54C, V_{CC} = 4.5V
						74C, V_{CC} = 4.75V
Logical "0" input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V
						74C, V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_D = - 360μA
						74C, V_{CC} = 4.75V, I_D = - 360μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.4	V	54C, V_{CC} = 4.5V, I_D = 360μA
						74C, V_{CC} = 4.75V, I_D = 360μA
Propagation Delay Time to A Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	t_{pd1} or t_{pd0}		250		ns	V_{CC} = 5.0V

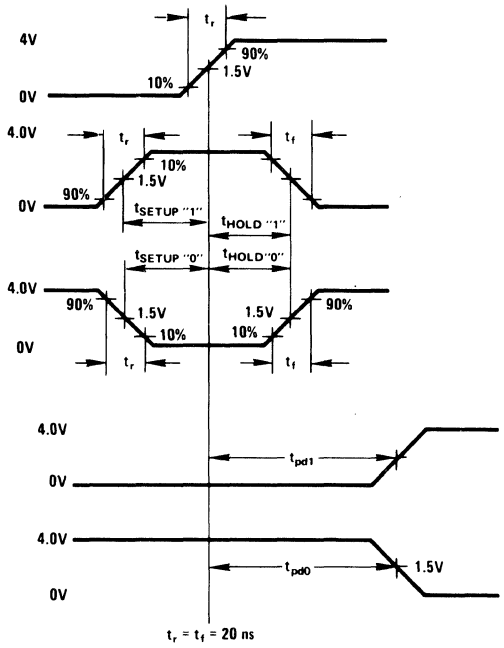
NOTE: These devices should not be connected under power on condition.

Waveforms

CMOS to CMOS

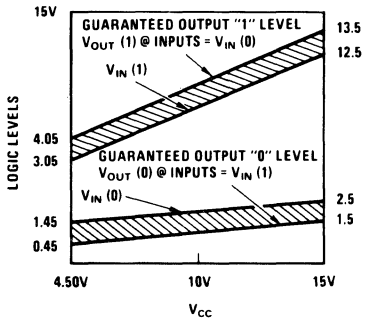


TTL to CMOS



Noise Margin

GUARANTEED NOISE MARGIN AS FUNCTION OF V_{CC}



HARRIS SEMICONDUCTOR
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Advanced Information

HD-54C200/HD-74C200

256-Bit Three-State Random Access Read/Write Memory

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- TTL COMPATIBILITY — FAN OUT OF 1 DRIVING STANDARD TTL
- LOW POWER — 500nW TYP.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package Code 1U and Code 9V.

Description

The HD-54C200/HD-74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a write enable line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of $\overline{CE}_3$ or $\overline{CE}_2$ inputs. The three state data output line working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs provides for easy memory expansion.

ADDRESS OPERATION: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$ or $\overline{CE}_2$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

READ OPERATION: The data is read out by selecting the proper address and bringing $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{CE}_3$ low and write enable high. Holding $\overline{CE}_1$ or $\overline{CE}_2$ at a high level forces the output into three state. When used in bus organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a three state control, provides for fast access times by not disabling the chip.

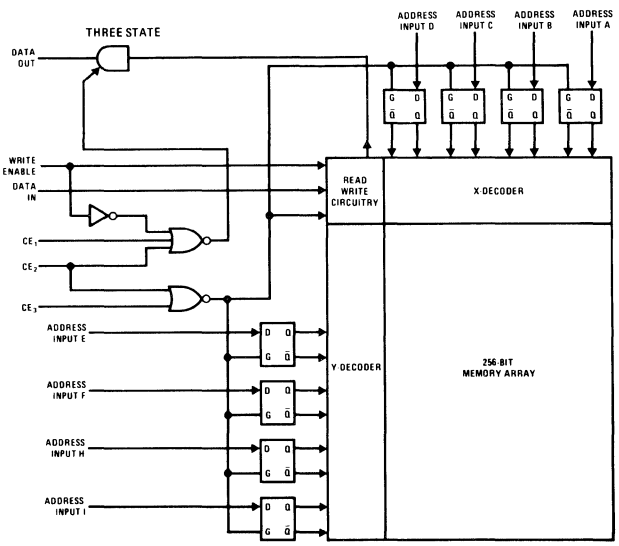
WRITE OPERATION: Data is written into the memory with $\overline{CE}_2$ and $\overline{CE}_3$ low and write enable low. The state of $\overline{CE}_1$ has no effect on the write cycle. The output assumes three state with write enable low.

Truth Table

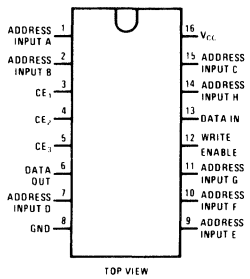
CE_1	CE_2	CE_3	$\overline{\text{WRITE ENABLE}}$	FUNCTIONAL CONDITION
X	0	0	0	Output in Three State Chip in Write Mode Address Held in Register
1	0	0	1	Output in Three State Address Held in Register
0	0	0	1	Chip in Read Mode Address Held in Register
X	1	X	X	Output in Three State Chip Disabled Address Registers will Accept Data
0	0	1	X	Output Assumes Previous Read or Write State Chip Internally Disabled Address Registers will Accept Data

X = Don't Care

Circuit Diagram



Connection Diagram



TOP VIEW

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin		-0.3V to V_{CC} + 0.3V	Package Dissipation	500mW
Operating Temperature Range	HD-54C200	-55°C to +125°C	Operating V_{CC} Range	-3.0V to 15.0V
	HD-74C200	-40°C to +85°C	Absolute Maximum V_{CC}	16.0V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

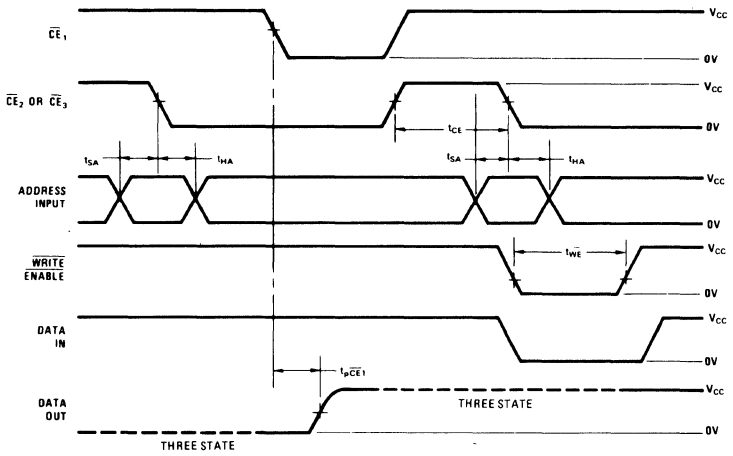
ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range, unless otherwise specified.
T_A = 25°C, C_L = 50 pF, Input rise and fall times = 20 ns unless otherwise specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Supply Current (I_{CC})	I_{CC}		0.10		μA	V_{CC} = 15V
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} −1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	54C, V_{CC} = 4.5V, I_O = -1.6mA 74C, V_{CC} = 4.75V, I_O = -1.6mA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4 0.4	V V	54C, V_{CC} = 4.5V, I_O = 1.6mA 74C, V_{CC} = 4.75V, I_O = 1.6mA
	OUTPUT DRIVE						
	Output source Current (P-Channel)	I_{Source}		-6.0		mA	V_{CC} = 5.0V, V_{Out} = 0V T_A = 25°C
	Output Source Current (P-Channel)	I_{Source}		-25		mA	V_{CC} = 10V, V_{Out} = 0V T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}		8.0		mA	V_{CC} = 5.0V, V_{Out} = V_{CC} T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}		30		mA	V_{CC} = 10V, V_{Out} = V_{CC} T_A = 25°C
A.C.	Access Time from Address	t_{ACC}		600 250		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay from $\overline{CE}_2$ or $\overline{CE}_3$	t_{pd}		550 230		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Propagation Delay from $\overline{CE}_1$	$t_{p\overline{CE}1}$		150 70		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Address Setup Time	t_{SA}		50 20		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Address Hold Time	t_{HA}		50 20		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width	$t_{\overline{WE}}$		170 80		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	$\overline{CE}_2$ or $\overline{CE}_3$ Pulse Widths	t_{CE}		250 100		ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Input Capacity	C_{IN}		5.0		pF	Any input (Note 2)
	Output Capacity in Three State	C_{Out}		9.0		pF	(Note 2)
	Power Dissipation Capacity	C_{pd}		300		pF	(Note 3)

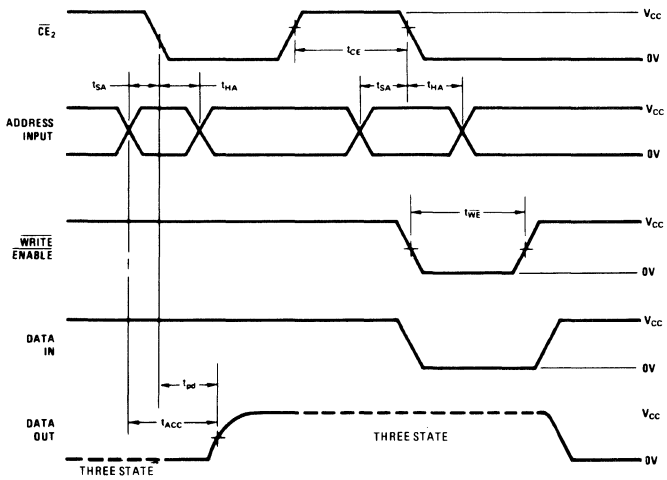
NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. C_{pd} determines the no load AC power consumption of any CMOS device.

Read and Write Cycles Using $\overline{CE}_1$ and $\overline{CE}_2$ (or $\overline{CE}_3$)



NOTE: USED FOR FAST ACCESS TIME IN BUSED SYSTEMS.

Read and Write Cycles Using $\overline{CE}_2$ ($\overline{CE}_1$ = $\overline{CE}_3$ = logic 0)



NOTE: IF $\overline{CE}_3$ IS USED IN PLACE OF $\overline{CE}_2$ THE OUTPUT WILL ASSUME PREVIOUS DATA RATHER THAN TRI-STATE.

HARRIS SEMICONDUCTOR
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HD-54C221/HD-74C221

Dual Monostable Multivibrator

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V to 15V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP
- LOW POWER T^2L COMPATIBLE — DRIVE 2 LT^2L LOAD

Description

The HD54C221/HD74C221 dual monostable multivibrators is monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input, and a clear input.

Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT}. The pulse width is stable over a wide range of temperature and V_{CC}. Pulse stability will be limited by the accuracy of external timing components. The R_{EXT} ranges from 10k to 100k. Throughout these ranges the pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT} R_{EXT}$.

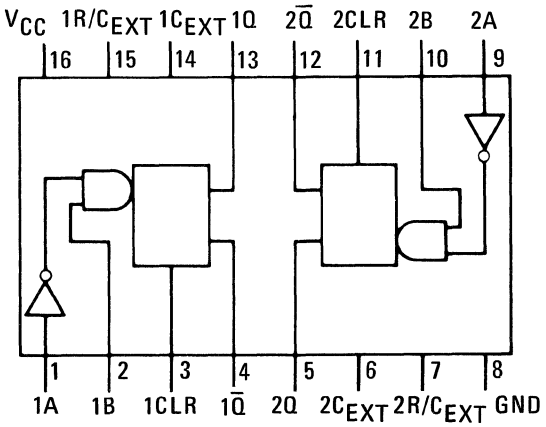
Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Connection Diagram

DUAL-IN-LINE PACKAGE



Truth Table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔

H = High Level

L = Low Level

↑ = Transition from Low to High

↓ = Transition from High to Low

⊓ = One High Level Pulse

⊔ = One Low Level Pulse

X = Irrelevant

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at any Pin		-0.3V to V_{CC} +0.3V	Package Dissipation	500mW
Operating Temperature Range	HD-54C221	-55°C to +125°C	Operating V_{CC} Range	4.5V to 15V
	HD-74C221	-40°C to +85°C	Absolute Maximum V_{CC}	16V
Storage Temperature Range		-65°C to +150°C	Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range, unless otherwise noted.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10 A V_{CC} = 10V, I_O = -10 A
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10 A V_{CC} = 10V, I_O = +10 A
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	A	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		A	V_{CC} = 15V, V_{IN} = 0V
				0.05	300	A	V_{CC} = 15V, $R_{Ext.}$ = Q1, Q2 = Logic 0 (Note 3)
	Supply Current	I_{CC}		15		mA	V_{CC} = 15V, Q1 = Logic 1 Q2 = Logic 0
				2			V_{CC} = 5.0V, Q1 = Logic 1 Q2 = Logic 0
	CMOS/LPTTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC}- 1.5			V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	54C, V_{CC} = 4.5V, I_O = -360 A 74C, V_{CC} = 4.75V, I_O = -360 A
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4 0.4	V V	54C, V_{CC} = 4.5V, I_O = 360 A 74C, V_{CC} = 4.75V, I_O = 360 A
	OUTPUT DRIVE						
	Output Source Current (P-Channel)	I_{Source}	-1.75	3.3		mA	V_{CC} = 5.0V, V_{Out} = 0V T_A = 25°C
	Output Source Current (P-Channel)	I_{Source}	-8.0	-15		mA	V_{CC} = 10V, V_{Out} = 0V T_A = 25°C
	Output Sink Current (N-Channel)	I_{Sink}	1.75	3.6		mA	V_{CC} = 5.0V, V_{Out} = V_{CC} T_A = 25°C
	Output Sink Current	I_{Sink}	8.0	16		mA	V_{CC} = 10V, V_{Out} = V_{CC} T_A = 25°C

Specifications

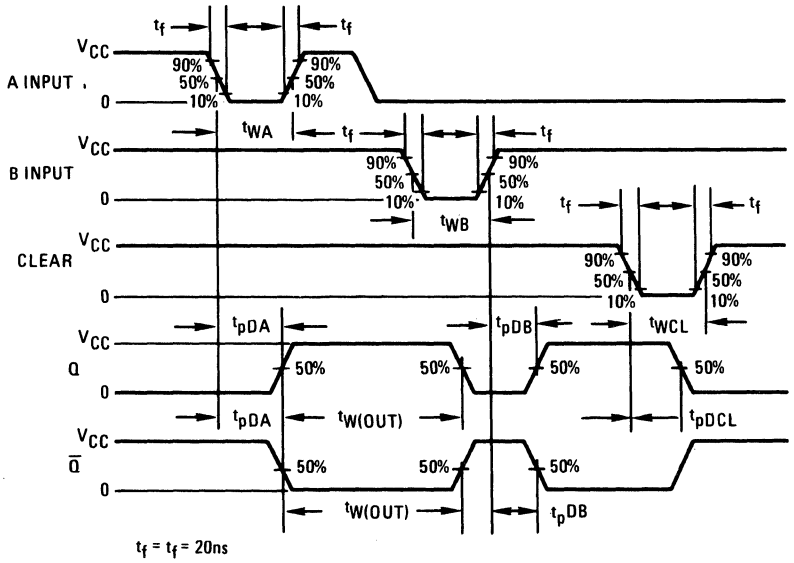
ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $C_L = 50pF$, Unless Otherwise Specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
A.C.	Propagation Delay From Trigger Input (A,B) to Output Q, $\overline{Q}$	$t_{PD\ A,B}$		250	500	ns	V_{CC} = 5.0V
				120	250	ns	V_{CC} = 10V
	Propagation Delay from Clear Input (CL) to Output Q, $\overline{Q}$	$t_{DP\ CL}$		250	500	ns	V_{CC} = 5.0V
				120	250	ns	V_{CC} = 10V
	Minimum Trigger Input (A,B) Pulse Width	$t_{w(A,B)}$	150	65		ns	V_{CC} = 5.0V
			70	30		ns	V_{CC} = 10V
	Minimum Clear Input (CL) Pulse Width	$t_{w(CL)}$	150	65		ns	V_{CC} = 5.0V
			70	30		ns	V_{CC} = 10V
	Q or $\overline{Q}$ Output Pulse Width	$t_{w(Out)}$	250			ns	V_{CC} = 5.0V, R = 10K
			250			ns	V_{CC} = 10V, C = 0pF
			250			ns	V_{CC} = 15V
			9.3		12.3	s	V_{CC} = 5.0V, R = 10K
			9		11	s	V_{CC} = 10V, C = 1000pF
			8.5		10.5	s	V_{CC} = 15V
			900		1200	s	V_{CC} = 5.0V, R = 10K
			900		1100	s	V_{CC} = 10V, C = 0.1 F
			900		1100	s	V_{CC} = 15V
	Output Duty Cycle				90	%	R = 10K, C = 1000pF
					95	%	R = 10K, C = 0.1 F
	Input Capacitance	C_{IN}		25		pF	R/C_{Ext} Input
				5		pF	Any Other Input

NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. In standby (Q = Logic 0) the power dissipated equals the leakage current plus V_{CC}/R_{Ext}.

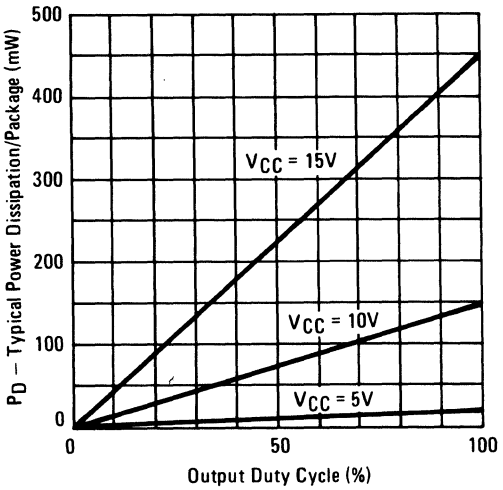
Switching Time Waveforms



$t_f = t_f = 20ns$

Typical Characteristics

TYPICAL POWER DISSIPATION PER PACKAGE



NOTE: Power shown is measured with both one shots switching together and R_{EXT} = 100K.

HARRIS SEMICONDUCTOR
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HD-54C901/HD-74C901 *Hex Inverting TTL Buffer*
HD-54C902/HD-74C902 *Hex Non-Inverting TTL Buffer*
HD-54C903/HD-74C903 *Hex Inverting PMOS Buffer*
HD-54C904/HD-74C904 *Hex Non-Inverting PROS Buffer*

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V TO 15.0V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} TYP.
- TTL COMPATIBILITY — FAN OUT OF 2 DRIVING STANDARD TTL

Description

These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply.

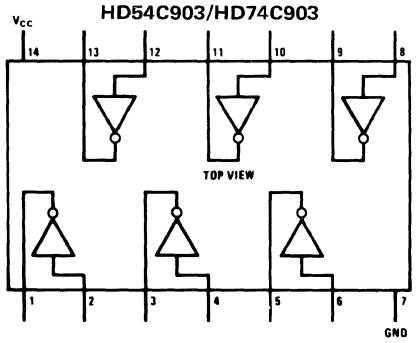
Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

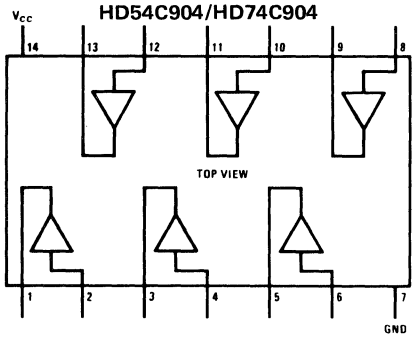
See package outline Code 1U and Code 9V.

Connection Diagrams

HD54C901/HD74C901
HD54C903/HD74C903

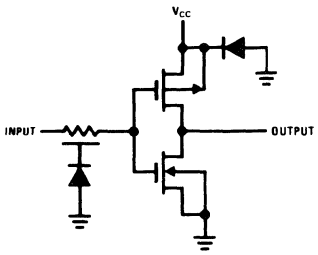


HD54C902/HD74C902
HD54C904/HD74C904

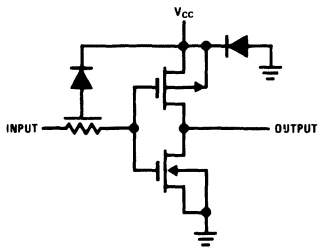


Circuit Diagrams

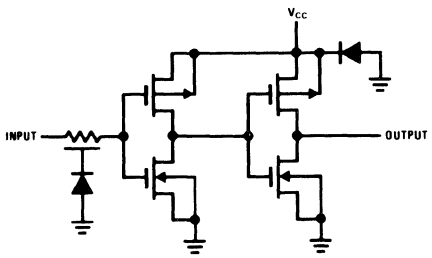
HD54C901/HD74C901
CMOS to TTL Inverting Buffer



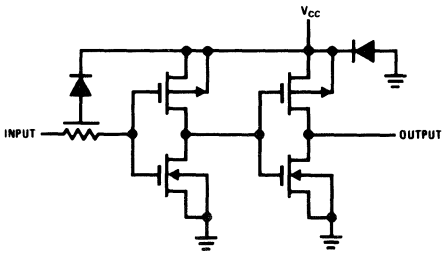
HD54C903/HD74C903
PMOS to TTL or CMOS Inverting Buffer



HD54C902/HD74C902
CMOS to TTL Buffer



HD54C904/HD74C904
PMOS to TTL or CMOS Buffer



Specifications

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage at Any Output Pin		-0.3V to V_{CC} +0.3V
Voltage at Any Input Pin	HD-54C901/HD-74C901	-0.3V to +15.0V
	HD-54C902/HD-74C902	-0.3V to +15.0V
	HD-54C903/HD-74C903	V_{CC} -17.0V to V_{CC} +0.3V
	HD-54C904/HD-74C904	V_{CC} -17.0V to V_{CC} +0.3V
Operating Temperature Range	HD-54C901, HD-54C902, HD-54C903, HD-54C904	-55°C to +125°C
	HD-74C901, HD-74C902, HD-74C903, HD-74C904	-40°C to +85°C
Storage Temperature Range		-65°C to +150°C
Package Dissipation		500mW
Operating V_{CC} Range		3.0V to 15.0V
Absolute Maximum V_{CC}		16.0V
Lead Temperature (Soldering, 10 Sec.)		300°C

ELECTRICAL CHARACTERISTICS

Min/Max limits apply across temperature range, unless otherwise noted.

DC

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	3.5			V	V_{CC} = 5.0V
		8.0			V	V_{CC} = 10V
Logical "0" Input Voltage	$V_{IN(0)}$			1.5	V	V_{CC} = 5.0V
				2.0	V	V_{CC} = 10V
Logical "1" Output Voltage	$V_{Out(1)}$	4.5			V	V_{CC} = 5.0V, I_O = -10μA
		9.0			V	V_{CC} = 10V, I_O = -10μA
Logical "0" Output Voltage	$V_{Out(0)}$			0.5	V	V_{CC} = 5.0V, I_O = +10μA
				1.0	V	V_{CC} = 10V, I_O = +10μA
Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
Logical "0" Input Current	$I_{IN(0)}$	-1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
Supply Current	I_{CC}		0.05	15	μA	V_{CC} = 15V
TTL TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} −1.5			V	54C, V_{CC} = 4.5V
					V	74C, V_{CC} = 4.75V
Logical "0" Input Voltage	$V_{IN(0)}$			0.8	V	54C, V_{CC} = 4.5V
				0.8	V	74C, V_{CC} = 4.75V
CMOS TO TTL						
Logical "1" Input Voltage						
HD-54C901/HD-54C903	$V_{IN(1)}$	4.0			V	V_{CC} = 4.5V
HD-54C902, HD-54C904		V_{CC}-1.5			V	V_{CC} = 4.5V
HD-74C901, HD-74C903		4.25			V	V_{CC} = 4.75
HD-74C902, HD-74C904		V_{CC}-1.5			V	V_{CC} = 4.75
Logical "0" Input Voltage						
HD-54C901, HD-54C903	$V_{IN(0)}$			1.0	V	V_{CC} = 4.5V
HD-54C902, HD-54C904				1.5	V	V_{CC} = 4.5V
HD-74C901, HD-74C903				1.0	V	V_{CC} = 4.75V
HD-74C902, HD-74C904				1.5	V	V_{CC} = 4.75V
Logical "1" Output Voltage	$V_{Out(1)}$	2.4			V	54C, V_{CC} = 4.5V, I_O = -800μA
		2.4			V	74C, V_{CC} = 4.75V, I_O = -800μA
Logical "0" Output Voltage						
HD-54C901, HD-54C903	$V_{Out(0)}$			0.4	V	V_{CC} = 4.5V, I_O = 2.6mA
HD-54C902, HD-54C904				0.4	V	V_{CC} = 4.5V, I_O = 3.2mA
HD-74C901, HD-74C903				0.4	V	V_{CC} = 4.75V, I_O = 2.6mA
HD-74C902, HD-74C904				0.4	V	V_{CC} = 4.75V, I_O = 3.2mA

Specifications (continued)

ELECTRICAL CHARACTERISTICS

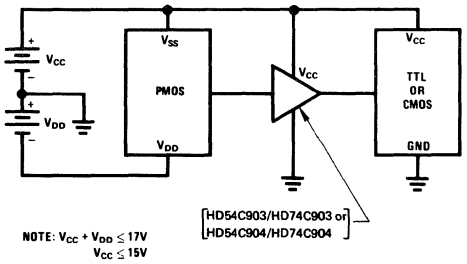
$T_A = 25^oC$, $C_L = 50pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	OUTPUT DRIVE (HD-54C901/HD-74C901, HD-54C903 /HD-74C903)						
	Output Source Current (P-Channel)	I_{Source}	5.0			mA	$V_{CC} = 5.0V$, $V_{Out} = 0V$ $T_A = 25^oC$, $V_{IN} = 0V$
	Output Source Current (P-Channel)	I_{Source}	20			mA	$V_{CC} = 10V$, $V_{Out} = 0V$ $T_A = 25^oC$, $V_{IN} = 0V$
	Output Sink Current (N-Channel)	I_{Sink}	11			mA	$V_{CC} = 5.0V$, $V_{Out} = V_{CC}$ $T_A = 25^oC$, $V_{IN} = V_{CC}$
	Output Sink Current (N-Channel)	I_{Sink}	3.8			mA	$V_{CC} = 5.0V$, $V_{Out} = 0.4V$ $T_A = 25^oC$, $V_{IN} = V_{CC}$
	OUTPUT DRIVE HD-54C902/HD-74C902, HD-54C904/HD-74C904						
	Output Source Current (P-Channel)	I_{Source}	5.0			mA	$V_{CC} = 5.0V$, $V_{Out} = 0V$ $T_A = 25^oC$, $V_{IN} = V_{CC}$
	Output Source Current (P-Channel)	I_{Source}	20			mA	$V_{CC} = 10V$, $V_{Out} = 0V$ $T_A = 25^oC$, $V_{IN} = V_{CC}$
	Output Sink Current (N-Channel)	I_{Sink}	11			mA	$V_{CC} = 5.0V$, $V_{Out} = V_{CC}$ $T_A = 25^oC$, $V_{IN} = 0V$
	Output Sink Current (N-Channel)	I_{Sink}	3.8			mA	$V_{CC} = 5.0V$, $V_{Out} = 0.4V$ $T_A = 25^oC$, $V_{IN} = 0V$
A.C.	HD-54C901/HD-74C901 HD-54C903/HD-74C903						
	Input Capacitance	C_{IN}		14		pF	Any input (Note 2)
	Power Dissipation Capacity	C_{pd}		30		pF	(Note 3) Per Buffer
	Propagation Delay Time to a Logical "1"	$t_{pd(1)}$		38 22	70 30	ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Propagation Delay Time to a Logical "0"	$t_{pd(0)}$		21 13	35 20	ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	HD-54C902/HD-74C902 HD-54C904/HD-74C904						
	Input Capacitance	C_{IN}		5.0		pF	Any input (Note 2)
	Power Dissipation Capacity	C_{pd}		50		pF	(Note 3) Per Buffer
	Propagation Delay Time to a Logical "1"	$t_{pd(1)}$		57 27	90 40	ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$
	Propagation Delay Time to a Logical "0"	$t_{pd(0)}$		54 25	90 40	ns ns	$V_{CC} = 5.0V$ $V_{CC} = 10V$

NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. C_{pd} determines the no load AC power consumption of any CMOS device.

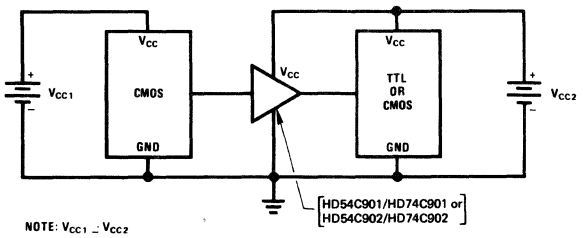
Typical Applications

PMOSto CMOS or TTL Interface



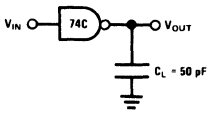
NOTE: $V_{CC} + V_{DD} \leq 17V$
$V_{CC} \leq 15V$

CMOS to TTL or CMOS at a Lower V_{CC}



NOTE: $V_{CC1} = V_{CC2}$

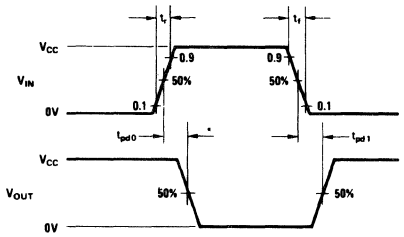
AC Test Circuit



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

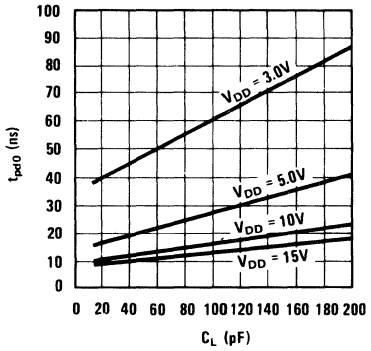
Waveforms

CMOS to CMOS

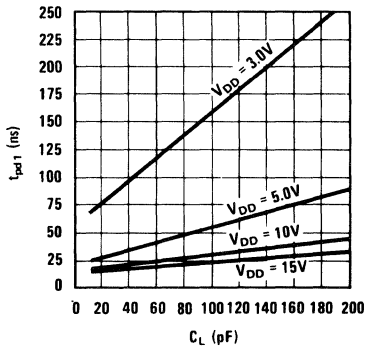


Typical Characteristics

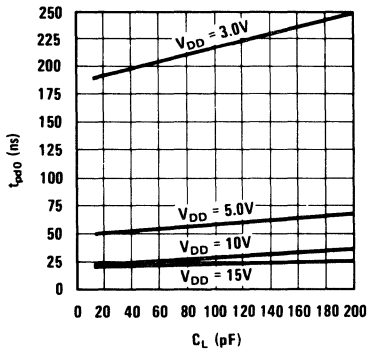
Typical Propagation Delay to a Logical "O" for the HD-54C901/ HD-74C901 and HD-54C903/ HD-74C903



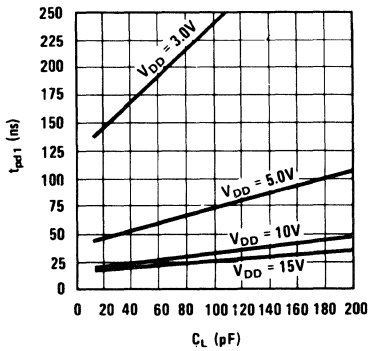
Typical Propagation Delay to a Logical "1" for the HD-54C901/ HD-74C901 and HD-54C903/ HD-74C903



Typical Propagation Delay to a Logical "O" for the HD-54C902/ HD-74C902 and HD-54C904/ HD-74C904



Typical Propagation Delay to a Logical "1" for the HD-54C902/ HD-74C902 and HD-54C904/ HD-74C904



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-70C95/HD-80C95
HD-70C97/HD-80C97

Three-State Hex Non-Inverting Buffer

Features

- WIDE SUPPLY VOLTAGE RANGE — 3.0V to 15V
- GUARANTEED NOISE MARGIN — 1.0V
- HIGH NOISE IMMUNITY — 0.45 V_{CC} (TYP)
- TTL COMPATIBLE — DRIVE 1 TTL LOAD

Description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P- channel enhancement mode transistors. Each of the devices are used to convert CMOS or TTL outputs to three-state outputs with no logic inversion. The HD-70C95/HD-80C95 has common three-state controls for all six buffers. The HD-70C97/HD-80C97 has two three-state controls, one for two buffers and one for the other four.

Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Truth Tables

HD-70C95/HD-80C95

DISABLE INPUT		INPUT	OUTPUT
DIS_1	DIS_2		
0	0	0	0
0	0	1	1
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

HD-70C97/HD-80C97

DISABLE INPUT		INPUT	OUTPUT
DIS_4	DIS_2		
0	0	0	0
0	0	1	1
X	1	X	Hi-Z*
1	X	X	Hi-Z**

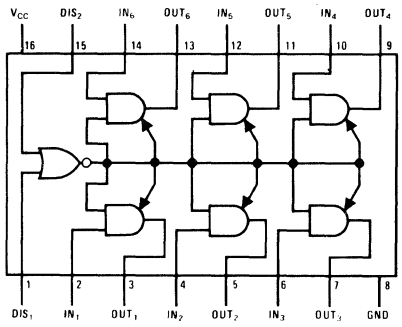
*Output 5-6 only
**Output 1-4 only
X - Irrelevant

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

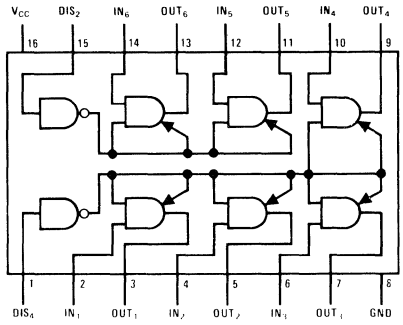
See package outline Code 1W and Code 9L.

Connection Diagrams



TOP VIEW

HD-70C95/HD-80C95



TOP VIEW

HD-70C97/HD-80C97

Specifications

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage at Any Pin	0.3V to V_{CC} +0.3V	Storage Temperature Range	-65°C to +150°C
Operating Temperature Range		Package Dissipation	500mW
HD-70C95, HD-70C97	-55°C to +125°C	Power Supply Voltage, V_{CC}	16V
HD-80C95, HD-80C97	-40°C to +85°C	Lead Temperature (Soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS

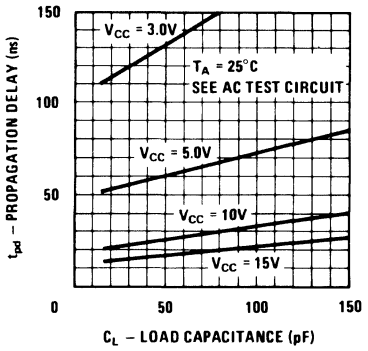
Min/max limits apply across temperature range unless otherwise specified.
T_A = 25°C, C_L = 50 pF, Input rise and fall times = 20 ns unless otherwise specified.

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
D.C.	CMOS TO CMOS						
	Logical "1" Input Voltage	$V_{IN(1)}$	3.5 8.0			V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "0" Input Voltage	$V_{IN(0)}$			1.5 2.0	V V	V_{CC} = 5.0V V_{CC} = 10V
	Logical "1" Output Voltage	$V_{Out(1)}$	4.5 9.0			V V	V_{CC} = 5.0V, I_O = -10μA V_{CC} = 10V, I_O = -10μA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.5 1.0	V V	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA
	Logical "1" Input Current	$I_{IN(1)}$		0.005	1.0	μA	V_{CC} = 15V, V_{IN} = 15V
	Logical "0" Input Current	$I_{IN(0)}$	1.0	-0.005		μA	V_{CC} = 15V, V_{IN} = 0V
	Output Current in High Impedance State			0.005 -0.005	1.0	μA μA	V_{CC} = 15V, V_O = 15V V_{CC} = 15V, V_O = 0V
	Supply Current	I_{CC}		0.01	15	μA	V_{CC} = 15V
	TTL INTERFACE						
	Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} —1.5			V	70C, V_{CC} = 4.5V 80C, V_{CC} = 4.75V
	Logical "0" Input Voltage	$V_{IN(0)}$			0.8 0.8	V V	70C, V_{CC} = 4.5V 80C, V_{CC} = 4.75V
	Logical "1" Output Voltage	$V_{Out(1)}$	2.4 2.4			V V	70C, V_{CC} = 4.5V, I_O = -1.6mA 80C, V_{CC} = 4.75, I_O = -1.6mA
	Logical "0" Output Voltage	$V_{Out(0)}$			0.4 0.4	V V	70C, V_{CC} = 4.5V, I_O = 1.6mA 80C, V_{CC} = 4.75, I_O = 1.6mA
	OUTPUT DRIVE CURRENT						
	Output Source Current	I_{Source}	4.35			mA	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{Out} = 0V
	Output Source Current	I_{Source}	20			mA	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{Out}= 0V
	Output Sink Current	I_{Sink}	4.35			mA	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{Out} = V_{CC}
	Output Sink Current	I_{Sink}	20			mA	V_{CC} = 10V, V_{IN} = 0V T_A = 25°C, V_{Out} = V_{CC}
A.C.	Input Capacitance	C_{IN}		5.0		pF	Any input (Note 2)
	Output Capacitance Three State	C_{Out}		9.0		pF	Any Output (Note 2)
	Power Dissipation Capacity	C_{pd}		60		pF	(Note 3)
	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output	t_{pd0} or t_{pd1}		60 25	100 40	ns ns	V_{CC} = 5.0V V_{CC} = 10V
	Delay from Disable Input to High Impedance State(from Logical "1" or Logical "0" Level)—70C95/80C95	t_{IH}, t_{OH}		80 50	135 90	ns ns	V_{CC} = 5.0V, C_L = 5.0pF, R_L = 10K V_{CC} = 10V, C_L = 5.0pF, R_L = 10K
	Delay from Disable Input to Logical "1" Level or to Logical "0" Level(from High Impedance State 70C95/80C95	t_{HI} or t_{HO}		120 50	200 90	ns ns	V_{CC} = 5.0V, C_L = 50pF, R_L = 10K V_{CC} = 10V, C_L = 50pF, R_L = 10K
	Delay from Disable Input to High Impedance State (from Logical "1" or Logical "0" Level)—70C97/80C97	t_{IH}, t_{OH}		70 50	125 90	ns ns	V_{CC} = 5.0V, R_L = 10K V_{CC} = 10V, R_L = 10K
	Delay from Disable Input to Logical "1" Level or to Logical "0" Level (from High Impedance State) 70C97/80C97	t_{HI}, t_{HO}		95 40	175 80	ns ns	V_{CC} = 5.0V, R_L = 10K V_{CC} = 10V, R_L = 10K
	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output	t_{pd0} or t_{pd1}		85 40	160 80	ns ns	V_{CC} = 5.0V, C_L = 150pF V_{CC} = 10V, C_L = 150pF

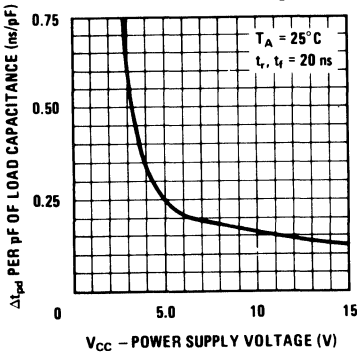
NOTES: 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Capacitance is guaranteed by periodic testing.
3. C_{PD} determines the no load AC power consumption of any CMOS device.

Typical Characteristics

Propagation Delay vs.
Load Capacitance

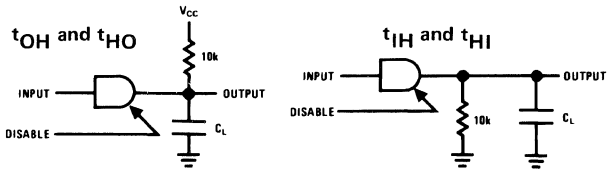


Δt_{pd}/pF vs.
Power Supply Voltage

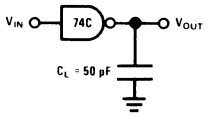


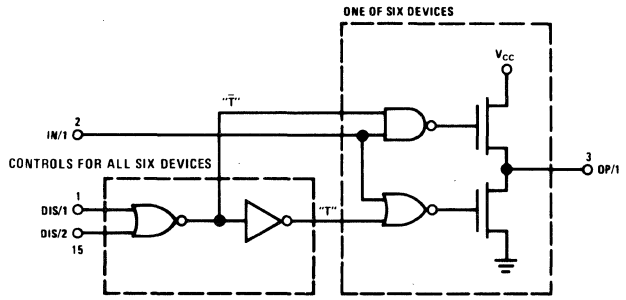
AC Test Circuits

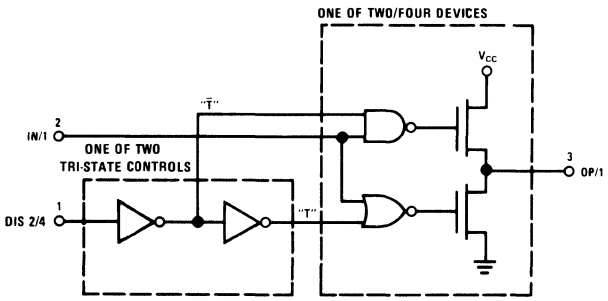
HD-70C95/HD-80C95 THREE–STATE



HD-70C97/HD-80C97

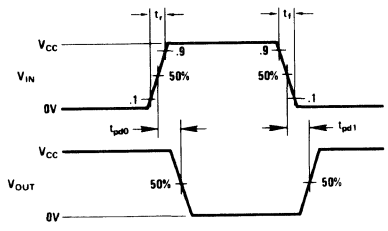




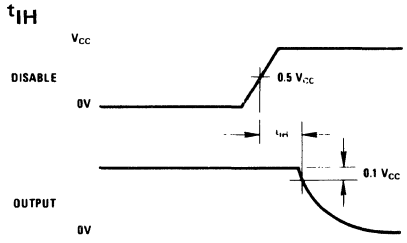


Waveforms

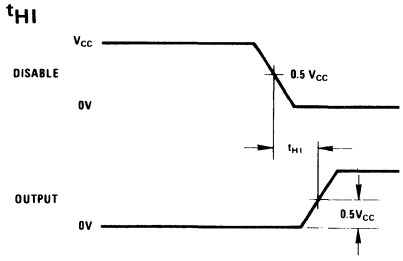
CMOS to CMOS



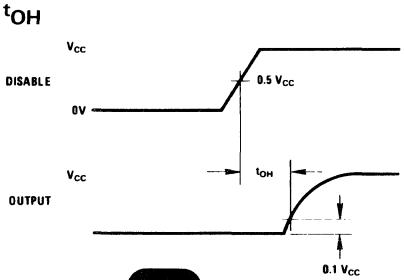
t_{IH}



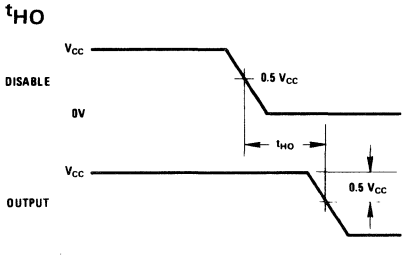
t_{HI}



t_{OH}



t_{HO}



HD-4000A Series

4

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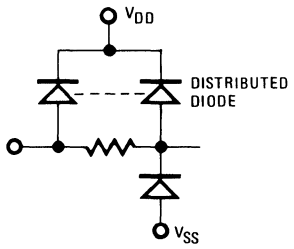
HD-4000A Series

These circuits employ complementary MOS (CMOS) to achieve low power dissipation, high noise immunity and wide power supply voltage ranges with symmetric rise and fall times. Features such as these make the 4000 series ideal for use in digital design systems. A popular feature of the 4000 series is this logic family's wide range of logic functions and readily abundant supply.

Family Features

- Wide Supply Voltage Range — 3.0V to 15V
- High Noise Immunity — 0.45 V_{CC} Typ.
- Low Power — 10nW Typ. for Gates
10 µW Typ. for MSI Circuits
- Supply Voltage Compatibility with Both DTL and T^2L
- All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND unless otherwise noted.



HARRIS SEMICONDUCTOR
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HD-4000A

Dual 3-Input "NOR" Gate Plus Inverter

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- SINGLE POWER SUPPLY OPERATION
- EFFECTIVE STATIC CHARGE PROTECTION

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

HD-4000 is a small scale CMOS integrated circuit providing the system designer with basic gate building blocks for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power consumption, high noise immunity, nearly symmetric output rise and fall times and wide power supply operating range.

Truth Table

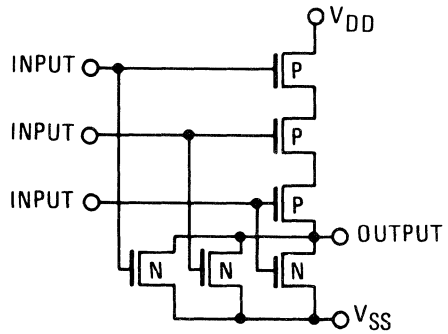
INPUTS			OUTPUT
0	0	0	1
1	X	X	0
X	1	X	0
X	X	1	0

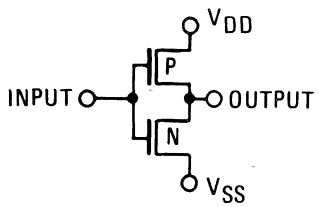
LOGIC "1" → V_{DD}

LOGIC "0" → V_{SS}

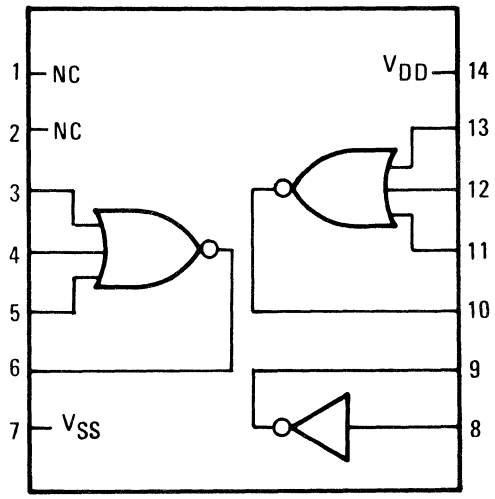
X = DON'T CARE

Circuit Diagram





Connection Diagrams



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		$-65^{o}C$ to $+150^{o}C$
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4000A-2	$-55^{o}C$ to $+125^{o}C$
	HD-4000A-9	$-40^{o}C$ to $+85^{o}C$

ELECTRICAL CHARACTERISTICS (STATIC)

				HD-4000A-2										CONDITIONS	
				-55°C			+25°C			+125°C					
	PARAMETER	SYM.		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}						10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}						10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}		1.5			1.5	2.25		1.4			V	5	$V_{OH} \geq 3.6$VDC
				3.0			3.0	4.5		2.9			V	10	$V_{OH} \geq 7.2$VDC
		V_{NH}		1.4			1.5	2.25		1.5			V	5	$V_{OL} \leq .95$VDC
				2.9			3.0	4.5		3.0			V	10	$V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}				.01		0	.01			.05	V	5	$V_{IH} = V_{DD}$
						.01		0	.01			.05	V	10	$I_O = 0A$
		V_{OH}		4.99			4.99	5		4.95			V	5	$V_{IL} = V_{SS}$
				9.99			9.99	10		9.95			V	10	$I_O = 0A$
	Quiescent Power Supply Current	I_{DD}				.05		.001	.05			3	μA	5	
						.10		.001	.10			6	μA	10	
	Output Drive Current	I_{OL}		0.5			.4	1		.28			mA	5	$V_{OL} = .4$VDC
				1.1			.9	2.5		.65			mA	10	$V_{OL} = .5$VDC
		I_{OH}		-.62			-.5	-2		-.35			mA	5	$V_{OH} = 2.5$VDC
				-.62			-.5	-1		-.35			mA	10	$V_{OH} = 9.5$VDC
	Input Capacitance							5					pF		

				HD-4000A-9										CONDITIONS	
				-40°C			+25°C			+85°C					
	PARAMETER	SYM.		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}						10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}						10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}		1.5			1.5	2.25		1.4			V	5	$V_{OH} \geq 3.6$VDC
				3.0			3.0	4.5		2.9			V	10	$V_{OH} \geq 7.2$VDC
		V_{NH}		1.4			1.5	2.25		1.5			V	5	$V_{OL} \leq .95$VDC
				2.9			3.0	4.5		3.0			V	10	$V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}				.01		0	.01			.05	V	5	$V_{IH} = V_{DD}$
						.01		0	.01			.05	V	10	$I_O = 0A$
		V_{OH}		4.99			4.99	5		4.95			V	5	$V_{IL} = V_{SS}$
				9.99			9.99	10		9.95			V	10	$I_O = 0A$
	Quiescent Power Supply Current	I_{DD}				0.5		.005	0.5			15	μA	5	
						5		.005	5			30	μA	10	
	Output Drive Current	I_{OL}		.35			.3	1		.24			mA	5	$V_{OL} = .4$VDC
				.72			.6	2.5		.48			mA	10	$V_{OL} = .5$VDC
		I_{OH}		-.35			-.3	-2		-.24			mA	5	$V_{OH} = 2.5$VDC
				-.3			-.25	-1		-.2			mA	10	$V_{OH} = 9.5$VDC
	Input Capacitance							5					pF		

Specifications (continued)

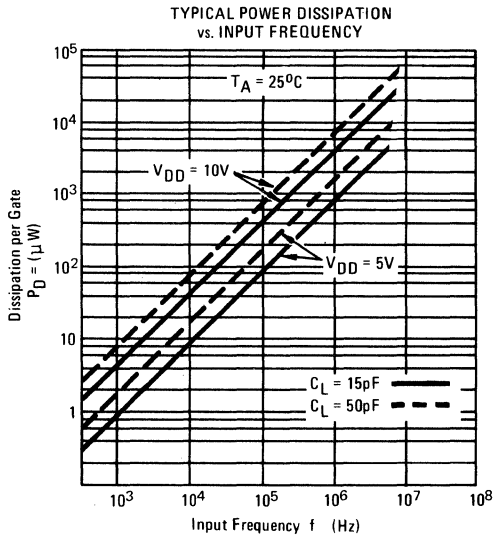
ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

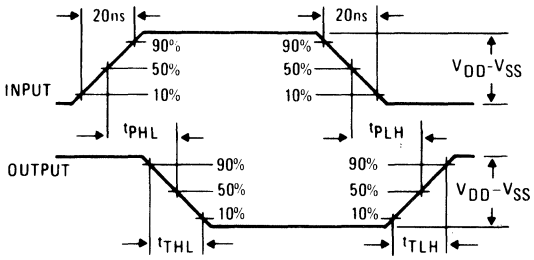
	PARAMETER	SYMBOL	HD-4000A-2 TYP.	HD-4000A-2 MAX.	HD-4000A-9 TYP.	HD-4000A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay	t_{PLH}	35 25	95 45	35 25	120 65	ns ns	5 10	Ref. to Switching Time Definitions $T_A = 25^oC$
		t_{PHL}	35 25	50 40	35 25	80 55	ns ns	5 10	
	Transition Time	t_{TLH}	65 35	175 75	65 35	300 125	ns ns	5 10	
		t_{THL}	65 35	125 70	65 35	200 115	ns ns	5 10	

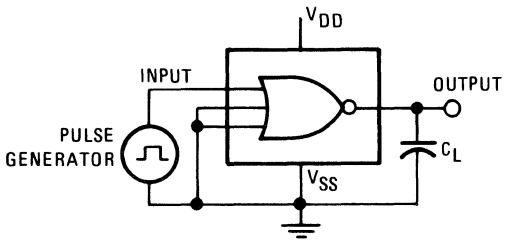
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

Typical Characteristics



Switching Time Definition and Conditions





HD-4001A

Quad 2-Input "NOR" Gate

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- SINGLE POWER SUPPLY OPERATION
- EFFECTIVE STATIC CHARGE PROTECTION

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

HD-4001 is a small scale CMOS integrated circuit providing the system designer with basic gate building blocks for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power consumption, high noise immunity, nearly symmetric output rise and fall times and wide power supply operating range.

Truth Table

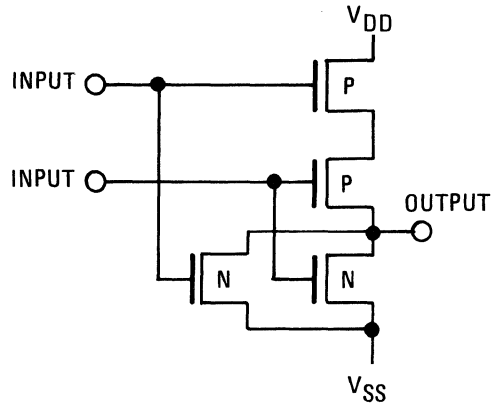
INPUT		OUTPUT
0	0	1
1	X	0
X	1	0

LOGIC "1" → V_{DD}

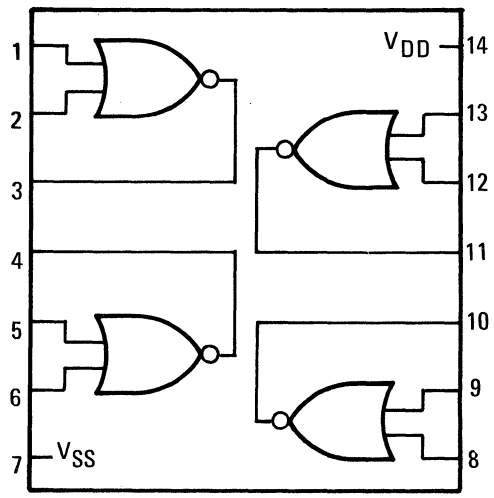
LOGIC "0" → V_{SS}

X = DON'T CARE

Circuit Diagram



Connection Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} -V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4001A-2	-55°C to +125°C
	HD-4001A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4001A-2											
			-55°C			+25°C			+125°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			.05 .10		.001 .001	.05 .10			3 6	μA μA	5 10	
	Output Drive Current	I_{OL}	0.5 1.1			.4 .9	1 2.5		.28 .65			mA mA	5 10	$V_{OL} = .4$VDC $V_{OL} = .5$VDC
		I_{OH}	-.62 -.62			-.5 -.5	-2 -1		-.35 -.35			mA mA	5 10	$V_{OH} = 2.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

			HD-4001A-9											
			-40°C			+25°C			+85°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			0.5 5		.005 .005	0.5 5			15 30	μA μA	5 10	
	Output Drive Current	I_{OL}	.35 .72			.3 .6	1 2.5		.24 .48			mA mA	5 10	$V_{OL} = .4$VDC $V_{OL} = .5$VDC
		I_{OH}	-.35 -.3			-.3 -.25	-2 -1		-.24 -.2			mA mA	5 10	$V_{OH} = 2.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

Specifications (continued)

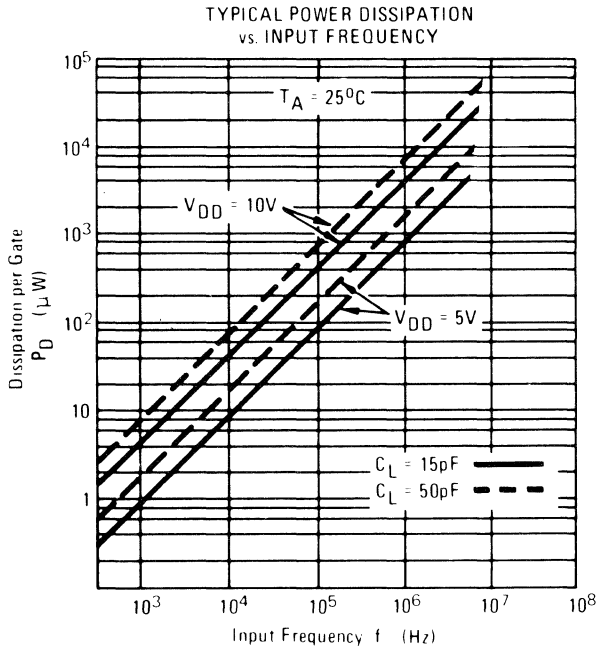
ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

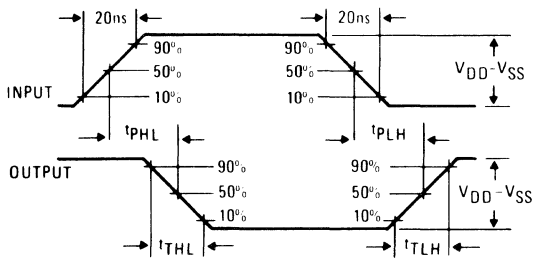
	PARAMETER	SYMBOL	HD-4001A-2 TYP.	HD-4001A-2 MAX.	HD-4001A-9 TYP.	HD-4001A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay	t_{PLH}	35 25	95 45	35 25	120 65	ns ns	5 10	Ref. to Switching Time Definitions $T_A = 25^oC$
		t_{PHL}	35 25	50 40	35 25	80 55	ns ns	5 10	
	Transition Time	t_{TLH}	65 35	175 75	65 35	300 125	ns ns	5 10	
		t_{THL}	65 35	125 70	65 35	200 115	ns ns	5 10	

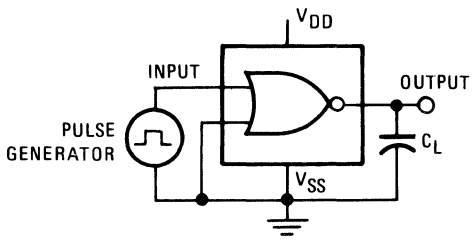
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

Typical Characteristics



Switching Time Definitions and Conditions





HARRIS SEMICONDUCTOR
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HD-4002A

Dual 4-Input "NOR" Gate

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- SINGLE POWER SUPPLY OPERATION
- EFFECTIVE STATIC CHARGE PROTECTION

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

HD-4002 is a small scale CMOS integrated circuit providing the system designer with basic gate building blocks for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power consumption, high noise immunity, nearly symmetric output rise and fall times and wide power supply operating range.

Truth Table

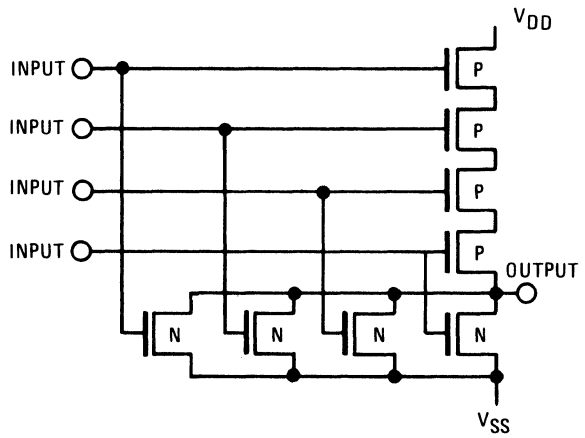
INPUTS	OUTPUT
0 0 0 0	1
X X X 1	0
X X 1 X	0
X 1 X X	0
1 X X X	0

LOGIC "1" → V_{DD}

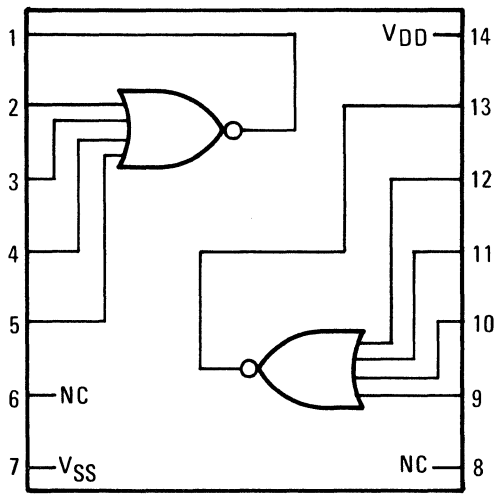
LOGIC "0" → V_{SS}

X = DON'T CARE

Circuit Diagram



Connection Diagram



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4002A-2	-55°C to +125°C
	HD-4002A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4002A-2											
			-55°C			+25°C			+125°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			.05 .10		.001 .001	.05 .10			3 6	μA μA	5 10	
	Output Drive Current	I_{OL}	0.5 1.1			.4 .9	1 2.5		.28 .65			mA mA	5 10	$V_{OL} = .4$VDC $V_{OL} = .5$VDC
		I_{OH}	-.62 -.62			-.5 -.5	-2 -1		-.35 -.35			mA mA	5 10	$V_{OH} = 2.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

			HD-4002A-9											
			-40°C			+25°C			+85°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			0.5 5		.005 .005	0.5 5			15 30	μA μA	5 10	
	Output Drive Current	I_{OL}	.35 .72			.3 .6	1 2.5		.24 .48			mA mA	5 10	$V_{OL} = .4$VDC $V_{OL} = .5$VDC
		I_{OH}	-.35 -.3			-.3 -.25	-2 -1		-.24 -.2			mA mA	5 10	$V_{OH} = 2.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

Specifications (continued)

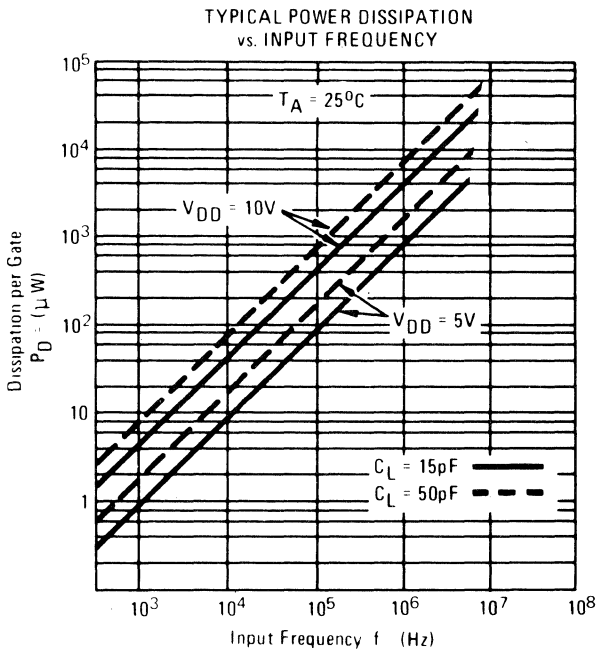
ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

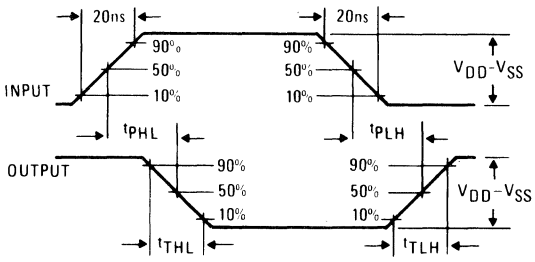
	PARAMETER	SYMBOL	HD-4002A-2 TYP.	HD-4002A-2 MAX.	HD-4002A-9 TYP.	HD-4002A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay	t_{PLH}	35 25	95 45	35 25	120 65	ns ns	5 10	Ref. to Switching Time Definitions $T_A = 25^oC$
		t_{PHL}	35 25	50 40	35 25	80 55	ns ns	5 10	
	Transition Time	t_{TLH}	65 35	175 75	65 35	300 125	ns ns	5 10	
		t_{THL}	65 35	125 70	65 35	200 115	ns ns	5 10	

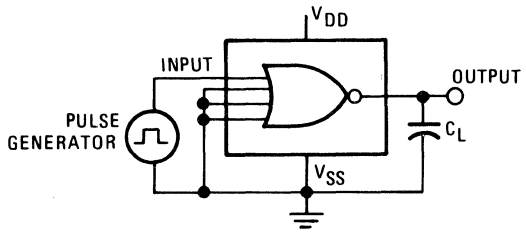
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

Typical Characteristics



Switching Time Definitions and Conditions





HD-4007A

Dual Complementary Pair Plus Inverter

Features

- POWER SUPPLY OPERATING RANGE +3VDC to +15VDC.
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE.
- SINGLE POWER SUPPLY OPERATION.
- EFFECTIVE STATIC CHARGE PROTECTION.

Package

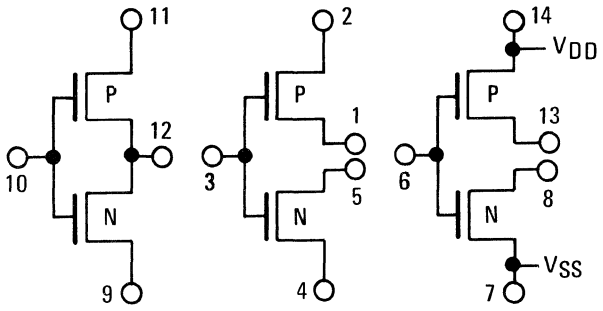
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

The HD-4007 is a special purpose CMOS integrated circuit. Source and drain terminals for two P-channel and two N-channel transistors are independently available at pins providing flexibility to configure several digital logic or linear MOS transistor functions.

Circuit Diagram



NOTE:
V_{DD} must be the most positive potential.
V_{SS} must be the most negative potential.

Functional Diagrams

FUNCTIONS	CONNECTIONS
Triple Inverters	14 - 2 - 11 8 - 13 1 - 5 7 - 4 - 9
3-Input NAND	1 - 12 - 13 4 - 8 5 - 9 2 - 14 - 11
3-Input NOR	13 - 2 1 - 11 12 - 5 - 8 7 - 4 - 9
Dual Bi-Directional Transmission Gate	1 - 5 - 12 2 - 9 11 - 4 8 - 10 - 13 3 - 6
Functional Logic	2 - 14 1 - 11 5 - 12 - 13 4 - 8 - 9 2 - 11 - 13 1 - 8 - 12 5 - 9 4 - 7
High Sink Current Driver	6 - 3 - 10 11 - 14 7 - 4 - 9 8 - 5 - 12
High Source Current Driver	6 - 3 - 10 14 - 2 - 11 7 - 9 13 - 1 - 12

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4007A-2	-55°C to +125°C
	HD-4007A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4007A-2											
			-55°C			+25°C			+125°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			.05 .10		.001 .001	.05 .1			3 6	μA μA	5 10	
	Output Drive Current	I_{OL}	.75 1.6			.6 1.3	1 2.5		.4 .95			mA mA	5 10	$V_{OL} = .4$VDC $V_{OL} = .5$VDC
		I_{OH}	-1.75 -1.35			-1.4 -1.1	-4 -2.5		-1 -.75			mA mA	5 10	$V_{OH} = 2.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

			HD-4007A-9											
			-40°C			+25°C			+85°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			.5 1		.005 .005	.5 1			15 30	μA μA	5 10	
	Output Drive Current	I_{OL}	.35 1.2			.3 1	1 2.5		.24 .8			mA mA	5 10	$V_{OL} = .4$VDC $V_{OL} = .5$VDC
		I_{OH}	-1.3 -.65			-1.1 -.55	-4 -2.5		-.9 -.45			mA mA	5 10	$V_{OH} = 2.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

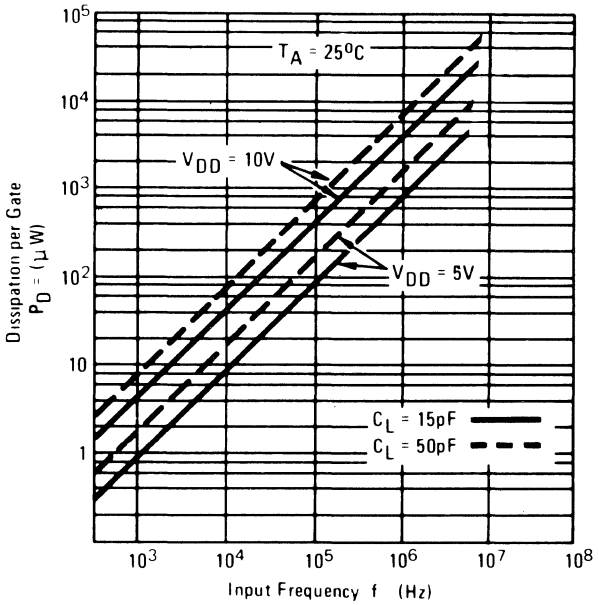
$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	HD-4007A-2 TYP.	HD-4007A-2 MAX.	HD-4007A-9 TYP.	HD-4007A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay	t_{PLH}	35 20	60 40	35 20	75 50	ns ns	5 10	Ref. to Switching Time Definitions $T_A = 25^oC$
		t_{PHL}	35 20	60 40	35 20	75 50	ns ns	5 10	
	Transition Time	t_{TLH}	50 30	75 40	50 30	100 50	ns ns	5 10	
		t_{THL}	50 30	75 40	50 30	100 50	ns ns	5 10	

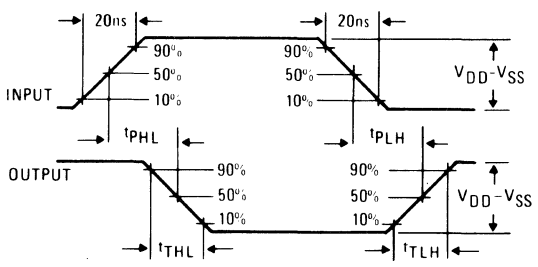
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

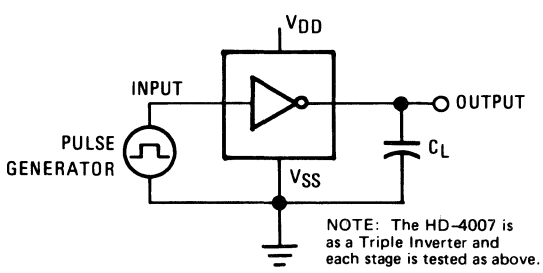
Typical Characteristics

TYPICAL POWER DISSIPATION vs. INPUT FREQUENCY



Switching Time Definitions and Conditions





NOTE: The HD-4007 is as a Triple Inverter and each stage is tested as above.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-4011A

Quad 2-Input "NAND" Gate

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- SINGLE POWER SUPPLY OPERATION
- EFFECTIVE STATIC CHARGE PROTECTION

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

HD-4011 is a small scale CMOS integrated circuit providing the system designer with basic gate building blocks for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power consumption, high noise immunity, nearly symmetric output rise and fall times and wide power supply operating range.

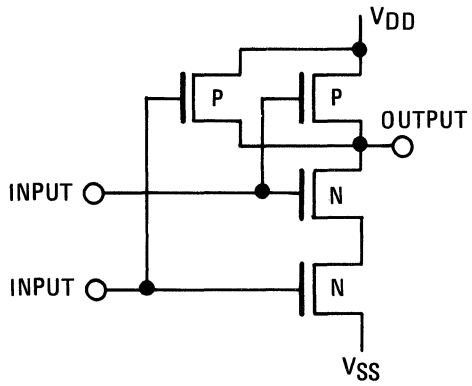
Truth Table

INPUT	OUTPUT
0 0	1
0 1	1
1 0	1
1 1	0

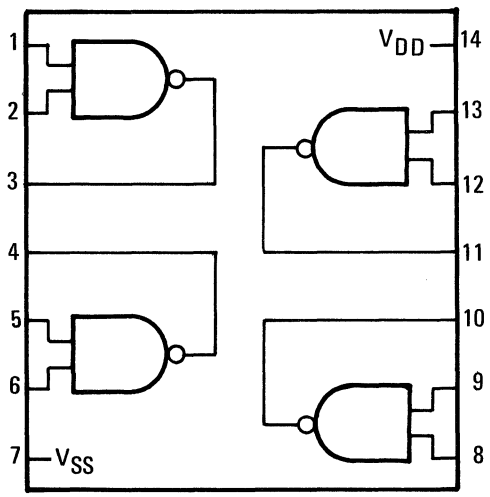
LOGIC "1" → V_{DD}

LOGIC "0" → V_{SS}

Circuit Diagram



Connection Diagram



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		$-65^{o}C$ to $+150^{o}C$
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4011A-2	$-55^{o}C$ to $+125^{o}C$
	HD-4011A-9	$-40^{o}C$ to $+85^{o}C$

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4011A-2											
			-55°C			+25°C			+125°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			.05 .10		.001 .001	.05 .10			3 6	μA μA	5 10	
	Output Drive Current	I_{OL}	.31 .62			.25 .5	.5 .6		.175 .35			mA mA	5 10	$V_{OL} = .5$VDC $V_{OL} = .5$VDC
		I_{OH}	-.31 -.75			-.25 -.6	-.5 -1.2		-.175 -.4			mA mA	5 10	$V_{OH} = 4.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

			HD-4011A-9											
			-40°C			+25°C			+85°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}					.005 .005	.5 5			15 30	μA μA	5 10	
	Output Drive Current	I_{OL}	.145 .3			.12 .25	.5 .6		.095 .2			mA mA	5 10	$V_{OL} = .5$VDC $V_{OL} = .5$VDC
		I_{OH}	-.145 -.35			-.12 -.3	-.5 -1.2		-.095 -.24			mA mA	5 10	$V_{OH} = 4.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

Specifications (continued)

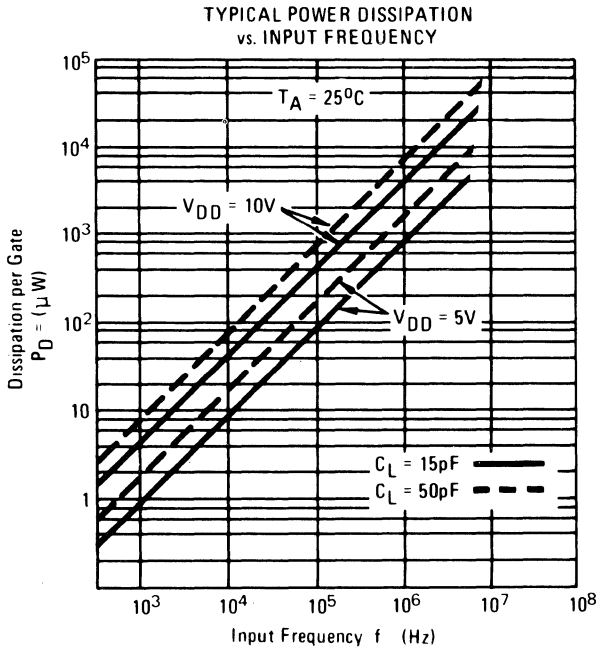
ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

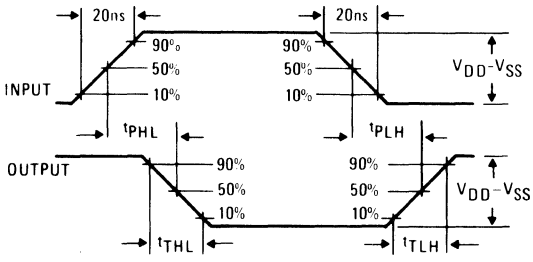
PARAMETER	SYMBOL	HD-4011A-2 TYP.	HD-4011A-2 MAX.	HD-4011A-9 TYP.	HD-4011A-9 MAX.	UNITS	V_{DD}	NOTES
Propagation Delay	t_{PLH}	50	75	50	100	ns	5	Ref. to Switching Time Definitions $T_A = 25^oC$
		25	40	25	50	ns	10	
	t_{PHL}	50	75	50	100	ns	5	
		25	40	25	50	ns	10	
Transition Time	t_{TLH}	75	100	75	125	ns	5	
		40	60	40	75	ns	10	
	t_{THL}	75	125	75	150	ns	5	
		50	75	50	100	ns	10	

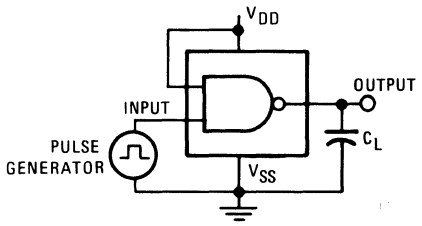
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

Typical Characteristics



Switching Time Definitions and Conditions





HD-4012A

Dual 4-Input "NAND" Gate

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- SINGLE POWER SUPPLY OPERATION
- EFFECTIVE STATIC CHARGE PROTECTION

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

HD-4012 is a small scale CMOS integrated circuit providing the system designer with basic gate building blocks for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power consumption, high noise immunity, nearly symmetric output rise and fall times and wide power supply operating voltage range.

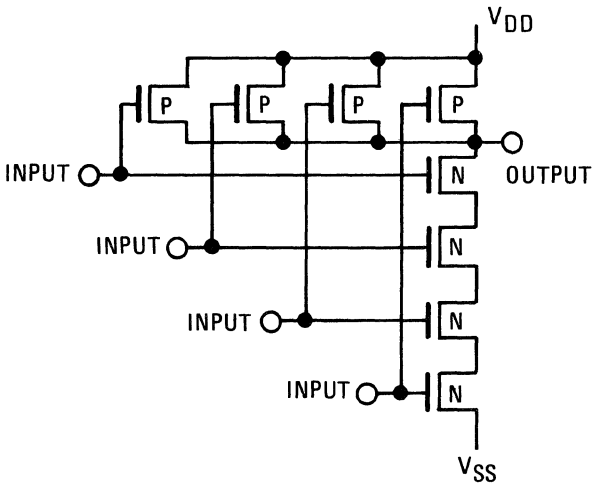
Truth Table

INPUT	OUTPUT
0 X X X	1
X 0 X X	1
X X 0 X	1
X X X 0	1
1 1 1 1	0

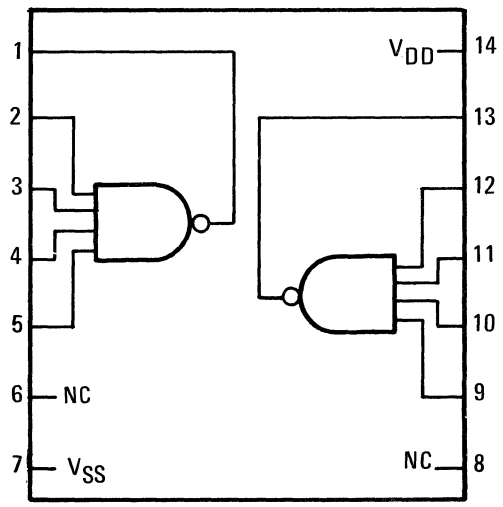
LOGIC "1" → V_{DD}
LOGIC "0" → V_{SS}

X = DON'T CARE

Circuit Diagram



Connection Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0,3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4012A-2	-55°C to +125°C
	HD-4012A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4012A-2											
			-55°C			+25°C			125°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			.05 .10		.001 .001	.05 .1			3 6	μA μA	5 10	
	Output Drive Current	I_{OL}	.15 .31			.12 .25	.25 .6		.085 .175			mA mA	5 10	$V_{OL} = .5$VDC $V_{OL} = .5$VDC
		I_{OH}	-.31 -.75			-.25 -.6	-.5 -1.2		-.175 -.4			mA mA	5 10	$V_{OH} = 4.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

			HD-4012-9											
			-40°C			+25°C			+85°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			.5 5		.005 .005	.5 5			15 30	μA μA	5 10	
	Output Drive Current	I_{OL}	.072 .155			.06 .13	.25 .6		.05 .105			mA mA	5 10	$V_{OL} = .5$VDC $V_{OL} = .5$VDC
		I_{OH}	-.145 -.35			-.12 -.3	-.5 -1.2		-.095 -.24			mA mA	5 10	$V_{OH} = 4.5$VDC $V_{OH} = 9.5$VDC
	Input Capacitance						5					pF		

Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

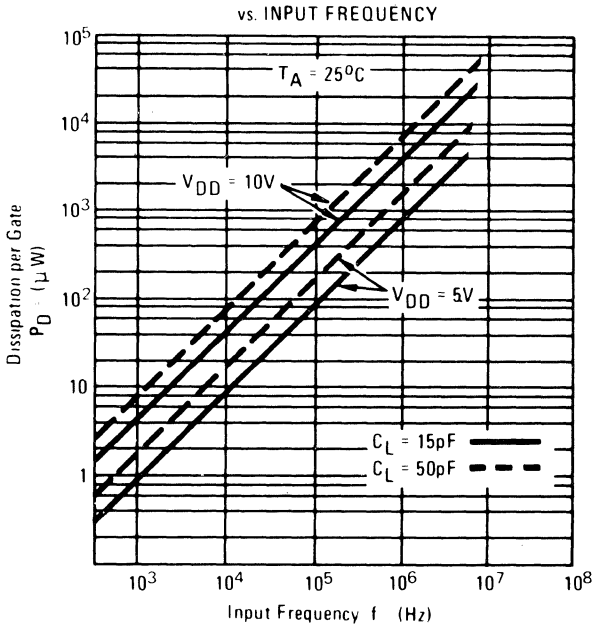
$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	HD-4012A-2 TYP.	HD-4012A-2 MAX.	HD-4012-9 TYP.	HD-4012-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay	t_{PLH}	50 25	75 40	50 25	100 50	ns ns	5 10	Ref. to Switching Time Definitions $T_A = 25^oC$
		t_{PHL}	100 50	150 75	100 50	200 100	ns ns	5 10	
	Transition Time	t_{TLH}	75 40	100 60	75 40	125 75	ns ns	5 10	
		t_{THL}	250 125	375 200	250 125	500 250	ns ns	5 10	

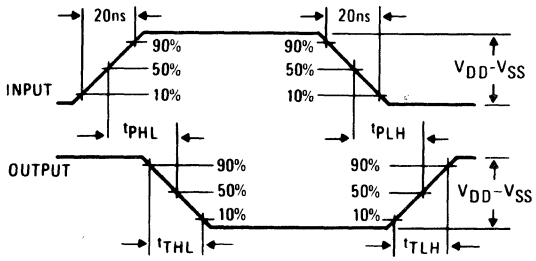
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

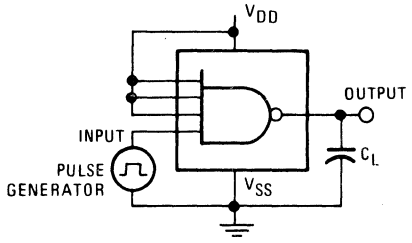
Typical Characteristics

TYPICAL POWER DISSIPATION vs. INPUT FREQUENCY



Switching Time Definitions and Conditions





HARRIS SEMICONDUCTOR
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HD-4013A

Dual "D" Flip-Flop

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- SINGLE POWER SUPPLY OPERATION
- EFFECTIVE STATIC CHARGE PROTECTION

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

The HD-4013 is a small scale CMOS integrated circuit providing the system designer with basic gate building blocks for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power consumption, high noise immunity, nearly symmetric output rise and fall times and wide power supply operating voltage range.

Truth Table

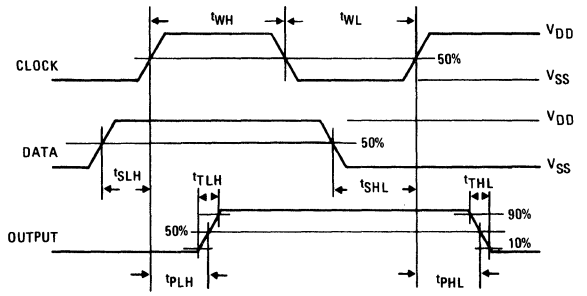
TRUTH TABLE

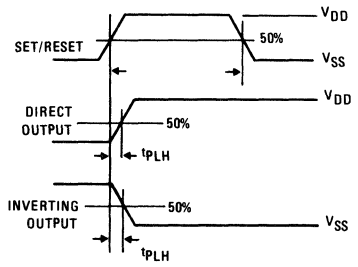
CL▲	D	R	S	Q	$\bar{Q}$
⌐⌐	0	0	0	0	1
⌐⌐	1	0	0	1	0
⌐_	X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

NO CHANGE

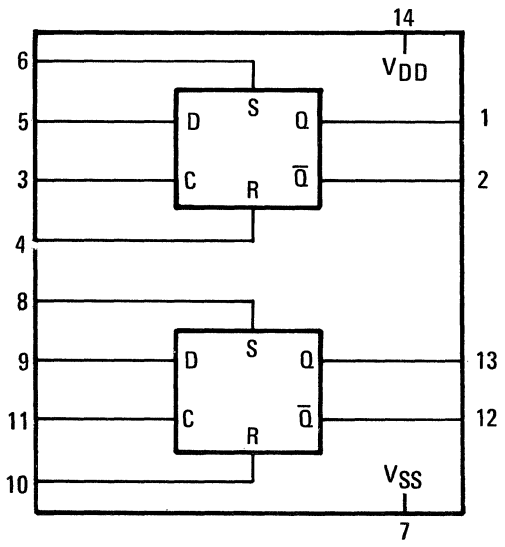
▲ LEVEL
X DON'T CARE CASE
** FF1/FF2 TERMINAL ASSIGNMENTS

Timing Diagram





Connection Diagram



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4013A-2	-55°C to +125°C
	HD-4013A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4013A-2											
			-55°C			+25°C			+125°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq$ 0.8VDC $V_{OH} \geq$ 1.0VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq$ 4.2VDC $V_{OL} \leq$ 9.0VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$I_{OL} = 0$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$I_{OH} = 0$
	Quiescent Power Supply Current	I_{DD}			1.0 2.0		.005 .005	1.0 2.0			60 120	μA μA	5 10	S = R = C = D = V_{SS}
	Output Drive Current	I_{OL}	.65 1.25			0.5 1	1 2.5		.35 .75			mA mA	5 10	V_{OL} = 5VDC V_{OL} = .5VDC
		I_{OH}	-.31 -.8			-.25 -.65	-.5 -1.3		-.175 -.45			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
	Input Capacitance						5					pF		

			HD-4013A-9											
			-40°C			+25°C			+85°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq$ .8VDC $V_{OH} \geq$ 1.0VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq$ 4.2VDC $V_{OL} \leq$ 9.0VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$I_{OL} = 0$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$I_{OL} = 0$
	Quiescent Power Supply Current	I_{DD}			10 20		.01 .02	10 20			140 280	μA μA	5 10	S = R = C = D = V_{SS}
	Output Drive Current	I_{OL}	.35 .72			.3 .6	1 2.5		.24 .5			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
		I_{OH}	-.17 -.4			-.14 -.33	-.5 -1.3		-.12 -.27			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
	Input Capacitance						5					pF		

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns otherwise specified.

	PARAMETER	SYMBOL	HD-4013A-2 MIN.	HD-4013A-2 TYP.	HD-4013A-2 MAX.	HD-4013A-9 MIN.	HD-4013A-9 TYP.	HD-4013A-9 MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
A.C.	Propagation Delay Clock to Q	$t_{PLH} = t_{PHL}$		150 75	300 110		150 75	350 125	ns ns	5 10	$S = R = V_{SS}$
	Transition Time	$t_{TLH} = t_{THL}$		75 50	125 70		75 50	150 75	ns ns	5 10	
	Minimum Clock Pulse Width	$t_{WL} = t_{WH}$		125 50	200 80		125 50	500 100	ns ns	5 10	
	Clock Rise, Fall Time	$t_{rCL} = t_{fCL}$			15 5			15 5	μs μs	5 10	
	Set Up Time	$t_{SLH} = t_{SHL}$		20 10	40 20		20 10	50 25	ns ns	5 10	
	Maximum Clock Frequency	f_{CL}	2.5 7	4 10		1 5	4 10		MHz MHz	5 10	
	Propagation Delay Set, Reset	$t_{PHL} = t_{PLH}$		175 75	300 110		175 75	350 125	ns ns	5 10	$D = C = V_{SS}$
	Minimum Set, Reset Pulse Width	$t_{WH(S)} = t_{WH(R)}$		125 50	250 100		125 50	500 125	ns ns	5 10	

NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

HD-4014A

8-Stage Static Shift Register

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- MSI COMPLEXITY – EIGHT SHIFT REGISTER STAGES WITH PARALLEL/SERIAL INPUT CONTROL AND BUFFERING ON BOTH INPUTS AND OUTPUTS.
- FULLY STATIC OPERATION
- CLOCK RATE 5MHz (TYP.) V_{DD}-V_{SS} = 10V

Description

The HD-4014 is an 8 stage shift register with parallel or serial data input and serial data output capabilities.

The state of the parallel/serial input determines the data entry mode. With a high on the parallel/serial control, input data is loaded from the parallel inputs synchronous with the positive going clock input. A low on the parallel/serial input enables serial data entry synchronous with the positive going clock.

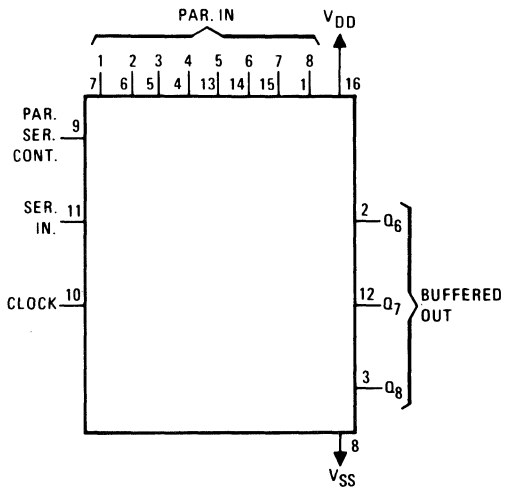
Parallel operation of two or more HD-4014's allows bit expansion beyond eight bits.

Truth Table

C_L▲	SER. IN	PAR. SER. CONTROL	PI-1	PI-n	Q_1 (INTERNAL)	Q_n	
⎍	X	1	0	0	0	0	
⎍	X	1	1	0	1	0	
⎍	X	1	0	1	0	1	
⎍	X	1	1	1	1	1	
⎍	0	0	X	X	0	Q_{n-1}	
⎍	1	0	X	X	1	Q_{n-1}	
⎎	X	X	X	X	Q_1	Q_n	(NO CHANGE)

X = DON'T CARE CASE ▲= LEVEL CHANGE

Connection Diagram

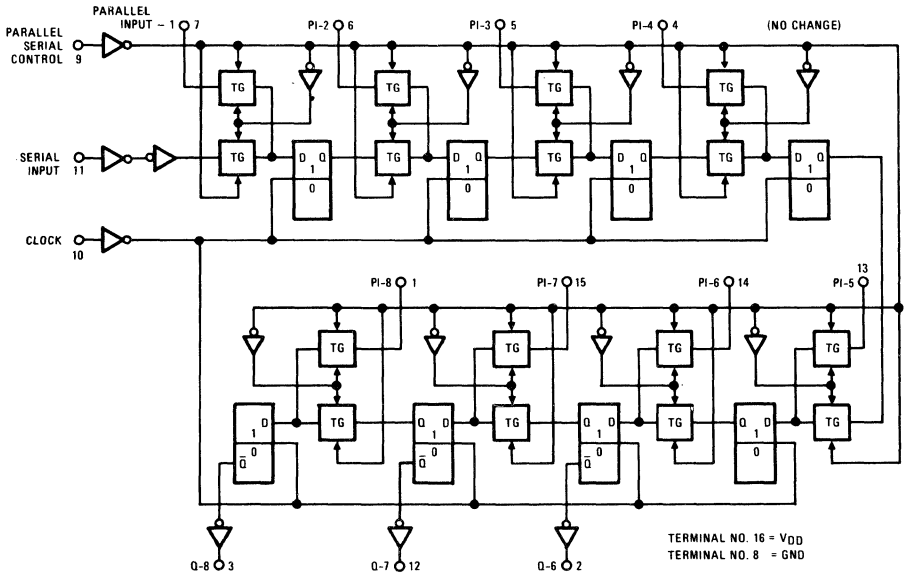


Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Logic Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD}-V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4014A-2	-55°C to +125°C
	HD-4014A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4014A-2										CONDITIONS	
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage						10					pA		
D.C.	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
	N-Channel Output Drive Current	I_{DN}	0.15 0.31			0.12 0.25	0.3 0.5		0.085 0.175			mA mA	5 10	V_O = 0.5 V_O = 0.5
	P-Channel	I_{DP}	-0.1 -0.25			-0.08 -0.20	-0.16 -0.44		-0.055 -0.14			mA mA	5 10	V_O = 4.5 V_O = 9.5
	Quiescent Device Current	I_L			5 10		0.5 1	5 10			300 600	µA µA	5 10	
	Quiescent Device Dissipation/Package	P_D			25 100		2.5 10	25 100			1500 6000	µW µW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

			HD-4014A-9										CONDITIONS	
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		
D.C.	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
	N-Channel Output Drive Current	I_{DN}	0.072 0.12			0.06 0.1	0.3 0.5		0.05 0.08			mA mA	5 10	V_O = 0.5 V_O = 0.5
	P-Channel	I_{DP}	-0.06 -0.12			-0.05 -0.1	-0.16 -0.44		-0.04 -0.08			mA mA	5 10	V_O = 4.5 V_O = 9.5
	Quiescent Drive Current	I_L			50 100		0.5 1	50 100			700 1400	µA µA	5 10	
	Quiescent Device Dissipation/Package	P_D			250 1000		2.5 10	250 1000			3500 14000	µW µW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

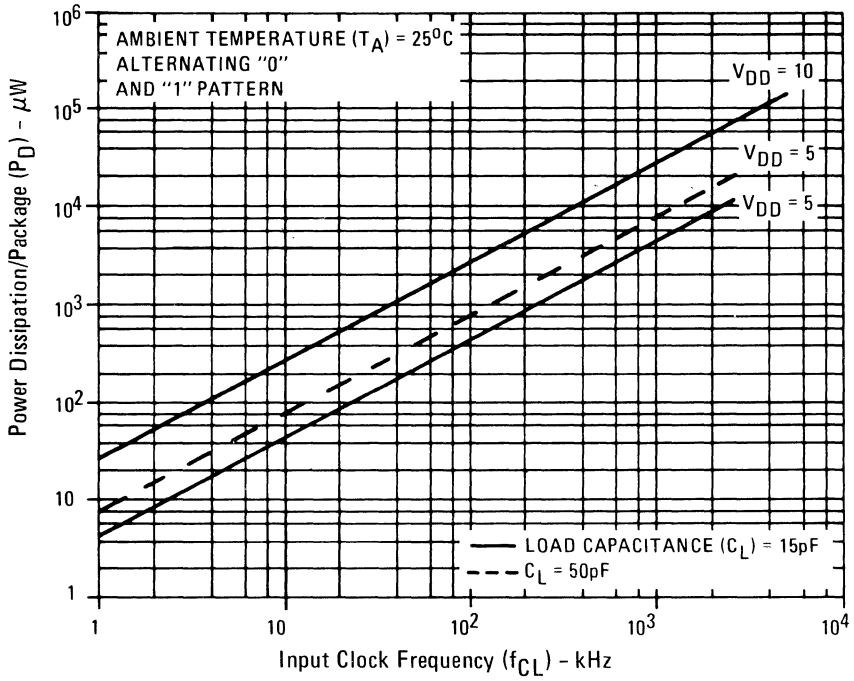
Specifications

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	HD-4014A-2			HD-4014A-9			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		V_{DD}	NOTES
Propagation Delay Time	$t_{PHL}=t_{PLH}$		300 100	750 225		300 100	1000 300	ns ns	5 10	
Transition Time	$t_{THL}=t_{TLH}$		150 75	300 125		150 75	400 150	ns ns	5 10	
Minimum Clock Pulse Width	$t_{WL}=t_{WH}$		200 100	500 175		200 100	830 200	ns ns	5 10	
Clock Rise & Fall Time	$t_rCL=t_fCL$			15 15			15 15	μs μs	5 10	
Set Up Time			100 50	350 80		100 50	500 100	ns ns	5 10	
Maximum Clock Frequency	f_{CL}	1 3	2.5 5		0.6 2.5	2.5 5		MHz MHz	5 10	
Input Capacitance	C_I		5			5		pF		Any Input

Typical Characteristics



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-4015A

Dual 4-Stage Static Shift Register

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- FULLY STATIC OPERATION
- MSI COMPLEXITY – 8 MASTER-SLAVE FLIP-FLOPS ON A SINGLE CHIP
- CLOCK RATE 5 MHz (TYP.) $V_{DD} - V_{SS} = 10V$

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

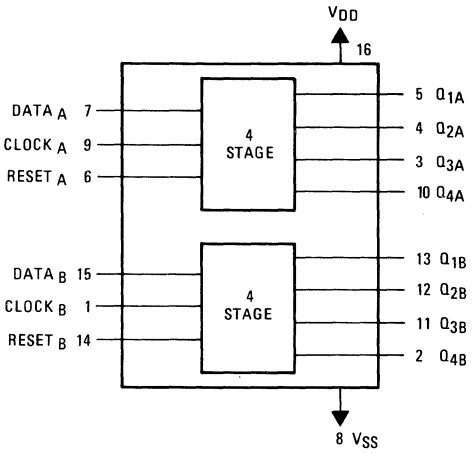
Description

The HD-4015 is a dual 4 stage static shift register. Both four bit segments are capable of independent operation. With an independent serial "Data", "Clock", and "Reset", input and "Q" output available from each stage.

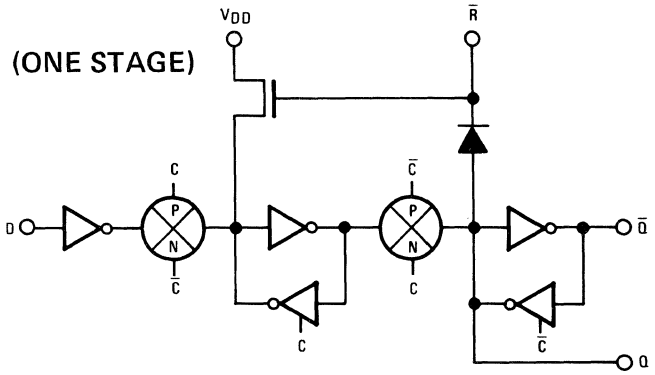
Resetting either four bit segment occurs when its respective reset line is held at a high level. Data shifting occurs on the positive-going clock transition.

The shift register function provided by the HD-4015 can easily be expanded in multiples of four stages by paralleling additional units as required.

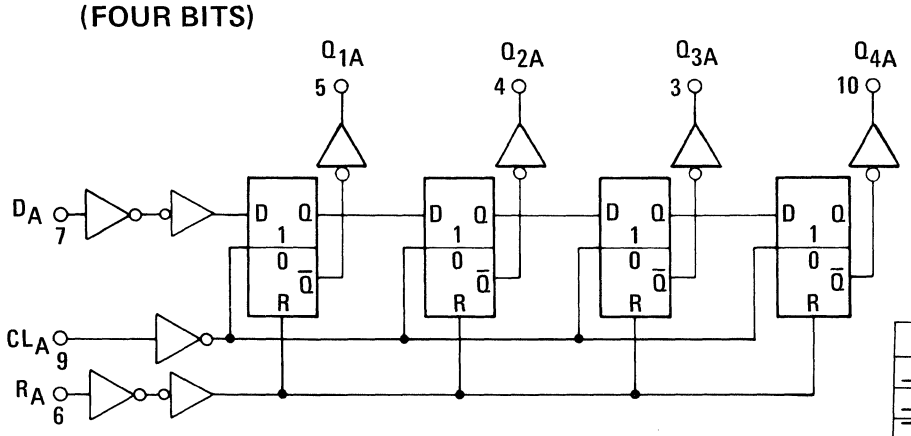
Connection Diagram



Circuit Diagram



Block Diagram



CL▲	D	R	Q_1	Q_n
⌐⌐	0	0	0	$Q_n - 1$
⌐⌐	1	0	1	$Q_n - 1$
⌐_	X	0	Q_1	Q_n (No Change)
X	X	1	0	0

▲ = Level Change
X = Don't Care Case

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}		-0.5VDC to +15VDC
Input Voltage Range (All Inputs), V_{IN}		V_{SS} -0.5VDC to V_{DD} +0.5VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4015A-2	-55°C to +125°C
	HD-4015A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4015A-2											
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Current						10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.1 V_O = 9.0
	N-Channel Output Drive Current	I_{DN}	0.15 0.31			0.12 0.25	0.3 0.5		0.085 0.175			mA mA	5 10	V_O = 0.5 V_O = 0.5
	P-Channel	I_{DP}	-0.1 -0.25			-0.08 -0.20	-0.16 -0.44		-0.055 -0.14			mA mA	5 10	V_O = 4.5 V_O = 9.5
	Quiescent Device CUrrent	I_L			5 10		0.5 1	5 10			300 600	µA µA	5 10	
	Quiescent Device Dissipation/Package	P_D			25 100		2.5 10	25 100			1500 6000	µW µW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

			HD-4015A-9											
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input current	I_I					10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
	N-Channel Output Drive Current	I_{DN}	0.072 0.12			0.06 0.1	0.3 0.5		0.05 0.08			mA mA	5 10	V_O = 0.5 V_O = 0.5
	P-Channel		-0.06 -0.12			-0.05 -0.1	-0.16 -0.44		-0.04 -0.08			mA mA	5 10	V_O = 4.5 V_O = 9.5
	Quiescent Device Current	I_L			50 100		0.5 1	50 100			700 1400	µA µA	5 10	
	Quiescent Device Dissipation/Package	P_D			250 1000		2.5 10	250 1000			3500 14000	µW µW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

Specification (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

			HD-4015A-2			HD-4015A-9			
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}
CLOCKED OPERATION									
Propagation Delay Time	$t_{PHL}=t_{PLH}$		300 100	750 225		300 100	1000 300	ns ns	5 10
Transition Time	$t_{THL}=t_{TLH}$		150 75	300 125		150 75	400 150	ns ns	5 10
Minimum Clock Pulse Width	$t_{WL}=t_{WH}$		200 100	500 175		200 100	830 200	ns ns	5 10
Clock Rise & Fall Time	$t_rCL=t_fCL$			15 15			15 15	μs μs	5 10
A.C. Set Up Time			100 50	350 80		100 50	500 100	ns ns	5 10
Maximum Clock Frequency	f_{CL}	1 3	2.5 5		0.6 2.5	2.5 5		MHz MHz	5 10
Input Capacitance	C_I		5			5		pF	
RESET OPERATION									
Propagation Delay Time	$t_{PHL(R)}$		300 100	750 225		300 100	1000 300	ns ns	5 10
Minimum Set and Reset Pulse Widths	$t_{WH(R)}$		200 100	500 175		200 100	830 200	ns ns	5 10

HD-4017A

Decade Counter/Divider

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- MSI COMPLEXITY – FIVE COUNTER STAGES, OUTPUT DECODING, AND INPUT/OUTPUT BUFFERING ON A SINGLE CHIP
- FULLY STATIC OPERATION
- SYNCHRONOUS CLOCKING

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

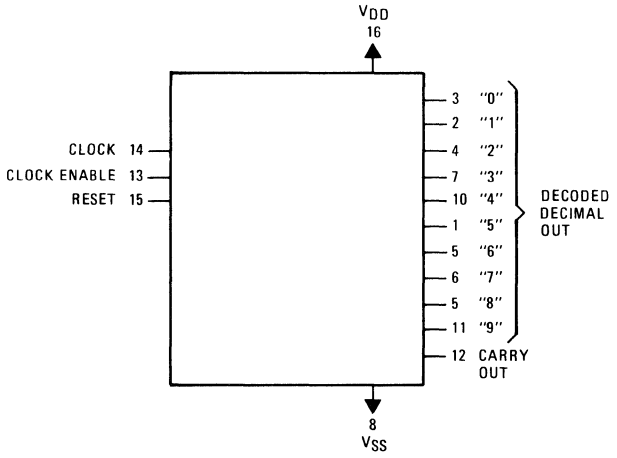
Description

The HD-4017 is a five stage Johnson decade counter with decoded outputs. The Johnson counter configuration provides high speed synchronous clocking and spike-free outputs. Clocking occurs on the positive going clock input with the clock enable input "low". Internal clock is inhibited when the clock enable signal is "high". A "high" on the reset input resets the counter the to "zero" state.

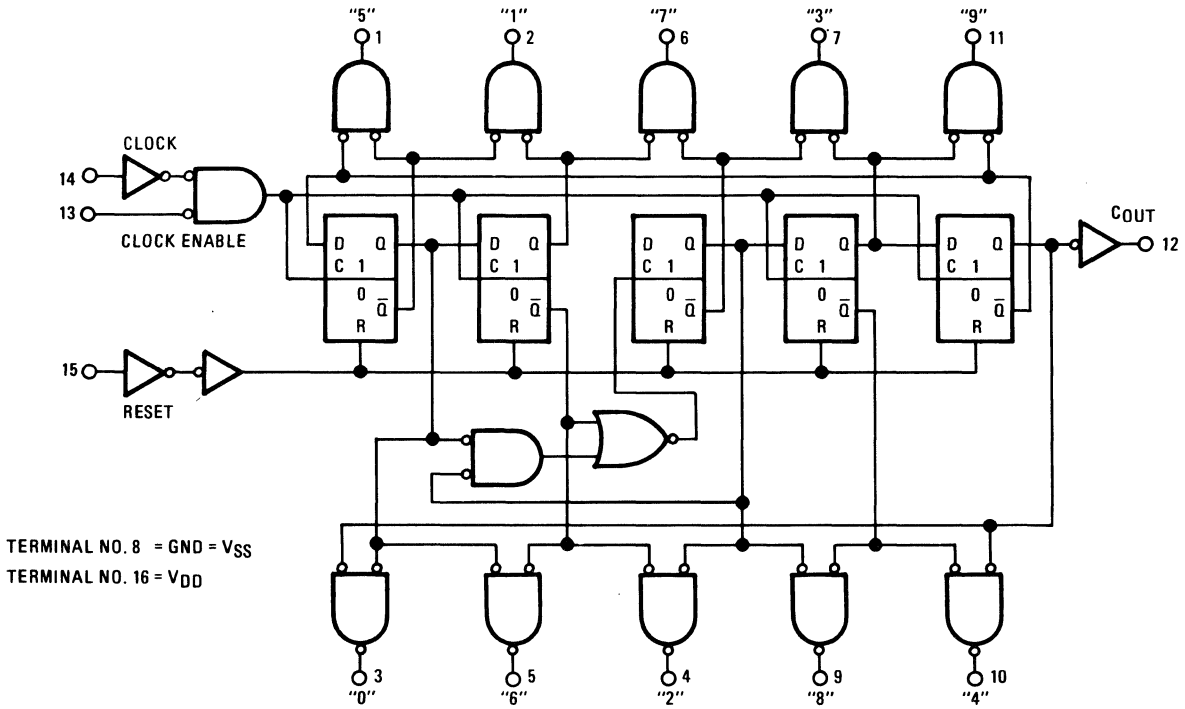
The state of the undecoded outputs is "low". The decoded output going and remaining high for one clock cycle.

A carry output is provided to allow for counter expansion to additional decades.

Connection Diagram



Logic Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Input Voltage Range (All Inputs), V_{IN}		V_{SS} -0.5VDC to V_{DD} +0.5VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4017A-2	-55°C to +125°C
	HD-4017A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

D.C.

PARAMETER	SYM.	HD-4017A-2 -55°C MIN.	-55°C TYP.	-55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C TYP.	+125°C MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		
Noise Immunity	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
Output Drive Current N-Channel	I_{DN}	0.06 0.12			0.05 0.1	0.1 0.4		0.035 0.07			mA mA	5 10	V_O = 0.5 Decoded V_O = 0.5 Outputs
		0.185 0.45			0.15 0.35	0.4 1		0.105 0.25			mA mA	5 10	V_O = 0.5 Carry V_O = 0.5 Output
Output Drive Current P-Channel	I_{DP}	-0.0375 -0.12			-0.03 -0.1	-0.075 -0.2		-0.021 -0.07			mA mA	5 10	V_O = 4.5 Decoded V_O = 9.5 Outputs
		-0.185 -0.45			-0.15 -0.35	-0.4 1		-0.105 -0.25			mA mA	5 10	V_O = 4.5 Carry V_O = 9.5 Output
Quiescent Device Current	I_L			5 10		0.3 0.5	5 10			300 600	μA μA	5 10	
Quiescent Device Dissipation/Package	P_D			25 100		1.5 5	25 100			1500 6000	μW μW	5 10	
Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
High Level Output Voltage	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

D.C.

PARAMETER	SYM.	HD-4017A-9 -40°C MIN.	-40°C TYP.	-40°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+85°C MIN.	+85°C TYP.	+85°C MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		
Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
Output Drive Current N-Channel	I_{DN}	0.03 0.085			0.025 0.07	0.1 0.4		0.02 0.055			mA mA	5 10	V_O = 0.5 Decoded V_O = 0.5 Outputs
		0.095 0.3			0.08 0.25	0.4 1		0.065 0.2			mA mA	5 10	V_O = 0.5 Carry V_O = 0.5 Output
Output Drive Current P-Channel	I_{DP}	-0.018 -0.085			-0.015 -0.07	-0.075 -0.2		-0.012 -0.055			mA mA	5 10	V_O = 4.5 Decoded V_O = 9.5 Outputs
		-0.095 -0.3			-0.08 -0.24	-0.4 1		-0.065 -0.20			mA mA	5 10	V_O = 4.5 Carry V_O = 9.5 Output
Quiescent Device Current	I_L			50 100		0.5 1	50 100			700 1400	μA μA	5 10	
Quiescent Device Dissipation/Package	P_D			250 1000		2.5 10	250 1000			3500 14000	μW μW	5 10	
Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
High Level Output Voltage	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

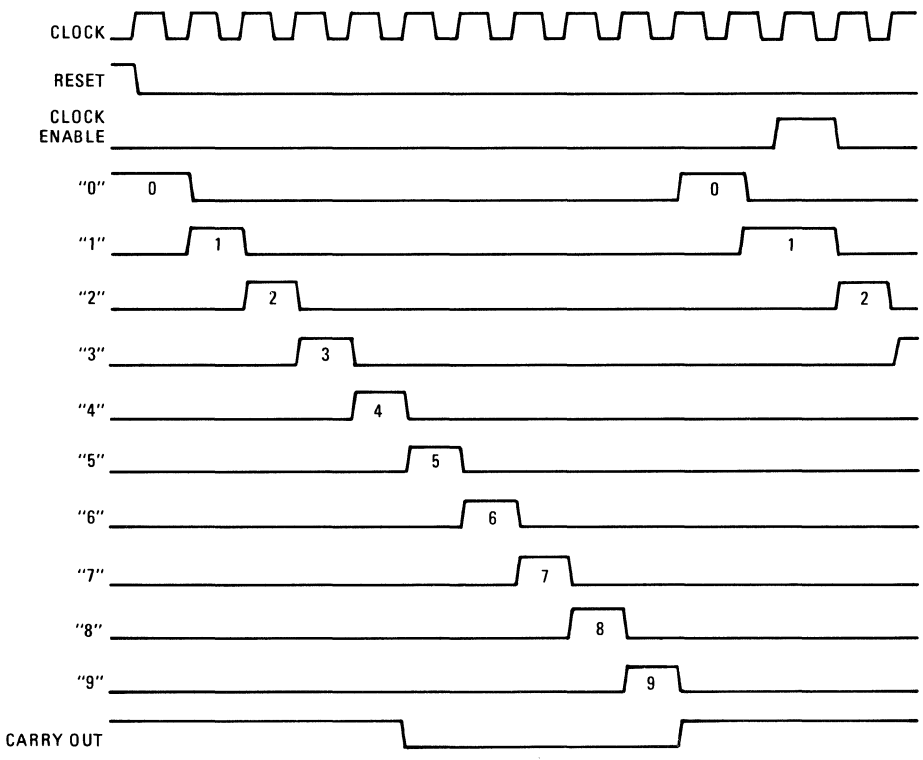
Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

A.C.

PARAMETER	SYMBOL	HD-4017A-2 MIN.	HD-4017A-2 TYP.	HD-4017A-2 MAX.	HD-4017A-9 MIN.	HD-4017A-9 TYP.	HD-4017A-9 MAX.	UNITS	V_{DD}	
CLOCKED OPERATION										
Carry Out Line Propagation Delay Time	t_{PHL}= t_{PLH}		350 125	1000 250		350 125	1300 300	ns ns	5 10	
Decode Out Lines	t_{PHL}= t_{PLH}		500 200	1200 400		500 200	1600 500	ns ns	5 10	
Carry Out Line Transition Time	t_{THL}= t_{TLH}		100 50	300 150		100 50	350 200	ns ns	5 10	
Decode Out lines	t_{THL}= t_{TLH}		300 125	900 350		300 125	1200 450	ns ns	5 10	
Minimum Clock Pulse Width	t_{WL}= t_{WH}		200 100	500 170		200 100	830 250	ns ns	5 10	
Clock Rise & Fall Time	t_rCL= t_fCL			15 15			15 15	μs μs	5 10	
Clock Enable Set Up Time			175 75	500 200		175 75	700 300	ns ns	5 10	
Maximum Clock Frequency	f_{CL}	1 3	2.5 5		0.6 2	2.5 5		MHz MHz	5 10	
Input Capacitance	C_I		5			5		pF		Any Input
RESET OPERATION										
Carry Out line Propagation Delay Time	$t_{PHL(R)}$		350 125	1000 250		350 125	1300 300	ns ns	5 10	
Decode Out Lines			450 200	1200 400		450 200	1600 500	ns ns	5 10	
Reset Pulse Width	$t_{WH(R)}$		200 100	500 165		200 100	830 250	ns ns	5 10	
Reset Removal Time			300 100	750 225		300 100	1000 275	ns ns	5 10	

Waveforms



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-4018A

Presettable Divide-By-'N' Counter

Features

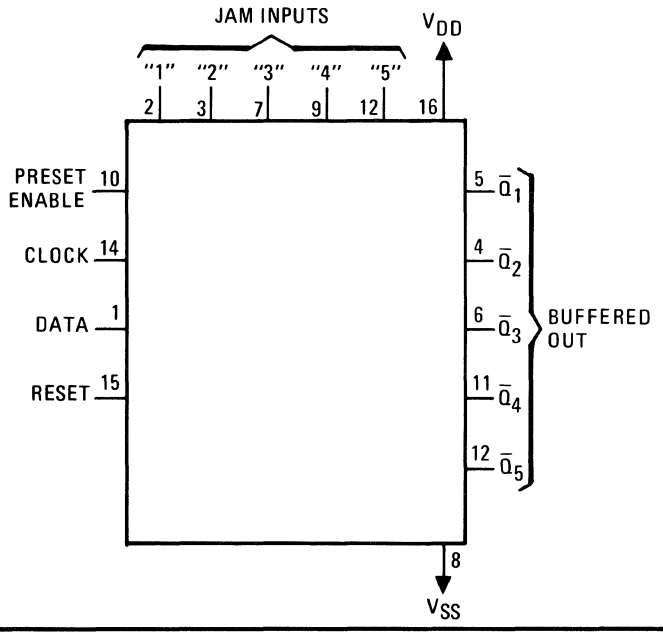
- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY AND LOW QUIESCENT POWER DISSIPATION
- MSI COMPLEXITY – FIVE COUNTER BITS, AND ASSOCIATED GATING AND BUFFERING
- FULLY STATIC OPERATION
- SYNCHRONOUS CLOCKING

Description

The HD-4018 is a 5-bit Johnson counter incorporating reset and load capabilities. Fixed and programmable frequency division can be implemented by hard wiring or gating feedback to the data input. Divide by 10, 8, 6, 4, and 2 result from feedback of Q_5, Q_4, Q_3, Q_2 and Q_1 to the data input. Proper gating of feedback results in division by 9, 7, 5, or 3. Division by numbers greater than 10 can be performed by using two or more HD-4018's.

Application of a "high" to the reset input clears the counter to the "zero" state. When the preset enable input is held high, data applied to the Jam inputs is loaded into the counter asynchronously with the clock. The counter increments synchronously with the positive-going clock transition.

Connection Diagram

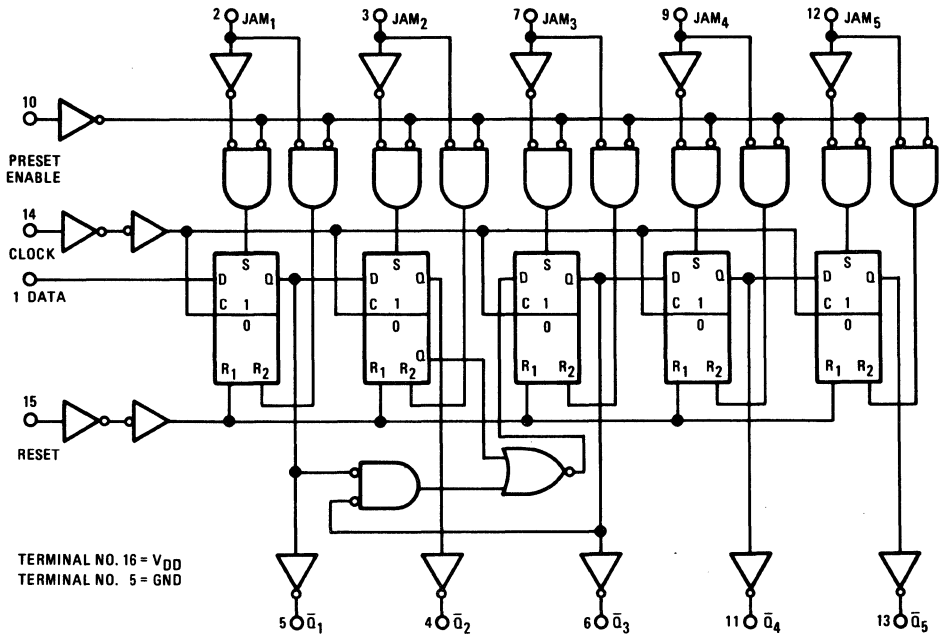


Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD}-V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4018A-2	-55°C to +125°C
	HD-4018A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4018A-2											
			-55°C			+25°C			+125°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		
	Noise Immunity (Any Input)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	N-Channel Output Drive Current	I_{DN}	0.18 0.45			0.15 0.35	0.4 1		0.105 0.25			mA mA	5 10	V_O = 0.5 $\overline{Q}_5$ V_O = 0.5
			0.06 0.25			0.05 0.2	0.1 0.4		0.035 0.14			mA mA	5 10	V_O = 0.5 $\overline{Q}_1, \overline{Q}_2$, V_O = 0.5 $\overline{Q}_3, \overline{Q}_4$
	P-Channel Output Drive Current	I_DP	-0.185 -0.45			-0.15 -0.35	-0.4 -1		-0.105 -0.25			mA mA	5 10	V_O = 4.5 $\overline{Q}_5$ V_O = 9.5
			-0.075 -0.25			-0.06 -0.2	-0.15 -0.4		-0.04 -0.14			mA mA	5 10	V_O = 4.5 $\overline{Q}_1, \overline{Q}_2$, V_O = 9.5 $\overline{Q}_3, \overline{Q}_4$
	Quiescent Device Current	I_L			5 10		0.3 0.5	5 10			300 600	µA µA	5 10	
	Quiescent Device Dissipation/Package	P_D			25 100		1.5 5	25 100			1500 600	µW µW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level Output Voltage	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

			HD-4018A-9											
			-40°C			+25°C			+85°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		
	Noise Immunity (Any Input)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	N-Channel Output Drive Current	I_DN	0.095 0.3			0.08 0.25	0.4 1		0.065 0.2			mA mA	5 10	V_O = 0.5 $\overline{Q}_5$ V_O = 0.5
			0.03 0.18			0.025 0.15	0.1 0.4		0.02 0.12			mA mA	5 10	V_O = 0.5 $\overline{Q}_1, \overline{Q}_2$, V_O = 0.5 $\overline{Q}_3, \overline{Q}_4$
	P-Channel Output Drive Current	I_DP	-0.095 -0.3			-0.08 -0.25	-0.4 -1		-0.065 -0.2			mA mA	5 10	V_O = 4.5 $\overline{Q}_5$ V_O = 9.5
			-0.035 -0.18			-0.03 -0.15	-0.15 -0.4		-0.024 -0.12			mA mA	5 10	V_O = 4.5 $\overline{Q}_1, \overline{Q}_2$, V_O = 9.5 $\overline{Q}_3, \overline{Q}_4$
	Quiescent Device Current	I_L			50 100		0.5 1	50 100			700 1400	µA µA	5 10	
	Quiescent Device Dissipation/Package	P_D			250 1000		2.5 10	250 1000			3500 14000	µW µW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level Output Voltage	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

Specifications

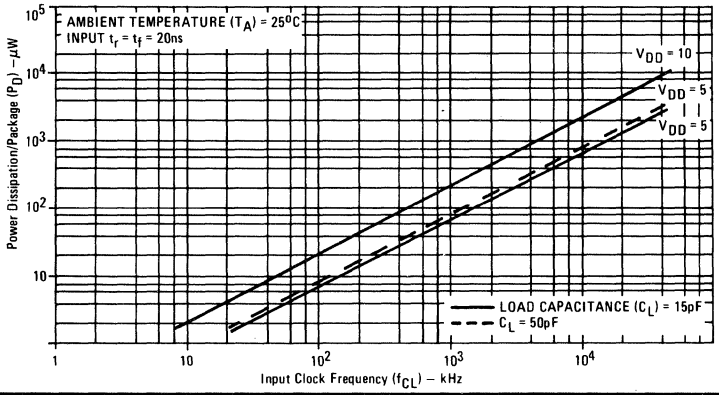
ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

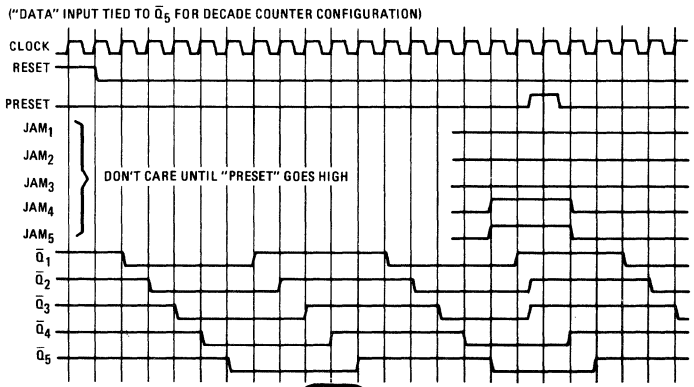
	PARAMETERS	SYMBOL	HD-4018A-2 MIN.	HD-4018A-2 TYP.	HD-4018A-2 MAX.	HD-4018A-9 MIN.	HD-4018A-9 TYP.	HD-4018A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	CLOCKED OPERATION										
	Propagation Delay Time To $\overline{Q}_5$ Output	$t_{PHL}=t_{PLH}$		350 125	1000 250		350 125	1300 300	ns ns	5 10	
	Propagation Delay Time To Other Outputs	$t_{PHL}=t_{PLH}$		500 200	1200 400		500 200	1600 500	ns ns	5 10	
	Transition Time To $\overline{Q}_5$ Output	$t_{THL}=t_{TLH}$		100 50	300 150		100 50	350 200	ns ns	5 10	
	Transition Time To Other Outputs	$t_{THL}=t_{TLH}$		300 125	900 350		300 125	1200 450	ns ns	5 10	
	Minimum Clock Pulse Width	$t_{WL} = t_{WH}$		200 100	500 170		200 100	830 250	ns ns	5 10	
	Clock Rise & Fall Time	$t_rCL=t_fCL$			15 15			15 15	μs μs	5 10	
	Data input Setup Time			175 75	500 200		175 75	700 300	ns ns	5 10	
	Maximum Clock Frequency	f_{CL}	1 3	2.5 5		0.6 2	2.5 5		MHz MHz	5 10	
	Input Capacitance	C_I		5			5		pF		Any Input
	PRESET OR RESET OPERATION										
	Propagation Delay Time To $\overline{Q}_5$ Output	$t_{PLH(R)}$		350 125	1000 250		350 125	1300 300	ns ns	5 10	
	Propagation Delay Time To Other Outputs	$t_{PHL(PR)}=$ $t_{PLH(PR)}$		500 200	1200 400		500 200	1600 500	ns ns	5 10	
	Preset or Reset Pulse Width	$t_{WH(R)}$, $t_{WH(PR)}$		200 100	500 165		200 100	830 250	ns ns	5 10	
	Preset or Reset Removal Time			300 100	750 225		300 100	1000 275	ns ns	5 10	

*At Preset Enable or Jam Inputs.

Typical Characteristics



Waveform



HD-4019A

Quad AND-OR Select Gate

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE.
- SINGLE POWER SUPPLY OPERATION
- EFFECTIVE STATIC CHARGE PROTECTION

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Description

The HD-4019 is a small scale CMOS integrated circuit providing the system designer with a logic building block for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power dissipation, high noise immunity, nearly symmetric output rise and fall times, and wide power supply operating voltage range.

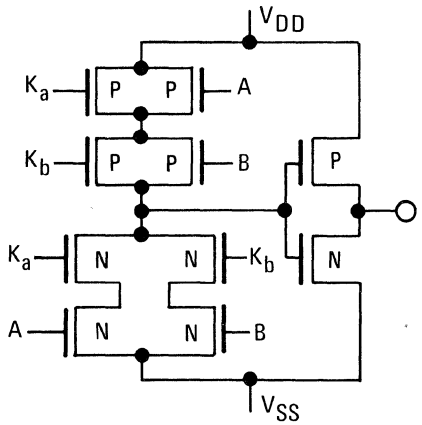
Truth Table

CONTROL		OUTPUT
K_a	K_b	D_1
0	0	0
0	1	B_1
1	0	A_1
1	1	$A_1 + B_1$

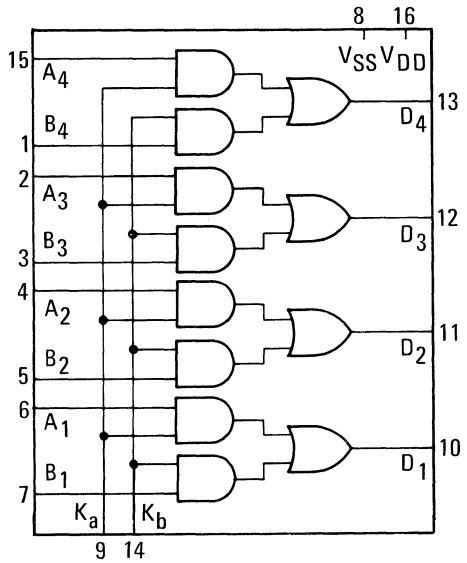
LOGIC "1" $\longrightarrow V_{DD}$

LOGIC "0" $\longrightarrow V_{SS}$

Functional Diagram



Connection Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4019A-2	-55°C to +125°C
	HD-4019A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4019A-2											
			-55°C			+25°C			+125°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OL} \leq$ .95VDC $V_{OL} \leq$ 2.9VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OH} \geq$ 3.6VDC $V_{OH} \geq$ 7.2VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ I_O = 0A
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ I_O = 0A
	Quiescent Power Supply Current	I_{DD}			5 10		.03 .05	5 10			300 600	μA μA	5 10	
	Output Drive Current	I_{OL}	0.6 0.9			.45 .75	.9 1.5		.3 .55			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
		I_{OH}	-.31 -.95			-.25 -.7	-.5 -1.5		-.175 -.5			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
	Input Capacitance	C_{IN}					5 12					pF pF		All A and B inputs K_a and K_b inputs

			HD-4019A-9											
			-40°C			+25°C			+85°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OL} \leq$ .95VDC $V_{OL} \leq$ 2.9VDC
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OH} \geq$ 3.6VDC $V_{OH} \geq$ 7.2VDC
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ I_O = 0A
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ I_O = 0A
	Quiescent Power Supply Current	I_{DD}			50 100		.1 .2	50 100			700 1,400	μA μA	5 10	
	Output Drive Current	I_{OL}	.37 .8			.3 .65	1 1.5		.23 .5			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
		I_{OH}	-.145 -.6			-.12 -.5	-.5 -1.5		-.095 -.4			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
	Input Capacitance	C_{IN}					5 12					pF pF		All A and B inputs K_a and K_b inputs

Specifications (continued)

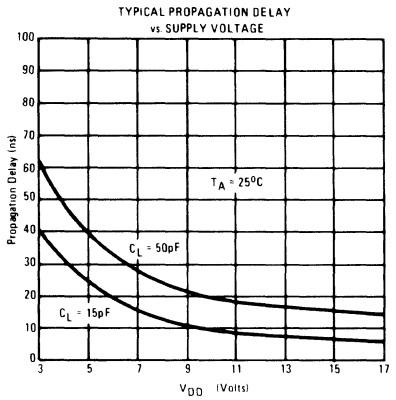
ELECTRICAL CHARACTERISTICS (DYNAMIC)

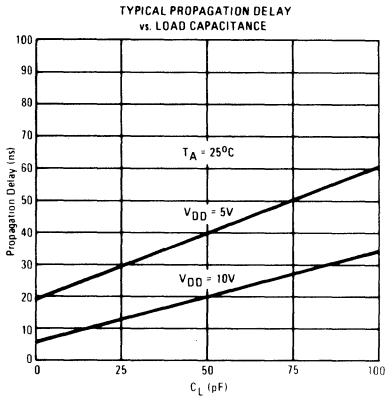
$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

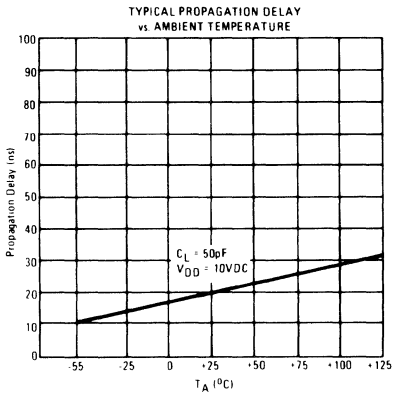
	PARAMETER	SYMBOL	HD-4019A-2 TYP.	HD-4019A-2 MAX.	HD-4019A-9 TYP.	HD-4019A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay	t_{PLH}	100 50	225 100	100 50	300 125	ns ns	5 10	Ref. to Switching Time Definitions
		t_{PHL}	100 50	225 100	100 50	300 125	ns ns	5 10	
	Transition Time	t_{TLH}	100 40	200 65	100 40	275 80	ns ns	5 10	
		t_{THL}	100 40	200 65	100 40	275 80	ns ns	5 10	

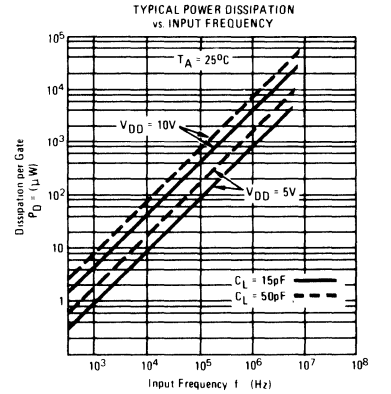
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

Typical Characteristics

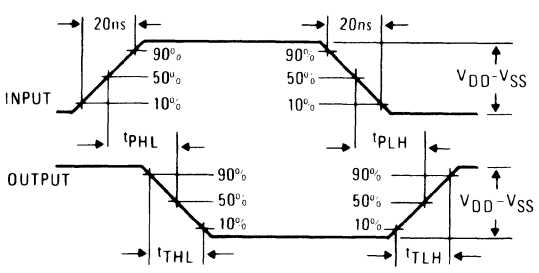


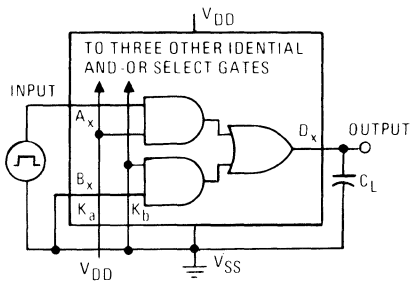






Switching Time Definitions and Conditions





HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-4020A

14-Stage Ripple-Carry Binary Counter/Divider

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- MSI COMPLEXITY – FOURTEEN BINARY COUNTER STAGES WITH INPUT/OUTPUT BUFFERING
- FULLY STATIC OPERATION
- CLOCK RATE 7MHz(typ.) $V_{DD} - V_{SS} = 10V$
- INPUT BUFFERING FOR REDUCED INPUT CAPACITANCE AND IMPROVED NOISE IMMUNITY

Description

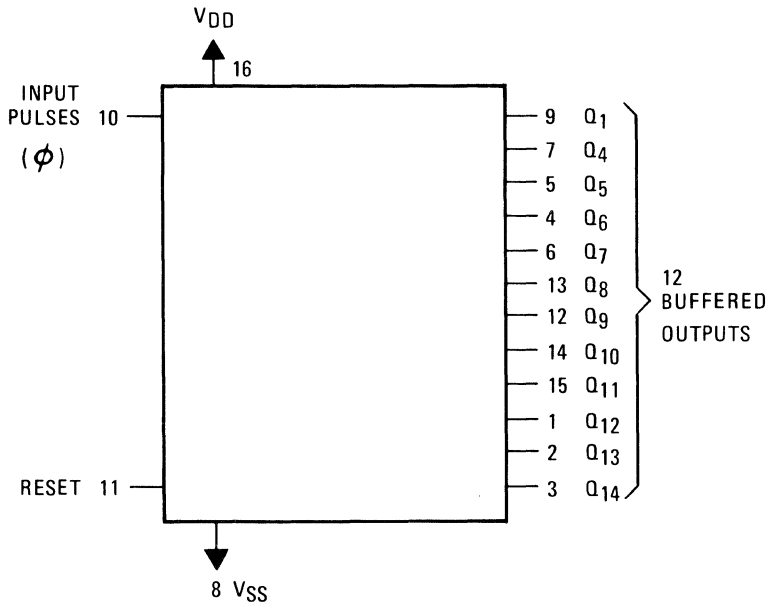
The HD-4020 is a 14 stage ripple-carry binary counter/ divider. Buffered outputs are available from stage 1, and stages 4 through 14. The counter increments on the negative going edge of the input pulse. Resetting of the counter to the "zero" state occurs when a "high" is applied to the reset input.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Connection Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD}-V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200 mW
Operating Temperature Range:	HD-4020A-2	-55°C to +125°C
	HD-4020A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4020A-2											
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_I					10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3.0			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3.0			V V	5 10	V_O = 4.2 V_O = 9.0
	N-Channel Output Drive Current	I_DN	0.09 0.185			0.075 0.15	0.2 0.4		0.05 0.105			mA mA	5 10	V_O = 0.5 V_O = 0.5
	P-Channel	I_DP	-0.11 -0.25			-0.09 -0.20	-0.25 -0.5		0.065 -0.14			mA mA	5 10	V_O = 4.5 V_O = 9.5
	Quiescent Device Current	I_L			15 25		0.5 1	15 25			900 1500	μA μA	5 10	
	Quiescent Device Dissipation/Package	P_D			75 250		2.5 10	75 250			4500 15000	μW μW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

			HD-4020A-9										CONDITIONS	
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_I					10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3.0			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3.0			V V	5 10	V_O = 4.2 V_O = 9.0
	N-Channel Output Drive Current	I_DN	0.09 0.16			0.08 0.13	0.33 0.5		0.065 0.10			mA mA	5 10	V_O = 0.5 V_O = 0.5
	P-Channel	I_DP	0.09 -0.18			-0.06 -0.15	-0.25 -0.5		-0.05 -0.12			mA mA	5 10	V_O = 4.5 V_O = 9.5
	Quiescent Device Current	I_L			50 100		1 2	50 100			700 1400	μA μA	5 10	
	Quiescent Device Dissipation/package	P_D			250 1000		5 20	250 1000			3500 14000	μW μW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

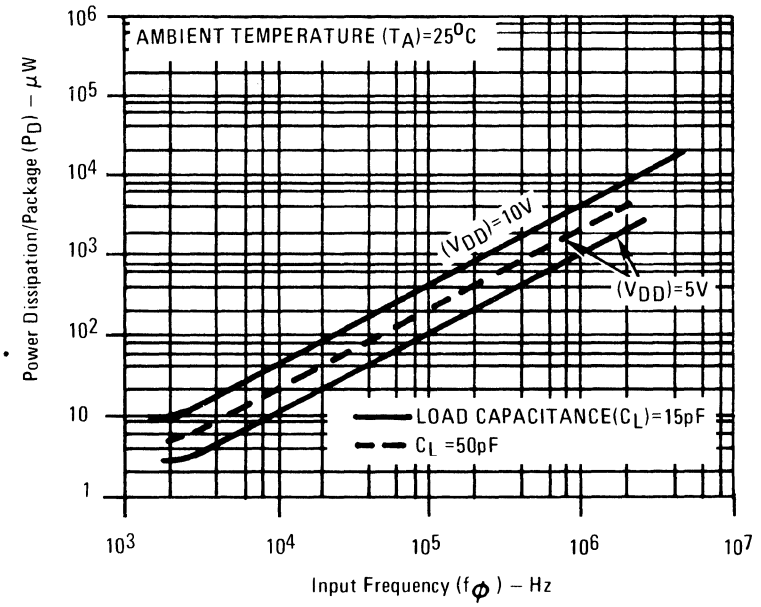
Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	HD-4020A-2 MIN.	HD-4020A-2 TYP.	HD-4020A-2 MAX.	HD-4020A-9 MIN.	HD-4020A-9 TYP.	HD-4020A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	CLOCKED OPERATION										
	Propagation Delay Time	$t_{PHL}=t_{PLH}$		450 150	600 225		450 150	650 250	ns ns	5 10	
	Transition Time	$t_{THL}=t_{TLH}$		450 200	600 300		450 200	650 350	ns ns	5 10	
	Minimum Clock Pulse Width	$t_{WL}=t_{WH}$		200 70	335 125		200 70	500 165	ns ns	5 10	
	Clock Rise & Fall Time	$t_rCL=t_fCL$			15 15			15 15	μs μs	5 10	
	Maximum Clock Frequency	f_{CL}	1.5 4	2.5 7		1 3	2.5 7		MHz MHz	5 10	
	Input Capacitance	C_I		5			5		pF		Any Input
	RESET OPERATION										
	Propagation Delay Time	$t_{PHL(R)}$		2000 500	3000 775		2000 500	3500 900	ns ns	5 10	
	Minimum Reset Pulse Width	$t_{WH(R)}$		1800 300	2500 475		1800 300	3000 550	ns ns	5 10	

Typical Characteristics



HD-4021A

8-Stage Static Shift Register

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- FULLY STATIC OPERATION
- MSI COMPLEXITY – 8 MASTER/SLAVE FLIP-FLOPS ON A SINGLE CHIP
- ASYNCHRONOUS PARALLEL OR SYNCHRONOUS SERIAL DATA INPUT

Description

The HD-4021 is an 8-stage parallel or serial input/serial output shift register. Inputs are provided for clock, parallel/ serial control, serial data, and parallel data (8 inputs). "Q" outputs for the sixth, seventh, and eighth stages are also available.

With the parallel/serial control high data is jammed into the register via the parallel input lines. With the parallel/serial input low data is shifted synchronously during the positive going clock.

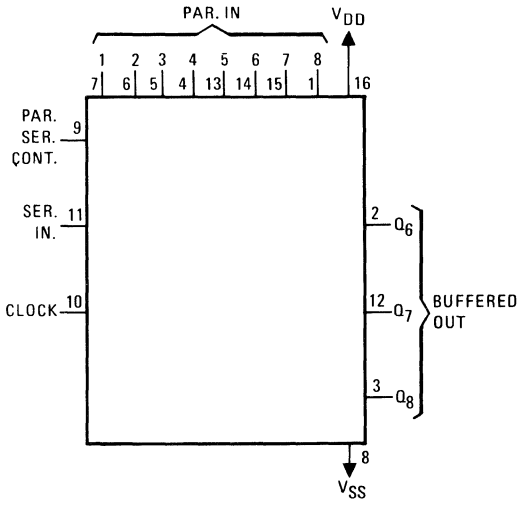
The HD-4021 register function can be easily expanded in multiples of eight stages by paralleling additional units as required.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Connection Diagram

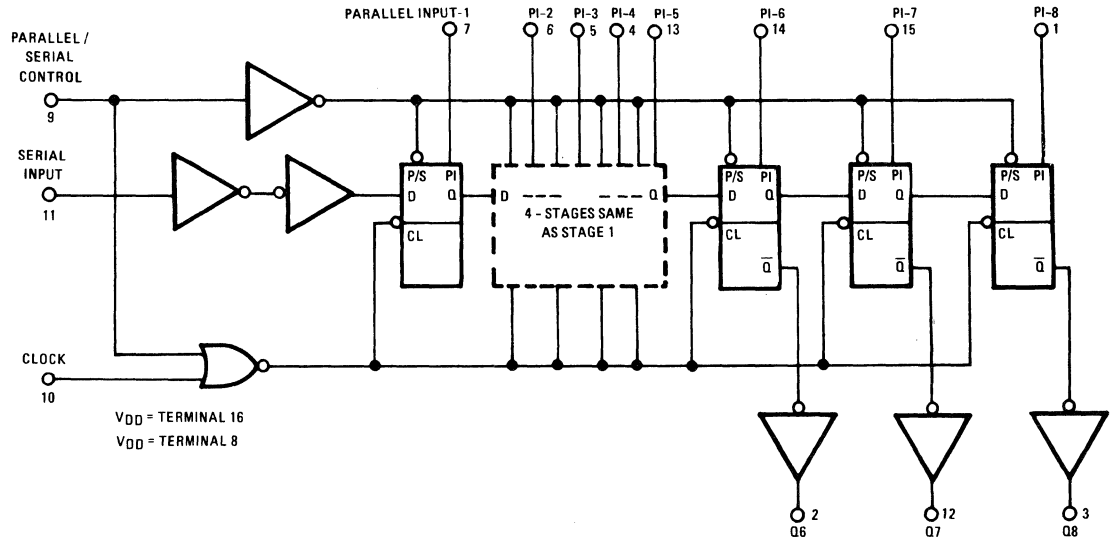


Truth Table

C_L▲	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI - 1	PI - n	Q_1 (INTERNAL)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⎍	0	0	X	X	0	Q_{n-1}	
⎍	1	0	X	X	1	Q_{n-1}	
⎎	X	0	X	X	Q_1	Q_n	NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD}-V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4021A-2	-55°C to +125°C
	HD-4021A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

D.C

		HD-4021A-2										CONDITIONS	
		-55°C			+25°C			+125°C					
PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		
Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
Output Drive Current N-Channel	I_{DN}	0.15 0.31			0.12 0.25	0.3 0.5		0.085 0.175			mA mA	5 10	V_O = 0.5 V_O = 0.5
P-Channel	I_{DP}	-0.1 -0.25			-0.08 -0.20	-0.16 -0.44		-0.055 -0.14			mA mA	5 10	V_O = 4.5 V_O = 9.5
Quiescent Drive Current	I_L			5 10		0.5 1	5 10			300 600	µA µA	5 10	
Quiescent Device Dissipation/Package	P_D			25 100		2.5 10	25 100			1500 6000	µW µW	5 10	
Output Voltage Low Level	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
Output Voltage High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

D.C.

		HD-4021A-9										CONDITIONS	
		-40°C			+25°C			+85°C					
PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		
Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
Output Drive Current N-Channel	I_{DN}	0.072 0.12			0.06 0.1	0.3 0.5		0.05 0.08			mA mA	5 10	V_O = 0.5 V_O = 0.5
P-Channel	I_{DP}	-0.06 -0.12			-0.05 -0.1	-0.16 -0.44		-0.04 -0.08			mA mA	5 10	V_O = 4.5 V_O = 9.5
Quiescent Deviee Current	I_L			50 100		0.5 1	50 100			700 1400	µA µA	5 10	
Quiescent Device Dissipation/Package	P_D			250 1000		2.5 10	250 1000			3500 14000	µW µW	5 10	
Output Voltage Low Level	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
Output Voltage High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

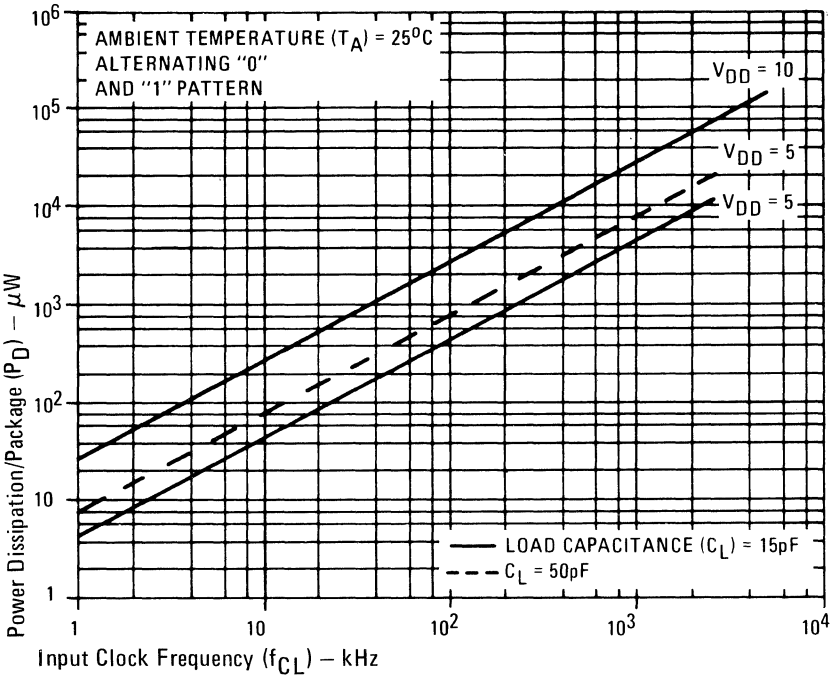
Specifications (continued)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	HD-4021A-9 MIN.	HD-4021A-9 TYP.	HD-4021A-9 MAX.	HD-4021A-2 MIN.	HD-4021A-2 TYP.	HD-4021A-2 MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
A.C.	Propagation Delay Time	$t_{PHL}=t_{PLH}$		300 100	750 225		300 100	1000 300	ns ns	5 10	
	Transition Time	$t_{THL}=t_{TLH}$		150 75	300 125		150 75	400 150	ns ns	5 10	
	Minimum Clock Pulse Width	$t_{WL}=t_{WH}$		200 100	500 175		200 100	830 200	ns ns	5 10	
	Minimum High Level Parallel/Serial Control Pulse Width	$t_{WH(P/S)}$		200 100	500 175		200 100	830 200	ns ns	5 10	
	Clock Rise & Fall Time	$t_rCL=t_fCL$			15 15			15 15	μs μs	5 10	
	Set Up Time			100 50	350 80		100 50	500 100	ns ns	5 10	
	Maximum Clock Frequency	f_{CL}	1 3	2.5 5		0.6 2.5	2.5 5		MHz MHz	5 10	
	Input Capacitance	C_I		5			5		pF		Any Input

From Clock or Parallel/Serial Control Input

Typical Characteristics



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-4022A

Divide-By-8 Counter/Divider with 8 Decoded Outputs

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- MSI COMPLEXITY – FIVE COUNTER STAGES, OUTPUT DECODING AND INPUT/OUTPUT BUFFERING ON A SINGLE CHIP
- FULLY STATIC OPERATION
- SYNCHRONOUS CLOCKING

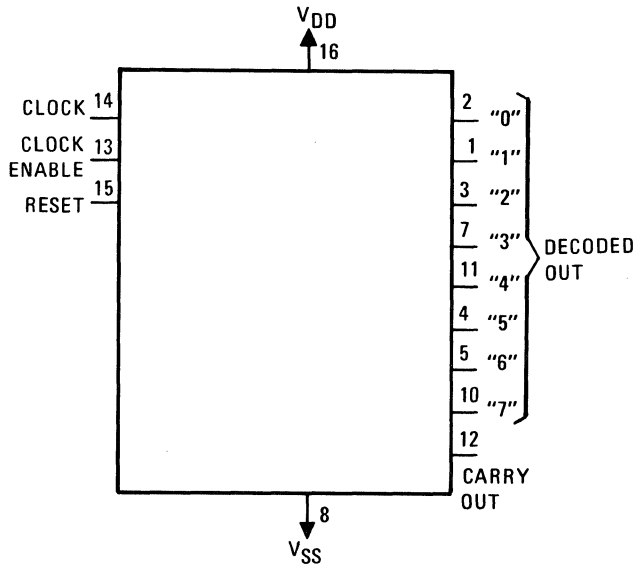
Description

The HD-4022 is a 4-stage Johnson counter with decoded outputs. The counter outputs internally drive the inputs of a one of eight decoder, with the decoder outputs available at the package pins. Buffered clock and reset pins are provided for maximization of circuit noise immunity and reduction of input capacitance. A clock enable pin is also available. The counter advances on the positive going clock signal if clock enable is low.

The Johnson counter configuration permits high speed spike-free operation with all counter stages clocking in parallel.

The normal state of an undecoded output is low, going high for one complete clock cycle when decoded. The carry-out signal goes high every 8 clock cycles, and can be used as a ripply carry input if two or more counters are used in parallel.

Connection Diagram

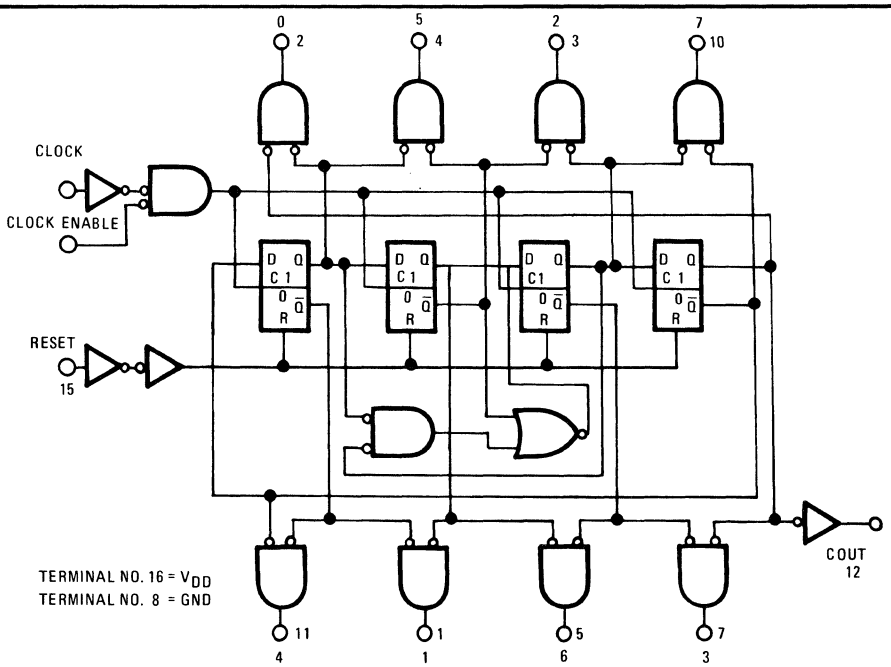


Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD}-V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		$-65^{o}C$ to $+150^{o}C$
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4022A-2	$-55^{o}C$ to $+125^{o}C$
	HD-4022A-9	$-40^{o}C$ to $+85^{o}C$

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4022A-2										CONDITIONS	
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	Output Drive Current N-Channel	I_{DN}	0.062 0.12			0.05 0.1	0.15 0.3		0.035 0.07			mA mA	5 10	V_O = 0.5 Decoded V_O = 0.5 Outputs
			0.185 0.375			0.15 0.3	0.5 1		0.105 0.21			mA mA	5 10	V_O = 0.5 Carry V_O = 0.5 Output
	Output Drive Current P-Channel	I_{DP}	-0.038 -0.062			-0.03 -0.05	-0.075 -0.15		-0.021 -0.035			mA mA	5 10	V_O = 4.5 Decoded V_O = 9.5 Outputs
			-0.185 -0.375			-0.15 -0.3	-0.4 -0.8		-0.105 -0.21			mA mA	5 10	V_O = 4.5 Carry V_O = 9.5 Output
	Quiescent Device Current	I_L			5 10		0.3 0.5	5 10			300 600	μA μA	5 10	
	Quiescent Device Dissipation/Package	P_D			25 100		1.5 5	25 100			1500 6000	μW μW	5 10	
	Output Voltage Low Level	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	Output Voltage High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

			HD-4022A-9										CONDITIONS	
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	Output Drive Current N-Channel	I_{DN}	0.03 0.06			0.025 0.05	0.15 0.3		0.02 0.04			mA mA	5 10	V_O = 0.5 Decoded V_O = 0.5 Outputs
			0.095 0.155			0.08 0.13	0.5 1		0.065 0.105			mA mA	5 10	V_O = 0.5 Carry V_O = 0.5 Output
	Output Drive Current P-Channel	I_{DP}	-0.018 -0.06			-0.015 -0.05	-0.075 -0.15		-0.012 -0.04			mA mA	5 10	V_O = 4.5 Decoded V_O = 9.5 Outputs
			-0.095 -0.155			-0.08 -0.13	-0.4 -0.8		-0.065 -0.105			mA mA	5 10	V_O = 4.5 Carry V_O = 9.5 Outputs
	Quiescent Device Current	I_L			50 100		0.5 1	50 100			700 1400	μA μA	5 10	
	Quiescent Device Dissipation/Package	P_D			250 1000		2.5 10	250 1000			3500 14000	μW μW	5 10	
	Output Voltage Low Level	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	Output Voltage High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

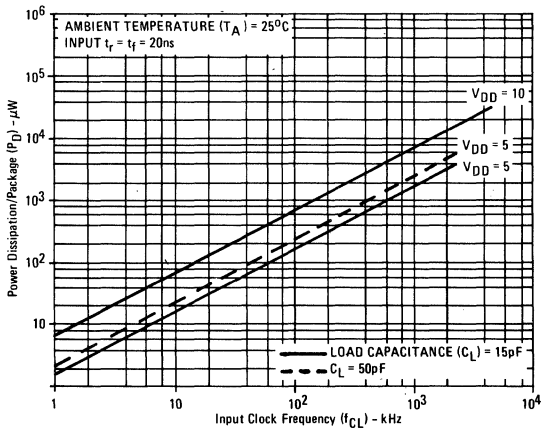
Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

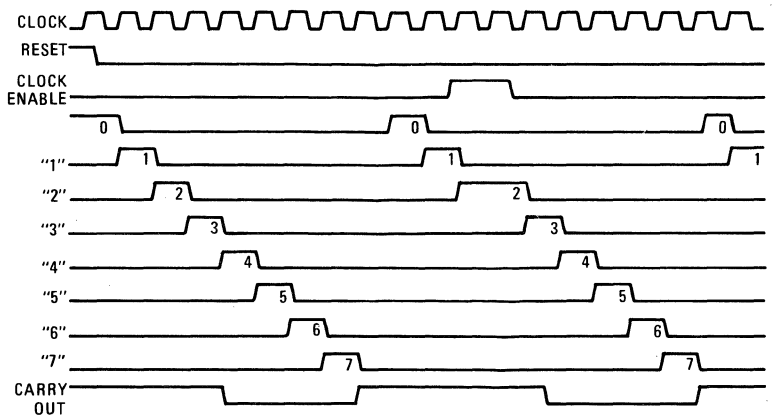
$T_A = 25^oC$, $C_L = 15pF$ Input Rise and Fall Times = 20ns unless otherwise specified.

			HD-4022A-2			HD-4022A-9			CONDITIONS	
PARAMETER	SYMBOLS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
A.C. CLOCKED OPERATION										
Carry out Line Propagation Delay Time	$t_{PHL}=t_{PLH}$		325	1000		325	1300	ns	5	
			125	250		125	500	ns	10	
Decode Out Lines			400	1200		400	1600	ns	5	
			200	400		200	800	ns	10	
Carry Out Line Transition Time	$t_{THL}=t_{TLH}$		85	300		85	340	ns	5	
			50	100		50	200	ns	10	
DecodeOut Lines			300	900		300	1200	ns	5	
			125	250		125	500	ns	10	
Minimum Clock Pulse Width	$t_{WL}=t_{WH}$		250	500		250	830	ns	5	
			85	170		85	250	ns	10	
Clock Rise & Fall Time	$t_rCL=t_fCL$			15			15	μs	5	
				15			15	μs	10	
Clock Enable Set Up Time		350	175		700	175		ns	5	
		150	75		300	75		ns	10	
Maximum Clock Frequency	f_{CL}	1	2.5		0.6	2.5		MHz	5	
		3	5		2	5		MHz	10	
Input Capacitance	C_I		5			5		pF		Any Input
RESET OPERATION										
Carry Out Line Propagation Delay Time	$t_{PHL}=t_{PLH}$		300	900		300	1200	ns	5	
			125	250		125	500	ns	10	
Decade Out Line	$t_{PHL}=t_{PLH}$		500	1250		500	2500	ns	5	
			200	400		200	800	ns	10	
Minimum Reset Pulse Width			150	300		150	600	ns	5	
			75	150		75	300	ns	10	

Typical Characteristics



Waveform



HD-4023A

Triple 3-Input "NAND" Gate

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- SINGLE POWER SUPPLY OPERATION
- EFFECTIVE STATIC CHARGE PROTECTION

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

The HD-4023 is a small scale CMOS integrated circuit providing the system designer with basic gate building blocks for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power dissipation, high noise immunity, nearly symmetric output rise and fall times, and wide power supply operating voltage range.

Truth Table

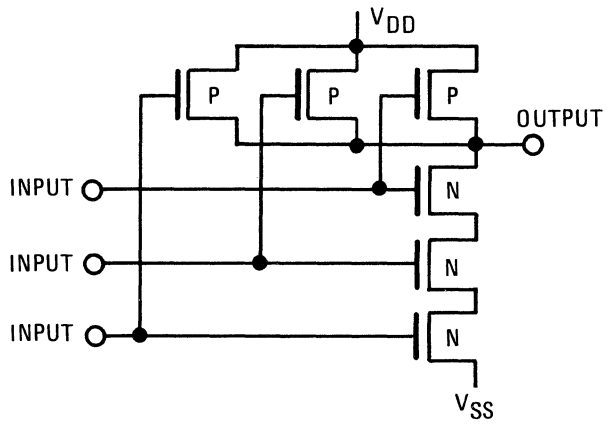
INPUTS			OUTPUT
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

X = DON'T CARE

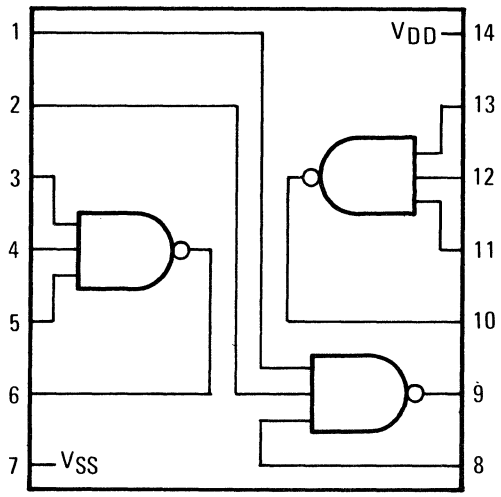
LOGIC "1" $\longrightarrow V_{DD}$

LOGIC "0" $\longrightarrow V_{SS}$

Circuit Diagram



Connection Diagram



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package	HD-4023A-2	200mW
Operating Temperature Range:	HD-4023A-9	-55°C to +125°C
		-40°C to +85°C

ELECTRICAL CHARACTRISTICS (STATIC)

D.C.

PARAMETER	SYM.	HD-4023A-2 -55°C MIN.	-55°C TYP.	-55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C TYP.	+125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
	I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
Quiescent Power Supply Current	I_{DD}			.05 .10		.001 .001	.05 .10			3 6	μA μA	5 10	
Output Drive Current	I_{OL}	.31 .62			.25 .5	.5 .6		.175 .35			mA mA	5 10	$V_{OL} = .5$VDC $V_{OL} = .5$VDC
	I_{OH}	-.31 -.75			-.25 -.6	-.5 -1.2		-.175 -.4			mA mA	5 10	$V_{OH} = 4.5$VDC $V_{OH} = 9.5$VDC
Input Capacitance						5					pF		

D.C.

PARAMETER	SYM.	HD-4023A-9 -40°C MIN.	-40°C TYP.	-40°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+85°C MIN.	+85°C TYP.	+85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
	I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6$VDC $V_{OH} \geq 7.2$VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95$VDC $V_{OL} \leq 2.9$VDC
Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
Quiescent Power Supply Current	I_{DD}					.005 .005	.5 5			15 30	μA μA	5 10	
Output Drive Current	I_{OL}	.145 .3			.12 .25	.5 .6		.095 .2			mA mA	5 10	$V_{OL} = .5$VDC $V_{OL} = .5$VDC
	I_{OH}	-.145 -.35			-.12 -.3	-.5 -1.2		-.095 -.24			mA mA	5 10	$V_{OH} = 4.5$VDC $V_{OH} = 9.5$VDC
Input Capacitance						5					pF		

Specifications (continued)

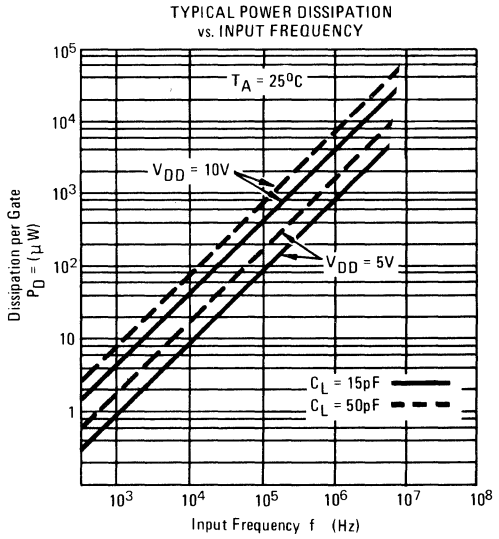
ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

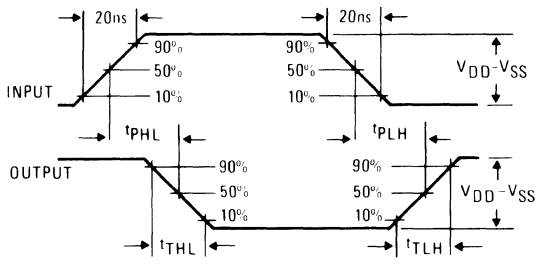
	PARAMETER	SYMBOL	HD-4023A-2 TYP.	HD-4023A-2 MAX.	HD-4023A-9 TYP.	HD-4023A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay	t_{PLH}	50 25	75 40	50 25	100 50	ns ns	5 10	Ref. to Switching Time Definitions $T_A = 25^oC$
		t_{PHL}	50 25	75 40	50 25	100 50	ns ns	5 10	
	Transition Time	t_{TLH}	75 40	100 60	75 40	125 75	ns ns	5 10	
		t_{THL}	75 50	125 75	75 50	150 100	ns ns	5 10	

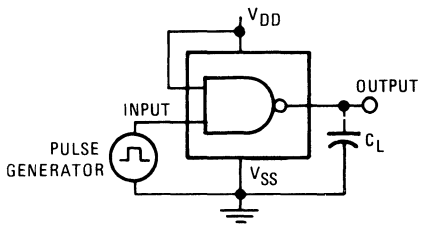
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

Typical Characteristics



Switching Time Definitions and Conditions





HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

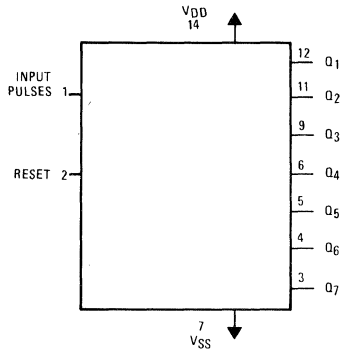
HD-4024A

7-Stage Binary Counter

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- MSI COMPLEXITY-SEVEN MASTER/SLAVE FLIP-FLOPS WITH ASSOCIATED BUFFERING ON A SINGLE CHIP
- FULLY STATIC OPERATION
- BUFFERED RESET INPUT FOR LOW CAPACITANCE AND HIGH NOISE IMMUNITY
- CLOCK RATE 7MHz(typ.) V_{DD}-V_{SS} = 10V

Connection Diagram



Description

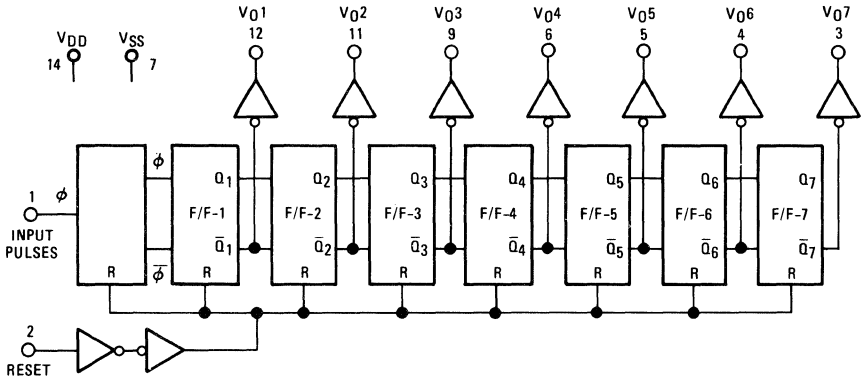
The HD-4024 is a 7-stage binary counter. Input pulse shaping and reset buffering are provided on chip. Application of a high logic level to the reset input resets all counter stages to "zero". The counter advances one count during the negative going transition of the input pulse.

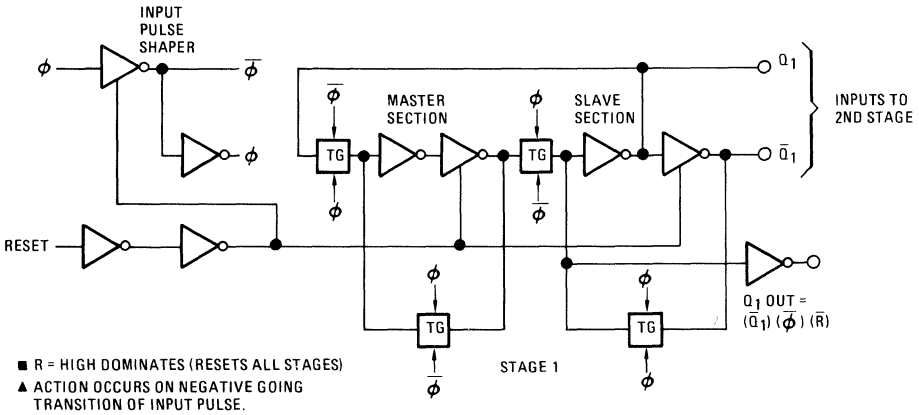
Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Logic Diagrams





■ R = HIGH DOMINATES (RESETS ALL STAGES)
▲ ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE.

EQUATIONS FOR STAGES 2 TO 7

Q_2 OUT = $(\bar{Q}_2)(Q_1)(\blacktriangle\bar{\phi})(\bar{R})$
Q_3 OUT = $(\bar{Q}_3)(Q_1)(Q_2)(\blacktriangle\bar{\phi})(\bar{R})$
Q_4 OUT = $(\bar{Q}_4)(Q_1)(Q_2)(Q_3)(\blacktriangle\bar{\phi})(\bar{R})$
Q_5 OUT = $(\bar{Q}_5)(Q_1)(Q_2)(Q_3)(Q_4)(\blacktriangle\bar{\phi})(\bar{R})$
Q_6 OUT = $(\bar{Q}_6)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(\blacktriangle\bar{\phi})(\bar{R})$
Q_7 OUT = $(\bar{Q}_7)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(Q_6)(\blacktriangle\bar{\phi})(\bar{R})$

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4024A-2	-55°C to +125°C
	HD-4024A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4024A-2											
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	N-Channel Output Drive Current	I_{DN}	0.31 0.62			0.25 0.5	0.5 1		0.175 0.35			mA mA	5 10	
	P-Channel	I_{DP}	-0.19 -0.45			-0.15 -0.35	-0.3 -0.7		-0.105 -0.25			mA mA	5 10	
	Quiescent Device Current	I_L			5 10		0.3 0.5	5 10			300 600	μA μA	5 10	
	Quiescent Device Dissipation/Package	P_D			25 100		1.5 5	25 100			1500 6000	μW μW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

			HD-4024A-9											
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	N-Channel Output Drive Current	I_{DN}	0.15 0.31			0.12 0.25	0.5 1		0.095 0.2			mA mA	5 10	V_O = 0.5 V_O = 0.5
	P-Channel	I_{DP}	-0.145 -0.31			-0.12 -0.25	-0.3 -0.7		0.095 -0.2			mA mA	5 10	V_O = 4.5 V_O = 9.5
	Quiescent Device Current	I_L			50 100		0.5 1	50 100			700 1400	μA μA	5 10	
	Quiescent Device Dissipation/Package				250 1000		2.5 10	250 1000			3500 14000	μW μW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

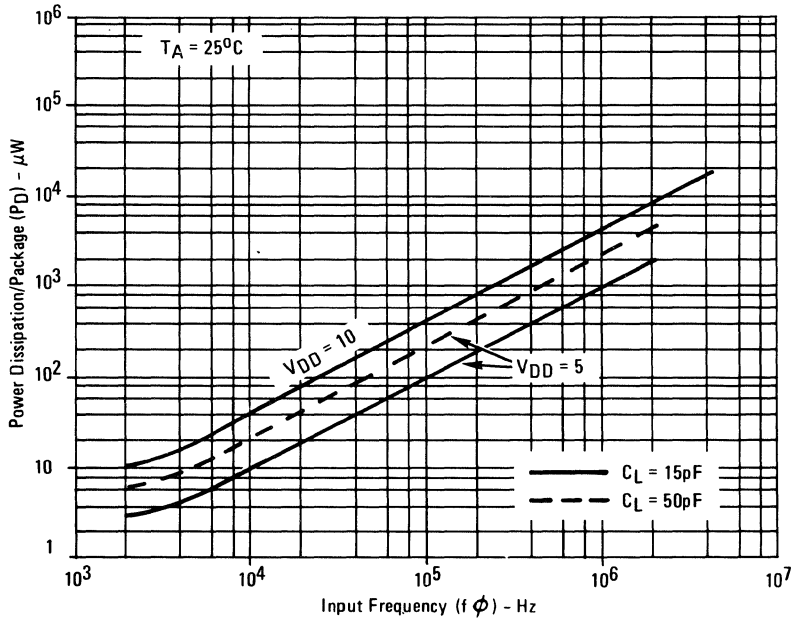
Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	HD-4024A-2 MIN.	HD-4024A-2 TYP.	HD-4024A-2 MAX.	HD-4024A-9 MIN.	HD-4024A-9 TYP.	HD-4024A-9 MAX.	UNITS	V_{DD}
A.C.	INPUT OPERATION									
	Propagation Delay Time	t_{PHL}, t_{PLH}		175 80	350 125		175 80	400 150	ns ns	5 10
	Transition Time	t_{THL}, t_{TLH}		175 80	225 125		175 80	250 150	ns ns	5 10
	Minimum Input Pulse Width	t_{WL}, t_{WH}		200 140	330 125		200 140	500 165	ns ns	5 10
	Input Pulse Rise & Fall Time	t_rO t_fO			15 10			15 10	μs μs	5 10
	Maximum Input Pulse Frequency	fO	1.5 4	2.5 7		1 3	2.5 7		MHz MHz	5 10
	Input Capacitance	C_I		5			5		pF	
	RESET OPERATION									
	Propagation Delay Time	$t_{PHL(R)}$		500 250	700 350		500 250	800 400	ns ns	5 10
	Minimum Reset Pulse Width	$t_{WH(R)}$		375 200	500 300		375 200	600 350	ns ns	5 10

Typical Characteristics



HD-4025A

Triple 3-Input "NOR" Gate

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC.
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE.
- SINGLE POWER SUPPLY OPERATION.
- EFFECTIVE STATIC CHARGE PROTECTION.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

HD-4025 is a small scale CMOS integrated circuit providing the system designer with basic gate building blocks for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power consumption, high noise immunity, nearly symetric output rise and fall times and wide power supply operating range.

Truth Table

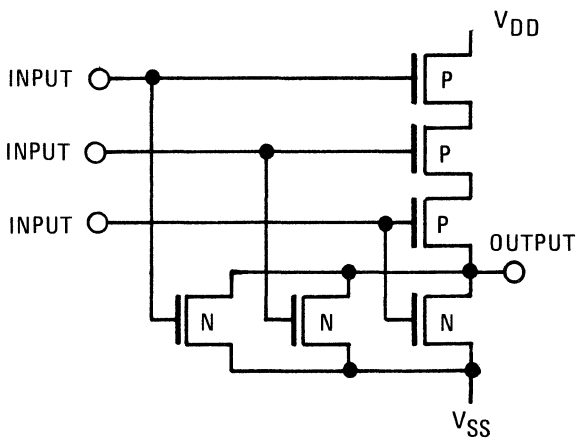
INPUTS			OUTPUTS
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

LOGIC "1" → V_{DD}

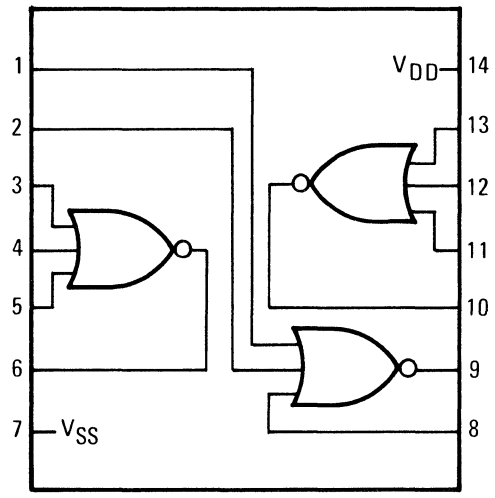
LOGIC "0" → V_{SS}

X = DON'T CARE

Circuit Diagram



Connection Diagram



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		$-65^{o}C$ to $+150^{o}C$
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4025A-2	$-55^{o}C$ to $+125^{o}C$
	HD-4025A-9	$-40^{o}C$ to $+85^{o}C$

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4025A-2											
			-55°C			+25°C			+125°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6VDC$ $V_{OH} \geq 7.2VDC$
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95VDC$ $V_{OL} \leq 2.9VDC$
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			.05 .10		.001 .001	.05 .10			3 6	μA μA	5 10	
	Output Drive Current	I_{OL}	0.5 1.1			.4 .9	1 2.5		.28 .65			mA mA	5 10	$V_{OL} = .4VDC$ $V_{OL} = .5VDC$
		I_{OH}	-.62 -.62			-.5 -.5	-2 -1		-.35 -.35			mA mA	5 10	$V_{OH} = 2.5VDC$ $V_{OH} = 9.5VDC$
	Input Capacitance						5					pF		

			HD-4025A-9											
			-40°C			+25°C			+85°C				CONDITIONS	
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
		I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
	Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.6VDC$ $V_{OH} \geq 7.2VDC$
		V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq .95VDC$ $V_{OL} \leq 2.9VDC$
	Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ $I_O = 0A$
		V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ $I_O = 0A$
	Quiescent Power Supply Current	I_{DD}			0.5 5		.005 .005	0.5 5			15 30	μA μA	5 10	
	Output Drive Current	I_{OL}	.35 .72			.3 .6	1 2.5		.24 .48			mA mA	5 10	$V_{OL} = .4VDC$ $V_{OL} = .5VDC$
		I_{OH}	-.35 -.3			-.3 -.25	-2 -1		-.24 -.2			mA mA	5 10	$V_{OH} = 2.5VDC$ $V_{OH} = 9.5VDC$
	Input Capacitance						5					pF		

Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

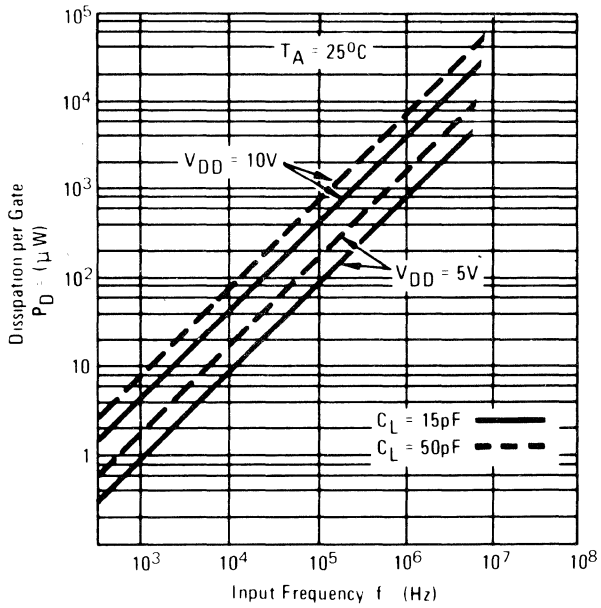
$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	HD-4025A-2 TYP.	HD-4025A-2 MAX.	HD-4025A-9 TYP.	HD-4025A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay	t_{PLH}	35 25	95 45	35 25	120 65	ns ns	5 10	Ref. to Switching Time Definitions
		t_{PHL}	35 25	50 40	35 25	80 55	ns ns	5 10	
	Transition Time	t_{TLH}	65 35	175 75	65 35	300 125	ns ns	5 10	
		t_{THL}	65 35	125 70	65 35	200 115	ns ns	5 10	

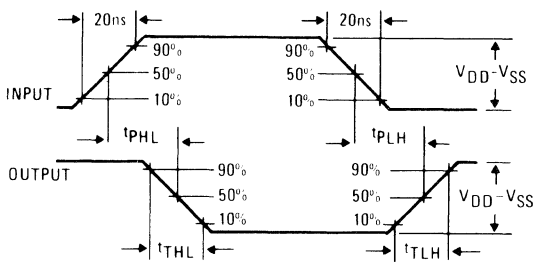
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

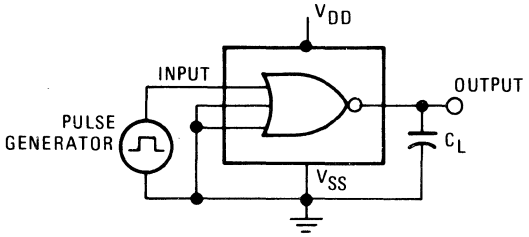
Typical Characteristics

TYPICAL POWER DISSIPATION vs. INPUT FREQUENCY



Switching Time Definitions and Conditions





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HD-4027A

Dual J-K Master-Slave Flip-Flop

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- FULLY STATIC OPERATION
- INDEPENDENT SET AND RESET
- BUFFERED OUTPUTS

Description

The HD-4027 consists of two "J-K" flip-flops with independent clock, set, and reset inputs. Buffered Q and $\overline{Q}$ outputs are available from both flip-flops.

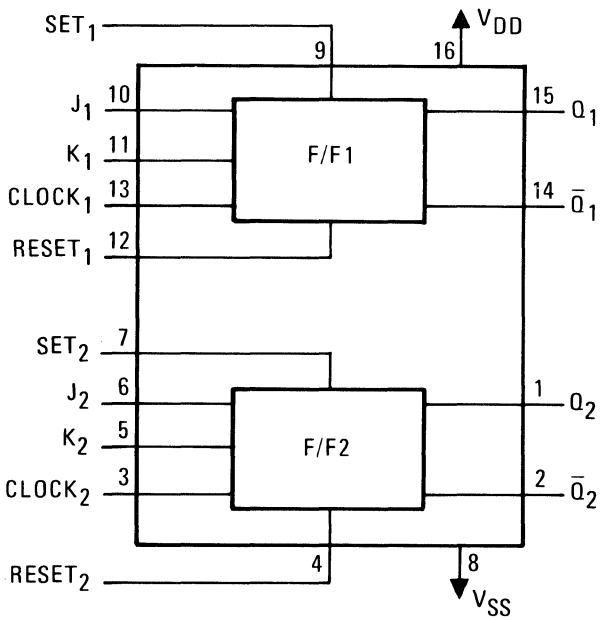
Flip-flop state changes are synchronous with a positive going clock signal. Setting or resetting either flip-flop occurs when a "high" is applied at its respective set or reset input.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Connection Diagram



Truth Table

PRESENT STATE					CL▲	NEXT STATE		
INPUTS				OUTPUT		OUTPUTS		
J	K	S	R	Q		Q	$\overline{Q}$	
1	X	0	0	0	⌒	1	0	
X	0	0	0	1	⌒	1	0	
0	X	0	0	0	⌒	0	1	
X	1	0	0	1	⌒	0	1	
X	X	0	0	X	⌣			←NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	1	1	

Where: 1 = HIGH LEVEL 0 = LOW LEVEL

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD}-V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		$-65^{o}C$ to $+150^{o}C$
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4027A-2	$-55^{o}C$ to $+125^{o}C$
	HD-4027A-9	$-40^{o}C$ to $+85^{o}C$

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4027A-2											
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		Any Input
	Noise Immunity (All Inputs)	V_{NL}	1.5 3.0			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3.0			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	N-Channel Output Drive Current	I_{DN}	0.63 1.25			0.5 1	1 2.5		0.33 0.7			mA mA	5 10	V_O = 0.5V V_O = 0.5V
	P-Channel	I_{DP}	-0.31 -0.8			-0.25 -0.65	-0.5 -1.3		-0.175 -0.45			mA mA	5 10	V_O = 4.5V V_O = 9.5V
	Quiescent Device Current	I_L			1 2		0.005 0.005	1 2			60 120	μA μA	5 10	
	Quiescent Device Dissipation/Package	P_D			5 20		0.025 0.05	5 20			300 1200	W W	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

			HD-4027A-9											
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		Any Input
	Noise Immunity (All Inputs)	V_{NL}	1.5 3.0			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3.0			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	N-Channel Output Drive Current	I_{DN}	0.3 0.72			0.3 0.6	1 2.5		0.24 0.5			mA mA	5 10	V_O = 0.5 V_O = 0.5
	P-Channel	I_{DP}	-0.17 -0.4			-0.14 -0.33	-0.5 -1.3		-0.063 -0.27			mA mA	5 10	V_O = 4.5 V_O = 9.5V
	Quiescent Device Current	I_L			10 20		0.01 0.05	10 20			140 280	μA μA	5 10	
	Quiescent Device Dissipation/Package	P_D			50 200		0.05 0.5	50 200			700 2800	μW μW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

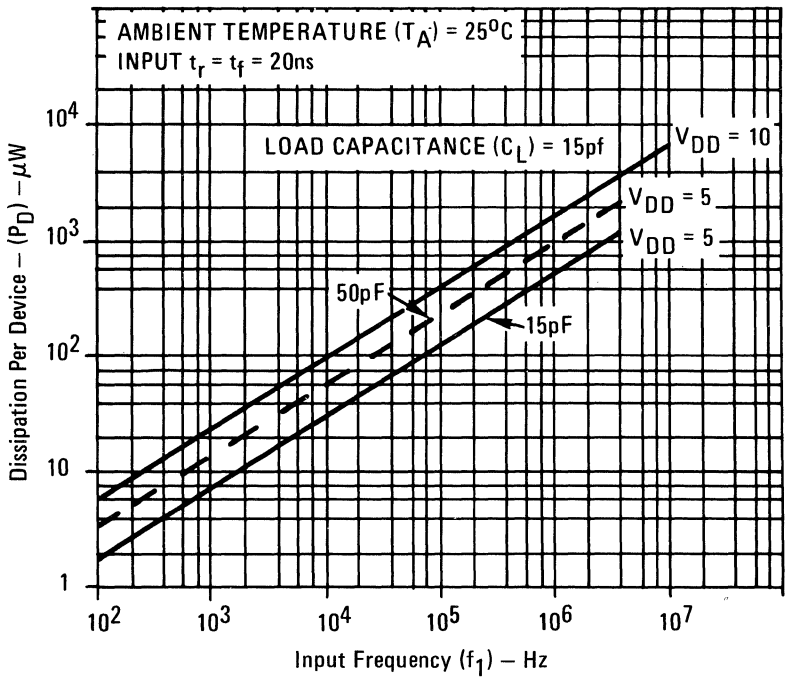
Specifications

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	HD-4027A-2 MIN.	HD-4027A-2 TYP.	HD-4027A-2 MAX.	HD-4027A-9 MIN.	HD-4027A-9 TYP.	HD-4027A-9 MAX.	UNITS	V_{DD}
A.C.	Propagation Delay Time	t_{PHL}, t_{PLH}		150 75	300 110		150 75	400 150	ns ns	5 10
	Transition Time	t_{THL}, t_{TLH}		75 50	125 70		75 50	250 140	ns ns	5 10
	Minimum Clock Pulse Width	t_{WL}, t_{WH}		165 65	330 110		165 65	500 165	ns ns	5 10
	Clock Rise & Fall Time	t_rCL, t_fCL			15 5			15 5	μs μs	5 10
	Set Up Time			70 25	150 50		70 25	200 75	ns ns	5 10
	Maximum Clock Frequency (Toggle Mode)	fCL	1.5 4.5	3 8		1 3	3 8		MHz MHz	5 10
	Input Capacitance	C_I		5			5		pF	
	SET & RESET OPERATION Propagation Delay Time	$t_{PHL(R)}$ $t_{PLH(S)}$		175 75	225 110		175 75	350 150	ns ns	5 10
	Minimum Set and Reset Pulse Widths	$t_{WH(S)}$ $t_{WL(R)}$		125 50	200 80		125 50	300 120	ns ns	5 10

Typical Characteristics



HD-4028A

BCD-to-Decimal Decoder

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY AND LOW QUIESCENT POWER DISSIPATION
- MSI COMPLEXITY – A COMPLETE BCD TO DECIMAL DECODER WITH OUTPUT BUFFERING
- BCD TO DECIMAL OR BINARY TO OCTAL DECODING

Description

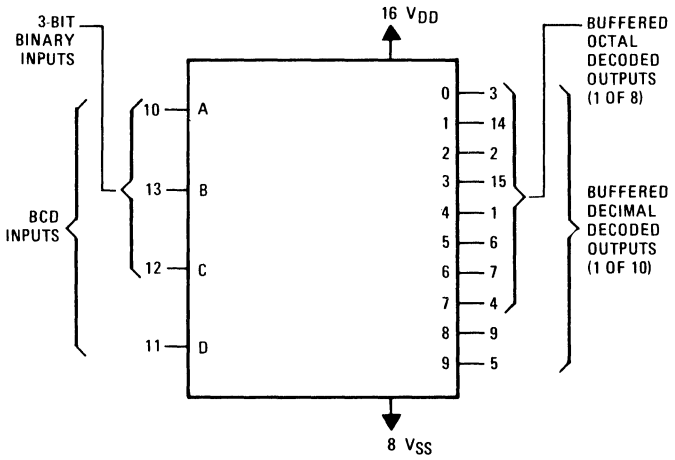
The HD-4028 is a BCD - decimal decoder or binary to octal decoder. Application of BCD at inputs A, B, C, and D will result in 1 of 10 outputs being decoded as defined in the truth table. Octal code will be decoded at outputs 0 to 7 with a 3-bit binary code applied to inputs A, B, and C and input D held "low". An output, when decoded, will be "high" with all other outputs "low".

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

Connection Diagram

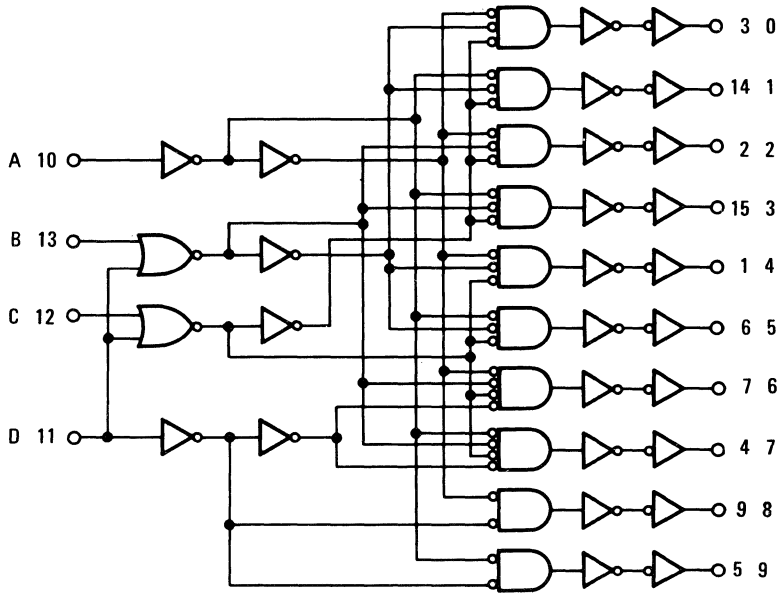


Truth Table

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

Where: 1 = High Level
0 = Low Level

Logic Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4028A-2	-55°C to +125°C
	HD-4028A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4028A-2											
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		Any Input
D.C.	Noise Immunity (All Inputs)	V_{NL}	1.5 3.0			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.95 V_O = 2.9
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3.0			V V	5 10	V_O = 3.6 V_O = 7.2
	N-Channel Output Drive Current	I_{DN}	0.75 1.5			0.6 1.2	1.2 2.4		0.45 0.9			mA mA	5 10	V_O = 0.5 V_O = 0.5
	P-Channel	I_{DP}	-0.7 -1.4			-0.45 -0.95	-0.9 -1.9		-0.32 -0.65			mA mA	5 10	V_O = 4.5V V_O = 9.5V
	Quiescent Device Current	I_L			5 10		0.5 1	5 10			300 600	µA µA	5 10	
	Quiescent Device Dissipation/Package	P_D			25 100		2.5 10	25 100			1500 6000	µW µW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

			HD-4028A-9											
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		Any Input
D.C.	Noise Immunity (All Inputs)	V_{NL}	1.5 3.0			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.95 V_O = 2.9
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3.0			V V	5 10	V_O = 3.6 V_O = 7.2
	N-Channel Output Drive Current	I_{DN}	0.35 0.7			0.3 0.6	1.2 2.4		0.25 0.5			mA mA	5 10	V_O = 0.5V V_O = 0.5V
	P-Channel	I_{DP}	-0.32 -0.65			-0.22 -0.48	-0.9 -1.9		-0.18 -0.4			mA mA	5 10	V_O = 4.5V V_O = 9.5V
	Quiescent Device Current	I_L			50 100		5 10	50 100			700 1400	µA µA	5 10	
	Quiescent Device Dissipation/Package				250 100		25 100	250 1000			3500 14000	µW µW	5 10	
	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	HD-4028A-2 MIN.	HD-4028A-2 TYP.	HD-4028A-2 MAX.	HD-4028A-9 MIN.	HD-4028A-9 TYP.	HD-4028A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay Time	t_{PHL}, t_{PLH}		250 100	480 180		250 100	700 290	ns ns	5 10	
	Transition Time	t_{THL}, t_{TLH}		60 30	150 75		60 30	300 150	ns ns	5 10	
	Input Capacitance	C_I		5			5		pF		Any Input

HARRIS SEMICONDUCTOR
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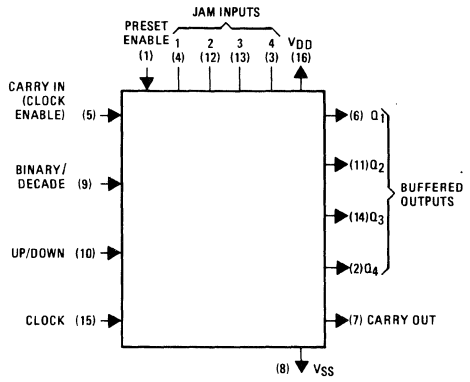
HD-4029A

Presettable Up/Down Counter

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY AND LOW QUIESCENT POWER DISSIPATION
- MSI COMPLEXITY – A 4-BIT COUNTER WITH ASSOCIATED CONTROL AND CARRY "LOOK" AHEAD CIRCUITRY
- FUNCTIONAL FLEXIBILITY – BINARY/BCD DECADE, UP/DOWN COUNTING, MULTI PACKAGE SYNCHRONOUS OR RIPPLE OPERATION
- LOADABLE TO ANY DESIRED STATE

Connection Diagram



Description

The HD-4029 is a four stage counter capable of counting up or down in either binary or BCD decade modes. Levels preset on the Jam inputs are loaded into the counter asynchronously with the clock when the Preset Enable input is "high". "Look ahead" carry capabilities are provided to facilitate high speed operation where two or more HD-4029's are used in parallel.

The counter toggles one count on the positive going clock input when the carry input and preset enable inputs are "low". If either carry input or preset enable are "high" clocking is inhibited.

The carry out signal is normally high, going low for one clock cycle under the following conditions providing the Carry Input signal is low:

The counter has reached its maximum count in the "Up" mode.

The counter has reached its minimum count in the "Down" mode.

The carry input signal functions as a clock enable permitting the counter to toggle only when "low". If the carry input is not used it must be tied to V_{SS}.

Operating modes for the HD-4029 are selected as follows:

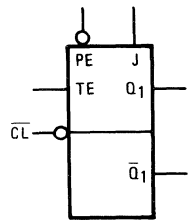
Binary/Decade input "high"	Binary Counter
Binary/Decade input "low"	Decade Counter
Up/Down input "high"	"Up" Counter
Up/Down Input "low"	"Down" Counter

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

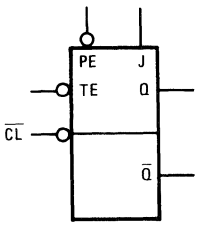
See package outline Code 1W and Code 9L.

Truth Tables



CLOCK	TE	PE	J	Q	Q̄
X	X	0	0	0	1
⌊	1	1	X	Q̄	Q
X	X	0	1	1	Q
⌊	0	1	X	Q	Q̄ NC
⌋	X	1	X	Q	Q̄ NC

NC – No Change
TE – Toggle Enable
X – Don't Care



CLOCK	TE	PE	J	Q	Q̄
X	X	0	0	0	1
⌊	0	1	X	Q̄	Q
X	X	0	1	1	0
⌊	1	1	X	Q	Q̄ NC
⌋	X	1	X	Q	Q̄ NC

NC – No Change
TE – Toggle Enable
X – Don't Care

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
CARRY IN (CI) (CLOCK ENABLE)	1	NO COUNTER ADVANCE AT POS CLOCK TRANSITION
	0	ADVANCE COUNTER AT POS CLOCK TRANSITION

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4029A-2	-55°C to +125°C
	HD-4029A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4029A-2											
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN..	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		Any Input
	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3.0			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	N-Channel Output Drive Current	I_{DN}	0.5 0.74			0.4 0.6	0.8 1.2		0.28 0.42			mA mA	5 10	V_O = 0.5 Q V_O = 0.5 Outputs
			0.1 0.4			0.08 0.32	0.16 0.64		0.06 0.22			mA mA	5 10	V_O = 0.5 Carry V_O = 0.5 Output
	P-Channel	I_{DP}	-0.18 -0.3			-0.12 -0.2	-0.24 -0.4		-0.08 -0.14			mA mA	5 10	V_O = 4.5 Q V_O = 9.5 Outputs
			-0.09 -0.15			-0.06 -0.1	-0.12 -0.2		-0.04 -0.07			mA mA	5 10	V_O = 4.5 Carry V_O = 9.5 Output
	Quiescent Device Current	I_L			5 10		0.3 0.5	5 10			300 600	μA μA	5 10	
	Quiescent Device Dissipation/Package	P_D			25 100		1.5 5	25 100			1500 6000	μW μW	5 10	
	Output Voltage Low Level	V_{OL}			0.01 0.01			0.01 0.01			0.05 0.05	V V	5 10	
	Output Voltage High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

			HD-4029A-9											
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
	Input Leakage	I_I					10					pA		Any Input
	Noise Immunity (All Inputs)	V_{NL}	1.5 3.0			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1.0
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3.0			V V	5 10	V_O = 4.2 V_O = 9.0
D.C.	N-Channel Output Drive Current	I_{DN}	0.24 0.36			0.2 0.3	0.8 1.2		0.16 0.24			mA mA	5 10	V_O = 0.5 Q V_O = 0.5 Outputs
			0.05 0.19			0.04 0.16	0.16 0.64		0.03 0.13			mA mA	5 10	V_O = 0.5 Carry V_O = 0.5 Output
	P-Channel	I_{DP}	-0.07 -0.14			-0.06 -0.1	-0.24 -0.4		-0.05 -0.08			mA mA	5 10	V_O = 4.5 Q V_O = 9.5 Outputs
			-0.04 -0.07			-0.03 -0.05	-0.12 -0.2		-0.02 -0.04			mA mA	5 10	V_O = 4.5 Carry V_O = 9.5 Output
	Quiescent Device Current	I_L			50 100		0.5 1	50 100			700 1400	μA μA	5 10	
	Quiescent Device Dissipation/Package	P_D			250 1000		2.5 10	250 1000			3500 14000	μW μW	5 10	
	Output Voltage Low Level	V_{OL}			0.01 0.01			0.01 0.01			0.05 0.05	V V	5 10	
	Output Voltage High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

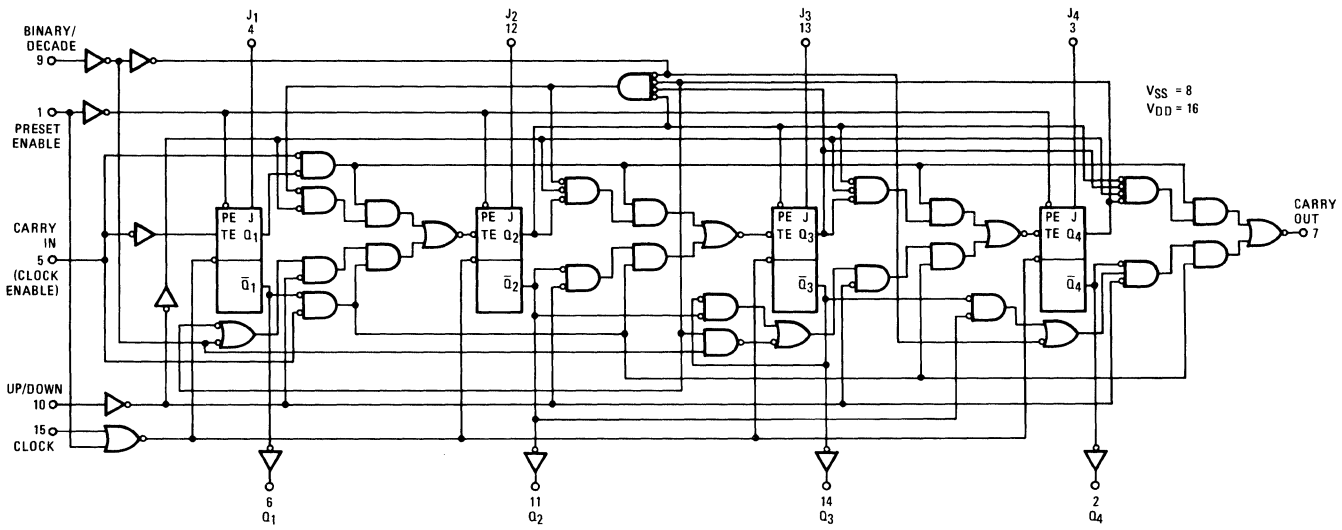
Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

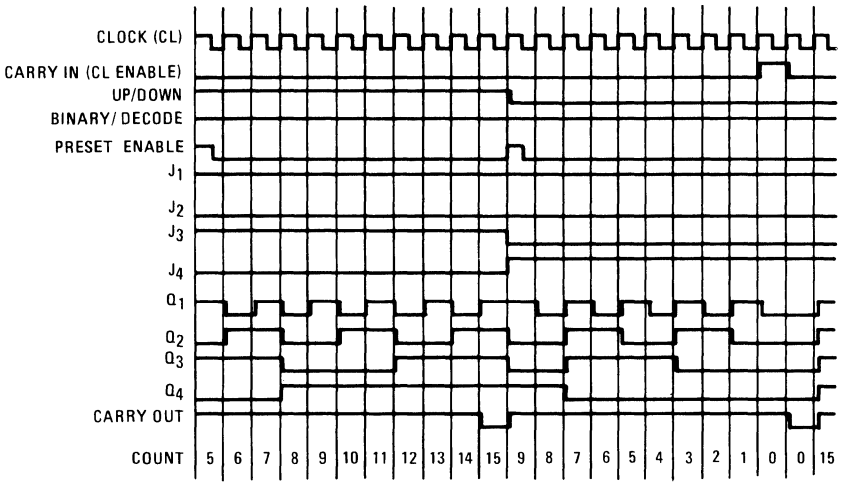
$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

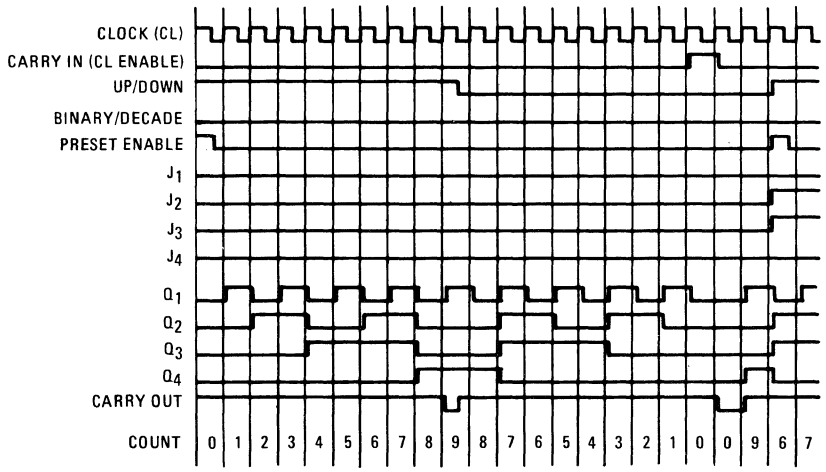
	PARAMETER	SYMBOL	HD-4029A-2 MIN.	HD-4029A-2 TYP.	HD-4029A-2 MAX.	HD-4029A-9 MIN.	HD-4029A-9 TYP.	HD-4029A-9 MAX.	UNITS	V_{DD}
A.C.	CLOCKED OPERATION									
	Q Outputs Propagation Delay Time	t_{PHL}, t_{PLH}		325 115	650 230		325 115	1300 460	ns ns	5 10
	Carry Output Propagation Delay Time	t_{PHL}, t_{PLH}		425 150	850 300		425 150	1700 600	ns ns	5 10
	Q Outputs Transition Time	t_{THL}, t_{TLH}		100 50	200 100		100 50	400 200	ns ns	5 10
	Carry Output Transition Time	t_{THL}, t_{TLH}		200 100	400 200		200 100	800 400	ns ns	5 10
	Minimum Clock Pulse Width	t_{WL}, t_{WH}		200 100	340 170		200 100	500 250	ns ns	5 10
	Clock Rise & Fall Time	t_rCL, t_fCL			15 15			15 15	μs μs	5 10
	Set Up Times	t_{SHL}, t_{SLH}		325 115	650 230		325 115	1300 460	ns ns	5 10
	Maximum Clock Frequency	f_{CL}	1.5 3	2.5 5		1 2	2.5 5		MHz MHz	5 10
	Input Capacitance	C_I		5			5		pA	
	PRESET ENABLE									
	Q Outputs Propagation Delay Time	t_{PHL}, t_{PLH}		325 115	650 230		325 115	1300 460	ns ns	5 10
	Carry Output Propagation Delay Time	t_{PHL}, t_{PLH}		425 150	850 300		425 150	1700 600	ns ns	5 10
	Reset Enable Pulse Width	t_{WH}		115 80	330 160		115 80	660 320	ns ns	5 10
	Preset Enable Removal Time	t_{rem}		325 115	650 230		325 115	1300 460	ns ns	5 10
	CARRY INPUT Propagation Delay Time Carry Output	t_{PHL}, t_{PLH}		175 50	350 100		175 50	700 200	ns ns	5 10

Logic Diagrams

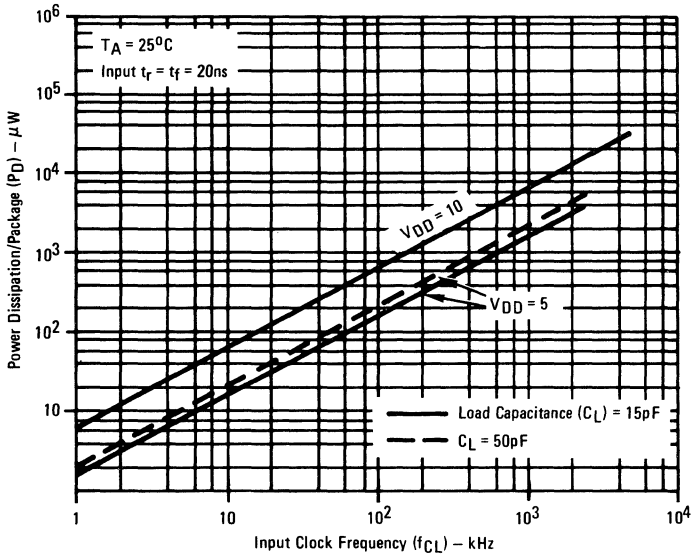


Waveforms





Typical Characteristics



HARRIS SEMICONDUCTOR
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HD-4030A

Quad Exclusive "OR" Gate

Features

- POWER SUPPLY OPERATING RANGE +3VDC TO +15VDC
- NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- SINGLE POWER SUPPLY OPERATION
- EFFECTIVE STATIC CHARGE PROTECTION

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

Description

HD-4030 is a small scale CMOS integrated circuit providing the system designer with basic gate building blocks for configuring more complex logic functions. The CMOS technology and design parameters employed result in low quiescent power consumption, high noise immunity, nearly symetric output rise and fall times and wide power supply operating range.

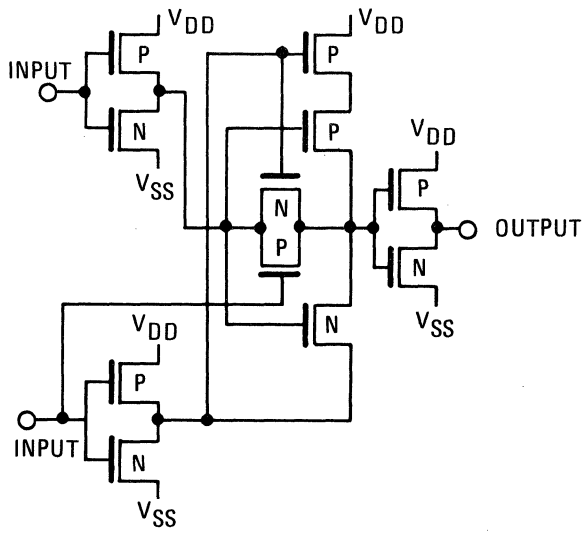
Truth Table

INPUTS		OUTPUT
0	0	0
0	1	1
1	0	1
1	1	0

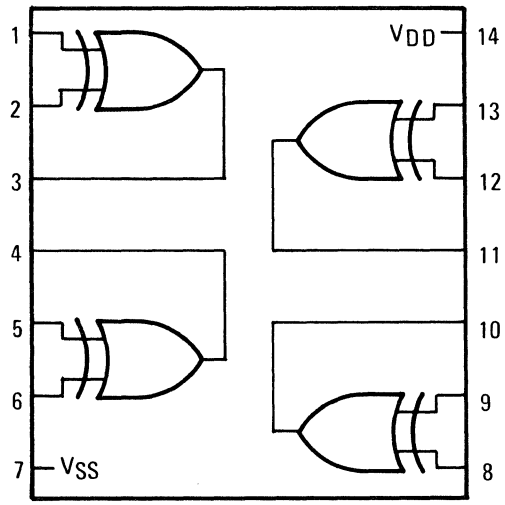
LOGIC "1" → V_{DD}

LOGIC "0" → V_{SS}

Circuit Diagram



Connection Diagram



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq$ V_{DD} +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4030A-2	-55°C to +125°C
	HD-4030A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

D.C.

PARAMETER	SYM.	HD-4030A-2 -55°C MIN.	-55°C TYP.	-55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C TYP.	+125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
	I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OL} \leq$ .95VDC $V_{OL} \leq$ 2.9VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OH} \geq$ 3.6VDC $V_{OH} \geq$ 7.2VDC
Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ I_O = 0A
	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ I_O = 0A
Quiescent Power Supply Current	I_{DD}			.5 1		.005 .01	0.5 1			30 60	μA μA	5 10	
Output Drive Current	I_{OL}	.75 1.5			.6 1.2	1.2 2.4		.45 .9			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.45 -.95			-.3 -.65	-.6 -1.3		-.21 -.45			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Input Capacitance						5					pF		

D.C.

PARAMETER	SYM.	HD-4030A-9 -40°C MIN.	-40°C TYP.	-40°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+85°C MIN.	+85°C TYP.	+85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}					10					pA	10	$V_{IL} = V_{SS}$
	I_{IH}					10					pA	10	$V_{IH} = V_{DD}$
Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OL} \leq$ .95VDC $V_{OL} \leq$ 2.9VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OH} \geq$ 3.6VDC $V_{OH} \geq$ 7.2VDC
Output Voltage	V_{OL}			.01 .01		0 0	.01 .01			.05 .05	V V	5 10	$V_{IH} = V_{DD}$ I_O = 0A
	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	$V_{IL} = V_{SS}$ I_O = 0A
Quiescent Power Supply Current	I_{DD}			5 10		.05 .10	5 10			70 140	μA μA	5 10	
Output Drive Current	I_{OL}	.35 .70			.3 .6	1.2 2.4		.25 .5			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.21 -.45			-.15 -.32	-.6 -1.3		-.12 -.25			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Input Capacitance						5					pF		

Specifications (continued)

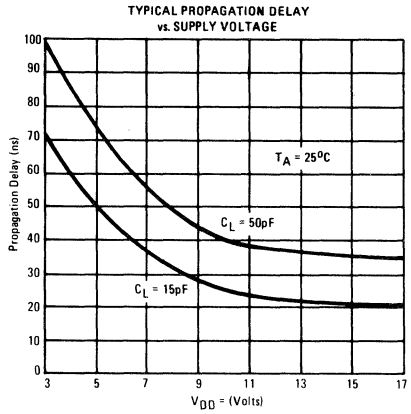
ELECTRICAL CHARACTERISTICS (DYNAMIC)

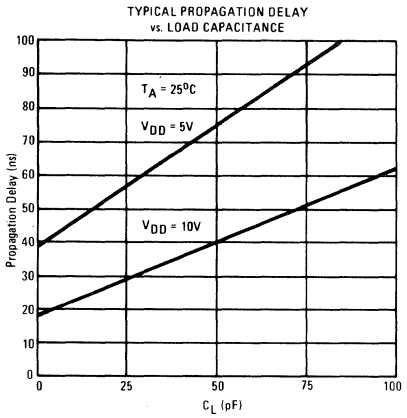
$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

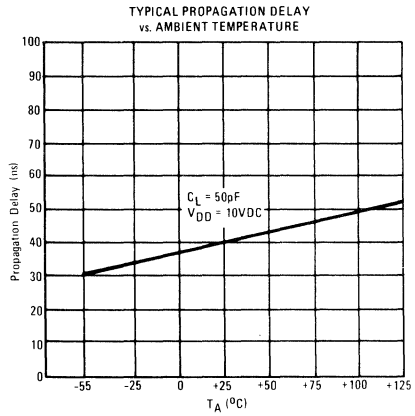
	PARAMETER	SYMBOL	HD-4030A-2 TYP.	HD-4030A-2 MAX.	HD-4030A-9 TYP.	HD-4030A-9 MAX.	UNITS	V_{DD}	NOTES
A.C.	Propagation Delay	t_{PLH}	100 40	200 100	100 40	300 150	ns ns	5 10	Ref. to Switching Time Definitions $T_A = 25^oC$
		t_{PHL}	100 40	200 100	100 40	300 150	ns ns	5 10	
	Transition Time	t_{TLH}	80 30	150 75	80 30	300 150	ns ns	5 10	
		t_{THL}	70 25	150 75	70 25	300 150	ns ns	5 10	

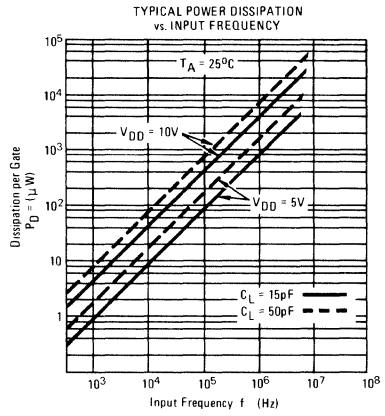
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

Typical Characteristics

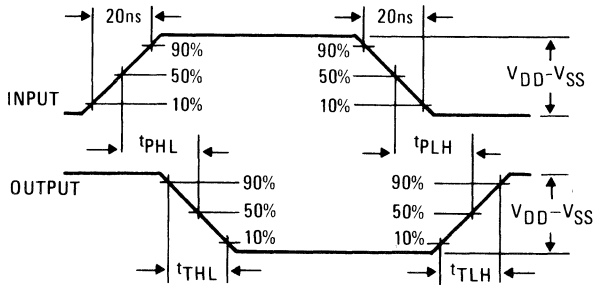


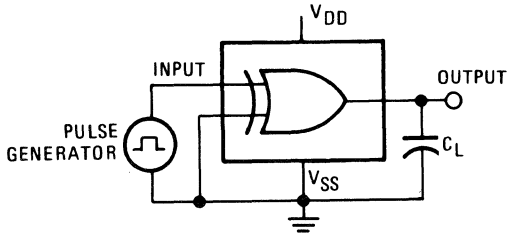






Switching Time Definitions and Conditions





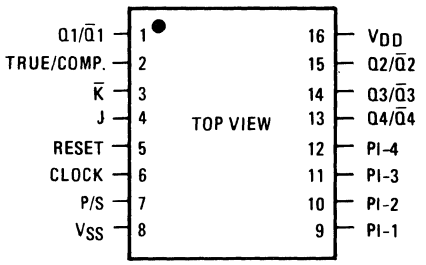
HD-4035A

4 Stage with J-K Input and True/Complement Output Shift Register

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- FULLY STATIC OPERATION
- J-$\overline{K}$ SERIAL INPUTS ON FIRST STAGE
- PARALLEL/SERIAL INPUT CONTROL
- TRUE/COMPLEMENT OUTPUT CONTROL
- BUFFERED OUTPUTS

Connection Diagram



Description

The HD-4035 is a four stage shift register capable of parallel input, serial input via J-$\overline{K}$ inputs and parallel output.

Data entry mode is controlled by the parallel/serial input. With P/S high, data is entered via the parallel inputs on the positive clock transition. Serial data is entered on the positive going clock with P/S low.

The True/complement input, when high, results in display of the true contents of the register at the outputs. When T/C is low, the complement of the register data is displayed.

The reset input, when high, asynchronously resets all four flip-flop stage.

Package

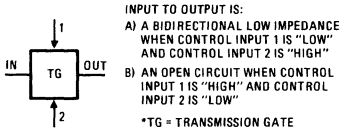
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and

See package outline Code 1U and Code 9V.

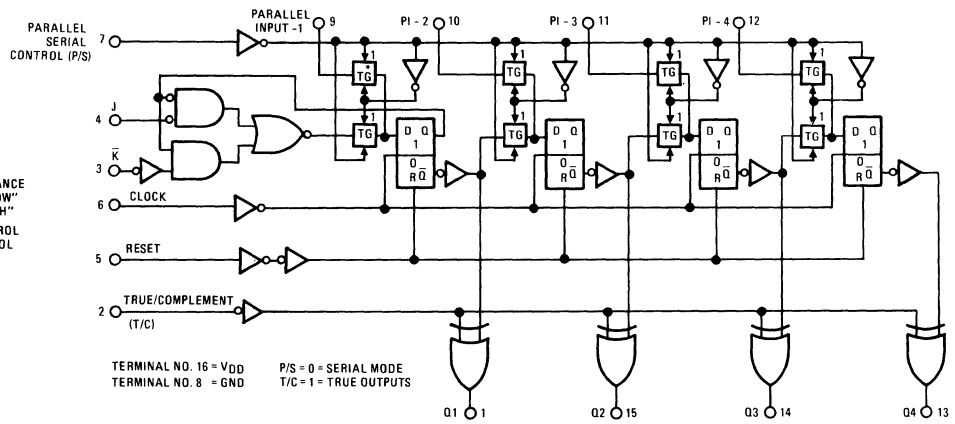
Truth Table

	$t_n - 1$ (INPUTS)				t_n (OUTPUTS)
CL	J	$\overline{K}$	R	$Q_n - 1$	Q_n
↑	0	X	0	0	0
↑	1	X	0	0	1
↑	X	0	0	1	0
↑	1	0	0	$Q_n - 1$	$\overline{Q_n - 1}$ TOGGLE MODE
↑	X	1	0	1	1
↓	X	X	0	$Q_n - 1$	$Q_n - 1$
X	X	X	1	X	0

Circuit Diagram



INPUT TO OUTPUT IS:
A) A BIDIRECTIONAL LOW IMPEDANCE WHEN CONTROL INPUT 1 IS "LOW" AND CONTROL INPUT 2 IS "HIGH"
B) AN OPEN CIRCUIT WHEN CONTROL INPUT 1 IS "HIGH" AND CONTROL INPUT 2 IS "LOW"
*TG = TRANSMISSION GATE



TERMINAL NO. 16 = V_{DD}
TERMINAL NO. 8 = GND
P/S = 0 = SERIAL MODE
T/C = 1 = TRUE OUTPUTS

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		$-65^{o}C$ to $+150^{o}C$
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4035A-2	$-55^{o}C$ to $+125^{o}C$
	HD-4035A-9	$-40^{o}C$ to $+85^{o}C$

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4035A-2											
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_I					10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8V V_O = 1V
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2V V_O = 9V
	Output Voltage Low Level	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	Output Voltage High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	
	Quiescent Device Current	I_L			5 10		0.3 0.5	5 10			300 600	µA µA	5 10	
	Quiescent Device Dissipation Package	P_D			25 100		1.5 5	25 100			1500 6000	µW µW	5 10	
	Output Drive Current N-Channel	I_{DN}	0.62 1.55			0.50 1.25	1 2.5		0.35 0.87			mA mA	5 10	V_O = 0.5V V_O = 0.5V
	Output Drive Current P-Channel	I_{DP}	-0.31 -0.81			-0.25 -0.65	-0.5 -1.3		-0.17 -0.45			mA mA	5 10	V_O = 4.5V V_O = 9.5V
	Input Capacitance	C_I					5					pF		Any Input

			HD-4035A-9											
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
D.C.	Input Leakage	I_I					10					pA		
	Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8V V_O = 1V
		V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2V V_O = 9V
	Output Voltage Low Level	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
	Output Voltage High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	
	Quiescent Device Current	I_L			50 100		0.5 1	50 100			700 1400	µA µA	5 10	
	Quiescent Device Dissipation Package	P_D			250 1000		2.5 10	250 1000			3500 14000	µW µW	5 10	
	Output Drive Current N-Channel	I_{DN}	0.43 1.05			0.35 0.85	1 2.5		0.24 0.59			mA mA	5 10	V_O = 0.5V V_O = 0.5V
	Output Drive Current P-Channel	I_{DP}	-0.2 -0.56			-0.18 -0.45	-0.5 -0.31		-0.12 -0.31			mA mA	5 10	V_O = 4.5V V_O = 9.5V
	Input Capacitance	C_I					5					pF		Any Input

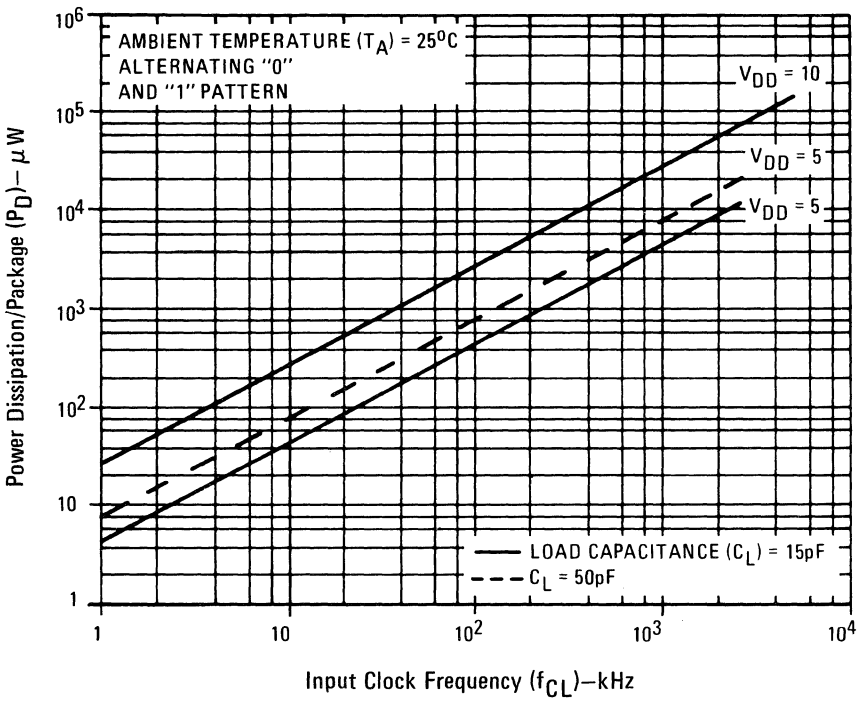
Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYM.	HD-4035A-2 MIN.	HD-4035A-2 TYP.	HD-4035A-2 MAX.	HD-4035A-9 MIN.	HD-4035A-9 TYP.	HD-4035A-9 MAX.	UNITS	V_{DD}
A.C.	CLOCKED OPERATION									
	Propagation Delay Time	t_{PLH}, t_{PHL}		250 100	500 200		250 100	700 300	ns ns	5 10
	Transition Time	t_{THL}, t_{TLH}		100 50	200 100		100 50	300 150	ns ns	5 10
	Minimum Clock Pulse Duration	t_{WL}, t_{WH}		200 100	335 165		200 100	500 250	ns ns	5 10
	Clock Rise & Fall Time	t_{rCL} t_{fCL}			15 5			15 5	μs μs	5 10
	J/$\overline{K}$ Lines Setup Time			250 100	500 200		250 100	750 250	ns ns	5 10
	Parallel-In Lines			100 50	350 80		100 50	500 100	ns ns	5 10
	Maximum Clock Frequency	f_{CL}	1.5 3	2.5 5		1 2	2.5 5		MHz MHz	5 10
	RESET OPERATION									
	Propagation Delay Time	t_{PHL}, t_{PLH}		250 100	500 200		250 100	700 300	ns ns	5 10
	Minimum Reset Pulse Duration	t_{WL}, t_{WH}		200 100	400 175		200 100	500 200	ns ns	5 10

Typical Characteristics



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-4040A

12-Stage Ripple-Carry Binary Counter/Divider

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- MSI COMPLEXITY– 12 COUNTER STAGES WITH INPUT PULSE SHAPING AND OUTPUT BUFFERING CIRCUITRY
- FULLY STATIC OPERATION
- BUFFERED INPUTS AND OUTPUTS
- LOW POWER TTL COMPATIBLE

Package

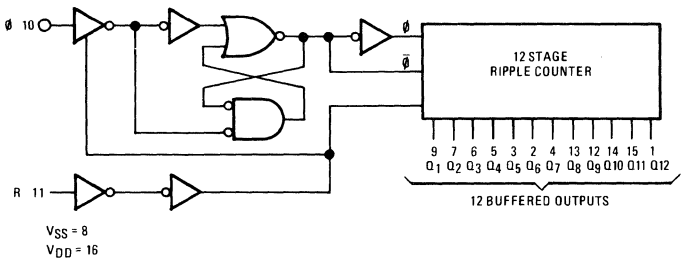
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1W and Code 9L.

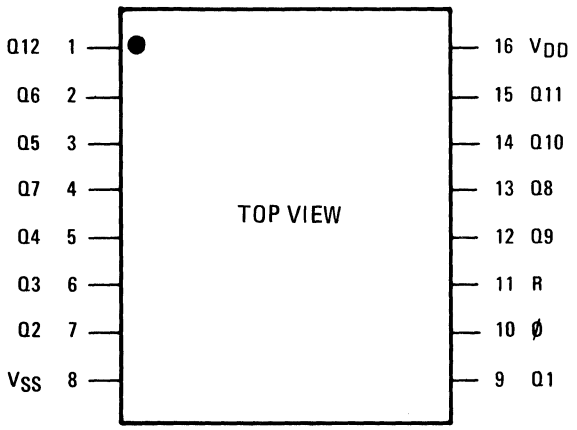
Description

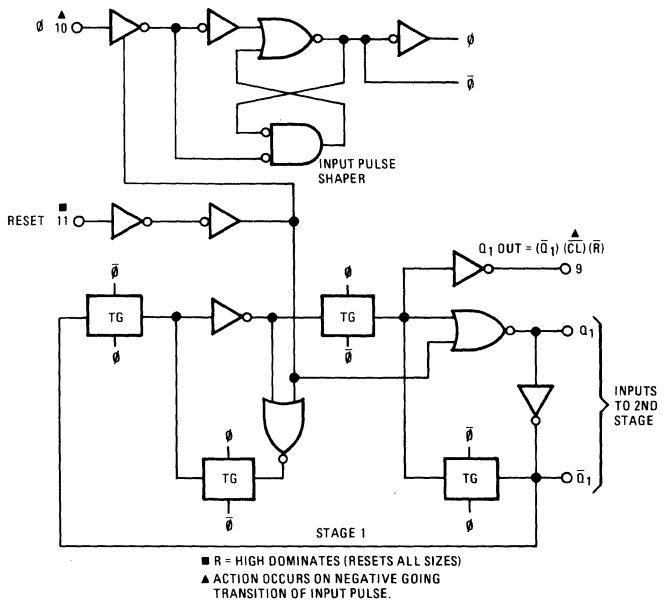
The HD-4040 is a 12-bit ripple carry binary counter. The counter incorporates input pulse shaping, buffering on the outputs of all 12 stages, and reset capabilities. A "high" on the reset input returns the counter to the "zero" state. The counter increments on the negative going input transition.

Logic Diagrams



Connection Diagram





■ R = HIGH DOMINATES (RESETS ALL SIZES)
▲ ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4040A-2	-55°C to +125°C
	HD-4040A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

D.C.

		HD-4040A-2											
		-55°C			+25°C			+125°C					
PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		
Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9
Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
High Level Output Voltage	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	
N-Channel Output Drive Current	I_{DN}	0.22 0.44			0.18 0.36	0.36 0.75		0.125 0.250			mA mA	5 10	V_O = 0.5 V_O = 0.5
P-Channel Output Drive Current	I_{DP}	-0.15 -0.3			-0.125 -0.25	-0.25 -0.5		-0.085 -0.175			mA mA	5 10	V_O = 4.5 V_O = 9.5
Quiescent Device Current	I_L			15 25		0.5 1	15 25			900 1500	µA µA	5 10	
Quiescent Device Dissipation/Package	P_D			75 250		2.5 10	75 250			4500 15000	µW µW	5 10	

		HD-4040A-9											
		-40°C			+25°C			+85°C					
PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		Any Input
Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.8 V_O = 1
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 4.2 V_O = 9
Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
High Level Output Voltage	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	
N-Channel Output Drive Current (Q, $\overline{Q}$ Outputs)	I_{DN}	0.21 0.42			0.18 0.36	0.36 0.75		0.15 0.3			mA mA	5 10	V_O = 0.5 V_O = 0.5
P-Channel Output Drive Current (Q, $\overline{Q}$ Outputs)	I_{DP}	-0.145 -0.29			-0.125 -0.25	-0.25 -0.5		-0.1 -0.2			mA mA	5 10	V_O = 4.5 V_O = 9.5
Quiescent Device Current	I_L			50 100		1 2	50 100			700 1400	µA µA	5 10	
Quiescent Device Dissipation/Package	P_D			250 1000		5 20	250 1000			3500 14000	µW µW	5 10	

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETERS	SYMBOL	HD-4040A-2 MIN.	HD-4040A-2 TYP.	HD-4040A-2 MAX.	HD-4040A-9 MIN.	HD-4040A-9 TYP.	HD-4040A-9 MAX.	UNITS	V_{DD}	
INPUT PULSE OPERATION										
Propagation Delay Time	t_{PHL}, t_{PLH}		450 225	900 450		450 225	950 475	ns ns	5 10	
Transition Time	t_{THL}, t_{TLH}		150 75	300 150		150 75	350 175	ns ns	5 10	
Min. Input Pulse Width	t_{WL}, t_{WH}		200 75	400 110		200 75	500 125	ns ns	5 10	f = 100kHz
Input Pulse Rise & Fall Time	t_{rO}, t_{fO}			15 7.5			15 7.5	s s	5 10	
Max. Input Pulse Frequency	f_O	1 3.5	1.75 5		0.9 3.25	1.75 5		MHz MHz	5 10	
Input Capacitance	C_I		5			5		pF		Any input
RESET OPERATION										
Propagation Delay Time	t_{PHL}		500 250	1000 500		500 250	1250 600	ns ns	5 10	
Minimum Reset Pulse Width	t_{WH}		500 250	1000 500		500 250	1250 600	ns ns	5 10	

NOTES:
1. Measured from the 50% level of the negative clock edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.
2. Maximum input rise or fall time for functional operation.
3. Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12).

HD-4042A

Quad Clocked "D" Latch

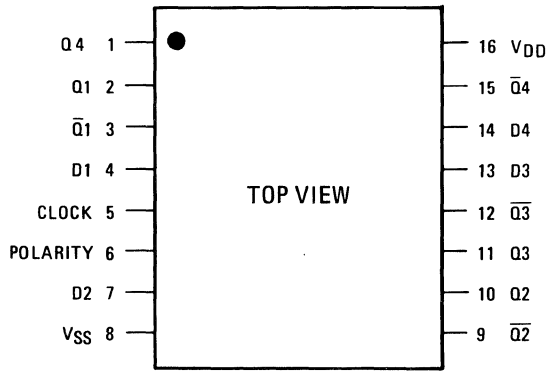
Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/LOW QUIESCENT POWER DISSIPATION
- CLOCK POLARITY CONTROL
- COMPLEMENTARY OUTPUTS
- LOW POWER TTL COMPATIBLE

Description

The HD-4042 is a Quad Clocked "D" latch featuring clock polarity control and buffered complementary outputs. The clock polarity control input is used to select the clock level which transfers information present at the data inputs into the latches. For a "low" on the polarity input, data is transfered when the clock is "low". When the polarity input is "high", data transfers when clock is "high". The latch contents will follow the data input if the proper enabling clock level is present.

Connections Diagrams



Package

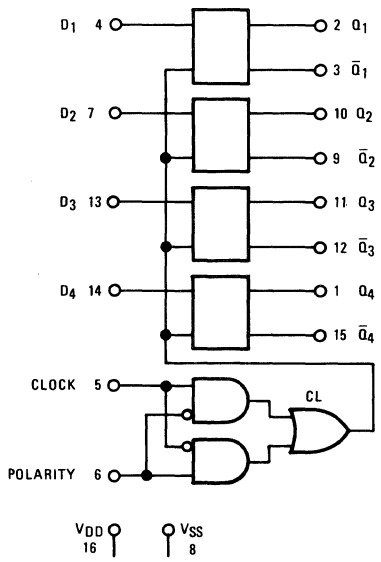
See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

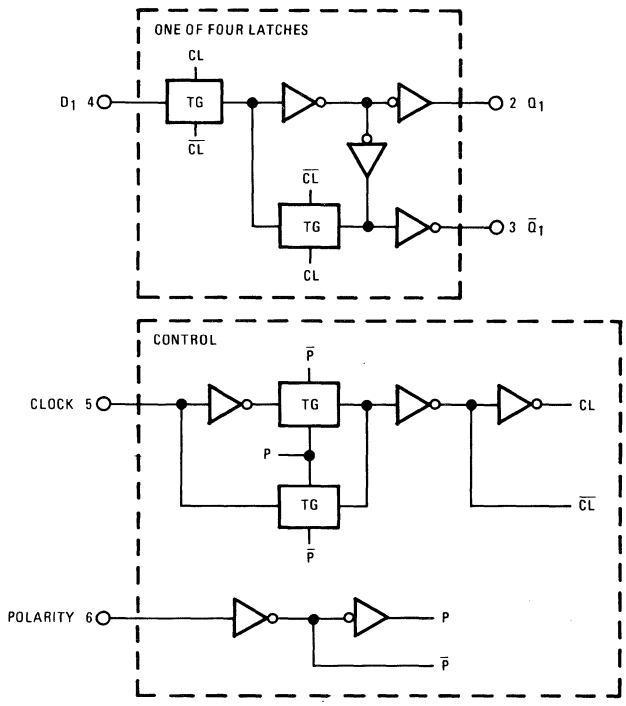
See package outline Code 1W and Code 9L.

Truth Table

CLOCK	POLARITY	Q
0	0	D
⌐	0	LATCH
1	1	D
⌙	1	LATCH

Circuit Diagrams





ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4042A-2	-55°C to +125°C
	HD-4042A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

		HD-4042A-2											
		-55°C			+25°C			+125°C					
PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		Any Input
Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.95 V_O = 2.9V
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 3.6 V_O = 7.2
Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	
N-Channel Output Drive Current	I_{DN}	0.5 1.25			0.4 1	1 2		0.27 0.7			mA mA	5 10	V_O = 0.5V V_O = 0.5V
P-Channel	I_{DP}	-0.45 -1.15			-0.35 -0.9	-1 -1		-0.25 -0.6			mA mA	5 10	V_O = 4.5 V_O = 9.5
Quiescent Device Current	I_L			1 2		0.005 0.005	1 2			60 120	μA μA	5 10	
Quiescent Device Dissipation/Package	P_D			5 20		0.025 0.05	5 20			300 1200	μW μW	5 10	

		HD-4042A-9											
		-40°C			+25°C			+85°C					
PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		Any Input
Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.95 V_O = 2.9
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 3.6 V_O = 7.2
Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	
N-Channel Output Drive Current	I_{DN}	0.24 0.6			0.2 0.5	1 2		0.18 0.45			mA mA	5 10	V_O = 0.5 V_O = 0.5V
P-Channel	I_{DP}	-0.2 -0.34			-0.175 -0.45	-1 -2		-0.15 -0.4			mA mA	5 10	V_O = 4.5 V_O = 9.5
Quiescent Device Current	I_L			10 20		0.01 0.02	10 20			140 280	μA μA	5 10	
Quiescent Device Dissipation/Package	P_D			50 200		0.05 0.2	50 200			700 2800	μW μW	5 10	

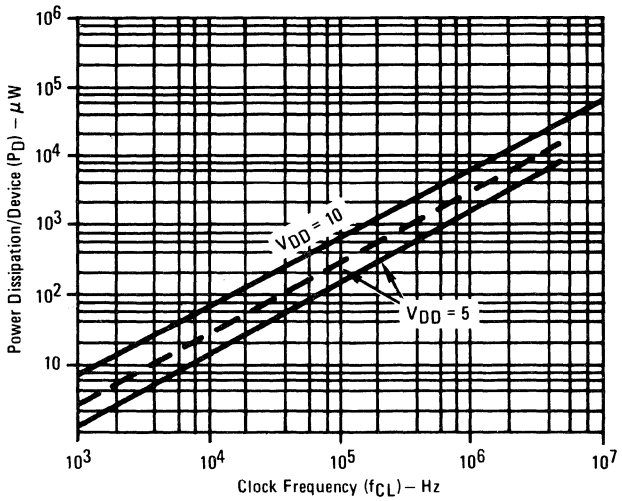
Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^0C$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	HD-4042A-2 MIN.	HD-4042A-2 TYP.	HD-4042A-2 MAX.	HD-4042A-9 MIN.	HD-4042A-9 TYP.	HD-4042A-9 MAX.	UNITS	V_{DD}
Propagation Delay Time	t_{PHL}, t_{PLH}		150 75	300 125		150 75	400 200	ns ns	5 10
Transition Time	t_{THL}, t_{TLH}		100 50	200 100		100 50	300 150	ns ns	5 10
Minimum Clock Pulse Width	t_{WL}, t_{WH}		175 50	250 75		175 50	350 175	ns ns	5 10
Clcok Rise & Fall Time	t_rCL, t_fCL			15 5			15 5	μs μs	5 10
Set Up Time			50 25	100 50		50 25	125 60	ns ns	5 10
Input Capacitance	C_I		5			5		pF	

Typical Characteristics



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-4043A
HD-4044A

Quad Three-State R/S Latches

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER DISSIPATION
- THREE STATE OUTPUTS
- INDIVIDUAL SET AND RESET INPUTS FOR EACH LATCH
- COMPATIBLE WITH LOW POWER TTL
- NOR GATE AND NAND GATE LATCHES FOR DESIGN FLEXIBILITY.

Description

The HD-4043 and HD-4044 types are respectively Quad Cross-Coupled Three State NOR Latches and Quad Cross-Coupled Three State NAND Latches featuring separate set and reset inputs for each latch, and a common enable input.

Application of a "high" to the enable input allows the latch "Q" outputs to propagate to their respective output pins. A "low" on the enable input results in a high impedance between the latch "Q" outputs and the output pins.

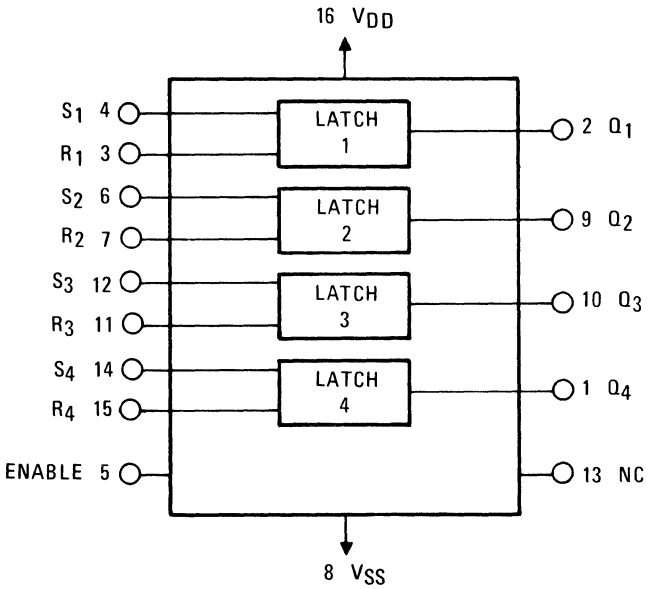
Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

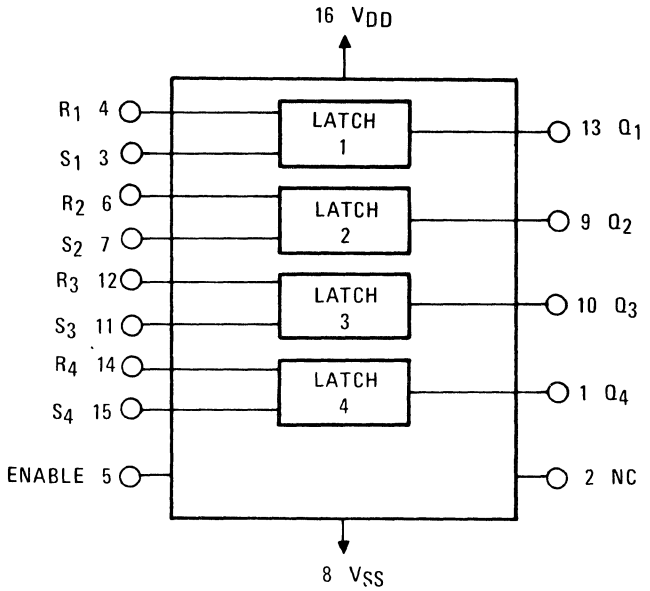
See package outline Code 1W and Code 9L.

Connection Diagrams

HD-4043 NOR LATCH



HD-4044 NAND LATCH



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD}-V_{SS}		-0.5VDC to +15VDC
Voltage at any Pin		V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range		-65°C to +150°C
Power Dissipation per Package		200mW
Operating Temperature Range:	HD-4043A-2 / HD-4044A-2	-55°C to +125°C
	HD-4043A-9 / HD-4044A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

		HD-4043A-2 / HD-4044A-2											
		-55°C			+25°C			+125°C					
PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		Any Input
Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.95 V_O = 2.9
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 3.6 V_O = 7.2
N-Channel Output Drive Current	I_{DN}	0.25 0.61			0.2 0.5	0.5 1		0.14 0.35			mA mA	5 10	V_O = 0.5V V_O = 0.5
P-Channel	I_{DP}	-0.22 -0.5			-0.175 -0.4	-0.5 -1		-0.12 -0.28			mA mA	5 10	V_O = 4.5 V_O = 9.5
Quiescent Device Current	I_L			1 2		0.005 0.005	1 2			60 120	µA µA	5 10	
Quiescent Device Dissipation/Package	P_D			5 20		0.025 0.05	5 20			300 1200	µW µW	5 10	
Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

		HD-4043A-9 / HD-4044A-9											
		-40°C			+25°C			+85°C					
PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{DD}	NOTES
Input Leakage	I_I					10					pA		
Noise Immunity (All Inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_O = 0.95 V_O = 2.9
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V V	5 10	V_O = 3.6 V_O = 7.2
N-Channel Output Drive Current	I_{DN}	0.12 0.3			0.1 0.25	0.5 1		0.09 0.22			mA mA	5 10	V_O = 0.5 V_O = 0.5
P-Channel	I_{DP}	-0.11 -0.24			-0.09 -0.2	-0.5 -1		-0.08 -0.18			mA mA	5 10	V_O = 4.5 V_O = 9.5
Quiescent Device Current	I_L			10 20		0.01 0.02	10 20			140 280	µA µA	5 10	
Quiescent Device Dissipation/Package	P_D			50 200		0.05 0.2	50 200			700 2800	µW µW	5 10	
Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
High Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	

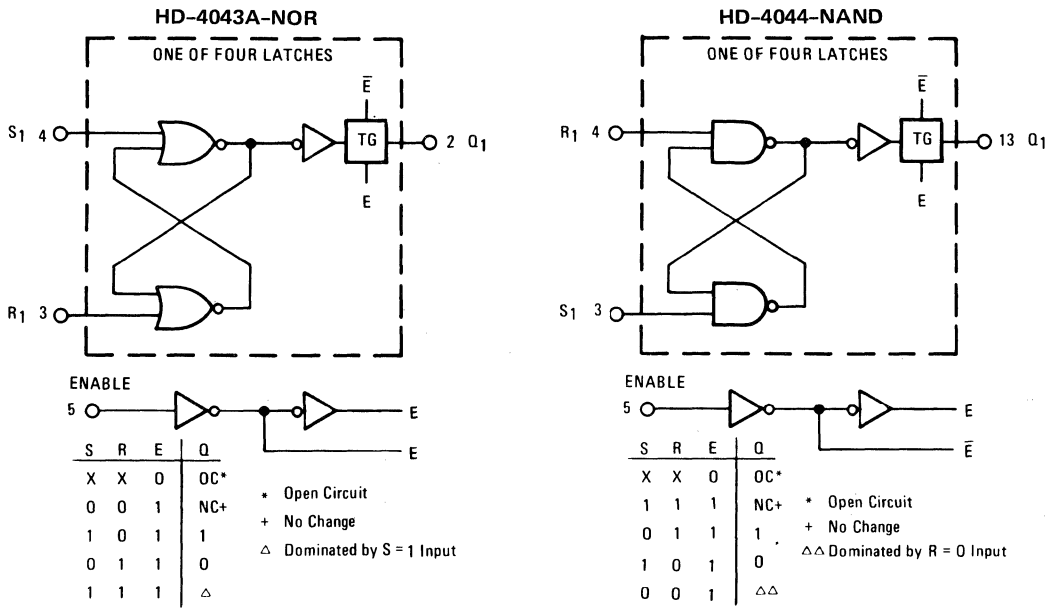
Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

PARAMETER	SYMBOL	HD-4043A-2 HD-4044A-2 MIN.	TYP.	MAX.	HD-4043A-9 HD-4044A-9 MIN.	TYP.	MAX.	UNITS	V_{DD}
Propagation Delay Time	t_{PHL}, t_{PLH}		175 75	350 175		175 75	400 200	ns ns	5 10
Transition Time	t_{THL}, t_{TLH}		100 50	200 100		100 50	250 125	ns ns	5 10
Minimum Set and Reset Pulse Width	$t_{WH(S)}$, $t_{WH(R)}$		80 40	200 100		80 40	225 110	ns ns	5 10
Input Capacitance	C_I		5			5		pF	

Logic Diagram



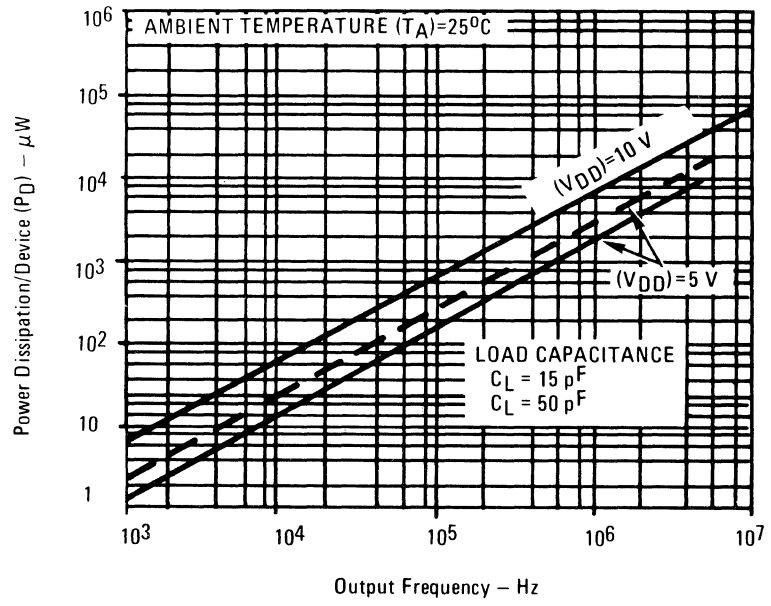
S	R	E	Q
X	X	0	OC*
0	0	1	NC+
1	0	1	1
0	1	1	0
1	1	1	△

* Open Circuit
\+ No Change
△ Dominated by S = 1 Input

S	R	E	Q
X	X	0	OC*
1	1	1	NC+
0	1	1	1
1	0	1	0
0	0	1	△△

* Open Circuit
\+ No Change
△△ Dominated by R = 0 Input

Typical Characteristics



HD-4049A
HD-4050A

Hex Buffer/Converters

Features

- CMOS TECHNOLOGY FOR HIGH NOISE IMMUNITY/ LOW QUIESCENT POWER
- DRIVE CAPABILITY FOR 2 TTL LOADS @ V_{CC} = 5V
- SINGLE POWER SUPPLY OPERATION
- DIRECT PLUG IN REPLACEMENT OF THE 4009 AND 4010

Description

The HD-4049 and HD-4050 are inverting and non-inverting hex buffer/level shifters. These devices perform the level shifting function utilizing a single supply voltage, V_{CC}. When level shifting, the V_{SS} logic "zero" level must be common to both input and output. The logic "one" level of the output equals V_{CC}. V_{IH} (logic one input) must be greater than or equal to V_{CC}. Table I illustrates power supply, input, and output voltage ranges for buffer and level shifting functions.

The HD-4049/HD-4050 are pin-for-pin replacements for HD-4009/HD-4010 functions, offering the advantage of single supply operation. Pin 16 of the HD-4009/HD-4010 is the V_{DD} supply. This pin on the HD-4049/HD-4050 is not internally connected, allowing direct plug in replacement with no effect on circuit operation.

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

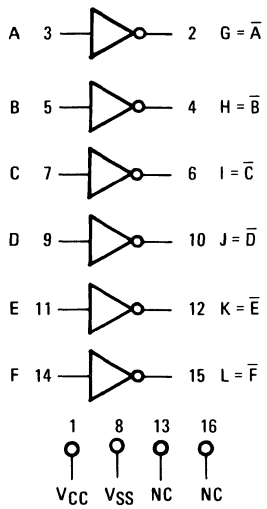
See package outline Code 1W and Code 9L.

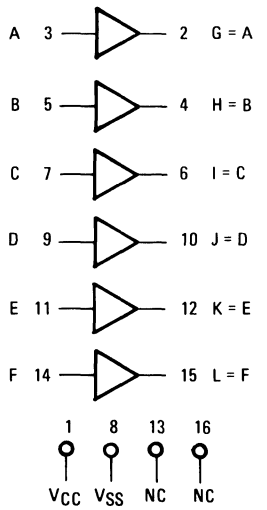
Operating Voltages

FUNCTION	CMOS VOLTAGE RANGE (INPUT)	DTL/TTL VOLTAGE RANGE (OUTPUT)	POWER SUPPLY VOLTAGE RANGE (V_{CC})
Hex Level Shifter	3 - 15V	3 - 6V	3 - 6V
Hex Inverter Hex Buffer	3 - 15V	3 - 15V	3 - 15V

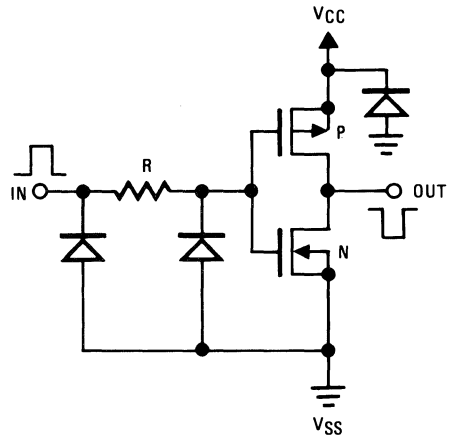
TABLE I

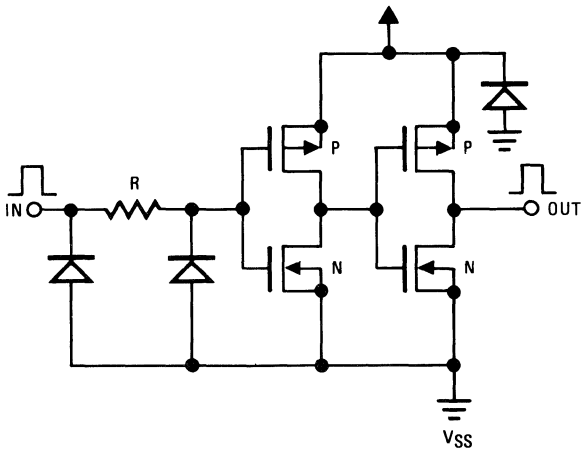
Functional Diagrams





Circuit Diagram





Specifications

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}	-0.5VDC to +15VDC
Voltage at any Pin	V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range	-65°C to +150°C
Power Dissipation Per Package	200mW
Operating Temperature: HD-4049A-2 / HD-4050A-2	-55°C to +125°C
HD-4049A-9 / HD-4050A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS (STATIC)

			HD-4049A-2 / HD-4050A-2											
			-55°C			+25°C			+125°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{CC}	NOTES
	Input Leakage	I_I					10					pA		$V_{IH} = V_{CC}$
	Noise Immunity (All Inputs)													
	HD-4049A-2	V_{NL}	1 2			1 2	2.25 4.5		0.9 1.9			V V	5 10	V_{OH} = 3.6V V_{OH} = 7.2V
	HD-4050A-2	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_{OL} = 0.95V V_{OL} = 2.9V
	HD-4050A-2	V_{NH}	2.9 1.4			3 1.5	4.5 2.25		3 1.5			V V	10 5	V_{OH} = 7.2V V_{OH} = 3.6V
	HD-4049A-2	V_{NH}	2.9 1.4			3 1.5	4.5 2.25		3 1.5			V V	10 5	V_{OL} = 2.9V V_{OL} = 0.95V
D.C.	Low Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
D.C.	High Level Output Voltage	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	
D.C.	N-Channel Output Drive Current	I_{DN}	3.3 3.75 10			2.6 3.0 8	5.2 6 16		1.8 2.1 5.6			mA mA mA	4.5 5 10	V_O = 0.4 V_O = 0.4 V_O = 0.5
D.C.	P-Channel Output Drive Current	I_{DP}	-0.62 -1.85 -1.85			-0.5 -1.25 -1.25	-1 -2.5 -2.5		-0.35 -0.9 -0.9			mA mA mA	5 5 10	V_O = 4.5 V_O = 2.5 V_O = 9.5
D.C.	Quiescent Device Current	I_L			0.3 0.5		0.01 0.01	0.3 0.5			20 30	μA μA	5 10	$V_{IH} = V_{CC}$ $V_{IH} = V_{CC}$
D.C.	Quiescent Device Dissipation/Package	P_D			1.5 5		0.05 0.1	1.5 5			100 300	μW μW	5 10	$V_{IH} = V_{CC}$ $V_{IH} = V_{CC}$

			HD-4049A-9 / HD-4050A-9											
			-40°C			+25°C			+85°C					
	PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{CC}	NOTES
	Input Leakage	I_I					10					pA		$V_{IH} = V_{CC}$
	Noise Immunity (All Inputs)													
	HD-4049A-9	V_{NL}	1 2			1 2	2.25 4.5		0.9 1.9			V V	5 10	V_{OH} = 3.6V V_{OH} = 7.2V
	HD-4050A-9	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V V	5 10	V_{OL} = 0.95V V_{OL} = 2.9V
	HD-4050A-9	V_{NH}	2.9 1.4			3 1.5	4.5 2.25		3 1.5			V V	10 5	V_{OH} = 7.2V V_{OH} = 3.6V
	HD-4049A-9	V_{NH}	2.9 1.4			3 1.5	4.5 2.25		3 1.5			V V	10 5	V_{OL} = 2.9V V_{OL} = 0.95V
D.C.	Low-Level Output Voltage	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V V	5 10	
D.C.	High Level Output Voltage	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V V	5 10	
D.C.	N-Channel Output Drive Current	I_{DN}	3.1 3.6 9.6			2.6 3 8	5.2 6.0 16		2.1 2.5 6.6			mA mA mA	4.5 5 10	V_O = 0.4 V_O = 0.4 V_O = 0.5
D.C.	P-Channel Output Drive Current	I_{DP}	-0.6 -1.5 -1.5			-0.5 -1.25 -1.25	-1 -2.5 -2.5		-0.4 -1 -1			mA mA mA	5 5 10	V_O = 4.5 V_O = 2.5 V_O = 9.5
D.C.	Quiescent Device Current	I_L			3 5		0.03 0.05	3 5			42 70	μA μA	5 10	$V_{IH} = V_{CC}$ $V_{IH} = V_{CC}$
D.C.	Quiescent Device Dissipation/Package	P_D			15 50		0.15 0.5	15 50			210 700	μW μW	5 10	$V_{IH} = V_{CC}$ $V_{IH} = V_{CC}$

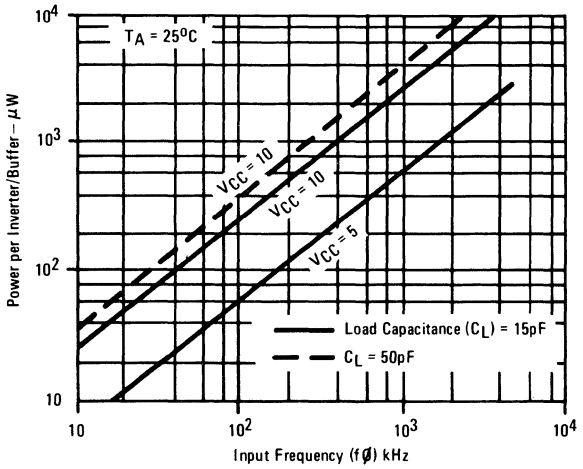
Specifications (continued)

ELECTRICAL CHARACTERISTICS (DYNAMIC)

$T_A = 25^oC$, $C_L = 15pF$, Input Rise and Fall Times = 20ns unless otherwise specified.

	PARAMETER	SYMBOL	HD-4049A-9 HD-4050A-9 MIN.	TYP.	MAX.	HD-4049A-9 HD-4050A-9 MIN.	TYP.	MAX.	UNITS	V_{CC}	NOTES
A.C.	High to Low Level Propagation Delay Time	t_{PHL}		15	55		55	110	ns	5	$V_{IH} = V_{CC}$
				10	30		25	55	ns	10	$V_{IH} = V_{CC}$
	Low to High Level Propagation Delay Time	t_{PLH}		50	80		75	140	ns	5	$V_{IH} = V_{CC}$
				25	55		35	85	ns	10	$V_{IH} = V_{CC}$
	High to Low Level Transition Time	t_{THL}		20	45		20	45	ns	5	$V_{IH} = V_{CC}$
				16	40		16	40	ns	10	$V_{IH} = V_{CC}$
	Low to High Level Transition Time	t_{TLH}		50	100		50	100	ns	5	$V_{IH} = V_{CC}$
				30	60		30	60	ns	10	$V_{IH} = V_{CC}$
	Input Capacitance (Any Input)										
	HD-4049A			15			15		pF		
	HD-4050A			5			5		pF		

Typical Characteristics



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-4066A

Quad Bilateral Switch

Features

- A WIDE RANGE OF OPERATING VOLTAGES FOR BOTH DIGITAL AND ANALOG APPLICATIONS
- BODY CONTROL IS EMPLOYED IN THE TRANSMISSION GATE SWITCHES IN ORDER TO MINIMIZE IMPEDANCE VARIATIONS OVER THE SIGNAL INPUT RANGE
- VARIATION IN IMPEDANCE FROM SWITCH TO SWITCH IN ONE PACKAGE IS LESS THAN 5Ω TYPICAL
- CONTROL INPUT IMPEDANCE – 10^{12} Ω TYPICAL

Package

See CMOS Packaging Section 5 for complete package information. This device is available in Ceramic Dual In-Line and Flat Packs.

See package outline Code 1U and Code 9V.

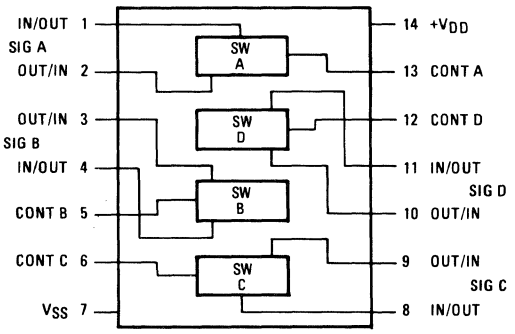
Description

The HD-4066 consists of four independent bilateral switches implemented with CMOS transmission gates.

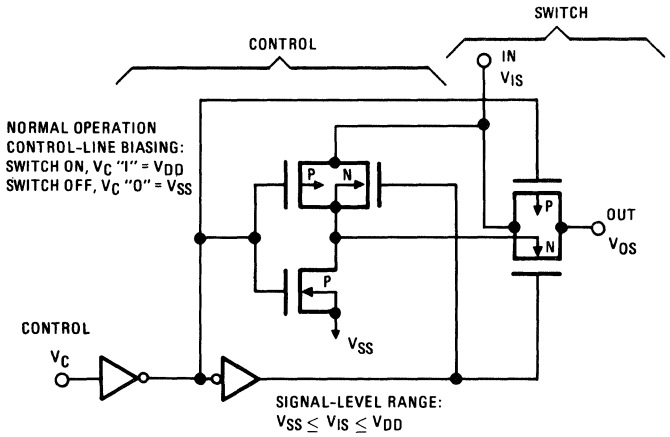
Each switch exhibits a low impedance between input and output terminals when its respective control input is "high". A "low" on the control input turns off the CMOS transmission gate yielding a high impedance between input/output terminals.

Pin-for-pin compatibility with the HD-4016 is maintained while incorporating improvements in circuit performance. Control inputs of the 4066 are fully buffered, resulting in improved noise immunity characteristics. For the HD-4066, "On" resistance is lower and more constant over the input signal range. Improved impedance characteristics result from control of the body voltage of the N-Channel transmission gate transistor. When the switch is "On", the body material is tied to the input, allowing the body voltage to track the input voltage. This improves control of the N-Channel threshold, reducing impedance variation in the switch. When the switch is "Off", the body material is tied to V_{SS}.

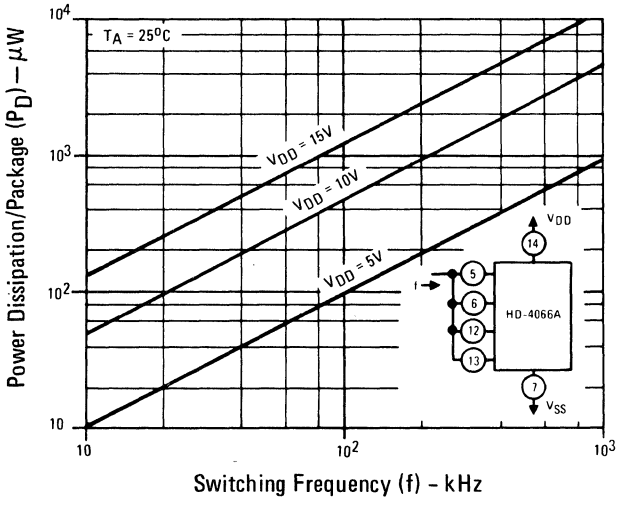
Pin Out



Connection Diagrams



Typical Characteristics



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$	-0.5VDC to +15VDC
Voltage at any Pin	V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range	-65°C to +150°C
Power Dissipation Per Package	200mW
Operating Temperature Range: HD-4066A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

		HD-4066A-2										
		-55°C			+25°C			+125°C				
PARAMETER	SYM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	NOTES
Quiescent Dissipation/ Package All Switches OFF	P_T			5		0.1	5			300	µW	Terminals / Volts Applied: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 GND; V_{IS} 1, 4, 8, 11 ≤+10; V_{OS} 2, 3, 9, 10 ≤+10
All Switches ON	P_T			5		0.1	5			300	µW	Terminals / Volts Applied: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 +10; $V_{IS}=V_{OS}$ 1, 4, 8, 11 ≤+10 (Thru 100Ω)
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})												$V_C = V_{DD}$ / V_{SS} / V_{IS}
ON Resistance	R_{ON}		60	220		80	280		145	320	Ω	+7.5V / -7.5V / -7.5V to +7.5V; +15V / 0V / 0 to +15V
			85	400		120	500		190	550	Ω	+5V / -5V / -5V to +5V; +10V / 0V / 0 to +10V
			160	3000		270	5000		360	5500	Ω	+2.5V / -2.5V / -2.5V to +2.5V; +5V / 0V / 0 to +5V
												R_L = 10KΩ
ΔON Resistance Between Any 2 of 4 Switches	ΔR_{ON}					5					Ω	+7.5V or +15V / -7.5V or 0V / +7.5 to -7.5V or +15 to 0V
						10					Ω	+5V or +10V / -5V or 0V / +5V to -5V or +10V to 0V
												R_L = 10KΩ
Sine Wave Response (Distortion)						0.4					%	+5V / -5V / 5V (p-p) (2); R_L = 10KΩ, f_{is} = 1kHz
Input or Output Leakage-Switch OFF (Effective OFF Resistance)				(1)			(1)			(1)		V_{DD} / $V_C = V_{SS}$ / V_{IS}
				±100		±0.1	±100			±200	nA	+7.5V / -7.5V / ±7.5V
				±100		±0.01	±100			±200	nA	+5V / -5V / ±5V
Frequency Response Switch ON (Sine Wave Input)						40					MHz	$V_C = V_{DD} = +5V, V_{SS} = -5V$; 20 Log 10 $\frac{V_{OS}}{V_{IS}}$ = -3dB; R_L = 1KΩ, V_{IS} = 5V(p-p)
Feedthrough Switch OFF						1.25					MHz	$V_{DD} = +5V, V_C = V_{SS} = -5V$; 20 Log 10 $\frac{V_{OS}}{V_{IS}}$ = -50dB; R_L = 1KΩ, V_{IS} = 5V(p-p)
Crosstalk Between Any 2 of the 4 Switches (freq. at -50dB)						0.9					MHz	$V_{CC}(A) = V_{DD} = +5V$, $V_C(B) = V_{SS} = -5V$; 20 Log 10 $\frac{V_{OS}(B)}{V_{IS}(A)}$ = -50dB; R_L = 1KΩ, $V_{IS}(A)$ = 5V (p-p)
Capacitance Input	C_{IS}					8					pF	$V_{DD} = +5V, V_C = V_{SS} = -5V$
Capacitance Output	C_{OS}					8					pF	$V_{DD} = +5V, V_C = V_{SS} = -5V$
Capacitance Feedthrough	C_{IOS}					0.5					pF	$V_{DD} = +5V, V_C = V_{SS} = -5V$
Propagation Delay Signal Input to Signal Output	t_{pd}					10					ns	$V_C = V_{DD} = +10V, V_{SS}$ = GND, C_L = 15pF; V_{IS} = 10V (Square Wave); $t_r = t_f$ = 20ns (Input Signal)
CONTROL (V_C)												
Noise Immunity	V_{NL}	2			2	4.5		2			V	$V_{DD} - V_{SS}$ = 10V, I_{IS} = 10µA; $V_{IS} \leq V_{DD}$
Input Current	I_C					±10					pA	$V_{DD} - V_{SS}$ = 10V, $V_C \leq V_{DD} - V_{SS}$; $V_{IS} \leq V_{DD}$
Average Input Capacitance	C_C					5					pF	
Crosstalk Control Input to Signal Output						50					mV	R_L = 10KΩ; $V_{DD} - V_{SS}$ = 10V, V_C = 10V (Square Wave), $t_{rc} = t_{fc}$ = 20ns
Propagation Delays	t_{pdC}					35					ns	R_L = 300Ω, $V_{IS} \leq$ 10V, C_L = 15pF
Maximum Allowable Control Input Repetition Rate						10					MHz	V_{DD} = 10V, V_{SS} = GND, R_L = 1KΩ, C_L = 15pF, V_C = 10V (Square Wave), $t_r = t_f$ = 20ns

D.C.

NOTES: 1. Limit determined by minimum feasible leakage measurement for automatic testing.
2. Symmetrical about 0 volts.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}	-0.5VDC to +15VDC
Voltage at any Pin	V_{SS} -0.3VDC $\leq V_{Pin} \leq V_{DD}$ +0.3VDC
Storage Temperature Range	-65°C to +150°C
Power Dissipation Per Package	200mW
Operating Temperature Range: HD-4066A-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	PARAMETER	SYM.	HD-4066A-9 -40°C MIN.	-40°C TYP.	-40°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+85°C MIN.	+85°C TYP.	+85°C MAX.	UNITS	NOTES
	Quiescent Dissipation/ Package All Switches OFF	P_T			50		0.1	50			300	µW	Terminals / Volts Applied: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 GND; V_{IS} 1, 4, 8, 11 ≤+10; V_{OS} 2, 3, 9, 10 ≤+10
	All Switches ON	P_T			50		0.1	50			300	µW	Terminals / Volts Applied: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 + 10; $V_{IS}=V_{OS}$ 1, 4, 8, 11 ≤+10 (Thru 100Ω)
	SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})												
	ON Resistance	R_{ON}		80	250		80	280		130	300	Ω	$V_C = V_{DD}$ +7.5V, V_{SS} -7.5V, V_{IS} -7.5V to +7.5V; R_L = 10KΩ
				100	450		120	500		170	520	Ω	$V_C = V_{DD}$ +15V, V_{SS} 0V, V_{IS} 0 to +15V; R_L = 10KΩ
				190	3500		270	5000		330	5200	Ω	$V_C = V_{DD}$ +5V, V_{SS} -5V, V_{IS} -5V to +5V; R_L = 10KΩ
												Ω	$V_C = V_{DD}$ +10V, V_{SS} 0V, V_{IS} 0 to +10V; R_L = 10KΩ
												Ω	$V_C = V_{DD}$ +2.5V, V_{SS} -2.5V, V_{IS} -2.5V to +2.5V; R_L = 10KΩ
												Ω	$V_C = V_{DD}$ +5V, V_{SS} 0V, V_{IS} 0 to +5V; R_L = 10KΩ
	ΔON Resistance Between Any 2 of 4 Switches	ΔR_{ON}					5					Ω	$V_C = V_{DD}$ +7.5V or +15V, V_{SS} -7.5V or 0V, V_{IS} +7.5 to -7.5V or +15 to 0V; R_L = 10KΩ
							10					Ω	$V_C = V_{DD}$ +5V or +10V, V_{SS} -5V or 0V, V_{IS} +5V to -5V or +10V to 0V; R_L = 10KΩ
	Sine Wave Response (Distortion)						0.4					%	$V_C = V_{DD}$ +5V, V_{SS} -5V, V_{IS} 5V (p-p) (2); R_L = 10KΩ, f_{is} = 1kHz
	Input or Output Leakage-Switch OFF (Effective OFF Resistance)				(1)			(1)					V_{DD} / $V_C = V_{SS}$ / V_{IS}
					±100		±0.1	±100			±200	nA	+7.5V / -7.5V / ±7.5V
					±100		±0.01	±100			±200	nA	+5V / -5V / ±5V
D.C.	Frequency Response Switch ON (Sine Wave Input)						40					MHz	$V_C = V_{DD} = +5V, V_{SS} = -5V$; $20 \text{ Log } \frac{V_{OS}}{V_{IS}} = -3dB$; R_L = 1KΩ, V_{IS} = 5V(p-p)
	Feedthrough Switch OFF						1.25					MHz	$V_{DD} = +5V, V_C = V_{SS} = -5V$; $20 \text{ Log } \frac{V_{OS}}{V_{IS}} = -50dB$; R_L = 1KΩ, V_{IS} = 5V(p-p)
	Crosstalk Between Any 2 of the 4 Switches (freq. at -50dB)						0.9					MHz	$V_{CC}(A) = V_{DD} = +5V$, $V_C(B) = V_{SS} = -5V$; $20 \text{ Log } \frac{V_{OS}(B)}{V_{IS}(A)} = -50dB$; R_L = 1KΩ, $V_{IS}(A)$ = 5V (p-p)
	Capacitance Input	C_{IS}					8					pF	$V_{DD} = +5V, V_C = V_{SS} = -5V$
	Capacitance Output	C_{OS}					8					pF	$V_{DD} = +5V, V_C = V_{SS} = -5V$
	Capacitance Feedthrough	C_{IOS}					0.5					pF	$V_{DD} = +5V, V_C = V_{SS} = -5V$
	Propagation Delay Signal Input to Signal Output	t_{pd}					10					ns	$V_C = V_{DD} = +10V$, V_{SS} = GND, C_L = 15pF; V_{IS} = 10V (Square Wave); $t_r = t_f$ = 20ns (Input Signal)
	CONTROL (V_C) Noise Immunity	V_{NL}	2			2	4.5		2			V	$V_{DD} - V_{SS}$ = 10V, I_{IS} = 10µA; $V_{IS} \leq V_{DD}$
	Input Current	I_C					±10					pA	$V_{DD} - V_{SS}$ = 10V, $V_C \leq V_{DD} - V_{SS}$; $V_{IS} \leq V_{DD}$
	Average Input Capacitance	C_C					5					pF	
	Crosstalk Control Input to Signal Output						50					mV	R_L = 10KΩ; $V_{DD} - V_{SS}$ = 10V, V_C = 10V (Square Wave), $t_{rc} = t_{fc}$ = 20ns
	Propagation Delays	t_{pdC}					35					ns	R_L = 300Ω, $V_{IS} \leq$ 10V, C_L = 15pF; $V_{DD} - V_{SS}$ = 10V, V_C = 10V (Square Wave), $t_{rc} = t_{fc}$ = 20ns
	Maximum Allowable Control Input Repetition Rate						10					MHz	V_{DD} = 10V, V_{SS} = GND, R_L = 1KΩ, C_L = 15pF, V_C = 10V (Square Wave), $t_r = t_f$ = 20ns

NOTES: 1. Limit determined by minimum feasible leakage measurement for automatic testing.
2. Symmetrical about 0 volts.

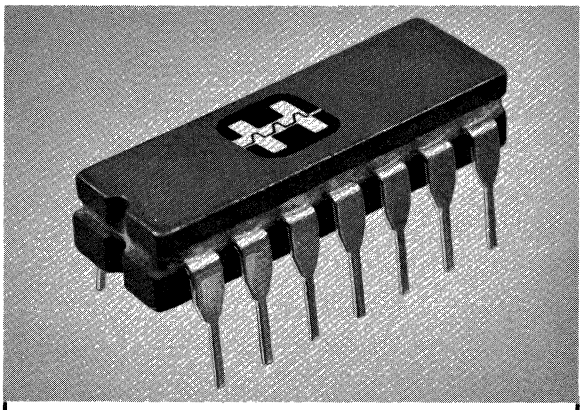
packaging, ordering and literature guide

5

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

CMOS Packaging

CERAMIC



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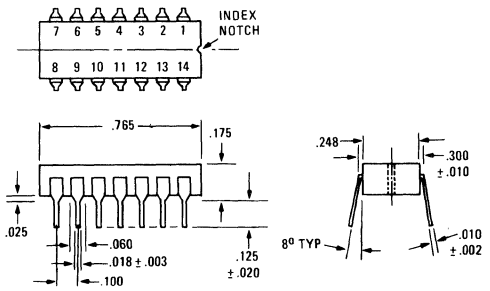

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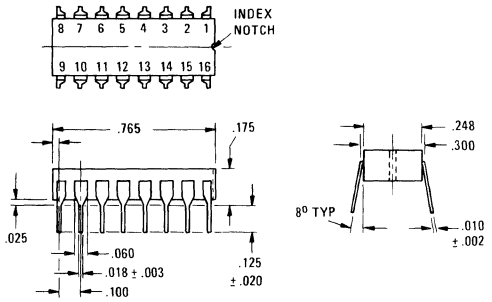

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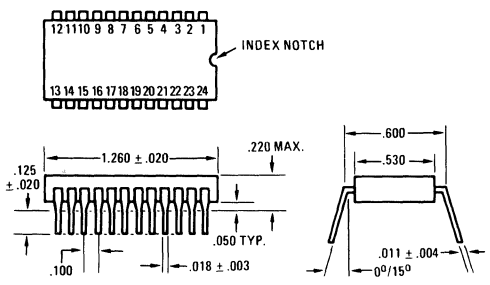
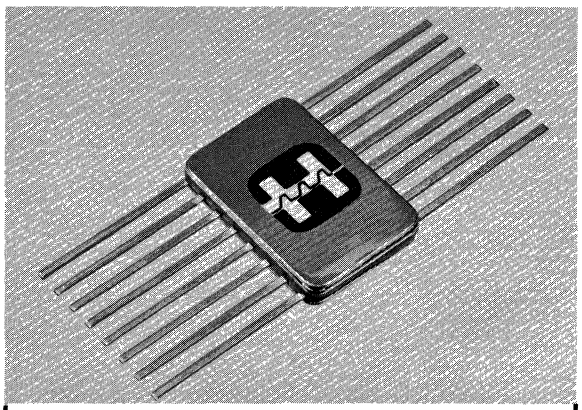


FLAT PACK



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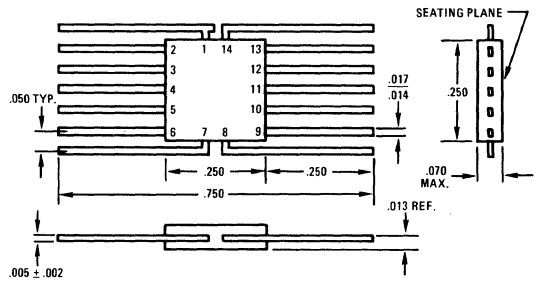

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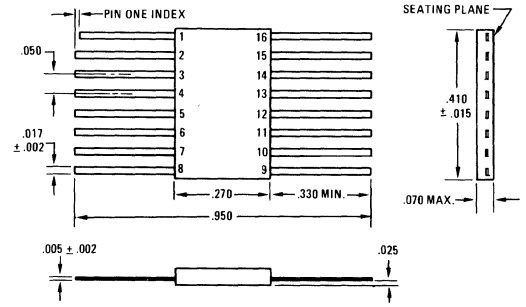
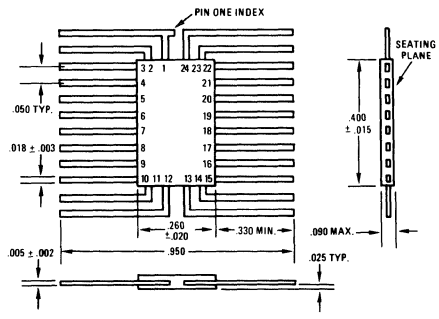


Code 9M 24 LEAD BRAZED SEAL FLAT PACK *



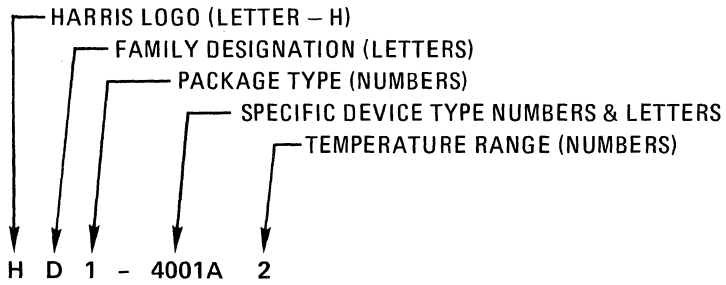
*NOTE: 1. All dimensions in inches.
2. All dimensions ±.010 unless otherwise shown.

CMOS Product Code

Harris CMOS Products are designated by "PRODUCT CODE". When ordering, please refer to products by the full code. Harris Products will always begin with "H". Specific device numbers will always be isolated by hyphens.

4000 SERIES

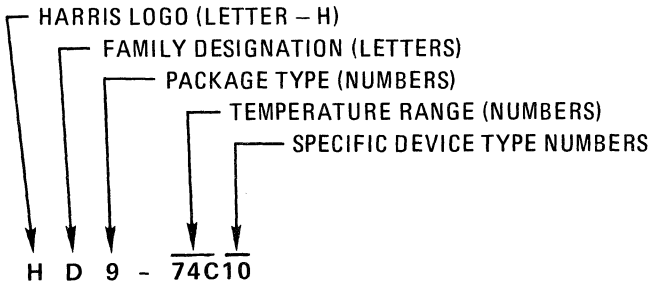
EXAMPLE:



FAMILY (LETTERS)	PACKAGE (NUMBERS)	TEMPERATURE RANGE
D – DIGITAL	1 – DUAL IN-LINE CERAMIC	2 – -55°C to +125°C
	9 – FLAT PACKAGE	9 – -40°C to +85°C

54C/74C SERIES

EXAMPLE:



FAMILY (LETTERS)	PACKAGE (NUMBERS)	TEMPERATURE RANGE
D – DIGITAL	1 – DUAL IN-LINE CERAMIC	54C – -55°C to +125°C
	9 – FLAT PACKAGE	74C – 0°C to +70°C

Harris Product Literature Guide

• *CATALOGS*

INTEGRATED CIRCUITS
CONDENSED FORM (Integrated Circuits Catalog)
HD-54C/74C CMOS

• *DATA SHEETS*

LINEAR

HA-909/911	Operational Amplifiers (See application notes 501,502)
HA-2000/2005/2000A 2005A	F.E.T. Input Preamplifier
HA-2050/2055/2050A 2055A	High Slew Rate F.E.T. Input Op Amp
HA-2060/2065/2060A 2065A	Wide Band F.E.T. Input Op Amp
HA-2111/2211	Precision Voltage Comparator
HA-2311	Precision Voltage Comparator
HA-2400/2404/2405	PRAM, Four Channel Op Amp (See application note 514)
HA-2420/2425	Sample & Hold, Gated Op Amp (See application note 517)
HA-2500/2502/2505	High Slew Rate Op Amp
HA-2510/2512/2515	High Slew Rate Op Amp
HA-2520/2522/2525	High Slew Rate Op Amp
HA-2530/2535	Wide Band High Slew Inverting Amp (See application note 516)
HA-2600/2602/2605	High Impedance Op Amp
HA-2620/2622/2625	Wide Band, High Impedance Op Amp (See application note 509)
HA-2630/2635	High Performance Current Booster
HA-2640/2645	High Voltage Op Amp
HA-2650	Dual High Performance Op Amp
HA-2700/2704/2705	High Performance Op Amp
HA-2720/2725	Current Programmable Op Amp
HA-2730	Dual, Current Programmable Op Amp
HA-2820/2825	Phase Locked Loop (See application notes 601, 602, 605)
HA-2900	Chopper Stabilized Op Amp (See application note 518)
HD-0165	Key Board Encoder (See application note 204)
HD-245 to 249	Line Transmitter Receivers (See application notes 205,207)
HD-1488/1489/1489A	Line Transmitter Receivers (See application note 205)
HI-200	Dual SPST CMOS Analog Switch
HI-201	Quad SPST CMOS Analog Switch
HI-506A/507A	16 Channel Analog Multiplexers
HI-508A/509A	8 Channel Analog Multiplexers
HI-1080/1085	8-Bit, D to A Converter High Speed Monolithic (See application notes 511, 512)
HI-1800A	DPDT CMOS Analog Switch
HI-1818A/1828A	8 Channel Analog Multiplexers

ANALOG SWITCHES

HI-5040	SPST	(75Ω)	HI-5048	Dual DPST	(30Ω)
HI-5041	Dual SPST	(75Ω)	HI-5049	Dual DPST	(30Ω)
HI-5042	SPDT	(75Ω)	HI-5050	SPDT	(30Ω)
HI-5043	Dual SPST	(75Ω)	HI-5051	Dual SPDT	(30Ω)
HI-5044	DPST	(75Ω)			
HI-5045	Dual DPST	(75Ω)			
HI-5046	DPDT	(75Ω)			
HI-5047	4 PST	(75Ω)			

DIGITAL

DIGITAL DATA SHEETS
(REF. SECTIONS 3 & 4 THIS CATALOG)

MEMORY

HD-234/534	Hex Interface Inverters
HD-235/535	Hex Interface Drivers
HD-536	Hex Interface Driver
HD-6600	Quad Power Strobe
HD-6605	Quad Logic Strobe
HMI-0110/0168/0104 0186	Commercial Diode Matrix
MONOLITHIC DIODE MATRICES AND INTERFACE CIRCUITS	
HPROM-8256	256-Bit, Bipolar PROM
HPROM-0512	512-Bit, Bipolar PROM
HPROM-1024/1024A	1024-Bit Field Programmable Bipolar PROM
HM-7200	256 x 1 Static CMOS Random Access Memory
HM-7202	1024 x 1 Static N-Channel RAM
HM-7220	4096 x 1 Dynamic N-Channel RAM
7600 Series	Bipolar Generic PROM Family
HM-7610/7611	256 x 4 Field Programmable Bipolar Generic PROM
HM-7620/7621	512 x 4 Field Programmable Bipolar Generic PROM
HM-7640/7641/7642	1024 x 4 Field Programmable Bipolar Generic PROM
HM-7643/7644	512 x 8 Field Programmable Bipolar Generic PROM

• APPLICATION NOTES

NOTE 202	HPROM-0512 Bipolar PROM
NOTE 203	Programming the HPROM-0512 in an Expanded Configuration
NOTE 204	Designing with the HD-0165 Keyboard Encoder
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NOTE 206	Monolithic Diode Matrices
NOTE 207	Receiver/Transmitter Noise Immunity
NOTE 208	Minimizing Gate Oxide Failures Due to Handling
NOTE 209	CMOS: Some Application Guidelines
NOTE 210	Using Junction Isolated CMOS
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NOTE 504	Automatic Phase Margin Testing
NOTE 505	A High Impedance Hystersis Circuit
NOTE 506	Equivalent Input Noise Measurements on High Gain Monolithic Operational Amplifiers
NOTE 507	A Simple Function Generator Using Operational Amplifiers
NOTE 508	Test Procedures for Operational Amplifiers
NOTE 509	A Simple Comparator Using the HA-2620
NOTE 510	A Simple Square-Triangle Waveform Generator
NOTE 511	Digital to Analog Converter Applications
NOTE 512	Counter Type A to D Converter
NOTE 514	The HA-2400 PRAM, 4 Channel Operational Amplifier
NOTE 515	Operational Amplifier Stability: Input Capacitance Considerations
NOTE 516	The HA-2530/2535 Wideband High Slew Inverting Amplifier
NOTE 517	Applications of a Monolithic Sample-and-Hold/Gated Operational Amplifier
NOTE 518	The HA-2900 Monolithic Chopper Stabilized Amplifier
NOTE 601	Introduction to the Phase Locked Loop
NOTE 602	A General Analysis of the Phase Locked Loop
NOTE 605	The HA-2820/2825 Low Frequency Phase Locked Loops

• CHIP SHEETS

CF-1085	8-Bit D to A Converter Monolithic Chip
CF-1800A	4 Channel CMOS Analog Switch Monolthic Chip
CF-1818A	8 Channel CMOS Analog Multiplexer Monolithic Chip
CF-1828A	8 Channel CMOS Analog Multiplexer Monolithic Chip
CF-2005	F.E.T. Input Preamplifier Monolithic Chip
CF-2405	PRAM™ 4 Channel Programmable Amplifier Monolithic Chip
CF-2425	Sample & Hold Gated Operational Amplifier Monolithic Chip
CF-2505	High Slew Rate Operational Amplifier Monolithic Chip
CF-2515	High Slew Rate Operational Amplifier Monolithic Chip
CF-2525	High Slew Rate Operational Amplifier Monolithic Chip
CF-2535	High Slew Rate, Wide Band Inverting Amplifier Monolithic Chip
CF-2605	High Input Impedance Operational Amplifier Monolithic Chip
CF-2625	Wide Band Operational Amplifier Monolithic Chip
CF-2635	Current Booster
CF-2645	High Voltage Operational Amplifier
CF-2650	Dual High Performance Operational Amplifier
CF-2705	High Performance Operational Amplifier Monolithic Chip
CF-2725	Current Programmable Operational Amplifier
CF-2735	Dual Current Programmable Operational Amplifier
CF-2825	Phase Locked Loop Monolithic Chip
CF-2905	Chopper Stablized Operational Amplifier Monolithic Chip
CF-200	Dual SPST CMOS Analog Switch
CF-201	Quad SPST CMOS Analog Switch
CF-506A	16 Channel Analog Multiplexer with Over Voltage Protection Monolithic Chip
CF-507A	Dual 8 Channel Analog Multiplexer with Over Voltage Protection Monolithic Chip
CF-508A	8 Channel Analog Multiplexer
CF-509A	8 Channel Analog Multiplexer

• SPECIAL LITERATURE

RELIABILITY REPORTS

Issue 3	Low Power Monolithic Op Amp
Issue 6	HA-2500 High Slew Rate Monolithic Op Amp
Issue 7	Complementary MOS Process
Issue 8	Field Programmable Read-Only Memory Devices HPROM-0512, HPROM-1024, HPROM-8256

MEMORY PRODUCTS TECHNICAL DATA BOOKLET
OEM PRICE SCHEDULE (dated May 1974)
NEW LINEAR PRODUCTS BOOKLET
OPERATIONAL AMPLIFIERS GUIDE
TECH BRIEF HM-7620/7621
TECH BRIEF 4096 BIT RAM
TECH BRIEF HM-7220

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